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HEATRING - SMART INVESTIGATION OF TEMPERATURE IMPACT ON INTEGRATED CIRCUIT DEVICES

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ABSTRACT

To investigate the electrical on-chip-transistor behavior at different temperatures usually the transistor area on the wafer is heated by external heat sources to operate at a specific temperature. To avoid using external heat sources a heatring structure was developed which directly controls the temperature of the investigated transistor area on the wafer, guaranteeing very fast warming up and cooling off duration times. Testing the heatring functionality was performed by electro-thermal simulations, the results of which were verified by measurements.
Keywords: heatring, electro-thermal simulation

1. MOTIVATION

For testing the reliability and temperature dependence of semiconductor devices it is necessary to operate these devices at different temperature. One possibility is to use an external heat source such as a thermo-chuck. A smart option is to use a heatring structure. This heatring structure is placed in the wafer around the test region. Electrical power loss in the heatring structure directly heats the small well defined test area. The very big advantage is that the heating process of this small device area has a duration of only a few milliseconds. The thermal stress stays locally limited. The thermal energy produced by the electric current is well tunable. For electrically analyzing a device within the heatring, the temperature profile inside the heatring area should stay constant. Therefore, in this work we investigate the temperature distribution in the heatring area by a given applied voltage and operating time by electro-thermal simulations. For the evaluation of these simulations the simulated temperature results are compared to measured values.

This heatring structure is patent pending.

2. INVESTIGATED STRUCTURE

The structure is implemented in a WLR-monitor (Wafer Level Reliability) or SLM (Scribe Line Monitor). A SLM module is used to validate the manufacturing process. It can consist of simple structures like resistors, capacitors, NMOS and PMOS transistors or even just simple rectangles to validate the lithography process step. A SLM is placed in the scribe line (the scribe line is the “virtual” line where the wafer will be sawed). The SLM contains two heatrings where two different PMOS transistors with different gate width are placed inside (Fig. <1>). The simulation of both heatrings is not necessary, since for both heatrings at the designated temperature the results would be the same. Here, only the temperature distribution over the heatring structure is simulated. The analysis of the electrical properties of the transistors is not the scope of this work and can be performed by a device simulator (Minimos-NT [1] or Dessis [2], for instance).

Fig. <2> shows the experimental heatring structure on the SLM. NDIFF is a high doped n-type area which represents the real heatring. SN is a middle doped n-type area. The test device is placed in the n-well DN, shielded from the former n-doped structures by the p-doped protection ring RP. These structures are embedded in the silicon wafer. Only the metallic supply pad M1 lies above the wafer. However, for the electro-thermal simulation it is sufficient to consider only the conducting heatring and its insulating environment with the corresponding thermal properties.

3. THERMAL SIMULATION AND MEASURED RESULTS OF THE HEATRING SLM

The temperature distribution which occurs directly on the wafer is measured by diodes (Fig. <3>) placed within the heatring. Fig. <4> illustrates the simulated temperature

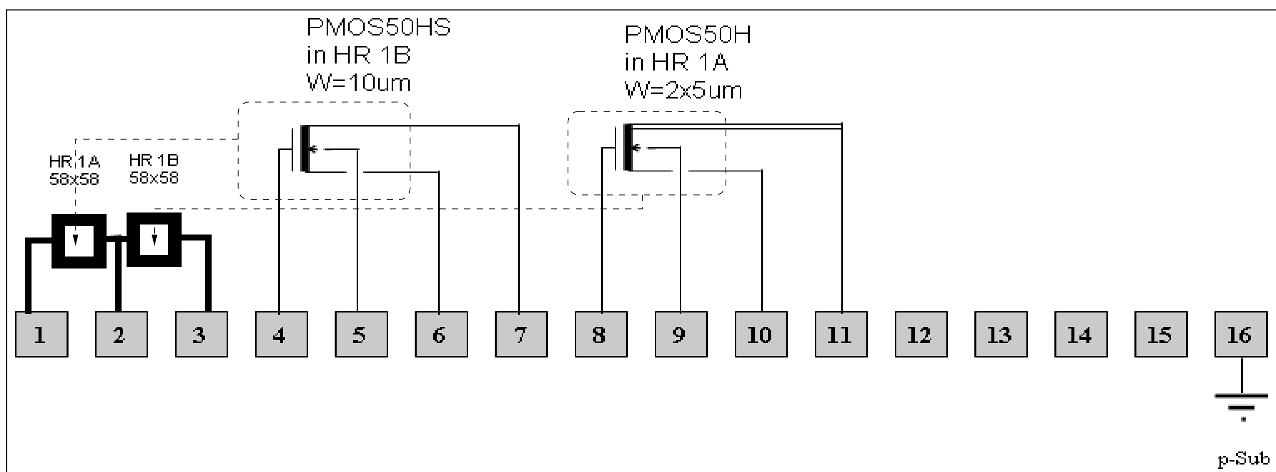

Figure 1: Schematic of the heatring SLM structure

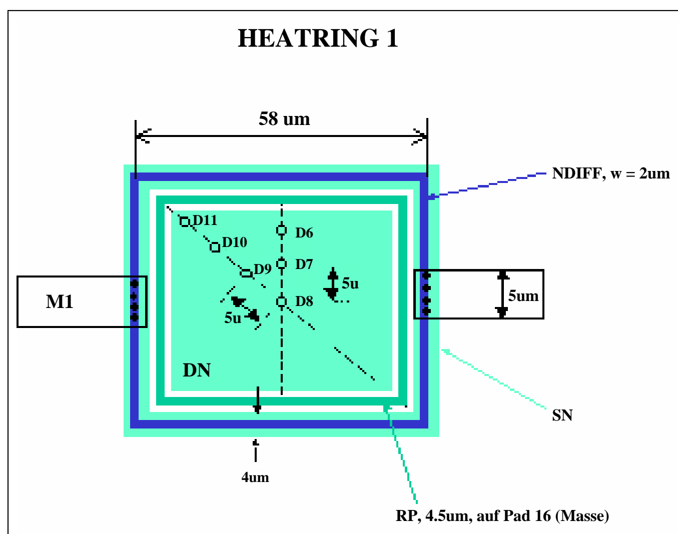

Figure 2: Heatring structure

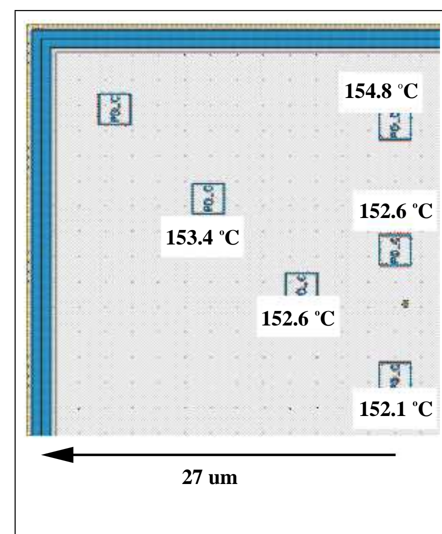

Figure 3: Measured heatring temperature distribution at $90V$

distribution within the heatring structure at $70V$. In this figure the top layer which consists of SiO_2 is removed for visualization purposes. However, in the simulation this oxide layer must not be neglected to take into account the materials around the heatring. The top of the oxide layer is exposed to room temperature (300K), corresponding to thermal Dirichlet boundaries. All remaining outer faces are adiabatic (zero Neumann boundary conditions). For the electrical problem at the outer faces of the simulation area zero Neumann boundary conditions are applied. The electrical Dirichlet boundary conditions are represented by the control voltage applied at the metal pads which are connected by vias to the middle of the left side of the heatring and to the middle of the right side, respectively. The simulation is performed by our in house interconnect simulation software *Smart Analysis Programs* [3]. It is based on the Finite Element Method [4] on tetrahedral grid elements [5]. The rise of the temperature from the center to the heat source is about the same as with the measured result shown in Fig. <3>. Fig. <5> shows the results of the simulated and measured temperature in the center of the heatring structure. Only at higher heatring temperatures the curves are slightly different. At 90V the simulated curve gets more than 160°C. Since the simulated structure is very small compared to a wafer, the temperature distribution is “cut” on the side areas (homogeneous

Neumann boundary conditions). So the heat-flow normal to the surface is stopped and thus the temperature of the whole model region is higher than expected. On the real wafer the heat-flow is not limited close to the heat source. Thus there is enough space for a wider heat spread and the measured curve is almost linear at higher heatring voltages. Enlarging the thermal simulation area overcomes this constraint, however, in this case longer simulation durations have to be accounted for.

4. THEORETICAL BACKGROUND

4.1. Electro-Thermal Simulation

For a coupled electro-thermal simulation the heat conduction system

$$c_p\rho\frac{\partial T}{\partial t} - \vec{\nabla}\cdot(\gamma_T\vec{\nabla}T) = p \qquad (1)$$

has to be considered [6] [7], where the solution of (1) gives the temperature T. The material properties are defined by the thermal conductivity γ_T, by the specific heat c_p, and by the mass density ρ. The source density function p corresponds to the electrical power loss density and is calculated by

$$p = \gamma_E(\vec{\nabla}\varphi)^2. \qquad (2)$$

Finally, the power loss density p in (2) is derived from the the electric potential φ, which is calculated by solving the Euler equation

$$\vec{\nabla}\cdot(\gamma_E\vec{\nabla}\varphi) = 0, \qquad (3)$$

where γ_E denotes the electrical conductivity. The partial differential equations (1), (2) and (3) couple the electrical and the thermal system.

The electrical conductivity and the thermal conductivity of most materials depend on the temperature. Usually the following model is used to describe this dependence:

$$\gamma(T) = \gamma_0\frac{1}{1+\alpha(T-T_0)+\beta(T-T_0)^2}.$$

γ_0 is the (electric/thermal) conductivity at reference temperature T_0 (300K). α and β denote a linear and a quadratic temperature coefficient, respectively.

4.2. Boundary Conditions

The boundary of the simulation area G is divided into two parts for the thermal system (G_{T1} and G_{T2}) and also into two parts for the electrical system (G_{E1} and G_{E2}). The Dirichlet boundary conditions for the thermal part of the system model the heat sinks.

$$T = T_c \quad \text{on } G_{T1}$$

An adiabatic (ideal thermally insulating) boundary is described by homogeneous Neumann boundary conditions

$$\vec{n}\cdot\vec{\nabla}T = 0 \quad \text{on } G_{T2}.$$

The applied electrical contact potentials φ represent Dirichlet boundary conditions for the electric part

$$\varphi = \varphi_c \quad \text{on } G_{E1}.$$

Constant current sources are implemented by Neumann boundary conditions

$$\vec{n}\cdot\vec{\nabla}\varphi = f_c \quad \text{on } G_{E2} \quad \text{with } J_n = \gamma\,\vec{n}\cdot\vec{\nabla}\varphi.$$

4.3. Initial Conditions

For transient thermal problems the condition T_0 for the temperature at initial time $t = 0$ has to be defined

$$\forall\vec{r}\in\mathcal{V},\, t=0:\ T(\vec{r},0) = T_0.$$

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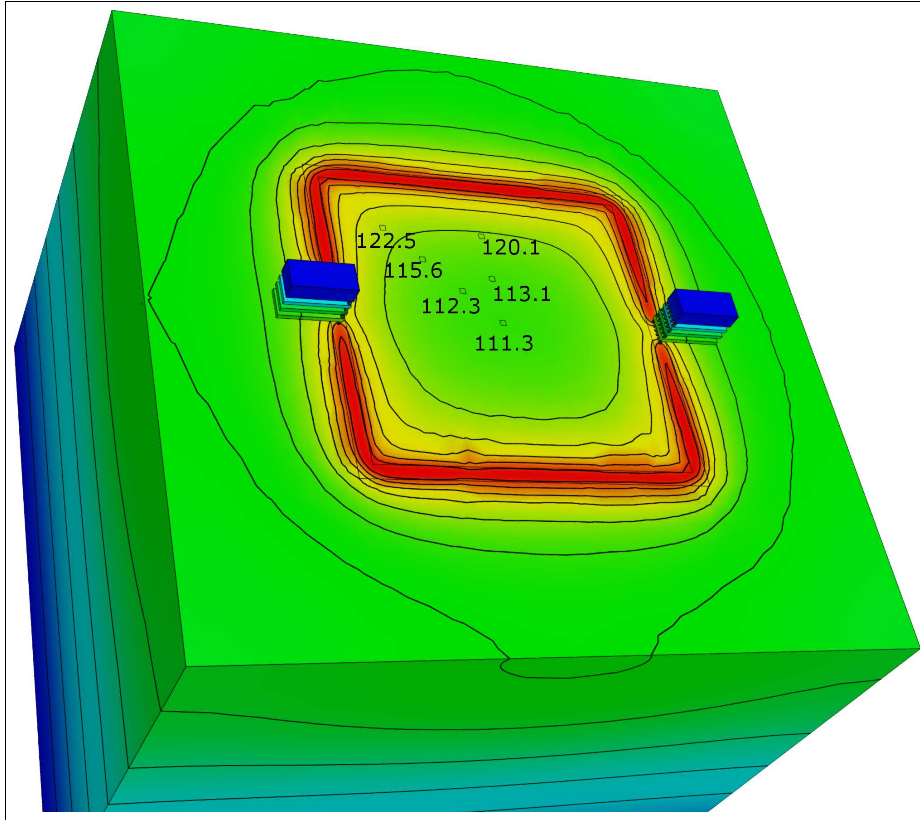

Figure 4: Simulated heatring temperature distribution at $U_{\mathrm{Heatring}} = 70V$

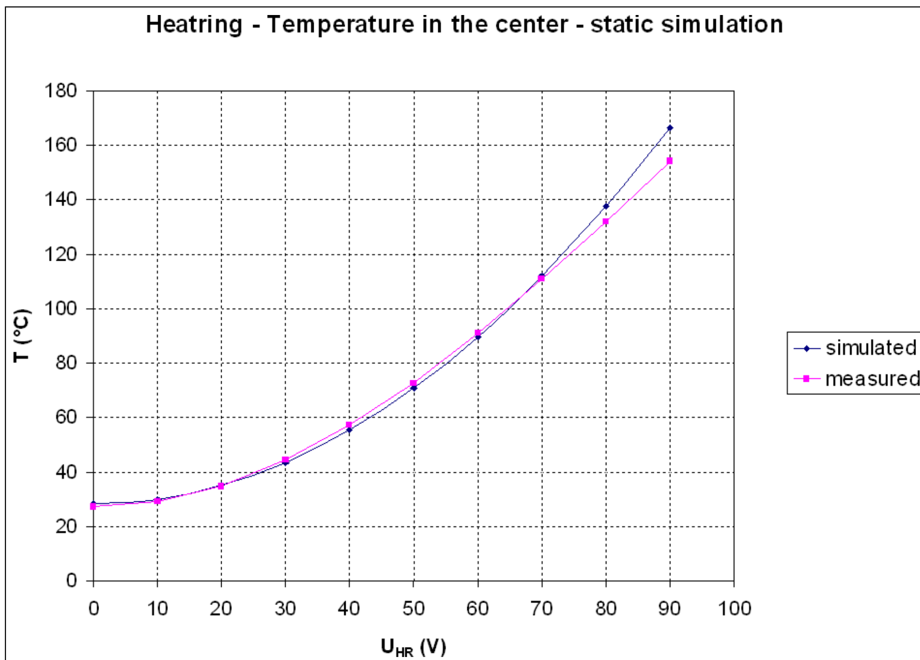

Figure 5: Temperature in the heatring center