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VALIDATION OF THE DJOSER ANALYTICAL THERMAL SIMULATOR FOR ELECTRONIC POWER DEVICES AND ASSEMBLING STRUCTURES

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ABSTRACT

The present communication deals with the tests for the validation of the DJOSER steady-state thermal simulation program, purposely designed for power electronic assembling structures and which is based on the resolution of analytical relationships. The validation experiments were carried out theoretically by comparing the thermal maps with those obtained using standard finite-elements programs and yielding temperature accuracy below 1%. Experimental tests were also performed on purposely built multi-layer structures and industrial circuits with power diodes mounted in naked-chip configuration. The simulated maps were compared with accurate thermo-graphic recordings and showed a good agreement, testifying the validity of the mathematical model.

1. INTRODUCTION

The DJOSER program is a simulation system for the steady-state temperature mapping of thee-dimensional assembling structures of power devices and circuits. Its main features are that it can be applied to pyramidal stacks of layers and it is based on analytical relationships between the temperatures and heat fluxes at the interfaces of the layers.
The analytical approach to the thermal problem generally has some advantages with respect to the conventional FEM analysis. The analytical model can operate with a 2-D rectangular meshing at the interfaces instead of 3-D volumetric meshing. This implies a dramatic decrease of the number of the unknown variables and of the matrices dimensions, therefore leading to a shorter computing time.
Furthermore, all the 2-D interface meshing may be uniform, i.e. composed by square cells with the same area, so that the pre-processing procedure and the model construction can be fully automatic.

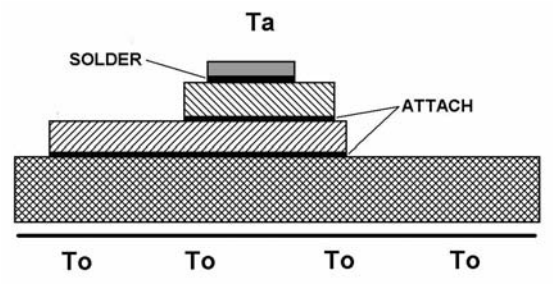

FIG. 1: Pyramidal assembling structure of a power electronic device composed by a stack of homogenous slabs connected with thin soldering or attaching layers. Ta is the environmental temperature. To is the temperature of the bottom heat sink.

Another important feature is that this tool, thanks to its speed and reduced complexity, is particularly suitable as a thermal solver in cyclic electro-thermal simulation programs based on the mutual interaction between the device electrical characteristics and the temperature distributions. A typical situation needing this type of tool is the so-called ‘hot-spot’ phenomenon occurring in high power bipolar transistors [1]. For all these reasons the DJOSER program can be a candidate for replacing conventional, general purpose, expensive and time consuming programs based on the finite elements method (FEM), at least in the simple geometrical configurations exposed in the next section suitable for power electronics.
This communication deals with the validation experiments of the thermal data obtained from the DJOSER program. The tests concerned the temperature mapping comparisons with the results obtained using standard FEM program on some virtual samples. Furthermore some experiments on real structures are also shown in which the temperature maps to be compared with the simulated ones were recorded by means of a thermo-graphic camera. The real samples were both purposely built stack of layers with a heating

resistor on the top and an industrial power circuit manufactured by Mitsuba Europe.

2. THE DJOSER MODEL

In this section the DJOSER analytical method for the steady state thermal mapping, elsewhere more completely exposed [2,3,4], is briefly presented.
Fig. 1 shows a typical assembling structure of a power electronic device which is composed by a stack of homogeneous layers of different materials, similar to a step pyramid, eventually also asymmetric.
The following assumption hold and are taken into account by the model.
a) The slabs composing the structure are rectangular and homogeneous. Their lateral sizes are greater or equal to those of the above layer and are smaller or equal to those of the lower one (see the Fig. 1).
b) The thermal power sources are two dimensional, with any spatial distributions and are located at any interface of the structure. There are two types of sources: those located at the top surface of the layers (p(x,y) in the Fig. 2) and those located at the bottom surfaces (p*(x,y) in the Fig. 2), just above the interface thermal resistances R*. This second kind of source was introduced to allow the simulation of particular mounting configurations of the electronic die, such as flip-chip.
c) Two adjacent layers may be separated by a zero thick contact thermal resistance R* representing the contribution of the thin soldering or attaching layers.
d) Each layer is in contact with the environment through the four lateral surfaces and the top surface not covered by the preceding layer. At those surfaces a heat exchange by convection may occur with different coefficient for each surface.
e) The bottom surface of the lower layer is in contact with a heat sink having known, eventually not uniform, temperature distribution.
If the geometrical configuration and the above defined boundary conditions hold, the steady-state thermal simulations may be performed by means of dedicated mathematical models and explicit analytical relationships [1] which can be implemented in faster and easily programmable simulation tools.
The problem of heat conduction corresponding to the above-defined boundary conditions is the calculation of the temperature and heat flux distributions at all the interfaces between the layers under the steady-state regime.
The resolution of this problem, which is practically an extension and an improvement of other models cited in literature [5,6], is based on the resolution of the single

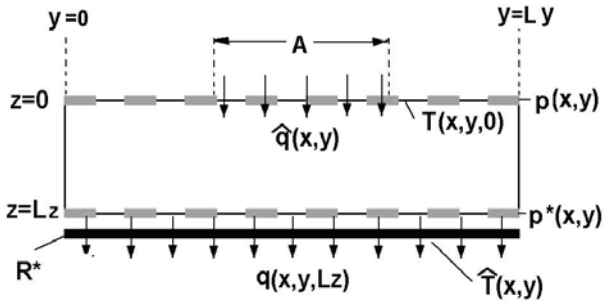

FIG. 2: Schematic cross-section of a single layer showing the known [q^(x,y,0), T^(x,y,Lz), p(x,y), p(x,y,Lz)] and unknown [q(x,y,Lz), T(x,y,0)] thermal functions. T are temperatures, q are heat fluxes, p and p* are power dissipations and R* is a contact thermal resistance.*

homogeneous slab shown in Fig. 2. Here the known thermal functions are the bottom temperature T^(x,y,Lz), the thermal flux q^(x,y,0), entering from the area A of the top surface and the power dissipation densities p(x,y) and p*(x,y) located at the top and bottom surfaces respectively.
The single slab solution can be obtained by means of the variable separations and superposition techniques, so that the upper temperature at z=0 and the heat flux at z=Lz are expressed by the two following integral relationships:

$$T(x,y,0) = \int_0^{L_x}\int_0^{L_y}\left[p(x',y') + \hat{q}(x',y')\right]\cdot G_{11}(x',y' \mid x,y)dx'dy' + \\ + \int_0^{L_x}\int_0^{L_y}\left[R^* p^*(x',y') + \hat{T}(x',y')\right]\cdot G_{12}(x',y' \mid x,y)dx'dy' \quad (2)$$

$$q(x,y,L_z) = \int_0^{L_x}\int_0^{L_y}\left[p(x',y') + \hat{q}(x',y')\right]\cdot G_{21}(x',y' \mid x,y)dx'dy' + \\ + \int_0^{L_x}\int_0^{L_y}\left[R^* p^*(x',y') + \hat{T}(x',y')\right]\cdot G_{22}(x',y' \mid x,y)dx'dy' \quad (3)$$

The spatial functions $G_{ij}(x',y'|x,y)$ are Green functions consisting of double harmonic cosine Fourier series. Using the coordinates system shown in Fig. 2, the G functions are just cosine and may be defined as follows:

$$G_{ij}(x',y' \mid x,y) = \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} C_{ij}(n,m)\cos(\beta_n x')\cos(\mu_m y')\cos(\beta_n x)\cos(\mu_m y) \quad (4)$$

where $C_{ij}(n,m)$ are suitable coefficients and the eigenvalues β_n and , μ_m are given by:

$$\beta_n = n\pi / Lx \ , \ \mu_m = m\pi / Ly \quad \text{with } n \text{ , } m \text{ integer} \quad (5)$$

in the adiabatic case, otherwise they are calculated from the zeros of a transcendent equation containing the top and lateral heat exchange convection coefficients.

TABLE 1 : Numerical data for the virtual sample Q0.

Layer	*k* (W/m°C)	Lx (mm)	Ly (mm)	Lz (μm)
Silicon	135	6.2	4.4	500
Silver	419	9	7	200
Alumina	24	14	10	500
Copper	386	30	24	2000

If we turn back to the case of step pyramid, it is quite evident that for a single slab of the stack the functions q^(x,y,0) e T^(x,y,Lz) are not really known but they are the thermal flux coming from the above layer and the temperature distribution of the contact area with the lower layer respectively. The temperature T^(x,y,Lz) at the bottom of the lowest layer is known and corresponds to the heat sink temperature. Therefore the set of relations (2) and (3) for all the layers are an integral system with 2(Ns-1) equations and where the 2(Ns-1) unknown variables are the functions q^ e T^, Ns being the number of slabs belonging to the whole structure. This is the mathematical core of the DJOSER model.
However the real implementation of the method and the knowledge of the q^ e T^ functions require the use of suitable numerical calculations and approximations. Firstly, the Green functions, given by equation (4), can be evaluated for a finite number of eigenvalues, being *Nnm* the maximum number of the indices n an m used for the calculations of the Fourier series. Secondly, the double integrals in equation (2) and (3) require the use of quadrature formulas and that the heat flux and temperature functions can be known in the form of a grid of sample values. This implies that all the interfaces of the structure must be divided into a regular two-dimensional grid of cells: each flux or temperature numerical value (q^(xi,yj) e T^(xi,yj)) in each layer corresponds or is relative to the centre of a single cell on a given interface defined by the relative coordinates (xi,yj). Therefore, by using the standard quadrature formulas for the double integrals and being *nx(s)* and *ny(s)* the arrays containing the dimensions of the interface cell grids, the system of 2(Ns -1) integral equations can be transformed into a linear system having the following number of M equations and unknown variables:

$$M = \left[2 \cdot \sum_{i=1}^{Ns} nx(i) \cdot ny(i)] \right] - nx(1) \cdot ny(1) - nx(Ns) \cdot ny(Ns) \qquad (6).$$

3. SIMULATIONS OF VIRTUAL SAMPLES

3.1. Structure of virtual samples and thermal maps

The DJOSER analytical simulation program, implemented in MATLAB 5.0, was tested on a purposely-designed multi-layer model representing an almost typical assembling structure of a packaged power electronic integrated chip. The geometrical and thermal conductivity data of the main sample model (Q0) are reported in the Table 1. This structure was designed with a sequence of high and low thermal conducting layers in order to test the effects of the different heat flux spreading capabilities induced by different thermal conductivities.
The first layer is a rectangular silicon die; the top heat generation density (total power 17.4 W) is organized in square islands, each having its own uniform power density. The whole silicon surface was divided into a grid of 31x22 square cells, 0.2 mm wide. The other layers are a thin and narrow silver conductive film, an insulating alumina slab and a wider copper base acting as a heat-spreading sub-mount. All the top and lateral surfaces were supposed to be adiabatic except the bottom one which is in contact with an ideal heat sink whose temperature was set constant to the value of 0 °C. The other models used for the test simulations were obtained by increasing the thickness of the insulator layer (Q1) or inserting a large degree of asymmetry between the layers (Q3). This last geometrical configuration was also used in order to observe the effects on the top temperature distribution of different properties of the lower layers representing the packages or the heat spreaders.
Fig. 3 shows the top dissipating power distribution on the clusters and the structure of the basic axisimmetrical model Q0 and the other samples.
In order to establish a reference for the DJOSER result validation, all the designed models were also simulated using the standard and consolidated finite element method performed using the program MARC and the pre-post-processor MENTAT, both by Mac Neal Schwendler Comp. The FEM simulations were carried out using a very dense 3-D meshing grid, (more than 64000 nodes) in order to avoid as much as possible the temperature and flux calculation error with respect to the reality. As an example, the silicon and the silver layers have been modeled using cubic elements with a side length of 0.1 mm, the half of that used by the analytical simulator DJOSER.

3.2. Thermal simulation results

The results of the temperature mapping performed using the DJOSER program are shown in Fig. 4 for both the temperatures and the heat fluxes at all the interfaces. The temperature maps on the top silicon layer for the samples Q0, Q1 and Q3 are shown in Fig. 5 using the same color scaling.
Furthermore, Fig. 6 shows the comparison among the temperature plots of the three samples along the two cross sections shown in the Q1 map of Fig. 5 and just crossing

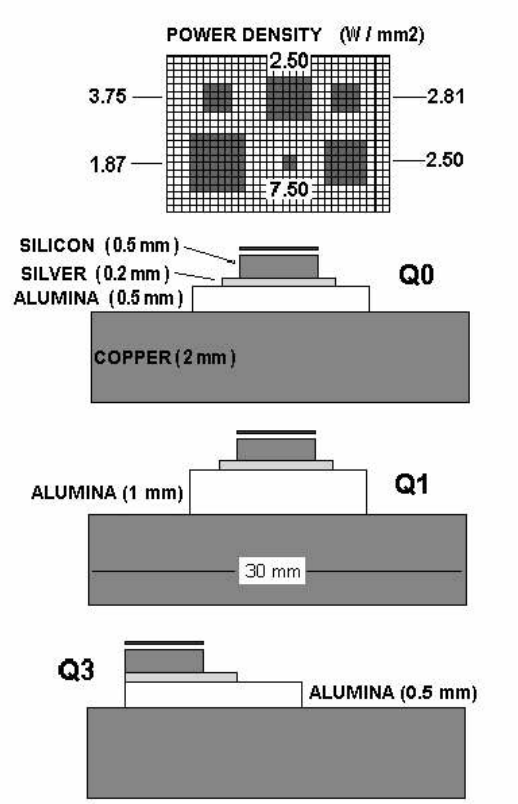

FIG. 3: Surface grid, power distribution (top) and cross-sections of the three virtual samples.

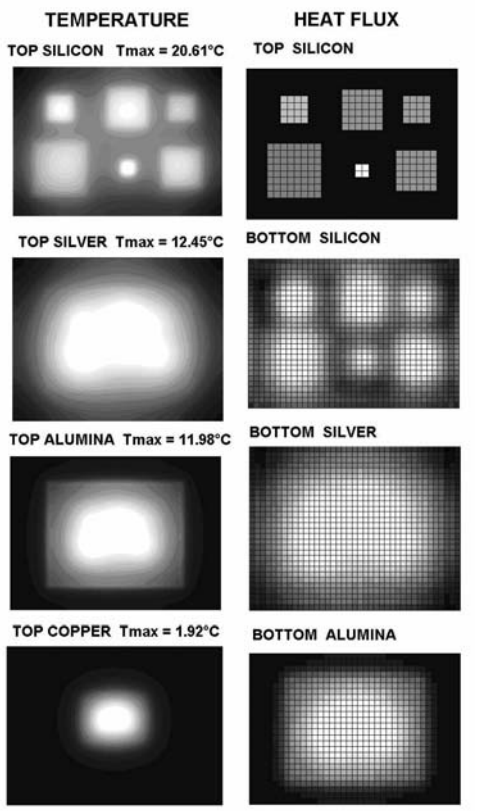

FIG. 4: Gray-scale maps of temperature (upper row) and heat fluxes (lower row) at the interfaces of sample Q0. In each map the color scale is normalized to its own maximum value. The cell grids used are traced in the flux maps.

the points where the higher temperature values occur. As can be seen, the maps in Fig. 5 and the plots in Fig. 5 show quite different temperature distributions for the three samples, despite they were obtained with the same heat generation. These differences are due and are perfectly consistent with the different geometrical configurations of the layers below the silicon die acting as heat spreaders. In fact Q1 shows a temperature distribution which is quite the same of Q0, but increased by a factor greater than one due to the double thickness of alumina, which is the most thermal resistive layer of the stack. The plots of Q3 show not only an increase with respect of Q0 but also a deformation. In this case the distortion of the temperature field is quite evident in the left lower corner of the Q3 map in Fig. 5; the different heat flux displacement across the layers caused by the large asymmetry of the structure is responsible for this different behavior. In fact, the location of the upper power source at a corner of a slab, practically avoids the lateral spreading of the heat flux, thus increasing here the upper temperature because of the higher flux concentration. The showed examples testify how the thermal simulation system is well sensitive also to the package geometrical configuration.

The temperature field of sample Q0 was also investigated in presence of a convective heat exchange over all the lateral and top surfaces in contact with the external environment. Fig. 7 shows the temperature plots on the top silicon surface along the usual cross sections, calculated for several values of the convective heat exchange coefficient (hv), from the adiabatic case (hv=0), to the quiet air condition (hv=8 W/^{o}Cm^{2}) until very high convection values (hv=20000 W/^{o}Cm^{2}) corresponding to the case of water in changing state. The environment temperature was set to –10 °C, below the bottom heat sink one (To = 0 °C) just in order to slightly enhance the heat exchange. As can be seen, in the Fig. 7 has been drawn only the plots for hv = 1000, 5000, 10000 e 20000 W/^{o}C m^{2} since those for lower convection coefficients cannot be distinguished from the adiabatic case, differing of about half degree centigrade. These weak influence of the convection means that the conductive heat exchange across the whole structure largely prevails on the convective one. However, if a contact thermal resistance is placed at bottom surface of the copper heat spreader,

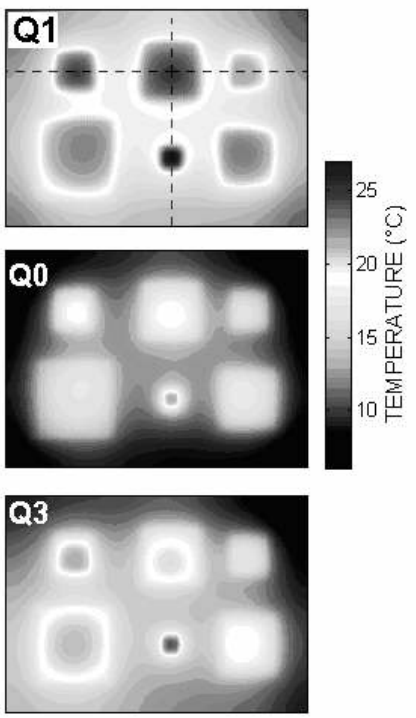

FIG. 5: Surface temperature maps for the three samples drawn with the same grey color scaling. The Q1 map shows the two main cross-sections location.

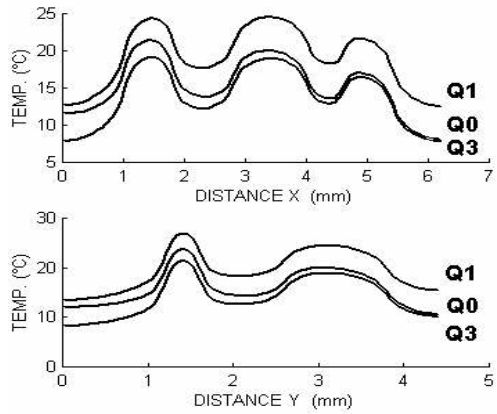

FIG. 6: Surface temperature plots along the cross sections in the top of Fig. 5 for the three samples.

the conductive thermal resistance of the whole structure tents to increase and the temperature decreasing effect of the convection may become more evident.

3.3. Comparison with finite elements analyses

In order to establish a reference for the DJOSER result validation, all the designed models were also simulated using the standard and consolidated finite element method

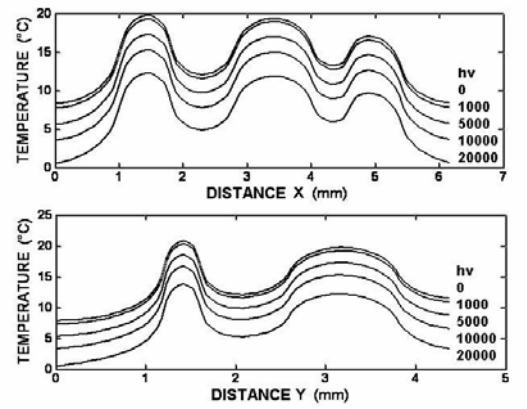

FIG. 7: Temperature profiles along the two cross sections for sample Q0 and for several values (expressed in W/°Cm^2) of the convection heat exchange coefficient on all the surface in contact with the external environment which in kept at -10 °C.

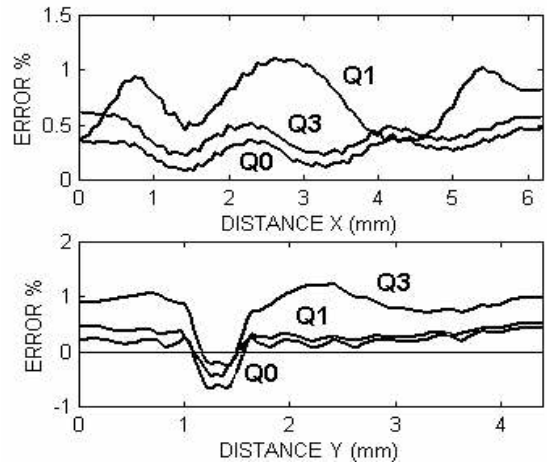

FIG. 8: Relative error percentage plots of the DJOSER simulations with respect to the corresponding FEM data along the cross sections of Fig. 5.

performed using the program MARC and the pre-post-processor MENTAT, both by Mac Neal Schwendler Comp. The FEM simulations were carried out using a very dense 3-D meshing grid, (more than 64000 nodes) in order to avoid as much as possible the temperature and flux calculation error with respect to the reality. As an example, the silicon and the silver layers of the above virtual samples were built using cubic elements with a side length of 0.1 mm, the half of that used by the analytical simulator DJOSER.

The accuracy of the DJOSER thermal simulation was verified by comparing the silicon surface temperature data with those obtained from the FEM thermal analysis. This comparison is here presented in terms of relative error percentage plots, shown in the Fig. 8, referred to the

maximum temperature within the corresponding FEM maps and along the same two orthogonal cross-sections shown in the Fig. 5. All the errors data were obtained by subtracting the temperature values calculated by the DJOSER model in the same nodes of the FEM grid.
As can be seen, the error percentage is everywhere within the 1% limit which is just the main goal of the present simulation model.

4. EXPERIMENTAL VALIDATION

4.1. Thermal analysis of real multilayer structures

The accuracy degree of DJOSER program has been verified from the experimental point of view too, by comparing the temperature data provided by simulations with the real thermal profiles measurements recorded by a thermo-camera AVIO 625XXXX.
The purpose of this experiment is to verify the data congruence not only from the maximum temperature point of view, but also from that of the temperature spatial distribution. To this aim some pyramidal structures composed of layers of different materials have been built.
The top layer consists of a thick film rectangular resistance (18x13 mm^2) of 1.1 ohm that is deposited on an alumina substrate. This resistance can support up to 40W power. Owing to the type of experiment and just to directly detect the temperature on the thermal source, the dissipated power has been placed on top of the layer stack.
The real multi-layer stack has been assembled by sticking to each other layers of various thickness and material (insulating or conductor) with well-known thermal conductivity. A special stick with high conductivity, specific to electronic packaging, has been used to guarantee the minimum thickness and a low thermal contact resistance.
Fig. 9 shows both the plan and cross-section of two samples used for the experiments, while in the Table 2 the layers sequences together with the dissipated power on the resistor are reported. For these structures, the top surface temperature behaviour and the maximum temperature mainly depend on the contact thermal resistances of the interfaces, namely on the thermal stick between different layers and on the thermal grease used to connect the sample to the thermostat. Actually, those values are really unknown because they depend on the contact surface roughness and co-planarity.
In order to know the total resistance without any uncertainty, in parallel to the pyramidal samples, some parallelepiped samples with the same layers but all with the same area were purposely built.

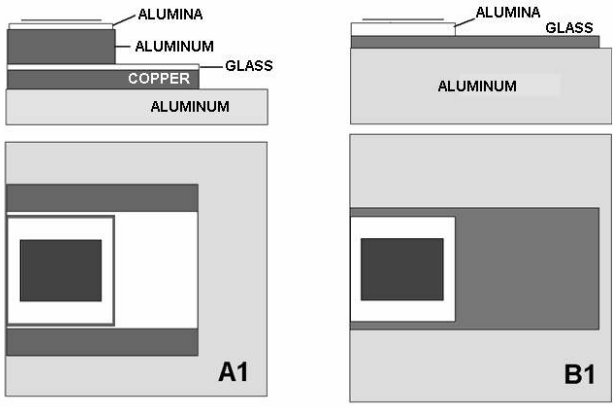

FIG. 9: Cross-section and top view of samples A1 and B1 used for thermo-graphic experiments. The power resistor is the dark rectangle in the middle of the alumina.

TABLE 2 referred to the*: Characteristics of the samples used for the thermo-graphic tests.*

	Sample A1			Sample B1		
Layer	Mat.	Lx*Ly mm^2	Lz mm	Mat.	Lx*Ly mm^2	Lz mm
1	Al_2O_3	23x23	1.0	Al_2O_3	23x23	1.0
2	Al	24x24	6.4	Glass	55x26	1.0
3	Glass	42x26	1.0	Al	57x58	6.0
4	Cu	42x38	3.6			
5	Al	58x56	6.4			
Po	18.73 W			10.86 W		

This area is the same as that of the alumina layer where the resistor has been deposited. In this way, the thermal flux through the layers of these samples has a uniform as possible distribution. Indeed, only in this condition it is possible to compute the contact thermal resistance as the product of the layer specific thermal resistance with the area. The values of these parameters for the different stick and grease layers have been obtained on the basis of the maximum and average temperature on top of the resistance, measured by a thermocouple and an infrared thermometer, respectively, subtracting the thermal drop contributions due to the massif layers with known conductivity and thickness. The multi-layer structure bottom surface was in contact with a thermostat at 20°C while the air temperature results to be equal to 24°C.
The steady-state thermal behaviour of the structures has been analyzed with an infrared video-camera AVIO Neo Thermo TVS-600: this apparatus can visualize the surface temperatures with an appropriate chromatic scale. The obtained thermal images also show the absolute temperature on three fixed points. The emissivity of the surfaces has been made uniform and equal to 0.97 by painting all the materials in smoke black soot.

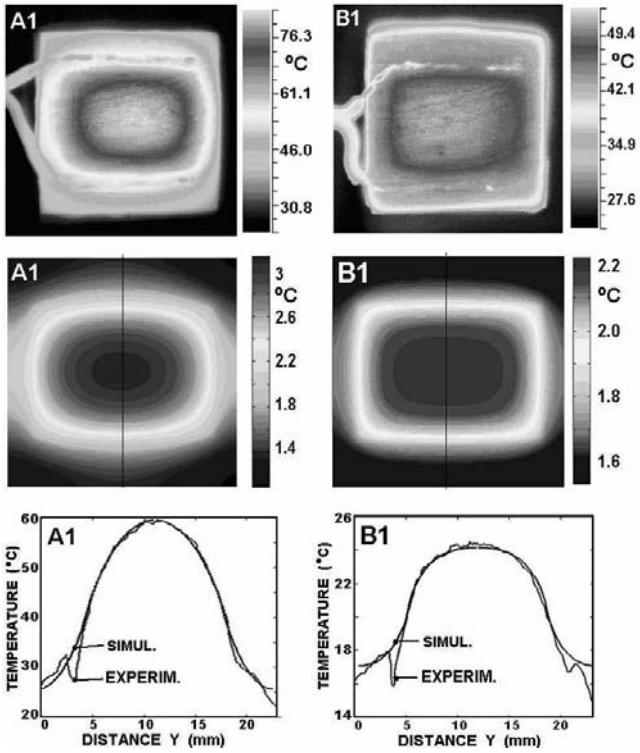

FIG. 10: Comparison among thermo-graphic pictures (top), simulated thermal maps (medium) and surface temperature plots along vertical the median section (down).

The recordings have been performed with two different degrees of resolution: the first with a 35 mm lens at lower resolution, the second with a 70 mm lens at higher resolution but with a smaller field of vision. The coefficient of convection between surfaces and air is 8 W/°Cm^2 because the tests were carried out in a room without ventilation.
The comparison between simulation results and experimental tests is shown in Fig.10 for the samples A1 and B1. The figure shows the thermo-graphic pictures (top), the simulated thermal maps (medium) and the comparison of the surface temperature plots along the vertical median section of alumina (bottom). The simulated thermal maps are normalized for 1 W dissipated power and they are referred to 0°C thermostat temperature. For the comparison with the thermo-graphic recordings, we need to multiply by the actual dissipated power and to add the temperature difference of the thermostats.
We can notice that the agreement between the simulated and measured values (see Fig. 10) is good regarding both the maximum temperature and the surface distribution. In fact, the two graphs show that the trend of the simulated temperature is very similar to real one in both cases.

In particular, we can observe the different shape of the spatial distributions in the two samples: more rectangular and uniform for the sample B1, more convex for A1. These differences, which depend on the different conductivity of the underlying layers, are faithfully replicated on the simulated temperature maps too. Possible small local differences between real and simulated trends, mainly along the resistor borders, are certainly due to side effects unpredictable by the simulator. Among them, we can cite the "wing" effect of the current wires which causes local deformation of the temperature field, the presence of the metallization of the resistor contact with the wire soldering, possible light differences in the resistor current density, the resistor surface roughness and/or the non-uniform blacking.

4.2. Thermal analysis of industrial power electronic circuit

The last experiment in test and validation of the DJOSER program concerns the thermal evaluation of a part of an industrial power electronic circuit, consisting of an electrical power regulator for motorbikes manufactured by Mitsuba Europe and shown in the photograph of Fig. 11. The main heating devices are three power mosfets and three power junction diodes driving up to 40 amperes. These devices are mounted on the board in naked-chip configuration with up to 50 gold bonding wires connecting the top terminal with the underlying copper metallization. The circuit was mounted on a IMS aluminium (Insulated Metal Substrate) substrate with high mechanical stability and high thermal dissipating characteristics. The set of the layer composing the assembling structure for a single diode are summarized in Table 3. As explained below, the most critical layer, from the thermal point of view, is the 80 microns thick insulator layer covering the aluminium substrate. This is composed with epoxy resin and a silica wire tissue.
Fig. 11 also shows an emphasized view of the area surrounding a diode, which was taken as the object of the thermal experiment. As can be seen, the silicon die was placed just at the corner of a copper frame which is physically separated from the surrounding metallization. The electrical power is dissipated on the whole top die surface, below the aluminium metallization.
The circuit was placed on a thermostat at 23 °C and tested at several electrical powers, ranging from 0.2 W to 11 W, by means of both electrical measurements, in order to measure the thermal resistance, and thermo-graphic mapping using the above cited apparatus. Equally, the sample was covered with smoke black soot to establish a uniform emissivity over the whole area. Using the average temperature data over the die area, both the methods

Table 3: Characteristics of the layers composing the circuit under investigation.

Mat.	Lx*Ly mm^2	Lz mm	k W/m°C	Contact Resistance mm^2°C/W
Al-Si	4x3	0.03	161	
Si *	4x3	0.3	131	Tin solder (0.5)
Cu	18x18	0.07	386	Insulator (230)
Al	32x32	2	204	Thermal grease (350)
Power =* 7.04 W				

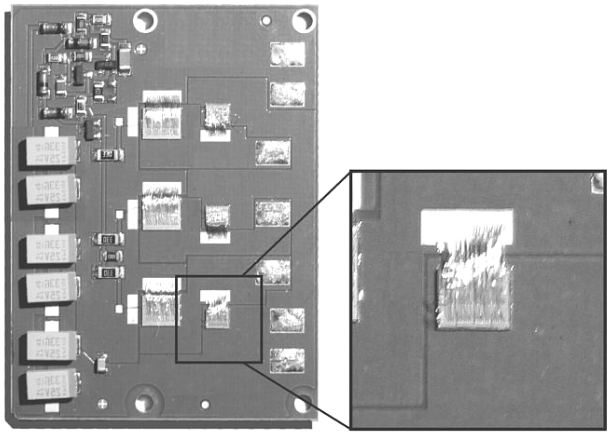

FIG. 11: Photograph of the power circuit and the planar junction diode subjected by the thermal analysis.

yielded the same value for the thermal resistance of the diode which was about 8.2 °C/W.
The model for the DJOSER thermal simulation was built on the basis of the data in Table 3, locating the power dissipation on the top silicon layer below the top metallization, respecting the asymmetry of the copper layer and neglecting the contribution of the thermal convection heat exchange with the environment.
The only differences in the DJOSER model are that the tin solder below the silicon and the thin insulating layer above the aluminium substrate were omitted and replaced with a zero-thick contact thermal resistance below the silicon and the copper layer. In fact as far the insulator is concerned, the presence of a very thin layer of a highly thermal resistive material is the most critical situation for the DJOSER program which can give unreliable results. This is probably due to the fact that in this case the matrix of the algebraic system to be solved may become badly conditioned. The contact thermal resistance values for the insulating layer and for the bottom thermal grease connecting the substrate to the thermostat were deduced from the electrical measurements analyzed by means of the TRAIT method [7,8]. Their value were about 230 mm^2°C/W for the insulator, which is higher than expected

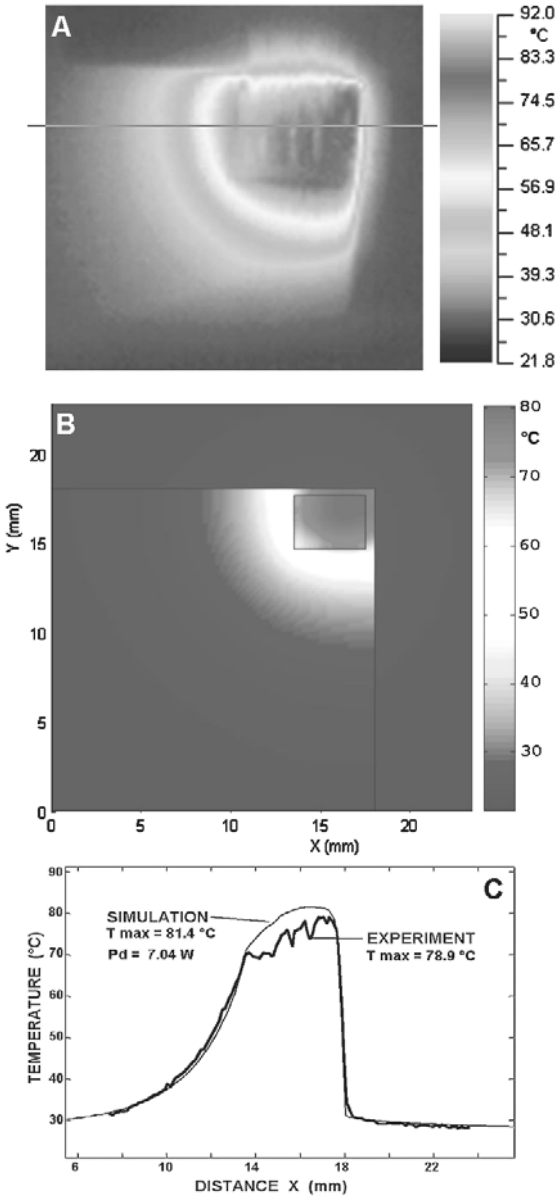

FIG. 12: A) Experimental thermo-graphic map of the junction diode; B) simulated temperature map; C) comparison between the experimental and simulated temperature plots along the cross-section shown in the map A.

from the epoxy resin thermal conductivity (1.8 W/m°C) data given by the vendor, but it is in agreement with results found in literature concerning the comparison of the thermal resistances of several types of IMS substrates [9,10] : those using the silicon wire tissue show worse thermal resistance per unit area.
The comparison between the thermo-graphic maps (A) and the simulated ones (B) are shown in the Fig. 12. The lower plot of the figure shows the comparison between

the temperature distributions along the cross-section drown in the upper viewgraph. As can be seen the agreement is well satisfactory except on the higher part of the plots due to the presence of the bonding wires with their heat dissipating effects. In particular, it can be pointed out the typical 'cornered' shape of the temperature field, reflecting of course the spreading of the heat flux, due to the cornered position of the silicon die on the underlying copper metallization.

5. CONCLUSIONS

In conclusion, the above exposed experiments demonstrated that the DJOSER simulation program may give reliable results for the steady state temperature maps of power devices and circuits having the usual planar assembling structure and therefore it can be proposed as a fast and easily programmable tool for the thermal management studies of these systems. However the mayor limitation for the applicability of the program is the need of uniform thermal characteristics of all the layers and of their thermal boundary conditions. This implies that many structural details of the packages, such as external metal pins, thermal vias across the layers, bonding wires, cannot be taken into account.
Finally, the experimental validation tests also focused the important contribution of the contact thermal resistances between the layers to the dissipating capabilities of the packaging structures. The values of these parameters are largely unpredictable and strongly depend on the actual deposition process runs.

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