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Logic circuit prototypes for three-terminal magnetic tunnel junctions with mobile domain walls

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Spintronic computing promises superior energy efficiency and nonvolatility compared to conventional field-effect transistor logic. But, it has proven difficult to realize spintronic circuits with a versatile, scalable device design that is adaptable to emerging material physics. Here we present prototypes of a logic device that encode information in the position of a magnetic domain wall in a ferromagnetic wire. We show that a single three-terminal device can perform inverter and buffer operations. We demonstrate one device can drive two subsequent gates and logic propagation in a circuit of three inverters. This prototype demonstration shows that magnetic domain wall logic devices have the necessary characteristics for future computing, including nonlinearity, gain, cascadability, and room temperature operation.

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There is great interest in encoding information in magnetic materials for future memory and logic[1–6]. Recent developments in perpendicular anisotropy materials[7,8] and spin Hall effect-assisted domain wall (DW) switching[9–11] have reduced the current density required to switch a magnet. Many groups are working on instantiations of magnetic logic and memory, for example, ratchet memory[12], three-terminal magnetic random access memory[13], majority logic gates[14,15], nanomagnetic logic[16] and mLogic[17]. These devices show promise for future computing, and work has been done to simulate and build them. However, so far, little work has shown experimentally verified DW-based devices that can perform logic, be used in circuits, and have a gate-like basic element that can be used to build more complex circuits.

In this work, we present magnetic device prototypes that are capable of integration in logic circuits and easily adaptable to the continuing advances in spintronics materials and scaling. The device is a memory cell that we adapt to logic. Information is stored in the position of a DW in a short, narrow ferromagnetic wire, written using spin-torque transfer[18] from pulsed voltage clocks, and read out using a magnetic tunnel junction (MTJ)[19]. The device is nonvolatile and is predicted to scale to switching energies competitive with field-effect transistors[1]. We demonstrate that a single device can perform buffer and inverter operations, one device can drive two subsequent devices and three devices in series act as a circuit of three inverters. These results provide a path for realizing spintronic circuits.

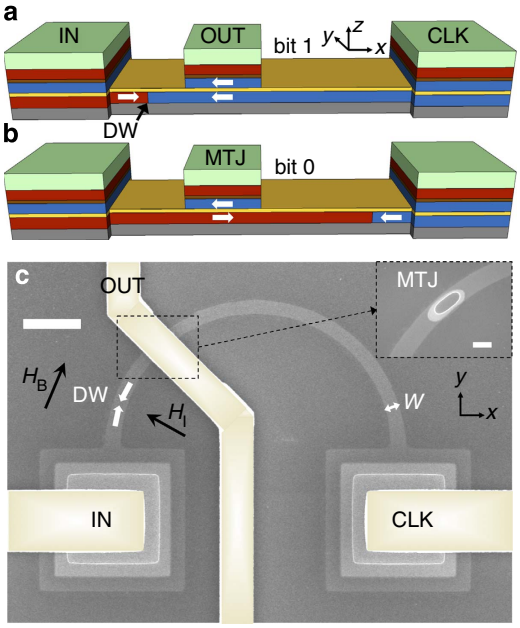

Figure 1 | Logic device cartoon and SEM. (**a**), Cartoon of the domain wall (DW) logic device, comprised of a magnetic wire with a DW and a magnetic tunnel junction (MTJ) to read out the DW position. Right-pointing magnetic moments are red and left-pointing are blue (grey represents Ta, brown Ru, and light green IrMn). Magnetization direction is also shown by the white arrows. The MgO tunnel barrier is shown in yellow. The device has three terminals, IN, CLK, and OUT. When the wire magnetization is parallel to the MTJ magnetization, the current at the OUT terminal is high, representing bit 1. (**b**), Cartoon showing the DW switched to the opposite side of the device, representing bit 0. (**c**), SEM image of a DW-Logic device prototype, showing the magnetic wire of width $w = 400$ nm and the MTJ under the center electrode with area 1 μm × 400 nm, also shown in the inset. Electrodes are coloured in light gold. The initial DW position is shown by the white arrows. The black arrows show the orientation of the initialization field $\mathbf{H}_I$ and bias field $\mathbf{H}_B$. Scale bars, 2 μm (**c**), 400 nm (**c**, inset).

Results

Domain wall logic device structure. The prototype is shown schematically in Fig. 1a,b. It consists of two parts: a ferromagnetic wire containing a DW and a MTJ. The wire is composed of sputter-deposited thin films on a Si substrate: SiO_2 (200 nm)/Ta (3 nm)/$Co_{40}Fe_{40}B_{20}$ ($t = 4$ nm)/MgO (1 nm). The CoFeB has in-plane magnetic anisotropy; while perpendicular anisotropy will be more energy-efficient in scaled devices[1,20], as explored in ref. 1, for initial prototypes the logic behaviour is independent of anisotropy type. The MTJ stack is CoFeB (2.5 nm)/Ru (0.8 nm)/CoFeB (2.5 nm)/$Ir_{20}Mn_{80}$ (10 nm)/Ta (3 nm)/Ru (7 nm). There are three terminals: IN, CLK and OUT.

Figure 1c shows a scanning electron microscope (SEM) image of a fabricated device. The wire width is $w = 400$ nm and is shaped into a curve to allow initialization of the DW using a globally applied field $\mathbf{H}_I$. Micromagnetic simulations predict that the DW is transverse, see Supplementary Fig. 1. The MTJ sits under the center electrode. The IN and CLK terminal pads are 5 μm × 5 μm MTJs used to contact the magnetic wire, much larger than the center MTJ. At this size there is negligible magnetoresistance in the pads due to pinholes in the MgO layer, so their tunnel junctions are ignored. The estimated series resistance of the pads is about 100 Ω, small compared with the wire resistance.

Device operation includes an initialization step, a write step and a read step. First, $\mu_0 H_I = 200$ mT is applied to initialize the DW on the left, where μ_0 is the permeability of free space. This field is large enough to saturate the magnetic moments in $\hat{\mathbf{H}}_I$, such that when the field is removed a DW is nucleated along the field direction. By having a curved wire, we can set the initial DW position by choosing the field angle. The magnetization is parallel on either side of the MTJ, and its resistance is low (bit 1, Fig. 1a). See Supplementary Figs 2 and 3 for field-driven device characteristics. For current-driven behaviour, a 1-μs voltage pulse is applied to the IN terminal with CLK grounded. It is theoretically possible to use a three-phase sinusoidal clock to save energy[1,21]. If the input current, I_{IN}, is above the threshold current of the DW, I_T, then the current can translate the DW past the MTJ using current-induced DW motion[22], switching the MTJ to a high-resistance state (bit 0, Fig. 1b). Most likely, the current-induced switching is a combination of spin transfer torque and heat-assisted depinning[23]. I_T depends on both intrinsic and extrinsic pinning of the DW from sources such as line edge roughness[24] and magnetocrystalline defects.

The device can then be read by a voltage pulse applied to CLK sunk to the input of the next device. The current at the output terminal, I_{OUT}, will be high or low depending on the position of the DW, and can be fed into the next device stage. To avoid damage to the devices at high current density, DW motion is assisted by a global bias field $\mathbf{H}_B$, aligned parallel to the initial DW position. The bias field could be eliminated by using a magnetic material with lower I_T, or by scaling the devices to smaller length scales. Simulations and experiments suggest that the current density required to depin a DW decreases with wire width to sub-50 nm sizes[1,22].

Single device behaviour as inverter and buffer gates. A single device can be used as a logic gate when the current at the input terminal, I_{IN}, is the sum of multiple input currents. Figure 2a shows an example of a device acting as an inverter, which can be used to do a two-input NAND operation, with parallel MTJ resistance $R_P = 23.7\,\Omega$, antiparallel MTJ resistance $R_{AP} = 25.7\,\Omega$, wire resistance $R_w = 1.18\,\mathrm{k}\Omega$ and tunnel magnetoresistance $TMR = (R_{AP} - R_P)/R_P \times 100 = 8.4\%$ (ref. 25). Initialization with $\mathbf{H}_I$ sets the MTJ initially in a parallel state (bit 1), with the DW on

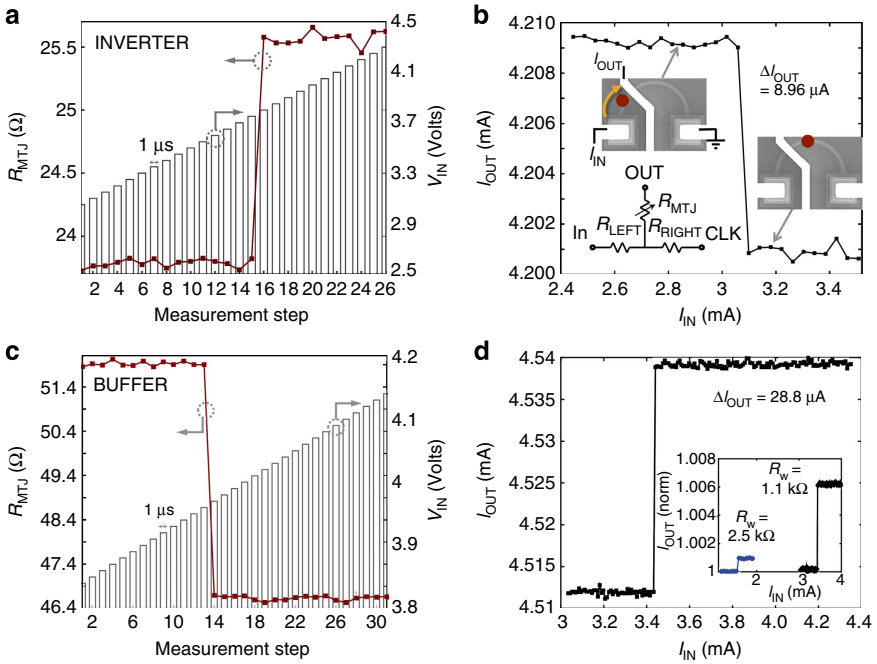

Figure 2 | Inverter and buffer operation. (**a**), Transient showing the MTJ resistance and applied voltage pulses between IN and CLK versus time. At 3.80 V, the device switches from low resistance (bit 1) to high resistance (bit 0). (**b**), Transfer characteristic of I_{OUT} through the MTJ versus I_{IN} across the wire. The SEM images show the configuration below I_T, with the DW position approximated by the red dot and I_{IN} electron flow direction shown by the yellow arrow, and the approximate DW position after I_T. inset, Simple circuit diagram to represent the device, including the wire resistance and the variable tunnel junction resistance. (**c**), Transient behaviour showing a buffer operation, plotting R_{MTJ} and V_{IN} versus measurement step as we increase the 1-µs voltage pulse amplitude in 0.01 V steps. This device has similar R_w to the previous device, but slightly higher R_{MTJ} and *TMR*. At 3.97 V, the device switches from a high-resistance output to a low-resistance output. (**d**), Transfer characteristic for the buffer. inset, Comparison of this transfer characteristic (right black curve) to that of another device (left blue curve) with less well matched R_w and R_{MTJ}.

the left as in Fig. 1a,c. A bias field $\mu_0 H_B = 3.0$ mT is then applied parallel to the DW. We apply a series of 1-µs voltage pulses, V_{IN}, increasing in 0.05 V steps, to the IN terminal. Each input pulse is followed by a 100 mV d.c. voltage applied to the CLK terminal to measure the resistance through the MTJ, R_{MTJ}. Between $V_{IN} = 3.75$ V to 3.80 V, corresponding to an input current of $I_T = 3.099$ mA ± 0.041 mA (with range determined by the voltage step) and current density $J_T = 1.9 \times 10^{12}$ A m^{-2}, the DW is translated across the MTJ, switching the output from R_P (high current, bit 1) to R_{AP} (low current, bit 0).

The current is calculated using the circuit in Fig. 2b (inset), with the wire resistance represented by $R_w = R_{LEFT} + R_{RIGHT}$ and the MTJ represented by a variable resistor R_{MTJ}. For an isolated device, we define the input current as

$$I_{IN} = \frac{V_{IN}}{R_S + R_{LEFT} + R_{RIGHT}} \quad (1)$$

where R_S is the load resistor from the voltage supply. If we read each device using V_{OUT}, then we define the output current for an isolated device as

$$I_{OUT} = \frac{V_{OUT}}{R_S + R_{RIGHT} + R_{MTJ}}. \quad (2)$$

Device stages are pulsed in sequence, where in each stage a device can also have an input resistor that is tuned to put the input current in the correct range to read the data from the previous stage. Thus, if the input current originates from two logic gates, with output resistances such that the input currents sum in the subsequent gate, then that device switches from 1 to 0 only when the input current exceeds I_T. The resulting transfer characteristic is in Fig. 2b. The change in the MTJ resistance modulates the output current by $\Delta I_{OUT} = 8.96$ µA, assuming a CLK voltage pulse of 3.80 V and no external load attached to the OUT terminal.

Figure 2c shows a device instead acting as a buffer gate. The buffer is shown for a different device: $R_P = 46.5\,\Omega$, $R_{AP} = 52.1\,\Omega$, $R_w = 1.10$ kΩ, and $TMR = 12\%$. The device is initialized the same as previously. We program it to act as a buffer rather than an inverter by applying a higher bias field $\mu_0 H_B = 4.8$ mT, above the field switch of the reference layer of the MTJ but below that of the DW, initializing the MTJ in the antiparallel state (bit 0). The DW switches across the MTJ between 3.96 and 3.97 V, or $I_T = 3.441$ mA ± 0.009 mA, $J_T = 2.0 \times 10^{12}$ A m^{-2}. The output switches from high resistance (low current, bit 0) to low resistance (high current, bit 1). Across multiple devices, the transfer characteristic shows a very sharp switch between resistance states, $\Delta V_{IN} < 0.01$ V, the limit of our voltage supply. This enables stable 0 and 1 outputs even with $TMR = 8$–20% seen in our devices. At the switch, $\Delta I_{OUT}/\Delta I_{IN} = 3.1$. In Fig. 2d we plot I_{OUT} versus I_{IN} for the isolated buffer device with $V_{OUT} = 3.97$ V. The change in current between the 0 and 1 output bits is $\Delta I_{OUT} = 28.8$ µA assuming no output load.

While $\Delta I_{OUT} = 28.8$ µA is an appreciable difference in current for stable 0 and 1 bits, the fractional output current change is $\Delta I/I = (I_P - I_{AP})/I_{AP} = 0.3\%$ of the bit 0 output current $I_{AP,OUT} = 4.5$ mA. In an ideal device, $\Delta I/I$ should be maximized for the best noise margin and potential fanout. Using Equation 2 with fixed V_{OUT}, and assuming that the gate drives a single subsequent ferromagnetic wire, we find

$$I_P = I_{AP} \frac{R_S + 2R_{RIGHT} + R_{LEFT} + R_{AP}}{R_S + 2R_{RIGHT} + R_{LEFT} + R_P}. \quad (3)$$

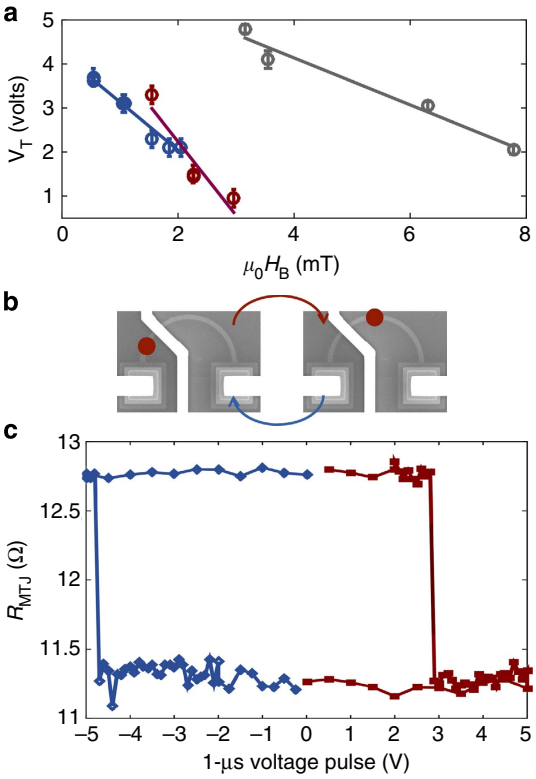

Figure 3 | Variability and reversibility. (**a**) Threshold voltage versus bias field for three different devices, where the error bars represent the depinning voltage standard deviation repeated at least 3 ×, with the DW reinitialized between each. Grey = device 1, red = device 2 and blue = device 3. The lines are a linear fit. Devices 2 and 3 were fabricated together, while device 1 was fabricated at a later time on a different wafer piece. (**b**) SEM images showing reversibility setup, with the DW moving back and forth past the MTJ as shown by the red dots. (**c**) R_{MTJ} versus pulsed V showing reversibility of device 1's state. In the positive direction $\mu_0 H_B = 3.3$ mT; in the negative direction $\mu_0 H_B = -6.2$ mT. The red dot in the SEM images is the approximate DW position at high and low R_{MTJ}, respectively.

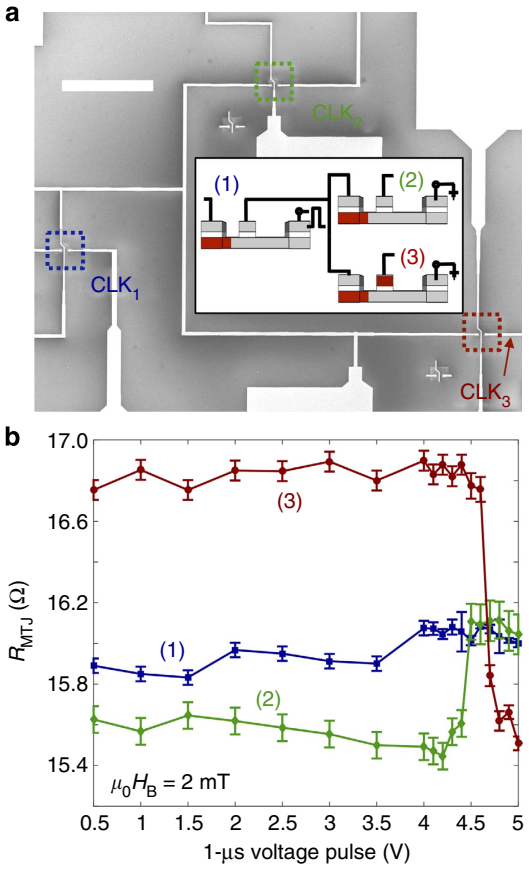

Figure 4 | Concatenation. (**a**) SEM image of one device output connecting to the inputs of two devices. Voltage pulses are applied to CLK$_1$ with CLK$_2$ and CLK$_3$ grounded. Scale bar, 100 μm. (inset) Cartoon of the initial configurations of the three devices, with the DWs initialized on the left. Red signifies magnetized right and grey signifies magnetized left. (**b**), Plot of MTJ resistance versus pulsed voltage applied at CLK$_1$, showing one device can power a switch in two subsequent devices. Here, the error bars represent the average noise fluctuation in R monitored for each device at each voltage step.

If we define the output resistance in the parallel state $R_{OUT} = R_P + R_{RIGHT}$ and the load resistance $R_{LOAD} = R_{LEFT} + R_{RIGHT} + R_S$, then we can define a figure of merit

$$\frac{\Delta I}{I} = \frac{TMR}{(R_{OUT} + R_{LOAD})/R_P}. \quad (4)$$

Equation 4 shows that the highest noise margin and fanout is obtained by maximizing the TMR and matching the MTJ parallel resistance and the resistance of the wire.

Figure 2d (inset) compares I_{OUT} versus I_{IN} of the original buffer device (black curve) to another tested device with higher $R_w = 2.54\,k\Omega$, $R_P = 12.4\,\Omega$, and $TMR = 21\%$ (blue curve). Even though the TMR is higher, since $(R_{OUT} + R_{LOAD})/R_P$ is also higher we find lower $\Delta I/I = 0.1\%$. For a given wire resistivity and MTJ resistance-area product, we can reduce the ratio between the wire and MTJ resistances by properly choosing the size of the wire and the size of the MTJ. Future devices with size optimized for resistance instead of fabrication constraints are expected to exhibit a substantially larger percent change in current. Increasing the MTJ quality to $TMR = 100$–600% (ref. 5) and choosing the wire and MTJ geometries to match $(R_{OUT} + R_{LOAD})$ and R_P would increase $\Delta I/I$ up to 100–600%, and implementing PMA and spin Hall-induced switching could reduce power consumption and J_T by 100 × (ref. 26).

Device variability and reversibility. In Fig. 3a we plot the threshold voltage, V_T, versus H_B for three different devices to assess the variability in $V_T = I_T(R_w)$ and between devices. The DW depinning voltage is repeatable within $\pm(0.15 \pm 0.1)$ V at each bias field. This is without externally fabricated pinning, such as notches[27], that can supply more repeatable depinning at the expense of higher depinning currents. There is a linear trend within a device, but variation between different devices. Devices 2 and 3 were fabricated at the same time from the same 10 mm × 10 mm thin-film wafer piece, while device 1 was fabricated at a different time from a separate wafer piece and shows higher device-to-device variation in the V_T versus H_B slope. Thus, we can conclude that the device-to-device variation seen in the prototypes arises from variations in fabrication, for example, electron-beam resist age and etching rates, and variation in the MgO thickness across the initial 3-inch diameter thin film wafer, which causes variation in TMR across the wafer.

We can estimate the zero-field current density from the linear trends: device 1 V_T $(H_B = 0) = 6.27$ V. Converting to I with $R_w = 4.4\,k\Omega$, we find I_T $(H_B = 0) = 1.4$ mA and J_T $(H_B = 0) = 8.75 \times 10^{11}$ A m^{-2}. This is in agreement with the current density needed to translate a DW in in-plane magnetic anisotropy wires[20].

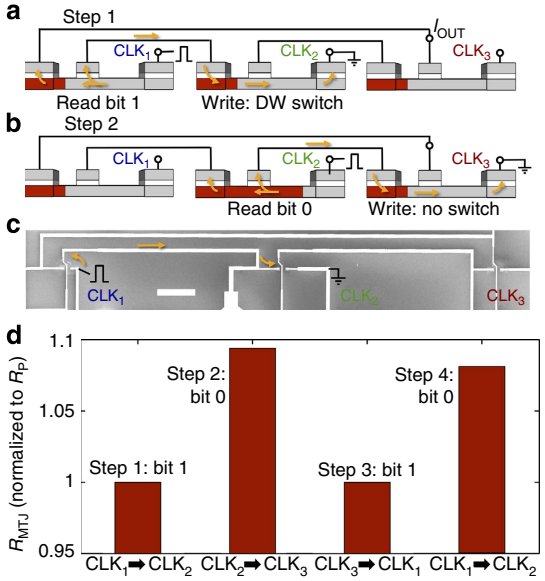

Figure 5 | Three inverters circuit. (**a**) Cartoon showing three devices connected in series, with the output of device 3 feeding back into the input of device 1. The devices are initialized with their domain walls (DWs) on the left and the tunnel junctions parallel. In the experiment, at Step 1 we apply a voltage pulse at CLK_1 to read the state of device 1 while writing the state of device 2. The voltage pulse is applied between CLK_n and CLK_{n+1}. Yellow arrows represent electron flow direction. In this case the DW in device 2 switches. (**b**) Cartoon of Step 2, where we now apply a voltage pulse at CLK_2 to read the state of device 2 while writing the state of device 3. In this case the DW in device 3 does not switch. In Step 3 and Step 4 this is repeated at CLK_3 and CLK_1, respectively. (**c**) SEM of three devices in series. $R_{P1}=23.8\,\Omega$, $R_{P2}=19.0\,\Omega$, and $R_{P3}=18.4\,\Omega$. Scale bar, 50 μm. (**d**) Plot of the MTJ resistance at each step in the three inverters circuit, showing the oscillation of the DW position at each step between the parallel (low MTJ resistance, bit 1) and antiparallel (high MTJ resistance, bit 0) device states.

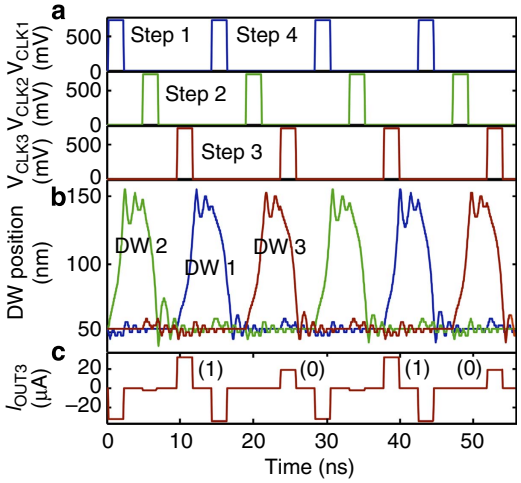

Figure 6 | Simulation of scaled three inverters circuit. Micromagnetic/circuit simulation of transient behaviour predicted in a scaled-down device circuit with $w=15$ nm and $TMR=100\%$. (**a**) 0.7 V, 2 ns clock voltages for each device applied sequentially in time. (**b**) Simulation of the domain wall (DW) behaviour of each device, where we can see the DW switches between the left side of the device (~50 nm) and the right (~150 nm). Once the DW switches, it oscillates about its position. (**c**), Current at the I_{OUT3} node from Fig. 5a versus time. The positive current oscillates between bit 1 (32 μA) and bit 0 (19 μA). The negative current is from current flowing back from subsequent clock pulses, but it does not disturb the DW position in device 3.

Figure 3b shows the reversibility behaviour of device 1. After initialization in the buffer configuration, at $+2.9$ V R_{MTJ} switches low; reversing $\hat{\mathbf{H}}_B$ we see R_{MTJ} switch high again at -4.8 V. H_B is higher on the negative side of the loop since the field direction is less parallel to the DW.

Concatenation behaviour of multiple devices in circuits. Figure 4a is a SEM image showing three devices concatenated together, with device 1's output feeding the input of device 2 and device 3. The dotted boxes identify devices shown in Fig. 1c. The initial state is conceptualized in Fig. 4a (inset). After initialization and $\mu_0 H_B=2.0$ mT, devices 1 and 2 are in an inverter configuration, and device 3 is a buffer. We then apply 1 μs voltage pulses to the CLK_1 terminal with the CLK_2/CLK_3 terminals maintained at ground and all other terminals floating. Figure 4b shows R_{MTJ} after each pulse. The output current from device 1 switches both device 2 and device 3, at $4.5\,V\pm0.3\,V$ and $4.7\,V\pm0.2\,V$, respectively (range is from three experiment repeats). The resistance of device 1 remains unchanged because its DW is initialized on the left side of its wire, and thus we are able to read device 1 without disturbing its logic state. This demonstrates that one gate can drive two gates, and that we can read the state of device 1 and then use that output current as the input to write devices 2 and 3. We can power more than two gates by further increasing the voltage pulse amplitude or tuning the resistance-area product of the MTJ to output higher current.

Figure 5 shows a circuit of three inverters that concatenates three devices in series. The output of device 3 is fed back into the input of device 1. We initialize all devices in the inverter configuration, depicted in Fig. 5a. To drive the logic flow, we apply sequential voltage pulses to CLK_1, CLK_2 and then CLK_3. For example, in Step 1, the voltage pulse applied to CLK_1 with CLK_2 grounded allows us to read device 1 while writing device 2. Since the output of device 1 is high (bit 1), the current is high enough to switch the DW in device 2, changing it from a 1 bit to a 0 bit. In Step 2, Fig. 5b, we apply a voltage pulse to CLK_2 with CLK_3 grounded to read device 2 while writing device 3. Since device 2's output current is now low (bit 0), the DW in device 3 does not switch and it stays as a bit 1.

Figure 5c shows an SEM image of a fabricated three inverters circuit, initialized in the inverter configuration with $\mu_0 H_B=3.0$ mT. In Fig. 5d, we measure R_{MTJ} as the information propagates around the circuit. The devices are clocked in sequence by 4.5-V pulses such that at each stage the data token is inverted. The voltage amplitude of 4.5 V is optimized for device 3, such that when device 2 is in the antiparallel state the DW of device 3 does not switch. To see the inverting operation, each resistance is normalized to its own R_P. The output resistance at each pulse step oscillates between R_P and R_{AP} as we move around the circuit, showing oscillation between 1 and 0 bits. Operation is stopped after four steps because additional propagation requires a reset step to return all DWs to the left side. We expect that scaled down devices or materials with lower threshold currents should operate without the need of a bias field, allowing the reset to occur during reading.

In Fig. 6, we model the behaviour of a scaled three-inverter circuit using a transient micromagnetic/circuit simulation[1] to predict scaling, switching energy, and switching delay. For the micromagnetic simulation, we use the Object-Oriented Micromagnetic Framework[28] model with a current-induced DW motion extension[29]. We assume $t=2.5$ nm, $w=15$ nm, wire length 200 nm, TMR = 100%, and material properties for in-plane anisotropy CoFeB (exchange energy 13×10^{-12} J m^{-1}, damping parameter $\alpha=0.01$, non-adiabatic parameter $\beta=0.05$,

saturation magnetization $M_S = 8 \times 10^5\,A\,m^{-1}$, and spin polarization factor $P = 0.4$ (ref. 18)). The simulation inputs current and outputs the new DW position in the wire. We then convert the DW position to a new R_{MTJ} value, which we input into the three-terminal SPICE circuit model[30] shown in Fig. 2b. The circuit model calculates I and V at every node of the circuit, which we input back into the micromagnetic model. We repeat this iterative process every 0.05 ns over the timescale of interest.

Figure 6 shows the simulated transient circuit behaviour. The information flows sequentially, driven by 0.7 V, 2-ns clock pulses. At Step 1 (equivalent to Fig. 5a) we apply V_{CLK1}, shown by the blue voltage pulse. The DW position versus time plot shows that the DW of device 2 switches across the device (green curve). At Step 2 (equivalent to Fig. 5b) we apply V_{CLK2}, shown by the green voltage pulse. In the DW position versus time plot, the red curve represents the position of the DW in device 3, and we see that its DW does not switch at Step 2. This oscillatory behaviour is repeated in Step 3, Step 4 and so on. The data token is inverted every stage, meaning that the DW moves in every other device, for example, device 2 (green), device 1 (blue) and device 3 (red). The simulated circuit differs from the implementation, however, because the implementation uses a bias field. In the absence of the bias field in the scaled simulation, the logic resets itself during the read operation. By monitoring the I_{OUT} node in the simulation, we see it oscillates between high current (bit 1, 32 μA) and low current (bit 0, 19 μA) depending on the DW position of device 3. The negative pulses in the current transient occur when current is flowing backward from the next gate.

Discussion

We have demonstrated the capability of DW-based devices as logic gates, including inverter, buffer, and circuit operation. The DW depinning is non-linear with a sharp switching threshold $\delta V < 0.01$ V, allowing stable 0 and 1 bits below and above the DW depinning voltage. The gates exhibit gain, one gate can drive two subsequent gates, and the three-device circuits shows that they can be cascaded into circuits. The micromagnetic/circuit simulation shows analogous switching behaviour to the experiment in further scaled devices.

While the information is encoded in the DW position, the inputs and outputs are current, maintaining compatibility with conventional field-effect transistors. The gate architecture is simple and adaptable to recent advances in magnetic materials, allowing an increase in $\Delta I/I$ up to 100–600% and a reduction in power consumption and J_T by 100 ×. These results show that magnetic-based logic has a realistic path to implementation, and may provide the basis for digital systems at the end of the semiconductor roadmap.

Methods

Fabrication. Thin film growth was done using UHV d.c. magnetron sputtering[31]. The sample was annealed *in situ* at 280 °C for 30 min with MgO exposed to vacuum to crystalize the CoFeB layer, and *ex situ* at 300 °C for 1 h in a 1-tesla field to set the IrMn exchange bias. Patterning was done using hydrogen silsesquioxane (HSQ) electron-beam resist and a Raith 150 electron-beam lithography tool. The pattern was etched into the thin film using non-reactive ion beam etching. HSQ was used as a spin-on insulator to prevent shorting of the device. A further electron-beam lithography step using polymethyl methacrylate was done to open holes on top of the three terminals for electrical contact. The darker ellipse on top of the MTJ in Fig. 1c shows a hole patterned in the SiO_2 insulating layer to electrically contact the MTJ top. Alignment of the hole on top of the MTJ to within 50 nm between two electron-beam lithography steps limited the initial size of the prototypes. Then Ta (5 nm)/Au (135 nm) electrodes were placed with an additional electron-beam lithography step.

Resistance and current-driven measurements. For testing, the devices were wire bonded to a chip carrier and placed in an electromagnet. A signal multiplexer alternated the device terminal connections between a resistance measuring set-up and a pulse driving set-up.

In the resistance measuring set-up, a lock-in amplifier performed a four-point resistance measurement by forcing a sinusoidal voltage (100 mV, 6.25 Hz quasi-DC) between one OUT terminal and the IN terminal and sensing the output voltage between a second OUT terminal and the CLK terminal. The forced current was known and kept low by a 100 kΩ ballast resistor connected in series with the measured resistance.

In the pulse driving set-up, a pulse generator provided the applied current pulse across the DW track between the IN and CLK terminals.

References

1. Currivan, J. A., Jang, Y., Mascaro, M. D., Baldo, M. A. & Ross, C. A. Low energy magnetic domain wall logic in short, narrow, ferromagnetic wires. *IEEE Magn. Lett.* **3,** 3000104 (2012).
2. Nikonov, D. E. & Young, I. A. in *2012 IEEE International Electron Devices Meeting (IEDM)* 25–4 (San Francisco, CA, USA 2012).
3. Parkin, S. S., Hayashi, M. & Thomas, L. Magnetic domain-wall racetrack memory. *Science* **320,** 190–194 (2008).
4. Kim, J. *et al.* Spin-based computing: device concepts, current status, and a case study on a high-performance microprocessor. *Proc. IEEE* **103,** 106–130 (2015).
5. Allwood, D. A. *et al.* Magnetic domain-wall logic. *Science* **309,** 1688–1692 (2005).
6. Imre, A. *et al.* Majority logic gate for magnetic quantum-dot cellular automata. *Science* **311,** 205–208 (2006).
7. Emori, S. & Beach, G. S. D. Enhanced current-induced domain wall motion by tuning perpendicular magnetic anisotropy. *Appl. Phys. Lett.* **98,** 132508 (2011).
8. Wang, W.-G., Li, M., Hageman, S. & Chien, C. L. Electric-field-assisted switching in magnetic tunnel junctions. *Nat. Mater.* **11,** 64–68 (2012).
9. Kim, K. W., Seo, S. M., Ryu, J., Lee, K. J. & Lee, H. W. Magnetization dynamics induced by in-plane currents in ultrathin magnetic nanostructures with Rashba spin-orbit coupling. *Phys. Rev. B* **85,** 180404 (2012).
10. Ryu, J., Lee, K.-J. & Lee, H.-W. Current-driven domain wall motion with spin Hall effect: Reduction of threshold current density. *Appl. Phys. Lett.* **102,** 172404 (2013).
11. Buhrman, R. A. Spin-torque switching with the giant spin Hall effect of tantalum. *Science* **336,** 555–558 (2012).
12. Lavrijsen, R. *et al.* Magnetic ratchet for three-dimensional spintronic memory and logic. *Nature* **493,** 647–650 (2013).
13. Fukami, S. *et al.* in *2009 Symposium on VLSI Technology* 230–231 (Honolulu, HI, USA, 2009).
14. Nikonov, D. E., Bourianoff, G. I. & Ghani, T. Proposal of a spin torque majority gate logic. *IEEE Electr. Device Lett.* **32,** 1128–1130 (2011).
15. Breitkreutz, S. *et al.* Majority gate for nanomagnetic logic with perpendicular magnetic anisotropy. *IEEE Trans. Magn.* **48,** 4336–4339 (2012).
16. Kurtz, S. *et al.* Non-majority magnetic logic gates: a review of experiments and future prospects for 'shape-based' logic. *J. Phys. Condens. Matter.* **23,** 053202 (2011).
17. Bromberg, D. M. *et al.* in *2014 International Electron Device Meeting* 33.1.1–33.1.4 (San Francisco, CA, USA, 2014).
18. Beach, G. S. D., Tsoi, M. & Erskine, J. L. Current-induced domain wall motion. *J. Magn. Magn. Mater.* **320,** 1272–1281 (2008).
19. Ikeda, S. *et al.* Tunnel magnetoresistance of 604% at 300 K by suppression of Ta diffusion in CoFeB/ MgO/ CoFeB pseudo-spin-valves annealed at high temperature. *Appl. Phys. Lett.* **93,** 082508 (2008).
20. Fukami, S., Suzuki, T., Ohshima, N., Nagahara, K. & Ishiwata, N. Micromagnetic analysis of current driven domain wall motion in nanostrips with perpendicular magnetic anisotropy. *J. Appl. Phys.* **103,** 07E718 (2008).
21. Sathe, V. S. *et al.* Resonant-clock design for a power-efficient, high-volume x86-64 microprocessor. *IEEE J. Solid State Circuits* **48,** 140–149 (2013).
22. Koyama, T. *et al.* Observation of the intrinsic pinning of a magnetic domain wall in a ferromagnetic nanowire. *Nat. Mater.* **10,** 194–197 (2011).
23. Emori, S., Umachi, C. K., Bono, D. C. & Beach, G. S. Generalized analysis of thermally activated domain-wall motion in Co/Pt multilayers. *J. Magn. Magn. Mater.* **378,** 98–106 (2015).
24. Currivan, J. A. *et al.* Polymethyl methacrylate/hydrogen silsesquioxane bilayer resist electron beam lithography process for etching 25 nm wide magnetic wires. *J. Vac. Sci. Technol. B* **32,** 021601 (2014).
25. Piotrowski, S. *et al.* Conductive atomic force microscopy of small magnetic tunnel junctions with interface anisotropy. *IEEE Trans. Magn.* **99,** 1 (2015).
26. Emori, S., Bauer, U., Ahn, S.-M., Martinez, E. & Beach, G. S. Current-driven dynamics of chiral ferromagnetic domain walls. *Nat. Mater.* **12,** 611–616 (2013).
27. Faulkner, C. C. Artificial domain wall nanotraps in $Ni_{81}Fe_{19}$ wires. *J. Appl. Phys.* **95,** 6717 (2004).
28. Donahue, M. J. & Porter, D. G. OOMMF User's Guide, Version 1.0. Interagency Report NISTIR 6376. *National Institute of Standards and Technology.* Available at http://math.nist.gov/oommf (1999).

29. Vanhaverbeke, A. Spintevolve. (IBM Research, Zurich, 2008) http://www.zurich.ibm.com/st/magnetism/spintevolve.html.
30. LTSpice v. 4 (Linear Technology, 2014).
31. Evarts, E. R. *et al.* Spin transfer torque switching of magnetic tunnel junctions using a conductive atomic force microscope. *Appl. Phys. Lett.* **95,** 132510 (2009).

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Author contributions

J.A.C.-I. designed the experiment, fabricated the devices and performed the measurements and analysis. S.S. assisted with fabrication and testing. S.D. contributed to the measurement set-up and assisted with analysis. E.R.E. grew the thin films. J.Z. and D.B. contributed to the measurement set-up. C.A.R. and M.A.B. designed the experiment, planned and supervised the project and contributed to the analysis.

Additional information

Supplementary Information accompanies this paper at http://www.nature.com/naturecommunications

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