An 11-bit 20-MSample/s pipelined ADC with OTA bias current regulation to optimize power dissipation

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Abstract— **This paper presents a pipeline analog to digital converter (ADC) consisting of five stages with 2.5 effective bit resolution. Several techniques were combined for the reduction of the power consumption and to preserve the converter linearity. To reduce the power consumption, the circuit has two scaled operational transconductance amplifiers (OTAs), which are shared by the first four pipeline stages. The last fifth stage is a single decoder with 2.5 effective bits. Each OTA includes additional circuitry to adapt the power consumption according to the stage that uses the OTA. This technique changes the bias current depending on the stage in operation. The ADC was optimized to obtain 11-bit resolution with frequencies from 1 kHz to 10 MHz. The technology used to simulate the ADC is a 3.3 V 0.35 μm CMOS process and the circuit consumes 17.9 mW at 20 MSample/s sampling rate. With this resolution and sampling rate, it achieves 67.28 dB SNDR and 10.88 bit ENOB at 0.1 MHz input frequency. The Figure of Merit is 0.473 pJ/step.**

Keywords—Analog-to-digital converter (ADC); pipeline; CMOS; OTA; op-amp sharing; low power

I. INTRODUCTION

The fast development of portable electronic devices which employ wireless data and video protocols requires the use of mixed signal circuits, and specifically analog to digital converters with low power consumption. Thus, power reduction becomes an essential specification in these circuits. Regarding pipelined ADCs, several techniques have been developed to reduce the power dissipation. They are basically classified in two main types, though. Reducing the power dissipation of the operational amplifiers is the first approach. This can be achieved by exploiting stage scaling techniques [1], where switched capacitor (SC) circuits in each stage are determined by noise requirements. It has been proven that thermal noise contribution of a given stage is reduced by the previous stage gain. In this way, the capacitor size in that stage is reduced. The other technique is based on amplifier sharing

between adjacent ADC stages working in opposite clock phases [2]. This allows a reduction of one half in the number of amplifiers and a theoretical reduction on the whole circuit power dissipation. However, the bias current required by amplifiers during the sampling phase is different from that required when they are working on the amplification phase. Thus, this technique cannot be considered totally optimal because a conventional operational transconductance amplifier (OTA) cannot be optimized for both stages at the same time. For this reason, the second adjacent stage that is sharing the OTA is normally oversized in power consumption. In [1] a technique to solve this problem is proposed employing parallel OTA scaling. However this technique requires to increase the number of OTAs in each stage. This work proposes an alternative technique to adapt the power consumption of the shared OTA to the requirements of each stage. Thus, by applying this technique a better Figure of Merit (FoM) can be reached.

The rest of the paper is organized as follows. Section II describes the proposed circuit and an architecture of OTA with adaptative bias current. Results from post extracted simulations are shown in Section III. Finally, conclusions are drawn in Section IV.

II. CIRCUIT IMPLEMENTATION

Fig. 1 shows the structure of a five stage pipeline ADC. Each single stage has a resolution of 2.5 bits and the last stage is a flash ADC. From all these stages a raw code of 15 bits per sample is obtained and after applying digital processing through the Redundant Signed Digital (RSD) algorithm, the final resolution of 11 bits is obtained. The circuit has two OTAs which are shared by stages 1 and 2 and by stages 3 and 4 respectively. Even and odd stages work in opposite clock signals and it takes two phases (one clock cycle) to produce an output signal.
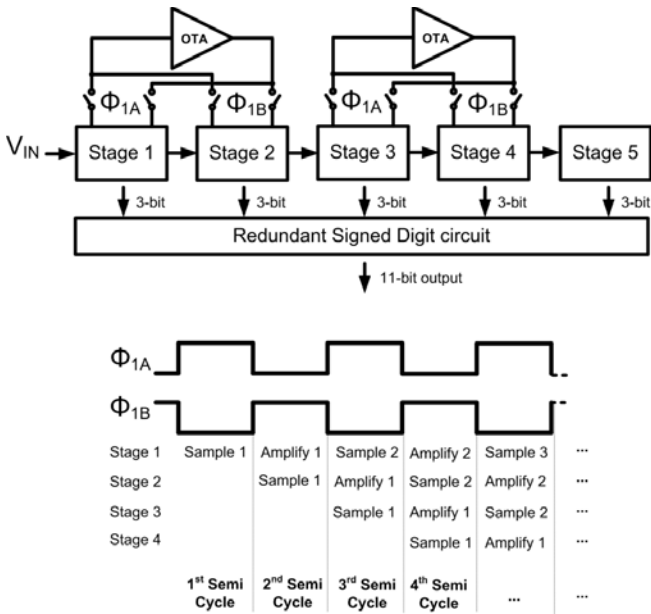
Fig. 1. *Structure of a '5 stages pipelined ADC with shared OTA between adjacent stages.*

The circuit includes transmission gates (TG) driven by clocks ϕ_{1A} and ϕ_{1B} working in opposite clock phases. So, each stage alternatively samples and amplifies its respective input.

A. Amplifier sharing

Fig. 2 shows a simplified structure of two stages sharing a two input OTA (Fig 2.a). In order to clarify the figure, it represents single ended circuits, although the real converter has been synthesized using a fully differential configuration to improve the common mode rejection ratio (CMRR). As it has been previously mentioned, each stage works in two semicycles. The conversion starts during the first semicycle. Capacitors Cs_1 and Cf_1 are charged with the input value V_{IN}. This input value is also taken to the analog comparators which feed the decoder (DEC). This decoder yields the 3-bit stage digital output (D_2, D_1, D_0). During the second semicycle, this voltage value is amplified according to:

$$V_{OUT} = 4V_{IN} + DVref \qquad (1)$$

where D={-3,-2,-1, 0, 1, 2 ,3}.

It is during this amplification that the OTA is used. The output value V_{OUT} is transferred to the input of stage 2, which samples this value by charging capacitors Cs_2 and Cf_2. Moreover the 3-bit digital output (D_5, D_4, D_3) is worked out. During the third semicycle, the value stored in Cs_2 and Cf_2 is amplified according to (1). Again, the OTA is used to perform this amplification.

Due to the requirements of the ADC, a telescopic OTA with gain boosting [3] is employed. This topology provides a high DC-gain, a high unity gain bandwidth and a fast settling time. Other topologies are susceptible to be used, though.
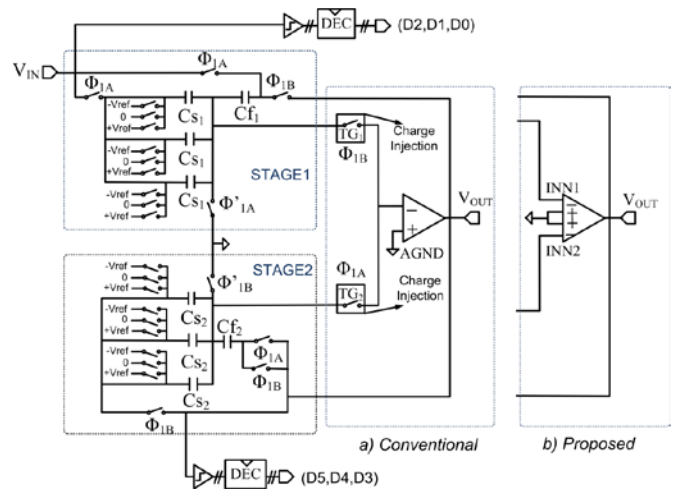

Fig. 2. *Two stage ADC with a shared single-ended OTA. a) Conventional amplifierusing an OTA with a differential pair. b) Proposed amplifier using an OTA with two differential pairs and bias regulation.*

The main disadvantage of the configuration shown in Fig. 2.a, is that when a conventional OTA with a differential pair is used, extra transmission gates connected to the inputs of the OTA are needed. This causes the shared OTA to consume the same power no matter the stage that is using the OTA. Furthermore, the TGs connected to the input of the OTA add charge injection. This causes non-linearity that affects the SNDR of the ADC.

This paper proposes a modification of the topology shown in Fig. 2.a (conventional) removing the transmission gates TG1, TG2 and replacing the conventional OTA by a four input one with bias regulation (Fig. 2.b). Moreover this new configuration also reduces the charge injection effects.

B. Four-input OTA with bias regulation

Fig. 3 shows the structure of the four input OTA with bias regulation. Each pair of inputs drives a differential pair (M11 or M13). Since each CMOS differential pair will be used in different phases (sampling phase or amplification phase), this will allow a better size fitting of the transistors according to the load capacitor and stage resolution. Three subcircuits are added to this circuit with respect a conventional four input OTA. The main one is the additional branch composed by devices M16 and M17 to drive the bias current in parallel to the existing device M19. The other two added subcircuits in Fig. 3 comprise, respectively, devices M20-M22 and devices M21-M23. These are required to keep the total bias current in the upper PMOS devices (M22, M5, M6 and M23) equal to the bias current in M17 and M19. Also, a second CMFB circuit is added in order to achieve a fast regulation of the common mode voltage.

When a given stage is sampling V_{IN}, signal ϕ_{1B} is low and signals ϕ_{1A} and $\overline{\phi}_{1B}$ are high. So, the differential pair M11A-B is disabled. The current mirrors formed by the transistors (M14-M17) and (M1-M22-M23) are also disabled and the bias current flows through M15 and M19 (Fig. 3.b).
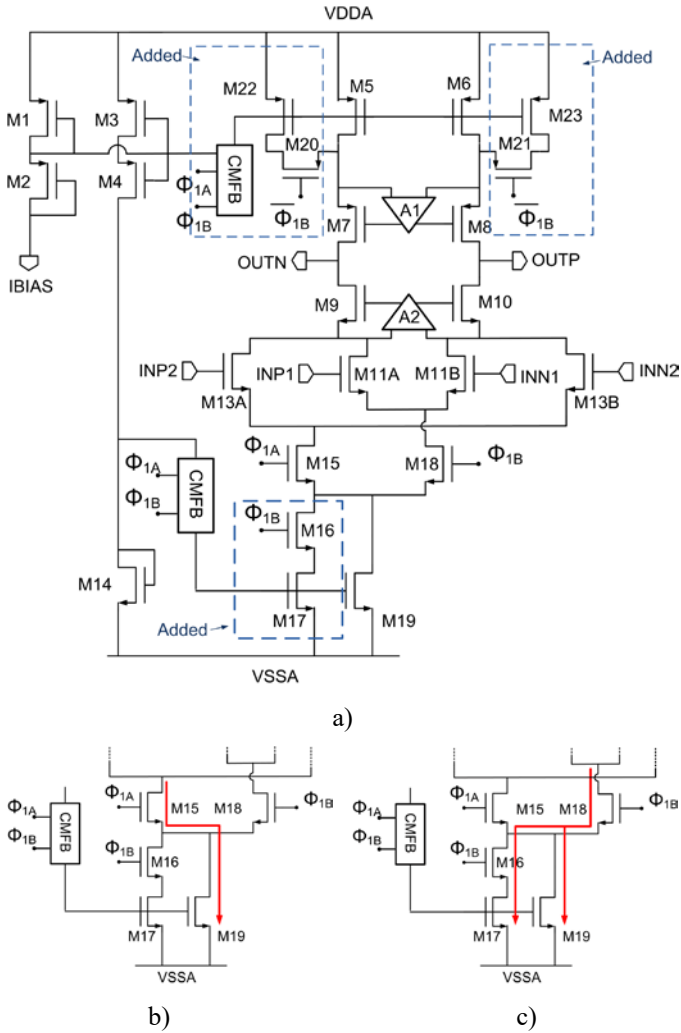
Fig. 3. *Four inputs OTA with CMFB and adaptive current consumption circuitry. a) Structure b) bias current during sampling phase c) bias current during amplification phase*

In the next semicycle, when the stage is amplifying, signal ϕ_{1B} is high while ϕ_{1A} and $\overline{\phi}_{1B}$ are low. Thus, the differential pair M13A-B is disabled allowing the two common mode feedback circuits (CMFBs) to regulate the common mode with the maximum bias current and consequently obtain the highest slew rate. In this case, the bias current flows through M18 and M16 and M17 in parallel to M19 (Fig. 3.c).

Thus, by means of the transistor M16, M18, M15, M20 and M21, the OTA adapts the power consumption to the requirement of the active stage. This technique is better than abruptly switching on and off the OTA bias current, because this last option has a negative impact on the circuit dynamic behavior. In addition, since the control signals of these devices (ϕ_{1A}, ϕ_{1B}, $\overline{\phi}_{1B}$) are the same as the control signals used in the CMFB circuits, a completed synchronization can be ensured. As all these changes are synchronized with the CMFBs and the clock signal Φ_{1A}, Φ_{1B}, Φ_{2A} and Φ_{2B}, the regulation of CMV is done with high precision and speed.
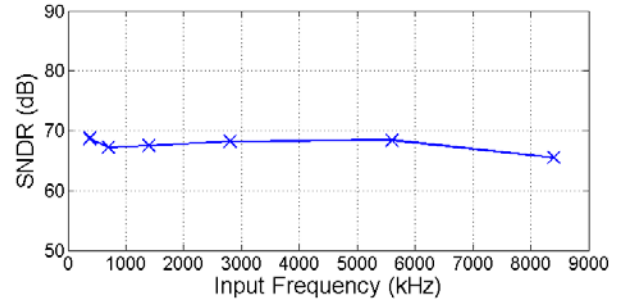

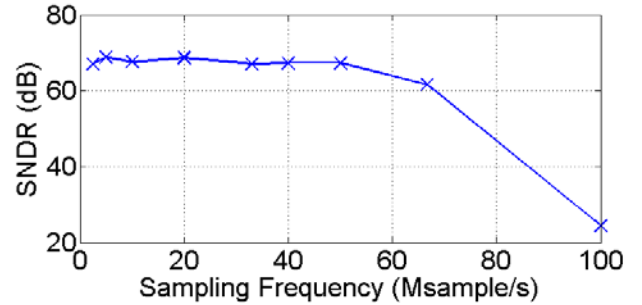Fig. 4. *Dynamic performance of the ADC versus input frequency at FS of 20MS/s.*

Fig. 5. *Dynamic performance of the ADC versus sampling frequency at FIN of 375kHz.*

III. SIMULATION RESULTS

The ADC has been developed in a 0.35 µm CMOS process from AMS. The area occupied including PADs is 1.85x1.55 mm^2. Figs. 4 and 5 show the SNDR obtained at schematic level simulations versus input and sampling frequencies. In both simulations the SNDR remains above 67.1 dB. It shows a slight decay for F_{IN}=8.4 MHz and a stronger worse behavior above 60 Ms/s sampling rates. The SNDR was calculated using the IEEE-STD-1241 4-parameters sine wave test. At this sampling rate and input frequency the ADC reached a value of 66.7 dB for typical means simulation that included parasitic resistors and capacitors and PADs circuitry.

The power dissipation and FoM of the converter were obtained from parasitic extracted simulations. The power consumption was 17.87 mW for a 3.3V DC power supply with a sampling frequency of 20 MSample/s and input frequency of 100 KHz.

The FoM defined in (2) under these conditions was 0.436 pJ/step.

$$FoM = \frac{Power}{F_s \cdot 2^{ENOB}} \quad (2)$$

The overall ADC performance is summarized in Table I and is compared with other circuits. The IEEE test gave as result a maximum and minimum error of +0.7 and -0.61 LSB respectively. The residual errors obtained from the sine wave test are shown in Fig. 6.a.

Fig. 6.b shows results from Monte Carlo simulations with process variation and mismatch for the SNDR. The results show a SNDR centered over 67.5 dB and a deviation of ±3 dB.

SNDR was also evaluated through corner simulations made according to the AMS foundry recommendations. Different values of power supply voltage and working temperature were combined with different parameter of the devices. Table II shows the obtained results for this simulation. The lower value obtained for this parameter was 64.23 dB.

Regarding the value of the bias current, its value through devices M17 and M19 of the first and second OTA of the circuit are, respectively, 2.7 mA and 1.6 mA. The first one requires more power because of the stage scaling technique applied.

The OTA with adaptative current allows the reduction of the bias tail current of OTA1 and OTA 2 by 24% and 45%, respectively (Fig. 7).

TABLE I.   SUMMARIZED PERFORMANCE OF THE PIPELINED ADC

Parameter	This work	[1]	[4]	[5] [a]
Technology (μm)	0.35	0.18	0.35	0.18
Area (mm²)	2.26 with PADS	1.99	4.8x4.3	0.93
Supply Voltage (V)	3.3	1.8	3.3	1.8
Resolution (bit)	11	12	12	12
Sampling Rate (Fs) (MS/s)	20	20	20	50
Power (mW)	17.85	36	56.3	21.6
SNDR@(F_{IN}) (dB)	67.28 (100kHz)	66.2 (1MHz)	41.3 (590kHz)	60.6 (60MHz)
ENOB@(F_{IN}) (Bits)	10.87 (100kHz)	10.7 (1MHz)	12.1 (47kHz)	
FoM (pJ/Step)	0.473	1.75	0.78	0.49
Input Voltage Dyn. Range (Vpp)	3	1.2	2	1.5

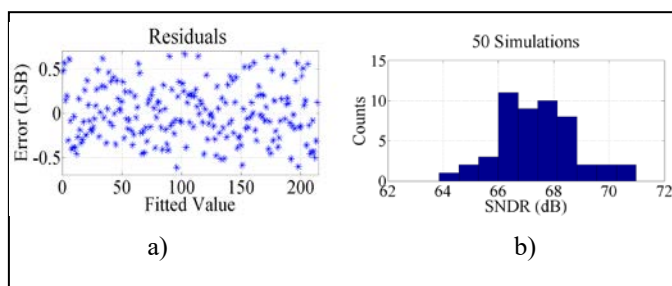a. Performance without calibration

Fig. 6. a) Residual error for F_{IN}=100 kHz b) Monte Carlo for 50 iterations for F_{IN}=100 KHz
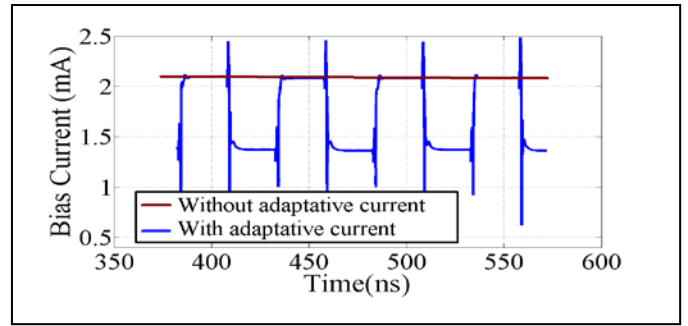

Fig. 7. *Bias current per stage in first OTA1 with and without adaptive current consumption circuitry*

TABLE II.   CORNER SIMULATIONS. TM: TYPICAL MEAN, WP: WORSE POWER, WS: WORSE SPEED, WZ: WORSE ZERO, WO: WORSE ONE. AMS AG

Corner	1	2	3	4	5	6	7
Capacitor	WP	WS	WS	WP	WS	WP	WS
Resistor	WP	WS	WS	WP	WS	WP	WS
CMOS	WP	WS	WS	WO	WO	WZ	WZ
Temp(ºC)	10	10	45	10	45	10	45
VDD [V]	3.4	3.2	3.2	3.4	3.2	3.4	3.2
SNDR	69.25	66.43	69.19	66.49	64.23	67.65	65.64

IV.   CONCLUSION

An alternative power optimization technique of pipelined ADC that uses the OTA sharing technique is presented. Adapting the OTA power consumption to the requirement of each stage reduces the power consumption of the entire pipeline ADC and thus improving the FoM. For this ADC, FoM and power consumption were improved by 13.5%. The ADC has also improved the FoM compared to other circuits developed in 0.35 μm and 0.18 μm technologies.

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