NS-SRAM: Neighborhood Solidarity SRAM For Reliability Enhancement of SRAM Memories

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***Abstract*—Technology shift and voltage scaling increased the susceptibility of Static Random Access Memories (SRAMs) to errors dramatically. In this paper, we present NS-SRAM, for Neighborhood Solidarity SRAM, a new technique to enhance error resilience of SRAMs by exploiting the adjacent memory bit data. Bit cells of a memory line are paired together in circuit level to mutually increase the static noise margin and critical charge of a cell. Unlike existing techniques, NS-SRAM aims to enhance both Bit Error Rate (BER) and Soft Error rate (SER) at the same time.**

Due to auto-adaptive joiners, each of the adjacent cells' nodes is connected to its counterpart in the neighbor bit. NS-SRAM enhances read-stability by increasing critical Read Static Noise Margin (RSNM), thereby decreasing faults when circuit operates under voltage scaling. It also increases hold-stability and critical charge to mitigate soft-errors. By the proposed technique, reliability of SRAM based structures such as cache memories and register files can drastically be improved with comparable area overhead to existing hardening techniques. Moreover it does not require any extra-memory, does not impact the memory effective size, and has no negative impact on performance.

I. Introduction

Single Event Upsets (SEUs) result from a voltage transient event induced by alpha particles from packaging material or neutron particles from cosmic rays [1]. This event is created due to the collection of charge at a p-n junction after a track of electron-hole pairs is generated. A sufficient amount of accumulated charge in the struck node may invert the state of a logic device, such as a latch, a static random access memory (SRAM) cell, or a logic gate, thereby introducing an error into the hit circuit. In the past technologies, this issue was considered for a small set of applications in which the circuits are operating under aggressive environmental conditions like aero-space applications. Nevertheless, shrinking the transistor size and reducing the supply voltage in new technologies result in a remarkable decrease of the capacitance per transistor. Less robust bits plus higher chip density, results in more vulnerability of chips against soft errors.

Hence, SEUs become a challenging limitation of reliability in CMOS circuits, especially for memories. Moreover, the Semiconductor Industry Association (SIA) roadmaps indicate that embedded memories will constitute more than 90% of the chip area in the next few years [2]. Consequently, the overall system reliability will considerably be affected by the memory immunity to errors. During the last decade, more and more industrial and academic efforts have been devoted to radiation hardening and error mitigation. For example, since 2010 NASA Electronic Parts and Packaging (NEPP) has been focusing on radiation induced issues and this topic a regular conference [3]. Another example is the Radiation Hardening-by-Design (RHBD) developed by Boeing Company [4]. Despite the numerous published works, SRAM reliability enhancement is still an open problem, especially for new technologies.

Other than radiation, noise and manufacturing variations are other causes for memory failure, which are intensified by technology shrinking or inevitable voltage scaling techniques. Stability of SRAM cell is a critical design parameter against such threats. Specifically, Static Noise Margin (SNM) is the traditional metric for measuring stability in SRAM cell. By definition, it is the maximum tolerable simultaneous DC noise on both CMOS inverter's inputs. Any stronger noise will flip cell value. Bit Error Rate (BER) is a metric widely used for SRAM failure rate. Static noise margins, particularly in read operation, highly influence this metric [5].

We propose, NS-SRAM, a circuit-level technique to enhance both stability and soft error resilience of SRAM memories. More specifically, this technique improves SRAM error mitigation by increasing the cell resistance to external events. Our approach exploits data in adjacent cells to mutually harden both bits against errors. Due to auto-adaptive joiners, each of the adjacent cells' nodes is connected to its counterpart in the neighbor bit. Thereby, every adjacent bits couple support each other's reliability without sacrificing from memory capacity. SPICE simulations show that NS-SRAM almost doubles the 6T SRAM cell critical charge with acceptable access power overhead and negligible performance cost. Moreover, critical read static noise margin (RSNM) is doubled on average, which this leads to dramatic BER improvement, especially in lower Vdd values.

This paper makes the following key contributions:

- We propose a new SRAM cell architecture, where adjacent cells of SRAM mutually harden one other by a joiner.
- We implement an adaptive joiner that connects a pair of nodes in a cell.
- We implement a flexible and an autonomous controlling mechanism to configure the coupling joiners in adjacent cells.

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- We achieve hardening without any change in SRAM decoder or higher layers of the system.

The rest of the paper is organized as follows: Section II provides a background on the SRAM architecture and the soft error mechanism followed by an overview of related works dealing with bit error rate and soft error mitigation in SRAM memories. The suggested architecture of NS-SRAM is given in Section III. Section IV details the experimental results. Finally, we conclude in Section V.

II. Background and Related Work

Single port six-transistor cell (6T) and other multi-port variants are prevalent SRAM memory cells built using a storage element and two or more access transistors. Register file and different levels of cache memories are most important parts inside any modern processor which are based on SRAM memories. Figure 1 shows a standard 6-T SRAM: the stored data is determined by the state of nodes S1 and S2. The storage nodes are driven by a pair of cross-coupled inverters and are accessed through two NMOS transistors (see Figure 1).

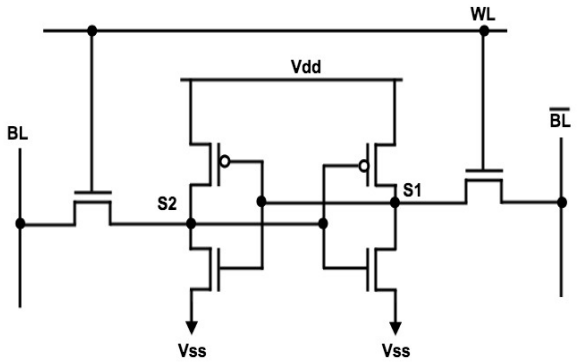

Fig. 1. Standard 6T-SRAM cell architecture, usually used in cache memories

A particle strike induces the generation of electrons and holes that are collected at the opposite voltage terminals of the reverse-biased junction. Hence, electrons move towards positive voltage and holes move towards negative voltage [6] and a current pulse appears in the struck node due to the movements of charges. Consequently, if a particle-induced current appears in one of the cell's sensitive nodes (S1 or S2), it may propagate through the struck inverter and cause a transient noise on the second sensitive node. This will cause the second node to propagate the corrupted value, thereby flipping both nodes and consequently, flipping the state of the bit stored in the SRAM cell. The minimum charge required to flip the cell is called the critical charge (Q_c) [7]. Therefore, a soft error occurs when the charge resulting from the electron-hole pairs induced by an ionizing particle, and collected at a junction, is greater than the hit node's critical charge. There are numerous works which focused on soft error mitigation to limit SER in SRAMs.

Architecture level error resilience techniques like Error Correcting Codes (ECCs) have been proposed and widely used [8]. The simplest form is the parity check method whose major weakness is its inability to correct the detected errors [9]. Another form of ECC used in memories is the SECDED (single error correction, double errors detection) [10]. The main problem of the SECDED is its area overhead and the supplementary latency leading to performance loss. This negative point is more pronounced in register files, where performance is an essential requirement. Therefore, while effective for cache memories, generally ECC is not considered as a reliability solution in register files. A multi-copy cache (MC^2) has been proposed in [11] to create a fault tolerant memory, where authors exploit the cache area by multi redundant lines in order to detect the possible faults and correct them by a majority vote. On the other hand, a fault tolerant architecture presented in [12] combines both parity and single redundancy to enhance memories' reliability. In [13], 2-D matrix codes (MC) have been proposed to efficiently correct soft errors per word with a low delay. A combination of ECCs and a circuit level hardening technique is presented in [14]. The main weakness of these techniques is their area, power, and delay overheads due to the additional memory cells and supporting circuits required for error detection and correction.

Circuit level techniques have also been proposed to overcome architecture level overheads. These techniques enhance soft error resilience in SRAM cells either by slowing down the response of the circuit to transient events, or by increasing its Q_c. Upsizing the memory cells' transistors increases the effective capacitance of the device and thus Q_c is also increased. This Q_c increment can make the cell less less susceptible to particle strikes [15]. However, as it is shown in [16], the gain in cell robustness depends on the exact transistors that are upsized. Authors in [17] propose a circuit level technique that aims to enhance both Bit Error Rate (BER) and Soft Error rate (SER) due to auto-adaptive joiners, each of the adjacent cells? nodes is connected to its counterpart in the neighbor bit. Other methods such as [18] suggest to harden the cell using a pass transistor that is controlled by a refreshing signal. The authors of [19] add a redundant cross-coupled inverter to the 6T-SRAM to increase the cell critical charge. In [20] the authors proposed a quad-node 10-T memory cell which uses negative feedback to prevent memory bit flip. In [21], a 11-T single ended memory cell has been proposed to enhance soft error tolerance using refreshing mechanisms. Based on hysteresis effect of Schmitt trigger, [22] proposes a hardened 13-T memory cell. However, this technique slows down the memory due to Schmitt trigger's hysteresis temporal characteristics. A modified hardened memory cell (RHM-12T) is proposed in [23] using 12 transistors.

Enhancing the robustness of SRAM structure against instabilities which mainly are due to process variation in deep sub-micron technologies have also been explored [**?**]. In these works increasing the noise margins, especially critical Read Static Noise Margin (RSNM) is addressed [5] to reduce

memory Bit Error Rate (BER) which is an important metric for fault rate of memories.

While SRAM reliability studies usually aim at tackling one of two problems: reducing SER or BER, in this work we propose a technique to address both problems at the same time. The next section details the proposed NS-SRAM cell design.

III. NS-SRAM: Neighborhood Solidarity SRAM

A. Architecture

Our approach tries to improve reliability of SRAM-based memories by exploiting adjacent cell values to mutually harden both bits. Two previous works, 7T/14T cell [25] and JSRAM [26], applied transistor level coupling technique to build more reliable SRAM cells. These techniques' main limitation is the loss in available memory capacity due to data redundancy in different cells. Moreover, they both require modifications to SRAM decoder for generating signals to activate/deactivate joining cells. In the former, one data bit is stored in two memory bits to have more robustness, whereas in the latter, one data bit is stored inside four memory bits to have error immunity and error correction. This paper suggests a fundamental contribution to overcome the aforementioned limitation. In fact, NS-SRAM circuit level hardening is achieved without memory capacity sacrifice and without additional bits. We exploit an intrinsic characteristic of SRAM cells that consists of the availability of both data and its complement within each cell nodes: S1 and S2 in Figure 1. Hence, instead of "occupying" adjacent bits to store the same redundant data, our technique proposes a regardless-value coupling. This is possible due to an adaptive joiner that connects a cell's node to its pair within the adjacent SRAM.

In fact, based on a flexible and autonomous controlling mechanism, the coupling configuration changes automatically depending on values stored in adjacent cells; If both cells store similar data (0-0 or 1-1), the two S1 nodes are joint together. The same happens for S2 nodes for both cells. However, in case of different values (0-1 or 1-0), S1 is joint with adjacent S2 and vice versa. The similarities are detected dynamically using an XOR gate and cells are coupled according to detected similarities. The main reason why this technique works is that the coupled nodes with the same value, electrically support each other if any instability threatens one of them. In order to have rational area overhead, the granularity of join operation is chosen as two bits.

It's with noting that NS-SRAM is a pure circuit-level technique which does not affect the higher layers. Operating system or compiler are totally oblivious to its existence. Therefore, it does not impose any strict requirements on higher system layers. Additionally, it requires no change in decoder of SRAM structure.

In order to take advantage from the simultaneous writing operation through the same word line (WL), the SRAM cells are in a horizontal organization. In fact, using vertical coupling of memory bits is not possible by activating more than one WL at once. Moreover, simulations show that the write operation on a single cell can affect the other one easily. Hence, NS-SRAM is applied horizontally within the same SRAM row (see Figure 4).

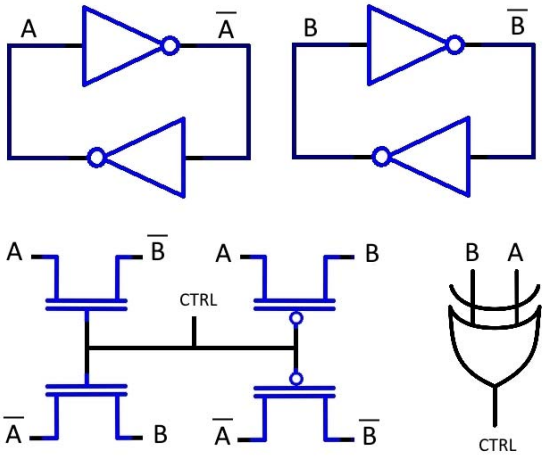

Fig. 2. NS-SRAM without showing access transistors of two SRAM cells. Depending on values stored in top and bottom cells, either NMOS or PMOS switches are activated to connect similar values one another.

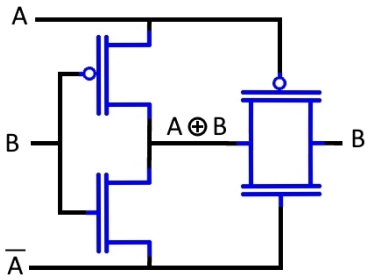

Fig. 3. Implementation of XOR gate with four transistors.

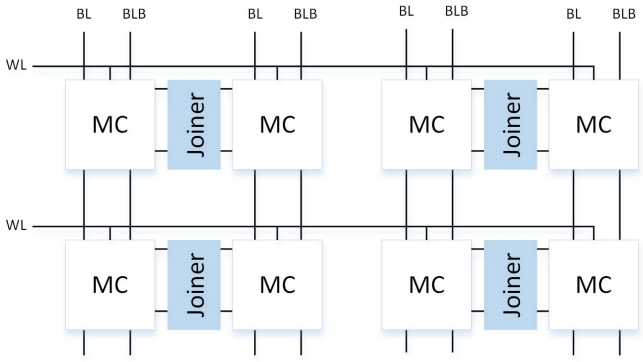

Fig. 4. NS-SRAM structure is composed of: two normal SRAM cells and joiner in between them. The rest of the system is oblivious to joiner existence. No change to memory decoder is required. Note that BL stands for Bit Line, BLB: Bit Line Bar, and WL for Word Line.

B. Write Operation

Due to the horizontal architecture of NS-SRAM (Figure 4), both bits are written simultaneously on the same word line. Therefore, the write mechanism is exactly like a normal write operation in conventional SRAM memory. In such a scenario, there is no need to modify the memory decoder. Since write data is pushed on both cells strongly, values are written easily and there is no major resistance against it. As illustrated in Figure 5, simulation shows that write time is not significantly affected, confirming the characteristics of a regular write operation.

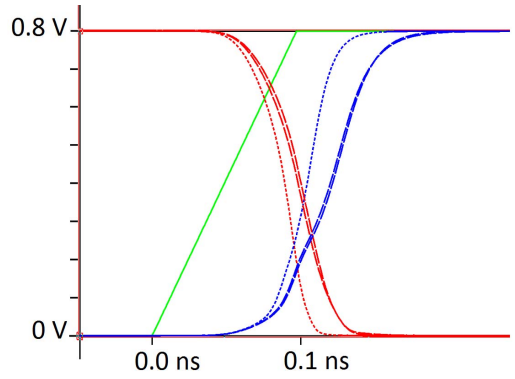

Fig. 5. Write operation: there is no major change in write time. Green: rising edge of word line(WL), solid red-blue: A and $\overline{A}$ nodes of normal SRAM cell, Dotted red-blue: A and $\overline{A}$ nodes of NS-SRAM for symmetric and asymmetric values.

C. Read Operation

The time taken by the read operation is not affected by NS-SRAM. In fact, the proposed architecture does not apply any change to cell storage elements and related components.

IV. Experimental Results

A. Setup

Simulations were performed in HSPICE simulator with 22nm predictive technology model library [27]. Transistor sizes for typical 22nm SRAM cell were chosen from [26]. In this section, first, we evaluate employing various types of elements as joiner circuit and show the improvement obtained in read and hold SNM. Second, enhancement in critical charge is explained.

B. Noise Margins

Noise margin is the traditional metric for evaluating SRAM cell stability. For calculating noise margins, we applied conventional methods that use two sources of identical DC noise between two inverters of victim SRAM cell. Based on this setup, we performed DC simulation to test the effectiveness of our approach [5]. In our circuit, two sources of noise are inserted between inverters of cell A, i.e. between node A and $\overline{A}$ as illustrated in Figure 2.

In the case of critical Read-SNM, as depicted in Figure 6, there is a considerable improvement in RSNM value due to

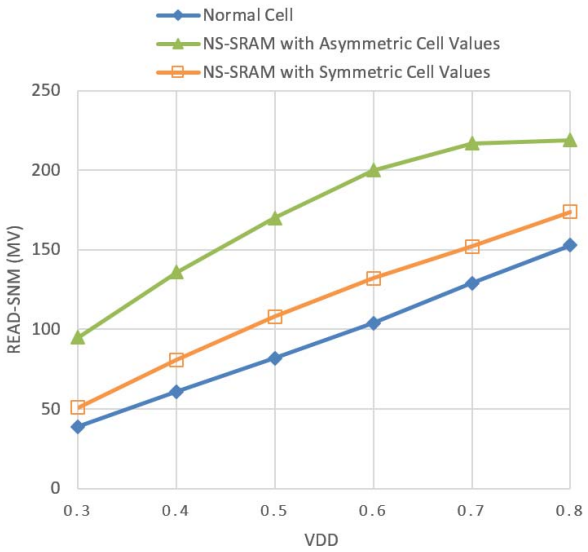

Fig. 6. Read Static Noise Margin (RSNM) of normal 6T-SRAM cell vs. NS-SRAM cell. RSNM of NS-SRAM depends on stored value.

NS-SRAM. Obviously, in all cases, bigger transistors provide better connectivity and better results. They require, nevertheless, more area. We used transistor sizes same as [26]. Our next set of experiments investigate the hold stability of our design. As shown in Figure 7, our approach improves Hold-SNM values. However, improvements are not as high as Read-SNM.

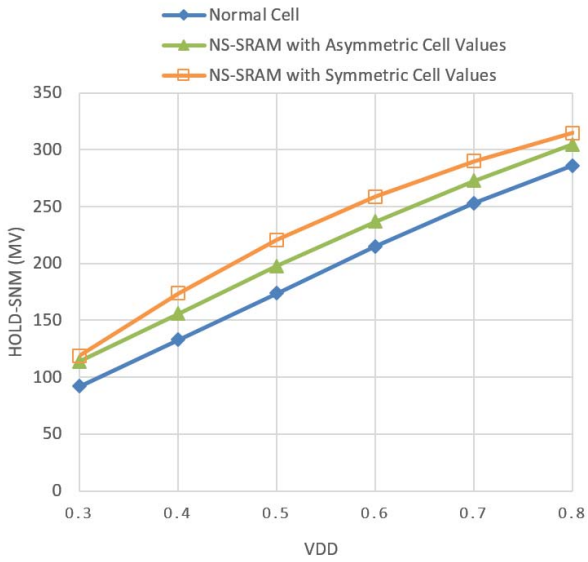

Fig. 7. Hold Static Noise Margin (HSNM) of normal 6T-SRAM cell vs. NS-SRAM cell. HSNM of NS-SRAM depends on stored value.

C. Critical Charge

The Q_c of a memory cell is the minimum charge collected due to a particle strike which results in a bit flip. Therefore,

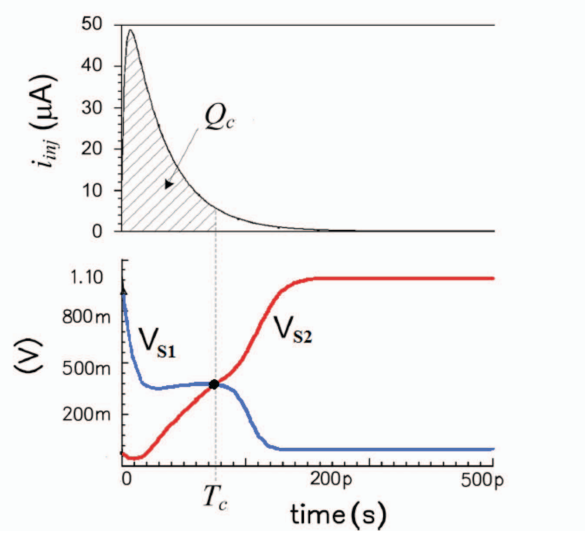

Fig. 8. Graphical definition of critical charge. V_{S1} and V_{S2} are node S1 and S2 voltages, referencing Fig 1.

the vulnerability of SRAM cells to soft errors is typically estimated based on its critical charge, Q_c [6]. The SER by cell decreases exponentially with the Q_c increase as shown in Equation 1 below [28]:

$$SER = K \times \phi \times A \times \exp\left(-\frac{Q_c}{Q_s}\right). \quad (1)$$

In this expression, K is a proportionality constant, ϕ is the neutron flux with energy greater than 1MeV, A is the sensitive area of the circuit and Q_s is the charge collection efficiency of the device in fC.

In our experiments, we determine Q_c by injecting current pulses into the sensitive nodes of the memory cell. These pulses simulate the current induced by the particle strike. To calculate Q_c, we determine the minimum magnitude and duration of an injected current pulse that is sufficient to flip the data in the memory cell. Hence, Q_c is determined by integrating the current pulse corresponding to the smallest charge injected that flips the memory cell. Figure 8 graphically illustrates the quantification of the cell's Q_c. The critical time (T_c) is the time between the beginning of the current pulse and the intersection between the two cell node voltages. As shown in [20], we assume that once the memory cell reaches the state where "t=T_c", the feedback between the cell nodes becomes strong enough to result in an erroneous stable state by flipping the initially stored data. Therefore, the injected charge below Tc is sufficient to flip the state of the cell and the critical charge is equal to the charge injected by the current pulse up to t=T_c:

$$Q_c = \int_0^{T_c} i_{inj}(t)dt \quad (2)$$

In the above expression, $i_{inj}(t)$ is the current pulse injected into the sensitive node to simulate the SEU.

Hence, we monitor the cell behavior under particle strike by observing its HSPICE simulation results. To highlight the reliability enhancement performed by NS-SRAM architecture, we use the critical charge as an indicator of the memory cell resistance to particle strikes. We performed HSPICE analysis to determine NS-SRAM's critical charge at nominal voltage which corresponds to 0.8V for 22nm and track its behavior under voltage scaling. Figure 9 shows the critical charge of NS-SRAM compared with 6T-SRAM in terms of supply voltage.

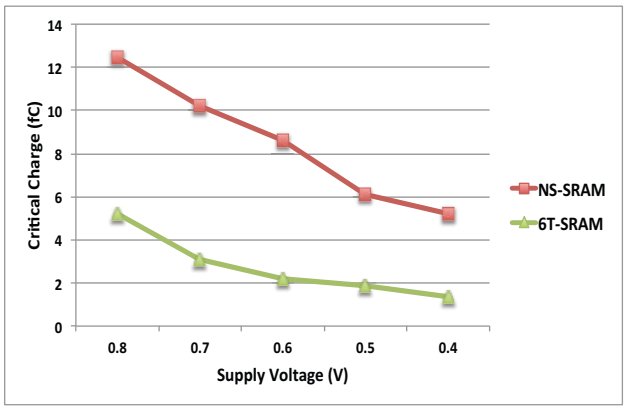

Fig. 9. Critical charge versus supply voltage for NS-SRAM and 6T-SRAM

Results presented in Figure 9 show that when VDD=0.4V (scaled down by 50%), NS-SRAM critical charge is almost equal to the standard SRAM's Q_c when operating under its nominal voltage.

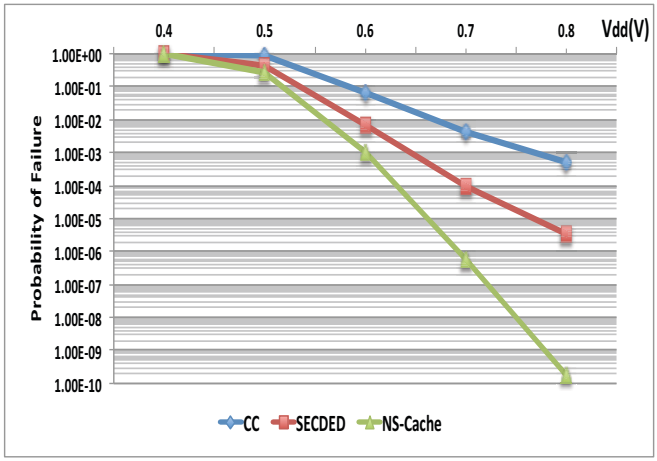

Fig. 10. Probability of failure (POF) vs VDD for a 16KB cache using SECDED cache, CC, and NS-SRAM-based cache for a given area

D. Architecture-level Reliability

In order to study the reliability of an NS-SRAM-based memory, we compare the probability of failure (POF) of a 16KB 4-way set associative cache implemented in different technologies: conventional cache (CC) based on 6T-SRAM

cells, a cache protected by SECDED (single error correction, double errors detection) [10] and an NS-SRAM-based memory. Let us assume that:

- N is the number of SRAM cells in a cache memory.
- $p(V)$ is probability of failure of each 6T-SRAM cell at voltage V.
- $p_{NS}(V)$ is probability of failure of each NS-SRAM cell at voltage V.

The POF of a conventional cache can be as:

$$P_{cc} = 1 - (1 - p(V))^N \tag{3}$$

The POF of an NS-SRAM-based memory, $P_{NS-mem}(V)$, can be expressed as:

$$P_{NS-mem}(V) = 1 - (1 - P_{NS}(V))^N \tag{4}$$

Figure 10 shows the POF comparison between the different technologies implementing a 16KB 4-way set associative cache memory. In order to perform a fair comparison, we test with the same area for all three technologies. $SECDED$ results are based on HSPICE simulation with PTM [27] models. As shown in this Figure, a cache memory using NS-SRAM cells carries out better reliability enhancement than SECDED for equal area. Moreover, unlike SECDED that needs additional circuitry to detect and correct errors, NS-SRAM-based memory performs significant error probability reduction without changing the memory architecture.

V. Conclusion

In this paper, we propose NS-SRAM, a new memory cell architecture to protect SRAM bits from soft errors and instabilities. At circuit level, the proposed architecture exploits adjacent memory cells data to mutually increase cells critical charge and static noise margin to reinforce the storage elements resistance to bit flips. Results show that NS-SRAM has the advantage of maintaining a reasonable reliability level even at lower supply voltage levels. Moreover, we demonstrated that NS-SRAM-based cache memory shows lower probability of failure compared to SECDED under equal area.

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