



Monitoring the operation of a graphene transistor in an integrated circuit by XPS



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ABSTRACT

One of the transistors in an integrated circuit fabricated with graphene as the current controlling element, is investigated during its operation, using a chemical tool, XPS. Shifts in the binding energy of C1s are used to map out electrical potential variations, and compute sheet resistance of the graphene layer, as well as the contact resistances between the metal electrodes. Measured shifts depend on lateral positions probed, as well as on polarity and magnitude of the gate-voltage. This non-contact and chemically specific characterization can be pivotal in diagnoses.

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1. Introduction

After the discovery of the two-dimensional honeycomb structured carbon about a decade ago, colossal academic activity has been witnessed around a single or few-layers of graphene. [1,2] Even a greater activity has also been devoted to the technological developments in terms of incorporation of graphene to the existing and well-developed infra-structure. [3–6] For characterization of the materials involving graphene, and more importantly, the devices fabricated from them, in addition to electrical, chemical characterization is also needed. In that respect, most of the commonly utilized optical techniques can only give indirect information about the electrical properties sought. [7–14] Similarly, information derived using the conventional and powerful electron spectroscopic techniques, like Auger (AES), Ultra-Violet (UPS), and X-ray (XPS) photoelectron spectroscopies are also indirect, when it comes to electrical properties. [15–19] However, under appropriate conditions, all of the electron spectroscopic techniques are capable of reflecting local electrical potentials developed, intentionally or not, on the analyzed material or the device, since such potentials are embedded into the measured kinetic energy of the ejected

electrons. Accordingly, difference between the obtained binding energy and the tabulated one gives the chemically-addressed local electrical potential, which has been extensively utilized by our group and others to harvest electrical information, difficult to obtain by other methods. [20–23] Using this methodology, we have previously reported on analyses of a device using graphene as the resistive sheet between the two electrodes, [20] and in another device where the graphene layer was operated in the back-gated transistor geometry. [21] The present work extends it to analyze one of the transistors of the 64 elements of an IC-device, where C1s binding energy position is measured with lateral resolution to probe and map-out electrical properties of the transistor. Investigation of a single element out of the 64, is presented as “a proof of principle”, since extension to the others are straightforward.

2. Experimental details

A picture of the device together with a survey XP spectrum of a graphene-only region is given in Fig. 1(a), where the dominating O1s feature belongs to the SiO₂ substrate, since probe depth is about 10 nm, but the C1s peak has the peak position of graphene at 284.7 eV. We synthesize single layer graphene on an ultra-smooth copper foil (purchased from Mitsui mining and smelting company, LTD, B1-SBS) by using a chemical vapor deposition (CVD) system connected to a vacuum pump. We heat up copper foils to 1035 °C

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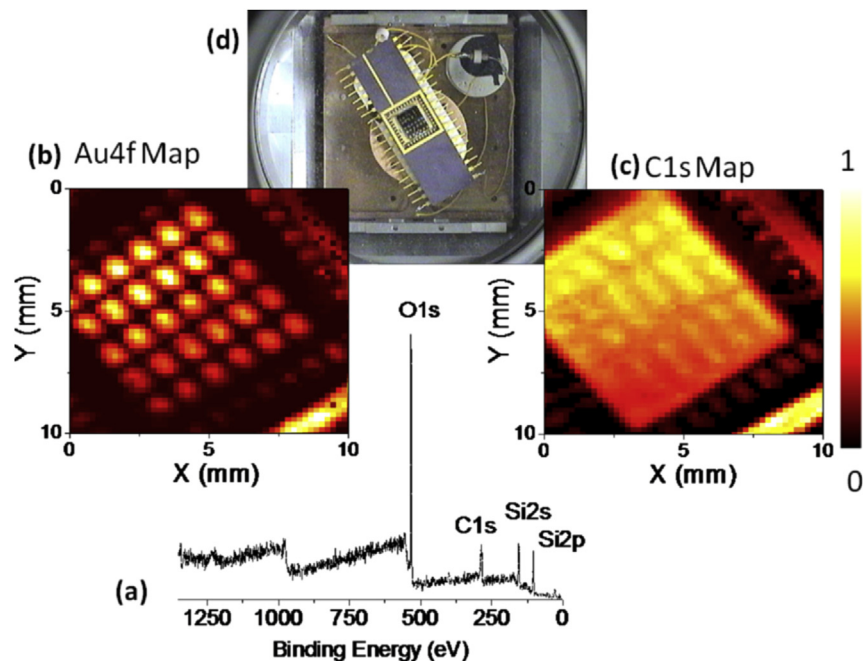


Fig. 1. (a) A survey XP spectrum recorded from the graphene-only part of one of the transistors. Areal intensity maps of the entire IC recorded in the snap-shot mode with 200 μm X-ray spot size and 200 μm steps of; (b) Au4f, and (c) C1s. (d) Picture of the IC inserted into the load-lock of the instrument.

under 100 sccm H_2 flow. We, then, grow graphene by flowing 10 sccm CH_4 to the chamber for 1 min at that temperature. The partial pressures of the H_2 and CH_4 are 1.5 Torr and 3 Torr, respectively, during the growth process. We cool down the chamber at a rate of 10°C/s to room temperature, while 100 sccm H_2 flows. To transfer graphene on SiO_2 substrates, we first coat the copper foil with the Shipley 1806 resist and dry them by annealing overnight at 80°C . Then, we etch the graphene grown copper in FeCl_3 aqueous solution. After washing and drying the resist-graphene stack, we put it on SiO_2 substrate and heat the resist-graphene- SiO_2 stack at 70°C for 2 min and at 120°C for 20 s. This process ensures that the resist-graphene stack perfectly sticks to the SiO_2 surface. We dissolve the dry resist with acetone and finally obtain a graphene transferred on SiO_2 substrate. To fabricate back-gated graphene transistors on Si^+/SiO_2 substrate, we evaporate 50 nm Au for source and drain contacts to the graphene. After isolating each transistor channel with a reactive ion etching (RIE) process, we evaporate 5 nm-Ti and

100 nm-Au to extend the area of source and drain contacts.

Mechanically strong metal contacts are required for wire-bonding. The fabricated transistors used in this work have 0.5 mm channel width and 1.0 mm channel length. Schematic drawing of the fabricated transistors is shown in Fig. 2(a). To measure the electrical performance of the fabricated transistors, we use HP-4153 probe station.

3. Results and discussion

We apply -1 V bias between the source and drain electrodes and measure the current as a function of the gate voltage, shown in Fig. 2(b). The result of the electrical-only measurements indicates the Dirac point to be near 0 V , and other Current-Voltage characteristics are depicted in Fig. 2(c). The calculated field effect mobility of the device used in this study is around 820 and $600\text{ cm}^2/\text{V}$ for holes and electrons, respectively (see the [Supplementary](#)

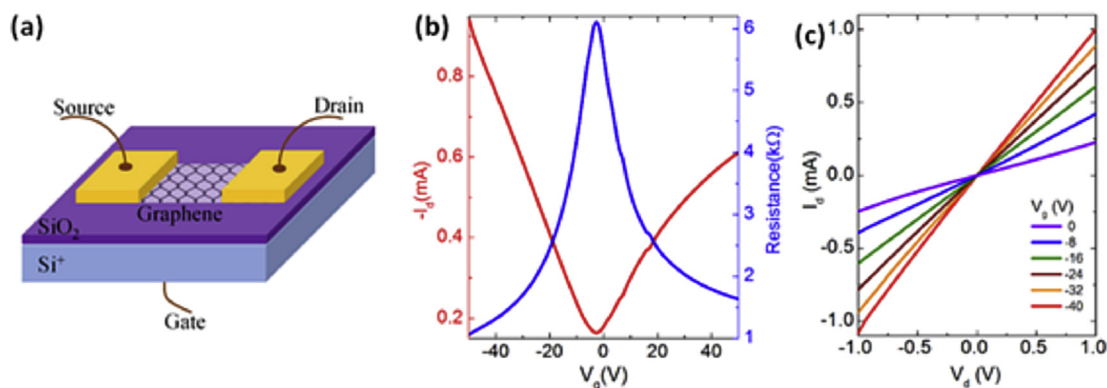


Fig. 2. Electrical characterization of graphene transistors. (a) Schematic drawing of a back-gated graphene transistor is shown. (b) Transfer curve of one of the graphene transistors as a function of back gate voltage. Red line shows the drain current with an applied bias of -1 V and blue line shows the corresponding resistance of graphene as a function of the gate voltage. (c) Output curves of one of the transistor as a function of bias with varying gate voltages. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

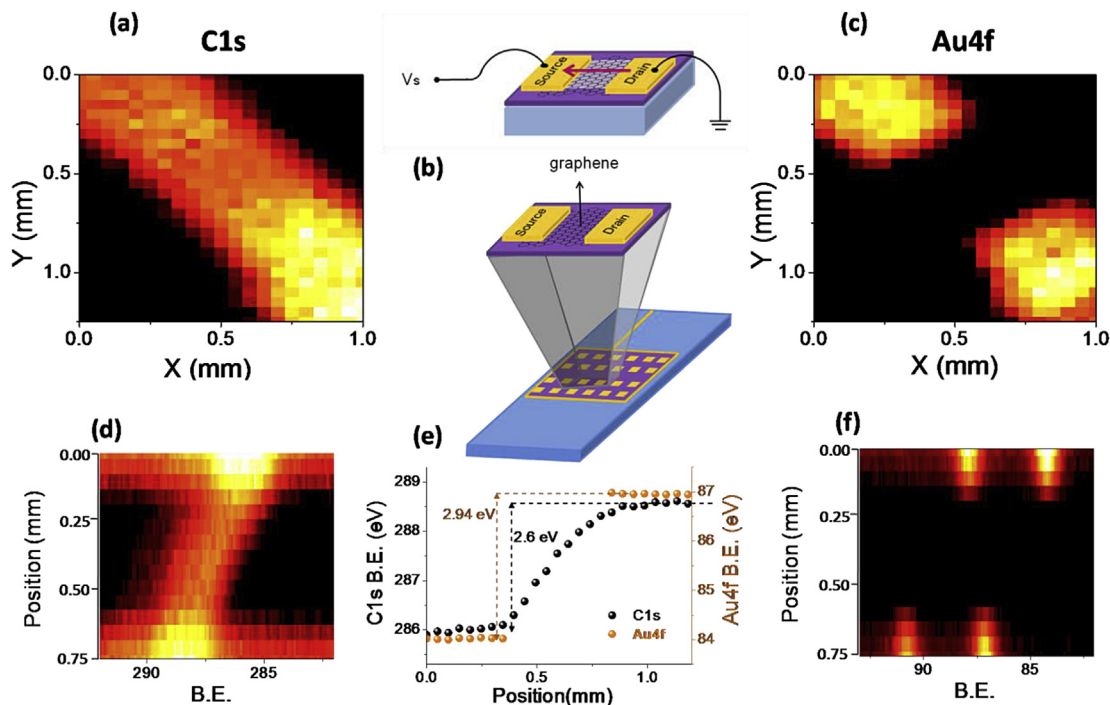


Fig. 3. XPS data of one of the transistors recorded with $50\ \mu\text{m}$ X-ray spot size and $50\ \mu\text{m}$ steps; (a) Areal intensity maps of C1s, and (c) Au4f peaks. A schematic representation of zooming to a single transistor connected in the source-drain configuration while the gate is grounded is displayed in (b). Spectra recorded in the line-scan mode are shown in (d) and (f), while the binding energy positions of the C1s and Au4f_{7/2} are displayed in (e).

Information (SI) section and Fig. S1), where the mobility is calculated using the maximum transconductance of the device. Once the integrity of the transistors has been established by electrical measurements, further contacts are attached for XPS characterization, a picture of which was given in Fig. 1. The entire IC is inserted into the analysis chamber of the Thermo Fisher K-Alpha X-ray photoelectron spectrometer, which uses monochromatic AlK α ($h\nu = 1486.6\ \text{eV}$) as the excitation source. Some of the measurements are done only in the source-drain, while the other in the source-drain-gate geometry. Therefore, the instrument is modified to provide two external voltage biases, where one is used as the source and the other as the gate, while the drain is grounded. Using the intensity of the O1s peak of the substrate and the C1s of graphene from the survey spectrum of the graphene-only region shown in Fig. 1, it is possible to estimate the thickness of the graphene layer as $\sim 1.1\ \text{nm}$. Computational details are given in the SI section.

In Fig. 1, areal intensity (computed area) maps of the entire IC recorded in the snap-shot mode with $200\ \mu\text{m}$ X-ray spot size and $200\ \mu\text{m}$ steps are also shown for the Au4f and C1s peaks. Since the probe depth of XPS is about $10\ \text{nm}$, gold electrodes and also the gold wire connections are easily identified, while carbon is everywhere. It is also possible to record the data with smaller spot size ($50\ \mu\text{m}$) of and steps ($50\ \mu\text{m}$), and zooming to only one of the transistors, as shown in Fig. 3, where the intensity of the C1s and Au4f are shown as areal maps (a) and (c). In the same Figure the peak positions are shown as regular scanned spectra recorded in the line-scan mode with inherently better precision in (d) and (f), while a $+3\ \text{V}$ bias is applied to the source electrode, and both the drain and the gate are grounded.

The extracted binding energies are shown in Fig. 3(e) for both peaks as a function of lateral position, and the actual spectra are reproduced in the SI section as Fig. S3. The binding energy of the Au4f_{7/2} peak, which is commonly used as a reference, is $84.00\ \text{eV}$,

and it is exactly what is measured at the grounded electrode. However, it is measured as $86.94\ \text{eV}$ at the source, yielding a difference of $2.94\ \text{eV}$ which reflects faithfully the applied voltage bias of $+3\ \text{V}$, within the precision of our measurements. The measured difference in the position of the C1s peak across the electrodes is less precise and is $2.6\ \text{eV}$, i.e. $0.3\ \text{eV}$ less. This small but significant difference can be attributed to the contact resistance(s) between the graphene and the gold electrodes, since application of $3\ \text{V}$ causes a sizable current of $\sim 2.6\ \text{mA}$, passing between the metal electrodes, consistent with the geometry of the graphene layer. The contact resistance, especially in devices with smaller dimensions is known to adversely affect the performance. [24–30] Therefore, location, as well as information related with its chemical nature is highly desirable. Besides the conventional electrical-only measurements, Kelvin probe force microscopy is the only other tool which can locate and quantify contact resistance(s), [27] but again it, too, falls short when it comes to chemical specificity. Hence use of XPS for this purpose is very unique.

In order to harvest the effect of gating, instead of applying a voltage bias, a current bias needs to be imposed, since the gate is the current controlling element of the circuit, which requires two biases. That is what is implemented for the data shown in Fig. 4, where a constant voltage bias of $+3\ \text{V}$ is applied to the source through a precision $1\ \text{k}\Omega$ series resistor, and a second variable voltage bias is applied to the gate, while grounding the drain, as schematically shown in the same figure. Here again, the voltage drop across the gold electrodes, as well as the potential variations through the graphene sheet, under three different gate voltages, are measured through the positions of the Au4f_{7/2} and C1s peaks, respectively, which are given in Table 1. Using these data together with a simple equivalent circuit model, both the sheet as well as the contact resistances can be obtained for all 4 different operational conditions of the transistor, in an all non-invasive fashion (details are given in the SI section). The values obtained are consistent with

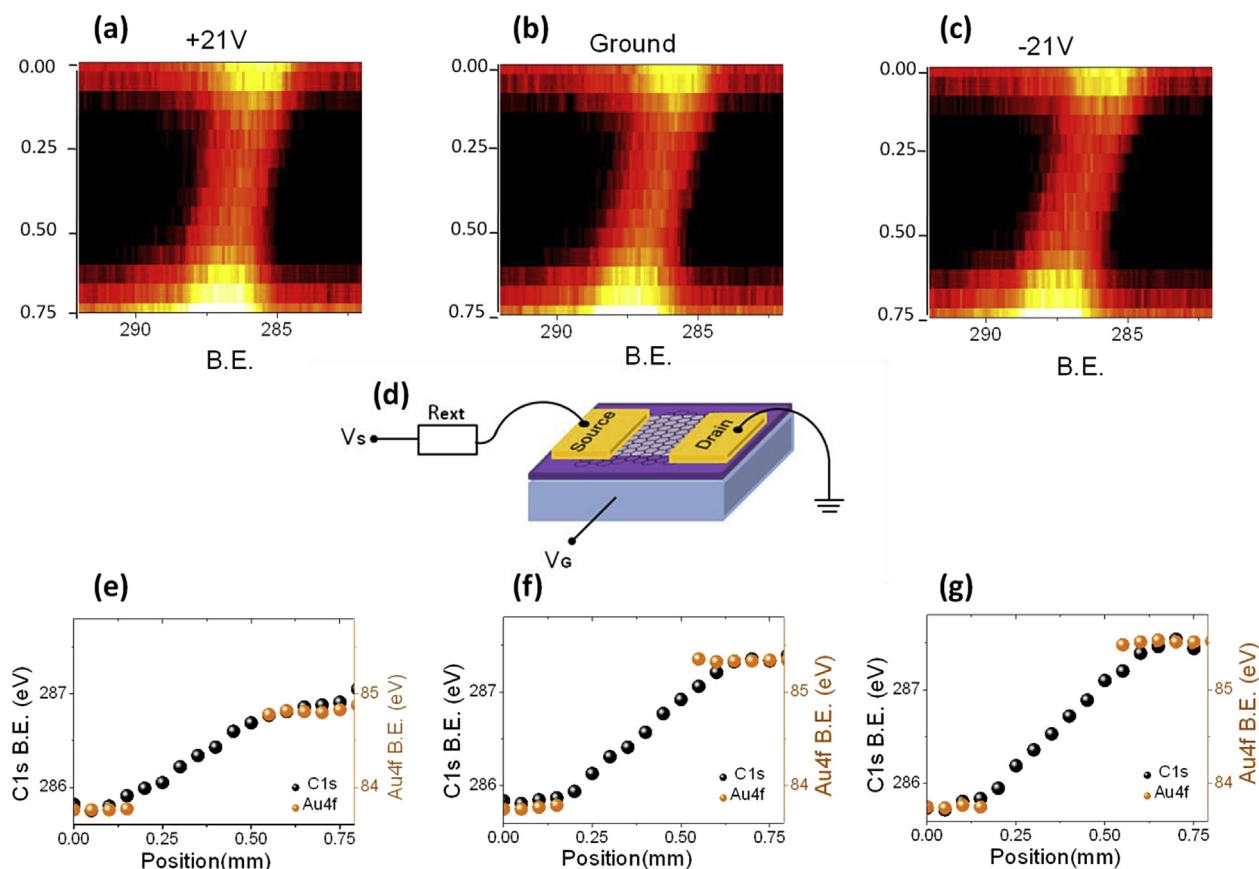


Fig. 4. XP spectrum of C1s recorded in the normal line-scan mode of the transistor under +3 V bias applied through a 1 k Ω series resistor, while the transistor is gated from the bottom with; (a) +21 V, (b) 0 V, and (c) –21 V. (d). A schematic representation of the electrical connections. (e), (f), and (g) are the measured binding energy positions of the C1s and Au4f_{7/2} for the corresponding data in (a), (b), and (c).

Table 1

Measured binding energies of Au4f_{7/2} and C1s peaks for the four different operational conditions of the graphene transistor. Computed electrical parameters are also given. Details of which are given in the SI section.

	Gate (V)	B.E. (Au4f _{7/2}) (eV)			B. E (C1s) (eV)			Sheet resistance (Ω)	IR drop (eV)	Contact resistance (Ω)
		S	D	Δ	S	D	Δ			
No gating (+3 V Bias)	–	86.94	84.00	2.94	287.5	284.9	2.6	1020 (1.2 k Ω /sq)	0.34	130 (52 k $\Omega\mu$ m)
+3 V over 1 k Ω Series Resistor	0	85.57	84.00	1.57	286.2	284.8	1.4	1020 (1.2 k Ω /sq)	0.17	120 (48 k $\Omega\mu$ m)
	+21	86.12	84.00	1.12	285.8	284.8	1.0	550 (0.6 k Ω /sq)	0.12	65 (26 k $\Omega\mu$ m)
	–21	86.75	84.00	1.82	286.5	284.8	1.7	1550 (1.6 k Ω /sq)	0.12	65 (26 k $\Omega\mu$ m)

our previous electrical-only measurements, [29] and also with reported ones. It must also be stressed that extracted values of the transistor using XPS, as given in Table 1, differs from those depicted in Fig. 2 using electrical means. Such a difference is common since, the XPS measurements are performed in vacuum, in the absence of air and humidity, whereas the electrical measurements are carried out in air ambient, and the position of the Dirac point can deviate significantly between the two diverse conditions.

4. Conclusions

In summary, through application of electrical bias, XPS is shown to be able to extract electrical parameters of an isolated graphene-based transistor of a 64-element IC during its operation in a chemically specific and non-contact fashion.

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Appendix A. Supplementary data

Supplementary data related to this article can be found at <http://dx.doi.org/10.1016/j.orgel.2016.06.027>

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