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A charge inverter for III-nitride light-emitting diodes

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In this work, we propose a charge inverter that substantially increases the hole injection efficiency for InGaN/GaN light-emitting diodes (LEDs). The charge inverter consists of a metal/electrode, an insulator, and a semiconductor, making an Electrode-Insulator-Semiconductor (EIS) structure, which is formed by depositing an extremely thin SiO_2 insulator layer on the p^+-GaN surface of a LED structure before growing the p-electrode. When the LED is forward-biased, a weak inversion layer can be obtained at the interface between the p^+-GaN and SiO_2 insulator. The weak inversion region can shorten the carrier tunnel distance. Meanwhile, the smaller dielectric constant of the thin SiO_2 layer increases the local electric field within the tunnel region, and this is effective in promoting the hole transport from the p-electrode into the p^+-GaN layer. Due to the improved hole injection, the external quantum efficiency is increased by 20% at 20 mA for the $350 \times 350\,\mu m^2$ LED chip. Thus, the proposed EIS holds great promise for high efficiency LEDs. © *2016 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4945257]

Replacing incandescent and fluorescent light sources, III-nitride based light-emitting diodes (LEDs) are expected to make significant contribution in relieving the global warming effect as a result of their energy saving feature if used at world scale.[1] However, in order to increase the saving in energy consumption and the scale of their use, there is room for further boosting their external quantum efficiency (EQE). One of the bottlenecks that hinder further enhancement of the quantum efficiency for III-nitride LEDs is the limited hole injection into the quantum wells.[2] The hole injection efficiency into the multiple quantum wells (MQWs) is affected by various factors, including the inhomogeneous hole concentration in the quantum wells, the blocking effect caused by the p-electron blocking layer (p-EBL), and the hole transport from the p-electrode to the p^+-GaN region. The non-uniform hole distribution that often takes place in the MQWs leads to a strong hole accumulation in the quantum wells close to the p-GaN side.[3] The hole injection can be homogenized by doping the quantum barriers with Mg acceptors,[4,5] using the InGaN instead of the GaN as the quantum barriers,[6] properly reducing the quantum barrier thickness,[7] increasing the thickness of the quantum well close to the p-GaN layer[8] and/or employing the cascaded active region.[9] As is well known, the p-EBL is adopted in the III-nitride LEDs to reduce the electron leakage, which nevertheless also blocks the hole injection due to the band offset between the p-EBL and the subsequent p-GaN layer.[10] Therefore, different p-EBL structures have been reported to increase the hole injection, such as the superlattice p-EBL[11] and staircase p-EBL.[12] Recently, the AlGaN/GaN/AlGaN p-EBL with a very thin GaN insertion layer is proposed where the valence subbands in the thin GaN insertion layer can significantly reduce the p-EBL barrier height for holes.[13] The p-EBL blocking effect can also be suppressed by making holes "hot"[14] and/or increasing the hole concentration in the p-GaN layer through a hole modulator.[15] Last but not the least, the hole injection is also substantially impacted by the p^+-GaN and the p-electrode. Considering the low Mg activation efficiency,[16] it is very difficult to shorten the width of the surface depletion region in the p^+-GaN layer, and this can cause the negative effect on the hole injection. In this work, we propose a charge inverter by growing a very thin SiO_2 insulator on the p^+-GaN surface, and the p^+-GaN surface will present a weak inversion layer when the device is biased. The weak inversion layer can reduce the tunnel region width, and in the meanwhile, compared to the p^+-GaN, the smaller dielectric constant of the SiO_2 layer also produces a stronger electric field, which can further promote hole injection. Most importantly, such a charge inverter can reduce the forward voltage and increase the quantum efficiency of the LED device. In addition, the charge inverter can be easily fabricated without increasing the fabrication complexity.

The physical mechanism of the proposed charge inverter for promoting the hole injection from the p-electrode into the p^+-GaN layer is illustrated in Fig. 1. We use ITO as the current spreading layer, which is a heavily doped n-type semiconductor. For device A in Fig. 1(a) that does not have the charge inverter, the p^+-GaN/ITO behaves as the p^+-GaN/

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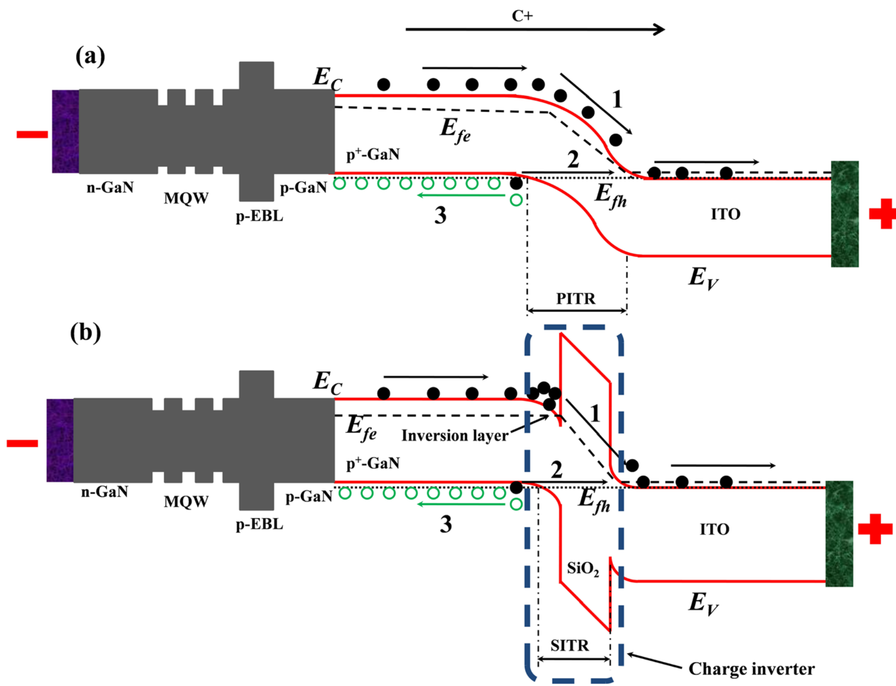

FIG. 1. Schematic energy band diagrams (layer thickness not in scale) for (a) device A without the charge inverter and (b) device B with the charge inverter. The carrier transport includes three processes: process 1 means the nonequilibrium electrons (solid circles) travel to the ITO layer from the conduction band of the p^+-GaN layer, process 2 means the electron interband tunneling which then simultaneously produces the holes (open circles), and the holes will then travel (process 3) to the MQW region. The charge inverter and the inversion layer are also shown in Fig. (b). E_C, E_V, E_{fe}, and E_{fh} represent the conduction band, valence band, quasi-Fermi level for electrons, and quasi-Fermi level for holes, respectively.

ITO tunnel region (PITR). Device B with the charge inverter is demonstrated in Fig. 1(b), from which we can see the inserted insulator between the p^+-GaN and the ITO layer, and we call this semiconductor-insulator tunnel region (SITR). Under forward-bias, the electrons will tunnel through the PITR and SITR for device A and device B, respectively, and then the holes are left and injected into the MQW region. The advantage of the SITR design is the formation of the weak inversion layer at the p^+-GaN/insulator interface when the device is forward-biased [see Fig. 1(b)]. The inversion layer is able to attract and confine the electrons at the p^+-GaN/insulator interface. This can then substantially shorten the width of the tunnel region, which can significantly increase the carrier tunnel efficiency.[17] Meanwhile, if the dielectric constant of the insulator is smaller than the GaN and the ITO layers, the electric field within the tunnel region can also be significantly enhanced, which is very useful to further facilitate the hole injection.

The effectiveness of the charge inverter in improving the LED performance is tested with blue InGaN/GaN LEDs, which were grown by the metal-organic chemical vapor deposition (MOCVD) system. The epi-wafers were initiated on the [0001] oriented planar sapphire substrate. We first grew the 20 nm thick GaN nucleation layer followed by the 4 μm thick unintentionally n-type GaN layer (u-GaN). The 2 μm n-GaN layer with the Si doping concentration of $5 \times 10^{18}\,cm^{-3}$ was achieved by the diluted SiH_4 precursor. Then, we grew the five-period $In_{0.15}Ga_{0.85}N$/GaN MQW stack in which the quantum well and the quantum barrier is 3 nm and 12 nm thick, respectively. We did not adopt any intentional dopants in the quantum barriers. The MQWs were then capped by the 25 nm thick p-$Al_{0.20}Ga_{0.80}N$ EBL structure to better confine the electrons. The holes are provided by the p-GaN layer, which was grown after the p-EBL. The thickness of the p-GaN layer is 0.2 μm. The p-type conductivity was realized by doping the epi-wafer with Mg dopants. We assume 1% as the ionization ratio for the Mg dopants, and the effective hole concentration in the p-EBL and the p-GaN layer is estimated to be $3 \times 10^{17}\,cm^{-3}$. We also grew the heavily Mg doped GaN layer (p^+-GaN) with the 20 nm thickness to enable the ohmic contact. The whole epi-wafers were finally *in situ* annealed (600 s at the temperature of 720 °C) in the N_2 atmosphere.

After the epitaxial growth, we measured the surface roughness of the p^+-GaN layer for the LED epi-wafer by the Atomic Force Microscope (AFM). The size of the scanned window is $1 \times 1\ \mu m^2$, and the scan rate is set to 1 Hz. The surface morphology for the tested LED is presented in Fig. 2, from which we can see that the surface roughness fluctuation is smaller than 1 nm. Therefore, in order to obtain the continuous film while not causing significant current blocking effect, we tentatively deposited an insulation layer as thin as 1 nm on the p^+-GaN surface.

The LED wafers were then fabricated by following the standard fabrication process. The LED epi-wafers were patterned into a mesa of $350 \times 350\ \mu m^2$ by the reactive ion etch

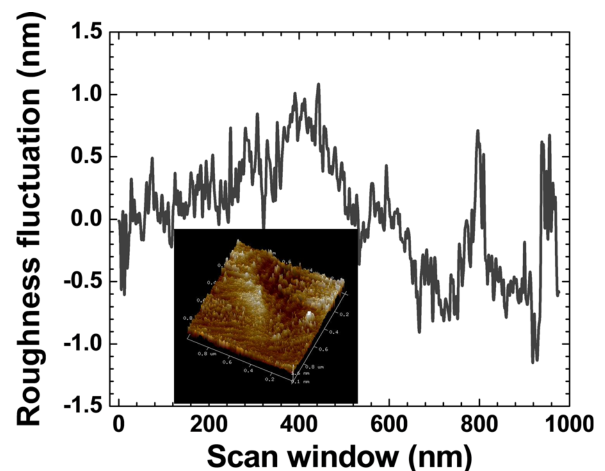

FIG. 2. The AFM image and surface roughness of the p^+-GaN layer for a complete InGaN/GaN MQW LED before depositing the insulation film.

(RIE) technology. For device A, we formed the ITO layer on the p^+-GaN layer by E-beam and the ITO layer thickness was 50 nm. For device B, before depositing the 50 nm thick ITO layer, we first grew a thin SiO_2 layer at 300 °C on the p^+-GaN surface, and the SiO_2 layer was obtained by optimizing the PECVD system and the thickness was set to ~1 nm. The thin SiO_2 layer was patterned and wet etched by using the diluted HF acid. Then, for both devices, the ITO layer was annealed in the ambient of N_2:O_2 (4:1) at the temperature of 630 °C for 1 min. We finally deposited the Ti/Au (30 nm/100 nm) metal stack on both the ITO surface and the n-GaN surface to form the p-electrode and the n-electrode.

We calculated the energy band diagrams [see Fig. 3(a), data calculated at 100 mA] in the vicinity of the PITR and the SITR for devices A and B, respectively. The numerical calculations were conducted by APSYS, which is able to solve the Poisson and Schrödinger equations self-consistently with the proper boundary conditions. The carrier transport was modeled by the carrier drift and diffusion processes. Besides the thermionic emission and field emission, we also considered the interband tunneling for the PITR and the SITR if we treat the ITO layer as the heavily doped n-type semiconductor. The piezoelectric and spontaneous polarization effect was taken into account for the [0001] oriented InGaN/GaN LEDs,[18] and here, we empirically assumed the 40% polarization level due to the strain release by generating dislocations.[5,14,15] Other important factors such as the band offset for InGaN/GaN and GaN/AlGaN heterostructures, Auger recombination coefficient, and Shockley-Read-Hall recombination can be found in our previous reports.[5,14,15]

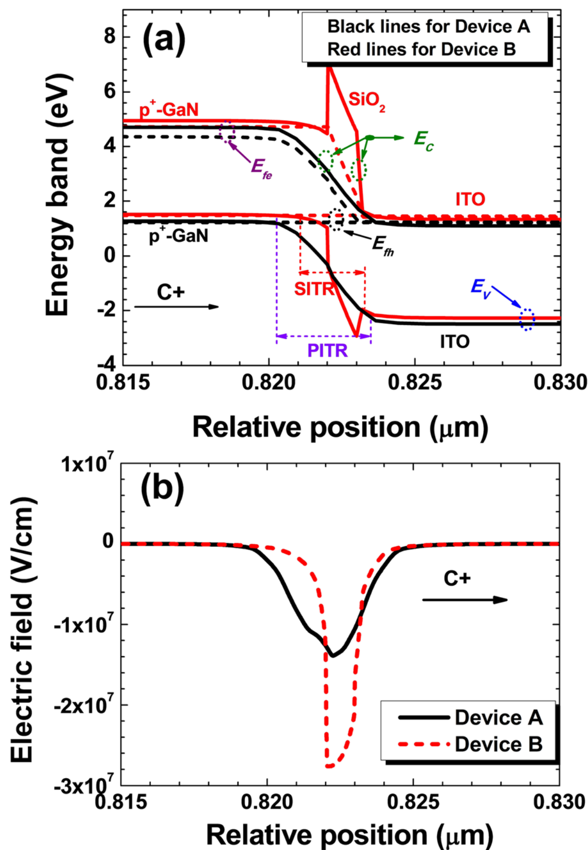

FIG. 3. Numerically calculated (a) energy band diagrams, (b) electric field profiles for the PITR and SITR at 100 mA. Here, E_C, E_V, E_{fe}, and E_{fh} denote the conduction band, valence band, quasi-Fermi level for electrons, and quasi-Fermi level for holes, respectively. The E_{fe} in (a) is higher than E_C at the relative position of 0.8214 μm, and this results in the electron accumulation and a reduced tunnel width. The positive direction of the electric field is pointed from the ITO layer to the p^+-GaN layer.

Investigations to Fig. 3(a) illustrate that the width of the SITR is substantially reduced compared to that of the PITR. The width of the PITR is ~3.5 nm while the width for the SITR is ~2 nm. Note the tunnel region width is defined as the distance between the two points at which the quasi-Fermi level for holes intersects with the valence band of the p^+-GaN layer and the conduction band of the ITO layer, respectively. The reduced tunnel width of the SITR is well attributed to the charge inverter, which enables the inversion layer at the p^+-GaN surface. The charge inversion in the SITR is evidenced by the alignment of the quasi-Fermi level (E_{fe}) of electrons and the conduction band (E_C). The E_{fe} overtakes the E_C in the energy level at the relative position of 0.8214 μm for the SITR as demonstrated in Fig. 3(a), and thus, the electrons accumulate at the interface of the p^+-GaN layer and the SiO_2 insulator. The electron accumulation shrinks the surface depletion in the p^+-GaN layer, which gives rise to the reduced width of the SITR for LED B. However, due to the lack of the SiO_2 layer, the charge inversion will not happen in the PITR as illustrated in Fig. 3(a). This leads to a wider surface depletion region in the p^+-GaN layer and makes the interband tunneling efficiency low. Meanwhile, according to our calculations, the width variation of PITR and SITR is negligible at different set biases in this work, which is consistent with the report in Ref. 17. We also show the electric field profiles for the PITR and SITR in Fig. 3(b) at 100 mA. According to Fig. 3(b), the electric field intensity for the SITR is larger than that for PITR, thanks to the lower dielectric constant of the SiO_2 layer ($\epsilon_r = 3.9$) compared to 8.9 of the p^+-GaN layer. The enhanced electric field can better promote the carrier interband tunneling efficiency of the SITR for device B.[17] Note that the SiO_2 layer thickness in the charge inverter has to be optimized and makes it properly thin. If the SiO_2 layer is too thick, the SITR will be significantly widened and this can severely block the hole injection, which leads to a poor quantum efficiency. We shall also pay attention to the dielectric constant (ϵ_r) of the thin insulator layer in the charge inverter, and a ϵ_r as low as possible is required to achieve the high electric field magnitude in the tunnel region.

We measured and calculated the device current in terms of the applied voltage (I-V) for the fabricated devices, which is presented in Fig. 4. We can see that the forward voltage of device B is smaller than that of device A, and this is ascribed to the facilitated hole injection efficiency from the p-electrode into the p^+-GaN layer for device B. Meanwhile, the increased electric field in the thin SiO_2 layer also enables a more smooth hole transport and improves the injected current. Note the experimentally measured forward voltage for both devices can be further reduced if the thermal annealing condition for the ITO layer is fully optimized.

The numerically calculated hole density profiles are illustrated in Fig. 5. Clearly, we can observe that the hole concentration in the quantum wells for device B is higher

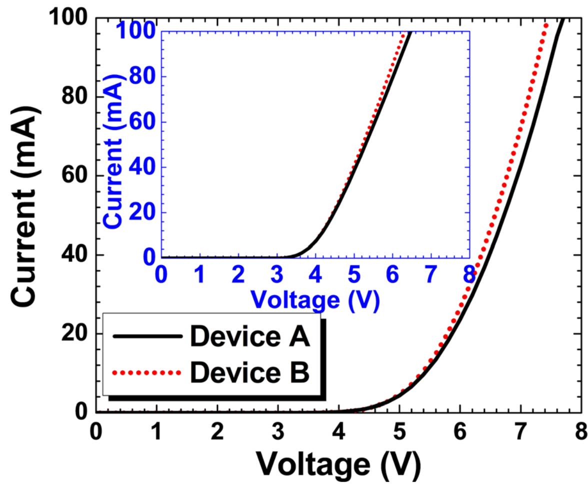

FIG. 4. Experimentally measured current-voltage characteristics for devices A and B. Inset shows the numerically calculated current-voltage characteristics for devices A and B.

than that for device A. As has been mentioned earlier, the charge inverter helps to reduce the width of the tunnel junction, and the SiO_2 layer with a lower ϵ_r increases the electric field intensity, which result in the enhanced hole transport from the p-electrode to the p^+-GaN layer, and this simultaneously increases the hole injection efficiency into the quantum wells. Since the quantum barriers in the proposed device is not engineered in the way of favoring the uniform hole distribution in the MQW region, we see the lowest hole concentration in the quantum well closest to the n-GaN side. The holes in the quantum barriers can be more homogeneously distributed by, e.g., employing the InGaN as the quantum barriers.[6]

The impact of the charge inverter is justified by measuring the optical performance for devices A and B as shown in Figs. 6(a) and 6(b), respectively. Fig. 6(a) presents the electroluminescence (EL) spectra for the two devices, for both of which the peak emission wavelength is 450 nm. Device B produces stronger EL intensity compared to device A within the tested current range. Note that, as the injection current increases, the peak emission wavelengths for both devices slightly show the blue shift that is due to the polarization screening in the quantum wells by the injected

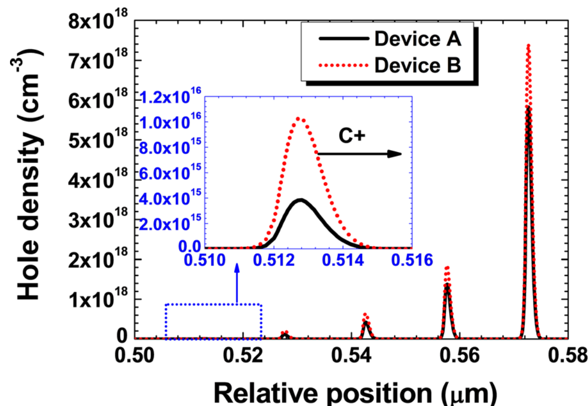

FIG. 5. Hole density profiles for devices A and B at the injection current level of 100 mA.

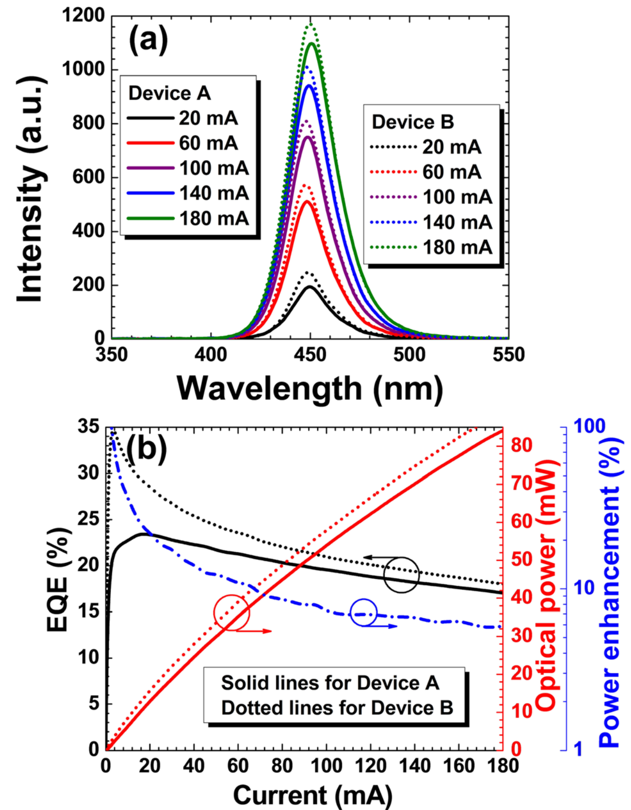

FIG. 6. Experimentally measured (a) EL spectra, (b) EQE, optical power and the power enhancement at different injection current levels for devices A and B. The mesa size for the tested devices is $350 \times 350\,\mu m^2$.

carriers, and then show the red shift that is caused by the self-heating effect. We also show the EQE and the optical power as a function of the injected current for both devices A and B in Fig. 6(b). We can see that device B has both higher EQE and optical power than device A, thanks to the promoted hole injection efficiency enabled by the charge inverter. For example, the EQE is increased by 20% at the injection current level of 20 mA for the $350 \times 350\,\mu m^2$ LED chip. However, if the current is further increased to 180 mA, the power enhancement for device B becomes less obvious, and the efficiency enhancement is smaller than 10%, such that though device B can increase the EQE, the efficiency droop is less improved, which is, for example, 27.6% for device A and 48.6% for device B at 100 mA. The observed efficiency droop for device B is likely due to the electron leakage caused by the inversion layer at the p^+-GaN/SiO_2 interface, given that more nonequilibrium holes are produced at the p^+-GaN/SiO_2 interface and the inversion layer occurs, which attract more electrons to bypass the MQW region. Thus, more efforts are necessary to optimize the electron injection layer and/or the p-EBL so that both the efficiency enhancement and the reduced efficiency droop can be obtained.

To summarize, in this work, we have reported a charge inverter for III-nitride LEDs. The effectiveness of the charge inverter is probed both numerically and experimentally by growing and fabricating the blue InGaN/GaN LEDs. The studies show that the charge inverter can reduce the width of the tunnel region by forming an inversion layer at the p^+-GaN surface. By adopting the insulator with a lower

dielectric constant (e.g., SiO_2), the electric field in the tunnel region can also be increased, which further promotes the hole injection. For that reason, the external quantum efficiency for the proposed LED device that has the mesa area of $350 \times 350\,\mu m^2$ is increased by 20% at 20 mA. Although the efficiency droop caused by electron leakage for the proposed device with the charge inverter is observed, one can minimize the electron leakage by increasing the blocking effect of the p-EBL, adopting the electron cooler and/or the n-EBL to reduce the thermal energy of electrons.[19–22] The charge inverter provides an easy way to enhance the hole injection and increase the quantum efficiency, and we believe it is especially promising for the UV LEDs which use p-AlGaN to provide the hole conduction, since compared to the p^+-GaN layer, the p^+-AlGaN layer can have a even larger surface depletion region.

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