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Atomic Layer Deposition for Vertically Integrated ZnO Thin Film Transistors: Toward 3D High Packing Density Thin Film Electronics

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We report on the first demonstration of the atomic layer deposition (ALD) based three dimensional (3D) integrated ZnO thin film transistors (TFTs) on rigid substrates. Devices exhibit high on-off ratio ($\sim 10^6$) and high effective mobility ($\sim 11.8\,cm^2\,V^{-1}\,s^{-1}$). It has also been demonstrated that the steps of fabrication result in readily stable electrical characteristics in TFTs, eliminating the need for post-production steps. These results mark the potential of our fabrication method for the semiconducting metal oxide-based vertical-integrated circuits requiring high packing density and high functionality.

1. Introduction

In conventional-integrated circuits (ICs), active devices are built on a single layer of silicon and different sections of the chip are connected with vertically stacked layers of interconnection wires. Today the scaling of ICs is approaching to its fundamental limits. Furthermore, as the scaling continues the interconnect delay becomes the dominant factor over gate delay.[1] To circumvent these bottlenecks, three dimensional (3D) vertical integration of active layers was proposed since it is possible to achieve high packing density, low power, high performance, parallel processing, lower interconnect lengths, and system-on-chip designs.[1]

One of the most widely used active semiconductor material in thin film electronics is amorphous silicon (a-Si).[2] However, a-Si has low carrier mobility and relatively high thermal budget. Furthermore, absorbance of a-Si in the visible spectrum makes it inadequate for display applications, one of the main market drivers for thin films electronics. Therefore a-Si is being replaced by other materials with superior properties, most notably ZnO-based materials.[3–5] ZnO is very attractive due its optical and electrical properties, and many ZnO-based high performance devices were demonstrated in the literature.[6,7] Moreover, high performance, ALD grown ZnO-based devices at various temperature ranges were shown in previous studies.[87] However, many of these studies reported stability issues of ZnO devices.[6,8] Furthermore, to the best of our knowledge, there has not been a study on 3D integration of ZnO-based devices.

Herein we report on the first 3D-integrated ALD grown ZnO TFTs with lowest thermal budget to date (<80 °C). The TFTs that are operating in two vertically stacked active layers are shown to be stable and they exhibit high performance. The devices are built on rigid substrates and their performances are investigated. It has been shown that, without any special annealing procedures, we were able to achieve highly stable ZnO TFTs by the combined effect of encapsulation and *in situ* annealing.

2. Methods

The fabrication of the proposed TFT structure on rigid substrate (Si) starts with RCA cleaning of the substrate which is followed by a 200 nm SiO_2 blanket oxide deposition with electron beam (E-Beam) evaporation at room temperature. Highly conductive Si (0.001–0.005 Ω-cm) is chosen to function as the bottom gate (BG) of the TFTs in the first active layer. Active area windows are patterned by standard wet HF etching. Next, 21 nm Al_2O_3 and 14 nm ZnO deposition follows for forming the gate stack of the BG TFTs using ALD at 80 °C. Trimethylaluminum and diethylzinc are used as Al and Zn precursors, respectively. Whereas milli-Q water is used as oxygen precursor in both growths. Afterwards, channels of the BG TFTs are patterned using inductively coupled reactive ion etching (ICP RIE) with BCl_3.[8] Then, source and drain contacts of BG TFTs are formed by 100 nm aluminum deposition with thermal evaporation, and a following lift-off process.

Upon the completion of the BG TFTs, several devices were characterized to assess the impact of subsequent processing. To form the second active layer, 14 nm ZnO is deposited, again using ALD at 80 °C by using diethylzinc and milli-Q water as the sources for Zn and O, respectively. Top gate (TG) TFTs are formed by first defining channel layers by BCl_3-based ICP RIE

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etching of ZnO, immediately followed by 21 nm Al_2O_3 deposited with ALD at 80 °C by using trimethylaluminum as the Al precursor and milli-Q water as the oxygen precursor. Next, 100 nm aluminum top gate deposition is performed with thermal evaporation, and patterned using lift off. At last, contact windows to buried source and drain areas are opened in Al_2O_3 using BCl_3-based ICP RIE etching. Overall process was completed exclusively below 80 °C. 3D structural sketch and the SEM image of the completed devices are shown in **Figure 1**.

3. Results and Discussion

The transfer and output characteristics of the bottom layer devices on Si substrate are shown in **Figure 2**, where source-to-drain current (I_{DS}) is plotted as a function of gate-to-source voltage (V_{GS}). All the transfer characterizations in this study are done while drain-to-source voltage (V_{DS}) is kept at 1 V. I_{ON}/I_{OFF} ratio of 1×10^8 is measured before the deposition of the second layer on top of the bottom layer devices. After the fabrication of the top layer devices, bottom layer devices are characterized again and 1×10^6 I_{ON}/I_{OFF} ratio is measured. It is reported that electrical characteristics of ZnO films, kept at the growth temperature after the deposition, which is called *in situ* annealing, change with time.[9] In our fabrication, during the deposition of the second layer, the bottom layer devices are *in situ* annealed. This annealing, in accordance with previous reports, increases the carrier concentration and therefore increases the off current, and lowers the I_{ON}/I_{OFF} ratio as it can be seen in Figure 2a.[10] As evident from the plots, the TFTs show n-type enhancement mode operation and clear post pinch-off saturation. The saturation mobility (μ_{sat}) and the threshold voltage (V_{TH}) is extracted by fitting a straight line to the plot of $\sqrt{I_{DS}}$ versus V_{GS} in the saturation region according to the Eq. (1) which is the drain current equation of a MOSFET in saturation, where

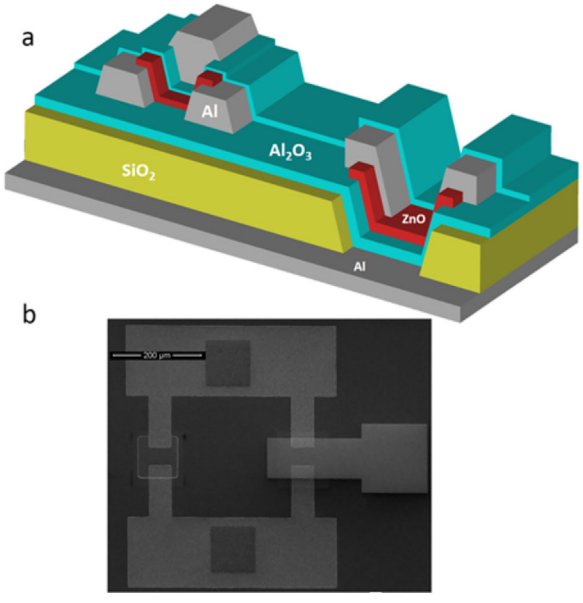

Figure 1. (a) 3D schematic of the vertically integrated TFTs. (b) SEM image of the fabricated devices.

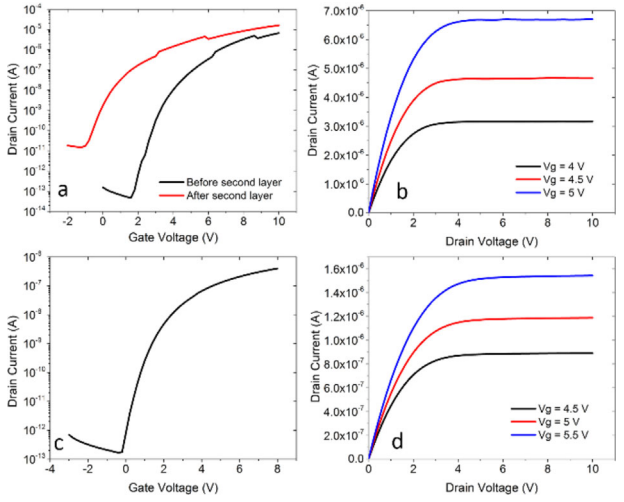

Figure 2. Electrical properties of TFTs on silicon substrates (a) bottom layer transfer characteristics. (b) Bottom layer output characteristics. (c) Top layer transfer characteristics. (d) Top layer output characteristics.

channel width (W) and channel length (L) are both 50 μm, and drain-to-source voltage (V_{DS}) is in the saturation regime. To calculate the gate oxide capacitance per unit area (C_{OX}), dielectric constant of ALD grown Al_2O_3, is acquired from a previous study.[11] Extracted μ_{sat} is around 11.8 $cm^2 V^{-1} s^{-1}$ and the extracted V_{TH} is around 2.66 V.

$$I_{DS} = \left(\frac{C_{ox}\mu_{sat}W}{2L}\right)(V_{GS} - V_{TH})^2 \quad V_{DS} > V_{GS} - V_{TH} \tag{1}$$

To analyze the effect of trapped charges in the operation of the devices, effect of the positive gate bias stress on the threshold voltage is investigated. Right before the stress, the devices are characterized and their threshold voltages are extracted. Then, gate bias is applied for 1000 s to the 21 nm gate dielectric with an effective electric field of 1.21 MV cm^{-1}, while source and drain contacts are kept at ground (0 V). Then immediately after stress, the transfer characteristics are measured again and threshold voltages were extracted again. The threshold voltage right after the stress is measured to be 2.67 V which showed a 17 mV (<1% change) increase with the stress. This increase in the threshold voltage is due to the increased number of trapped electrons in the dielectric which screen the applied gate bias and thus increase the threshold. Such a low shift in the V_{TH} compared to those obtained in the literature, where 50% shifts are commonly reported, is unprecedented for similar ZnO-based TFTs.[12,13] Therefore it is demonstrated that the fabricated bottom layer devices are stable devices, without the need for any special annealing protocol. This stable nature of the devices may be attributed to encapsulation of the devices during the deposition of the second layer in accordance with the literature.[14] However, during this growth since the bottom layer devices are also *in situ* annealed, to distinguish the effects of encapsulation and annealing on the stabilization of the devices, further tests are required. This issue is addressed below for top layer devices.

The transfer and output characteristics of the top layer devices on Si substrate are shown in Figure 2. I_{ON}/I_{OFF} ratio of 3.2×10^5 is measured. Throughout the device operation, the gate leakage current of the TFTs on rigid substrates is measured to be at least four orders of magnitude smaller than the drain current of the devices. The V_{TH} is extracted as 0.745 V and μ_{sat} as 0.172 $cm^2 V^{-1} s^{-1}$. This lower mobility and I_{ON}/I_{OFF} ratio of the top layer devices may be attributed to the trapped charges on the oxide–semiconductor interface of the top layer devices, since there is an extra fabrication step between the growth of oxide and semiconductor layers as opposed to the bottom layer devices. Bottom layer devices did not show such behavior because the gate stack was formed in a single ALD step. Gate bias stress of 1.21 $MV cm^{-1}$ is applied for 1000 s and then the threshold voltage is measured to be 0.94 V, demonstrating a 0.2 V (20%) shift. Stability tests show that the BG TFTs are more stable than TG TFTs. Both devices are encapsulated during the fabrication, however, the bottom layer is also annealed during the deposition of the second layer.

To assess the effects of annealing on stabilization, we grew an additional layer of 21 nm Al_2O_3 with ALD at 80 °C. This insulating layer is expected for any subsequent (3, 4, ... etc.) active device layers for high density integration. After this growth, the TG TFTs are characterized again and 9.2×10^6 I_{ON}/I_{OFF} ratio is measured. The V_{TH} is extracted as 1.46 V and μ_{sat} as 0.09 $cm^2 V^{-1} s^{-1}$. The increase of I_{ON}/I_{OFF} ratio suggest that the oxide–semiconductor interface was passivized during annealing and trap charge density is decreased. Same gate bias stress as before was conducted and 0.015 V (ca 1%) shift was measured. This suggests that, with the fabrication of additional layers of devices, the devices on the lower layers become stable. Therefore more stable operation of the devices are observed due to the combined effects of encapsulation and *in situ* annealing. Hence, the ALD-based 3D integration technology offers a self-stabilizing effect by subsequent layers without requiring any extra capping layers or special annealing protocols.

4. Conclusions

In conclusion, 3D integrated, ZnO based, ALD grown, high performance, and stable TFTs with the lowest thermal budget to date (<80 °C) are fabricated on rigid substrates for the first time. Electrical characterizations, gate bias stability tests are performed and the nature of the stabilization is investigated. This study demonstrates the feasibility of 3D integration of ZnO-based devices. In future works, with further developments of p-type materials, 3D-integrated TFT CMOS analog and digital circuits can be realized for commercial large area applications.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

3D integration, atomic layer deposition, thin film transistors

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