Voltage-to-Time Converter for High-Speed Time-Based Analog-to-Digital Converters

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ABSTRACT OF THE
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In modern complementary metal oxide semiconductor (CMOS) technologies, the supply voltage scales faster than the threshold voltage (V_{th}) of the transistors in successive smaller nodes. Moreover, the intrinsic gain of the transistors diminishes as well. Consequently, these issues increase the difficulty of designing higher speed and larger resolution analog-to-digital converters (ADCs) employing voltage-domain ADC architectures. Nevertheless, smaller transistor dimensions in state-of-the-art CMOS technologies leads to reduced capacitance, resulting in lower gate delays. Therefore, it becomes beneficial to first convert an input voltage to a 'time signal' using a voltage-to-time converter (VTC), instead of directly converting it into a digital output. This 'time-signal' could then be converted to a digital output through a time-to-digital converter (TDC) for complete analog-to-digital conversion. However, the overall performance of such an ADC will still be limited to the performance level of the voltage-to-time conversion process.

Hence, this thesis presents the design of a linear VTC for a high-speed time-based ADC in 28 nm CMOS process. The proposed VTC consists of a sample-and-hold (S/H) circuit, a ramp generator and a comparator to perform the conversion of the input signal from the voltage to the time domain. Larger linearity is attained by integrating a constant current (with high output impedance) over a capacitor, generating a linear ramp. The VTC operates at 256 $MSPS$ consuming 1.3 mW from 1 V supply with a full-scale 1 $V_{pk-pk_{differential}}$ input signal, while achieving a time-domain output signal with a spurious-free-dynamic-range (SFDR) of 77 dB and a signal-to-noise-and-distortion ratio (SNDR) of 56 dB at close to Nyquist frequency ($f = 126.5\,MHz$). The proposed VTC attains an output range of 2.7 ns, which is the highest linear output range for a VTC at this speed, published to date.

Keywords: complementary metal oxide semiconductor, voltage-to-time converter, time-to-digital converter, time-based analog-to-digital converter, differential, comparator

Preface

I want to thank Professor Jussi Ryynänen for providing me the opportunity to work in his team. I would also like to thank my instructor Marko Kosunen for constantly guiding me throughout the design phase, and providing insightful feedback for improving the performance of the circuits as well as during the thesis writing phase, and Kari Stadius for managing everything behind the scenes.

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Finally, I would like to thank my parents, especially my father Abid Hassan Siddiqui. He has been an immense beacon of support for me at every stage of my life, both emotionally as well as financially. All the success and happiness that I have ever achieved, and the ones that I hopefully will and can ever have the slightest capability to achieve, has only been possible through his continuous and constant efforts, sacrifices, guidance and prayers. And for that, I am eternally grateful to him.

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Contents

Symbols and abbreviations

Abbreviations

ADC	Analog-to-digital converter
DNL	Differential non-linearity
ENOB	Effective number of bits
MSB	Most significant bit
LSB	Least significant bit
INL	Integral non-linearity
SFDR	Spurious-free dynamic range
SNR	Signal-to-noise ratio
SNDR	Signal-to-noise-and-distortion ratio
KSPS	Kilo samples per second
MSPS	Mega samples per second
GSPS	Giga samples per second
kHz	Kilo Hertz
MHz	Mega Hertz
TDC	Time-to-digital converter
VTC	Voltage-to-time converter
FDC	Frequency-to-Digital Converter
FFT	Fast Fourier transform
FOM	Figure of merit
DAC	Digital-to-Analog converter
PVT	Process, voltage and temperature
RMS	Root mean square
SAR	Successive approximation register
VCO	Voltage controlled oscillator
dB	Decibels
FS	Full scale signal
MUX	Multiplexer
opamp	Operational amplifier
RF	Radio frequency
S/H	Sample and hold
TBADC	Time-based-analog-to-digital converter
w.r.t	With respect to
V_{DD}	Supply voltage
V_{in}	Input voltage
V_{ref}	Reference voltage
V	Voltage
I	Current
R	Resistance
g_m	Transconductance
r_o	Transistor output impedance

1 Introduction

Recently, there has been a shift to improve the characteristic features of a device or a machine by appending a feedback electronic control system rather than modifying the physical characteristics of that device. For example, innovation in mechanical parts inside motor vehicles has been slow over the years. Nevertheless, electronic controls, such as electronic fuel injection (EFI) and automatic braking system (ABS), have been added to improve the overall performance of the automotive. In fact, the cost of modern automobiles is largely dictated by the cost of electronic systems rather than mechanical systems [1]. Therefore, the success of automotive industry falls predominantly upon differentiating their products using electronic and software innovations. Thus, electronic control systems have become an integral part in the development of human civilization.

These electronic control systems almost always contain some sort of a digital signal processor (DSP). Digital signal processing has changed the course of technological development swiftly. This is because processing, transport and storage of data is much more robust, cost effective, fast and accurate when performed in the digital domain, compared to when performed in the analog domain. However, DSPs could only process digital information. Moreover, our universe is analog in nature, and data sent and received to and from it is in a continuous analog form. Hence, intermediate systems are needed that behave as an interface between the real world signals and the DSP module. These interface circuits comprise analog-to-digital (ADC) or digital-to-analog (DAC) converters.

Considering interface circuits, ADCs are indispensable part of numerous communication systems. They are incorporated in devices used for measurement and testing, sensor networks, data acquisition, smart-phones, bio-medical equipment, audio and video processing etc. There are two key characteristics that define the performance of an ADC: resolution and throughput. Based on the application, the requirement for the ADC could either be very high resolution, or throughput, or both. For example, audio processing requires low-speed and high-resolution output for the converter, analog signal received by interferometer antennas in radio astronomy utilize high-speed and low-resolution ADCs, and wireless display application for high definition televisions require high-speed as well as high-resolution ADCs. Nonetheless, achieving the required performance for an ADC in any CMOS technology will always be at the expense of power consumption and silicon area.

Information in analog domain is typically represented by a voltage or a current, which is continuous in both time and amplitude domain. However, various methods could be used to convert that into a discrete domain signal. For example, a sample-and-hold circuit converts a continuous time and amplitude signal to a discrete time and continuous amplitude signal. Similarly, a voltage-to-time converter (VTC) converts a continuous time and amplitude signal into continuous time and discrete amplitude signal, and a voltage-domain ADC converts a continuous time and amplitude signal into discrete time and amplitude signal.

Voltage-domain ADCs usually consist of one or more comparators, with or without a feedback system, followed by a sample-and-hold circuit, in order to determine the

corresponding digital code for an analog input signal. To attain higher speed and larger resolution simultaneously, pipelined ADCs are typically utilized. However, voltage-domain pipelined ADCs require high gain and bandwidth opamps to amplify the residual signal for successive stages. However, smaller gain, lower overdrive voltage and larger noise (due to smaller transistor dimensions) makes the opamp design extremely challenging, especially for high speed and resolution applications [2].

Due to these challenges, focus has recently shifted towards designing high-speed converters, that do not require opamps in its design. One such architecture is a time-based ADC [3]. Compared to voltage-domain ADCs, time-based ADCs perform the conversion of analog signal to a digital code in two distinct steps; initially an analog signal is converted to a time signal using a voltage-to-time converter (VTC), which is then processed and converted to a digital code using a time-to-digital converter (TDC). Moreover, as the technology nodes becomes successively smaller, attaining lower timing resolution might become more realistic than finer voltage resolution, since supply voltages will be reduced, whereas gate delays, rise/fall times, and parasitic capacitances within CMOS transistors will simultaneously diminish [4]. Thus, time-based ADCs have a few potential advantages compared to voltage-domain architectures [5].

In designing a time-based ADC, the linearity and performance of the complete ADC is largely limited by the performance of the VTC. This is because VTC is the analog core of the time-based ADC, and hence, its design will be dictated by the thermal noise levels and the transistor characteristics (linearity, gain, output impedance, bandwidth). While, typical architectures employing time-based ADCs are either limited to lower resolution [6] or speed [7], little attention has been paid towards designing higher speed and larger resolution time-based ADCs.

Therefore, the purpose of this thesis is to design and develop a linear voltage-to-time converter for a high-speed time-based ADC. The proposed design contains a sample-and-hold circuit, a ramp generator and a comparator for converting 'analog signal' to a 'time signal'. Furthermore, the proposed design is implemented at transistor-level using a 28 nm CMOS process. To corroborate the performance of the implemented circuits, 'Cadence Virtuoso' is used for simulating the transistor-level performance.

However, main focus of the thesis will be limited to the design and verification of the VTC architecture, which could potentially be combined with a TDC to complete the analog-to-digital conversion. Hence, the design and analysis of a TDC is beyond the scope of this thesis.

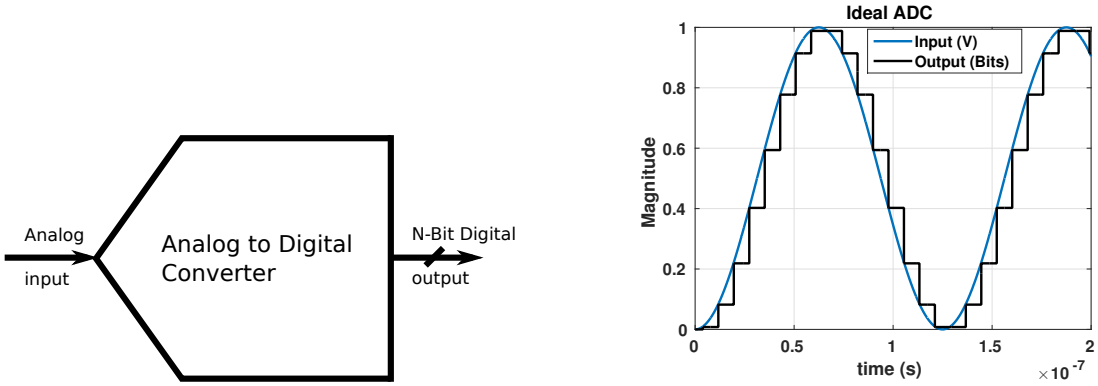
The thesis is divided into five chapters as follows. Chapter 2 reviews some voltage-domain ADCs as well as provides a concise description of performance metrics to evaluate analog-to-digital converters. Chapter 3 reports the literature review of the time-based ADCs by presenting a brief description of a few commonly employed time-based architectures. The design specification for the VTC are discussed in detail in Chapter 4. Chapter 5 presents the the transistor level implementation as well as the results of the proposed VTC, followed by the conclusion of the thesis in Chapter 6.

2 Background

This chapter provides a brief description of the voltage-domain ADC architectures as well as the specifications and the metrics to analyze the performance of an ADC. Consequently, it presents a basic understanding of ADCs as well as the challenges in designing ADC structures, since knowledge of the performance specifications and the metrics is critical for architecture selection of the ADC.

2.1 Analog-to-Digital Converter

ADCs are circuits that convert a signal from the analog domain to its corresponding digital code. The block diagram representation of an ADC as well as the input and output for an ideal ADC are shown in the Figs. 1a and 1b respectively.



(a) (b)

Figure 1: (a) Block Diagram of an ADC and (b) Input and outputs of an ADC.

Conversion in a voltage-domain ADC is performed such that a continuous analog signal is first sampled at discrete time intervals using a sample/track and hold stage. Then, the sampled signal is quantized in its amplitude for complete transition from analog to digital domain.

Since there are only a finite amount of quantized output levels, depending upon the resolution of the ADC, there is bound to be some amount of error between the actual analog input signal, and the corresponding output of the ADC. This error is known as quantization error, usually denoted by Δ. In an ideal ADC, the output will have error bounded between ± 0.5 LSB. Moreover, ADC also has a predefined reference signal (V_{ref}), which is used for comparison with the input signal to determine the corresponding digital output code. Usually, the reference signal defines the limits of detectable full-scale amplitude (V_{FS}) for the input analog signal. In addition to this, the smallest signal distinctly detectable by the ADC is known as the least significant bit (LSB), and is given by

$$LSB = \frac{V_{FS}}{2^N}, \tag{2.1}$$

where N represents the number of output bits for the converter.

2.2 Voltage-Domain ADC architectures

There are various architectures of ADCs. Each ADC architecture has its own strength and weakness, and there is no single architecture that could be employed in all possible applications. Rather, architecture selection is one of the most critical part in designing an ADC. Moreover, there are a few methods that could be applied to these architectures for increasing the overall performance (speed and resolution) of the ADC.

In addition, ADCs can be differentiated based on the signal bandwidth and the sampling clock frequency. For example, ADCs can be be Nyquist-rate converters, where the sampling clock frequency is close to twice that of the input signal bandwidth. However, Nyquist-rate converters cannot take advantage of noise shaping methods and are usually limited to 14 bits of linearity. On the other hand, oversampling converters have a signal bandwidth much lower than that of the sampling clock frequency. For instance, a sigma-delta ADC, which is an oversampling ADC, could achieve much larger SNR (up to 20 bits of resolution) due to noise shaping.

A few commonly used ADC architectures will be briefly described in this section.

- **Flash ADC:** Flash ADCs are very fast converters. An N-bit flash ADC will have $2^N - 1$ comparators. All of the these comparators will compare the input signal level with $2^N - 1$ different references simultaneously to determine the corresponding digital code of the analog input. However, achieving larger resolution with this type of ADC is challenging, since the number of required comparators increase exponentially with the resolution. Details of flash ADC are described in Appendix A.1.

- **Successive Approximation Register ADC:** Successive approximation register (SAR) ADC has a reasonably good resolution and throughput. An N-bit SAR ADC will only contain one comparator, resulting in much smaller silicon area for the converter. However, they are slower than flash ADCs. This is because each bit in the ADC requires a clock cycle for the conversion. Hence, a 10 bit SAR ADC will provide a 10 bit output after every 10 cycles, compared to a flash ADC, that provide an output at every clock cycle. Details of SAR ADC are described in Appendix A.2.

- **Sigma Delta ADC:** Also known as over sampled converters, sigma delta (SD) ADCs could provide much larger resolution, compared to SAR as well as flash ADCs, at high oversampling ratios. However, larger oversampling ratios result in lower input bandwidth for the ADC. Details of SD ADC are described in Appendix A.3.

- **Pipelined ADC:** In a pipelined ADC, multiple lower resolution ADCs are cascaded to attain an overall higher resolution conversion. Furthermore, the architecture of the cascaded smaller resolution ADC could be independently selected (flash, SAR, SD etc.). However, pipelining results in latency in the output, depending upon the number of pipelined stages. Moreover, calibration

is required between the cascaded stages to avoid mismatches and subsequent errors in the results. Details of pipelined ADC are described in Appendix A.4.

- **Time Interleaved ADC:** In-time interleaved ADCs, multiple low-speed and high-resolution ADCs are connected in parallel to attain an overall higher data rate. Similar to the case of pipelined ADC, architecture of a single branch in time interleaved ADCs could be independently selected. However, time-interleaving results in higher silicon area and power consumption. Moreover, timing mismatches between interleaved branches could severely degrade the results. Details of time interleaved ADC are described in Appendix A.5.

2.3 Challenges in Voltage-Domain ADC Designs

The performance of a voltage-domain ADC is highly reliant on the characteristics of the transistors within a process. However, CMOS processes are designed and optimized from the digital design's perspective. Thus, the main focus of the process development is to improve the switching speeds and the transistor density while simultaneously lowering the supply voltages. Nonetheless, system-on-chip (SoC) development demands the integration of radio frequency (RF), analog, mixed signal, and digital design on the same chip. Hence, RF, analog and mixed signal designs suffer to attain high performance using the processes optimized mainly for digital designs.

Additionally, as the transistor's channel length decreases in successive smaller processes, gate oxide layer also becomes narrower. Consequently, the breakdown voltage for the transistor is lowered, and it becomes necessary to reduce the voltage supply across the transistor for a reliable operation over the lifetime of the circuit [8]. However, the threshold voltage (V_t) of the transistors does not scale linearly with the supply voltages. Hence, the overdrive voltage (V_{OV}) for the transistors is effectively reduced with technology scaling. Moreover, technology scaling reduces the inherent gain of the transistors. In addition, signal-to-noise ratio (SNR) of the analog circuits become smaller, owing to smaller signal swings, and power consumption of these circuits has to be increased for maintaining the SNR [2, 9].

Thus, capability of the transistors for handling information in analog-domain is gradually decreasing with subsequent technological evolution. Therefore, it has become necessary to find alternative solutions of designing ADCs, that rely less on the transistor gain and more on its speed. One such method is a time-based ADC, which will be covered more in detail in Chapter 3.

2.4 Performance Metrics

There are numerous metrics that define the overall performance of an ADC. Most commonly used performance metrics are defined in [10], and are summarized in the following section:

2.4.1 Static Performance Parameters

- **Gain and Offset Errors:** Gain and offset errors do not contribute towards linearity degradation of the converter. Nonetheless, they still need to be determined and corrected for proper operation of the ADC. A graphical representation of gain and offset errors in an ADC are shown in Figs. 2a and 2b respectively.

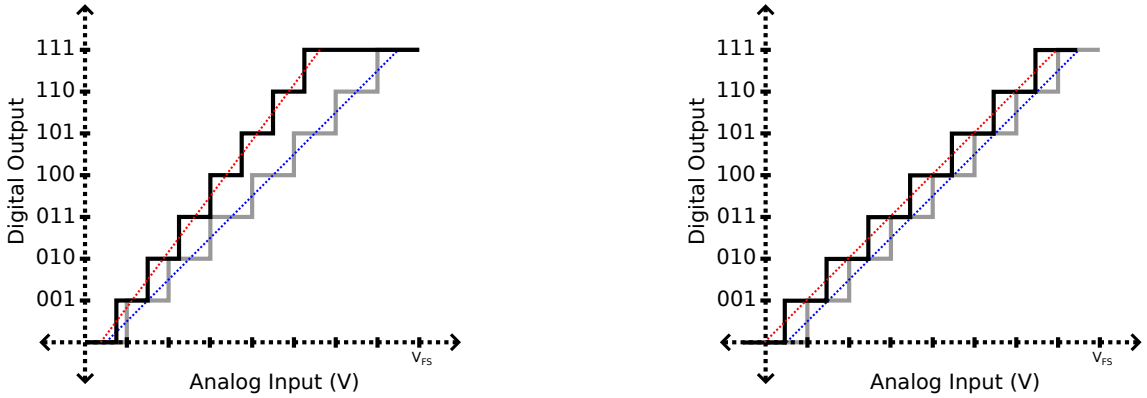


Figure 2: (a) Gain Error and (b) Offset Error.

An ideal ADC operates such that the smallest input signal corresponds to the lowest output digital code, and the largest corresponds to the highest code. However, if there is a gain error in the converter, the steps might still be uniform while being smaller or larger than the expected steps. Mathematically,

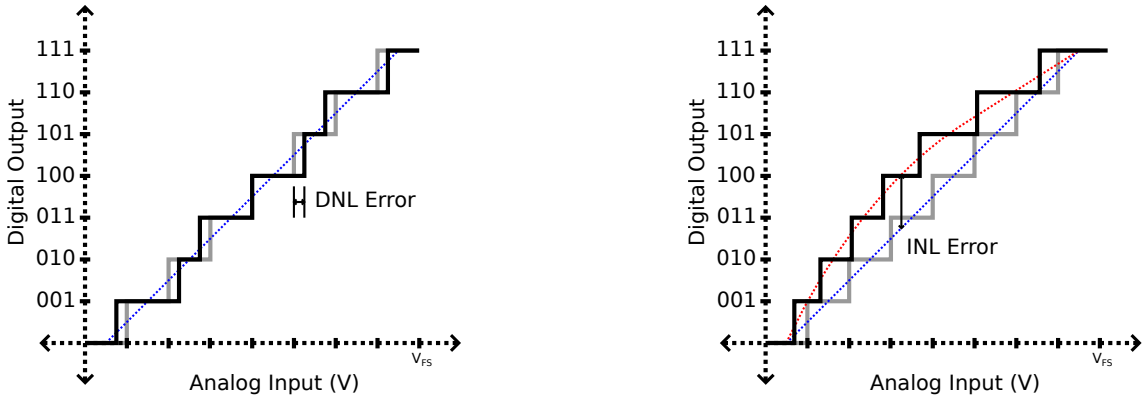
$$LSB = Gain\ \frac{V_{FS}}{2^N}\,, \tag{2.2}$$

where gain is equal to one for the case of an ideal ADC. However, this is usually not the case for a real ADC. Consequently, the full-scale input signal will not correspond to the highest digital output code as depicted in Fig. 2a. Moreover, ADCs could also have an offset error, resulting in a transfer function as shown in Fig. 2b. Both gain and offset errors are usually easily calibrated out of the converter.

- **Non-Linearity Errors:** There are two kinds of static non-linearity errors that are of critical significance for optimal performance of an ADC. They are depicted graphically in Figs. 3a and 3b respectively.

  To understand differential non-linearity (DNL), it should be established that every successive step taken by the ADC should have a difference of exactly one LSB. DNL is the variation of the step taken by the ADC, compared to the step that should have been taken by the ADC, as shown in Fig. 3a. Mathematically,

$$DNL(i) = \frac{V_{out}(i+1) - V_{out}(i)}{\Delta} - 1\,, \tag{2.3}$$



(a) (b)

Figure 3: (a) Differential Non-Linearity and (b) Integral Non-Linearity.

where Δ is the ideal LSB width. For monotonic operation, it is required that the maximum DNL should not exceed the bounds of ± 0.5 LSB.

Integral non-linearity (INL) is defined as the deviation of actual output of the converter from the ideal straight line response. As shown in Fig. 3b, the blue line joins the center points of all the steps for the ideal ADC response, whereas the red line joins the mid points of actual ADC outputs. Usually, INL is defined as the largest deviation of the actual line from that of the ideal line. As a rule of thumb, maximum INL should not exceed more than ± 0.5 LSB. Nevertheless, it may be relaxed, depending upon the application of the ADC.

2.4.2 Dynamic Performance Parameters

There are numerous dynamic performance parameters, that define the ADC characteristics. Details can be found in [10], and are summarized as follows:

- **Signal-to-Noise Ratio:** Signal-to-noise ratio (SNR) is defined as the ratio of the signal power to the noise power. Mathematically,

$$SNR = 10\, log_{10} \left[\frac{signal\ power}{noise\ power} \right]. \tag{2.4}$$

- **Total Harmonic Distortion:** Total harmonic distortion (THD) is defined as the ratio of the signal power to harmonic distortion power. Mathematically,

$$THD = 10\, log_{10} \left[\frac{signal\ power}{distortion\ power} \right]. \tag{2.5}$$

- **Signal-to-Noise-and-Distortion Ratio:** Signal-to-noise-and-distortion ratio (SNDR) is defined as the ratio of the signal power to the sum of the distortion and the noise power. Mathematically,

$$SNDR = 10\, log_{10} \left[\frac{signal\ power}{distortion\ power + noise\ power} \right]. \tag{2.6}$$

- **Effective Number of Bits:** Effective number of bits (ENOB) is usually calculated using SNDR in the following manner:

$$ENOB = \frac{SNDR - 1.76}{6.02}\,. \tag{2.7}$$

- **Figure of Merit:** In order to compare numerous ADCs with different topologies and applications, figure of merit (FOM) could be used to determine the efficiency of the converter. There are numerous methods to evaluate FOM. One of the very famous one is called Walden FOM [11]. It gives conversion energy per unit step, and is calculated as follows:

$$FOM = \frac{2 \cdot 2^{ENOB}\, BW}{P}\,, \tag{2.8}$$

  where BW is the bandwidth, and P is the power consumption.

2.5 Specifications

The selection of an ADC architecture is a critical step in the design procedure, which is based on the defined specifications of the ADC, as presented briefly in this section:

- **Resolution:** Resolution is one of the key factors in defining the selection of an ADC architecture. It is defined as the smallest change in the input signal, that will be sensed by the ADC and the output will correspondingly change by 1 LSB. It is mathematically given by (2.1).

- **Power Consumption:** Even though reducing the power consumption is always one the main goals of an ADC design, it usually is much more critical in mobile devices, especially for internet of things (IoT) or similar applications.

- **Area:** Larger the silicon area, more will be the cost and vice versa. Hence, ADCs that span over smaller areas are always desirable.

- **Dynamic Range:** It is the ratio of the largest input signal, linearity detected by the ADC, to the smallest input signal level, discernible from the noise floor. Based on the application, dynamic range might become one of the main factors in deciding the architecture of the ADC.

- **Latency:** Pipelined ADCs have the advantage of reducing the overall size and area of a high resolution ADC, e.g. using flash converters. However, pipelining inherently adds latency in the output. Hence, latency tolerance is also a key factor in the selection of an ADC architecture.

3 Time-based Analog-to-Digital Converters

This chapter reviews the design methodologies of some of the commonly employed time-based ADCs, their architectures, performances, and limitations. These include integrator-based, voltage-controlled-oscillator (VCO) based, and voltage-to-time converter (VTC) based ADCs. Since the performance of the VTC is highly dependent on the selected structure, therefore, a basic understanding of the commonly employed time-based ADC structures is extremely critical.

3.1 Integrating ADC

Integrating ADC, also known as dual-slope ADC, is one of the simplest and robust time-based ADC architecture. The structure of an integrating ADC is shown in Fig. 4.

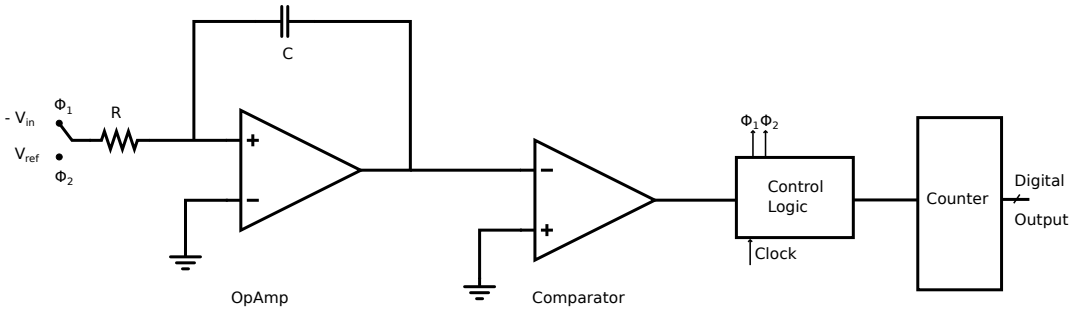


Figure 4: Dual Slop Integrating ADC.

The operation of dual-slope ADC has two distinct phases. In the first phase, the input signal creates a ramp at the output of the integrator for a fixed amount of time (t_1), defined by

$$V_{out_1} = -\int_0^{t_1} \frac{-V_{in}}{R\,C}\,dt = \frac{V_{in}\,t_1}{R\,C}\,.$$

In the second phase, a fixed known voltage (V_{ref}) generates a slope in the opposite direction for an known amount of time (t_2), defined by

$$\begin{aligned} V_{out_2} &= -\int_{t_1}^{t_2} \frac{-V_{ref}}{R\,C}\,dt\,, \\ &= \frac{V_{ref}\,(t_2 - t_1)}{R\,C}\,. \end{aligned}$$

Also,

$$V_{out} = V_{out_1} + V_{out_2}\,.$$

The conversion is complete when the integrator output becomes logic low, i.e., $V_{out} = 0$. Hence,

$$t_2 = t_1\,\frac{V_{in}}{V_{ref}}\,. \tag{3.1}$$

Furthermore, a counter starts counting the number of clock cycle during the elapsed time, i.e., from the beginning of the second phase to the moment the output of the integrator becomes 0 V. Thus, an analog input is converted into a digital output.

This architecture has the following benefits and limitations.

- **Advantages:** From (3.1), it is apparent that the output is independent of absolute component values (R and C), and hence, it is a very robust design for low-speed and medium resolution applications. For example, [12] uses dual slope ADC to attain 9.3 bits of ENOB at 10 kHz frequency consuming only 350 μW power. Furthermore, employing zero crossing based comparators, such as in [13] instead of opamps, could slightly mitigate the speed limitations of this architecture.

- **Disadvantages:** The performance of dual slope ADCs are limited by the characteristics of the opamp. Since at very high throughput, the opamp design becomes power hungry and extremely challenging, such architectures are usually limited to low speed applications.

3.2 Voltage-Controlled-Oscillator-based ADC

A simplistic model of a voltage-controlled-oscillator (VCO) based ADC is shown in Fig. 5. The architecture consist of a voltage-to-frequency converter (VFC), followed by a frequency-to-digital converter (FDC). Voltage-to-frequency conversion is usually achieved by employing a VCO, such that its oscillation frequency (or output phase) is directly proportional to the input signal voltage level [14]. This frequency (or phase) is calculated using a FDC to obtain the corresponding digital output.

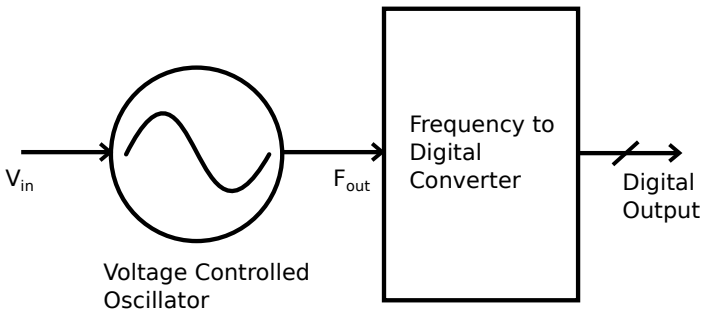


Figure 5: VCO based ADC.

Frequency-to-digital conversion could be achieved by employing numerous techniques, as implemented in [14–17]. However, the methodologies will not be discussed in detail. Nonetheless, the advantages as well as the shortcomings of this architecture is summarized as follows:

- **Advantages:** Unlike delta sigma ADCs, VCO-based converters can be implemented using only a VCO in addition to a few digital logic circuits. Furthermore,

an all-digital-implementation of an ADC becomes possible by employing this structure.

- **Disadvantages:** The performance of a VCO-based ADC is highly dependent on the linearity of VFC. This, however, is almost always quite a challenging task. Consequently, VCO-based ADCs usually operate with small input signal range and employ huge amounts of post processing on the output data to improve the SNR of the output [18]. Moreover, the oscillating frequency of the VCO should be much higher than the throughput of the ADC, which has a physical limitation imposed by the parasitic capacitances of CMOS transistors within a particular technology. Hence, achieving larger resolution at higher throughput is extremely tedious with this architecture.

3.3 Voltage-to-Time Converters

Voltage-to-time Converters (VTCs) have recently gained a lot of interest. As mentioned in Section 2.3, the reduction of tolerable supply voltages is increasing the challenges in voltage-domain ADC designs. However, the resolution of TDCs have been improving with CMOS node scaling, since digital gates are almost impervious to the negative effects of reduced power supply, whereas smaller transistor dimensions consequently result in improved speeds of the digital circuits [19]. Hence, it is becoming more and more lucrative to design ADCs using this topology, and therefore, is also the selected architecture for this thesis.

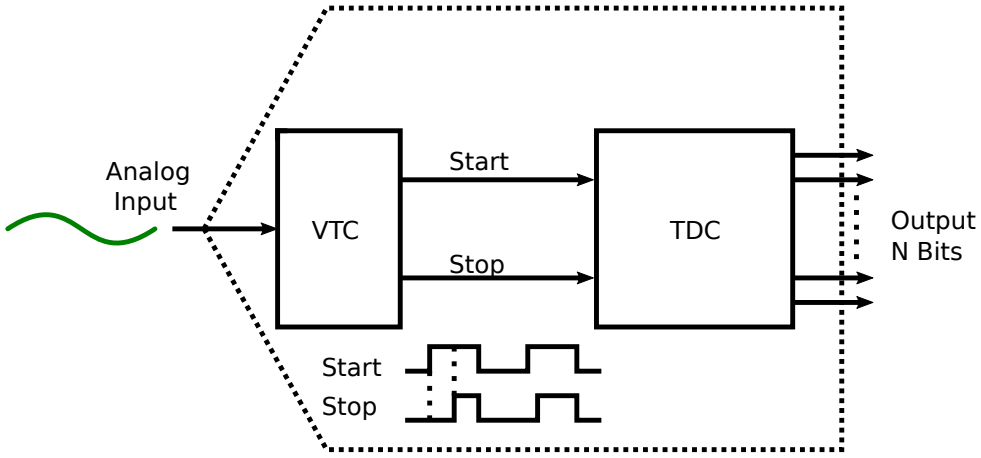


Figure 6: VTC-based ADC.

The block level representation of a VTC-based ADC is shown in Fig. 6. As shown, VTC-based ADCs comprise two distinct blocks. First block is known as the voltage-to-time converter (VTC). This is followed by the second block, known as the time-to-digital converter (TDC).

VTC is an analog circuit, that converts an analog (continuous time and amplitude) signal to a time (continuous time and discrete amplitude) signal. There are various

ways to design a VTC. However, current starved inverter (CSI) based VTCs [3,20–23] and ramp-and-comparator based VTCs [7,24–26] are the most commonly employed architectures. Both of these methods rely on converting an input analog signal to a time signal by charging or discharging a capacitor with a current source. However, the employed methodology greatly influences the achievable speed and resolution of the VTC.

Irrespective of the selected architecture for voltage-to-time conversion, there are a few advantages of employing time-based A/D conversion. Two of them are mentioned as follows:

- Modern CMOS processes have very limited isolation between digital and noise sensitive analog circuits [27]. However, in time-based ADCs, analog and digital portions could spatially be far away from each other, and thus, the analog section could be well protected from the noise injected by the digital circuitry. Moreover, the complexity of the analog section in time-based ADC can potentially be reduced at the expense of increasing complexity in the digital domain.

- The difficulty in time-based ADCs shift more towards digital domain. However, since the digital circuits could potentially be synthesized, the overall difficulty in designing the converter reduces. Moreover, CMOS scaling could reduce the overall area and power consumption, mainly because the power consumption of the digital section is larger than the analog counterpart in time-based converters, especially in larger resolution and higher speed applications.

Due to the these reasons, time-based ADCs might provide a more efficient solution of data conversion, compared to voltage-domain ADC architectures.

Since the resolution of the VTC-based ADC is usually limited by the performance of the VTC, therefore, selecting an appropriate architecture for voltage-to-time conversion is an extremely critical step in the design of such an ADC. Hence, these structures of VTCs will be discussed in the following sections.

3.3.1 Current-Starved-Inverter-Based VTC

It is one of the most commonly used VTC structure for VTC-based ADC applications. A simplified structure and the operation of a CSI-based VTC are shown in Figs. 7 and 8 respectively.

A CSI-based VTC comprises two cascaded inverters. As shown in Fig. 7, the speed of the first inverter (M_1 and M_2) is limited by input signal level via transistor M_3, and therefore, is the current starved section of this VTC. This stage drives a load capacitance, which is equal to the sum of drain capacitances at the output of the first inverter and the gate capacitances at the input of the second inverter. Consequently, the fall time at the output of the first inverter becomes directly proportional to the input signal. On the other hand, the speed of the second inverter is only limited by the technology, and it therefore behaves as a threshold level detector for the current starved inverter.

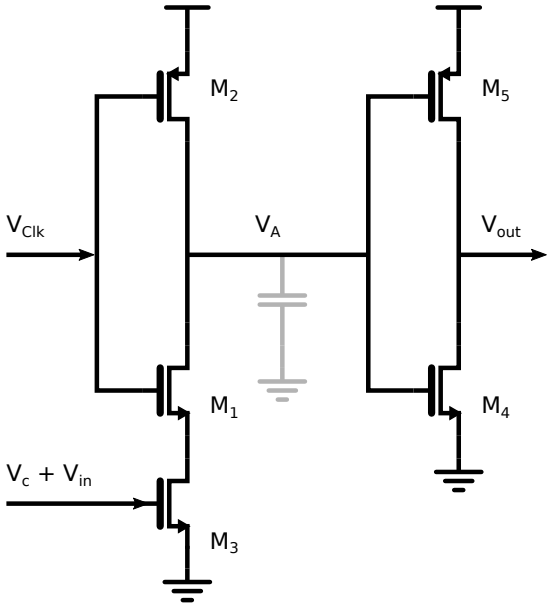


Figure 7: CSI-based VTC.

The timing diagram of the operation is presented in Fig. 8. The VTC has a total of two variable input voltages 'in' as well as 'clk' and a constant DC input voltage 'c'. DC voltage 'c' is selected such that input transistor M_3 still remains in ON state even at the lowest applied input signal. This results in an offset voltage at the lowest applied input signal, represented in Fig. 8 as the 'constant margin', and it should be greater than the threshold voltage of the NMOS transistor (V_{tn}) for M_3. Without the DC offset, M_3 will turn OFF completely at lowest input voltage resulting in an extremely large discharge time at the output node of the first inverter (node A), and there might not be any output generated by the VTC. Consequently, this will interfere with the operation of the TDC, as the TDC expects a valid time signal at its input to be converted to a digital code. The operation of a TDC will be discussed briefly in Section 3.4.

In order to keep M_3 in saturation

$$V_{DS_3} \geq V_{GS_3} - V_{tn}\,.$$

This puts a cap on the upper limit of the input voltage 'in'. Therefore, to achieve better linearity and proper functionality, the input signal should be limited between a upper bound (defined by saturation level) and a lower bound (to keep the transistor in ON state at the lowest input signal level).

When the clock signal 'clk' is logic low, 'node A' is charged to the supply voltage (V_{DD}) through M_2. Since, this process is not limited by any other factors, the rise time at 'node A' will be instantaneous. Consequently, output voltage 'out' will discharge to logic low level quickly. When clock signal 'clk' goes to logic high, 'node A' starts discharging through a cascade of M_1 and M_3. Since, in this phase, gate of M_1 is connected to the supply voltage (V_{DD}), the discharge rate at 'node A' will

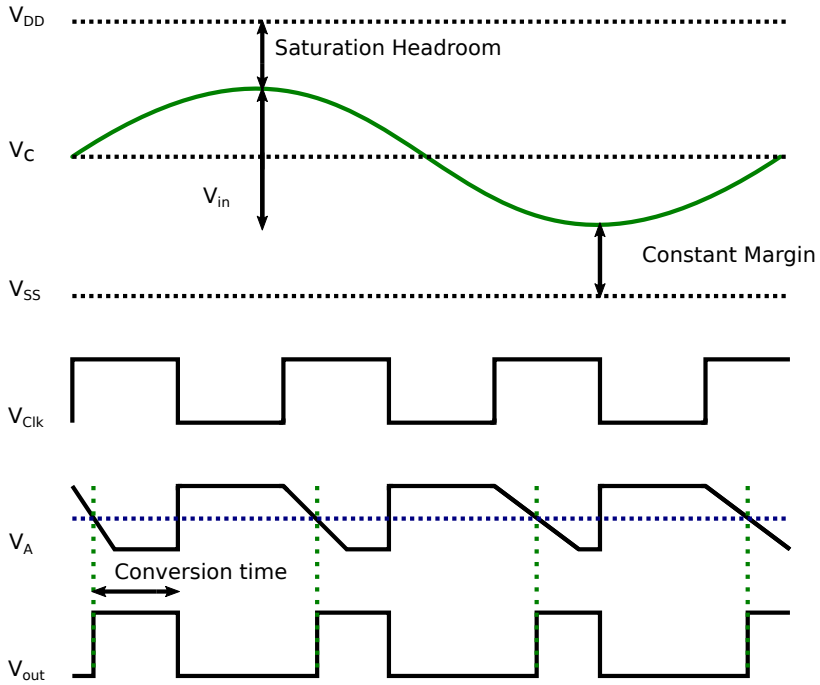


Figure 8: CSI-based VTC timing diagram.

become directly proportional to the input voltage 'in'.

We know that, during saturation and neglecting channel length modulation, the current through an N-type CMOS transistor is given by

$$I_D = \frac{1}{2} k_{n'} \frac{W}{L} (V_{GS} - V_{tn})^2 \,, \tag{3.2}$$

where V_{GS} is the difference between the gate and source voltage, W is the width, L is the length, $k_n{}'$ is a constant for the transistor and V_{tn} is the threshold voltage of the NMOS transistor. Moreover,

$$\frac{I}{C} = \frac{dV}{dt} \,, \tag{3.3}$$

where I is the current through transistor M_3, and C is the parasitic capacitance at 'node A'. Assuming that the input transistor M_3 is in saturation when voltage at 'node A' is at the threshold of the inverter, the maximum discharging current will be given by

$$I_3 = \frac{1}{2} k_{n'} \frac{W_3}{L_3} (V_{in} + V_C - V_{tn})^2 \,. \tag{3.4}$$

Moreover, total capacitance at 'node A' is given by

$$C = C_A = C_{sd_2} + C_{sg_5} + C_{gs_4} \,,$$

where C_{sd_2} is the source-to-drain capacitance of M_2, C_{sg_5} is the source-to-gate capacitance of M_5, and C_{gs_4} is the gate-to-source capacitance of M_4. The drain-to-source capacitance of M_1 (C_{ds_1}) should not be considered during this phase, as it

will be shorted through M_1. Now, from (3.3), the discharging time will be given by

$$dt = \frac{C_A\, dV}{I_3}\,. \tag{3.5}$$

The output voltage 'out' will change when voltage at 'node A' crosses the threshold voltage of the inverter (V_{th}), defined by the ratio of the widths and mobility of PMOS and NMOS transistor within the inverter. The mobility of an NMOS transistor is usually about twice than that of the PMOS transistor. Therefore, to compensate for that, the size of PMOS is kept double than that of the NMOS transistor. In such a case, the threshold voltage (V_{th}) of the inverter can be assumed to be at $0.5\,V_{DD}$. Therefore, $dV = V_{DD} - V_{th} = V_{DD} - \frac{1}{2}V_{DD} = \frac{1}{2}V_{DD}$. Hence, during the conversion time, the voltage goes from V_{DD} to $0.5\,V_{DD}$ in 0 s to t_c s time. Hence, integrating (3.5), we get

$$\int_0^{t_c} dt = \frac{C_A}{I_3}\int_{V_{DD}}^{0.5\,V_{DD}} dV\,,$$
$$t_c = \frac{0.5\,V_{DD}\,C_A}{I_3}\,.$$

Substituting (3.4), we get

$$t_c = \frac{V_{DD}\,C_A}{k_{n'}\frac{W_3}{L_3}(V_{in} + V_C - V_{tn})^2}\,. \tag{3.6}$$

Applying Taylor series approximation to estimate non-linearity, we get

$$T(V_{in}) \approx \frac{V_{DD}\,C_A}{k_{n'}\frac{W_3}{L_3}}\left[\frac{1}{(V_C - V_{tn})^2} - \frac{2\,V_{in}}{(V_C - V_{tn})^3} + \frac{3\,{V_{in}}^2}{(V_C - V_{tn})^4} - \frac{4\,{V_{in}}^3}{(V_C - V_{tn})^5}\right]. \tag{3.7}$$

From (3.7), it is clear that the delay at the output is non-linearly related to the input signal level. The advantages and limitation of this structure are summarized as follows:

- **Advantages:** Since CSI-based VTC consist of only a few transistors, it consumes very small silicon area. Additionally, the architecture has very high speed, since the operation depends upon discharging a very small capacitance through an input signal dependent current source. Hence, very high operating frequency is possible using this architecture. For example, [23] uses a current starved VTC architecture to achieve 6 bits of resolution at 10 GSPS throughput while consuming 98 mW of power by employing differential architecture and post-processing.

- **Disadvantages:** As is evident from (3.7) that the relationship between V_{in} and t_c is not linear. Moreover, the input range is limited, as larger input swing will result in higher non-linearity. Consequently, achievable resolution using this architecture is usually limited to 4 bits [3], and attaining linearity of more than 6 bit is extremely challenging.

Since the main objective is to explore highly linear VTC architectures, CSI-based VTC will not be considered further in this thesis.

3.3.2 Ramp-and-Comparator-Based VTC

Ramp-and-comparator-based VTC also converts a voltage signal to a time signal. However, contrary to CSI-based VTC where the discharging current was dependent on the input signal, this architecture generates a fixed ramp using a constant current source integrated over a capacitor, and compares the ramp with the applied input signal. The architecture and its timing diagram are shown in Figs. 9 and 10 respectively.

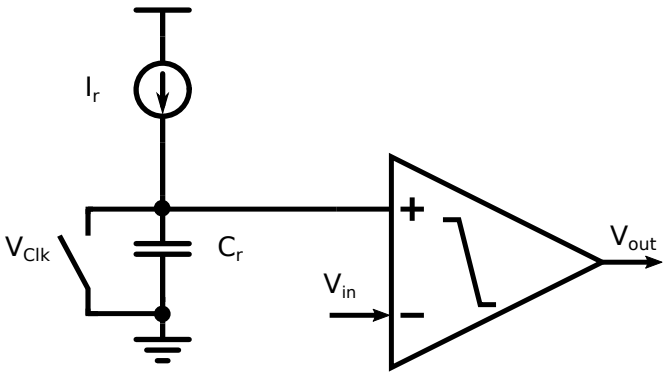


Figure 9: Ramp-and-comparator-based VTC.

When the clock signal 'Clk' is logic high, the ramp capacitor is discharged to ground (0 V), and the comparator output (V_{out}) will be logic low in this phase. As soon as the clock goes to logic low, the constant bias current starts to integrate over a fixed capacitor to generate a ramp, as shown in Fig. 10, and the time-to-digital conversion starts simultaneously. The generated ramp will be given by (3.3). When the ramp crosses the input signal (V_{in}), the comparator's output (V_{out}) switches to logic high, signaling the end of time-to-digital conversion. Therefore,

$$\int_0^{t_c} dt = \frac{C_r}{I_r} \int_0^{V_{in}} dV \,,$$
$$t_c = \frac{C_r}{I_r} V_{in} \,. \tag{3.8}$$

Since peak ramp voltage has to be equal to the full scale input signal, this puts a limit on the upper level of the input signal. This is because any real bias current, designed using transistors, requires a minimum voltage headroom for proper operation. In case the minimum voltage headroom limitation is violated, the bias current will change, inducing non-linearity in the operation of the VTC. This limitation is also known as 'bias compliance' voltage for the current source. This non-linearity effect will be discussed further in Section 4.1.2.

The benefits and the shortcomings of this structure are summarized as follows:

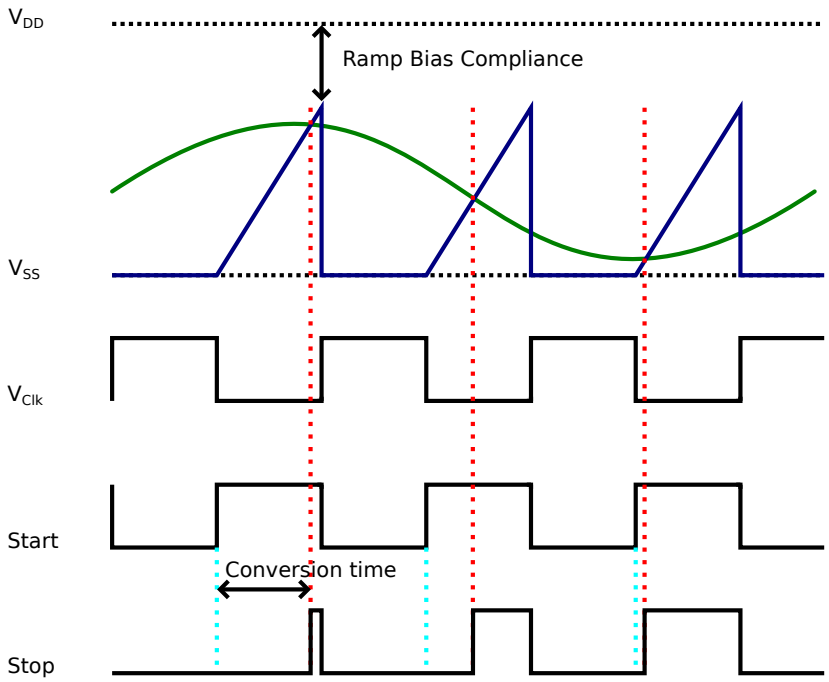


Figure 10: Timing diagram of the ramp-and-comparator-based VTC.

- **Advantages:** Observing (3.8), it should be clear that the generated ramp is quite linear, and resolution of more than 6 bits could be possible using this architecture. For example, [7] uses this architecture to achieve 7.9 bits of ENOB at 1 $MSPS$ using 14 μW of power. Similarly, [26] achieves an ENOB of 6.45 bits at 80 $MSPS$ while consuming 6.4 mW of power. Furthermore, the input range is only limited by the bias compliance of the ramp, and the output range could be modified to achieve varying ranges based on the speed of the generated ramp.

- **Disadvantages:** The speed of operation is slower compared to CSI-based architecture. Moreover, a comparator has to be designed with high common mode rejection to avoid non-linearities from the comparator. The power consumption of this structure is also higher than that of the CSI-based topology.

Even though there are a few disadvantages of this architecture, the main objective of this thesis is to design high speed and resolution ADCs, which is not possible using CSI-based VTC owing to its limited resolution, as discussed in Section 3.3.1. Hence, ramp-and-comparator based VTC structure will be discussed more in detail in Chapter 4.

3.3.3 Significance of Sample-and-Hold Circuit

VTCs can be designed with or without a preceding sample and hold (S/H) stage. However, as explained in [28, 29], the performance of the ADC degrades severely

when the input signal frequency becomes comparable to the sampling frequency. Hence, S/H stages are of paramount importance in Nyquist rate ADCs. In order to determine the performance degradation without a S/H circuit, lets assume that a sine wave input signal is applied to an ADC, such that

$$V_{in} = V_{peak}\, sin\left(2\,\pi\, f_{in}\, t\right),$$

where V_{in} is the signal at time t with a peak amplitude of V_{peak}, f_{in} is the frequency of the input signal, and t is the time in seconds. For the ADC to accurately convert the analog signal to a digital code, the fastest rate of change of the input signal must not exceed 0.5 LSB during the sampling time. However, a sine wave has the largest rate of change at $t = 0$. Hence, the fastest rate of change will be determined by taking the derivative of the input signal with respect to time at $t = 0$. Thus,

$$\begin{aligned}\frac{V_{in}}{dt} &= \frac{d}{dt}\Big[V_{peak}\, sin\left(2\,\pi\, f_{in}\, t\right)\Big],\\ &= V_{peak}\, 2\,\pi\, f_{in} \cdot\, cos\left(2\,\pi\, f_{in}\, t\right).\end{aligned}$$

At $t = 0$, the cosine term will be equal to 1. Thus, the equation becomes

$$\left.\frac{V_{in}}{dt}\right|_{t=0} = 2\, V_{peak}\, \pi\, f_{in}\,.$$

Furthermore, since the LSB is given by (2.1), it could also be defined as

$$V_{LSB} = \frac{2\, V_{peak}}{2^N}\,.$$

For a clock duty cycle of 50 %, the sampling time will be $t_c = 0.5/f_{clk}$. Therefore, for the ADC to have a performance of N-bits, the change in the input signal should not be more than 0.5 LSB during that time. Hence,

$$\begin{aligned}\left.\frac{V_{in}}{dt}\right|_{t=0} &\leq \frac{V_{LSB}}{2}\,,\\ f_{in} &\leq \frac{f_{clk}}{\pi\, 2^N}\,.\end{aligned}$$

This equation could be rearranged to determine the number of attainable bits as follows:

$$N \leq log_2\left(\frac{f_{clk}}{\pi\, f_{in}}\right). \tag{3.9}$$

From (3.9), it is clear that the performance will be highly degraded when input frequency is closer to the Nyquist rate [29]. In order to corroborate this analysis, an ideal test setup for a time-based ADC was simulated for a sampled and an unsampled system as shown in Fig. 11. Its timing diagram is shown in Fig. 12.

The defined system consist of an ideal ramp generator, comparators and 15-bit time-to-digital converters. However, one of the time-based ADC was fed the input signal after an S/H circuit. Both ADCs were provided a clock of 256 MHz with

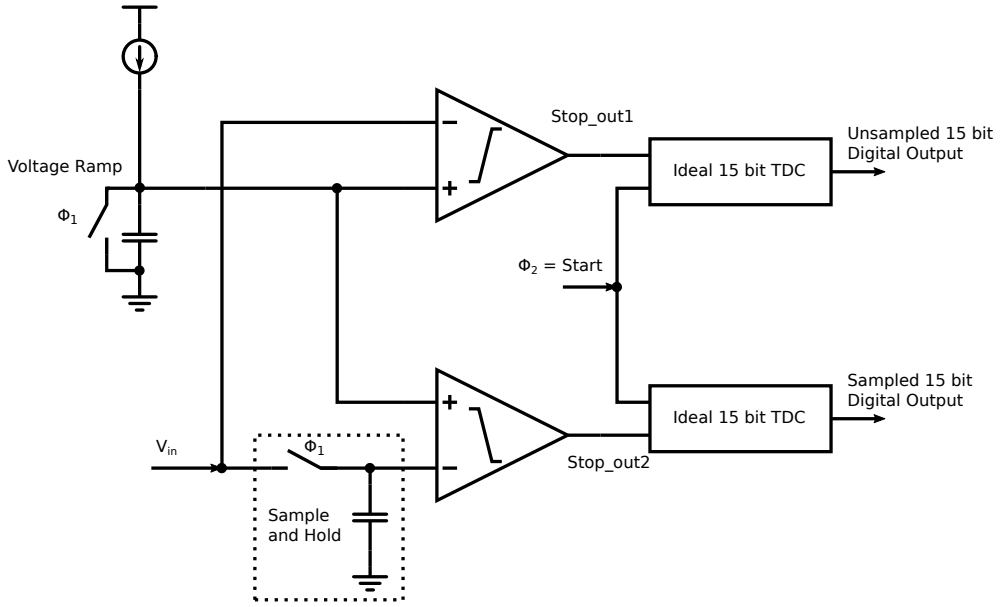


Figure 11: Simulation test bench to corroborate the effect of sampling on the performance.

50 % duty cycle. The ENOB of the corresponding outputs in the simulation were calculated as shown in the Fig. 13. Analyzing the simulation results, it should be obvious that without a S/H circuit, obtaining higher linearity at the Nyquist rate might not be possible.

The advantages and disadvantages of not using a S/H circuit are summarized as follows:

- **Advantages:** S/H circuit increases the complexity of designing the converter. Moreover, the capacitor loads the input buffer for the ADC, which becomes problematic at very high input frequencies.
- **Disadvantages:** As is evident from (3.9), S/H circuit is extremely important to achieve high linearity in Nyquist-rate converter.

Since, the objective of this thesis is to design a Nyquist-rate high-speed ADC, a S/H circuit will be incorporated in the VTC design.

3.4 Time-to-Digital Converters

The main function of a time-to-digital converter is to measure a time interval between two events. Time interval measurement is not a new concept, and it has been applied in various applications such as laser range-finders [30], high energy physics applications [31] and phase measurements [32]. However, due to the diminishing gate delays in modern CMOS processes, TDCs are gaining a lot of interest in all digital phase-locked-loops [33] and in time-based ADC designs.

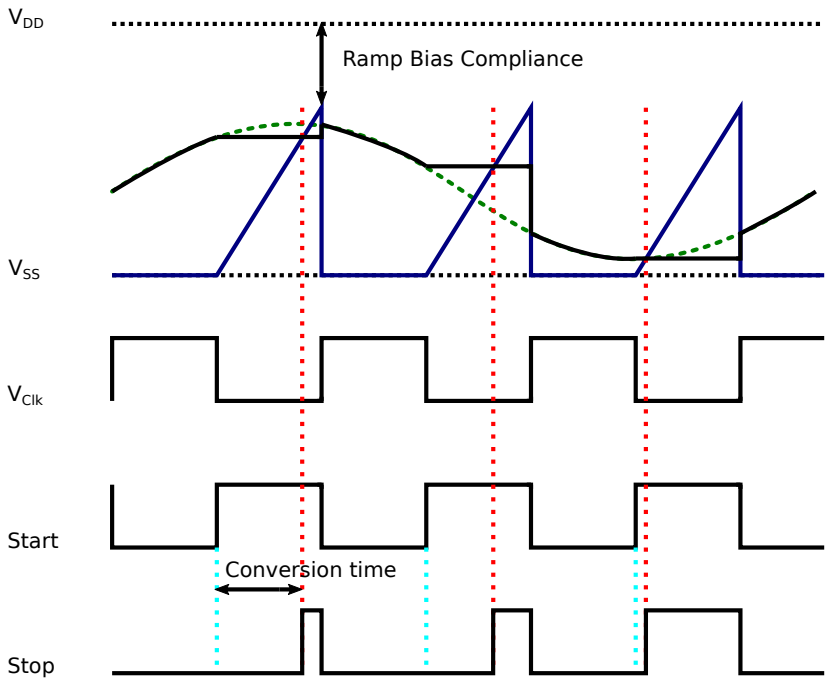


Figure 12: Timing diagram of sampled ramp-and-comparator-based VTC.

There are various architectures of TDCs, and each has its benefits as well as shortcomings. Nonetheless, each structure follows a similar operation principle. The TDC block has two inputs, a start signal and a stop signal, as is shown in Fig. 6. The start signal indicates the beginning of time-to-digital conversion process. At that instant, a digital counter or a delay line keeps track of the time elapsed till the stop signal arrives. When the stop signal is asserted high, the conversion completes, and the TDC transforms the calculated time into a binary N-bits output for the complete time-to-digital conversion.

Irrespective of the topology employed for time-to-digital conversion, there are two important aspects that define the performance of a TDC; its resolution and its complete range. Similar to voltage-domain ADC architectures, certain TDC architectures are better suited for larger range, whereas others are good at achieving higher resolution. Some of the commonly used TDCs are mentioned as follows:

- **Delay-Chain:** Delay-chain TDCs are simplest among time-to-digital conversion techniques. They could be considered as the time-domain counterpart of the flash ADCs. For an N-bit operation, a delay-chain-based ADC will require a cascade of $2^N - 1$ delay stages. Moreover, the throughput is limited to the delay of a single buffer in a particular technology node. Details of the delay-chain-based TDC are described in Appendix B.1.

- **Delay-Ring:** Delay-ring-based TDC is quite similar to delay-chain TDC in its operation. However, instead of employing a simple delay-chain with $2^N - 1$ stages, it uses M delay stages that loop over itself. Consequently, the same ring

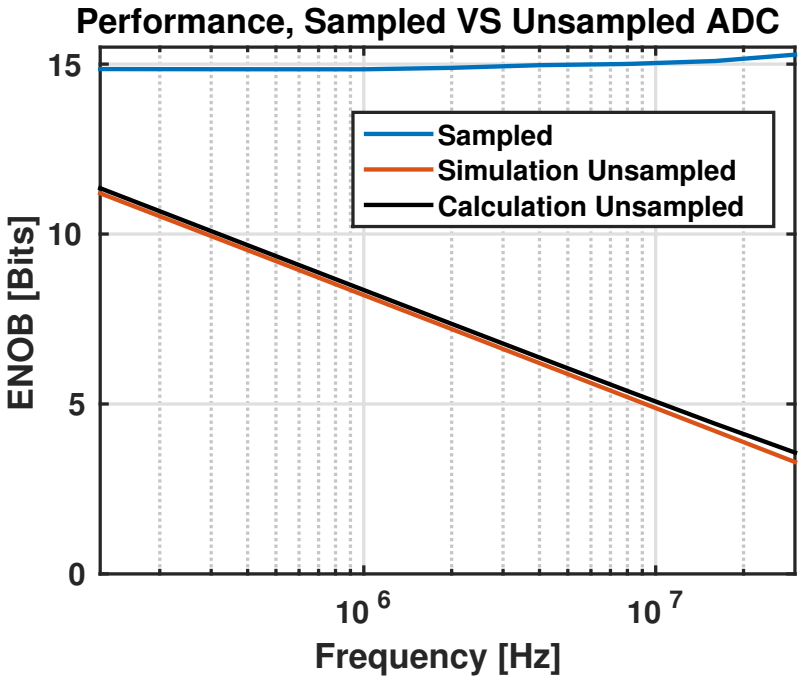


Figure 13: Simulation results for the sampled, unsampled and calculated performance.

could be used for different resolutions of the TDC. However, some additional counters and flip-flops are incorporated for proper operation of the design. Details of the delay-ring-based TDC are described in Appendix B.2.

- **Vernier-Chain:** Timing resolution of the delay-chain and delay-ring based TDCs are limited by the gate delay within the technology node. However, timing resolution below the smallest gate delay can be achieved using vernier delays. A vernier-delay-chain employs two delay chains, each having $2^N - 1$ stages with slightly different unit delays, and the timing resolution is defined by the difference between the unit delays in the two chains. Details of the vernier-chain-based TDC are described in Appendix B.3.

- **Vernier-Ring:** Similar to the delay-ring, vernier-ring-based TDC employs two rings of M delays, with each ring having a slightly different delay compared to the other. Details of this TDC are described in Appendix B.4.

- **Hybrid TDC:** Hybrid TDC contains a combination of coarse and fine time-to-digital conversion sections in order to increase the throughput as well as the resolution of the TDC. Details of this TDC are described in Appendix B.5.

- **Pipelined TDC:** Similar to voltage-domain pipelining, time-domain pipelined TDCs attains larger resolution and throughput by cascading a number of high-speed and low-resolution TDCs along with residue amplification. Details of the pipelined TDC are described in Appendix B.6.

4 Voltage-to-Time Converter Design

This chapter presents the general design constraints in a ramp-and-comparator VTC architecture. Furthermore, the chapter also determines the key factors limiting the linearity of this architecture, and proposes design modifications to enhance its performance. Additionally, The final optimized structure of the VTC is implemented to have a differential topology for a robust operation against the common mode as well as the power supply noise sources.

4.1 Design of the Ramp-and-Comparator VTC

As discussed in section 3.3.1, the performance of CSI-based VTC is limited to 6 bits. Hence, the VTC will be designed using the ramp-and-comparator topology with a preceding S/H circuit. The block diagram of a ramp-and-comparator architecture is shown in the Fig. 14.

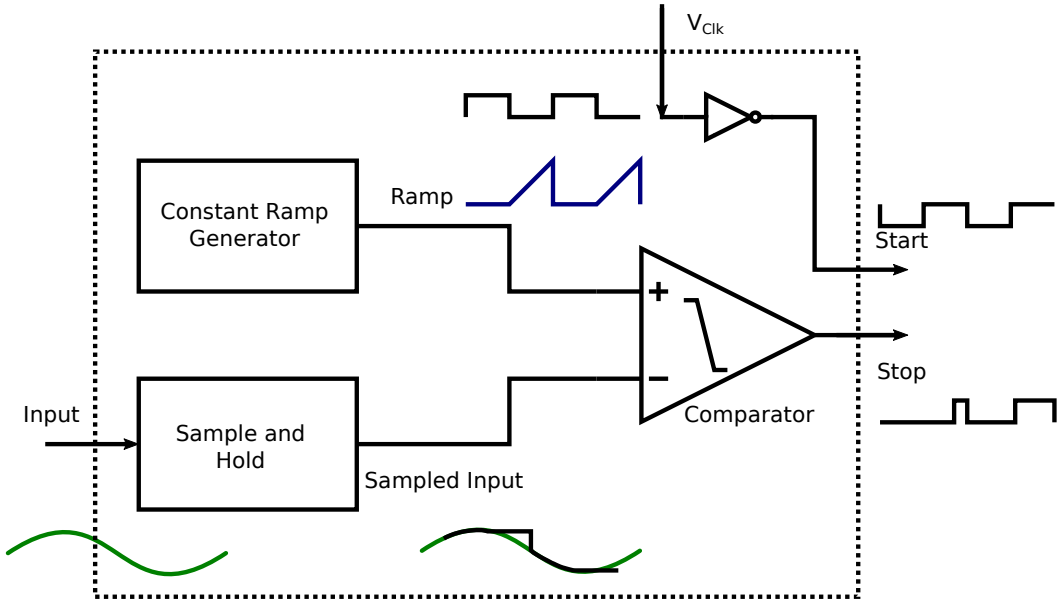


Figure 14: Block diagram of the selected VTC architecture.

Based on the functionality, this topology has three distinct functional blocks within its structure. They are:

- **Sample-and-Hold Circuit:** The first stage is a sample-and-hold (S/H) circuit. As the name suggests, its main function is to linearity charge a capacitor during the sampling phase, and disconnect the capacitor from the input source completely during the hold phase.
- **Constant Ramp Generator:** This block generates a constant ramp by integrating a DC current into a capacitor over a fixed period of time. Its main

function is to maintain the slope from the bottom to the top of the ramp as well as from sample-to-sample.

- **Comparator:** This block compares the ramp with a reference voltage, and provides an output when the ramp voltage crosses that reference level.

The VTC takes input and clock signals, and provides outputs of 'start' and 'stop' signals, which are the expected inputs of the TDC. The 'start' signal can just be the invert of the clock, whereas the 'stop' signal is the respective input dependent output of the VTC.

4.1.1 Sample-and-Hold Circuit

The S/H is very critical stage in the entire ADC, as the performance of the ADC cannot usually exceed more than the performance of its S/H circuit. Simplest S/H stage could be designed using a single transistor switch and a capacitor. However, the input signal could have coupled noise from numerous adjacent cells as well as various supplies. Hence, input is usually provided as a differential signal to minimize the effects of such noise sources. A single-ended S/H stage along with its sources of non-linearities is shown in Fig. 15.

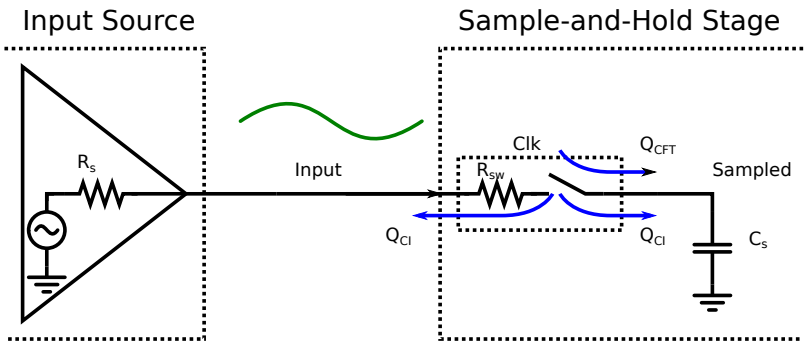


Figure 15: Single-ended S/H circuit with non-linearity contributions.

The 'Input Source' in Fig. 15 is the input buffer for the ADC, and is not included as the inherent part of the ADC. Nonetheless, in designing the S/H circuit, the source impedance is critical and hence, it has been included in the model for designing the S/H circuit.

There are various parameters to consider while designing a S/H block. They include thermal noise, jitter noise, settling time, charge injection (Q_{CI}) and clock-feed-through (Q_{CFT}) issues. Based on these parameters, the limitation and consequently, design parameters can be defined. For instance, the sampling capacitor size will be defined by the thermal noise level, the switch impedance will be defined by the settling time requirements, and the switch size will be limited by the charge injection as well as the clock-feed-through effects. They are described as follows:

- **Thermal Noise:** Thermal noise is the most critical part of S/H design. Therefore, the design process will be initiated by analyzing the thermal noise. From Fig. 15, it could be deduced that the S/H circuit is essentially a low pass filter with a series impedance and a shunt capacitance. However, for an RC type filter, the thermal noise over the passband [34] is determined by

$$\bar{V_{n_{samp}}}^2 = \frac{kT}{C_s}\,, \tag{4.1}$$

where k is the Boltzmann constant, T is the temperature in Kelvin, and C_s is the sampling capacitor. Let N be the resolution of the ADC, and V_{FS} be the full-scale input signal amplitude, then

$$V_{LSB} = \frac{V_{FS}}{2^N}.$$

Moreover, the quantization noise power of an ADC is given by

$$\bar{V_{n_q}}^2 = \frac{{V_{LSB}}^2}{12}\,. \tag{4.2}$$

Now, the thermal noise power should not be larger than the quantization noise power. Therefore,

$$\begin{aligned} \bar{V_{n_s}}^2 &\leq \frac{{V_{LSB}}^2}{12}\,, \\ \frac{kT}{C_s} &\leq \frac{1}{12}\left(\frac{V_{FS}}{2^N}\right)^2, \\ C_s &\geq \frac{12 \cdot 2^{2N}\, k\, T}{{V_{FS}}^2}\,. \end{aligned} \tag{4.3}$$

Hence, from (4.3), it is apparent that the minimum size of the sampling capacitor is limited by the thermal noise level, and is defined based on the resolution of the converter as well as the full-scale input signal level.

- **Jitter Noise:** Jitter noise becomes a serious concern for high-speed ADCs, as it becomes a dominant SNR limiting factor at high signal frequencies [35–37].

Assuming that a sinusoidal signal is applied to an ADC having a full-scale amplitude of V_{FS}, a frequency of f_{in}, and the clock signal RMS jitter specifications of t_{jitter}, then, from [37], the jitter error power will be given by

$$E(e^2) = 2\,(\pi f_{in} V_{FS} t_{jitter})^2\,. \tag{4.4}$$

Therefore, the jitter limitation on SNR [35, 36] can be determined from

$$SNR = -20\, log_{10}(2\pi f_{in} t_{jitter})\,. \tag{4.5}$$

Analyzing (4.5), it is clear that the SNR limitations by the jitter noise is independent of the sampling frequency. Hence, clock signals of very low jitter become necessary for Nyquist-rate or undersampled converters.

- **Settling Time:** The settling time of the S/H circuit is dependent on the time constant of the stage. Referring to Fig. 15, the time constant is given by

$$\tau = R_{eq}\, C_s\,.$$

Here,

$$R_{eq} = R_s + R_{sw}\,, \tag{4.6}$$

where R_s is the source impedance, and R_{sw} is the 'ON' switch impedance. For the ADC to have N bits of resolution, it should be settled within at least 0.5 LSB level during the sampling time. Hence, the impedance of the source and the switch become critical. To determine the minimum time required for 0.5 LSB settling, consider the case of a S/H circuit as depicted in Fig. 15. The voltage at time t will be given by

$$V_{(t)} = V_{in}\,(1 - e^{-t/\tau})\,.$$

Taking natural log on both sides and rearranging, the equation becomes

$$t = -\tau\; ln\left(1 - \frac{V_{(t)}}{V_{in}}\right).$$

For the worst case scenario, the input will take a step equal to the full-scale signal. Hence, it should settle to 0.5 LSB. The voltage at this setting level will be given by

$$V_{(t)_{LSB/2}} = V_{FS} - \frac{V_{FS}}{2^{N+1}}\,.$$

Thus, for $V_{in} = V_{FS}$, the settling time will be given by

$$t_{LSB/2} = -\tau\; ln\left(1 - \frac{V_{(t)_{LSB/2}}}{V_{FS}}\right).$$

Hence,

$$t_{LSB/2} \geq -R_{eq}\, C_s\; ln\left(\frac{1}{2^{N+1}}\right). \tag{4.7}$$

In other words, this equation could be used to determine the impedance level required for N bit settling in a certain amount of time, as given in the following equation:

$$R_{eq} \leq \frac{t_{LSB/2}}{ln(2^{N+1})\, C_s}\,. \tag{4.8}$$

Thus, from (4.7), it is apparent that the settling time of the S/H increases with the resolution of the converter. Moreover, from (4.3), it is apparent that the sampling capacitor also increases with increasing the resolution of the ADC. Hence, the source and the switch impedances have to be reduced at higher resolution to attain the required level of settling.

- **Charge Injection:** The switches inside the S/H block are designed using transistors. When the transistor is 'ON', a channel exist beneath the oxide layer. This channel is composed of charges, and the total charge stored in the channel of an NMOS transistor [38] during the 'ON' phase is given by

$$Q_{ch} = C_{ox} W L \left(V_G - V_{in} - V_{tn}\right).$$

When the transistor is turned 'OFF', channel discharges and the charge exits the transistor through its drain and source terminals. However, as described in [38], predicting the amount of charge specifically injected in the source and drain is quite complicated and as such, does not yield any clear rule of thumb. Nonetheless, it is quite a common practice to assume equal amount of charge injection in the source and the drain terminals. Consequently, the charge injected onto the sampling capacitor results in inducing non-linearity. Utilizing the general assumption, approximate amount of charge entering the sampling capacitor is given by

$$Q_{ch} = \frac{C_{ox} W L \left(V_G - V_{in} - V_{tn}\right)}{2}.$$

Also,

$$Q = CV.$$

For this case,

$$\Delta V = \frac{Q_{ch}}{C_s}.$$

Thus, the voltage change created by this charge will be given by

$$\Delta V = \frac{C_{ox} W L \left(V_G - V_{in} - V_{tn}\right)}{2\, C_s}. \tag{4.9}$$

Analyzing (4.9), it is apparent that transistors with larger width (W) and length (L) will have higher charge injection effect. Moreover, the injected charge is an input dependent factor, and hence, will induce non-linearity in the sampled output.

- **Clock-Feed-Through:** Clock-feed-through also injects charge onto the sampling capacitor. The injected charge is defined in [38], and the voltage change created by this charge is given by

$$\Delta V = \frac{V_{clk}\, W\, C_{ov}}{W\, C_{ov} + C_s}, \tag{4.10}$$

where C_{ov} is the gate-source and gate-drain overlap capacitance. Assuming that $C_{samp} >> C_{ov}$, then (4.10) reduces to

$$\Delta V = \frac{V_{clk}\, W\, C_{ov}}{C_s}.$$

Analyzing the above equation, it is apparent that transistors with larger width (W) will have higher clock-feed-through effect. However, the clock-feed-through is not an input dependent factor, and hence, will be less problematic than charge injection effects.

4.1.2 Ramp Generator

The simplest method to generate a constant ramp is to integrate a DC current on a capacitor for a fixed amount of time and is given by the (3.3). A ramp generation circuit is shown in Fig. 16.

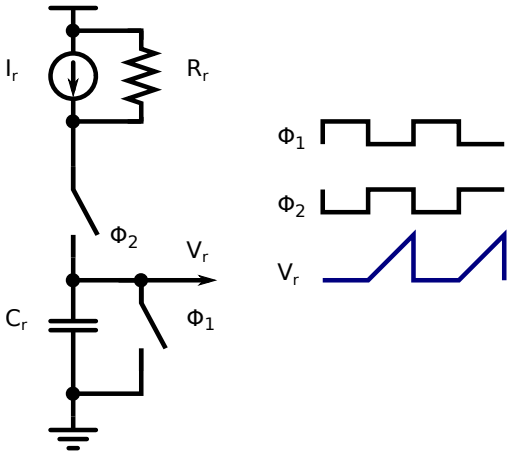


Figure 16: Constant ramp generation with finite output impedance.

There are two main performance limiting factors in a ramp generation circuit. These are the non-linearities due to the finite output impedance of the DC current source and the output noise in the current source.

- **Finite Output Impedance of the Current Source:** Biasing currents are generated using transistors in saturation mode. However, instead of having an infinite output impedance like an ideal current source, transistor based bias currents have a finite output impedance. This impedance is approximately given by

$$r_o = \frac{1}{\lambda\, I_D}\,, \tag{4.11}$$

where I_D is the DC current through the transistor and λ is a technology dependent constant.

To analyze the affect of the finite output impedance on the linearity of the VTC, lets assume a DC bias current I_r with an output impedance of R_r integrated over a capacitor C_r as shown in Fig. 16. If the ramp voltage rises from $0\,V$ to V_{DD} in t_c duration, then the instantaneous output voltage of the ramp (V_r) will be given by

$$V_r = I_r\, R_r\, [1 - e^{-t_c/(R_r\, C_r)}]\,.$$

Since during the conversion phase, V_r is being compared with the input signal (V_{in}), the VTC will provide an output when the $V_r = V_{in}$. Therefore,

$$\begin{aligned} V_{in} &= I_r\, R_r\, [1 - e^{-t_c/(R_r\, C_r)}]\,, \\ t_c(V_{in}) &= -R_r\, C_r\, ln\left(1 - \frac{V_{in}}{I_r\, R_r}\right). \end{aligned} \tag{4.12}$$

Using Taylor series expansion up to third order, we get

$$T(V_{in}) \;\approx\; -R_r\, C_r\, \left[\; 0 \;-\; \left(\frac{V_{in}}{I_r\, R_r}\right) \;-\; \frac{1}{2!}\;\cdot\; \left(\frac{V_{in}}{I_r\, R_r}\right)^2 \;-\; \frac{2}{3!}\;\cdot\; \left(\frac{V_{in}}{I_r\, R_r}\right)^3\right].$$

Hence, the equation could be condensed as

$$T(V_{in}) \approx \frac{V_{in}\, C_r}{I_r} \;+\; \frac{{V_{in}}^2\, C_r}{2\, I_r\, (I_r\, R_r)} \;+\; \frac{{V_{in}}^3\, C_r}{3\, I_r\, (I_r\, R_r)^2}\,. \tag{4.13}$$

Analyzing (4.13), it is apparent that larger output impedance (R_r) will yield better linearity and vice versa. For a single transistor in saturation, this output impedance will be given by (4.11). However, λ increases in successively smaller processes. Hence, impedance boosting techniques might be necessary to increase linearity of the ramp. One method of improving output impedance of the current source is through the addition of cascode transistors. However, lower supply headroom impedes the stacking of multiple cascode transistors.

The effect of finite output impedance could also be mitigated if the voltage over the current source is held constant. This can be achieved by appending a feedback amplifier circuit [39] as shown in Fig. 17.

Assuming that the amplifier has a gain of A_o, then the equivalent impedance of the current source will be given by

$$R_r{}' = R_r\, A_o\,.$$

Then (4.12) becomes

$$\begin{aligned} t_c(V_{in}) &= -R_r{}'\, C_r\, ln\left(1 - \frac{V_{in}}{I_r\, R_r{}'}\right), \\ t_c(V_{in}) &= -R_r\, A_o\, C_r\, ln\left(1 - \frac{V_{in}}{I_r\, R_r\, A_o}\right). \end{aligned} \tag{4.14}$$

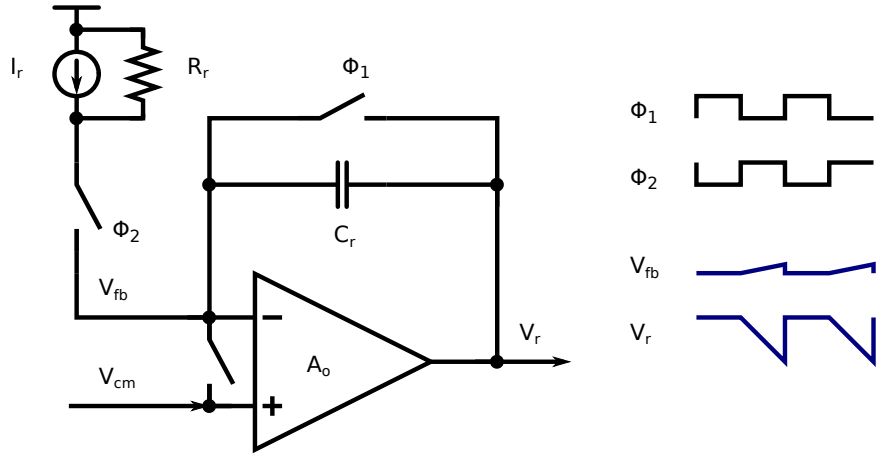


Figure 17: Current source impedance boosting with an amplifier.

Hence, (4.13) becomes

$$T(V_{in}) \approx \frac{V_{in}\, C_r}{I_r} + \frac{{V_{in}}^2\, C_r}{2\, I_r\, (I_r\, R_r\, A_o)} + \frac{{V_{in}}^3\, C_r}{3\, I_r\, (I_r\, R_r\, A_o)^2}\,. \tag{4.15}$$

Analyzing (4.15), it is clear that an opamp can be incorporated in the ramp generator to relax the output impedance limitations of ramp-and-comparator based VTC. Hence, this method will be employed in the proposed architecture to increase linearity of the VTC.

- **Noise of the Current Source:** Since the input signal level is being compared with the ramp, it is very critical to reduce the noise level of the bias current as well. The effect of noise current on the ramp is shown in Fig. 18.

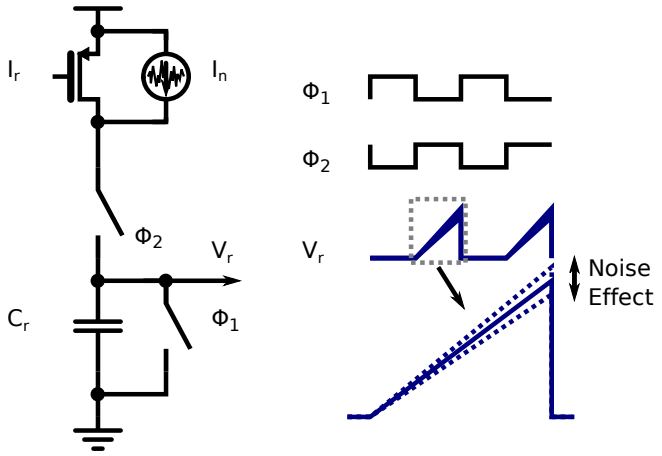


Figure 18: Effect of noise on the ramp.

The noise spectral density of a CMOS transistor based current source is mentioned in [38], and is given by

$$\bar{I_{n_r}}^2 = 4kT\gamma g_m \,.$$

Now, from [40],

$$\begin{aligned} \bar{V_{n_r}}^2 &= \frac{\bar{I_{n_r}}^2}{2C^2}\, t_c \,, \\ \bar{V_{n_r}}^2 &= \frac{2kT\gamma g_m}{C^2}\, t_c \,. \end{aligned} \tag{4.16}$$

However, again, this noise voltage should be less than the quantization noise. Then

$$\begin{aligned} \bar{V_{n_r}}^2 &\leq \frac{(V_{FS})^2}{12 \cdot 2^{2N}} \,, \\ \frac{2kT\gamma g_m}{C^2}\, t_c &\leq \frac{(V_{FS})^2}{12 \cdot 2^{2N}} \,, \\ N &\leq 0.5\, log_2 \left[\frac{(V_{FS}C)^2}{24kT\gamma g_m t_c}\right] . \end{aligned} \tag{4.17}$$

For a MOS transistor,

$$g_m = \frac{2I_D}{V_{OV}} \,. \tag{4.18}$$

where V_{OV} is the overdrive voltage of the transistor. For an NMOS, it is given by $V_{OV_n} = V_{GS} - V_{tn}$ and for PMOS, it is given by $V_{OV_p} = V_{SG} - |V_{tp}|$.

Analyzing (4.17) and (4.18), it is apparent that for a certain ramp slope, the noise improves only with $\sqrt{V_{OV}}$ and the overdrive voltage is limited by V_{DD}. Nevertheless, since the slope is defined by I/C, doubling the current and capacitor will maintain the slope while simultaneously reducing the current noise to $\sqrt{\bar{I_n}}$. However, since the conversion time (t_c) is in the denominator, hence, the noise performance will degrade at lower sampling frequencies and vice versa.

To analyze the noise effects of impedance boosting amplifier, refer to the Fig. 19.

In addition to the noise from the ramp generating current source, there will be an additional noise from the amplifier. The input referred noise for a differential pair amplifier is given in [38], and can be approximated to

$$\bar{V_{n_{amp}}}^2 \approx \frac{8kT\gamma}{g_{m_{amp}}} \,. \tag{4.19}$$

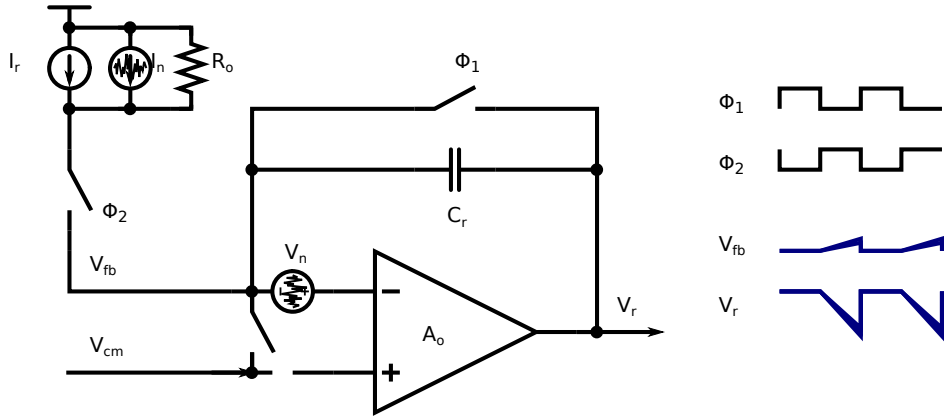


Figure 19: Effect of Noise on the impedance boosted ramp.

4.1.3 Comparator

Non-linearity is a less critical parameter in defining the performance of the comparator for the ramp-and-comparator VTC. However, input referred noise, common mode rejection and propagation delay are critical, and will be analyzed in the proceeding sections.

- **Input Referred Noise:** Comparator is inherently an open loop differential amplifier. Therefore, similar to an amplifier, the comparator will have an input referred noise component [38] given by

$$\overline{V_{n_{comp}}}^2 \approx \frac{8kT\gamma}{g_{m_{comp}}},$$

  where $g_{m_{comp}}$ is the transconductance of the input transistors of the comparator. This noise will be at the output of another amplifier in impedance boosted ramp generator. Hence, it could further be referred back to the input of the impedance boosting opamp, and this noise component will become

$$\overline{V_{n_{comp_{amp}}}}^2 \approx \frac{8kT\gamma}{{A_o}^2\, g_{m_{comp}}}, \tag{4.20}$$

  where A_o is the gain of the impedance boosting amplifier.

- **Common Mode Rejection:** An important issue with the structure of Fig. 9 is the input common mode range. Therefore, the designed comparator is supposed to have a large operating common mode range. In other words, it should have a good common mode rejection ratio for a large input range. For example, referring to Fig. 12, the common mode input signals constantly keeps changing, based on the input signal level. The problem can be mitigated by sampling the input signal onto a capacitor, and then generating the ramp over

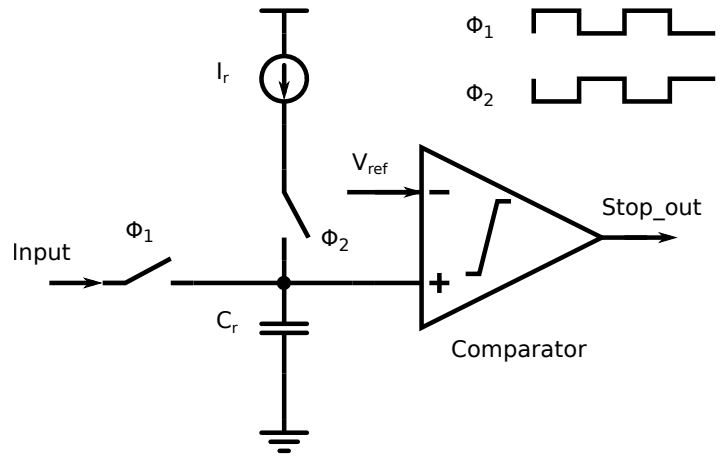


Figure 20: VTC with single capacitor for sampling and ramp generation.

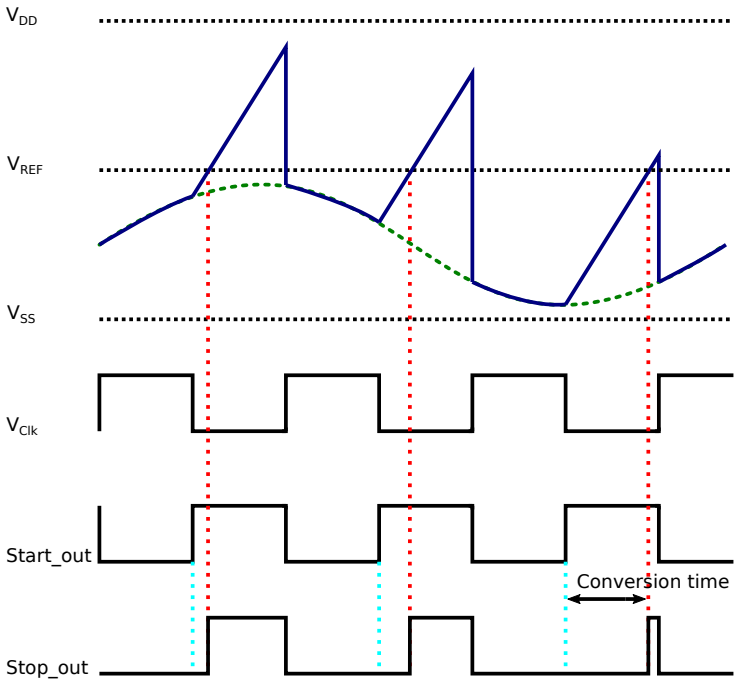


Figure 21: Timing Diagram of VTC with single capacitor for sampling and ramp generation.

the same capacitor. The resulting circuit and its timing diagram are shown in Figs. 20 and 21 respectively.

Consequently, by sampling the input signal and generating the ramp onto the same capacitor ($C_s = C_r$), the input common mode for the comparator will remain fixed throughout the conversions, independent of the input signal level, since the comparator always compares the ramp with a constant reference voltage as shown in Fig. 21.

- **Propagation Delay:** The comparator takes a finite amount of time to generate the output results. Consequently, there is a propagation delay from the input to the output. This propagation delay will reduce the VTC output range. The delay could be minimized by increasing power consumption of the comparator. However, the objective in this thesis is to simply optimize the delay with minimum possible power consumption.

4.2 Optimized Single-Ended Architecture

In order to further improve the performance of the VTC, two modifications have been implemented in the design. These include incorporating a gain boosting opamp with the current source, and using a single capacitor for sampling as well as ramp generation to simplify comparator design.

By incorporating a gain boosting opamp into the ramp generator, the output voltage of the current source of the ramp generator will be fixed at V_{cm}. However, this will lead to clipping of the output time-signal of the VTC, if the input signal also swings around V_{cm}. This issue can be analyzed by considering the schematic and its timing diagram shown in Figs. 22 and 23 respectively.

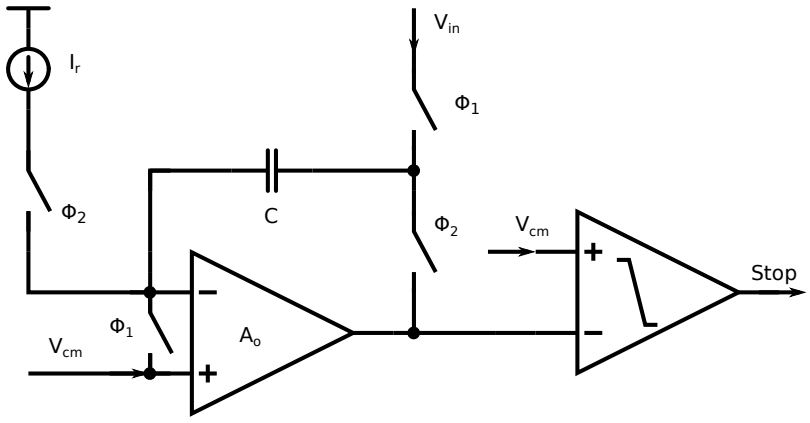


Figure 22: Impedance boosted VTC with sampling common mode voltage issue.

Lets assume that the input signal (V_{in}) has a peak of $V_{DD}/4$ around the common mode voltage (V_{cm}) of $V_{DD}/2$, and the reference voltage for the comparator is also equal to the V_{cm}. The assumption for comparator reference voltage should be valid, as the final objective is to design a differential VTC, where the comparator will compare differential input ramps instead of a single ramp w.r.t. a reference voltage.

When the input signal level is greater than V_{cm}, the voltage stored onto the sampling capacitor will be positive, and the generated ramp will start from an initial voltage above the comparator's reference. Therefore, the output of the VTC will ramp down for a finite amount of time (greater than zero) to cross comparator's reference voltage, and the resulting time-signal output will be proportional to the input signal level.

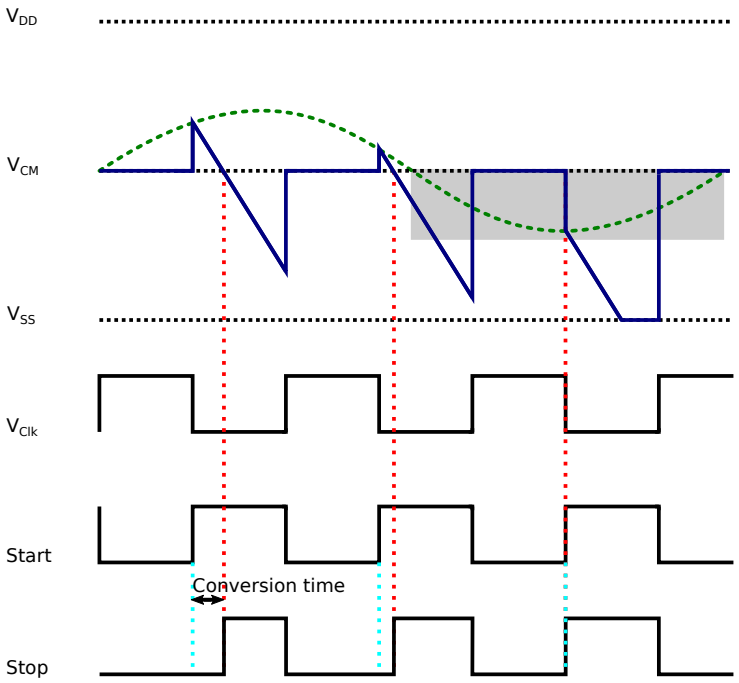


Figure 23: Timing Diagram of Impedance boosted VTC with sampling common mode voltage issue.

However, when the input signal level goes below V_{cm}, the voltage stored onto the sampling capacitor will be negative, and generated ramp will instead start from a voltage level below the comparator's reference during the conversion phase. Hence, the output of the VTC will assert stop-signal as logic high as soon as the conversion starts for all the input signal levels below V_{cm}, thereby clipping the output. This is represented in the Fig. 22 by the shaded region.

This issue can be rectified by incorporating a separate reference voltage (V_{ref}) for the capacitor during the sampling phase, where the value of this reference voltage should be equal to the lowest voltage level of the input signal. The modified circuit and its timing diagram are shown in Figs. 24 and Fig. 25 respectively.

Consequently, the resulting voltage stored onto the capacitor will be positive for all input voltages either above or below V_{cm} level and hence, the issue of clipping of the output time-signal will be resolved.

At this point, the single ended architecture of the VTC has been completely determined. Therefore, the transfer function and the noise analysis of this VTC will be presented in the following section.

- **Transfer Function:** The ramp is generated during the conversion phase. The transfer function of this VTC in that phase is given by (3.8). However, there will be non-zero settling time delay of the opamp as well as propagation delay of the comparator. Hence, the transfer function could be modified to include these delays as follows:

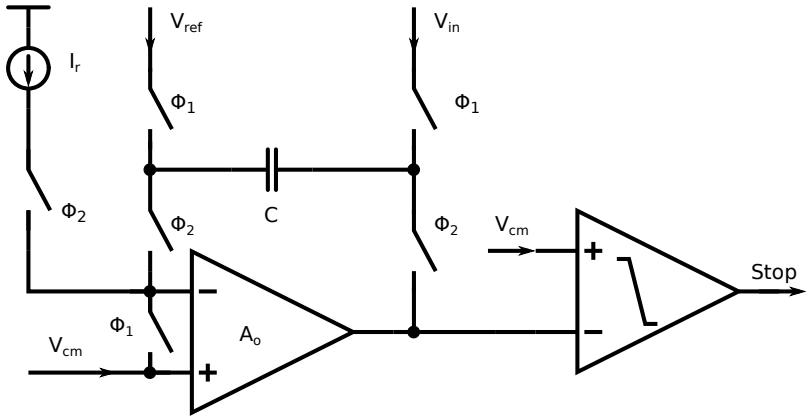


Figure 24: Impedance boosted VTC with dedicated reference voltage during sampling phase.

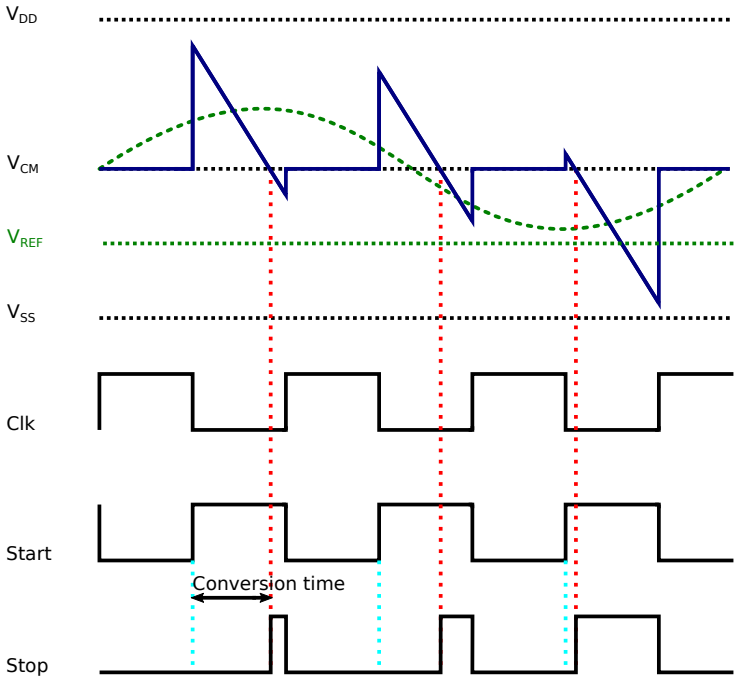


Figure 25: Timing diagram of impedance boosted VTC with dedicated reference voltage during sampling phase.

$$t_{out} = V_{in}\frac{C_r}{I_r} + t_{del_{amp}} + t_{del_{comp}}, \tag{4.21}$$

where $t_{del_{amp}}$ is the settling delay of the opamp and $t_{del_{comp}}$ is the propagation delay of the comparator. Since the $t_{del_{amp}}$ and the $t_{del_{comp}}$ will limit the output range of the VTC, they should be minimized as much as possible to maximize th output range of the VTC. However, minimizing these delays require larger power

consumption in the opamp and the comparator (to attain larger bandwidth). Thus, the delays have to optimized in contrast with the power consumption and the operating frequency of the VTC.

- **Noise:** The overall noise of this VTC can be determined from equations 4.1, 4.16, 4.19 and 4.20. The combination of these noise sources should be less than the quantization noise of the ADC. Therefore

$$\frac{kT}{C_s} + \frac{2kT\gamma g_m t_c}{{C_s}^2} + \frac{8kT\gamma}{g_{m_{amp}}} + \frac{8kT\gamma}{{A_o}^2 g_{m_{comp}}} \leq \frac{(V_{LSB})^2}{12}\,. \tag{4.22}$$

4.3 Proposed Differential VTC Architecture

The structure discussed so far has been single ended in its operation. However, single ended analog circuits are quite prone to interfering signals coupled from other circuits or via the power supplies. Therefore, this thesis proposes a differential architecture to minimize the common mode interference and noise effects from the performance of the VTC. The finalized structure of the VTC along with this timing diagram are shown in Figs. 26 and 27 respectively.

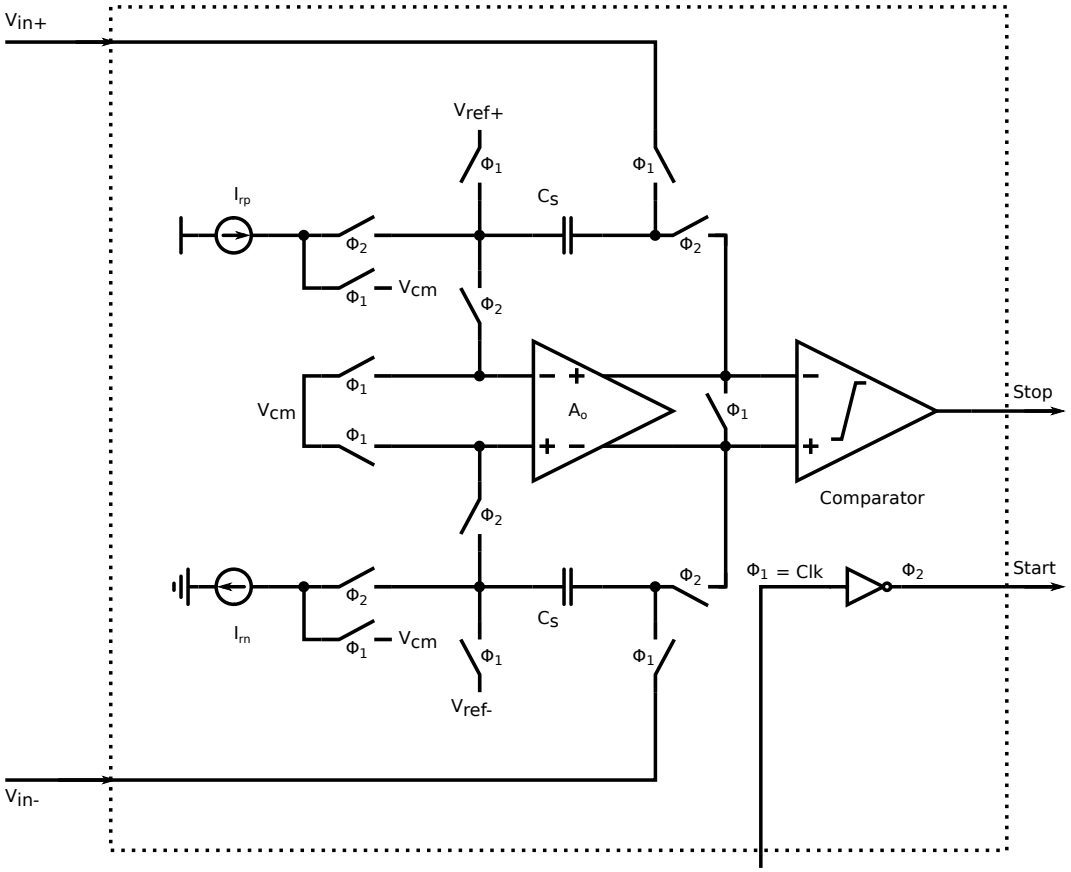


Figure 26: Proposed differential VTC.

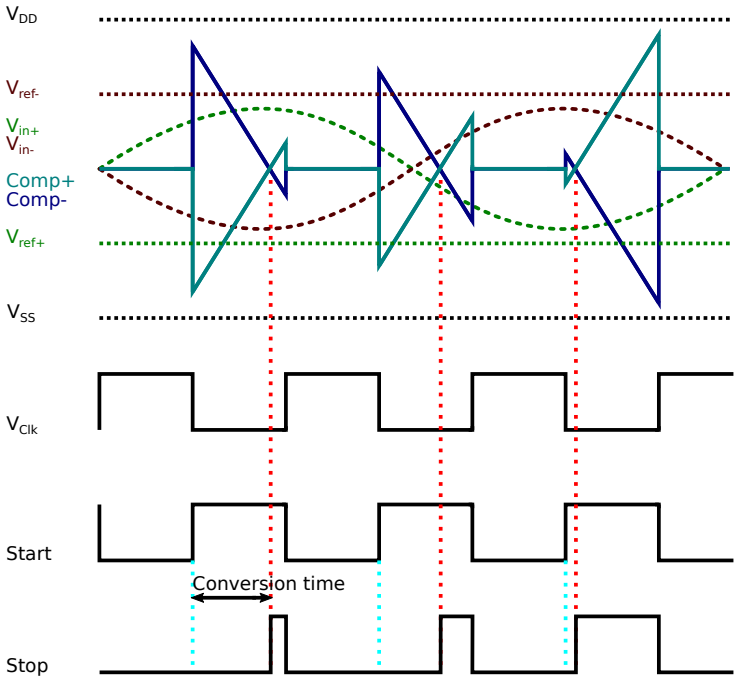


Figure 27: Proposed differential VTC timing diagram.

The proposed architecture is the differential counterpart of the optimized single-ended structure discussed in Section 4.2. It consist of two sampling capacitors for the differential positive and negative inputs, two ramp generators with a positive and a negative slope, and a comparator. During the sampling phase, the positive input V_{in+} is sampled onto a capacitor with reference to V_{ref+} (equal to lowest input voltage level) and the negative input V_{in-} is sampled onto another capacitor with reference to V_{ref-} (equal to highest input voltage level).

During the conversion phase, a current source 'I_{rp}' (PMOS) creates a ramp with a negative slope at the negative terminal of the comparator and a current sink 'I_{rn}' (NMOS) generates a similar ramp but with a positive slope at the positive terminal of the comparator. When both the ramp voltages crosses each other, output of the comparator is asserted high to signal the end of voltage-to-time conversion.

Assuming that $I_{rp} = I_{rn} = I_r$, then the transfer function for the differential VTC will be given by

$$t_{out} = \frac{V_{in_{diff}}}{2}\frac{C_r}{I_r} + t_{del_{amp}} + t_{del_{comp}}\,. \tag{4.23}$$

5 Transistor Implementation and Results

This chapter presents the transistor level implementation as well as the simulation results of the VTC proposed in Section 4.3. The implementation will be described at block levels in the VTC. There are three distinct blocks in the VTC. They are the sample-and-hold circuit, the ramp generator and the comparator. Since the aim of this work is to demonstrate the speed and linearity performance of a VTC, hence, the target has been set to design a low power VTC for a Nyquist rate TBADC with an output linearity of at least 8 bits of ENOB while sampling beyond 200 MHz of clock frequency at 1 V_{pk-pk} full-scale (FS) signal. Furthermore, the transistor level circuits will be implemented in 28 nm CMOS technology using 1 V of power supply.

5.1 Sample-and-Hold Circuit

The S/H block contains the sampling switch and the capacitor. Their design parameters will be discussed in the following sections.

5.1.1 Sampling Capacitor

The size of the sampling capacitor is determined by the thermal noise, as is given by the (4.1). Here, k is the Boltzmann constant ($k = 1.38 \cdot 10^{-23} m^2 kg\, s^{-2} K^{-1}$), T is the temperature is ($T = 300K$) and V_{FS} is the full-scale input signal ($V_{FS} = 1\, V_{pk-pk_{diff}}$). Even though the target is set to attain a performance of greater than 8 bits ENOB as mentioned in Chapter 4, the capacitor will be selected for thermal noise level of at least 10 bits. This is because of two main reasons. Firstly, there are other noise sources in the system, as is evident from the (4.22), and the objective is to minimize the contribution of every noise source. Secondly, the size of the capacitor should be large enough so that the effect of the parasitic capacitance of the switches or the routing could be minimized.

Since the circuit is differential, one half of the circuit will have a swing of $0.5V$. Therefore, substituting these parameters in (4.3) for 10 bits of thermal noise level, the minimum value of the sampling capacitor is determined to be

$$C_{samp} \geq 208\, fF.$$

However, the capacitor is dimensioned larger in size to keep the noise below 10 bits level. Thus, the selected size is

$$C_{samp} = 277\, fF. \tag{5.1}$$

Analyzing (4.3), it is evident that increasing resolution by one bit will result in a sampling capacitor of 833 fF, which is very large, both in size and as the load for the input buffer. On the other hand, reducing one bit will only reduce the capacitor size to 52 fF. Hence, 10 bit performance should be considered an optimized value for this VTC.

5.1.2 Switches

The switch size is determined by the settling time constraint of the S/H block. Since the capacitor size has been calculated in (5.1), the impedance limitation for the S/H block can now be determined. The setting time will be determined for 12 bits performance, so that it does not become a dominant contributor is limiting the performance of the VTC. Furthermore, the settling time will be limited to $500\,ps$, so that larger time could be allocated for time-to-digital conversion.

Substituting these values in (4.8), the equivalent impedance comes out to be

$$R_{eq} \leq 200\,\Omega\,.$$

However, from (4.6), the total impedance is determined by a combination of source and switch impedance. Moreover, (4.6) was determined for single ended scenario. Therefore, for the differential case, it becomes

$$R_{eq} = 2\,(R_s + R_{sw})\,.$$

If the single ended source impedance (R_s) is assumed to be a $50\,\Omega$, then the switch impedance should be

$$R_{sw} \leq 50\,\Omega\,. \tag{5.2}$$

The impedance of a MOS transistor in triode region is given by

$$R_{ON} = \frac{1}{k'\frac{W}{L}V_{OV}}\,. \tag{5.3}$$

There are numerous methods of designing the switch in CMOS processes. These include employing a single MOS transistor, a transmission gate or a boot-strapped switch.

A single MOS transistor could be employed as the switch. However, the V_{OV} of the transistor during ON state will be dependent on the input signal level. At peak value of the input signal, the V_{OV} could becomes less than zero. Consequently, the transistor might go into the cut off region. Hence, single MOS transistor based switch is not a viable option for the switch.

A transmission gate provides a better alternative to a single MOS transistor. A transmission gates is simply a PMOS and an NMOS transistor with their drains and sources shorted together, whereas the gates are connected to inverted signals. Since one of the transistors within the transmission gates will be ON at the peak input signal levels, it operates over the entire voltage swing of the input signal. However, the impedance of the transmission gate will vary with the input signal level, resulting in inducing non-linearity in the sampled signal.

Higher linearity could be achieved if a boot-strapped switch is incorporated in the S/H circuit [41]. The schematic for the boot-strapped switch is shown in Fig. 28.

A brief description of the operation of this switch is as follows. When the clock is logic low, the gate of the switch transistor M_1 is connected to V_{SS} through transistors M_{10} and M_{11}, while the level shifting capacitor C_{BAT} gets charged to V_{DD} through transistor M_5.

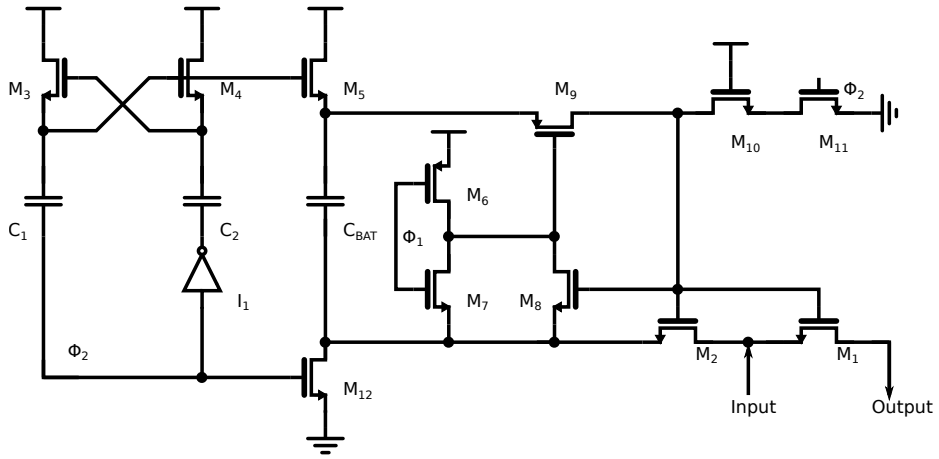


Figure 28: Boot-strapped switch.

When the clock is asserted high, one terminal of capacitor C_{BAT} gets connected to the input signal via M_2. Since the capacitor hold a voltage equal to V_{DD} in it, the other terminal jumps to $V_{DD} + V_{in}$. Hence, V_{GS} of M_1 remains at V_{DD} irrespective of the input signal level. Consequently, the impedance of the switch remains constant and independent of the input signal level. This is evident from the comparison of the simulation results obtained by sweeping the input signal from 0 V to V_{DD} and plotting the respective impedance of the transmission gate and a boot-strapped switch, as shown in Fig. 29.

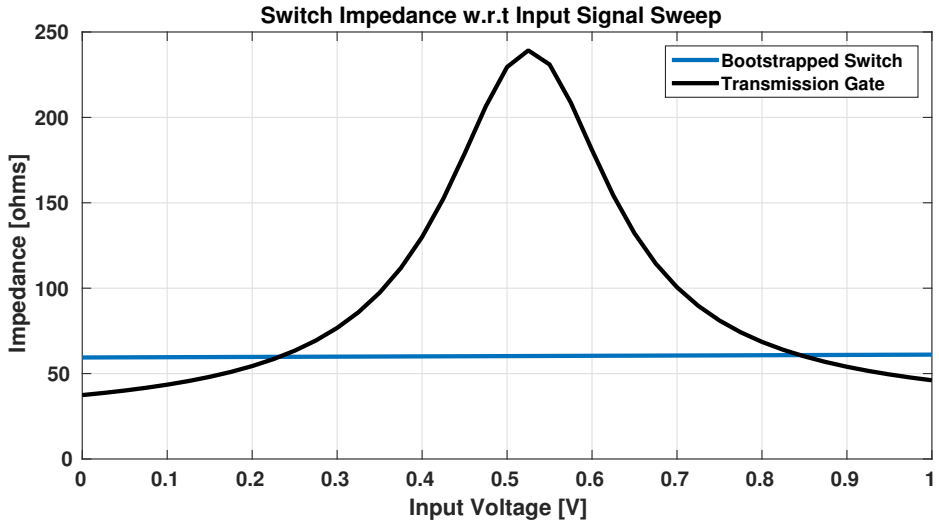


Figure 29: Transmission gate vs boot-strapped switch impedance with input voltage variations.

Furthermore, since the settling time becomes independent of the input signal level in a boot-strapped switch, the linearity of the sampled signal increases as well. To

corroborate this phenomena, an input frequency of 126.5 MHz with a clock frequency of 256 MHz was applied to both the transmission gate and the boot-strapped switch and the linearity of the sampled signal was analyzed. The resulting performance is presented in Fig. 30.

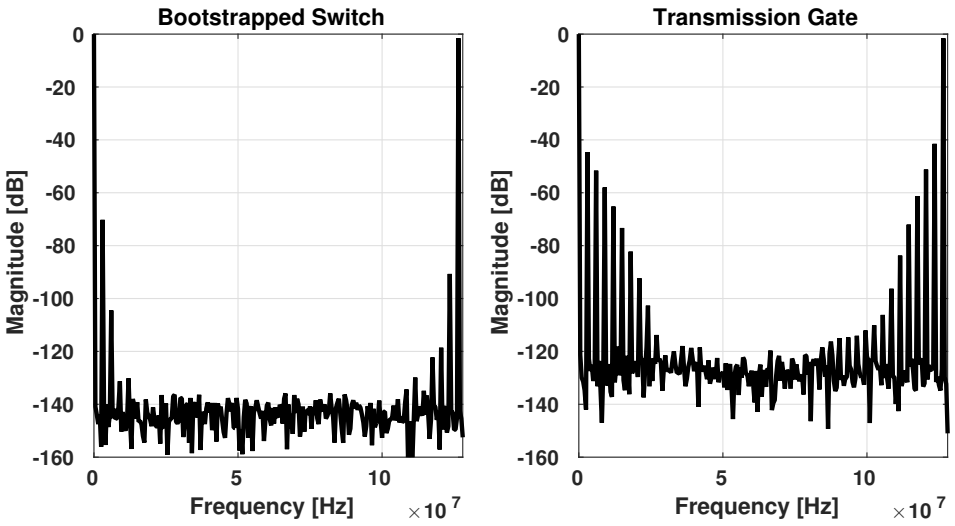


Figure 30: Transmission gate vs boot-strapped switch linearity comparison at 126.5 MHz input frequency.

Thus, higher linearity could be achieved using a boot-strapped switch. For the same sampling capacitor, the transmission gate provide a linearity of 5.9 bits ENOB, whereas the boot-strapped switch provides a linearity of 11.1 bits of ENOB.

There are two drawbacks of boot-strapped switch as well. Firstly, at very slow clock speeds, the capacitor C_{BAT} gets slightly discharged due to leakages through the transistors, resulting in inducing non-linearity. Secondly, since the structure employs three capacitors in the design, it consumes much larger silicon area than transmission gate based switches. Nevertheless, owing to its high linearity, boot-strapped switches are selected for the S/H circuit.

The variation in the output impedance of the designed bootstrapped switch is presented in Table 1.

Table 1: Corner simulation results of the boot-strapped switch impedance.

	Worst Case	Typical Case	Best Case
Impedance [ohms]	78.45	61.10	47.35

5.2 Ramp Generator

The ramp generator consist of a sampling capacitor, a DC current source as well as a current sink and a differential amplifier. Since the same capacitor will be used for

sampling and ramp generation as discussed in Section 4.1.3, therefore, the size of the ramp capacitor has already been determined and is given by (5.1).

5.2.1 Constant Current Sources

An ideal current source can maintain a constant current across its terminals, independent of the voltage variations across it. The condition for saturation region operation for an NMOS transistor is given by

$$V_{DS} \geq V_{GS} - V_{tn} \,.$$

A method of generating a DC current using PMOS transistors is shown in Fig. 31.

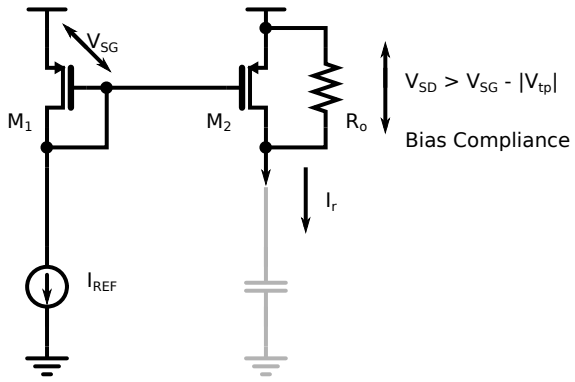


Figure 31: Transistor-based current source.

As discussed in Section 3.3.2, 'bias compliance' is the voltage across a transistor-based bias, necessary to keep the transistors in the saturation region. For a transistor to operate in saturation region

$$V_{DS} \geq V_{sat} \,,$$

where

$$V_{sat} = \sqrt{\frac{2I_D}{k' \frac{W}{L}}} \,. \tag{5.4}$$

Therefore, from (5.4), it is apparent that transistors with larger width have lower V_{sat}, whereas transistors with larger length have higher V_{sat}. Hence, bias compliance voltage could potentially be reduced by increasing the width of the transistor. Analyzing (4.16), it is apparent that increasing width will also increase the g_m of the transistor, resulting in higher noise. Therefore, there is a trade off between compliance voltage and the thermal noise level of a current source.

It can also be observed from (4.12) that the output impedance of the current source should be very large to attain higher linearity from the VTC. Therefore, the impedance of the bias current will be boosted using a cascode transistor. A cascode transistor is inherently a 'common-gate' transistor. When a single cascode transistor is stacked on the bias transistor, the output impedance is boosted by the gain of the

cascode transistor. Assume that output impedance of the bias transistor is R_{o1}, and the gain of the cascode transistor is about $g_{m2}R_{o2}$, then the output impedance would become

$$R_{out} = R_{o1} \cdot g_{m2}\, R_{o2}\,.$$

If the V_{sat} of the transistors is small enough, another cascode transistor could be added to futher boost the output impedance. Assuming that the second cascode transistor has a gain of $g_{m3}R_{o3}$, then the output impedance becomes

$$R_{out} = R_{o1} \cdot g_{m2}\, R_{o2} \cdot g_{m3}\, R_{o3}\,. \tag{5.5}$$

Modified current source and sink with double cascodes, along with cascode biasing voltages are shown in Figs. 32 and 33 respectively.

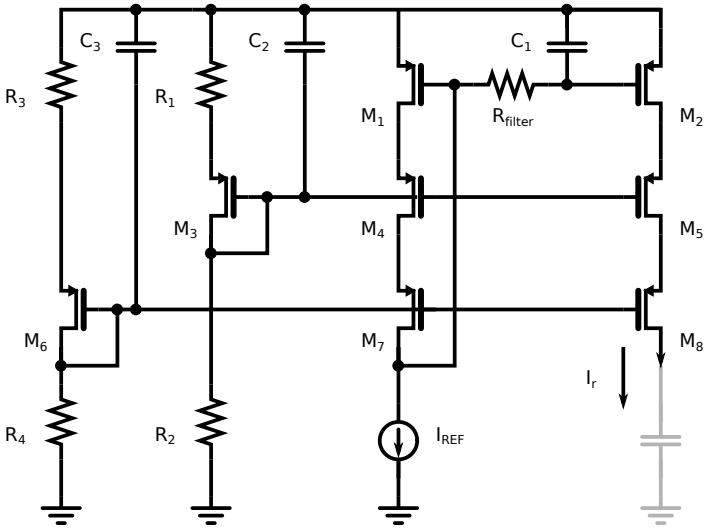


Figure 32: Double cascoded biasing current source for ramp generation.

Now, the value of the DC current can be determined by

$$I_r = \frac{V_{FS}\, C_r}{2\, t_c}\,. \tag{5.6}$$

Here, the sampling clock is selected as 256 MHz, and the sampling time has been reduced to only 500 ps. Therefore, t_c should be approximately 3.4 ns. However, the opamp and the comparator add delays in the output, as is evident from (4.23). Therefore, t_c is reduced to 2.7 ns. Hence, from (5.6), the value of DC current is calculated to be

$$I_r = 58\,\mu A\,. \tag{5.7}$$

The output impedance variations of the current sources w.r.t. the compliance voltage is shown in the Fig. 34. Here, larger voltage means larger headroom across the bias. Hence, it is apparent that the output impedance reduces sharply below

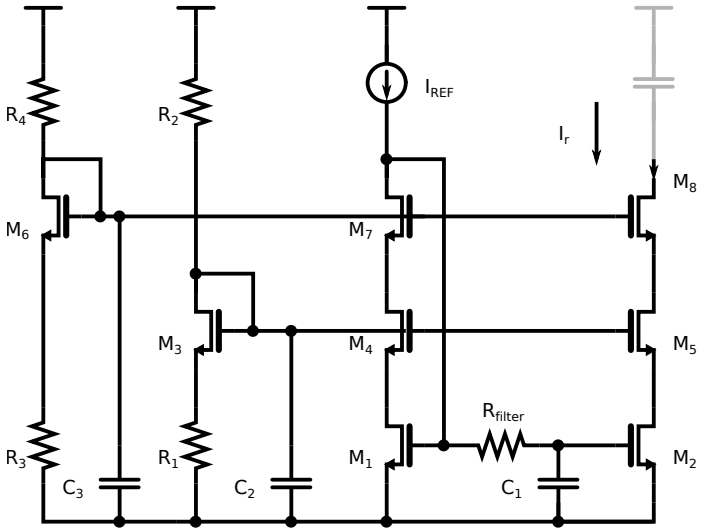


Figure 33: Double cascoded biasing current sink for ramp generation.

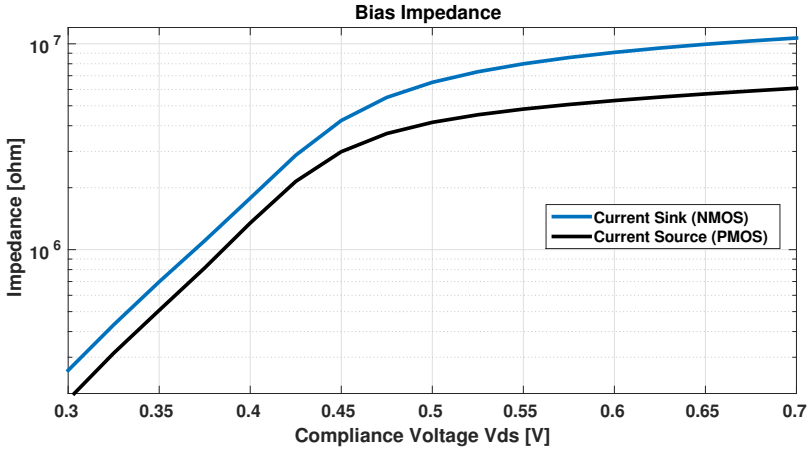


Figure 34: Output impedance of the current source and sink w.r.t the voltage headroom across the bias.

the compliance voltage limit, whereas the impedance has almost a flat response for higher voltage headroom.

The noise of the current source and sink is shown in Fig. 35.

5.2.2 Operational Amplifier

As mentioned in Section 4.1.2, the impedance of the ramp generation current could be boosted using an operational amplifier. Since it is quite challenging to design opamps at lower supply voltages, therefore such an opamp architecture is selected that provides a rail-to-rail input and output operation. The schematic of the designed operational amplifier is shown in Fig. 36.

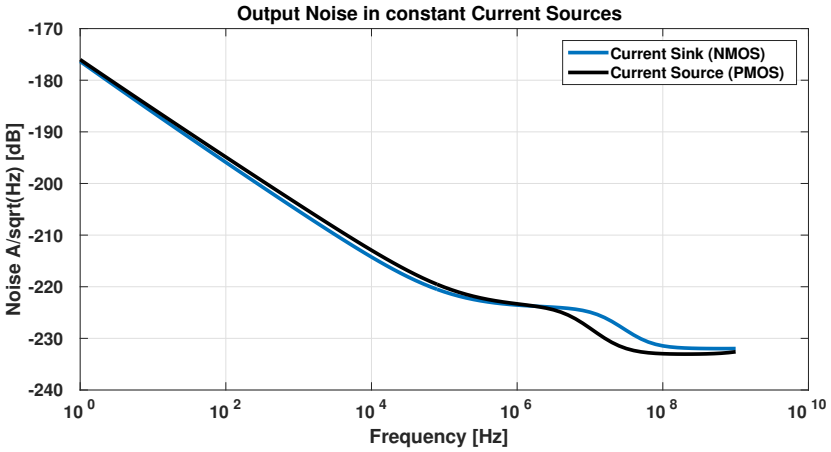


Figure 35: Noise of Current Source and Sink.

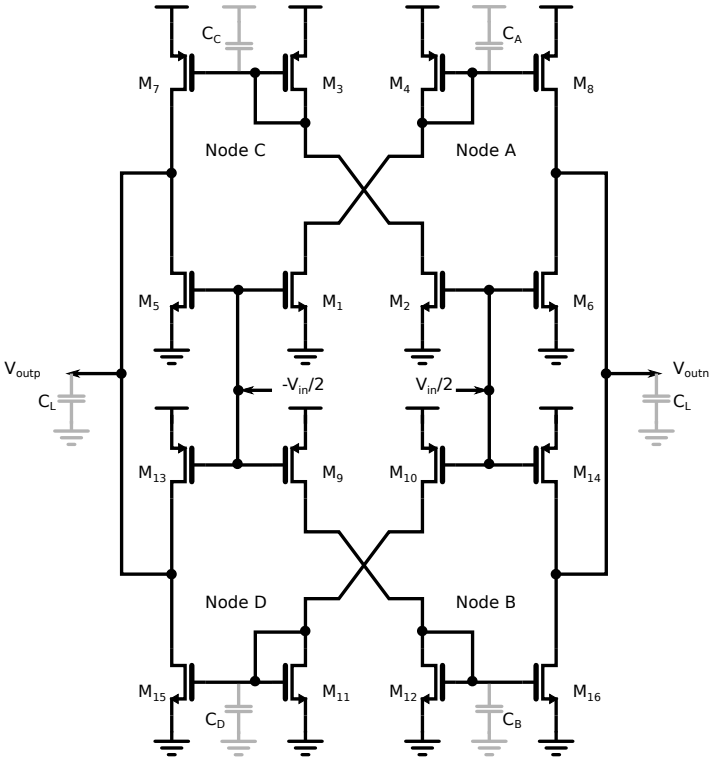


Figure 36: Rail-to-rail input and output operational amplifier.

The opamp does not contain any source coupled nodes at the input differential pair. Consequently, it can operate at large input voltage swings. Furthermore, the output consist of a PMOS and an NMOS common-source transistor stacking only. Therefore, this structure also provides a rail-to-rail output swing.

The opamp contains similar, albeit complementary amplifiers having PMOS and NMOS input transistors respectively, while their outputs are shorted to each

other. To analyze the frequency response, the small signal model of the half circuit is analyzed, as shown in Fig. 37.

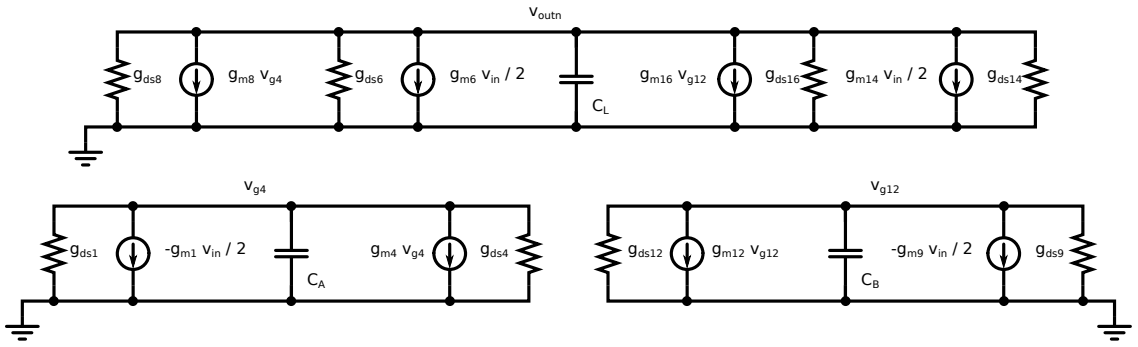


Figure 37: Small signal model of the half circuit of the opamp.

Applying nodal analysis on the small signal model in Fig. 37, at the nodes 'V_{outn}', 'Node A' and 'Node B' of Fig. 36 respectively, we get

$$g_{m8}\, v_{g4} \;+\; \frac{1}{2}\,(g_{m6} + g_{m14})\, v_{in} \;+\; g_{m16}\, v_{g12} + \;v_{outn}\,(s\,C_L + g_{ds6} + g_{ds8} + g_{ds14} + g_{ds16}) = 0\,, \tag{5.8}$$

where

$$v_{g4} = \frac{g_{m1}\, v_{in}}{2\,(s\,C_A + g_{ds1} + g_{ds4} + g_{m4})}\,, \tag{5.9}$$

$$v_{g12} = \frac{g_{m9}\, v_{in}}{2\,(s\,C_B + g_{ds9} + g_{ds12} + g_{m12})}\,. \tag{5.10}$$

Now, substituting (5.9) and (5.10) in (5.8), the transfer function of the half circuit (v_{outn}/v_{in}) is determined to be

$$\frac{v_{outn}}{v_{in}} = -\frac{\dfrac{g_{m1}\, g_{m8}}{(s\,C_A + g_{ds1} + g_{ds4} + g_{m4})} + \dfrac{g_{m9}\, g_{m16}}{(s\,C_B + g_{ds9} + g_{ds12} + g_{m12})} + g_{m6} + g_{m14}}{2\,(s\,C_L + g_{ds6} + g_{ds8} + g_{ds14} + g_{ds16})}\,. \tag{5.11}$$

Since the opamp is a symmetrically differential circuit, the overall transfer function will be twice in magnitude of (5.11), compared to its half circuit counterpart. In order to simplify the analysis, assume that all transistors have same transconductance ($g_{mx} = g_m$) as well as the output impedance ($g_{dsx} = g_{ds}$), while $g_m >> g_{ds}$. Then (5.11) can be simplified to determine the DC gain of the differential circuit as follows:

$$A_o \approx \frac{4\, g_m}{4\, g_{ds}} = \frac{g_m}{g_{ds}}\,. \tag{5.12}$$

The simulated frequency response of the designed opamp is shown in Fig. 38.

The performance of the opamp on typical (typical corner @ 27^o C), worst (slow corner @ 125^o C) and best (fast corner @ -40^o C) case in the 28 nm CMOS process is summarized in Table 2.

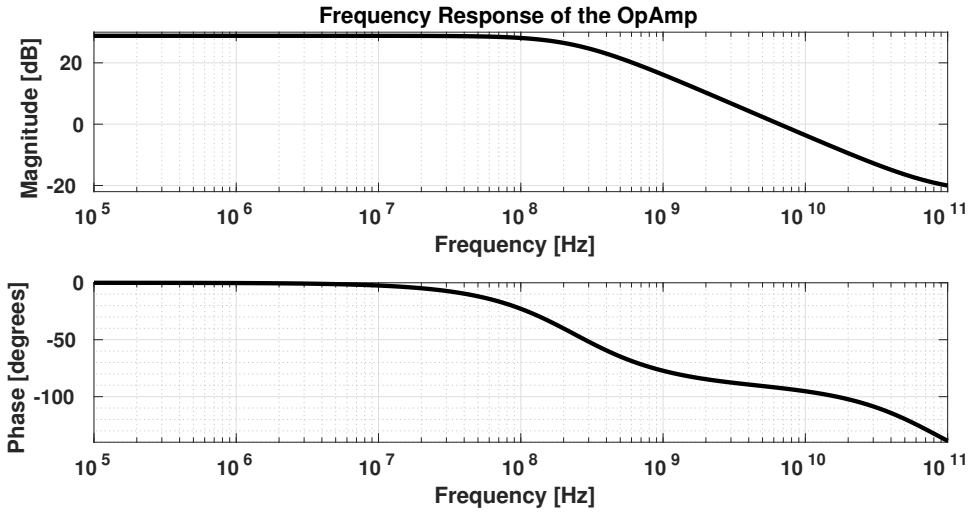


Figure 38: Frequency response of the opamp.

Table 2: Corner simulation results of the impedance boosting opamp.

	Worst Case	Typical Case	Best Case
DC Gain [dB]	27.6	28.8	29.2
Unity Gain Frequency [GHz]	7.6	6.6	6.6
Phase Margin [degres]	87.9	87.6	87.6
Bandwidth [MHz]	323.7	237.3	222.7
Power Consumption [mA]	1.14	0.72	0.62

5.3 Comparator

Comparator designs fall into two categories: continuous time and synchronous comparators. However, the proposed VTC functions by comparing two continuous ramp signals. Therefore, a continuous time comparator will be designed for this VTC.

There are numerous parameters that specify the performance of a comparator. These include the gain, input common mode rejection, propagation delay, power consumption, silicon area, input referred noise and hysteresis. However, based on the application, not all parameters are equally important.

Since the applied inputs will be ramps, the input difference will keep on increasing after crossing the threshold level and hence larger gain might not be that critical. Similarly, owing to the differential nature of the VTC and the input ramps, the ramps will always cross each other at the same common mode level. Hence, common mode rejection also becomes less critical performance parameter for the comparator. Furthermore, as an operational amplifier is being used to boost the output impedance of the current source, the input referred noise of the comparator becomes less critical when referred to the input of the opamp.

On the other hand, propagation delay is a critical parameter, since the output of the VTC is a time-signal, and any delay in the output will results in reduction of the available output range. Similarly, larger hysteresis also translates to higher input-to-output propagation delay. Additionally, lower power consumption and silicon area are and will always be of grave significance in any of the circuit designs.

Due to these reasons, the functional block diagram of of the selected comparator architecture is shown in Fig. 39.

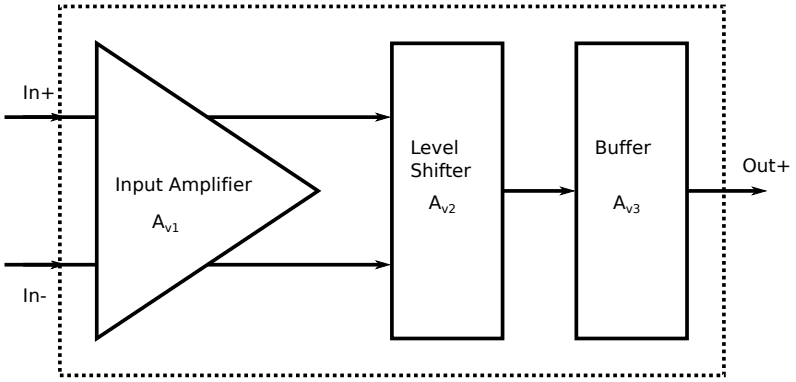


Figure 39: Comparator functional block diagram.

The comparator has three stages: input amplifier stage, level shifting stage and the buffer stage. The schematic of the designed comparator is shown in Fig. 40.

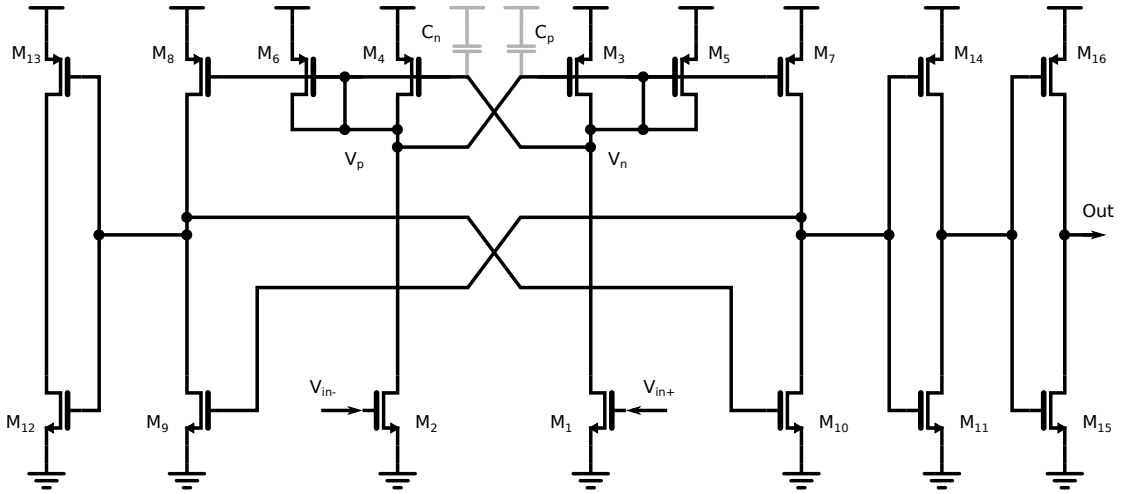


Figure 40: Comparator schematic.

The input amplifier stage is designed such that it has only a small amount of hysteresis, since larger hysteresis might lead to higher delay of the comparator. The amplified signal is then magnified to a rail-to-rail signal using the level shifting stage. The transition time of this signal is then further improved via buffers at the output of the level shifter.

In order to determine the transfer function of the comparator, consider the small signal equivalent of the half circuit as shown in Fig. 41. Since the circuit is differential, it is assumed that half of the input signal is applied at the positive ($V_{in+} = v_{in}/2$) input and the other half at the negative ($V_{in-} = -v_{in}/2$) input of the comparator in Fig. 40 respectively.

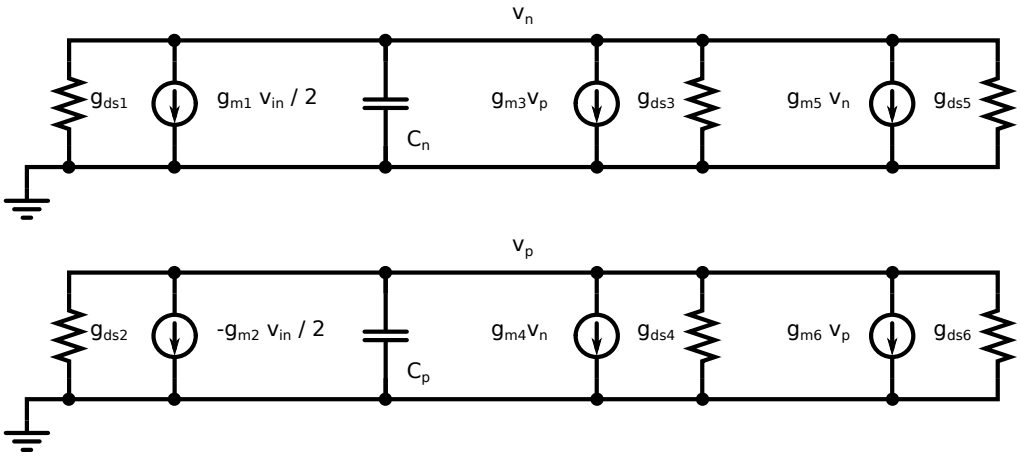


Figure 41: Comparator small signal model.

Using nodal analysis, the equations at node 'v_n' and 'v_p' of Fig. 41 are

$$v_n\,(s\,C_n + g_{ds1} + g_{ds3} + g_{ds5} + g_{m5}) \;+\; \frac{1}{2}\,g_{m1}\,v_{in} \;+\; g_{m3}\,v_p = 0\,, \tag{5.13}$$

$$v_p\,(s\,C_p + g_{ds2} + g_{ds4} + g_{ds6} + g_{m6}) \;-\; \frac{1}{2}\,g_{m2}\,v_{in} \;+\; g_{m4}\,v_n = 0\,. \tag{5.14}$$

Therefore, by simultaneously solving (5.13) and (5.14), the transfer function for half circuit (v_n/v_{in}) will be given by

$$\frac{v_n}{v_{in}} = -\frac{0.5\,(g_{m1} + g_{m2})\,(s\,C_p + g_{ds2} + g_{ds4} + g_{ds6} + g_{m6})}{(s\,C_p + g_{ds2} + g_{ds4} + g_{ds6} + g_{m6})\,(s\,C_n + g_{ds1} + g_{ds3} + g_{ds5} + g_{m5}) - g_{m3}\,g_{m4}}\,. \tag{5.15}$$

The frequency response of the first stage for the designed comparator is shown in Fig. 42.

The second stage of the comparator is a level shifter with only a positive feedback, as its objective is to convert the amplified signal into a rail-to-rail signal. The last stage of the comparator is simply a buffer to increase its output driving capability. The transient response of the comparator is shown in Fig. 43. When the differential input crosses 0 V, the output of the comparator is asserted after the propagation delay.

The performance of the comparator over corners is summarized in Table 3.

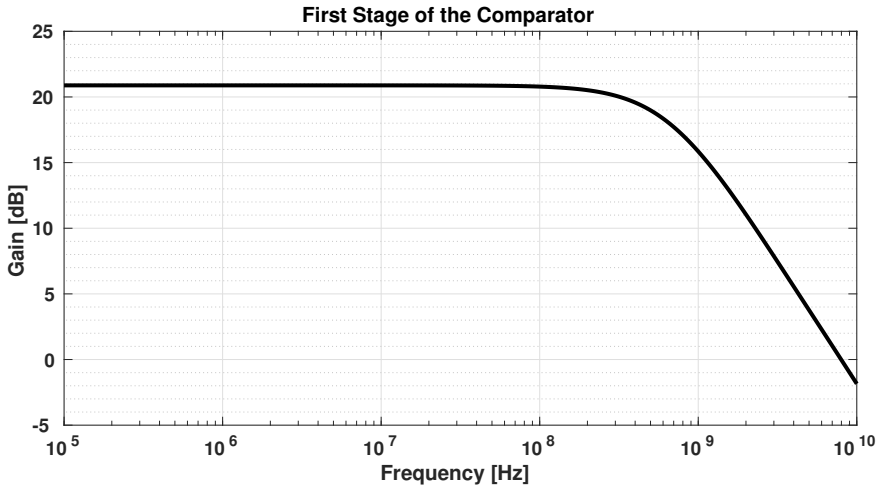


Figure 42: Frequency response of the first stage of the comparator.

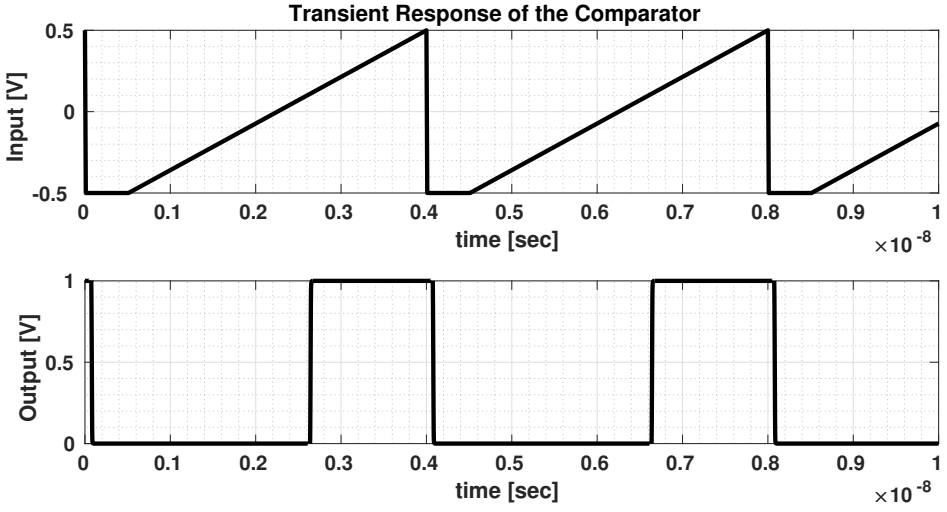


Figure 43: Transient response of the comparator.

5.4 Simulation Results

To determine the performance of the VTC, a 'verilog-A' code was written for an ideal TDC having a resolution of 15 bits. Furthermore, the VTC was operated at 256 MHz clock frequency, where the sampling time was kept at 500 ps, and rest of the clock cycle, i.e., 3.4 ns, was used for conversion, as discussed in Section 5.1.2. Since the design of the input buffer is beyond the scope of this thesis, it was modeled using an ideal signal source with a known output impedance.

Table 3: Corner simulation results of the comparator.

	Worst Case	Typical Case	Best Case
Stage 1 DC Gain [dB]	20.1	20.8	21.3
Stage 1 Bandwidth [MHz]	810.7	673.7	418.4
Propagation Delay [ps]	446.0	388.3	340.2
Power Consumption [uA]	201.2	201.8	228.5

5.4.1 Estimated Performance

The performance levels can be predicted using the derived mathematical models in Chapter 4. Therefore, the linearity and noise performance estimations are presented as follows:

- **Linearity:** The linearity could be predicted using (4.15), where the first term represents the fundamental tone, the second terms represents the second harmonic and the third term provides an estimate of the third harmonic. Since the input signal is less than one ($0.5\,V$) for the half circuit, contribution of the third harmonic in inducing non-linearity will be negligible. Hence, the ratio of the power of the fundamental tone to that of the second harmonic should predict the level of spurious-free-dynamic-range (SFDR) for this VTC. Hence,

$$SFDR \approx 20\, log_{10}\Big[\frac{2\, I_r\, R_r\, A_o}{V_{in}}\Big]\,, \tag{5.16}$$

  where ramp current I_r is given by (5.7), gain A_o at typical condition is determined using simulations as shown in Table 2, output impedance R_r is determined to be approximately 2 $M\Omega$ from Fig. 34 at the lowest compliant voltage level, and the input voltage is 0.5 V. Substituting these values in (5.16), we get

$$SFDR \approx 82\, dB\,. \tag{5.17}$$

- **Noise:** At the current defined by (5.7), the g_m of the transistor was determined to be equal to 514.2 μS through simulation in 28 nm process at 300° K. Furthermore, a single ended input signal of $0.5\,V$ resulted in an output time signal range of 2.7 ns. Additionally, from [38], the value of γ for a transistor in saturation is approximately 2/3. Therefore, using (4.17), the maximum number of bits achievable using a ramp capacitor from (5.1) will be

$$N = 8.84\, Bits\,. \tag{5.18}$$

Hence, it is apparent the the overall performance of the VTC will be limited by the thermal noise level of the ramp generation circuit.

5.4.2 Top Level Simulation Results

Since the VTC is designed for a Nyquist rate ADC, therefore, all the corner simulations were performed at $f_{in} = 126.5\,MHz$ for the typical, the worst and the best conditions and their results are presented in Figs. 44, 46 and 47 respectively. The corner simulations were performed to demonstrate the robustness of the design. The power supply was $1\,V$ over all the corners.

The output range in all of the corners was adjusted at about 2.7 ns. The adjustment was performed simply by changing the DC ramp current. This changed the slope of the ramp and consequently, the output range was adjusted to compensate for the corner variations. Compared to the typical corner simulation, the DC ramp current had to be increased to 125 % at the worst corner and reduced to 82 % at the best corner for compensating the capacitance variations over the respective corners.

Concerning the noise analysis, the VTC was simulated with transient noise from 1 Hz to 4 GHz. As is evident from Fig. 45, the ENOB is reduced to 9.04 bits when simulated with noise, compared to 12.4 bits of ENOB without noise as shown in Fig. 44.

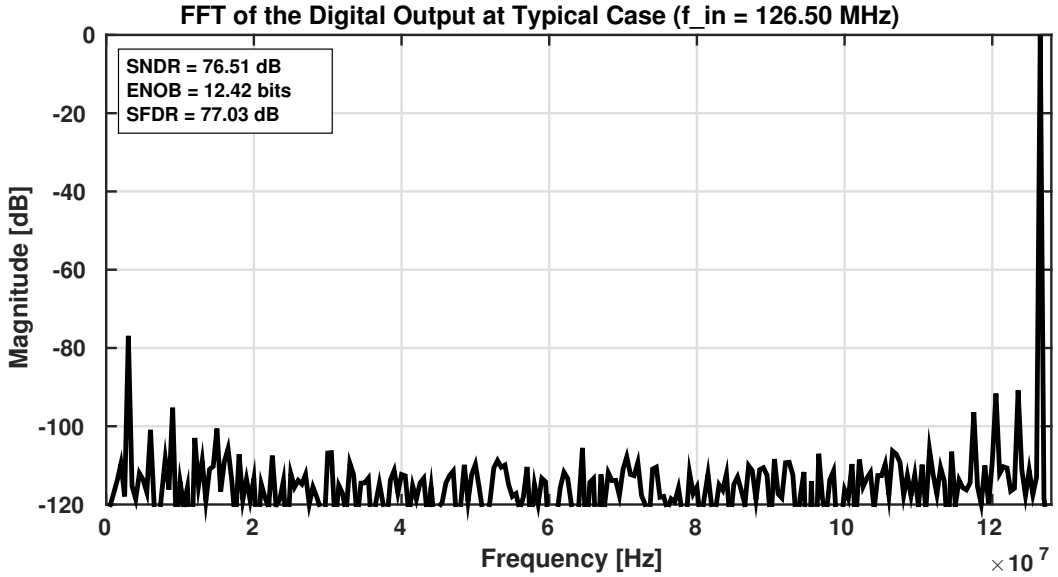


Figure 44: Typical corner VTC output performance.

5.4.3 Performance Summary

The performance of this VTC is summarized in Table 4.

Since the input signal is applied at 126.5 MHz and the VTC is clocked at 256 MHz, the second harmonic will appear at 253 MHz. However, this tone is beyond the Nyquist frequency, and will be aliased back to 3 MHz. From Fig. 44, a spur is clearly visible at 3 MHz, and thus, this spur is actually the second harmonic of the

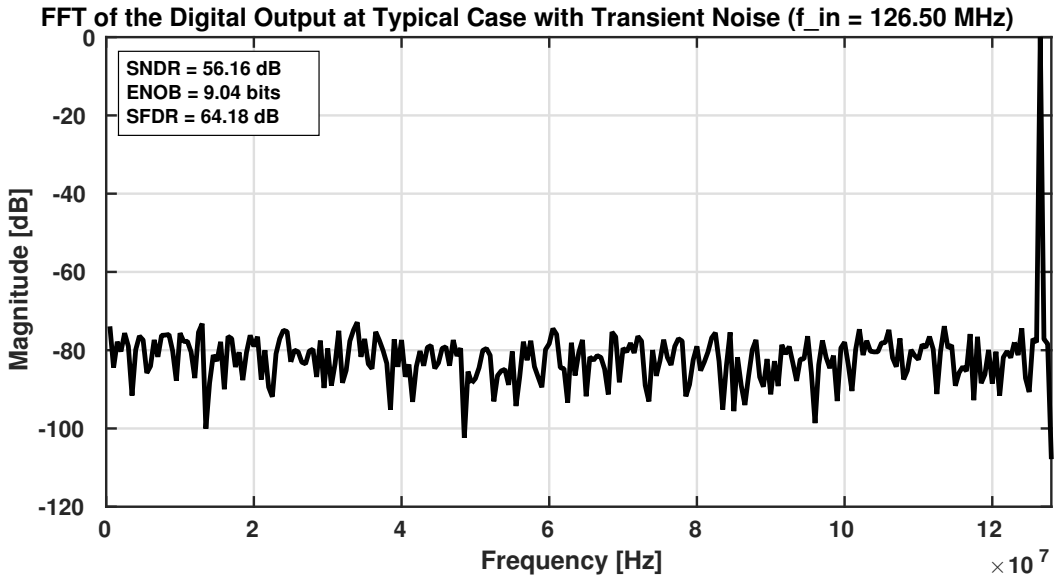


Figure 45: Typical corner VTC output performance with noise.

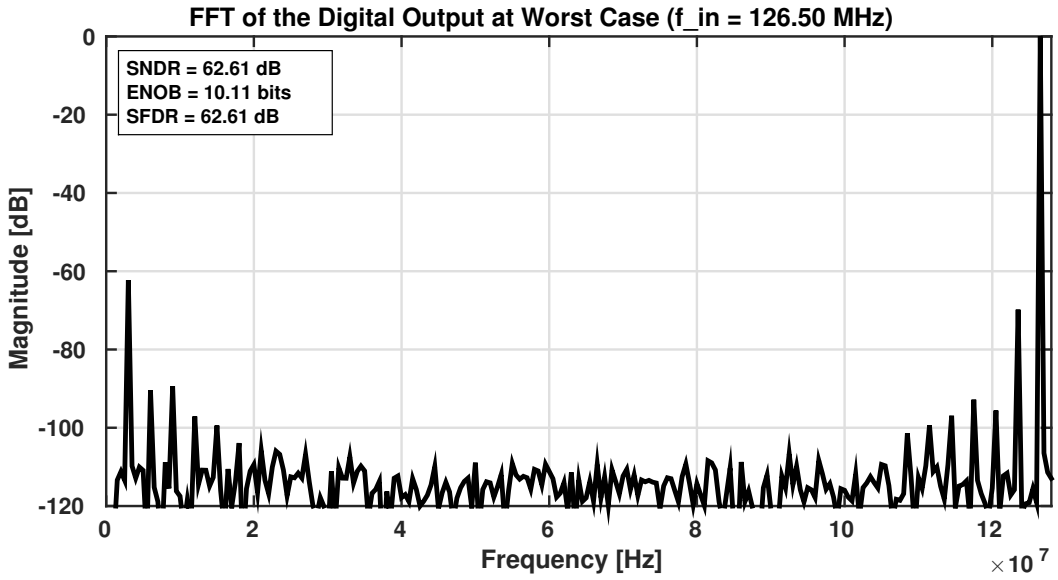


Figure 46: Slow corner VTC output performance.

VTC. As there is no other non-fundamental tones higher than the second harmonic, hence, it will define the SFDR for the ADC.

Analyzing (5.17), the calculated value of the SFDR is quite close to the simulated result, as presented in Table 4. The slight difference in the results could be attributed to the non-linearity effects injected from the sample-and-hold circuit, the opamp and the comparator.

The SFDR of simulations over the worst and the best corner is lower than the

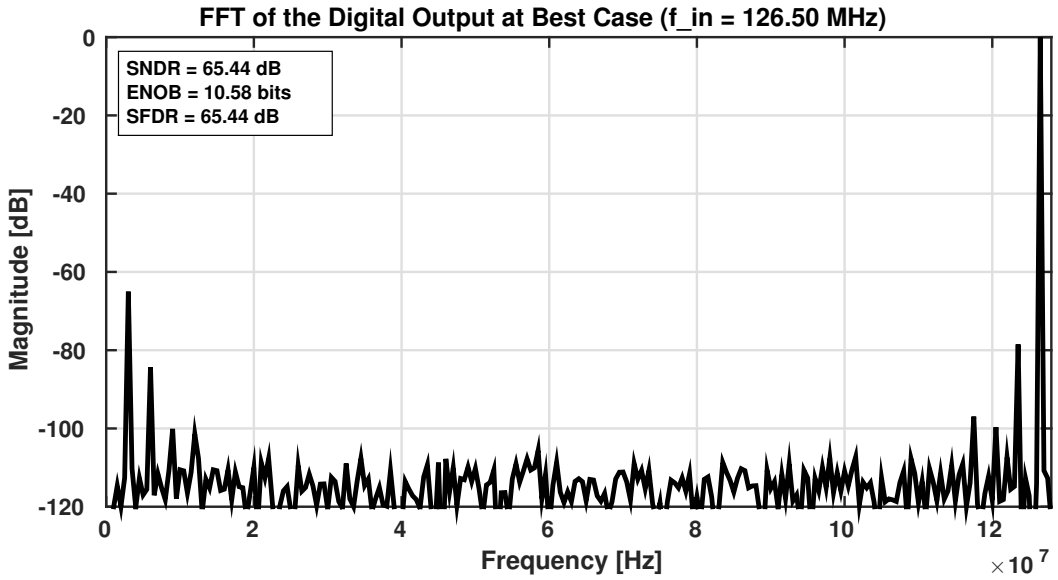


Figure 47: Fast corner VTC output performance.

Table 4: Performance summary of the VTC for f_{in} of 126.5 MHz at typical corner.

Process	28 nm CMOS
Supply	1 V
Input Signal (Differential)	1 V_{pk-pk}
Input Load	277 fF
F_s	256 MHz
Power	1.3 mA
Output Range	2.7 ns
SFDR (Without transient noise)	77 dB
SNDR	56 dB
ENOB	9.04 Bits

typical corner results, as is apparent in Figs. 46 and 47 respectively. However, main reason of simulating the corners was to establish the robustness of the design over process variations, and therefore, the circuit was not fine tuned for operation over these corners.

Furthermore, from (5.18), the calculated noise performance agrees reasonably well with the simulated performance as shown in Table 4.

6 Conclusion

This thesis has successfully designed a linear high-speed VTC. The proposed VTC was implemented using the ramp-and-comparator architecture. The final optimized design consist of a sample-and-hold circuit, a ramp generator and a comparator. The implemented VTC architecture achieves a high linearity performance, as confirmed by simulation results in Section 5.4 (an SFDR of 77 dB and an SNDR of about 56 dB), while operating at a speed as high as 256 MSPS in 28 nm CMOS process. This was achieved by first sampling the input signal over a capacitor, and then comparing it with a fixed ramp to generate the output 'time signal'. Since the overall performance of this VTC is highly dependent on the linearity of the generated ramp, an operational amplifier was employed to maintain the output voltage of the current source. Additionally, the architecture was modified to incorporate differential topology for minimizing the common mode noise and distortion effects. Consequently, these methods further improved the linearity and the performance of the VTC architecture.

In this thesis, since the sampling time for the VTC was fixed at 500 ps, the designed VTC can potentially be time-interleaved (up to 8 times) to obtain a throughput as high as 2 $GSPS$ without additionally loading the input buffers. At an input frequency close to the Nyquist rate ($f_{in} = 126.5\,MHz$), the VTC provides a linear performance of up to 9 bits ENOB with a differential input signal of 1 V peak-to-peak, while consuming a power of about 1.3 mW from a 1 V supply. Additionally, analyzing calculated results of (5.17) and (5.18) as well as the simulated results of Table 4, it is evident that the simulated performance agrees reasonably well with the calculated performance.

In order to compare the performance of this VTC, it should be combined with any TDC for completing time-based A/D conversion. For example, the pipelined TDC implemented in [42] provides 9 bit resolution at 250 $MSPS$ while consuming 15.4 mW of power in a 65 nm process. Integrating such a TDC along with the proposed VTC would constitute a time-based ADC that should be able to provide 9 bits of output at 250 $MSPS$ while consuming 16.7 mW. Therefore such a time-based ADC would have a Walden FOM of 131 $fJ/conv$. Furthermore, since the VTC contributes less than 10% of this power, the efficiency of such an ADC could potentially be further improved by optimizing the power consumption of the TDC alone.

Even though recent state-of-the-art ADCs have performance below 20 $fJ/conv$ [43], none of these highly efficient ADCs have employed a solely time-based architecture. Therefore, based on the attained performance of the proposed VTC, it can be concluded that the time-based ADC architecture has the potential to become one of the most efficient ADC structures for high-speed and resolution applications.

Hence, in order to enhance the efficiency and performance of the VTC, the power consumption could be reduced by optimizing the opamp and the comparator designs. Furthermore, calibration algorithm could be developed to track the process, voltage and temperature variations for robust operation of the proposed VTC. In addition, the thesis results could be better corroborated by fabricating this VTC on a chip, possibly along with a TDC, and measuring its performance.

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Appendices

A Voltage-Domain ADC Architectures

A brief review of the operation and the performance of voltage-domain ADCs is presented in this chapter. Detailed analysis can be found in [44].

A.1 Flash ADC

Flash ADC is the simplest architecture that helps to understand the operation of an ADC. As the name "flash" suggests, they are very fast converters, and they provide the digital converted output at every clock cycle. Architecture for a 3 bit flash ADC is shown in the Fig. 48.

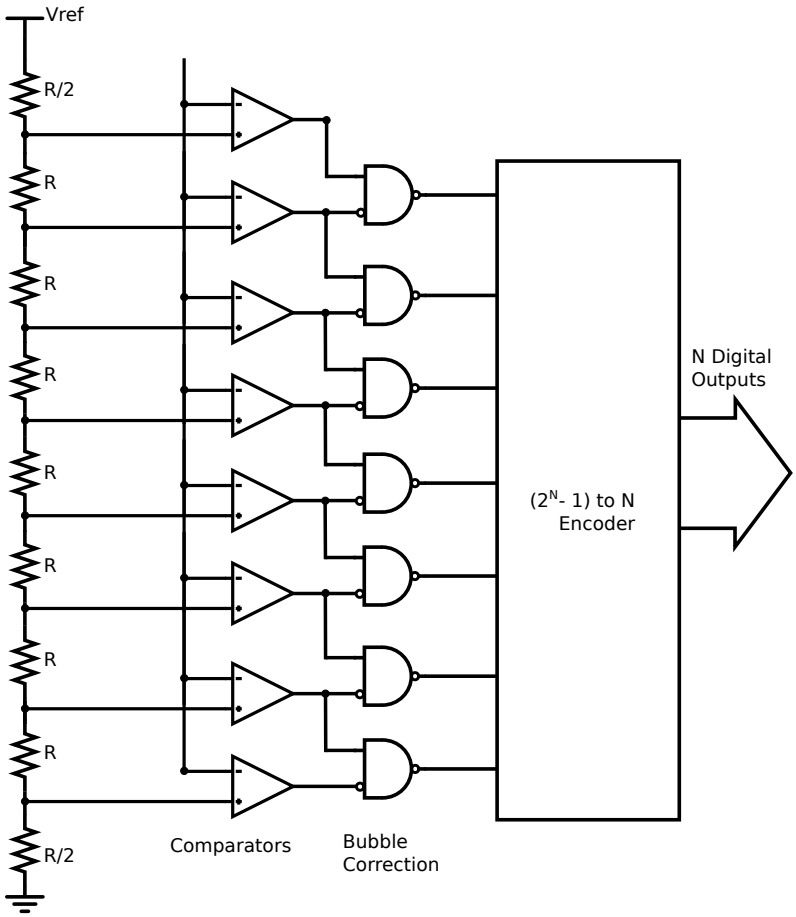

Figure 48: 3 bit Flash ADC.

Lets assume that a flash ADC has a resolution of N-bits, and a full-scale input signal of V_{FS}, then $2^N - 1$ reference voltages have to be generated (e.g. using resistor string voltage divider). These references are then compared with the input signal

using $2^N - 1$ comparators. Consequently, all the comparators with input signal level lower than the reference signal will have a logic low at the output, whereas all of the comparators with input signal level higher than the reference signal will have a logic high at the output. Such type of digital data is known as thermometer code (owing to the resemblance of such code with the mercury bar in a thermometer). This data is then converted into binary using an encoder.

The advantages and disadvantages of this architecture are summarized as follows:

- **Advantages:** For high-speed and low-resolution operations, this is probably the best (fastest) solution for analog-to-digital conversion. For example, [45] provides 6 bit output at 1.3 GSPS data throughput using a flash ADC architecture.

- **Disadvantages:** Since N-bit operation requires $2^N - 1$ converters and reference voltages, the size and complexity of the structure increases exponentially with increasing resolution. Moreover, there could be bubble error at the thermometer output of the comparators, which need extra digital logic for error correction. In addition, the comparators will introduce kick back noise at the input, which will limit the overall linearity of the converter. The comparators will also add parasitic capacitive loading at the input, and the input buffer for the ADC will need more driving capability, depending upon the number of comparators in the ADC. Larger resolution will require more comparators, leading to higher power consumption and additional silicon area. Therefore, as a rule of thumb, flash ADCs are limited to less than 7 bits of resolution due to these problems.

A.2 SAR ADC

Contemporary ADCs are mostly overshadowed by successive approximation register (SAR) ADC architecture. This is because, compared to flash ADCs, they provide reasonably better resolution at the expense of reduced speed without inducing much penalty on silicon area, complexity and overall power consumption. Basic architecture for an N-bit SAR ADC is shown in Fig. 49.

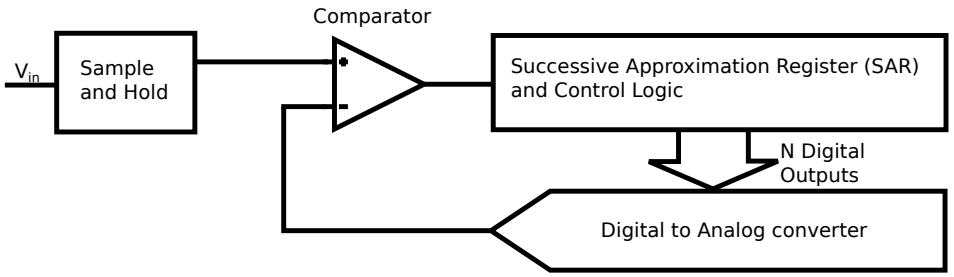

Figure 49: N-bit SAR ADC.

SAR ADC operates using a binary search algorithm to determine the digital output code for a corresponding analog input signal. This is achieved by using a

feedback loop consisting of a control logic, successive approximation register and a digital to analog converter. The behavior of this feedback loop is similar to that of a random guessing game, where the player knows the bounds of the input signal (by the definition of smallest and the largest signal i.e. full-scale signal) and the feedback from the system is only a "yes/no" type reply. The player starts by asking if the input signal is larger than half of the full-scale range (V_{mid}). If the answer is yes, the player reduces its own definition of full scale from (V_{mid}) to V_{FS} and asks again if the input signal is larger than the mid point of the new full-scale ($V_{mid_{new}}$), and based on that, the player keeps on adjusting the full-scale range until no more questions are left (the amount of questions directly corresponds to the resolution of the SAR ADC).

The advantages and disadvantages of this architecture are summarized as follows:

- **Advantages:** Increasing the resolution reduces the conversion speed of the ADC, but does not increase the area and power consumption. Thus, for nominal speed and resolution operations, this is probably the best solution for analog-to-digital conversion. For example, [46] provides 10 bits output at 50 MSPS data throughput using SAR ADC architecture.

- **Disadvantages:** Since it uses a DAC in its feedback, that DAC has to have a linearity equal to or larger than that of the SAR ADC's linearity. However, this becomes extremely tedious to achieve beyond 10 bits of resolution. Moreover, the throughput reduces with increasing resolution. Hence, it is not a good option for high speed and resolution applications.

A.3 Sigma Delta ADC

For high resolution and low speed applications, there is probably no substitute for a sigma delta (SD) based ADC. There are many variations of sigma delta ADC, and dedicated books specifically discussing and analyzing sigma-delta converters are frequently available [47, 48]. They are a special class of data converters, known as over-sampled converters. Basic architecture for a 1st order, N-bit SD ADC with M-bit quantizer is shown in the Fig. 50.

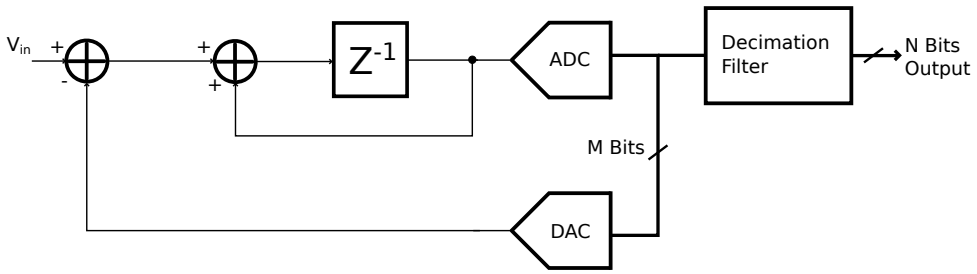

Figure 50: N-bit 1st order SD ADC with M-bit Quantizer.

SD ADC also consist of a feedback architecture, where data is converted into digital using a single or a multi-bit quantizer, and then reconverted into an analog

signal using a DAC. To achieve higher resolution, SD ADCs make use of noise shaping to increase the SNR. Mathematically, for a 1st order and single-bit quantizer SD ADC, the SNR is given by

$$SNR = 6.02N + 1.76 + 10\,log_{10}\,(OSR)\,, \tag{A.1}$$

where OSR is the oversampling ratio, given by

$$OSR = \frac{f_s}{2f_0}\,. \tag{A.2}$$

In the above equation, f_s is the sampling frequency, and $2f_0$ is the Nyquist rate for the converter. Moreover, due to oversampling, a decimation filter is employed after the quantized output to generate the required digital data. Even though it uses an ADC and a DAC within the loop, a single-bit quantizer and a DAC have no non-linearity issues, and hence, it eases the design constraints tremendously, compared to the SAR topology.

The advantages and disadvantages of this architecture are summarized as follows:

- **Advantages:** Extremely high resolution is possible using this architecture. Even though increasing the SNR reduces the signal bandwidth of the ADC, it does not increase much of the area and power consumption. Thus, for low-speed and high-resolution applications, this is probably the most optimal solution for an analog-to-digital conversion. For example, [49] provides 15 bits output at 24 KSPS data throughput using SD ADC architecture.

- **Disadvantages:** From the (A.1) and (A.2), it is clear that the oversampling ratio has to be increased to achieve larger SNR. Hence, for the order of MHz of signal bandwidth, the sampling frequency could be up to a few GHz for resolutions greater than 10 bits. Hence, it is very difficult to achieve higher bandwidths through this type of ADCs. Oversampling ratio requirements could be relaxed by increasing quantizer bits and order of the loop. However, this leads to numerous matching problems and increased complexity of the system.

A.4 Pipelined ADCs

Pipelining ADCs is one of the most common methods employed to increase the resolution in data converters. It is incorporated to achieve higher overall resolution by cascading numerous smaller resolution ADCs. A pipelined ADC is shown in the Fig. 51.

Lets assume that M-bit ADCs are pipelined to achieve a target of N-bit resolution (where N > M). To perform this conversion, the sampled input is first converted to digital using an M-bit ADC. Subsequently, the M-bits are reconverted into an analog signal using an M-bit DAC, which is then subtracted from the input signal to generate the residue signal. The residue signal is then given a gain of 2^M to convert it back to a full-scale signal, which is then fed to the next pipelined stage to determine the next M-bits.

The advantages and disadvantages of this architecture are summarized as follows:

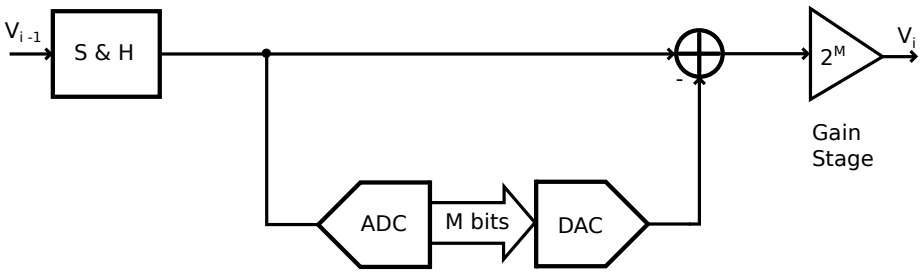

Figure 51: Single Stage of M Bit Pipelined ADC.

- **Advantages:** High speed and resolution conversion is possible using this method. Furthermore, pipelining could to incorporated in any architecture of an ADC. Pipelining might also help in reducing silicon area for the converter. For example, consider the case of a flash ADC. As mentioned in Section A.1, $2^N - 1$ comparators are required for N-bit resolution. Hence, 1023 comparators will be needed for 10 bits conversion. However, the same performance could be achieved by pipelining, say, 2 bit converters for 5 stages. Consequently, this method reduces the number of comparators from 1023 to 15 only. For example, [50] uses pipelining to achieve 12-bits of resolution at 600 MSPS throughput.

- **Disadvantages:** Providing linear gain becomes extremely critical in the residue amplifier. Hence, its design becomes challenging. Moreover, there is always going to be a latency between the input and the data output, which will be equal to the number of stages pipelined in the converter.

A.5 Time-Interleaved ADCs

Time-interleaving is also a common technique used in high-speed converters. It is incorporated to achieve higher overall throughput using numerous low-speed ADCs in parallel. It uses silicon area and power to compensate for low speed of either the technology or the architecture. Moreover, the architecture used for the core ADC could independently be selected (it could be flash, SAR or any other ADC architecture). A time-interleaved ADC is shown in the Fig. 52.

Lets consider the case of an ADC that outputs the data at f_s clock frequency. In order to reduce the operating frequency for the ADC architecture by, say, M times, M number of ADCs are connected in parallel with a sampling clock of f_s/M for each ADC. The output of these ADCs are connected to a digital multiplexer that provides a data throughput at f_s at the final output.

The advantages and disadvantages of this architecture are summarized as follows:

- **Advantages:** High speed and resolution converter designs are possible using this method. For example, [51] uses time interleaving to achieve 6 bits of resolution at 24 GSPS throughput, way beyond the typical operating speeds of single channel ADC architectures in CMOS technologies.

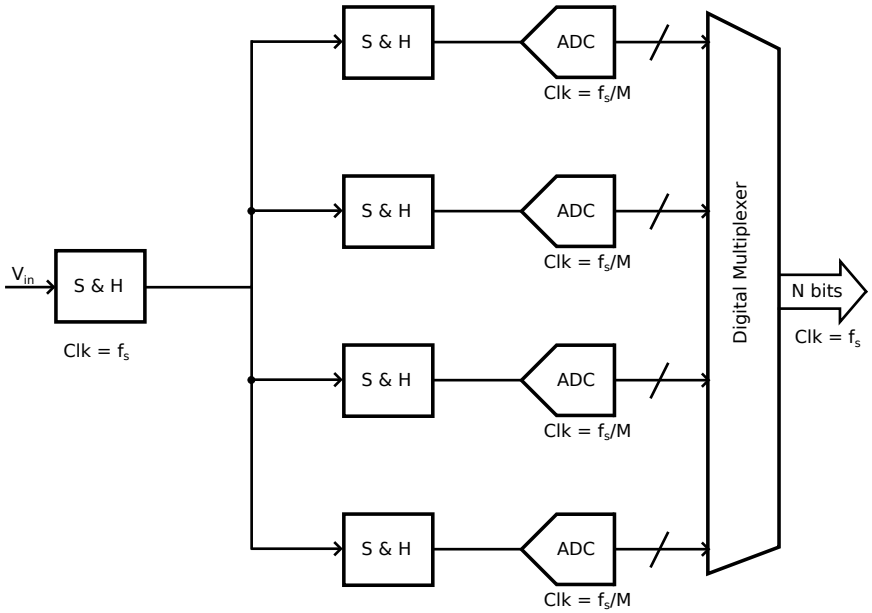

Figure 52: Time Interleaved ADC.

- **Disadvantages:** Performance of time interleaved architectures degrade severely by offset and mismatch errors. Moreover, overall silicon area increases, as multiple instance of the complete ADC operates in parallel to each other. Compared to the single channel counterparts, the overall power consumption also increases, primarily due to the additional hardware incorporated for the time-interleaving operation.

B Time-to-Digital Converter Architectures

Commonly employed TDC architectures, their operation principles, as well as their benefits and shortcomings are summarized in this section.

B.1 Delay-Chain-based TDC

Delay-chain-based TDC, also known as delay-line-based or Flash TDC, is probably the simplest method of time-to-digital conversion. A delay-chain TDC is shown in Fig. 53.

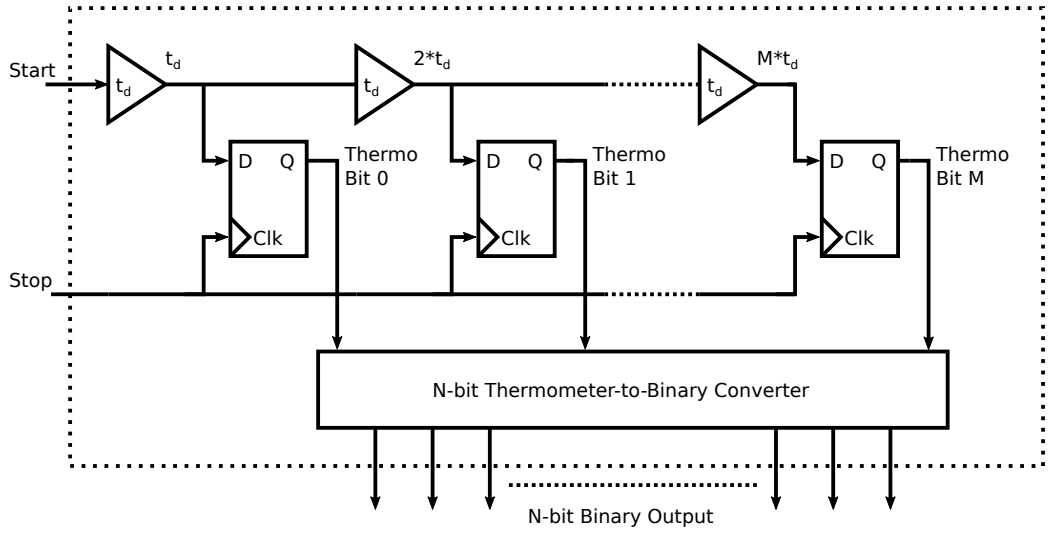

Figure 53: Delay-chain-based TDC.

Delay-line-based TDC consist of cascaded buffer stages, with the output of each stage recorded using a D flip-flop by connecting the data input of the flip-flops with the outputs of the buffer stages. The block operates with two inputs, a start signal and a stop signal. When the start signal is low, all the flip flops are reset to logic low, and the output of all the buffers will also be logic low. As soon as the start signal is asserted, it begins propagating through the delay chain. At the instant when the stop signal arrives, all the flip-flops record the data at the output of the buffer stages. However, this data is in the form of a thermometer code, and a thermometer-to-binary encoder is utilized to transform that data into an N-bit binary code.

The operating speed and resolution of such a TDC is dependent on the technology. Lets assume that τ is the smallest possible delay of a CMOS inverter in a technology, and the TDC has to provide N-bits output range within 0.5 f_{clk} of time interval. Therefore, the TDC will can maximally operate at

$$f_{max} = \frac{1}{2 \cdot 2\tau \left(2^N - 1\right)} \,. \tag{B.1}$$

The advantages and disadvantages of this structure are summarized as follows:

- **Advantages:** It is one of the simplest method for high-speed and low-resolution applications. For example, [3] uses delay lines to attain a performance of 2.9 bits ENOB at 2.5 $GSPS$ consuming 13 mW of power and utilizing very small silicon area. Furthermore, this type of TDC could also be implemented using an FPGA [52].

- **Disadvantages:** Analyzing (B.1) reveals that there is a trade off between the speed and the resolution for such architectures. For example, lets assume that a certain CMOS technology has an inverter delay of 10 ps. Then for a 10 bit operation, this TDC can provide a maximum throughput of 24.4 $MSPS$. Moreover, silicon area increases exponentially, since an N-bit operation require $2^N - 1$ buffer and flip-flop elements. Moreover, the INL of the chain increases by $INL \propto \sqrt{M}$ with the length of the chain, where M are the number of delay elements in the complete chain [7].

The delay of inverter also varies over PVT corners and an adjustment method, such as Delay-Locked-Loop (DLL), has to be added in the circuit to maintain the delay of the chain. Since, the LSB is dependent on the delay of gates within a particular technology node, this puts an upper limit on the achievable data rate for a certain target resolution in that technology node. Hence, due to a plethora of disadvantages, this method is not the most commonly employed architecture for high resolution time-to-digital conversion.

B.2 Delay-Ring-based TDC

Delay-ring-based TDC is quite similar to the delay-chain in its operation. The block diagram of a delay-ring-based TDC is shown in Fig. 54.

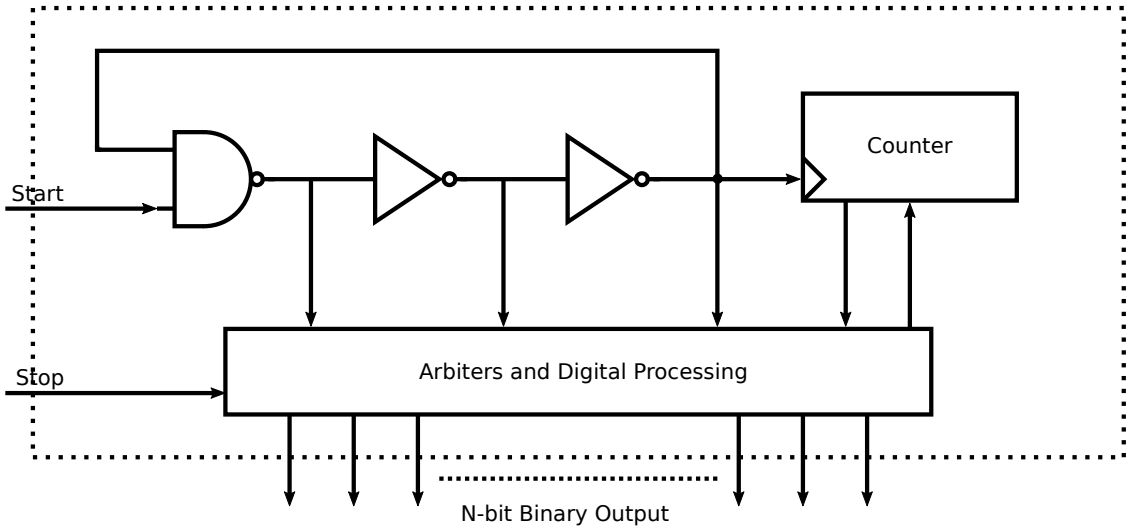

Figure 54: Delay Ring based TDC.

Delay-ring TDC could be analyzed as a delay-chain that loops over itself. Consequently, the length of delay-line becomes subjective to the frequency of operation, rather than the amount of physical hardware. However, instead of using buffer as delay elements, this architecture employs inverters to generate the delay stages. This is because a single-ended ring can only operate with an odd number of inverting stages (even inversions convert the ring into a latch). Therefore, every successive delay stage has to sense the opposite edge to acquire the correct data. Hence, both rising and falling edge triggered flip-flops have to be incorporate in the delay-ring.

The frequency of the ring is determined by the number of stages employed in the rings, as well as the delay of each stage. Therefore,

$$f_{ring} = \frac{1}{2\,L\,\tau}\,,$$

where τ is the delay of a single inverter and L are the number of inverting stages in the ring. Lesser number of delays in the ring correspond to a smaller silicon area. However, the ring frequency will increase, and auxiliary circuits (flip-flops etc.) might fail at such high speeds. Additionally, a counter is incorporated with the ring, which keeps account of the number of loops covered by the ring during the elapsed time. Moreover, every flip flop registering the output states of the ring has to be reset at the end of every lap. In addition to this, the LSB cannot be made smaller than the minimum delay of the gates in a particular technology. However, techniques such as multi-path gate delays could be employed to achieve sub-gate delays [53].

The advantages and disadvantages of this structure are summarized as follows:

- **Advantages:** The length of the ring is considerably smaller than the corresponding length of the delay-chain, and this improvement is highly prominent in TDCs with higher range. Consequently, it saves a lot of silicon area for higher resolution TDCs. Furthermore, the errors due to mismatch in delay elements diminishes and transforms into a mere cyclic linearity error. For example, [54] achieves 6 ps of resolution and 11 bits operation at 50 $MSPS$ using multi-path gated-ring-oscillator-based TDC.

- **Disadvantages:** A counter has to be added to the TDC along with its digital logic to process the data and convert it in the required binary form. Additionally, since the flip-flops have to be reset after every loop of the ring, very high frequency rings increase the difficulty in quickly resetting and registering data in the flip-flops. Moreover, since the stop signal is asynchronous, the counter should have gray coding topology to avoid any errors in registering the data due to multiple simultaneously changing bits. In addition to these issues, care has to be taken to match the parasitic load at the output of each inverting stage.

B.3 Vernier-Chain-based TDC

One of the key issues of delay-chain/ring-based TDC is that the achievable resolution cannot be smaller than the minimum delay of the gates within a particular technology

node. This issue, however, is resolved by using a vernier-chain-based TDC. This type of delay-line is called vernier-delay-chain/line because, similar to a vernier caliper which can measure smaller distances precisely, vernier-delay-lines can measure smaller time intervals accurately. The block diagram of a vernier-chain-based TDC is shown in Fig. 55.

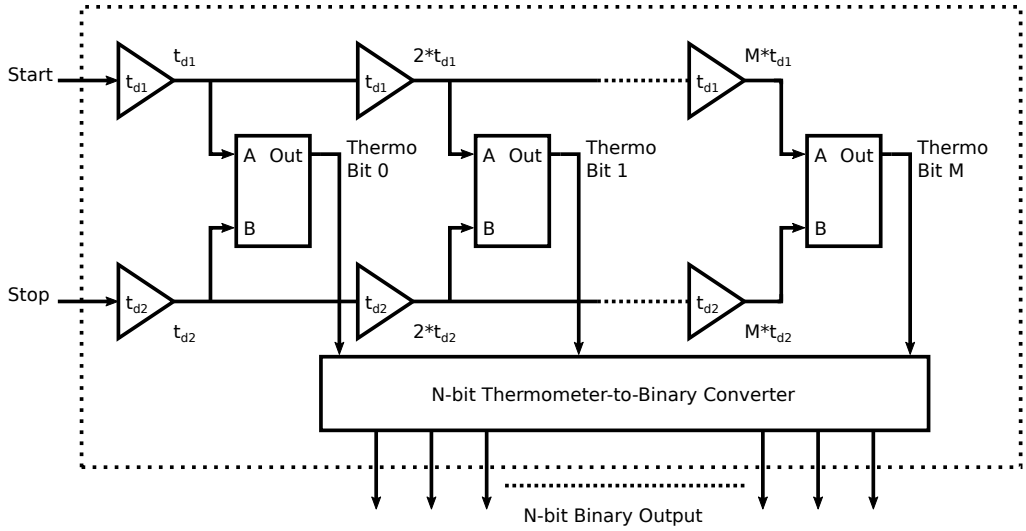

Figure 55: Vernier Chain based TDC.

Its structure consist of two delay lines, d_1 and d_2. However, d_1 has delay elements of τ_1 and d_2 has elements of τ_2. Moreover, instead of simple registering blocks, vernier delay line require arbiter blocks. An arbiter has two inputs, and its function is to decide precisely which one of the two inputs 'A' or 'B' arrived earlier and provide an output accordingly. If 'A' arrives earlier, the output will be logic high, else it will be logic low. When the start signal is asserted, it begins transitioning through d_1, and when the stop signal arrives, it begins propagating through d_2. However, the delay in d_2 is kept smaller than d_1, such that

$$\tau_1 - \tau_2 = \tau \,,$$

where τ is the LSB of the vernier-chain TDC. Hence, the signal will be propagating slightly faster in d_2 than d_1. At the point in the chain where signal in d_2 arrives earlier than d_1, the output of arbiters becomes logic low for all of the successive points in the chain, and a thermometer-code output is obtained. This is then processed and converted to binary data using combinational logic.

The advantages and disadvantages of this structure are summarized as follows:

- **Advantages:** Sub-gate delays can be achieved using this methodology. Hence, they are beneficial in applications where very high precision is required. For example, [55] achieves resolution of up to 5 *ps* using the vernier-delay-chain topology in 700 nm CMOS technology.

- **Disadvantages:** Even though the resolution becomes smaller, the overall range also scales proportionally. Hence, for the same number of elements, the output range of vernier-delay-chain is usually quite smaller than their delay-chain counterparts. Moreover, maintaining smaller delay difference over longer chains becomes extremely difficult. Hence, such architectures are usually limited to the applications which require lesser number of output bits with high precision.

B.4 Vernier-Ring-based TDC

Similar to the delay-ring-based TDCs, vernier-chains could also be reduced in length by folding on itself and converting into rings. The structure and operation of this TDC is similar to the vernier-chain TDC. However, instead of two long chains with different delay elements, this structure contains two rings operating at correspondingly different frequencies. The block diagram of the vernier-ring-based TDC is shown in Fig. 56.

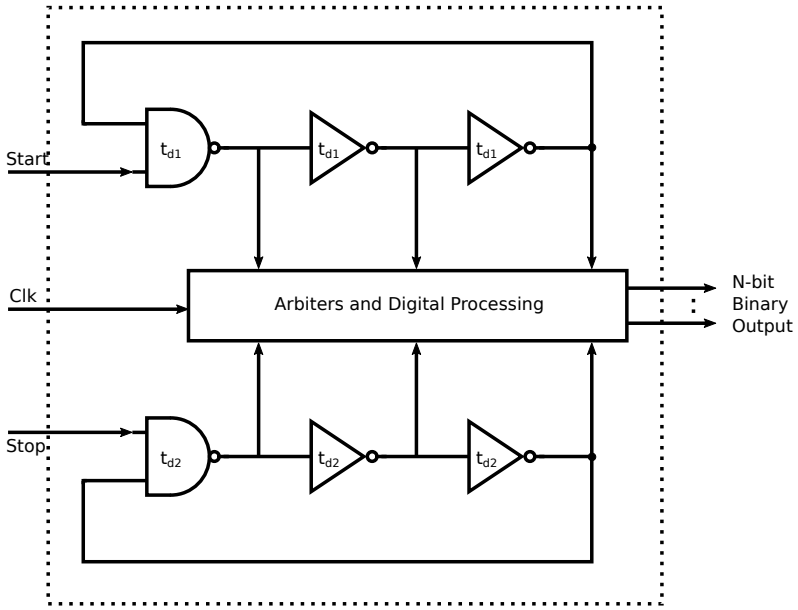

Figure 56: Vernier-ring-based TDC.

The advantages and disadvantages of this structure are summarized as follows:

- **Advantages:** The size of the rings is considerably smaller than the chain counterpart. Hence, this structure provides precision with tolerable INL and silicon area. Consequently, this method is one of the most commonly explored area of research for TDC designs. For example, [56] attains 12 bits of linearity with a resolution of 8 ps in 130 nm technology consuming 7.5 mW of power at 15 MHz of clock frequency.

- **Disadvantages:** This structure will have two rings oscillating at slightly different frequencies (due to small difference in delay elements). Hence, it will have

similar issues as the ones with delay-ring-based TDCs. Due to the presence of two rings oscillating at different frequencies, however, parasitic effects might induce injection-locking. Injection-locking is a phenomenon where two rings with slightly different frequencies lock and then oscillate at the same frequency. This will result in severe performance degradation for the TDC.

B.5 Hybrid TDC

Even though vernier-ring-based TDCs provide good resolution, attaining large output range along with good resolution is usually not possible. This problem is mitigated using a hybrid TDC. The block diagram of a hybrid TDC is shown in Fig. 57.

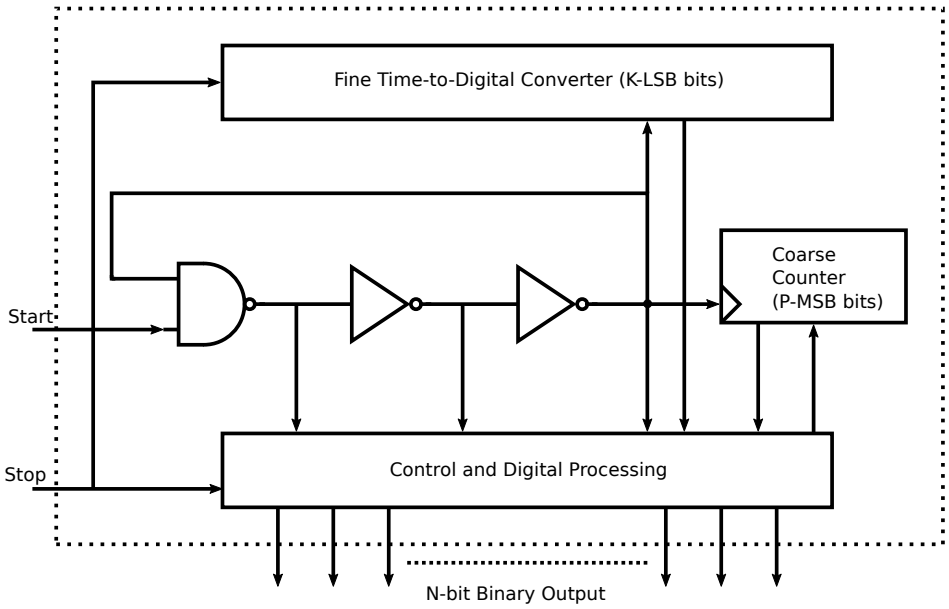

Figure 57: Hybrid TDC.

The structure of this TDC consist of a coarse and a fine TDC. When the start signal is asserted, the coarse TDC starts to count the time elapsed using a slow clock, providing the MSBs for the conversion. This adds the necessary larger range to the performance of the TDC. As soon as the stop signal arrives, the fine TDC starts measuring the time elapsed with a finer resolution, thus providing the LSBs for the conversion. The final data is then processed and combined to obtain a binary time-to-digital converted output.

The advantages and disadvantages of this structure are summarized as follows:

- **Advantages:** High speed and high resolution TDC performance is possible using this structure. For example, [7] uses hybrid TDC to attain 8 bits of resolution at 1 $MSPS$ utilizing only 7 μW of power. Moreover, the overall power consumption is reduced, since the power hungry fine TDC operates for only a portion of the total conversion time.

- **Disadvantages:** Combining the coarse and fine sections of the TDC increases the complexity of the system, since they have to be matched precisely with each other for the proper operation. Hence, numerous calibration options have to be added and exercised to attain better performance from this TDC.

B.6 Pipelined TDC

The concept of the pipelined TDC is quite similar to that of the pipelined ADC discussed in Apprendix A.4. It follows that, instead of converting an analog input to a digital output of complete resolution in a single clock cycle, this method emphasizes on converting smaller chucks of the data in a serial fashion until the required resolution is achieved. However, instead of 'voltage signals', this type of ADC deals with 'time signals'. The block diagram of a pipelined TDC is shown in Fig. 58.

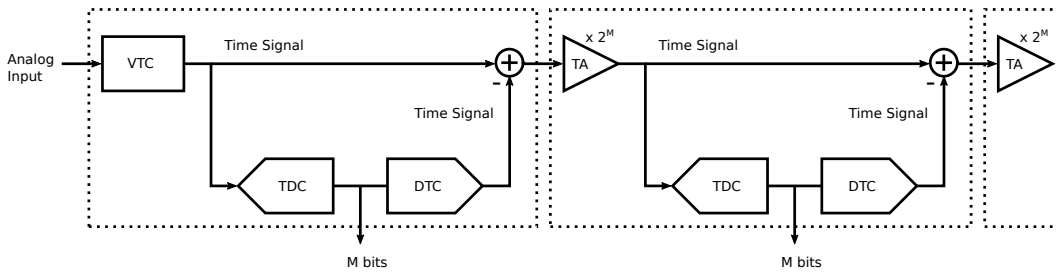

Figure 58: Pipelined TDC.

Various methods have been employed for the residue amplification [42, 57, 58] in pipelined time-to-digital conversion. However, the goal is to achieve a high speed and resolution operation using these methods in the TDC.

The advantages and disadvantages of this structure are summarized as follows:

- **Advantages:** Since only a small number of bits are resolved during a single clock cycle, timing constraints are relatively relaxed in such type of TDCs. Furthermore, high speed and resolution converters are possible. For example, [42] provides 9 bits output at 250 $MSPS$ consuming 15.4 mW of power by cascading three 2.5-bit stages while achieving 1.12 ps of resolution. Such high frequency operation is extremely difficult using any other topology of TDC.

- **Disadvantages:** Complex calibration algorithms are required to minimize the gain and the offset mismatches, which would otherwise severely degrade the performance of the converter.