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Effect of $CdCl_2$ Treatment on CdTe and CdS Solar Cell Characteristics after Exposure to Light for 1000 Hours

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by

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of the requirements for the degree of
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ABSTRACT

The CdTe solar cell is a leading candidate for cost-effective thin-film solar cells having demonstrated small area cell efficiencies of 16.4%. A Key issue associated with CdTe thin film photovoltaic modules is the analysis of degradation behavior of the device. The analysis is complicated as changes due to degradation may be reversible. Solar cell measurement techniques were used to understand the changes in device parameters after light soaking for 1000 hours. An automated measurement setup was implemented as part of this thesis work. The main objective of this thesis was to study the effect of $CdCl_2$ heat treatment on the device stability. The temperature for this heat treatment was varied from 360^oC to 400^oC. Cells were stressed under illumination at both short circuit and open circuit conditions. It was found that the increase $CdCl_2$ heat treatment temperature slowed down the degradation rate.This was true for both short and open circuit stress conditions. Also short circuit stress condition slowed down the degradation of the device when compared with the open circuit condition. It became evident that the recombination current mainly got affected when the device was said to be degraded.

Chapter 1
Introduction

The only reason for time is so that everything doesn't happen at once ...

Albert Einstein

The stability of solar cells acquires importance since it is generally assumed that terrestrial photovoltaic systems must have a useful life of at least 20 years. Thin film fabrication processes are being developed as low cost technique for producing terrestrial solar cells. Semiconductors with band gaps of around 1.5eV are optimum in terms of efficiency. Hence CdTe is the material of choice. Published data [1][2] show that CdTe/CdS solar cells may exhibit instability under certain conditions.

In general, degradation of solar cells occurs when they are light soaked for prolonged time and/or at elevated temperatures. The reasons for the observed degradation may be junction degradation, degradation of the electrical contact to CdTe and shunting. The degradation is frequently represented by perturbation of current voltage characteristics, the development of rollover at high forward bias, a decrease in open circuit voltage (Voc), an increase in the series resistance and a decrease in the fill factor (FF).

The most suspected cause for cell instability is the diffusion of Cu from the back contact into the CdTe region and the CdTe/CdS interface. A small amount of Cu

is often added to back contacts to effectively p^+ dope the CdTe surface and allow the formation of better ohmic contacts to CdTe[3][4]. At the cell junction Cu was proposed to form recombination centers and shunting pathways, limiting the lifetime of the cell.

Other probable degradation mechanisms in CdTe/CdS solar cells are oxidation, electromigration and diffusion of native and other impurities.

1.1 Objectives

The objectives of this work were:

- to Construct and automate a measurement setup needed for stability testing of CdTe/CdS solar cells under various stress conditions and
- to study the effect of prolonged illumination and $CdCl_2$ heat treatment on the performance of CdTe/CdS solar cells.

Chapter 2
Solar Cells Under Illumination

It is necessary to first understand the device behavior under illumination to know the effect of prolonged illumination on device stability.

A solar cell is generally a p-n diode. In our case, CdS was used as the n-type semiconductor and CdTe as the p-type semiconductor. The junction formed between CdS and CdTe is called heterojunction. If the light passes through the substrate first, then device is said to have a superstrate structure. CdTe solar cells for this experiment had the superstrate structure as shown in fig. 5.1. When the radiation is received from the sun, it gets absorbed in the semiconductors which generates charge carriers in them. The most of these carriers are separated by the junction due to its internal electrical field and then collected at the contacts of the device, thus delivering power to an external load connected to the solar cell.

The following regions of a solar cell are of interest to explain the electronic process involved:

- The back contact to CdTe: can form barrier with CdTe, possibly increasing series resistance and roll over
- The bulk of CdTe: where electron/hole pairs are generated by the absorption of light outside the depletion region

- The heterojunction: where the change in interface states and high recombination takes place, increasing the dark current
- The bulk of CdS, which contributes to series resistance, but does not contribute to Jsc.

The idealized junction current in the dark is given by

$$I = I_0[\exp[qV/AkT] - 1] \tag{2.1}$$

where I_0 is the reverse saturation current, k is the boltzman constant,q is electric charge,T is temperature in $^o kelvin$ and A is the diode factor.

Some heterojunction solar cell structures show a variation in Io and A with illumination level and wavelength. This is because, when trapping centers at or near junction are not in good thermal communication with conduction or valence bands (slow states), their occupancy and hence charge can be changed by illumination. Also the ionized donor or acceptor density in the n or p type semiconductor may change upon illumination, which in turn modifies the depletion layer width, the shape of the junction barrier, and finally the junction transport[7].

Under illumination, the equation 2.1 becomes

$$I = I_0[\exp[qV/AkT] - 1] - I_L \tag{2.2}$$

Where I_L is the light generated current determined by the processes in CdTe during illumination.

Equation 2.2 is valid only if the shunt (R_{sh}) and series (R_s) resistances of the solar cell approach ∞ and 0 respectively. In practical devices, this is not true. Equation 2.3 includes the effect of these resistances.

$$I = I_0[\exp[q(V - IR_s)/AkT] - 1] + [(V - IR_s)/R_{sh}] - I_L \tag{2.3}$$

Here the shunt resistance R_{sh} may account for the effects of the current paths provided by imperfections like pinholes, surface recombination, three dimensional imperfections in the junction etc. R_s is due to bulk resistances of layers present in the device,front and back contact resistances etc.

If the the device is kept open(i.e. no load),the potential difference across the front and back contacts is measured as the open-circuit voltage, V_{oc}. When the contacts are shorted with zero resistance load, the resultant photo generated current is known as short circuit current I_{sc}. J_{sc} is the corresponding current density. At a certain load, the output power is maximized(P_{max}). The ratio between P_{max} to the product of V_{oc} and J_{sc} is called the fill factor(FF) which is the measure of the "squareness" of the current-voltage characteristics under illumination.

R_{sh} affects the current-voltage characteristics in the low voltage region and R_s at high current region of current-voltage curve.

2.1 Interface States

Optical absorption by states at the interface and in the bulk material near the junction produces changes in the junction profile, and hence changes in Io and A upon illumination.

The interface states density N_{ss} affects the carrier transport. These surface states act as a recombination centers, which can provide a tunnelling path for the carriers[6].

The increase in interface states density due to illumination will lead to a decrease in the barrier height Φ_b and consequently enhance the saturation current. The consequences of the decrease in potential barrier height are an increase in both dark current and series resistance, and a decrease in open circuit voltage, photocurrent and conversion efficiency of the solar cell[6].

Chapter 3
Literature Review

It is important to understand the failure mechanisms that lead to cell degradation. Table 3.1 lists major failure modes in CdTe/CdS solar cells along with the possible causes.

Table 3.1 CdTe Failure Modes and Possible Causes[8]

Failure Modes	Possible Causes
Main junction, increased recombination	Diffusion of dopants, impurities etc., electromigration
Back barrier, loss of ohmic contact	Diffusion of dopants, impurities etc., electromigration
Shunting	Diffusion of metals, impurities etc.

These mechanisms can cause the following change in the current-voltage (I-V) characteristics:

- an increase in Roc and "Rollover" in I-V curves at voltages larger than Voc, possibly from the back contact barrier formation,
- a reduction in Voc and

- an increase in the slope of I-V curve, through Jsc, possibly from increased shunting or from increased recombination in the space charge region[9].

Roc is the slope of light I-V curve at Voc. It is found that the formation of back contact barrier leads to high values of Roc and "Rollover". A high series resistance can also lead to an increase in Roc.

A Non ohmic back junction can be due to[10]

- loss in acceptor density in the p^+ layer and
- Oxide interface layer.

A loss in acceptor density is mainly caused by diffusion of impurities. Here, Cu with diffusion coefficient of 5E-14 cm^2/sec at 100^oC and activation energy of 0.66 eV is a prime suspect. The degradation also depends on bias, as the charge state of vacancies can affect the rate of diffusion of an atom. Also, grain boundaries have some effect on diffusion, electromigration of charged atoms, and local compensation effects in degradation[10].

3.1 Effect of Copper Diffusion on device Stability

Even though Cu forms better ohmic contact at the back contact interface, it can degrade the cell, by diffusing through the CdTe layer to the junction and CdS, as Cu is the fast diffuser in single crystal CdTe(Diffusion Coefficient $D \sim 3E-12cm^2$). Cu as an interstitial ion $[Cu_i^+]$ gives shallow donor state or substitutes Cd atom to form

a deep acceptor state in single crystal CdTe. In polycrystalline films, the diffusion of Copper is even more as the surface bonds are weaker and two surfaces are available at grain boundaries.Electric field may also enhance Cu diffusion. "Roll over" after light soaking indicates the decrease in Cu density near the back contact and possible increase of Cu density near the junction[10]. When cells with and without Cu in in the carbon back contact was light soaked, only cells with Cu showed some recovery after rested in dark for 6-12 months. This suggests that Cu can return to the CdTe/back contact interface under some circumstances[10].Also when the Cu content in the back contact was increased, Voc and FF degraded faster[10].

One possible mechanism which drives the Cu into junction and CdS may be grain boundary diffusion and surface reaction to form Cu-S bonds. This process would be aided by S/Te interdiffusion and also due to the fact that Cu-S bond is stronger than Cu-Te bond as derived from the heats of formation[10].It is to be noted here that the interdiffused CdS_xTe_{1-x} region adjacent to the CdS acquires a low concentration of Cu compared to the less Te-rich CdS[10].

While the built in voltage slows the concentration gradient driven Cu diffusion, forward bias and/or light lowers that barrier for diffusion[11].

3.2 Effect of $CdCl_2$ Treatment on Device Stability

After $CdCl_2$ treatment, Cl moves via grain boundary (GB) diffusion through the CdTe layer. The accumulation of Cl near the CdS interface is due to the greater GB

area in the smaller-grain CdS layer compared to the CdTe. This is also due to the fact that Cl of atomic radius 167 pm is expected to substitute for S(170 pm) in CdS over Te(207 pm) in CdTe[2].This accumulation improves the initial performance. The net acceptor concentration near the interface increases by increasing the temperature of $CdCl_2$ heat treatment[2].

Also structural changes in CdTe thin films occur only when $CdCl_2$ is present due to recrystallization and subsequent grain growth. Recrystallization is the function of lattice-strain energy, and initial strain energy increases due to Cl diffusion[12].

It has been shown that during vapor $CdCl_2$ treatment diffusion of CdS into the absorber layer proceeds faster than the diffusion of CdTe into window layer and is enhanced by reaction temperature[14].

Chapter 4

Solar Cell Characteristics and Characterization Techniques

4.1 Current-Voltage Characteristics

4.1.1 Current-Voltage Characteristics in Dark

Under thermal equlibrium, when the diode is zero biased or reverse biased, no current flows due to the potential barrier. When it is forward biased, barrier potential is reduced, holes(or electrons) from the p(or n) region are injected to create excess minority carrier in (n or p) region.

In low injection, the majority carrier concentration doesnt change significantly. But minority carriers change several orders of magnitude.The total current in the junction is the sum of the individual electron and hole currents. Since the electron and hole currents are continuous functions through the junction, the total pn current will be sum of minority carrier diffusion currents. Since it is assumed that the electric field at space charge edges is zero, there is no minority drift current.

So for ideal p-n junction diode,current density equation in dark is,

$$J = J_s[\exp \frac{qV}{kT} - 1] \tag{4.1}$$

where

$$J_s = qn_i^2[\frac{1}{N_a}\sqrt{\frac{D_n}{\tau_{n0}}} + \frac{1}{N_d}\sqrt{\frac{D_p}{\tau_{p0}}}] \tag{4.2}$$

Here J_s is called ideal reverse saturation current density.

But this ideal diode equation neglects any effects occurring within the space charge region. Since other current components are generated within space charge region, the actual I-V characteristics deviate from the ideal one.These additional currents are generated from the recombination processes. Under reverse bias,since number of electrons or holes are said to be zero in the space charge region as they are swept away,electrons and holes are generated to reestablish thermal equilibrium.This reverse bias generation current should be added to get the total reverse saturation current.It is given by,

$$J_0 = J_s + J_{r0} \tag{4.3}$$

Where J_0 and J_s are total and ideal reverse saturation current densities. J_{r0} is the reverse generation current in the space charge region and is given by,

$$J_{r0} = \frac{qn_iW}{2\tau_O} \tag{4.4}$$

Where W is the depletion width and τ_O the average carrier life time.

Under forward bias, some excess carriers are injected into the space charge region. Recombination current density is then,

$$J_{rec} = J_{r0} \exp[\frac{qV}{2kT}] \tag{4.5}$$

Hence in general, the diode equation becomes

$$J = J_0[\exp \frac{qV}{AkT} - 1] \tag{4.6}$$

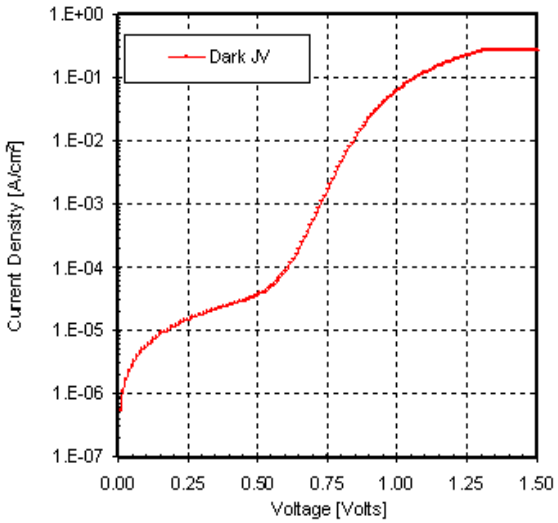

Figure 4.1 Typical dark JV characteristics

where A is the diode factor. For a large forward bias voltage, A≈1 when diffusion dominates and for a low forward bias voltage,A≈2 when recombination dominates. There is a transition region where $1 < A < 2$.

The typical dark JV characteristics is shown in fig.4.1. The dark JV characteristics bend over at high current region due to series resistance[21].

4.1.2 Current Voltage Characteristics Under Illumination

The simplest model for a solar cell is a diode in parallel with a voltage independent current source.For an ideal cell, the I-V curve is just shifted along the current axis as the device is illuminated. This implies that light and dark characteristics will not cross.

But in real devices, there is a cross-over of dark and light J-V characteristics. Such cross-over relates to change in diode parameters with illumination; the light may cause a lowering of the junction barrier. Also there is change in dI/dV at small reverse bias as the light intensity increases.Since conduction is negligible at this bias, the change in slope must be a result of a voltage dependent current source. The cross over can be explained by the collection function g(V), the factor that includes the bias dependance of light generated current. This effect is included to J as,

$$J = J_0(exp(\frac{qV}{AkT}) - 1) - g(V)J_L^{\Delta} \tag{4.7}$$

where g(V) is the collection function and J_L^{Δ} is the voltage independent light generated current.

Since both the current transport and junction barrier may be sensitive to light, the diode factor A often takes on different values as the illumination intensity and wavelength is varied. Light saturation current J_{OL} is related to dark saturation current J_0 as,

$$J_{OL} = \frac{g(0)}{g(Voc)}J_0 \tag{4.8}$$

J_{OL} is slightly higher than J_0 due to collection function. There is also the change in junction barrier when cells are light soaked[17].

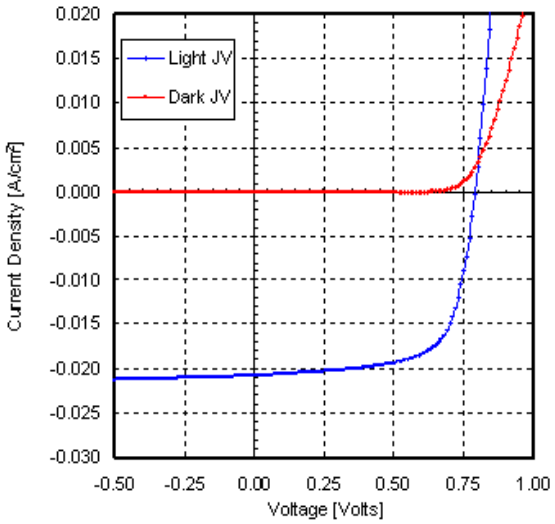

Figure 4.2 Cross over in IV curves

4.1.3 Roll Over in IV Curves Due to Back Contact Barrier

The roll over of IV curves occurs because the junction voltage saturates at high bias.This saturation occurs because of a back contact barrier. The saturation voltages for roll over under dark and illumination are given by[18],

$$V_{sdark} \simeq \frac{nkT}{q} \ln \frac{J_c}{J_s} \tag{4.9}$$

and

$$V_{slight} \simeq V_{sdark} + \frac{nkT}{q} \ln[1 + \frac{J_c}{J_s}] \tag{4.10}$$

respectively.Where J_c is the contact saturation current density and J_0 is the total reverse saturation current density.

4.1.4 Dynamic Resistance

The derivative dV/dJ is used to understand light and dark JV characteristics more clearly. Due to the non linearity of the physical phenomenon of the solar cell, the current voltage characteristics is non ohmic. This behavior is shown in the plot of the derivative dV/dJ with respect to voltage. The minimum resistance corresponding to a chosen value of high forward current(say 0.08 A/cm^2) can be taken as Rs, though this quantity doesn't reflect the real value of seies resistance of the device[20]. However this quantitity is useful to the extent, can represent the degradation of the device quantitatively.

The shunt resistance R_{sh} can be approximated by the slope of the current voltage characteristics in the low voltage region (say, -1.7V to -1 V).

4.1.5 Fill Factor Loss Due to Back Contact Barrier

The non-ideal FF is given by[18],

$$FF \approx FF_o(V_{oc}^1)[1 - \frac{kT}{qV_{oc}} \ln[1 + \frac{J_L}{J_c}]] \tag{4.11}$$

where,

$$FF_o(V_{oc}^1) \approx [1 - \frac{\ln V_{oc}^1}{V_{oc}^1}][1 - \frac{1}{V_{oc}^1}][\frac{1}{1 - \exp(-V_{oc}^1)}]$$

and

$$V_{oc}^1 = \frac{q(V_{oc} - \Delta V)}{nkT}.$$

Where ΔV is the forward bias at the back contact when light current flows under reverse bias. When the back contact diode saturation current J_c is larger than or equal to the light current, the FF loss due to the back contact is only a few percent. In contrast, considerable FF losses occur, if J_c is considerably smaller than J_L.

4.2 Spectral Response

There are a variety of possible optical losses before photons reach a solar cell's absorber, and there are additional losses from non radiative recombination or from photons exciting the absorber. Figure 4.3 is one example of the fraction of photons of each wavelength that contributed to photocurrent and the fractions that are lost in each of several ways. The loss includes the reflection from the cell, the absorption of the glass substrate,the absorption of the SnO_2 contact,and the absorption of the CdS window layer. Some photons are lost due to deep penetration at CdTe region.

4.3 CV Measurement

Information like doping profile, depletion width,acceptor concentration and barrier height of the junction Φ_b can be obtained from Capacitance-Voltage (CV) characteristics. As the CdS film has carrier concentration (approximately 1E+16 to 1E+17 electrons / cm^2) several orders of magnitude higher than that of CdTe (approximately 1E+13 to 1E+15 holes/cm^2), the depletion layer mainly spreads into the CdTe absorber layer to separate the photo-generated carriers. Hence only the permittivity of

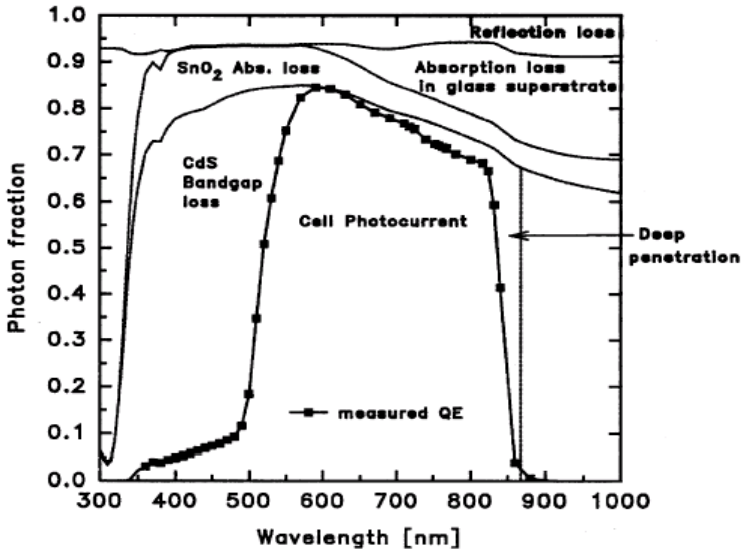

Figure 4.3 Photon Accounting for a CdTe Solar Cell [19]

CdTe layer is used to calculate the depletion layer width(W_d). This width changes as the external bias V is applied across the contacts of the solar cell. The depletion layer width(W_d) at particular bias V is calculated using

$$W_d = \frac{\epsilon_o \epsilon_r}{C/A} \tag{4.12}$$

Where ϵ_o is permittivity of free space(8.854E-14F/cm),ϵ_r is relative permittivity of CdTe layer(10.2), C is the capacitance(F) at that bias V and A is the effective contact area of the device.

The net acceptor concentration is then found from

$$N_A = \frac{2}{[q\epsilon_o\epsilon_r][d[C^2/A^2]/dV]} \tag{4.13}$$

where q is electic charge,1.6022E-19 Coulombs.

The accuracy of predicting real values using equations 4.12 and 4.13 may be affected due to following reasons:

- The equation 4.13 is valid only for homogeneously doped uncompensated p-type CdTe. For partially compensated CdTe layer, the value equals $N_A - N_D$ as $N_A > N_D$.

- The equations completely neglect minority carriers and assume total depletion of majority carriers in the space charge region[SCR].This is valid only when the SCR is reverse biased and substrate is uniformly doped.

- Also these equations are based on a single junction model.But CdTe/CdS has separate capacitance components for the main junction as well as the junction due to back contact schottky diode.This two diode circuit also affects the accuracy of values.

Though these sources of errors affect the real device parameter values, a relative comparison of the device parameter values may be valid in general.

Chapter 5
Experimental

5.1 Device Structure

The device used for this study had the superstrate structure (that is light enters through substrate first, which is 7059 Boro silicate glass) as shown in the fig.5.1.

The deposition procedures are described in detail elsewhere [22]. In brief, the front contact SnO_2 was deposited by the MOCVD [Metal Organic Chemical Vapor Deposition] technique and was deposited as $low-\rho/high-\rho$ bilayer. The sheet resistance of SnO_2 was below $10\Omega/\Box$. Cadmium sulfide of approximately $1000\mathring{A}$ was deposited using Chemical bath deposition(CBD) method. The CdTe deposition was carried out by Closed space sublimation(CSS) method at $550-600^oC$ as substrate temperature. The CdTe/CdS structure was then heat treated in the presence of $CdCl_2$.

The main objective of this thesis work was to analyze the the effect of $CdCl_2$ heat treatment on device stability. For this, the $CdCl_2$ annealing temperature was varied from 360 to 400^oC. Excess $CdCl_2$ was then removed by etching the samples in methanol/bromine solution for 8 seconds which results in smooth Te rich surface for contacting. Cu doped graphite paste or sputtered Cu_2Te was applied as back contact and heat treated at 270^oC for 25 minutes in vacuum.

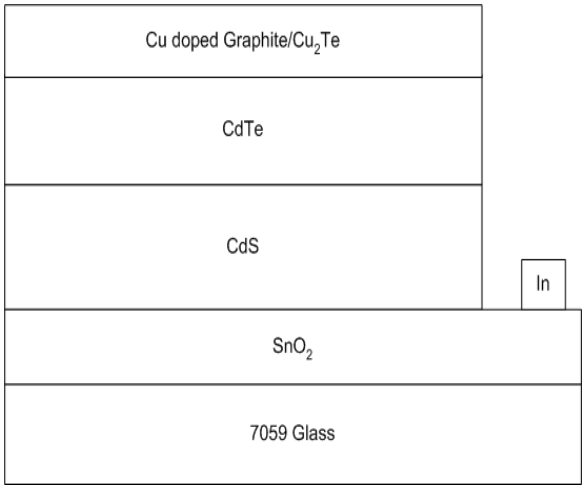

Figure 5.1 Device Structure

5.2 Measurement Setup

The measurement setup shown in fig.5.3 consists of a vacuum chamber which can be evacuated and back filled with ultra high purity N_2 gas prior to the beginning of light soaking. All devices under test were fabricated under identical conditions except the annealing temperature of the $CdCl_2$ treatment. Eight identical cells for each annealing temperature were stressed under one sun(AM1.5) illumination intensity(4 at short circuit and 4 at open circuit conditions).

The cells were placed on the copper plate sample bed as shown in fig.5.2.The samples were placed in such a way that the front contact(glass side) facing the light and back contact was in contact with a thin foil. The heat is transferred from the devices to cooling water with the help of high thermal conductivity compound.

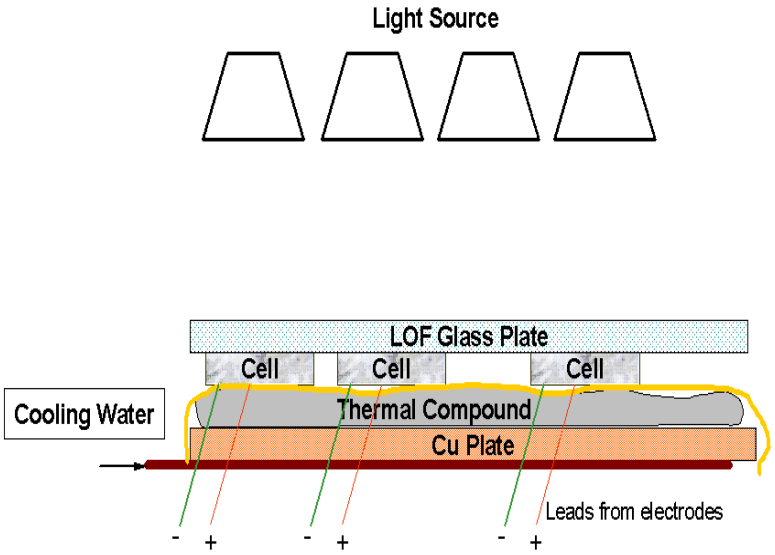

Figure 5.2 Sample Bed

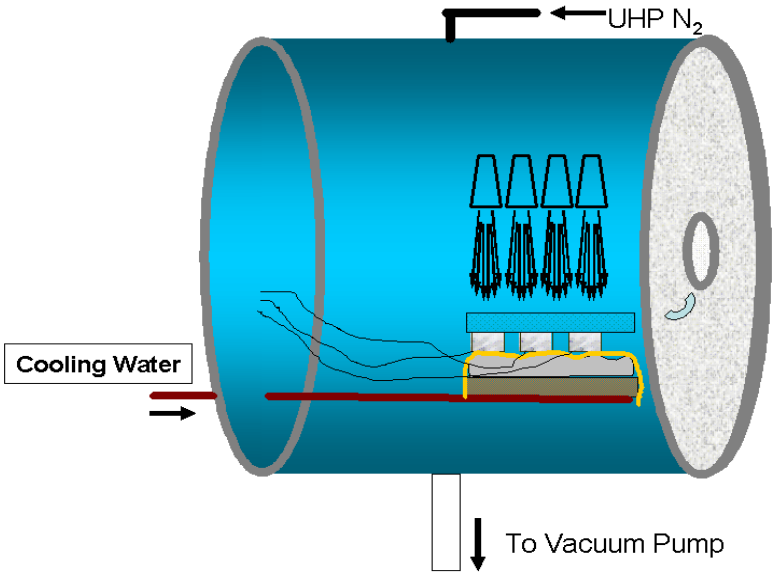

Figure 5.3 Measurement Setup

The light intensity was calibrated to approximately AM1.5 conditions($\pm 15\%$). Samples were under continuous light stress and N_2 ambient during the measurement.The samples were kept at dark and light cycle of 4 hours each.The temperature of the copper plate sample bed was controlled using water circulation.

The light source was made using GE 12V,71 W 25^o Beam MR16 lamps. Two sets of 10 lamps each were used to illuminate the samples in the front and back row of the sample bed.

The sample leads were connected to the Keithley Source Meter via low resistance copper electrical wires. The leads were attached to the front and back contacts (which is silver and indium respectively) using conductive silver epoxy. A brief heat treatment of 5 minutes was given to the samples at 100^oC for good adhesion. The samples were kept at vacuum desiccator before light soaking to avoid possible degradation caused by humidity. A clean soda lime glass was used to press the samples to the sample bed for better heat transfer. The light was diffused uniformly throughout the sample bed using quartz plates.

The temperature was continuously monitored and controlled using thermocouples and Euro Therm Controllers which control the water flow. The system was automated during this work and the details are given in the appendix.

Routine current-voltage(IV) measurements were done when the samples were being stressed inside the oven. A Keithley 2400 source meter was used for both Voltage

sweep and current measurement. The voltage sweep was from -2V to +2V with steps of 0.01V.

It should be mentioned that the following events could have an impact on the JV results presented in this thesis.

- The lamps failed 6-7 times during light soaking which introduced extended dark period and in turn could lead to unpredictable recovery in JV parameters of some cells.

- There was a water leak inside the chamber after 200 light soaked hours, though the cells did not get wet.

Capacitance-Voltage(CV) and Capacitance-frequency(CF) measurements were done using HP impedance analyzer 4145A. Spectral analysis for desired bandwidth of wavelengths of photons was done using Oriel Cornerstone monochromator (model 74100) with light source of GE 400W/120V quartz line lamp (model 43707). Silicon reference was used to adjust the light intensity prior to measurement.

Chapter 6
Results and Discussions

6.1 Effect of $CdCl_2$ Heat Treatment

The samples were prepared as described in section 5.2. The temperature of $CdCl_2$ heat treatment was varied from 360^oC to 400^oC. The dependance of the device parameters on the $CdCl_2$ treatment was given in fig.6.1. The Open circuit voltage (V_{oc}) was in the range of 800-850 mV for different annealing temperatures. The fill factor (FF) had a maximum for the cells annealed at 390^oC and decreased for both higher and lower temperatures. The deviation in FF was larger at high temperatures. The results were in good agreement with that of Okamato et.al[23].

The samples were then light soaked under the conditions specified in section 5.2. For this experiment, eight cells were selected for each annealing temperature. Four of them were stressed at Open circuit(OC) and four at short circuit (SC) conditions. It should be mentioned that the maximum operating temperature during the light soaking period could be 60^oC ($\pm 10^oC$) (refer fig.6.2) depending on the location on the sample bed.

6.1.1 Effect of Light Soaking on Voc and FF

Figure 6.3 shows the change in Voc and FF for samples annealed at 360^oC and light soaked at OC. The 1st Voc data point was taken at operating temperature, which

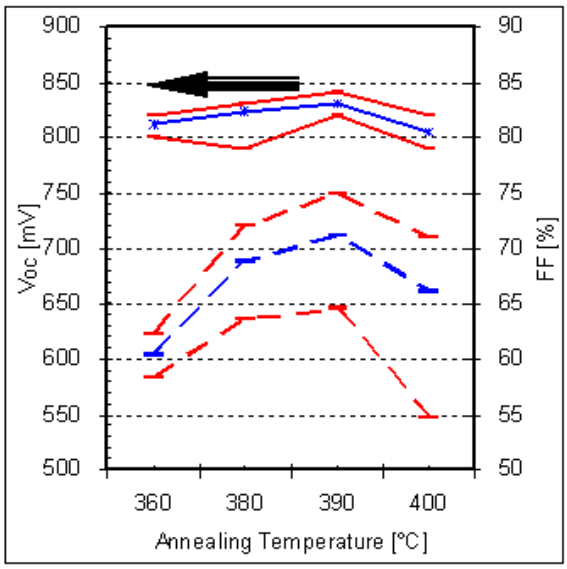

Figure 6.1 Effect of $CdCl_2$ Heat Treatment on Device Parameters

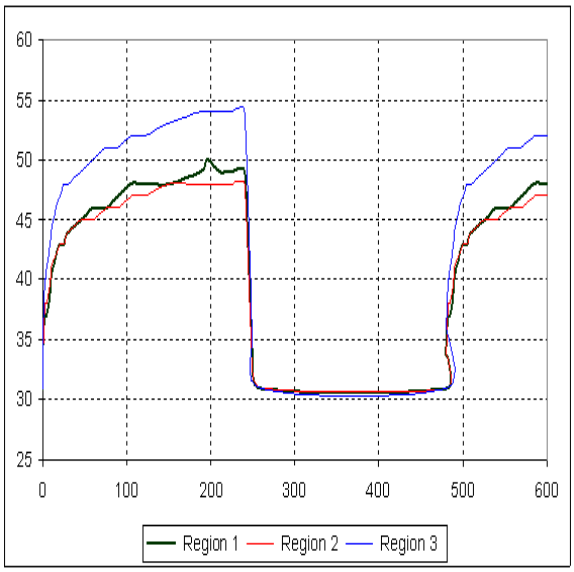

Figure 6.2 Temperature Profile During Stress Period(Temperature(^oC) Vs Time(min)).

is the reason for it being approximately 70-80 mV higher. Excluding this effect, the Voc was increased initially (up to 10 hours of light soaking) and stayed constant essentially thereafter for these samples. Near 1000 hours of light soaking, the Voc appears to decrease. The FF was nearly constant up to 100 hours of light soaking and decreased thereafter. The measurements at room temperature (at AM1.5 simulator after taking the samples out from the stability oven) are also given for comparison.

Figure 6.4 shows the change in Voc and FF for samples annealed at 360^oC and light soaked at SC. There was nearly no difference in the Voc behavior when compared to the OC stress condition. Whereas the FF was nearly unchanged up to 300 hours of light soaking, and decreased thereafter(sample 5-20A-1). Sample 5-20B-1 showed a deviation from this behavior. It can be speculated that the devices were not identical as assumed, though the reasons are not clear at this time. As the operating temperature increased during the ON cycle, the Voc measured during the 4th hour of light soaking was always lower than that of 1st hour.

Figures 6.5 shows the change for samples annealed at 400^oC and light soaked at OC. The change in Voc was essentially the same when compared to 360^oC samples. But the FF was improved and stayed unchanged up to 400 hours of light soaking and dropped thereafter.

Figure 6.6 shows the change in Voc and FF for samples annealed at 400^oC and light soaked at SC. There was essentially no change in Voc. Whereas the FF was

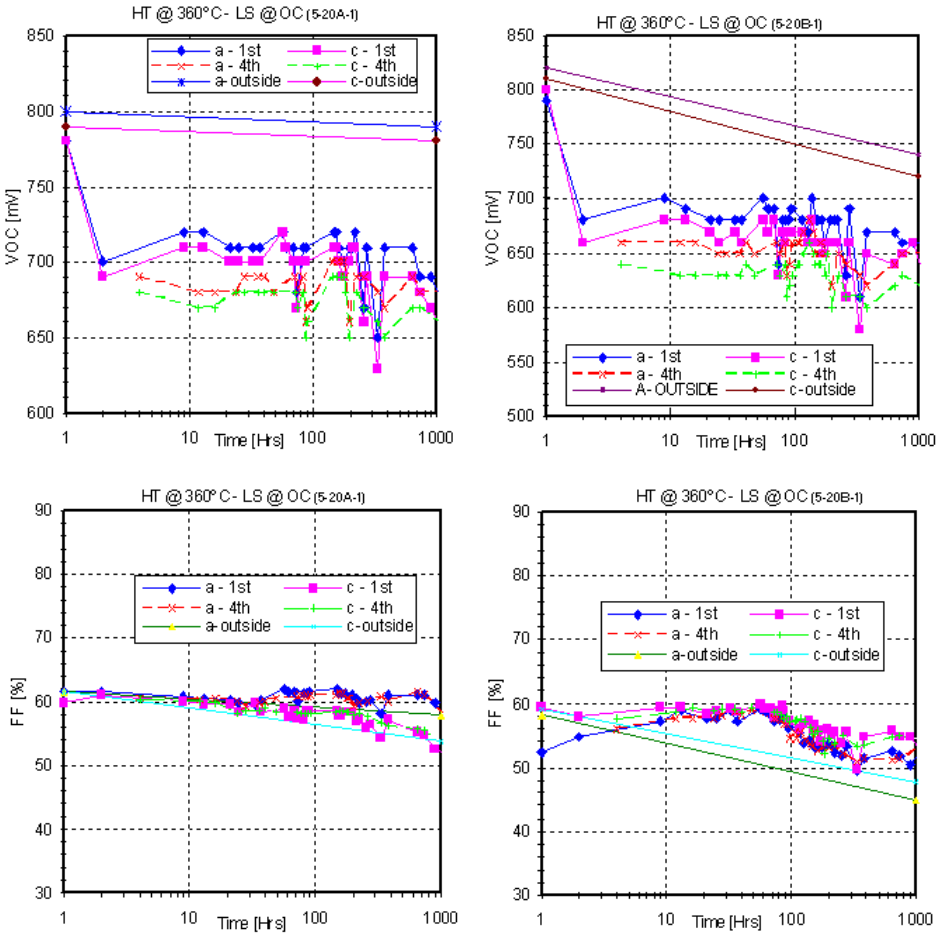

Figure 6.3 Degradation Behavior of Devices Heat Treated(HT) at 360^oC and Light Soaked(LS) @O.C

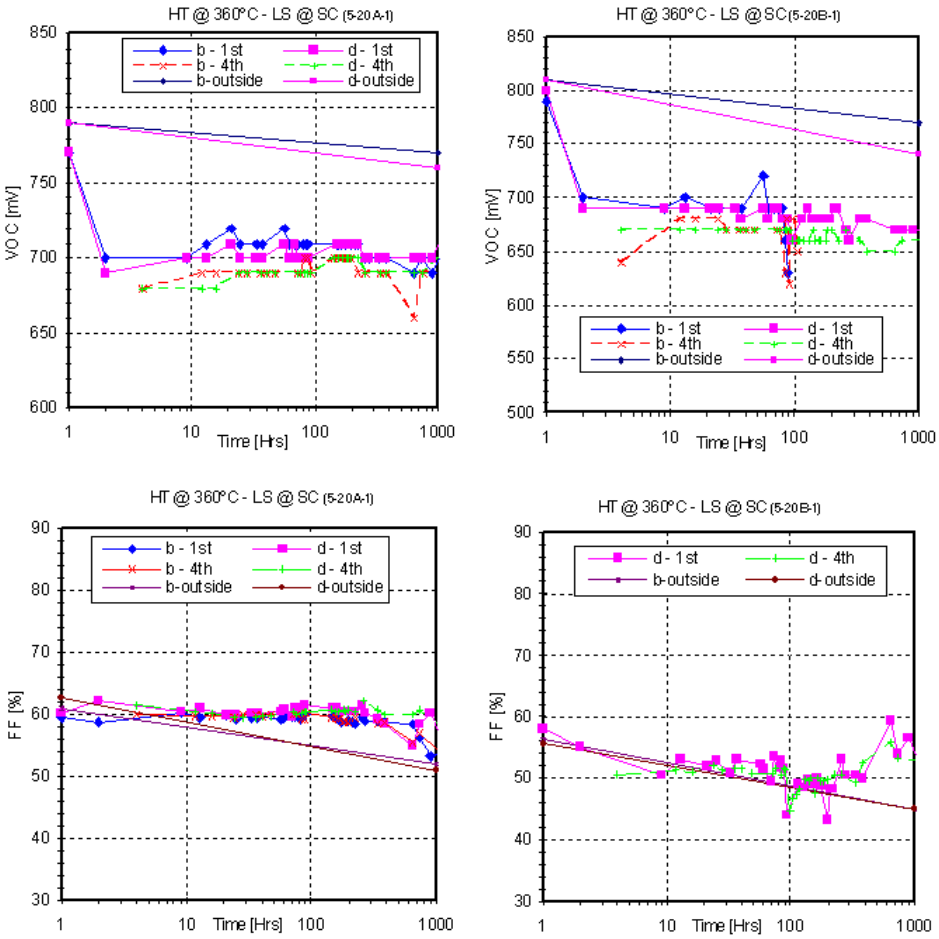

Figure 6.4 Degradation Behavior of Devices HT at 360^oC and LS @Short Circuit (S.C) Condition

decreased initially and stayed essentially constant thereafter up to 1000 hours of light soaking. It is not clear that what caused data scattering near 1000 hours.

6.1.2 Recombination Current

The increase in current at small voltages (below 0.5 V) for dark JV curves can be identified as either "shunting" or increase in recombination currents. From the J-V it appears that the dark current at low voltages(0.3V) is dominated by shunting. But in the 0.4-0.75V range, it also appears that the recombination current has increased. However, this "dark shunting" does not appear to lead to light shunting as the slope of the light JV is higher.

For samples annealed at 360^oC and light soaked @ OC, the major increase in recombination current and/or shunting occurred initially within 100 hours of light soaking (refer fig.6.7). Whereas, the SC stress condition limited this increase initially, though changes after 1000 hours of light soaking were same(refer fig.6.7).The cells shown were from the same substrate(5-20A-1) for both SC and OC stress conditions.

For samples annealed at 400^oC(shown in figures 6.9 and 6.10), the recombination current and/or "dark shunting" was increased after 100 hours of light soaking at OC similar to 360^oC case, though changes were less compared to that of the 360^oC samples. In this case also, S.C stress condition provided good control over recombination current change.

To summarize, the change in the $CdCl_2$ heat treatment or stress condition essen-

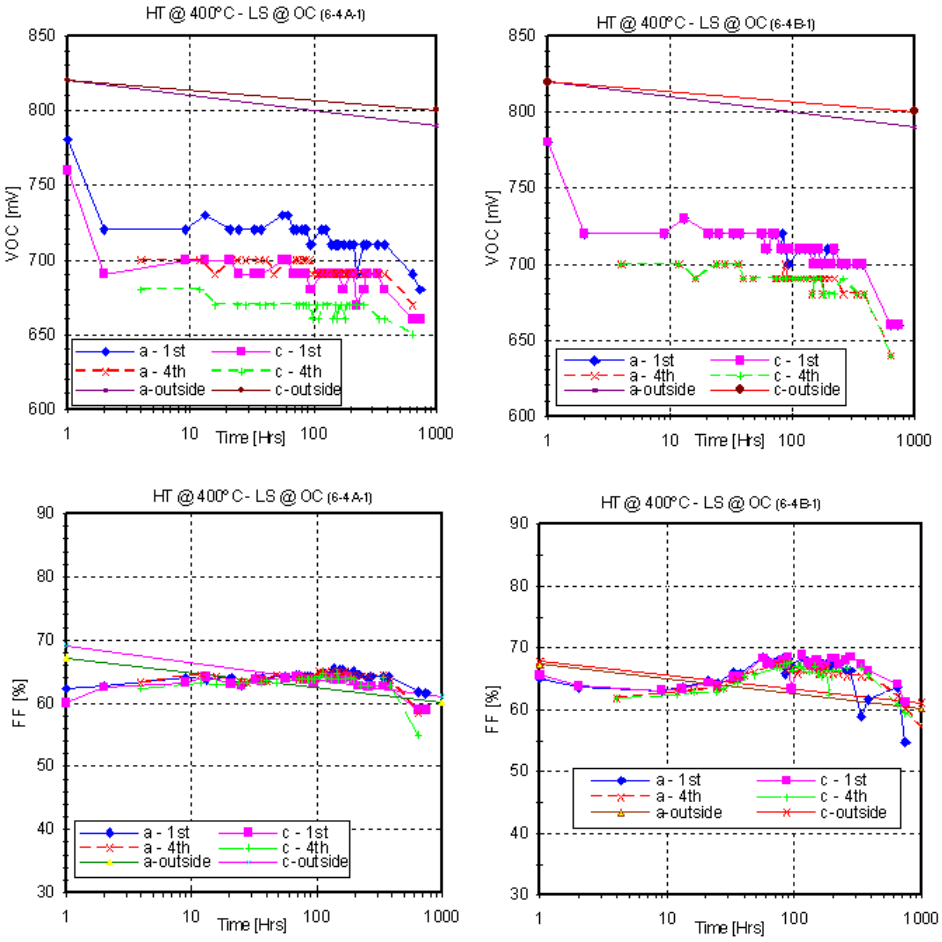

Figure 6.5 Degradation Behavior: HT @ 400^oC and LS @O.C

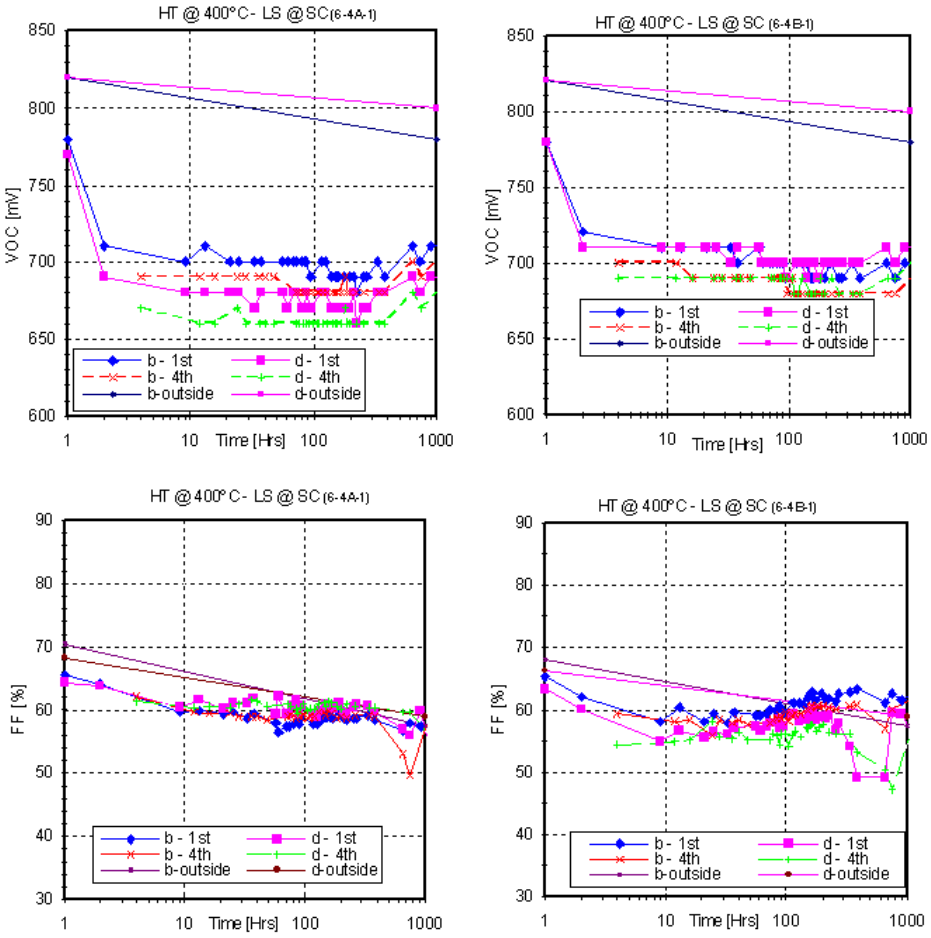

Figure 6.6 Degradation Behavior: HT @ 400^oC and LS @S.C

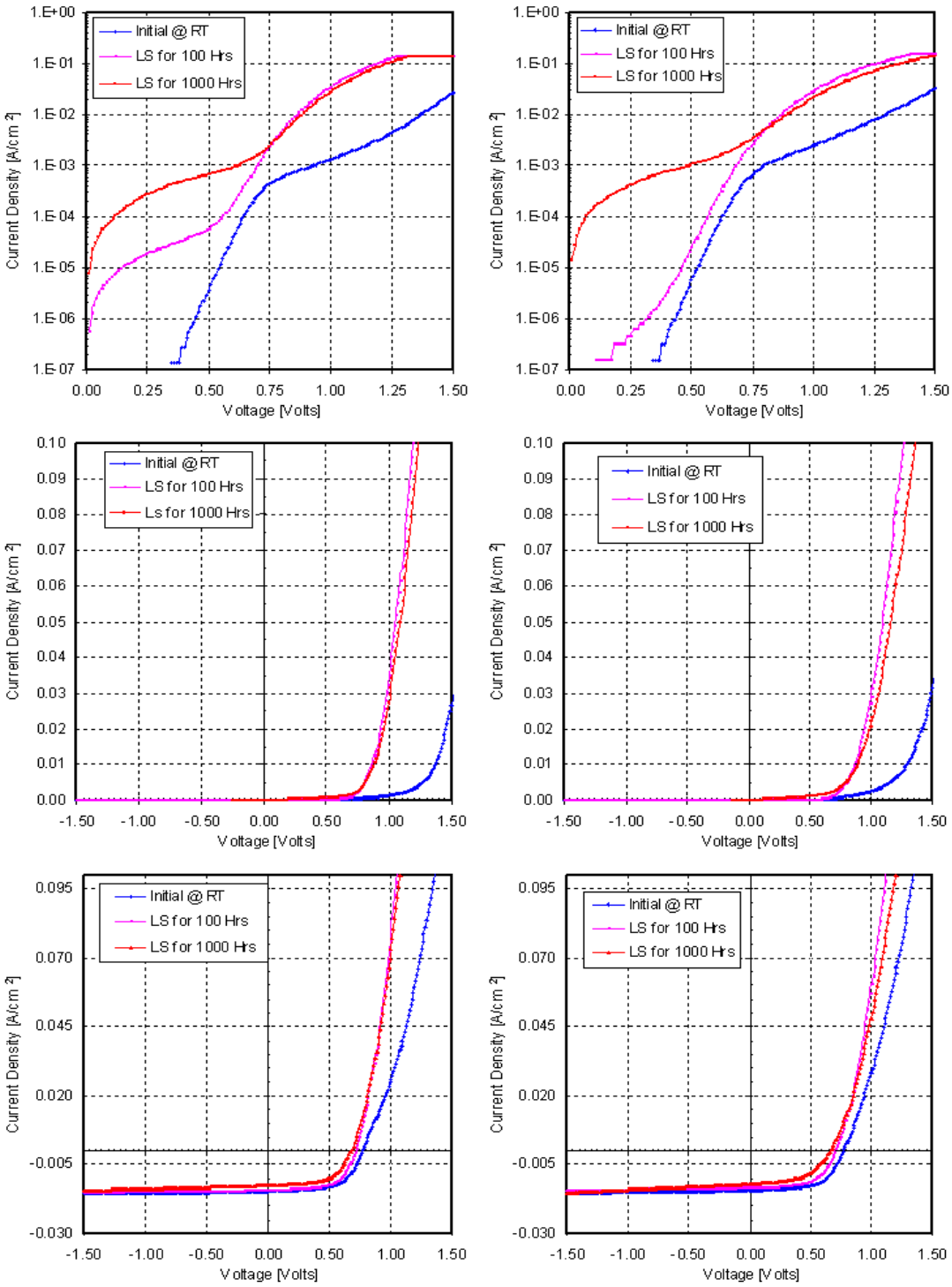

Figure 6.7 JV Characteristics. HT at 360^oC and LS at OC.(Top and Middle: Dark JV and Bottom: Light JV.)

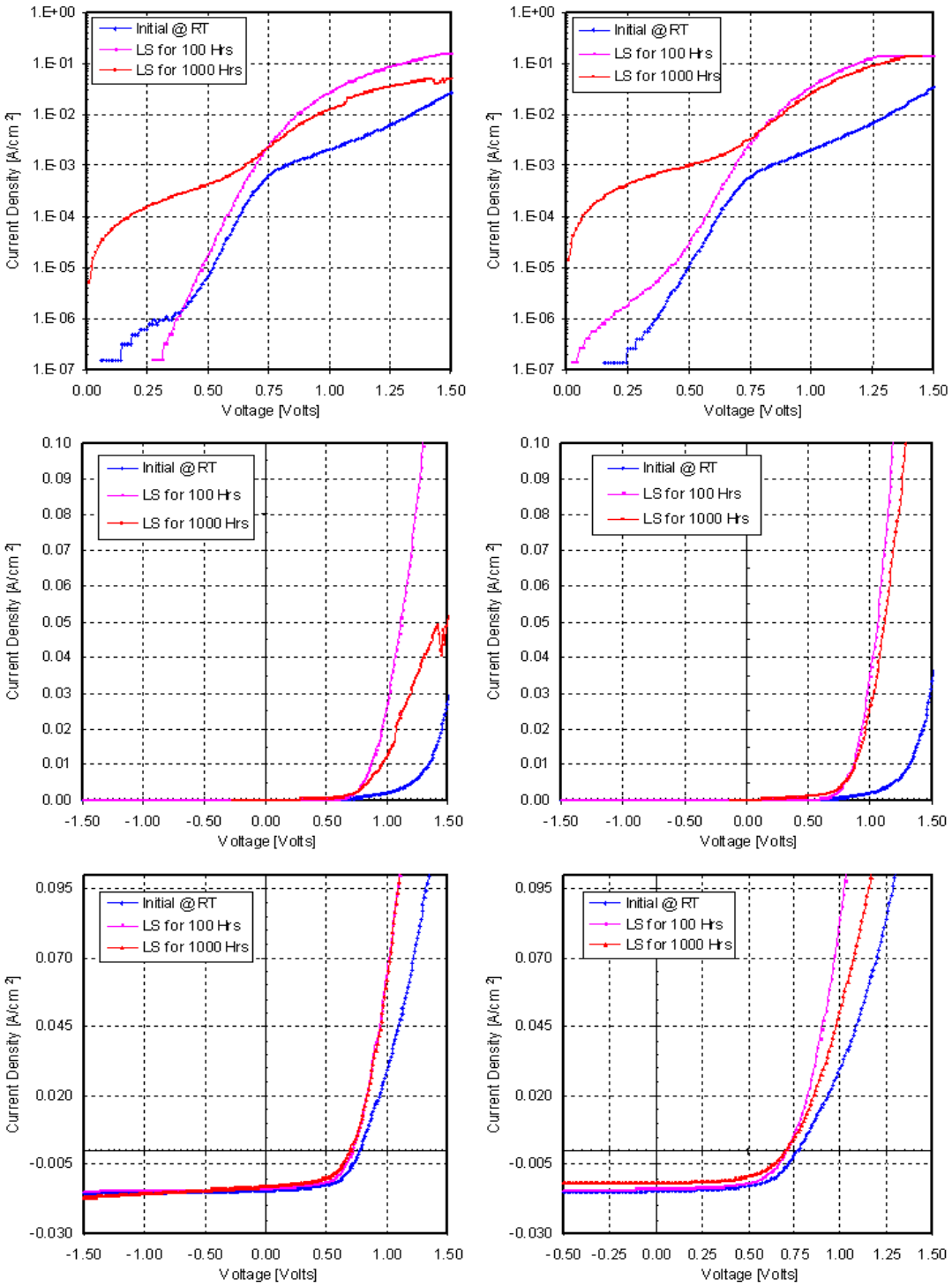

Figure 6.8 JV Characteristics. HT at 360^oC and LS at SC

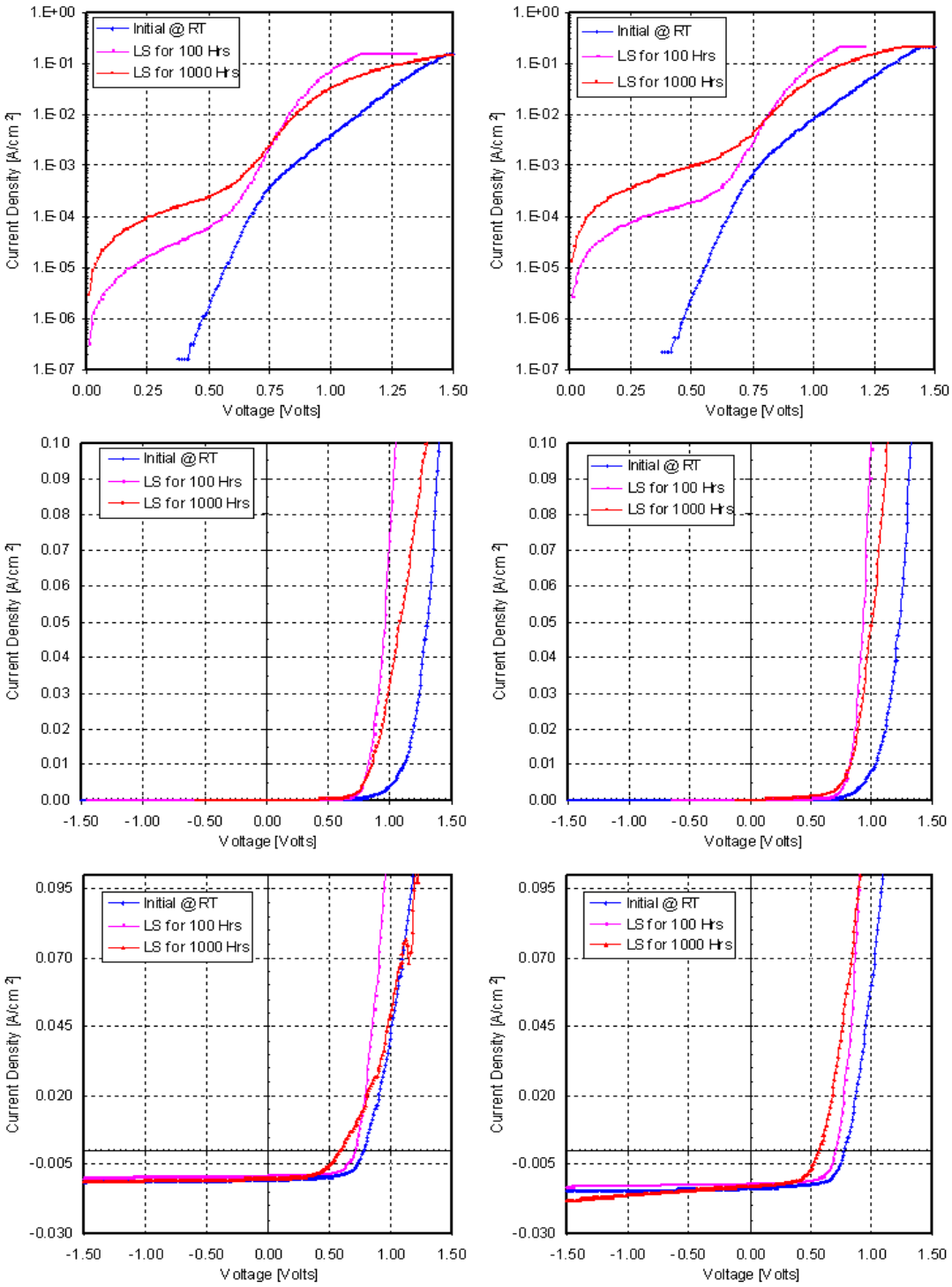

Figure 6.9 JV Characteristics. HT at 400^oC and LS at OC

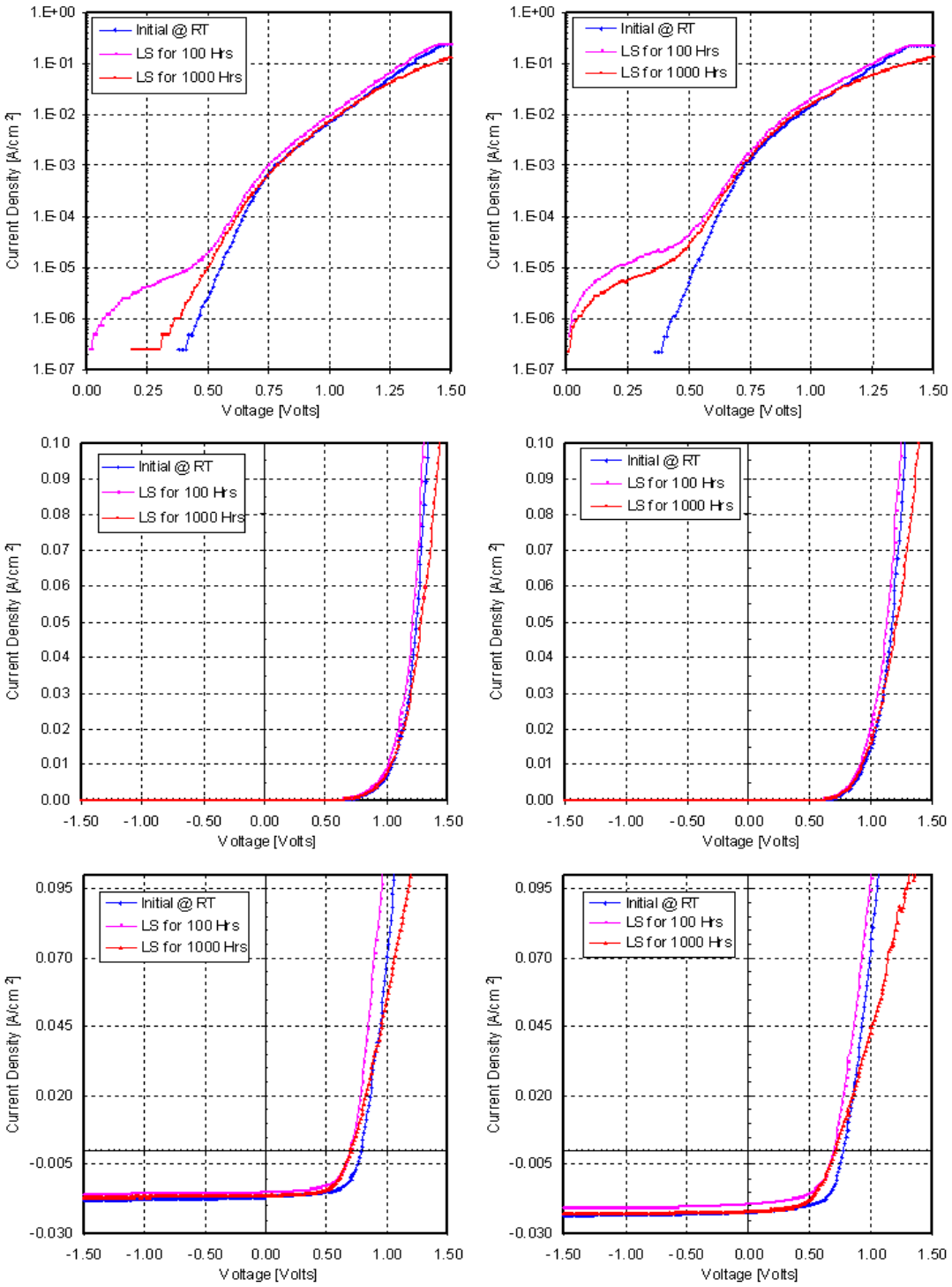

Figure 6.10 JV Characteristics. HT at 400^oC and LS at SC

tially did not affect the change in Voc during light soaking. Whereas the increase in the temperature of $CdCl_2$ heat treatment slowed down the drop in FF. Also when the device was stressed at SC, the drop in FF was delayed when compared to the samples at OC. The increase in recombination current were rapid if the $CdCl_2$ heat treatment was at low temperature. Also, the SC stress condition slowed down the change in the recombination current and/or "dark shunting" compared with OC.

6.1.3 Optimum Temperatures

The change in Voc and FF for samples with annealing temperatures of 380^oC and 390^oC during light soaking period was shown in the appendix. Poor contact for sample 5-13B-1 resulted in loss of data. The degradation rate was minimum for this optimum annealing temperatures of 380 and 390^oC. Only after 750 hours of light soaking, there was a change in the recombination current/"dark shunting" region. Still these changes were low compared with the 360^oC samples at OC. In case of short circuit condition, there was no change even after 1000 hours of light soaking. This implied that the device annealed at optimum temperature gave good performance during light soaking.

To summarize, the devices annealed at optimum temperature exhibited smaller increase in their recombination current and/or dark shunting. Also the SC condition appears to cause smaller changes in all instances.

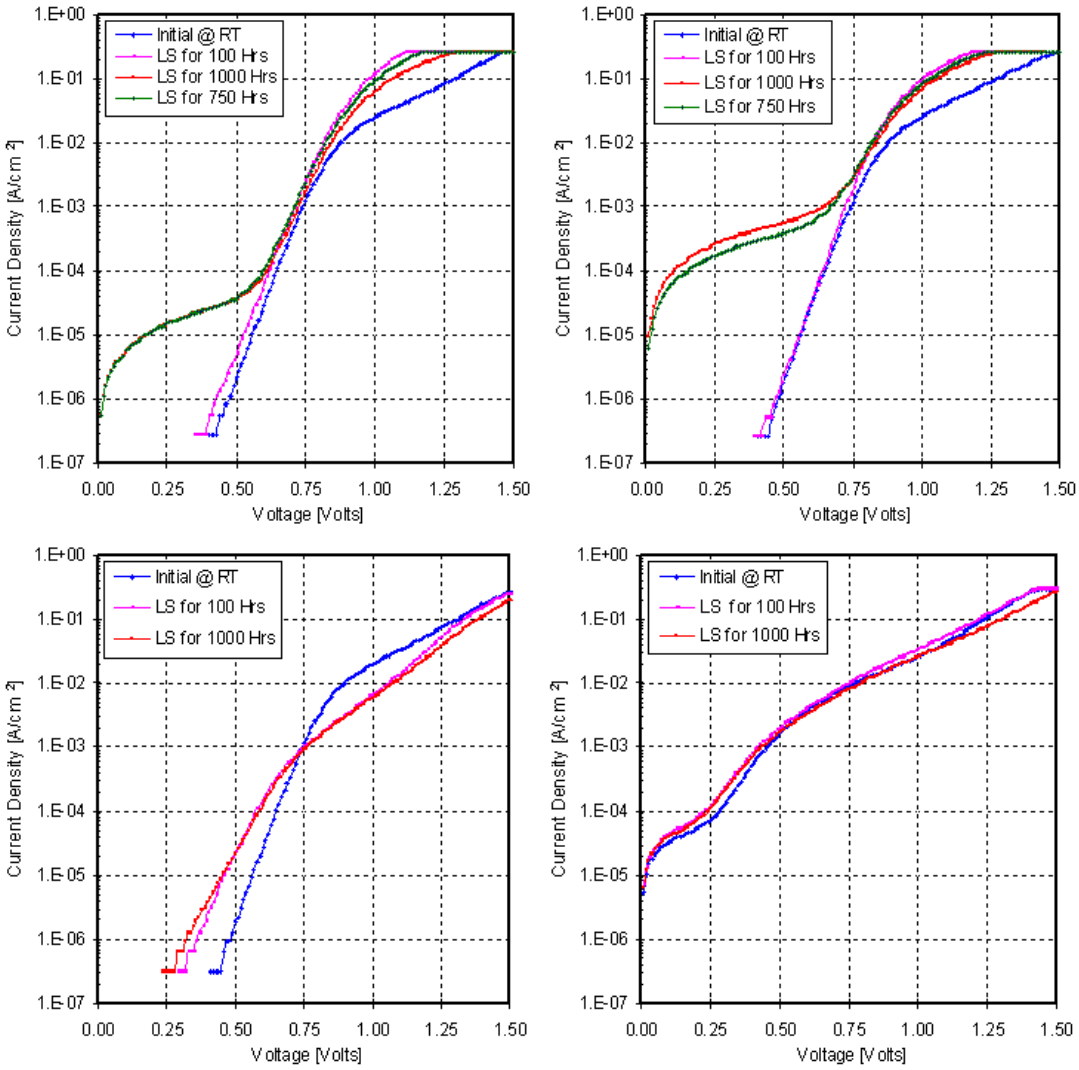

Figure 6.11 Dark JV Characteristics.(HT at 380^oC and LS at Top: OC and Bottom: SC.)

6.1.4 Effect of Micro Defects

Micro defects such as pinholes had a great impact on the performance in the device shown in table 6.1. The device that was light soaked for 1000 hours had the low Voc and FF. After breaking this device, the Voc and FF of one part increased dramatically. This shows that even a very small localized defect in a device can cause the entire device to be failed.

Table 6.1 Effect of Micro Defects on Results

Device	Voc(mV)	FF(%)
Device as whole	270	29
First half	810	64
Second half	160	28

6.1.5 Summary

The change in Voc and FF under OC and SC stress conditions are summarized in fig.6.12 by averaging similar devices under same stress conditions. The change in the $CdCl_2$ heat treatment or stress condition essentially did not affect the change in Voc during light soaking. Whereas the increase in the temperature of $CdCl_2$ heat treatment slowed down the drop in FF. Also when the device was stressed at SC, the drop in FF was delayed when compared to the samples at OC.Also the

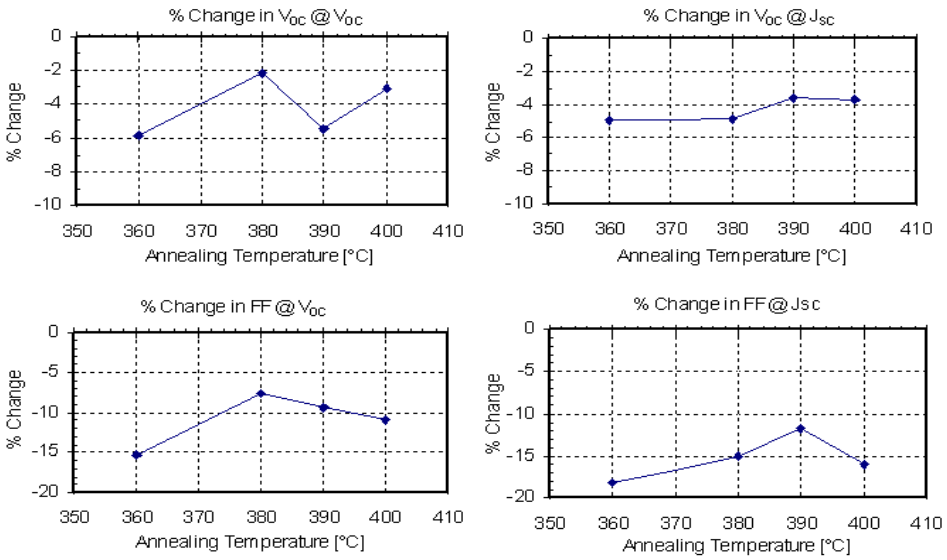

Figure 6.12 Summary of Degradation Behavior

devices annealed at the operating temperatures of 380^oC and 390^oC gave the better performance during light soaking. The effect of the stress condition on the device dark currents decreased, as the $CdCl_2$ annealing temperature was increased. The degradation can be attributed mainly to the change in recombination currents.

Series resistances were calculated as explained in section 4.1.4. The results are given in the appendix .

6.2 Cu_xTe As Back Contact

Even though a detailed study of the effect of the Cu_xTe back contact on device stability was not done, some cells were stressed during the initial phase of this work. The device structure was 7059 glass substrate/SnO_2/CBD CdS/CSS CdTe/Cu_2Te.

The Cu_xTe contact was applied using optimized procedures described elsewhere. Briefly,Cu_xTe was sputtered onto CdTe after the surface was etched in Br_2/Methanol. The thickness of the Cu_xTe was varied. Following Cu_xTe deposition, Mo was deposited to a thickness of $1\mu m$.

The dark and light JV characteristics for samples with Cu_2Te of $60\mathring{A}$ and $70\mathring{A}$ respectively were shown in fig.6.13. The J-V of of $70\mathring{A}$ shows that the device has a back contact barrier, which after light soaking for 1000 hours increases severely limiting the FF.

The J-V of $60\mathring{A}$ shows no barrier. After 1000 hours, there was a drop in Voc without roll over. This conveys that there is a condition for "right" amount of Cu to at least limit the degradation of the back contact.

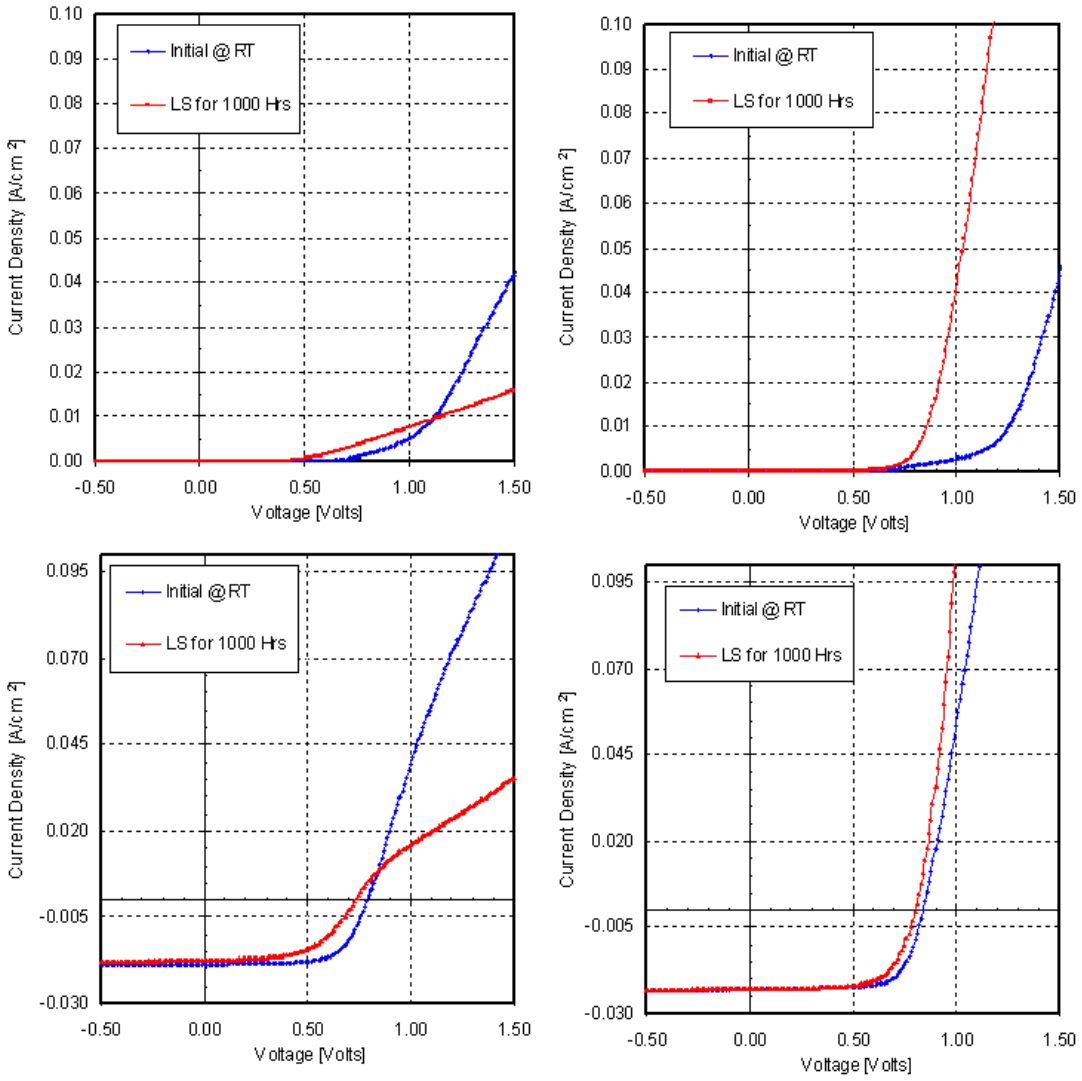

Figure 6.13 Degradation behavior of samples with Cu_2Te as Back contact with Thickness Left: 70^oA and right: 60^oA respectively.

Chapter 7
Conclusion

Light soaking experiment of CdTe/CdS solar under different stress conditions was conducted up to 1000 hours. The cells are made at different process conditions to observe the effect of process conditions on device stability.

The change in the $CdCl_2$ heat treatment or stress condition caused approximately 5% change in the Voc regardless of stress or process conditions. Whereas the increase in the temperature of $CdCl_2$ heat treatment slowed down the drop in FF. Also when the device was stressed at SC, the drop in FF was delayed when compared to the samples at OC. When the $CdCl_2$ heat treatment reached optimum temperature of $380-390^oC$, the degradation was minimum.The degradation can be attributed mainly to the change in recombination current.

7.1 Recommendations for Future Studies

As the duration of this investigation is too short to make complete analysis of stability behavior of CdTe/CdS solar cells, the following studies are recommended to be conducted in future.

- The range of stress conditions can be widened to characterize their effect on stability of devices produced under various process conditions.

- Advanced analytical techniques must be used to reveal the course for the increases in the dark currents.

- Since the back contact also contains HgTe, the Effect of Hg on device degradation can also be analyzed.

References

1. S.E. Asher et. al, Determination of Cu in CdTe/CdS Devices Before and After Accelerated Stress Testing,IEEE PV Spec. Conf.,Vol.28, pp. 479-482 (2000)

2. D. Cahen et. al, Overcoming Degradation Mechanisms in CdTe Solar Cells,Final Report,Weizmann Institute of Science,Israel, NREL (1998-2001)

3. D. L. Btzner et al, Thin Solid Films,Vol.387, No.1-2, pp. 151-154 (2001)

4. S.S.Hegedus et al,Analysis of Stress Induced Degradation in CdS/CdTe Solar Cells, NCPV Program Review Meeting, Denver, CO, April 16-19 (2000)

5. Su-Hai Wei et. al, Electronic structures and defect physics of Cd-based semiconductors,IEEE PV Spec. Conf.,Vol.28, pp. 483-486 (2000)

6. E.H Rhoderick et. al, J.Appl.Phys,D:App. Phy.,Vol.4,pp. 1589-1601 (1971)

7. Alan L. Fahrenbruch and Richard H. Bube, Fundamentals of Solar Cells,Academic Press,New York,pp. 234 (1983)

8. T.J.McMahon et. al, Progress toward a CdTe Cell Life Prediction,NCPV Photovoltaics Program Review,CP 462, pp. 54-61(1999)

9. R.C Powel et. al, Stability Testing of CdTe/CdS Thin Film PV modules,IEEE PV Spec. Conf.,Vol.25, pp. 785 (May,1996)

10. K.D.Dobson et.al, Stability of CdTe/CdS Thin Film Solar Cells,Solar Energy Materials and Solar Cells,Vol.62, pp. 295-235 (2000)

11. D.Grecu et.al, Appl.Phys.Letter,Vol.75, No.6, pp. 361-363 (1999)

12. H.R.Moutinho et. al, Studies of Recrystallization of CdTe Thin Films After $CdCl_2$ Treatment,IEEE PV Spec. Conf.,Vol.26, NREL (1997)

13. K.M.Al Shibani, Effect of Iso Thermal Annealing on CdTe and the study of electrical Properties of Au-CdTe Schottky Barriers,Physica B.,Vol.322,pp. 390-396 (2002)

14. B.E McCandless et al, 25th PVSC Conference,IEEE,Vol.25,pp. 781 (1996)

15. R.Ludeke, A Survey of Optical and Electrical Properties of Thin Films of II-VI Semiconducting Compounds,J.Vacuum Science and Tech.,Vol.8,pp. 199-207 (1971)

16. H.Oumous et al, Optical and Electrical Properties of Annealed CdS thin films Obtained from a Chemical Solution,Thin Solid Films,Vol.386,pp. 87-90 (2001)

17. Fredrick Buch, Photovoltaic II-VI Compound Heterojunctions For Solar Energy Conversion,PhD Dissertation, Stanford University, June (1976)

18. A.Niemegeer and M.Burgelman, J.Appl.Phys.,Vol.81, No.6, pp. 2881-2885 (1997)

19. James R.Sites, Solar Energy Materials and Solar Cells,Vol.75, No.1-2, pp. 243-251 (2003)

20. Donald Thomas Morgan, An Investigation into Degradation of CdTe Solar Cells,M.S.Thesis, Colorado School of Mines, pp. 20-29 (1998)

21. Donald A. Neamen, Semiconductor Device Physics: Basic Principles, Third Edition, Tata McGraw Hill, pp. 238-318 (2002)

22. C.S Ferekides et.al, Thin Solid films,Vol. 361-362, pp. 520-526 (2000)

23. T.Okamoto et.al, Thin Solid Films, 387, pp. 6-10 (2001)

APPENDICES

Appendix A

Measurement Automation

Automation of the Stability measurement system fulfills the following needs

- Consistency and accuracy of measured data,
- Reduction in measurement time and hassles involved,
- Easy Configuration of Stress Conditions,
- Massive Data Collection and
- Data logging and monitoring of stress temperature,humidity and stress period.

The hardware part consists of solid state relays which is controlled by PCI digital IO card via opto couplers.The relay is in NC position when not energized.The required stress conditions can be configured in this position via terminals provided from NC and GND(which is connected to n side of diode to be tested) outputs.The possible configurable stress conditions are open circuit,short circuit,maximum Load and, forward and reverse bias.When the relay is energized,the device under test(DUT) is connected to measurement device.Care must be taken while programming relays to avoid simultaneous activation of more than one relay.The dip switch is provided to isolate a relay from experiment in case of circuit failure.Totally 48 relays are controlled by a single 48 DIO card which consists of 2-8255 PPI chips. DUT is thus continuously maintained in the desired stress condition except for the duration in few seconds during measurement.Keithley 2400 source meter is used to sweep the voltage from -2V to +2V in steps of 0.02V and measure the current during I-V measurement.

Omega 44-M data logger is used to monitor temperature and humidity.It is connected from the stress oven via RS 232 interface.Software is provided by Omega to collect the data. It contains internal temperature and humidity sensors and two external thermistors.Sampling interval can be varied from 0.5 sec.

The software is developed using LabView.The front panel of main vi program and its block diagram of data flow during dark cycle are shown.Some of the salient features of the software are

- Day and night cycle are monitored and logged,
- Logic is entirely based on real time test condition,
- The measurements are avoided in case of lamp failure,

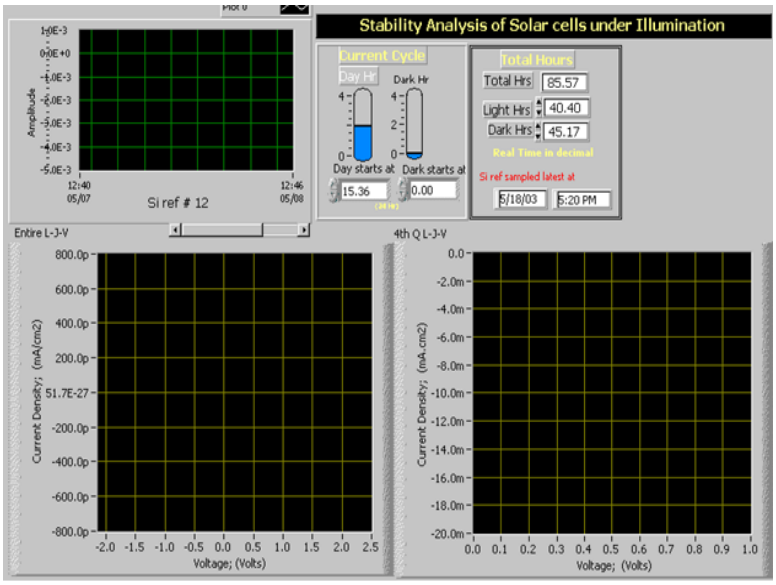

Figure A.1 Front Panel of VI Program for Stability Testing

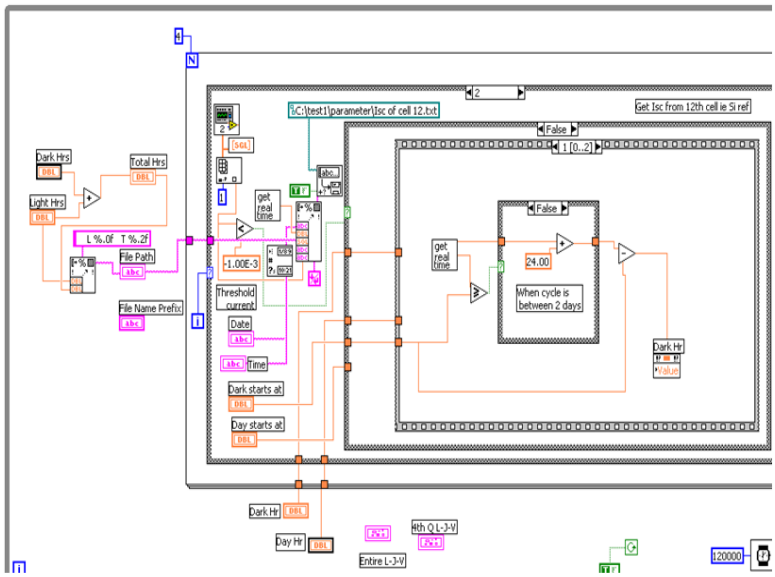

Figure A.2 Snap Shot of Block Diagram

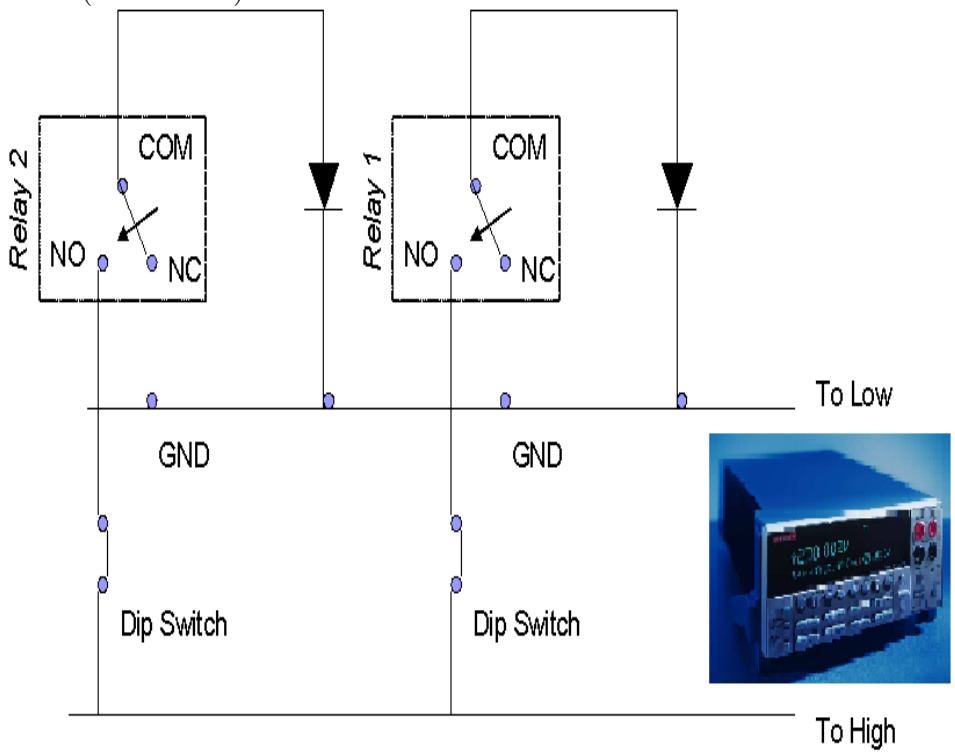

Figure A.3 Circuit Configuration of Hardware Setup

- The total light soaked hours are calculated with milli second accuracy,
- Day transition will not cause problems,
- Measurement timings can be custom defined for any number of times needed
- The code is optmised to avoid memory leaks and
- The device parameters are stored in well defined manner for easy retrieval for data analysis.

  The measurement timings must be given in ascending order.Also the interval should be greater than the single measurement set period of (18+5) minutes to avoid missing of data points.

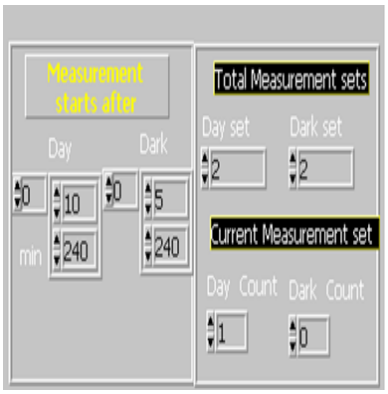

Figure A.4 Input Panel for Measurement Interval Specification

Appendix B

JV Characteristics

Table B.1 Average Estimates of and Series Resistance after LS @ OC.

HT(^oC) after $CdCl_2$ treatment	LS Period	$R_{s,light}[\Omega - cm^2]$	$R_{s,dark}[\Omega - cm^2]$
360	Initial	3.0275	3.975
	LS for 1000 Hrs	3.38	3.535
380	Initial	2.525	6.23
	LS for 1000 Hrs	2.99	1.405
400	Initial	1.882	2.81
	LS for 1000 Hrs	3.36	3.25

Table B.2 Average Estimates of and Series Resistance after LS @ SC.

HT(^oC) after $CdCl_2$ treatment	LS Period	$R_{s,light}[\Omega - cm^2]$	$R_{s,dark}[\Omega - cm^2]$
360	Initial	2.73	3.85
	LS for 1000 Hrs	3.53	3.1
380	Initial	2.39	11.62
	LS for 1000 Hrs	4.10	4.95
400	Initial	2.11	2.63
	LS for 1000 Hrs	3.74	5.45

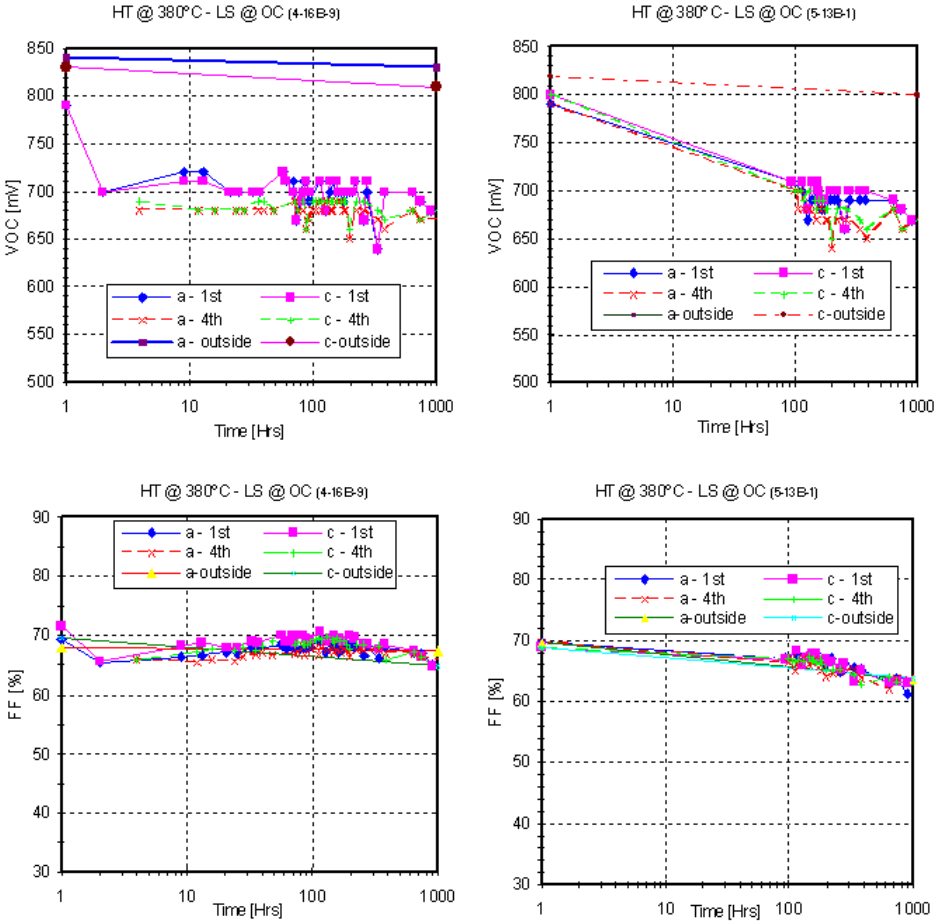

Figure B.1 Degradation Behavior: HT @ 380^oC and LS @O.C

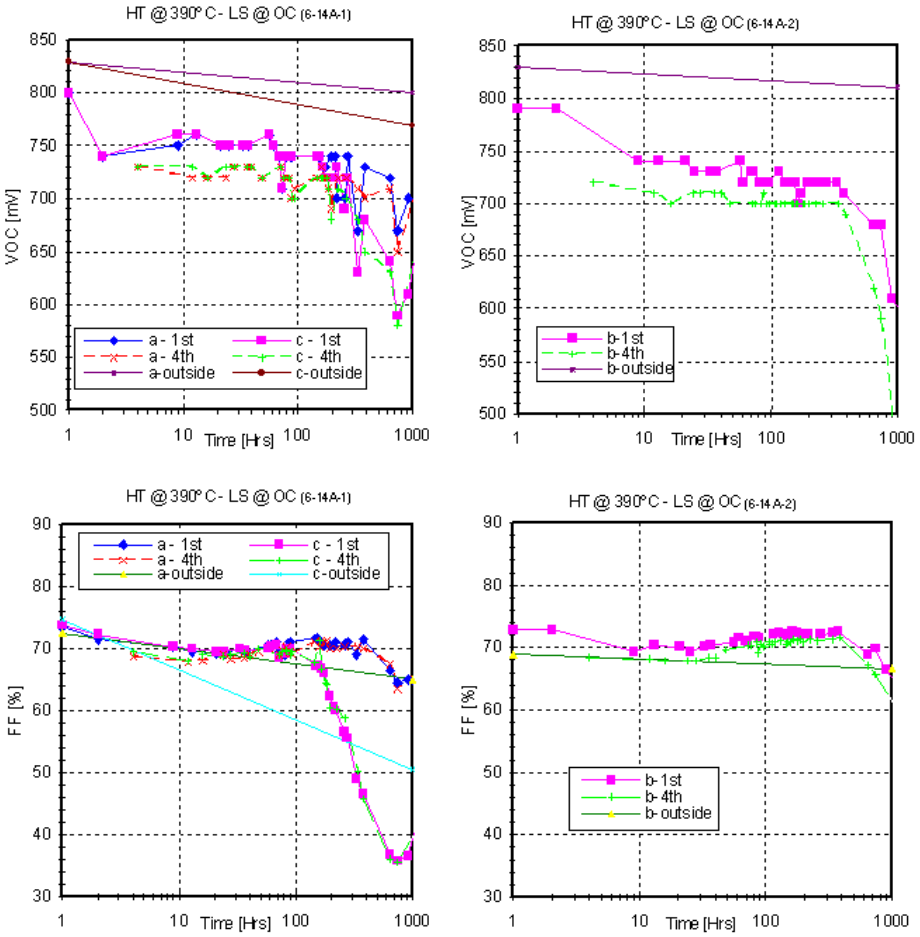

Figure B.2 Degradation Behavior: HT @ 390^oC and LS @O.C

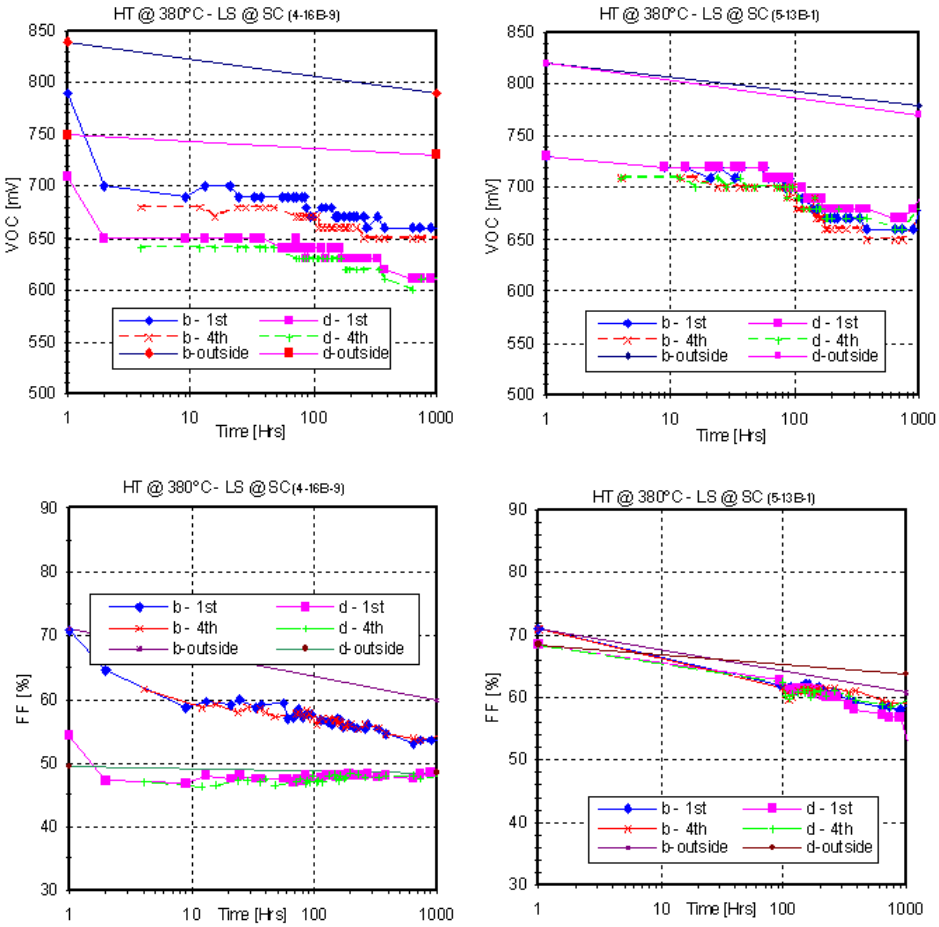

Figure B.3 Degradation Behavior: HT @ 380^oC and LS @S.C

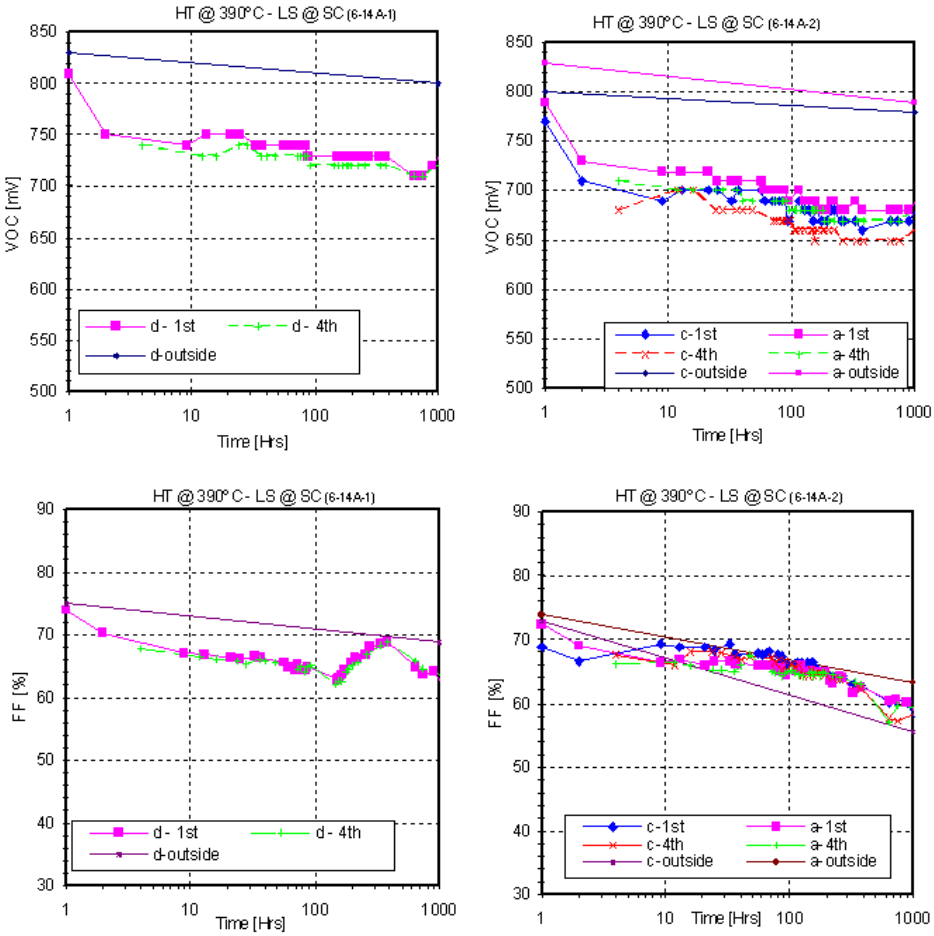

Figure B.4 Degradation Behavior: HT @ 390^oC and LS @S.C

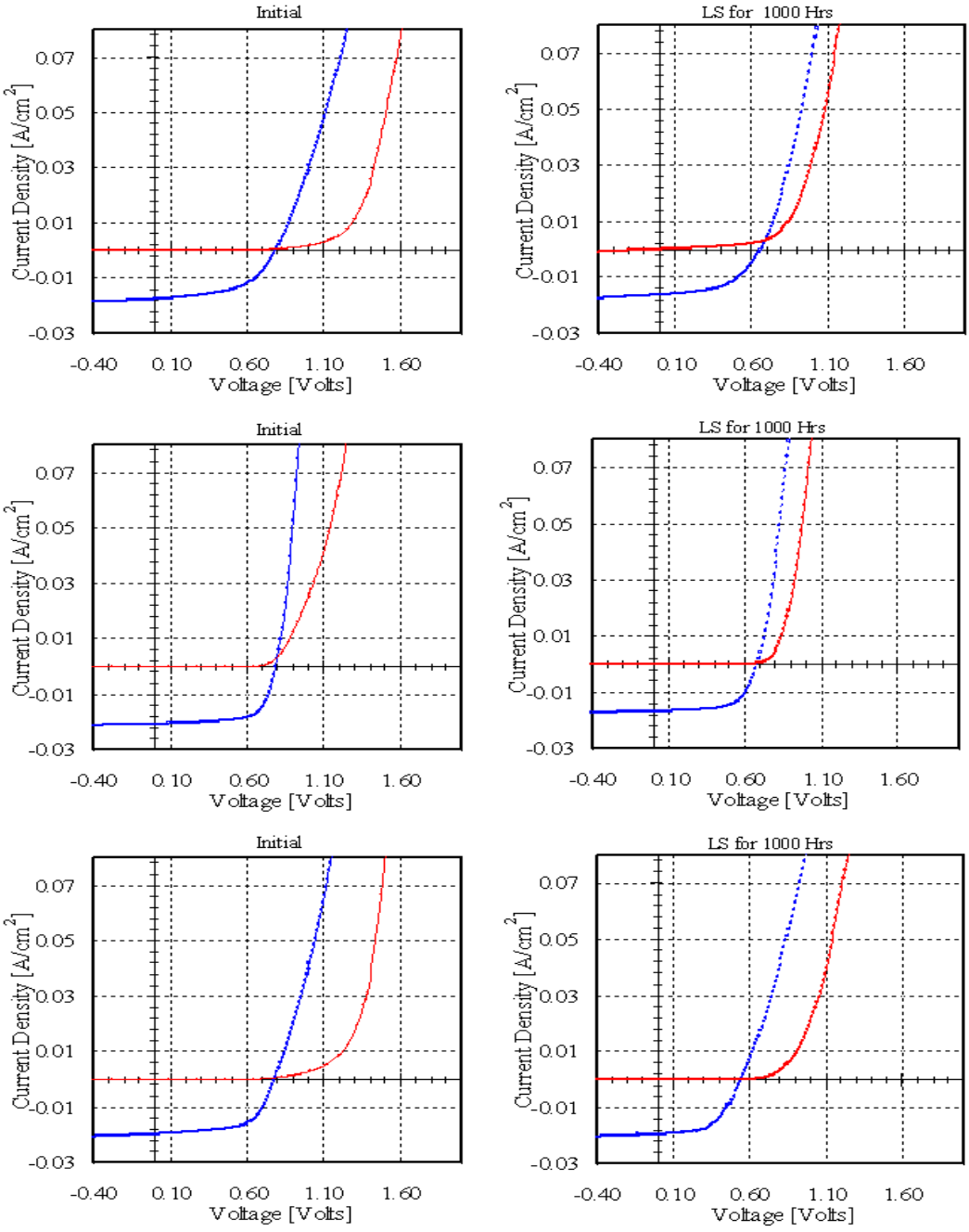

Figure B.5 Cross Over Effect for Samples LS @ OC and HT @ Top : 360^oC , Middle : 380^oC and Bottom : 400^oC

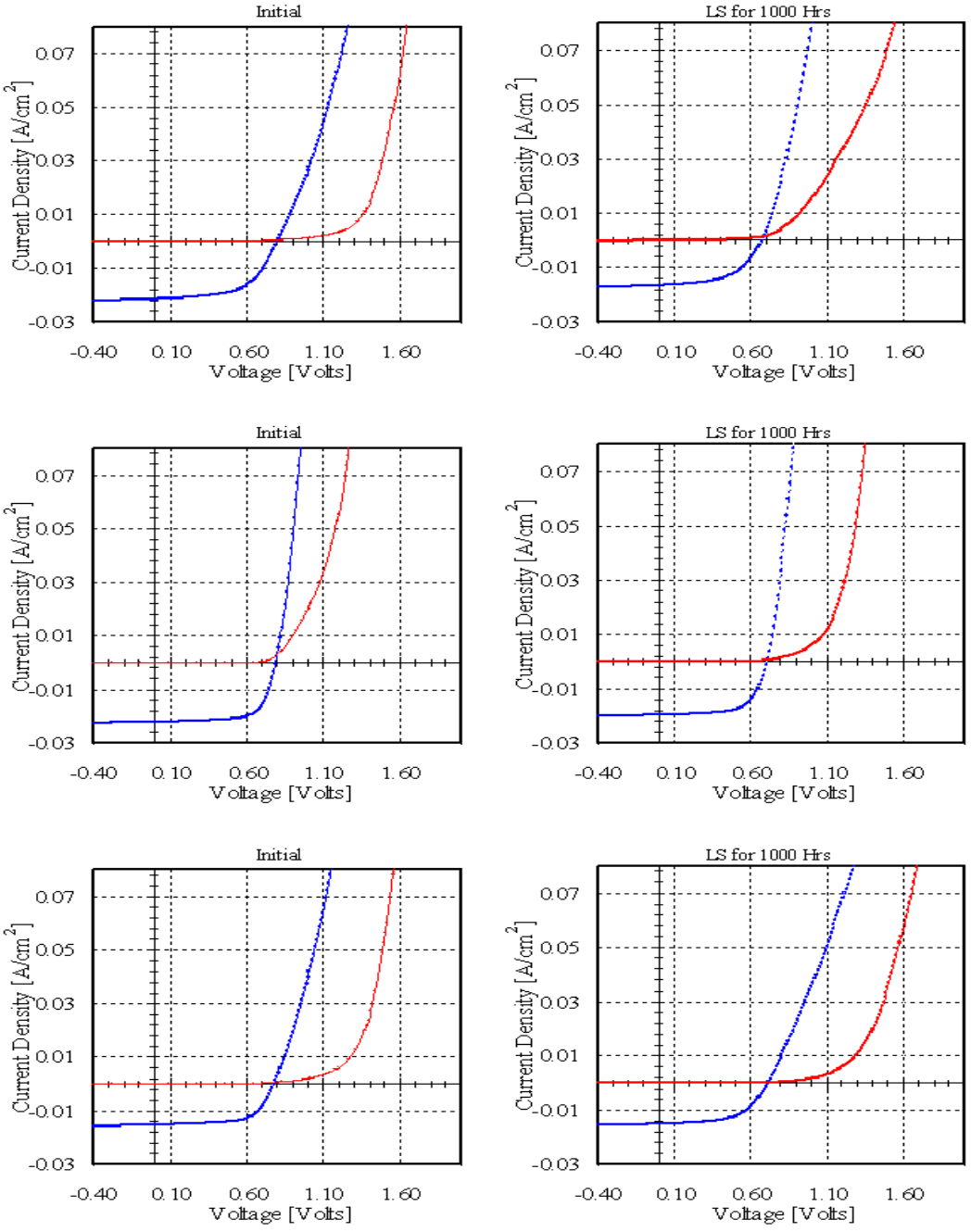

Figure B.6 Cross Over Effect for Samples LS @ SC and HT @ Top : 360^oC Middle : 380^oC and Bottom : 400^oC

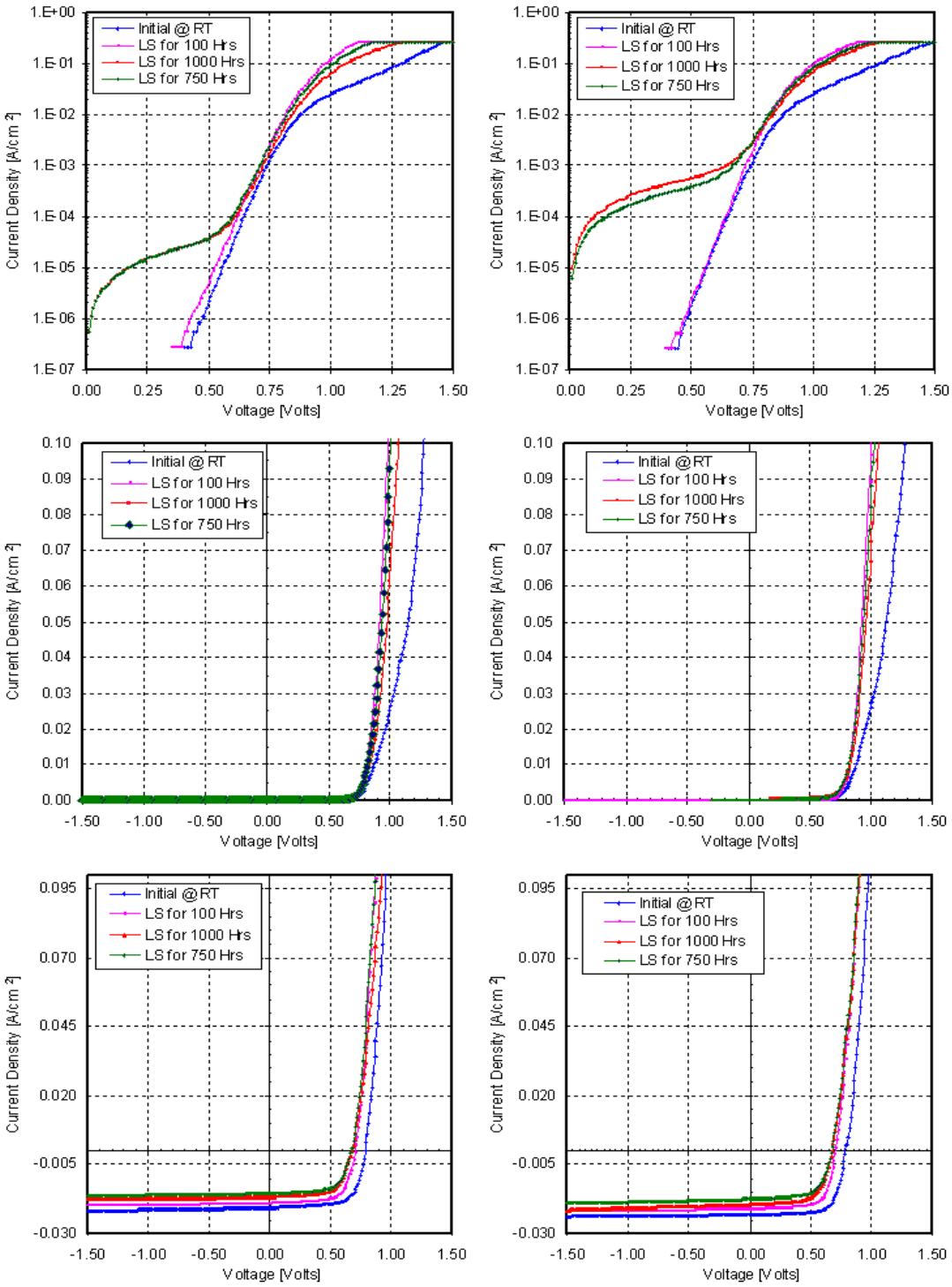

Figure B.7 JV Characteristics. HT at 380^oC and LS at OC.(Top and Middle: Dark JV and Bottom: Light JV.)

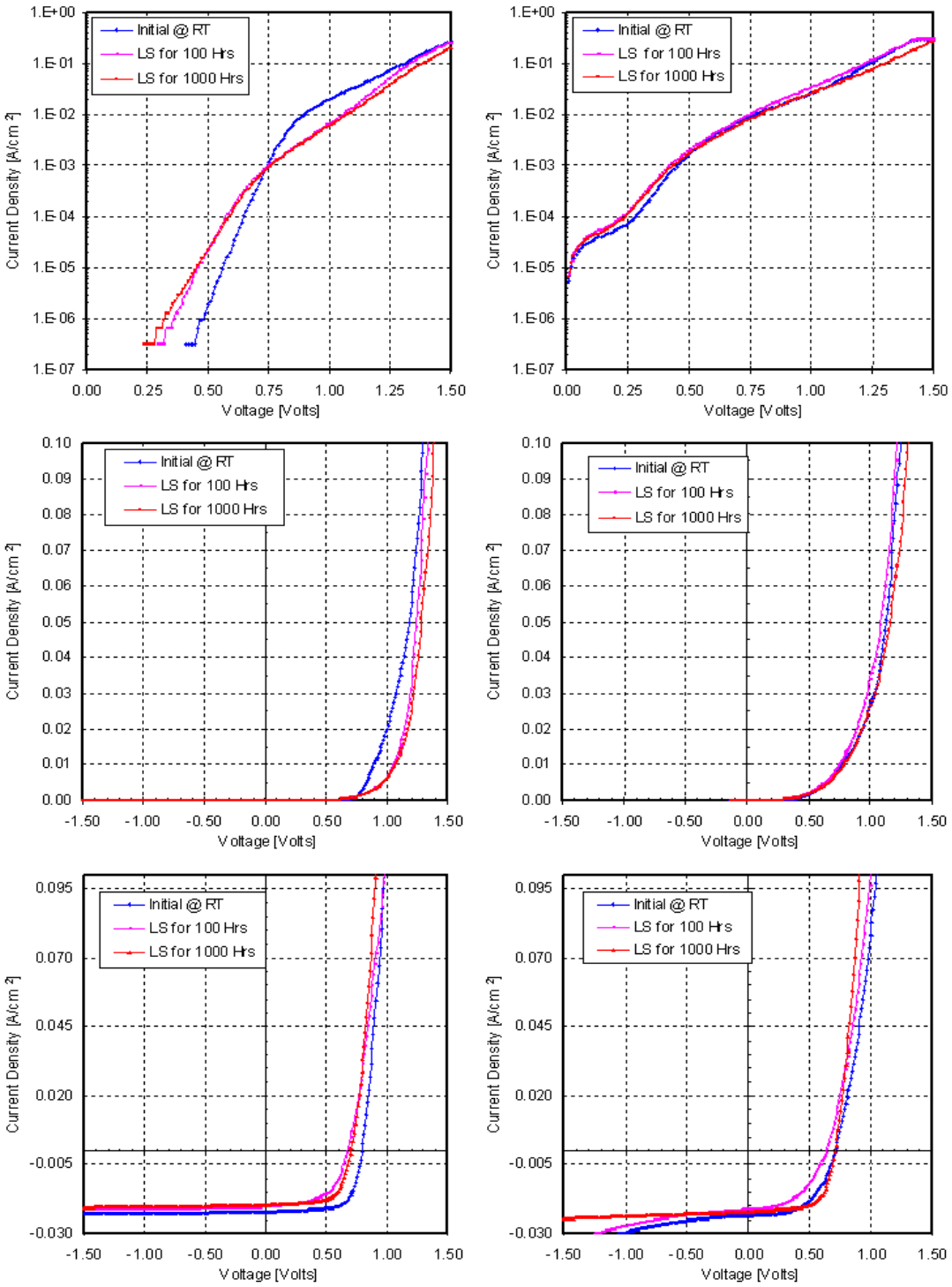

Figure B.8 JV Characteristics. HT at 380^oC and LS at SC

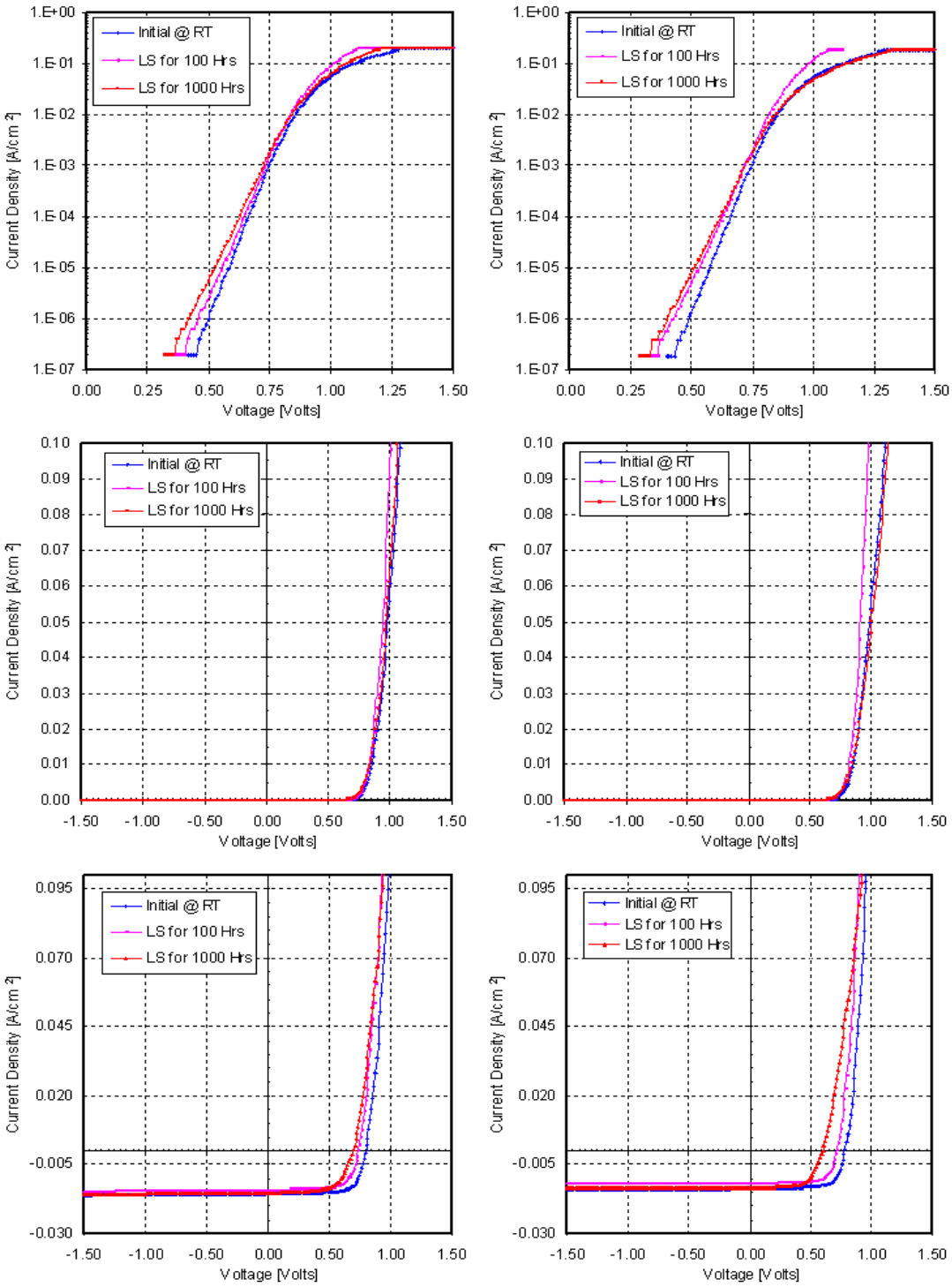

Figure B.9 JV Characteristics. HT at 390^oC and LS at OC

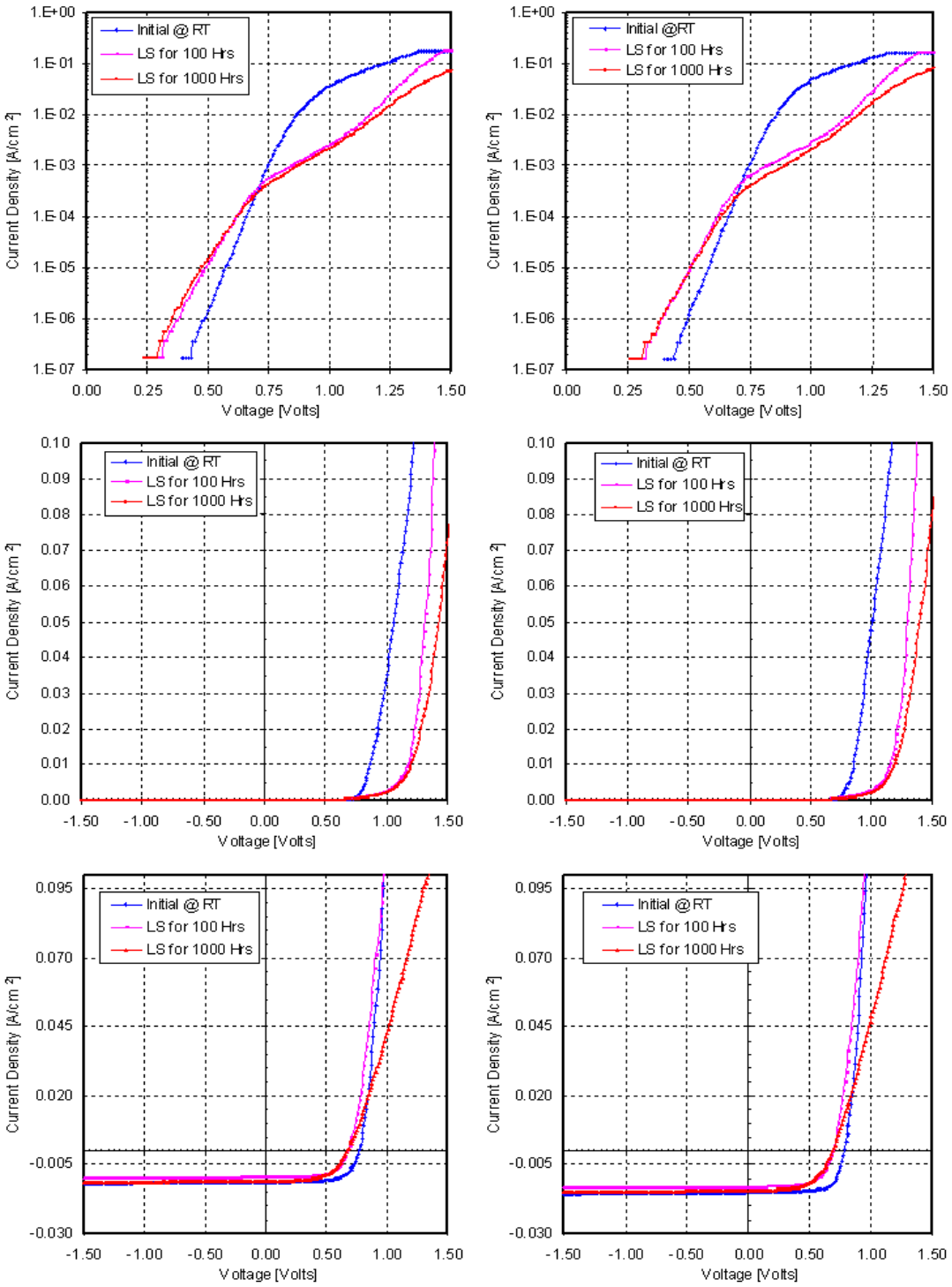

Figure B.10 JV Characteristics. HT at 390^oC and LS at SC