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Adaptive Digital Predistortion Linearizer for Power Amplifiers in Military UHF Satellite

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Adaptive Digital Predistortion Linearizer for

Power Amplifiers in Military UHF Satellite

By

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ADAPTIVE DIGITAL PREDISTORTION LINEARIZER FOR POWER AMPLIFIER IN MILITARY UHF SATELLITE

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ABSTRACT

The existing UHF Satellite Communications (SATCOM) transponders used for military applications use efficient, saturated power amplifiers, which provide one earth-coverage antenna beam. The amplifier is dedicated to small frequency band and only handles a few carriers simultaneously.

The communications capacity needed to support future military forces on the move will require satellite payload power amplifiers to support hundreds of channels simultaneously, with the channels spread over the entire military UHF SATCOM band. To meet the capacity requirements and simultaneously meet the out-of-band emission, power amplifiers will have to be highly linear. The high-efficiency, ultra-linear power amplifier architecture proposed to support the requirements can only be met by use of linearity improvement techniques.

The literature search revealed many power amplifier linearity improvement techniques. Each technique was reviewed to determine its suitability for the proposed power amplifier architecture.

The adaptive digital predistortion technique was found to be the most suitable in terms of bandwidth, correction achievable, and complication.

A discussion on common linearization techniques is presented, followed by analysis of the adaptive digital predistortion technique. A SIMULINK simulation model of an adaptive digital predistorter was developed. The simulation results show that adaptive digital predistortion was able to significantly reduce the Inter-Modulation Distortion (IMD) terms generated by a memory-less power amplifier operating in the 240 MHz to 270 MHz range. An actual hardware implementation of adaptive digital predistorter was constructed and the test results show that there was a large reduction in IMD terms generated by a memory-less power amplifier. In the contrary, the results show there is only moderate improvement in IMD performance if the power amplifier has memory. The electrical memory in the power amplifier with memory was minimized, but this resulted only a modest improvement in the IMD performance. Therefore, it was concluded the majority of the memory effect was due to thermal memory.

1.0 INTRODUCTION

1.1 Background

The existing UHF Satellite Communications (SATCOM) transponders used by the US military use highly efficient, saturated power amplifiers, which provide one earth-coverage antenna beam. The amplifier is dedicated to small frequency band and only handles a few carriers simultaneously. The out-of-band inter-modulation distortion generated by the output of the saturated power amplifier is suppressed by the use of narrow, band-pass filters (see Figure 1.1). This approach can support up to 39 channels through a single earth coverage antenna.

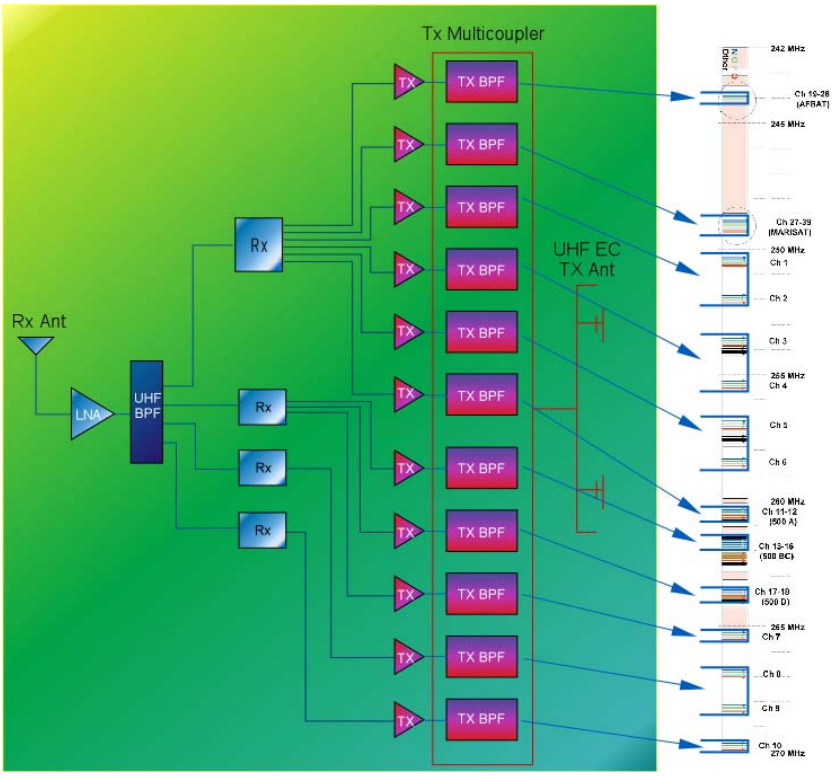

Figure 1.1 Conventional UHF Satellite Transponder Architecture

The communication capacity needed to support future military forces on the move will require satellite to support hundreds of channels simultaneously with the channels spread over the entire UHF satellite communications band. This capacity and the availability requirements for the next generation satellite can be met by providing multiple downlink beams, which can change direction and channel assignment within the beam. In the multi beam approach each beam can have few channels to hundreds of channels, occupying full downlink spectrum. The multi-beam system requires each power amplifier to operate over the full downlink band of 240 to 270 MHz [1].

1.2 Motivation and Research Objectives

In 1981, at bilateral coordination meeting between US and Russia, US agreed to limit the radiated power within the Russian satellite (VOLNA) bands which are interposed between the US military satellite bands as shown in Figure 1.2. The VOLNA treaty limits the inter-modulation distortion to –52 dB relative to full power in a single channel.
The next generation of satellite power amplifiers have to operate over the full downlink band, carry hundreds of channels simultaneously, generate out-of-band emissions level which do not require further filtering and meet the VOLNA emissions limits. Therefore, new power amplifiers have to be highly linear, thereby creating only minimal out-of-band energy when transmitting hundreds of channels simultaneously.

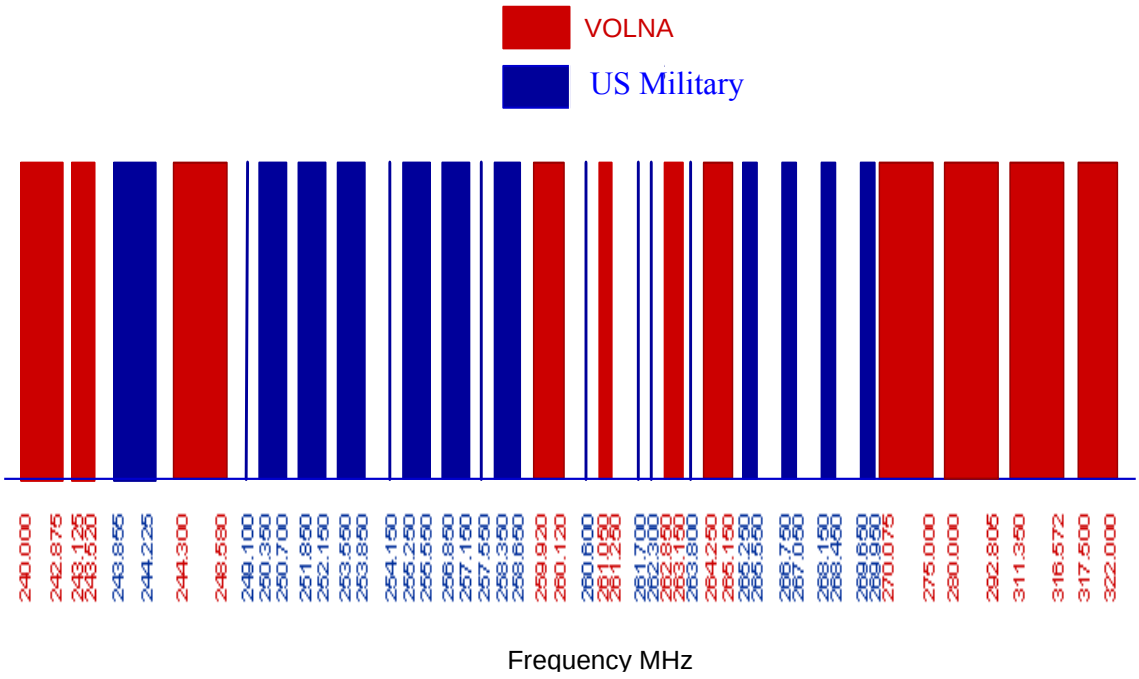

Figure 1.2 US Military SATCOM Downlink Bands and Russian VOLNA Bands

The conventional approach of moderately linear power amplifier followed by narrow band filters can be used to implement proposed architecture, but the system would be extremely complex and impractical for a satellite.
The size, weight and power restriction placed on the power amplifier because of satellite application, means that the strict out-of-band emissions limits can only be met with linearity improvements techniques [1].

The literature search revealed many power amplifier linearity improvement techniques. Each technique was evaluated to determine its suitability for the proposed power amplifier architecture. Adaptive digital predistortion technique was found to be the most suitable in terms of bandwidth, correction achievable and complication. SIMULINK model of adaptive digital predistortion was developed to evaluate sensitivity to parameter changes and determine the complexity of the adaptation scheme.
Hardware demonstration models were also built to show to the prospective users the viability of proposed power amplifier architecture.

1.3 Thesis Outline

This section serves as an introduction to the need for ultra linear power amplifier for the next generation of military satellites. Section 2.0 presents power amplifier characteristics followed by a review of different linearization techniques. Each technique was reviewed to determine its suitability for the proposed power amplifier architecture. The digital predistortion techniques are treated in more detail because of its suitability for the proposed power amplifier architecture. Section 3.0 details hardware demonstration model results for a non-adaptive digital predistorter. Section 4.0 details the simulation results for a adaptive digital predistorter and sensitivity analysis of predistorter to various parameter changes. Section 5.0 details results of actual hardware model built for adaptive digital predistorter for memory-less power amplifier. Also, the methods used to detect memory in power amplifiers and techniques used to overcome memory in power amplifiers are presented in this chapter. Section 6.0 presents possible adaptive digital predistorter architecture for a power amplifier with memory. Section 7.0 details conclusions reached and recommendations for future work.

2.0 POWER AMPLIFIER LINEARIZATION TECHNIQUES STUDY

2.1 Satellite Transmitter

The satellite transmitter section consists of channel filtering/limiter at Intermediate Frequency (IF) followed by an Up-Converter, which translates the filtered signal to desired carrier frequency. The power amplifier amplifies the signal to the required power level before being fed to the antenna

2.2 Power Amplifier Requirements

In addition to the operating bandwidth of 30 MHz, from 240 to 270 MHz and linearity requirement that generates Inter-modulation distortion (IMD) products of less then –52 dB in the VOLNA bands.
Another requirement is that the average power per amplifier would be 12 Watts with peak power of 120 Watts, with efficiency of approximately 20%. The input drive level of -16 dBm was selected for maximum power and –23 dBm drive level was chosen for minimum channel capacity.

2.3 Power Amplifier Characteristics

The three main classes of linear amplifiers are A, AB and B. Class A is the most linear

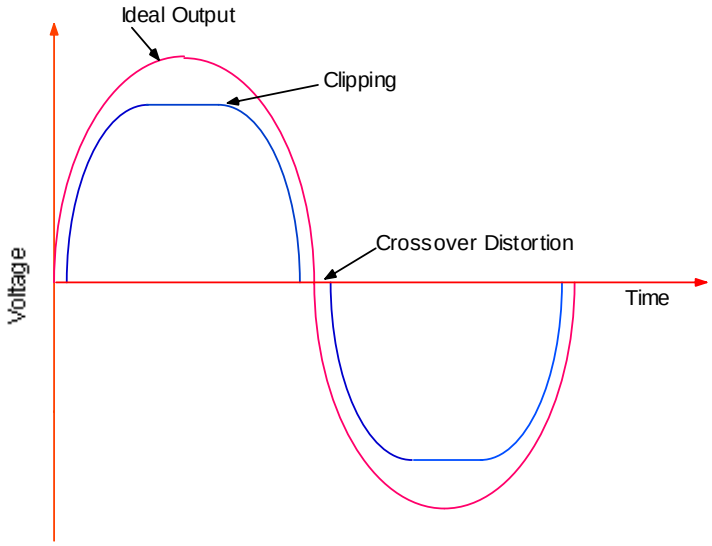

Figure 2.1 Power Amplifier Distortion Characteristics

and least efficient. The amplitude dependent characteristics of a power amplifier can split into three regions. The cut-off region is when the amplifier is not conducting, the linear region is where the amplifier starts conducting and signal amplification occurs, and finally the saturation region where the amplifier output starts to flatten (see Figure 2.1). The main characterizations of power amplifier are the second and third-order intercept point, 1 dB gain compression point and input back-off. Figure 2 illustrates, when the input is increased, the second harmonic will increase in proportion to square of the input signal and the third harmonic will increase in proportion to cube of the input signal. Thus, the second and the third harmonics will increase at a greater rate than that of the fundamental component. There comes a point where the harmonic components equal the fundamental. The signal level at which the second harmonic is equal to the fundamental is called the second order intercept point and the point at which the third harmonic is equal to the fundamental is called the third order intercept point.

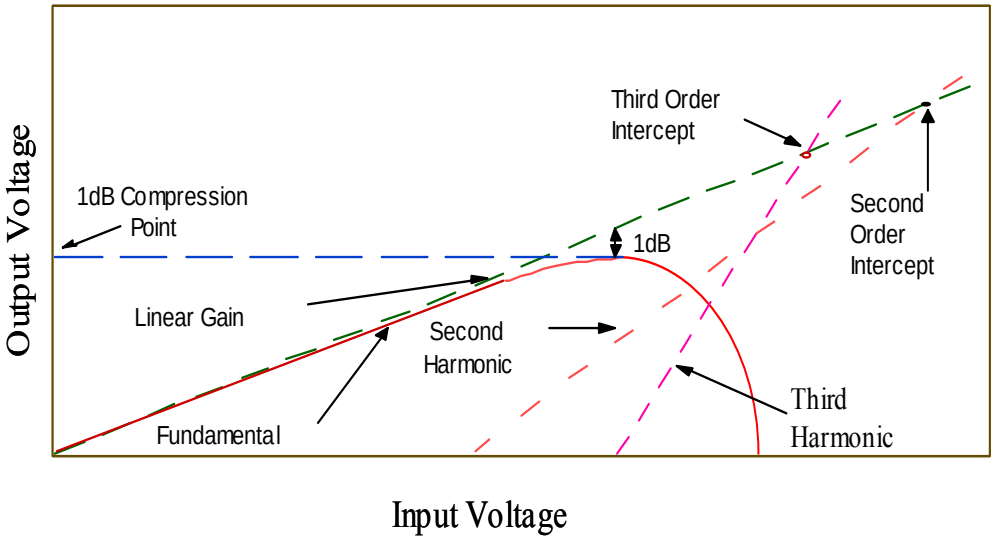

Figure 2.2 Illustration of Compression and Intercept Points

It is possible that this intercept point may be beyond the maximum output power of the amplifier. In this case, points are shown by dotted line to where intersection occurs. The intercept point indicates the linearity performance of the amplifier and is a fixed quantity from which the distortion level at a particular operating point may be predicated. The 1 dB compression point is defined as the point at which the output power level has dropped 1 dB below the ideal output power. Input back-off is defined as the ratio of the signal power measured at the input to the power amplifier to the input signal power that produces the maximum signal power at the amplifier's output.

2.3.1 AM-AM and AM-PM Conversion Effects in Power Amplifier

The nonlinear relationship between the input power and output power present in the power amplifier is referred to as AM-AM conversion. Another effect is conversion from

amplitude modulation on the input signal to phase modulation on the output signal. This is known as AM-PM conversion. Figure 2.3 shows the IMD terms generated by this two conversion effects [2].

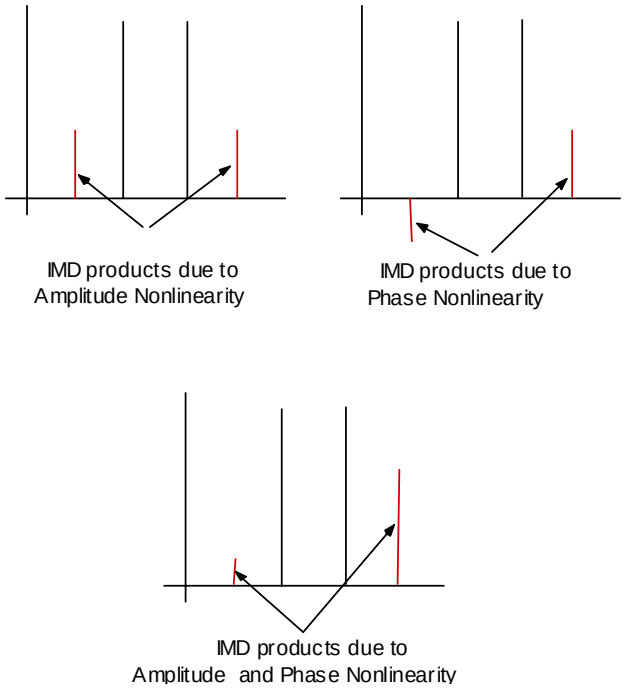

Figure 2.3 Illustrates IMD Products due to Conversion Effects [2]

The amplifier used in this design is nonlinear and assumed to be memory-less[4] i.e. the transfer function is not frequency dependent. Therefore, real-valued, nonlinear and memory-less function can be expanded into a power series as follows:

$$V_o(t) = a_0 + a_1 \cdot V_{in}(t) + a_2 \cdot V_{in}(t)^2 + a_3 \cdot V_{in}(t)^3 + a_4 \cdot V_{in}(t)^4 + a_5 \cdot V_{in}(t)^5 \quad (2.1)$$

2.4 Two Tone Test

A standard two-tone test is used to assess the amplitude and phase distortions present in a power amplifier. In the two-tone test the envelope of the input signal is varied throughout its complete range so the amplifier is tested over its whole transfer characteristics. Input signal is represented by:

$$V_in(t) = v \cos(\omega_1 t) + v \cos(\omega_2 t) \quad (2.2)$$

So the output voltage is

$$\begin{aligned} V_o(t) = {} & a_1 v[\cos(\omega_1 t) + \cos(\omega_2 t)] + a_2 v^2[\cos(\omega_1 t) + \cos(\omega_2 t)]^2 \\ & + a_3 v^3[\cos(\omega_1 t) + \cos(\omega_2 t)]^3 + a_4 v^4[\cos(\omega_1 t) + \cos(\omega_2 t)]^4 \\ & + a_5 v^5[\cos(\omega_1 t) + \cos(\omega_2 t)]^5 + a_6 v^6[\cos(\omega_1 t) + \cos(\omega_2 t)]^6 \\ & + a_7 v^7[\cos(\omega_1 t) + \cos(\omega_2 t)]^7 + \end{aligned} \qquad (2.3)$$

Each product term in equation 2.3, other than the fundamental generates number of distortion products. In general, the even order terms IMD terms will be well out-of-band of interest where as the odd order IMD terms may fall in-band (see Figure 2.4). It is understood that the IMD distortion causes major problems to a communication system as opposed to harmonic distortion. The harmonic distortion is far away from the fundamental signal and thus much easier to suppress by use of filters.

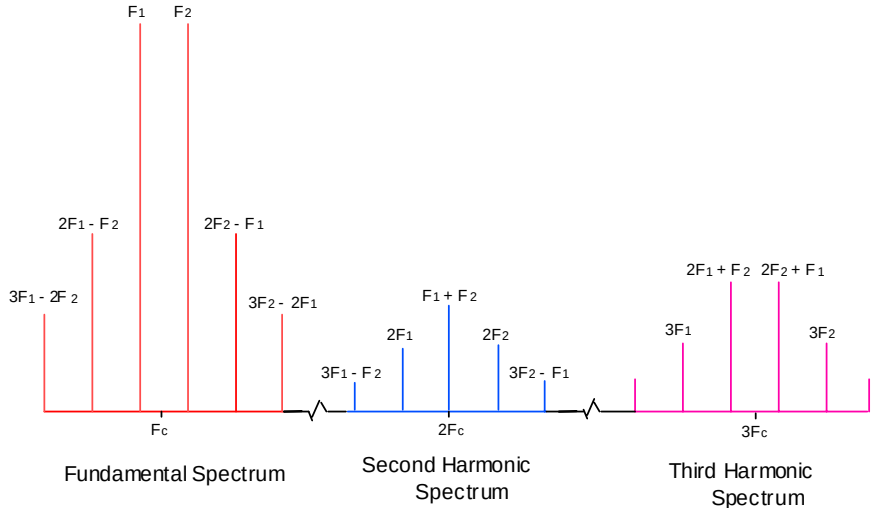

Figure 2.4 Illustration of Harmonic Distortion

2.5 Power Amplifier Technology

New device technologies that have been developed for cellular base stations and microwave communications satellites have been surveyed. The power amplifier built with these latest technology devices when subjected to the two-tone test revealed that IMD performance could be as good as –40 dB. Adding 6 dB (to account for multi-tone) and allowing 2 dB degradation (for multistage and environmental effects) shows that power amplifier linearization technique is required which provides at least 20 dB of correction to meet –52 dB IMD specification [1].

2.6 Power Amplifier Linearization Techniques

To obtain both linear amplification and high power efficiency, a linearizer is required. The linearizer allows the amplifier to be operated at much higher operating point since the distortion generated by the amplifier because of the peaks in input signals can be corrected up to the saturation level of the amplifier as shown in Figure 2.5. Any input signal which drives the amplifier to hard saturation, the resulting distortions cannot be

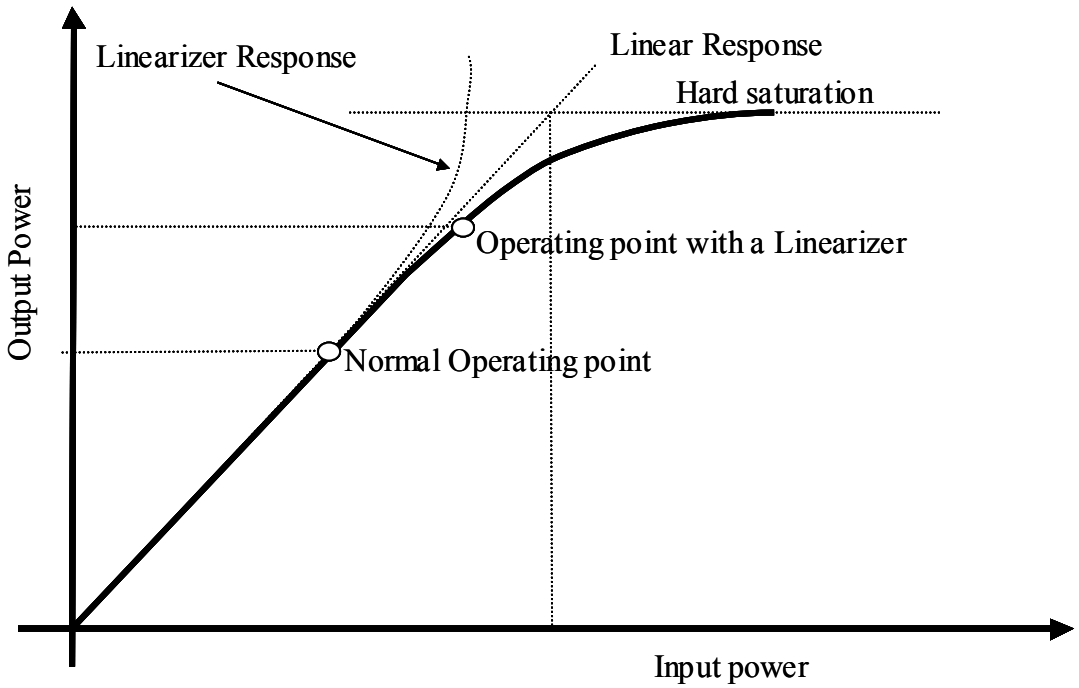

Figure 2.5 Illustration of Performance Improvement of a Power Amplifiers with a Linearizer

corrected since any increase in input power beyond this point will not result in an increase in output power. The linearization methods reported in the literature can be classified into Feedback, Feedforward, Predistortion and Digital Predistortion (Signal Processing).

2.6.1 Feedback Linearization Technique

The simplest method of reducing amplifier distortion is by some form of feedback. The Figure 2.6 illustrates the use of negative feedback around an amplifier with the effect of distortion n(t). G is the gain of the amplifier and K is the feedback attenuation.

$$\text{Output: } y(t) = G \cdot e(t) + n(t) \qquad (2.4)$$

Feedback: $f(t) = y(t)/K$ (2.5)

Error: $e(t) = x(t) - f(t)$ (2.6)

Therefore,

$$y(t) = K(G \cdot x(t) + n(t)) / (G + K) \quad (2.7)$$

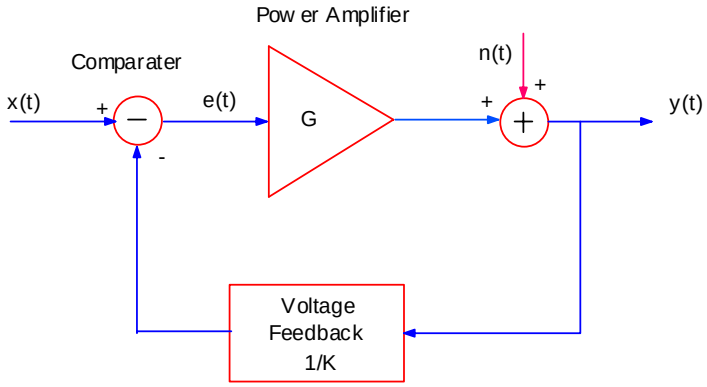

Figure 2.6 Illustration of Simple Feedback to Linearize Power Amplifiers

If the amplifier gain is much greater than the feedback ratio G>>K, then K + G approximates to G. So

$$y(t) = K \cdot x(t) + (K \cdot n(t))/G \quad (2.8)$$

Therefore, the distortion produced by the main amplifier is reduced by a factor K/G. The disadvantage of this approach is that the improvement in distortion performance is at the expense of the gain of the power amplifier and also feedback needs more bandwidth than signal.

2.6.2 Simple Envelope Feedback

Simple envelope feedback has matched envelope detectors coupled to the power amplifiers input and output ports. A differential amplifier forms amplitude error-correcting amplifier based on the detected envelope signals. The resulting error is used to control the gain of the amplifier. This technique has been widely employed to improve the IMD performance of VHF and UHF solid-state power amplifier in the mobile communication industry. The main draw back is that since this technique performs simple amplitude correction, it starts generation IMD products when the envelope operates in the compression region of the amplifier. The delays in the detection and signal processing can cause phase differences between AM and PM processes. This may

cause asymmetry IM side bands as discussed earlier and may substantially reduce any correction obtained by amplitude feedback process. The analysis has shown that that envelope correction does not provide correction over the operating bandwidth for this satellite application [1][5].

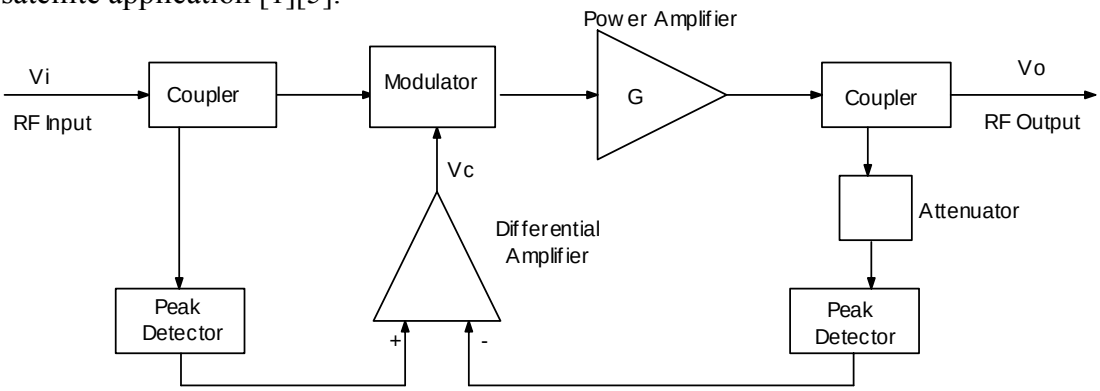

Figure 2.7 Illustration of Envelope Feedback to Linearize Power Amplifier

2.6.3 Polar Feedback

The polar feedback technique combines the envelope feedback with an additional feedback loop to account for phase shift variation through the power amplifier by dynamically adjusting the phase of the Radio Frequency (RF) input. The phase correction shown in Figure 2.8 uses a phased locked loop to maintain a constant phase shift over the amplifier's dynamic range. The two feedback loops are interdependent, any variation in the AM/AM loop, will produce phase as well as gain variation and similarly AM/PM will interact with the AM/AM loop if the insertion loss of the phase shifter varies. It has been reported in the literature that phase amplifier requires much higher bandwidth, which is a major limiting factor in the performance of the polar feedback [6].

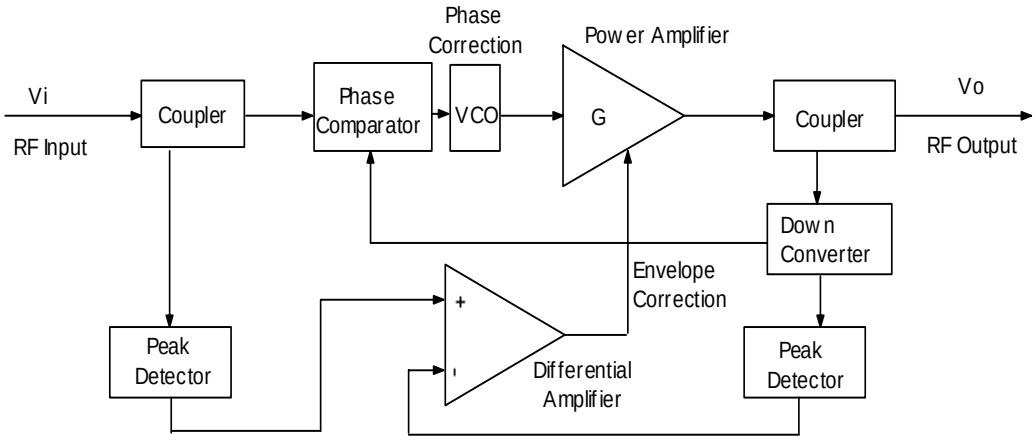

Figure 2.8 Illustration of Polar Feedback to Linearize Power Amplifier

2.6.4 Cartesian Feedback

The cartesian feedback is similar to polar feedback described previously, however, the baseband signal information is processed in I and Q form. Therefore the I and Q channels are well matched, eliminating the problems of different bandwidth and processing requirements for magnitude and phase paths as in polar feedback.

Figure 2.9 shows the cartesian feedback loop. The input signal is separated into I and Q and fed to differential amplifier where input signals is subtracted from the feedback signal. The error signal is upconverted to RF using a local oscillator and then combined to produce the complex RF, which is amplified by the power amplifier. The output of the power amplifier is sampled using a directional coupler and down converted and separated into I and Q using the same local oscillator used in up conversion process. The down convert output forms the feed back to the differential amplifiers. A phase shift network is required to ensure that the up and down conversion processes are correctly synchronized. The main advantages of cartesian over polar feedback is that a significant reduction in bandwidth requirement for the feedback loop allows more reduction of IMD and secondly simplicity of implementation.

The experimental results in the literature have shown that 10-30 dB of improvement in IMD performance is achievable, however the stability criteria limits the maximum bandwidth to a few megahertz. Also the linearizing bandwidth is 5-10 times larger than the channel bandwidth [7][8].

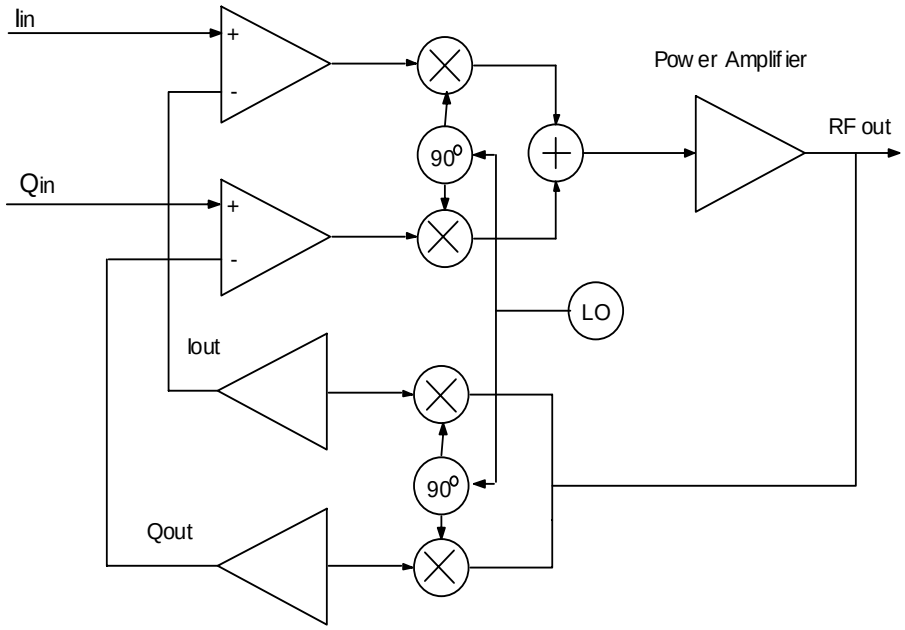

Figure 2.9 Illustration of Cartesian Feedback to Linearize Power Amplifier

2.6.5 LINC

Linear amplification with Nonlinear Components (LINC) is, different from all other techniques of linearization of power amplifier, because no feedback from the output of the power amplifier is used. The power amplifier can be highly non linear. The theory of operation is that the baseband processing accepts a gain and phase modulated input signal, and generate two wideband constant envelope phase modulated signals. These signals are up-converted through two well matched non linear amplifier chains and summed. The complex signal are generated such that all undesired out-of-band components are in exact anti-phase in the two amplifier chains and cancel at the output, while the wanted components are in phase and reinforced (see Figure 2.10).

The generation of two wideband constant envelope phase modulated signals $S_1(t)$ and $S_2(t)$ have to be accurate. The DSP technology allows $S_1(t)$ and $S_2(t)$ to be generated more accurately. Thus, the linearity performance of the technique is determined by the gain and phase match between the two amplifiers [9][10].

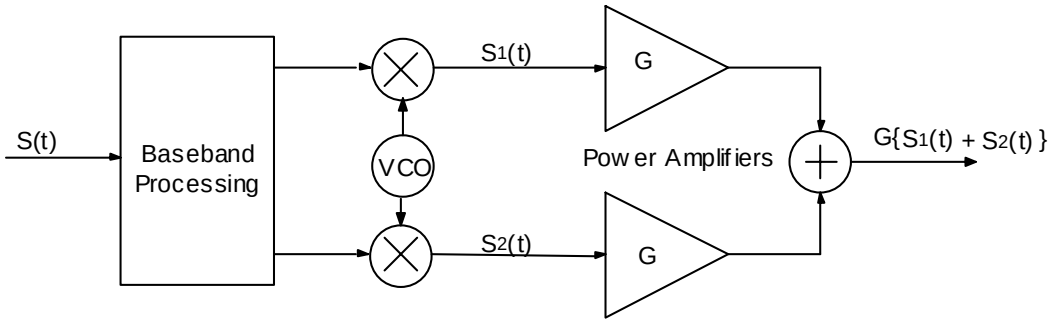

Figure 2.10 Illustration of LINC method to Linearize Power Amplifiers

The input signal S(t) is complex representation of bandlimited signal and can be written as

$$S(t) = r(t) \cdot e^{j\emptyset(t)};\ 0 < r(t) < r_{max} \qquad (2.9)$$

This signal can be split into two signals, $S_1(t)$ and $S_2(t)$, with modulated phase and constant amplitudes as described in [10]. This gives:

$$S_1(t) = S(t) - e(t)\ ;\ S_2(t) = S(t) + e(t);\ \text{ and } |S_1(t)| = |S_2(t)| = r_{max}\ ; \qquad (2.10)$$

Where e(t) is in quadrature to the source signals $S_1(t)$ and $S_2(t)$,

$$e(t) = j.S(t).\sqrt{\{\frac{r_{max}^{2}}{|S(t)|^{2}} - 1\}} \qquad (2.11)$$

The output is given by:

$$S_{out}(t) = G \cdot 2\,S(t); \qquad (2.12)$$

The quadrature signal e(t) is added to one leg of forward loop and subtracted from the other leg of forward loop to give a constant envelope signal as shown in Figure 2.11.
The main disadvantage with this approach is the generation of two constant envelope signals is complicated and additionally good power combining with low loss and high isolation is very difficult to achieve.

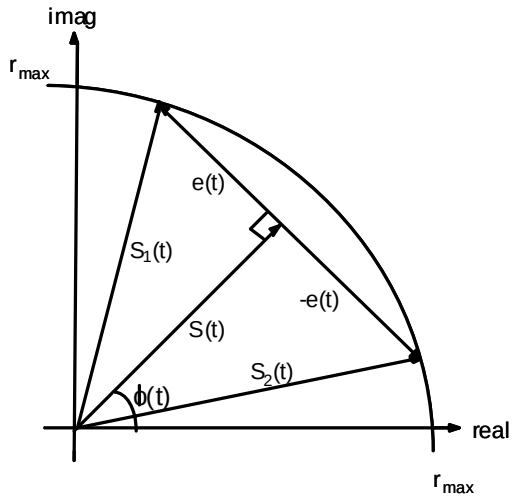

Figure 2.11 Illustration of Constant Envelope Signals

2.6.6 Combined Analog-Locked Loop Universal Modulator (CALLUM)

The Combined Analog Locked Loop Universal Modulator (CALLUM) is similar to the LINC technique where it combines two constant amplitude signals to form the output signal. CALLUM has two Voltage Controlled Oscillators (VCO) which generate separate phase modulated vectors of amplitude S and phase $Ø_1$ and $Ø_2$ as shown in Figure 2.12. The addition of these two vectors results in gain and phase modulated output vector (S_O, $Ø_o$) [11]. The main problem of CALLUM is stability which limits its use to narrowband applications.

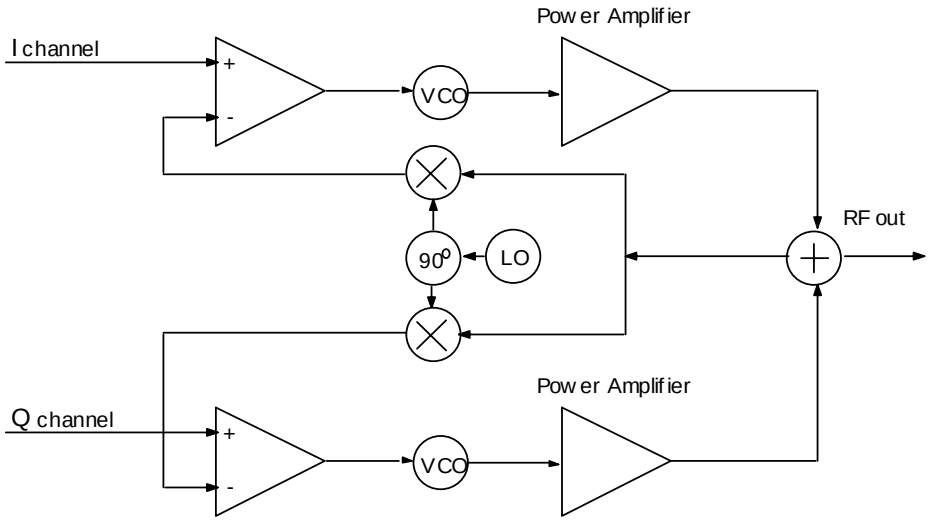

Figure 2.12 Illustration of CALLUM Feedback to Linearize Power Amplifier

2.6.7 Single Loop Feedforward

In the feedforward system the power amplifier is fed directly with the RF source signal. The delayed sample of the undistorted input RF signal is compared with an attenuated sample of the power amplifier output.

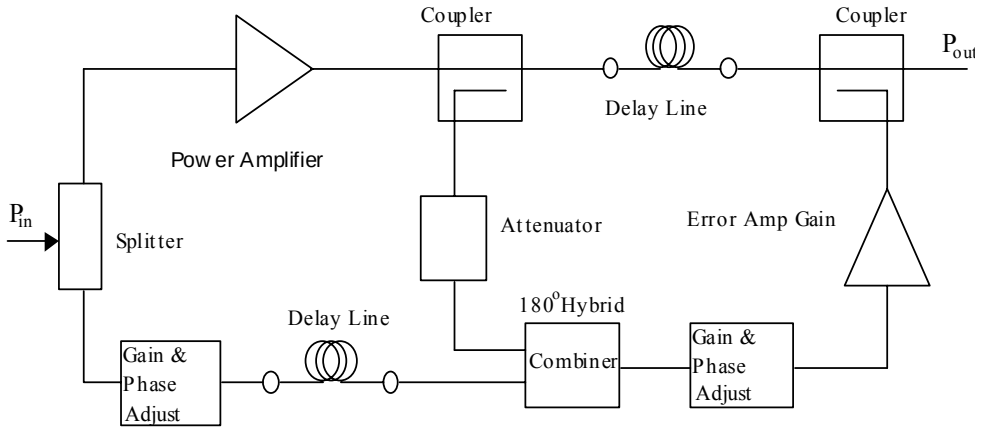

Figure 2.13 Illustration of Feedforward Technique to Linearize Power Amplifier

The error signal is then amplified linearly to the required level and is recombined with the output, following a delay line in the main signal path, which compensates for the delay in the error amplifier (see Figure 2.13). The error signal cancels the distortion present in the main path leaving an amplified version of the original signal.

The distortion generated by the power amplifier is cancelled in the feedforward loop by subtracting the source signal from the power amplifier output. The resulting error signal is subtracted from the amplifier output RF components. Additionally, it does not require a phase-locked loop to maintain phase correction.

The advantage of feedforward technique is the bandwidth is determined by frequency response of the couplers, delay lines, and phase shift components, which can be made to be very stable over a wide operating range [1][12]. The disadvantages are need for error amplifier which will be of a similar size as the main amplifier. Delay line in forward path needs to be rated for output power.

2.6.8 Muti-Stage Feedforward

In theory the feedforward loops can be nested as many times as necessary to obtain required level of correction. However this adds cost, complexity, weight and high power dissipation, is considered not practical of this satellite application.

2.6.9 Envelope Elimination and Restoration

The Envelope Elimination and Restoration (EER) technique to linearize the power amplifier was first proposed by Khan [13] to improve short-wave broadcast transmitter. The EER has an envelope detector, which extracts the magnitude information and limiter, which eliminates RF envelope and generates a constant amplitude phase signal (See Figure 14). The magnitude and phase signal are amplified, with the delay path of two signal matched. The magnitude and phase are then recombined using switch-mode power amplifier. The experimental results have shown that EER provides greater than 28 dB of linear output power with 33-49% efficiency. This method was not suitable since it would require the switching power converter to modulate its output at rates above 27 MHz [14].

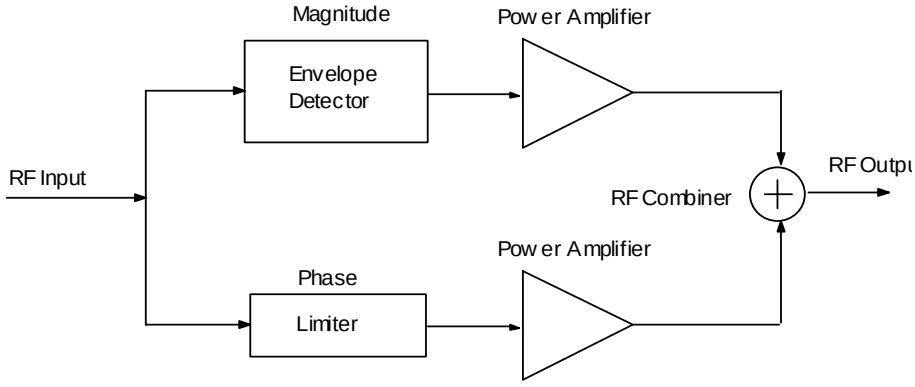

Figure 2.14 Illustration of EER Technique to Linearize the Power Amplifier

2.6.10 RF/IF Predistortion

Predistortion technique in its simplest form consists a predistorter of preceding the nonlinear power amplifier which has the inverse transfer characteristics of the power amplifier. Figure 2.15 shows predistortion in its simplest form. It is an open loop system. However, most solutions presented in literature have some kind of feedback to enable adaptation of the predistorter.

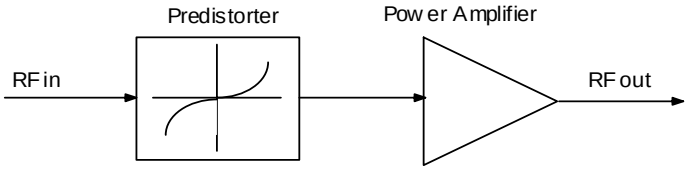

Figure 2.15 Illustration of simple Predistortion Technique to Linearize Power Amplifier

A large number of predistortion networks have been reported in the literature. Some networks use non-linear devices to input, while other networks curve-fit the distortion characteristics of the power amplifier. An example of RF predistorter is Cubic predistorter, which eliminates the third order distortion by generating a correctly phased addition of a cubic component to the input signal to the power amplifier. The advantage of the RF predistorter is its ability to linearize the entire bandwidth of the power amplifier, while the advantage of IF predistorter is that same design can be used for range of carrier frequencies by altering the Local Oscillator (LO) frequency.

2.6.11 Digital Predistortion

The digital predistortion method uses digital processing to synthesize the inverse transfer characteristic of a power amplifier. The digital predistortion is generally performed at baseband. The distorted baseband signal is translated to a convenient intermediate frequency (IF) and then the RF signal is generated by mixing the IF with a LO. An alternative to generating IF frequency is a direct conversion to RF signal using an Analog Quadrature Modulator (AQM).

The digital predistortion parameters are stored in a look-up table or register table which can be updated with adaptive feedback. The predistortion scheme works on the orthogonal I and Q components of the input and the feedback signals, thus providing both amplitude and phase correction (see Figure 2.16). Furthermore, since the power amplifier's non-linearity is a function of power, frequency, temperature and aging the look-up tables must updated continuously, otherwise there will be a degradation in IMD

performance and these appear as interferers in the adjacent channels. The main advantages of this approach is that the correction is applied before the power amplifier where insertion loss is less critical and significant IMD reduction is achieved over a wide signal bandwidth.

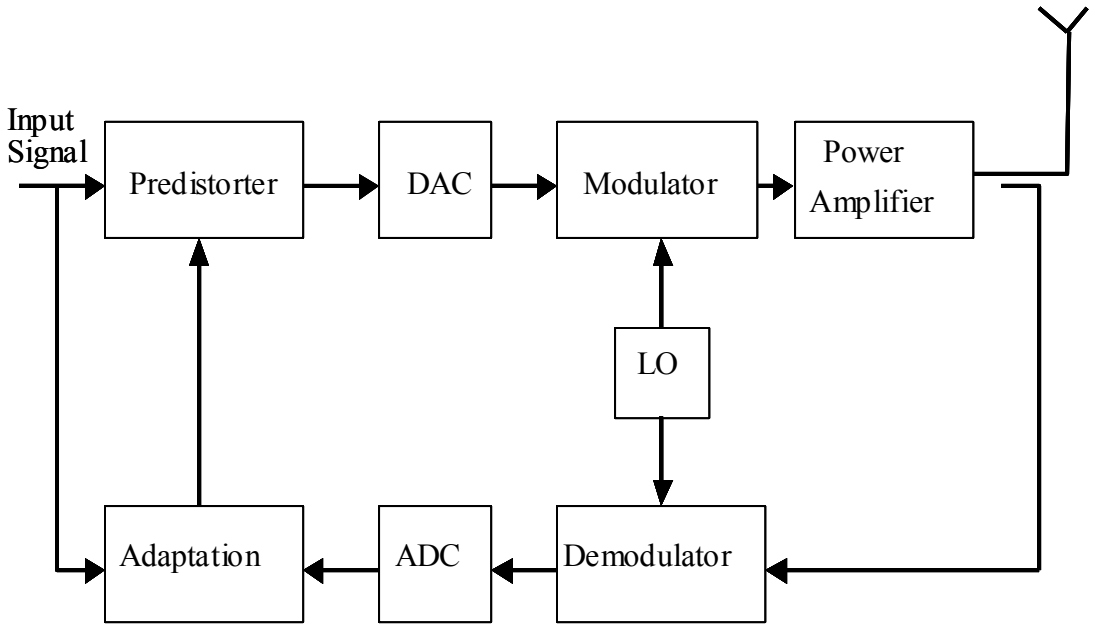

Figure 2.16 Digital Predistortion

2.7 Selection of Linearizer Topology for Power Amplifier

The literature search shows that from all the linearization techniques that have been developed, the predistortion is the most commonly used in the new systems today. The digital predistortion technique is moderately complex, offers good IMD reduction over a wide signal bandwidth and automatic adaptation maintains performance regardless of variation in power supply, frequency, temperature and component aging.

The SIMULINK model developed for adaptive digital predistorter showed large improvement in IMD performance, which is discussed in section 4.0. The simulation results for adaptive digital predistorter are consistent with literature search which also shows several authors reporting greater than 20 dB improvement in IMD performance over a wide signal bandwidth [25-27]. Additionally, the size, weight, power and IMD performance analysis performed for multi-beam power amplifier architecture showed that only adaptive digital predistortion technique can satisfy all these requirements [1]. The next section initially discusses one of the first powerful digital predistorter, the mapping predistorter. This is followed by a detailed analysis of the gain based adaptive digital predistorter, which is the subject for this thesis research.

2.7.1 Mapping Predistorter

Mapping predistorter was the first powerful digital predistorter based on a look-up table method, reported by Nagata [15](see Figure 2.17). In this method all the combination of complex input ($V_{\mathrm{mod}}(t)$) are mapped to unique location to provide a predistorted output ($V_{pd}(t)$). The sum of $V_{\mathrm{mod}}(t)$ and $V_{pd}(t)$ generates an inverse characteristics of the power amplifier, thereby canceling the distortion at power amplifier output.
The amplifier input can be written as:

$$V_a(t) = \{V_{\mathrm{mod}}(t) + V_{pd}(t)\}\ e^{jw_0 t}, \tag{2.13}$$

Where w_0 is the RF input to the PA translated by LO frequency and the look-up table output is,

$$\mathrm{Re}(V_{pd}) = F_I\{\mathrm{Re}(V_{\mathrm{mod}}), \mathrm{Imag}(V_{\mathrm{mod}})\} \tag{2.14}$$

$$\mathrm{Imag}(V_{pd}) = F_Q\{\mathrm{Re}(V_{\mathrm{mod}}), \mathrm{Imag}(V_{\mathrm{mod}})\} \tag{2.15}$$

Therefore the look-up table is two-dimensional.
The transfer function of predistorting signal can be written as:

$$G.(V_{\mathrm{mod}}(t)).\ e^{jw_0 t} = F\{V_{\mathrm{mod}}(t) + V_{pd}(t)\}\, e^{jw_0 t} \tag{2.16}$$

Where G is amplifier gain and $F\{V_{\mathrm{mod}}(t)) + V_{pd}(t)\}\ e^{jw_0 t}$ is the nonlinear gain and phase characteristic of the power amplifier.

The look-up table entries require updating when the ($V_{pd}(t)$) does not satisfy equation 2.16. The output of the power amplifier is demodulated and feedback as baseband complex signal.($V_{fb}(t)$). The delayed version of the reference signal $V_{\mathrm{mod}}(t)$ is compared with $V_{fb}(t)$ and the error is multiplied with an adaptation constant (a) and the result is used to iteratively update the predistorter look-up table to reduce the error to zero as per equations 2.17 and 2.18.

$$V_{err} = V_{\mathrm{mod}} - V_{fb} \tag{2.17}$$

$$V_e = a\,.V_{err} \tag{2.18}$$

$$V_a = V_{pd} + V_{\mathrm{mod}} \tag{2.19}$$

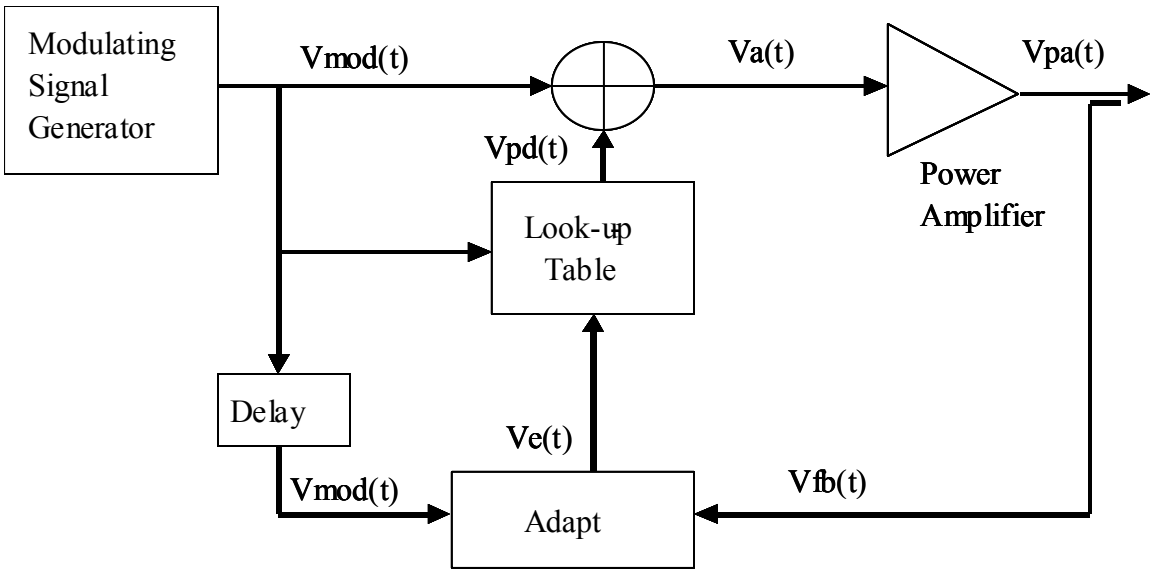

Figure 2.17 Mapping Predistorter

V_{mod} in the equation 2.17 is delayed by the same amount as the delay in the feedback path. Therefore there is no delay between V_{mod} and V_{fb}. Nagata also provides an update algorithm for update of table and a delay compensation see [15]. The drawback of mapping predistorter is that it requires a very large look-up table (size = $2x(2^n)^2$) and phase shifter in the feedback path for stability in the adaptation update. Also, the phase shifter requires readjustment when switching to a new channel.

2.7.2 Complex Gain Based Predistorter

Complex gain based predistorter is illustrated by Figure 2.18 and uses a two, one dimensional look-up tables and is based on the concept of maintaining constant loop gain at all power levels. This is achieved by addressing the look-up table with the magnitude of the input complex envelope to obtain complex gain scale factor stored in the LUT. The input signal is the multiplied with the complex gain to obtain a predistorted output which is the inverse of the power amplifier.

The complex envelope of the input (V_a) and the output (V_{pa}) of the power amplifier are related by

$$V_{pa} = V_a \cdot G(|V_a|^2) \qquad (2.20)$$

$G(|V_a|^2)$ is the complex gain of the amplifier, and represents its AM/AM and AM/PM characteristics and V_a is the predistorted signal [16].

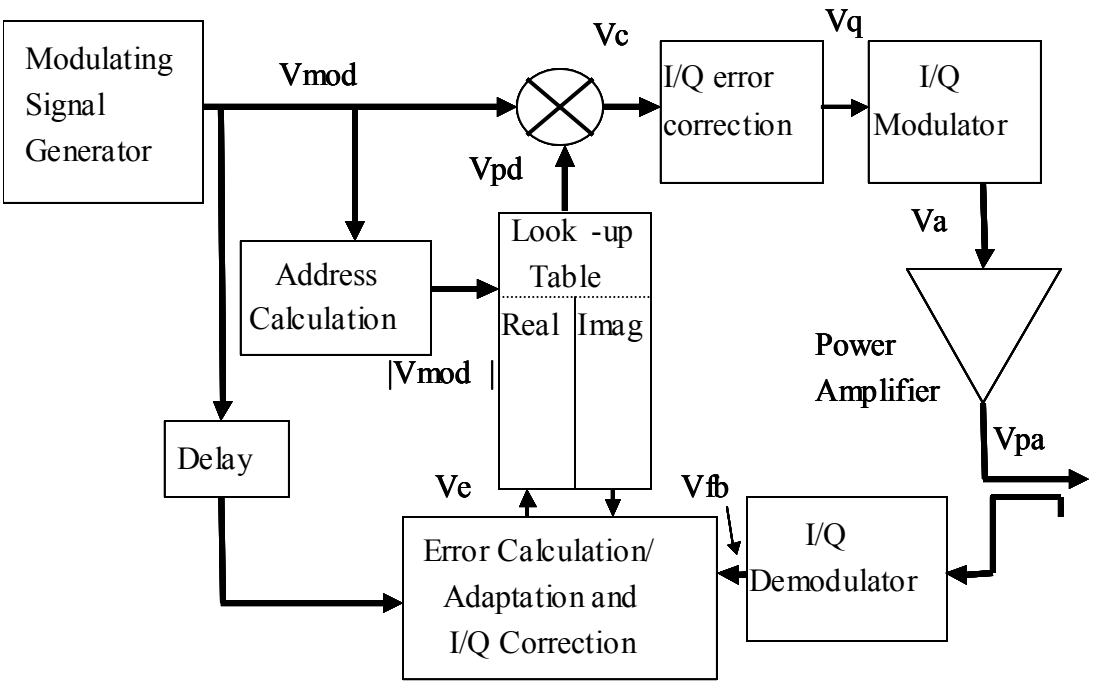

Figure 2.18 Illustration of Complex Gain based Predistorter

The IQ table contains complex gain factors (see Figure 2.16) represented as,

$$V_e = \mathrm{F}\{\mathrm{Re}(V_e), \mathrm{Im}(V_e)\} \tag{2.21}$$

The gain function from the look-up table is multiplied with modulated input signal. The resulting complex quantity is based on the envelope of the input signal is represented by,

$$V_c\ (\mathrm{t}) = V_{\mathrm{mod}}\ (\mathrm{t}) \cdot \mathrm{F}\{|V_{\mathrm{mod}}\ (\mathrm{t})|^2\} \tag{2.22}$$

2.7.2.1 Predistorter Table

The gain-based predistorter only requires two one-dimensional look up table since most power amplifier suffer from distortion caused by amplitude variations. The table can be based on I/Q representation or polar coordinates. Both approaches require additional signal processing to perform complex multiply. The polar co-ordinate table also requires polar/rectangular conversions.

The gain function from the look-up table is multiplied with modulated input signal. The resulting complex quantity is based on the envelope of the input signal and is represented by equation 2.22 where F{|Vmod(t)|²} represents the inverse transfer characteristics of the power amplifier.

Also,

$$V_c\ (t)\ = V_{\text{mod}}\ (t) \cdot V_{pd}\ (t) \tag{2.23}$$

The polar table approach (see Figure 2.19.) consists of two one-dimensional tables, one containing amplitude gain error and the other table containing phase rotation error.
The polar table can be represented as follows:

$$V_e = \text{F}\{\text{R}(V_e), Ø(V_e)\} \tag{2.24}$$

The amplitude part corrects for AM/AM distortion, represented below

$$|V_e\ (t)| = \text{gain error} \tag{2.25}$$

The phase table corrects for AM/PM distortion and represented below:

$$\angle V_e(t)\ = \text{phase error} \tag{2.26}$$

The output from the polar table is converted back to IQ representation to a add sight variation from the standard approach in literature where polar table output is used to predistort the modulating input signal.

Therefore, the gain function obtained after polar to rectangular conversion from polar tables is identical to the gain function in IQ representation look-up table. This gain function is multiplied with modulated input signal. The resulting complex quantity is based on the envelope of the input signal is represented by equation 2.22.

Assuming a perfect modulator $V_c = V_a$, then for both table approaches we can write,

$$V_a\ (t) = V_{\text{mod}}\ (t) \cdot V_{pd}\ (t) \tag{2.27}$$

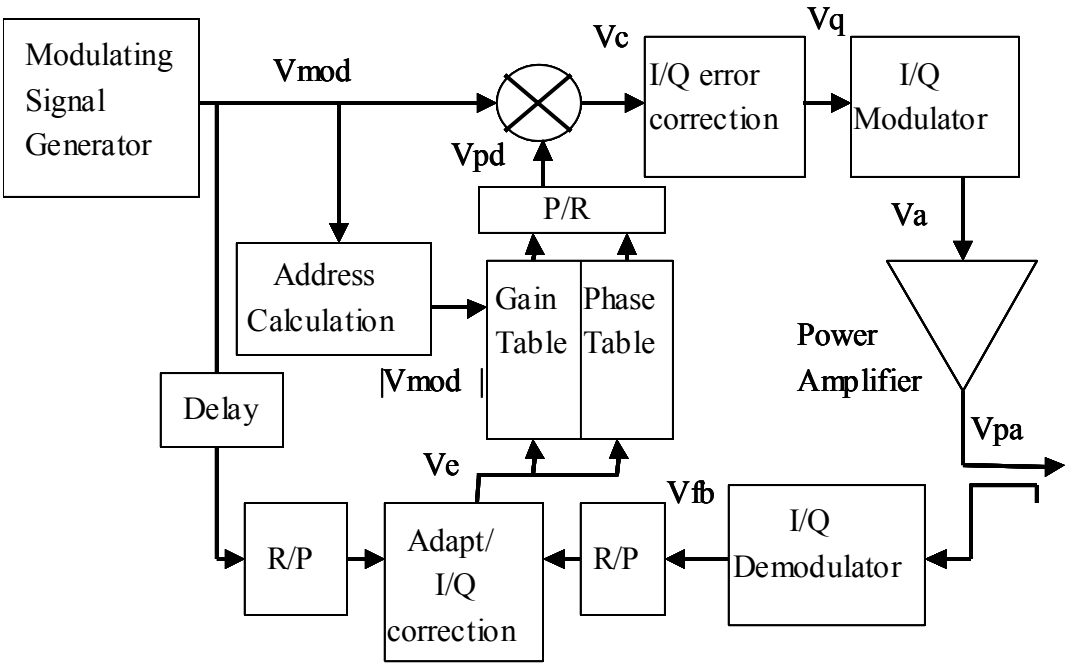

Figure 2.19 Illustration of Complex Gain based Predistorter-Polar Tables

2.7.2.2 Table Addressing

The look table for both methods is addressed by the magnitude of the source signal so the error is distributed throughout the table, so more accurate predistortion output is obtained at all power levels. However, since magnitude squared is easier to calculate, this may also be used to address the table, but this concentrates the entries to high amplitudes thus making low amplitude coarse. This may be acceptable since majority of distortion is caused when the amplifier is operated close to the compression region.
The magnitude calculation of the input signal is given by,

$$\sqrt{|V\bmod|} = \sqrt{real(V\bmod)^2 + imag(V\bmod)^2} \qquad (2.28)$$

The calculation of equation 2.28 is the most time consuming operation of the algorithm compared to the other operations in the predistorter. It has been reported that the accuracy of square function is not critical since it lead to about 2 dB of adjacent channel degradation when a table based square root function is employed this reduces the burden on Digital Signal Processor (DSP) and also reduces the adaptation time. A table-based square root is shown in Figure 2.20 [18]. The table method employ two small look-up tables, one containing $\sqrt{Y_i}$ and the other containing $\sqrt{Y_{i+1}} - \sqrt{Y_i}$ addressed by the integer part of $I^2 + Q^2$ address. The $\sqrt{Y_i}$ table gives an absolute square root value for an integer

point and the $\sqrt{Y_{i+1}} - \sqrt{Y_i}$ table gives difference of a square root value between a integer point and its neighbor. The difference square root table value is multiplied by the fractional part of the integer point, thus giving a weighted version of the difference table output. The absolute square root value and weighted difference table output are added to give an approximate square root value of I/Q input. The result is used to address the complex gain look-up table. The nine entry square root table was shown to be adequate [19].

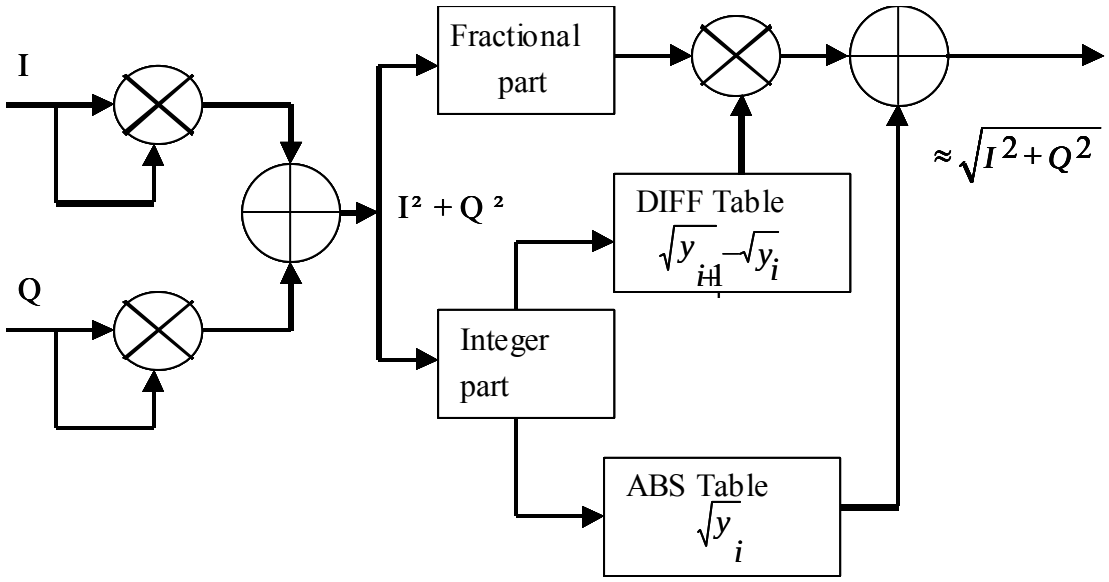

Figure 2.20 Look-Up Table Address Calculation

2.7.2.3 Table Adaptation

The two methods of the look-up table operation in both access and update are the continuous update and block update. In continuous look-up table update method, the input ($V_{\mathrm{mod}}(t)$) is delayed to align with feedback ($V_{fb}(t)$) from the power amplifier and the resulting difference $V_{err}(t)$ which should only contain the distortion is computed on sample by sample basis.

In block update, a block of data of input ($V_{\mathrm{mod}}(t)$) and feedback ($V_{fb}(t)$) are captured and the DSP is used to align the two signals using cross-correlation, followed by taking the difference ($V_{err}(t)$) of the two signal which should only contain the distortion. The block processing is performed at a fixed time interval.

$$V_{err}\ (\mathrm{t}) = V_{\mathrm{mod}}\ (\mathrm{t}) - V_{fb}\ (\mathrm{t}) \qquad (2.29)$$

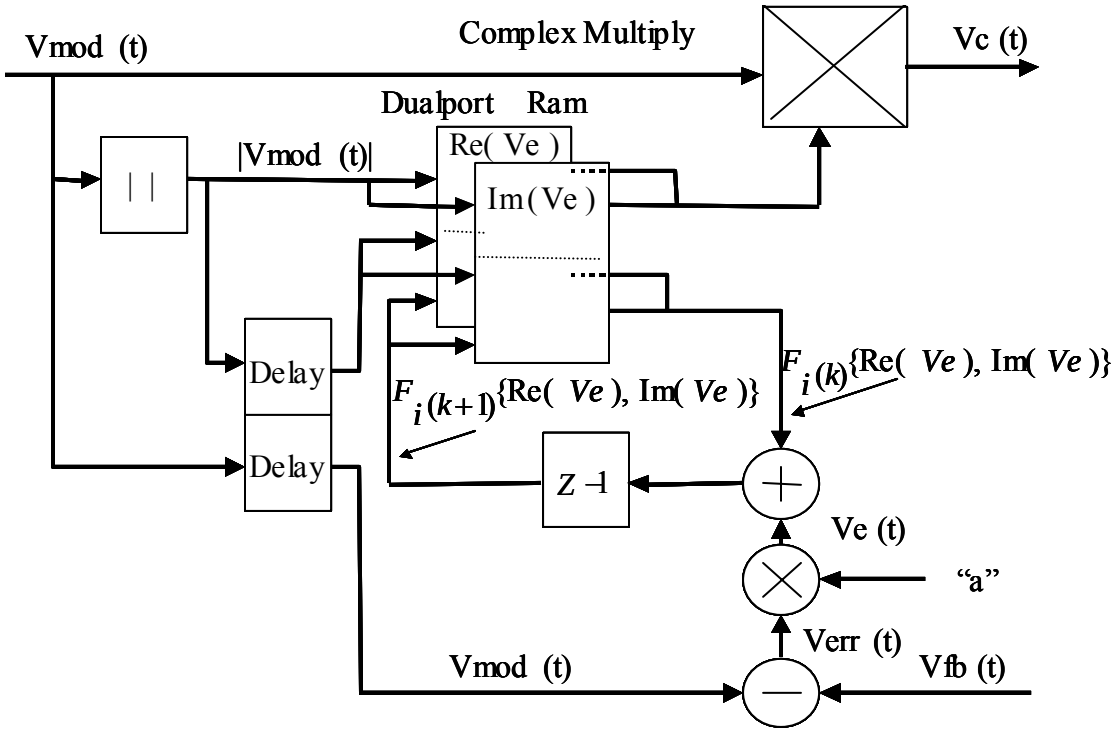

Figure 2.21 Linear Convergence –I/Q Table

There are various techniques described in the literature for adaptation of look-up table entries, such as linear convergence, secant method, rotate and scale, and steepest decent method. The method of adaptation selected will determine speed of convergence, stability of the system, and computation load on the DSP.

The linear convergence is based on classical feedback theory, and it is computationally simplest and the least stable for adaptation look-up table entries. The error (V_{err}(t)) in linear convergence is modified by the adaptation constant "a" and resulting V_e(t) is summed with the previous entry in the table $F_{i(k)}\{\mathrm{Re}(V_e), \mathrm{Im}(V_e)\}$. The new entry in the table is $F_{i(k+1)}\{\mathrm{Re}(V_e), \mathrm{Im}(V_e)\}$ and is stored at the magnitude envelope address of V_{mod}(t) (see Figure 2.21). This iteration update occurs every time the modulating signal envelope passes through a given table entry. The subscript "i" represents a specific entry in the table and k represents the kth iteration. The adaptation constant "a" is generally selected to be less than unity and controls the rate of convergence. If the adaptation constant "a" is large then their exists a possibility that the table entries will not converge, but oscillate and result in an unstable system.

In principles of secant adaptation method is based on a straight line approximation. For a given function f(x), the secant convergence algorithm is depicted by a geometrical representation in Figure 2.22. The function *f*(*x*) is being approximated by a straight line *"be"* which is an extrapolation based on the two points x_i and $x_{i-1.}$ The line passing through the x-axis at x_{i+1} gives the new value. Figure also shows that the secant line *"be"* deviates from the ideal line *"jk"* resulting in a small error.

It can be seen that the triangles *"abe"* and "dce" are similar. Therefore,

$$\frac{\text{ab}}{\text{ae}} = \frac{\text{dc}}{\text{de}} \tag{2.30}$$

$$\frac{f(x_i)}{x_i - x_{i+1}} = \frac{f(x_{i-1})}{x_{i-1} - x_{i+1}} \tag{2.31}$$

Rearranging equation 2.31, the new value is given by,

$$x_{i+1} = x_i - \frac{f(x_i)(x_i - x_{i-1})}{f(x_i) - f(x_{i-1})} \tag{2.32}$$

Applying the secant method of convergence for adaptation of look-up table entries is given by the following equation,

$$F_i(k+1) = \frac{F_i(k-1)e_g(F(k)) - F_i(k)e_g(F(k-1))}{e_g(F(k)) - e_g(F_i(k-1))} \tag{2.33}$$

where $F_i(k)$ is the kth iteration of look-up table entry i and e_g is the quantization error at the PA output. For detailed derivation of equation 2.33 refer to [16].

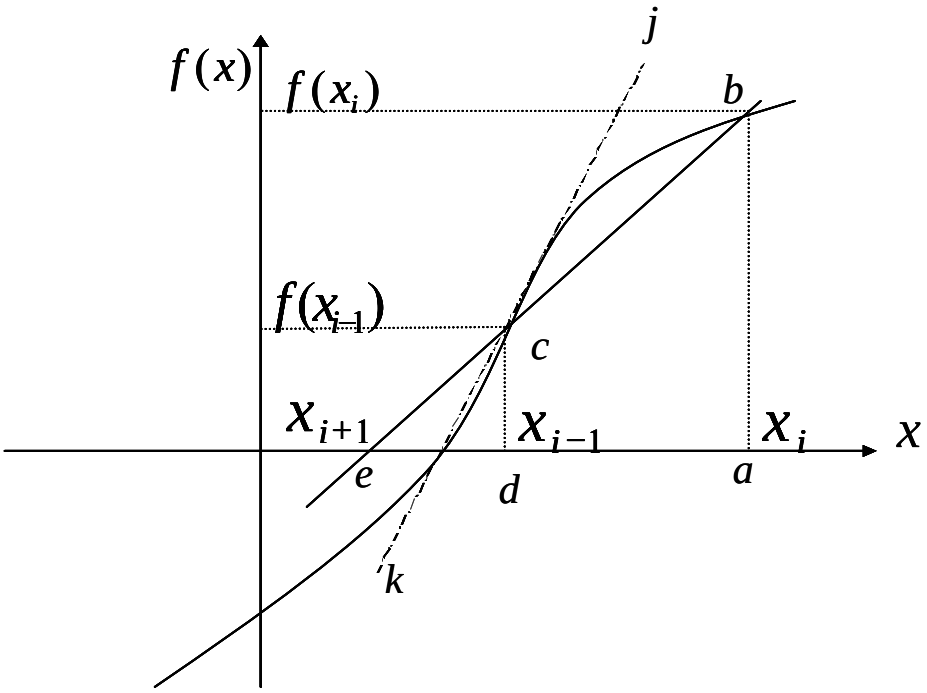

Figure 2.22 Secant Method

The rotate and scale method of adaptation is used for polar tables and is similar to the linear convergence method described above. The equation 2.29 is rearranged to give gain (scale) and phase (rotate) error,

$$|V_{err}\ (\mathrm{t})| = |V_{\mathrm{mod}}\ (\mathrm{t})| - |V_{fb}\ (\mathrm{t})| \tag{2.34}$$

$$\angle V_{err}(t) = \angle V_{\mathrm{mod}}(t) - \angle V_{f\,b}(t) \tag{2.35}$$

The gain and phase look-up table entry update at kth iteration is given by

$$F_{i\,(k+1)}\{Gain(V_e)\} = F_{i\,(k)}\{\mathrm{Gain}(\mathrm{V_e})\} + a\,|\,\mathrm{V_{err}}\,| \tag{2.36}$$

$$F_{i\,(k+1)}\{Phase(V_e)\} = F_{i\,(k)}\{\mathrm{Phase}(\mathrm{V_e})\} + a\angle V_{err} \tag{2.37}$$

Since the table size is small, the envelope address is unlikely to directly fall on a table entry, therefore either a linear interpolation between the table entries of adjacent address may be required or a larger size look-up table to improve the IMD performance.

2.7.2.4 Delay Adjustment Estimation

The propagation delays in transmit and receive path results (see Figure 2.23) in the sampled feedback signal $V_f(n)$ being of later time interval then the input complex signal $V_{\text{mod}}(n)$. This delay has to be accurately computed so the time aligned V_f (n) and $V_{\text{mod}}(n)$ can be compared to generate the error vector $V_e(n)$. If the delay is not computed accurately, then the adapation tables will have noise distortion component in the tables resulting in a less accurate inverse table. Therefore the distortion products generated by the power amplifier will not be cancelled resulting in a non optimal IMD correction. A simple method for compensation of delay in feedback sample $V_f(n)$ is to delay the input sample $V_{\text{mod}}(n)$ by the required number of samples before a comparison is made between the input and the feedback samples.

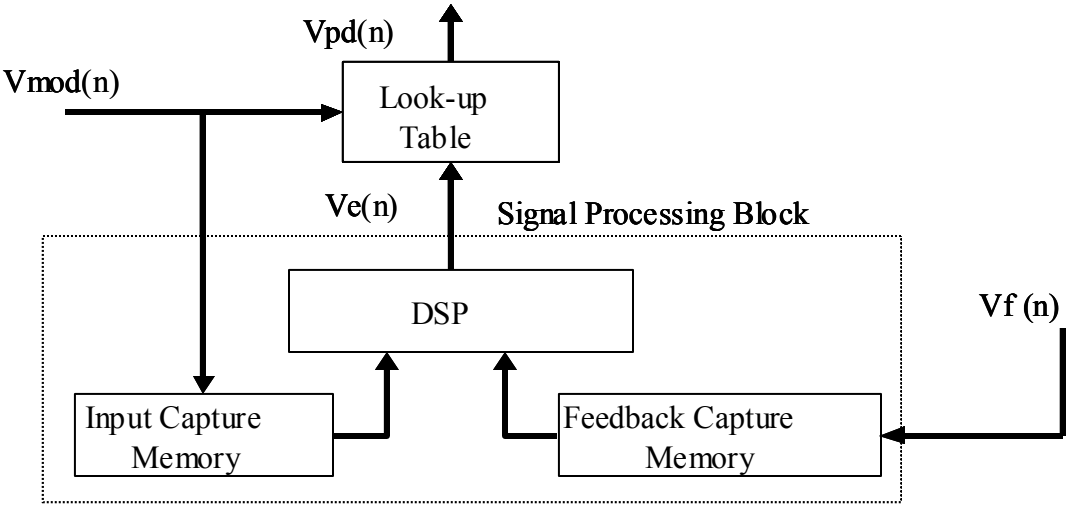

Figure 2.23 Delay Processing Block Diagram

There are several techniques described in the literature to compute the delay which exits in the forward and the feedback paths of the PA chain. A common technique to determine the delay requires the use of DSP which computes cross correlation between the input $V_{\text{mod}}(n)$ and the feedback $V_f(n)$ samples to determine the delay.

This method requires a block of input and feedback samples to be stored in capture memories at a periodic interval. The DSP computes the magnitude of baseband input and feedback samples and then interpolates samples by a predefined factor to increase accuracy of time delay estimation, followed by computing cross correlation of the two series The cross correlation of V_{mod} and V_f in discrete time domain is defined as,

$$R_{V_{\text{mod}}V_f}[n] = \frac{1}{N}\sum_{k=n}^{n+N-1} V_{\text{mod}}[k-n]V_f[k] = \frac{1}{N}\sum_{m=0}^{N-1} V_{\text{mod}}[m]V_f[m+n] \quad (2.38)$$

where $m \geq 0$

The sum will be maximum when the two samples streams line up. Therefore delay between the two signals is the from origin to time where the peak occurs in their cross correlation as shown in Figure 2.24. This delay is not constant and dependent on the modulation rates and amplifier characteristics. The amplifier characteristics change due to temperature, age and voltage. Therefore, the tables are required to be updated continually.

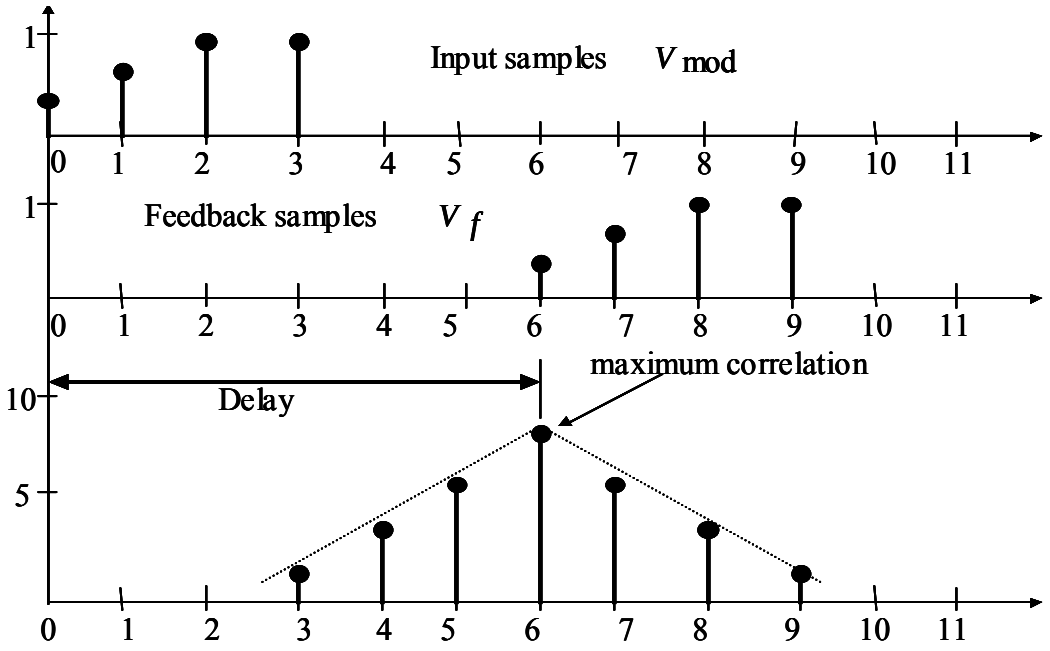

Figure 2.24 Cross Correlation Block Diagram

Other techniques employed for delay estimation are by comparing the slope of the magnitude of the input and feedback to determine direction of delay adjustment as

described in detail by Nagata [15]. Another simple technique exploits the properties of the modulation scheme [24].

2.8 Up-Conversion Topology

There are two main types of RF up conversion topologies suitable for Adaptive Digital Predistortion system. The first approach is using an Analog Quadrature Modulator (AQM) with direct up-conversion from complex baseband and the second approach is Direct Digital Modulator (DDM) with up-conversion from Digital IF.

2.8.1 AQM Up-Conversion Topology

Figure 2.25 illustrates the AQM up conversion topology. In this approach, the AQM imbalance compensated outputs I (real) and Q (imaginary) from the predistorter are feed to two separate Digital to Analog Converters (DAC).

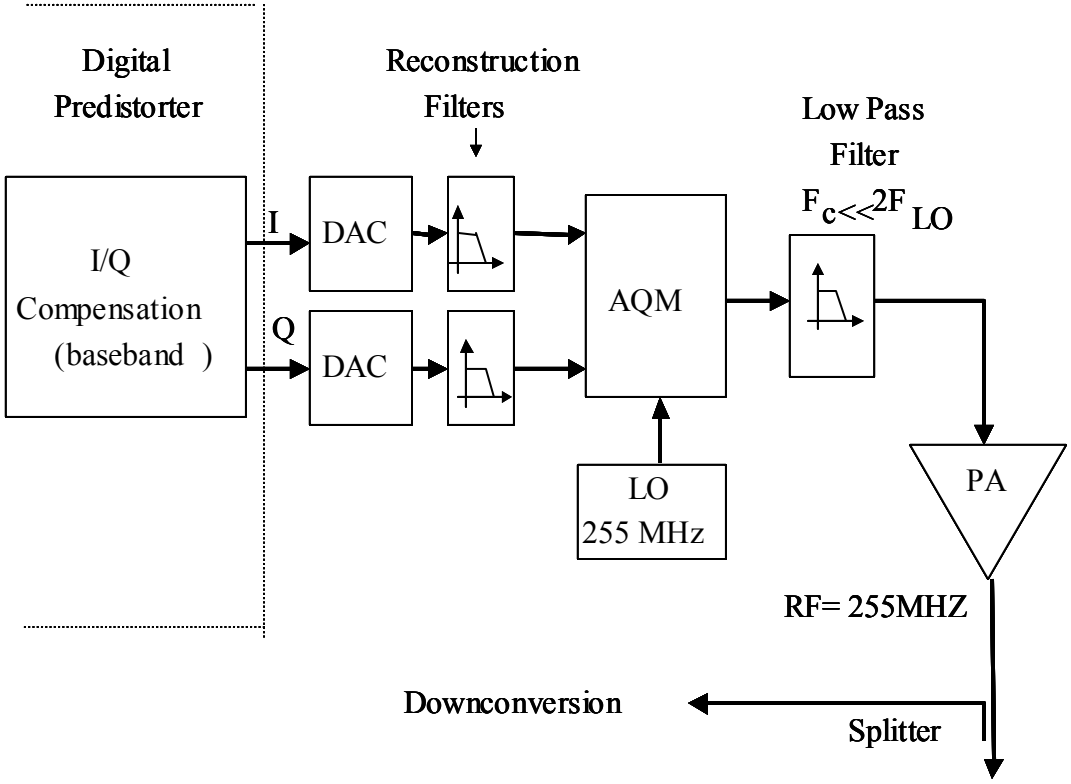

Figure 2.25 AQM Up Conversion Topology

The output from the DAC's is passed through lowpass reconstruction filters which remove the digital images that occur at multiples of sampling frequency (see Figure 2.26) and minimize the DAC quantization noise.

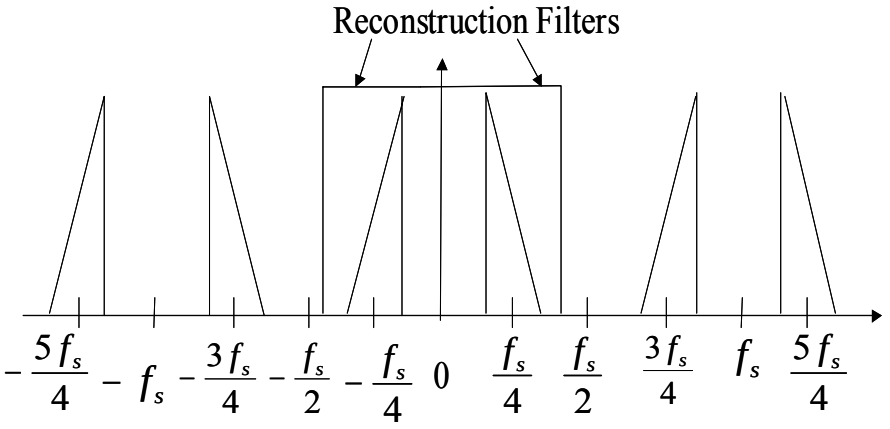

Figure 2.26 Filtered DAC Output

The complex filtered outputs are fed to the AQM which perform a direct up-conversion from complex baseband to RF. The output of the AQM (see Figure 2.27) is filtered to remove the 2nd harmonic of the RF before being fed to the Power Amplifier. The LO feedthrough and difference in gain between I and Q leg and cross coupling between the

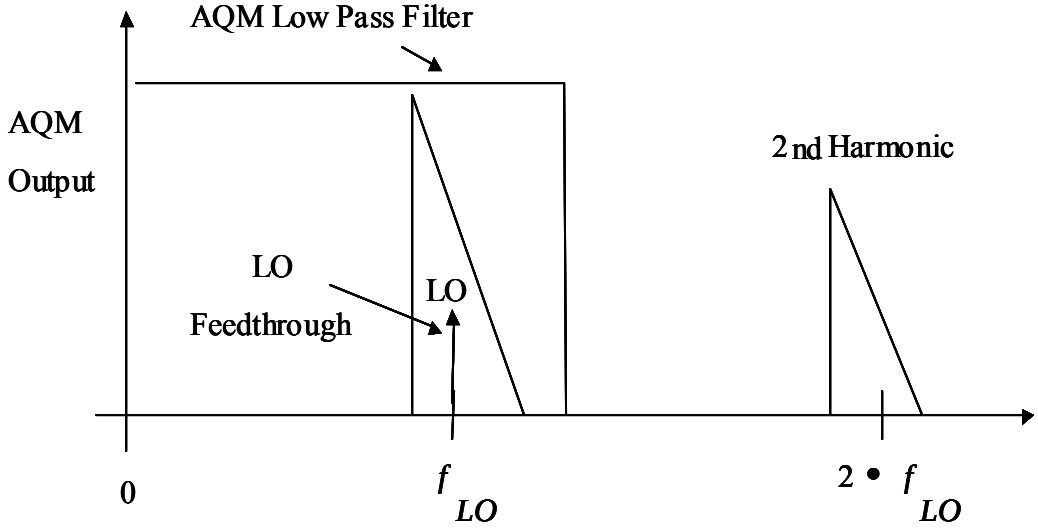

Figure 2.27 AQM Up-Conversion Output

two legs in the AQM are corrected for in the compensation circuit. This circuit is incorporated in the digital predistorter.

A typical quadrature modulator compensation circuit is shown in Figure 2.28, the DAC's and reconstruction filters are not shown for clarity.

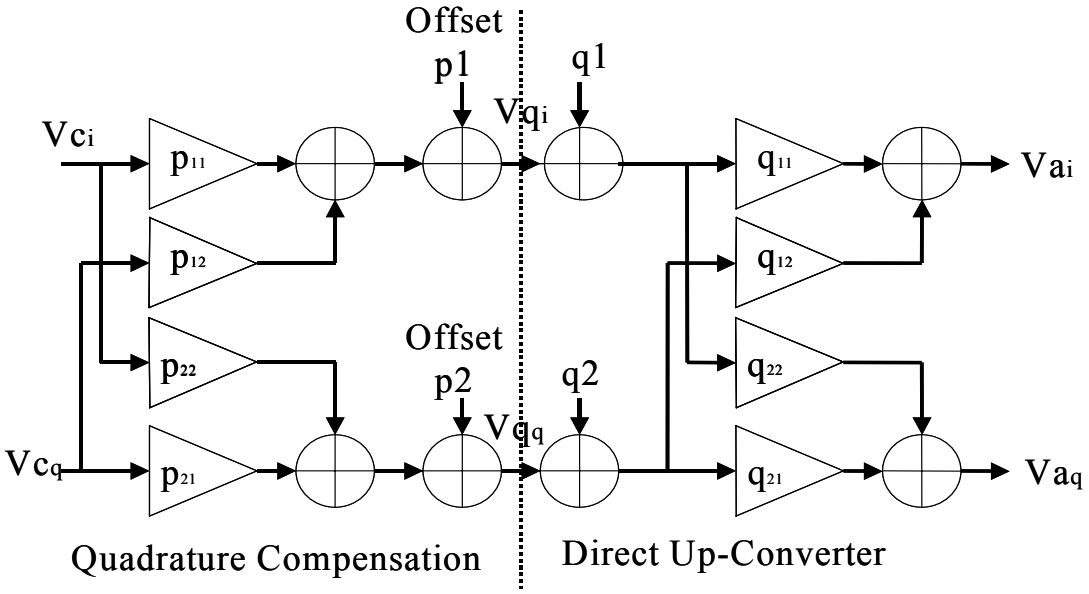

Figure 2.28 Quadrature Modulator Compensation Circuit

The amplitude gain in the I and Q legs are represented α and β, phase error of Ø and LO leakage into the output signal has effect similar to a DC offset is represented by p1 and p2. Then the gain imbalance is given by,

$$\gamma = (\alpha/\beta) - 1 \tag{2.39}$$

The up-conversion output is given by,

$$\begin{bmatrix} Vai(t) \\ Vaq(t) \end{bmatrix} = \begin{bmatrix} q11 & q12 \\ q21 & q22 \end{bmatrix} \left(\begin{bmatrix} Vqi(t) \\ Vqq(t) \end{bmatrix} + \begin{bmatrix} q1 \\ q2 \end{bmatrix} \right) \tag{2.40}$$

or can be written as $V_a(t) = Q.V_q(t) + q$

where q11 = α · cos(Ø/2),
q12 = β · sin(Ø/2),
q21 = α · sin(Ø/2),
q22 = β · cos(Ø/2)

The up-conversion error compensation output is given by,

$$\begin{bmatrix} Vqi(t) \\ Vqq(t) \end{bmatrix} = \begin{bmatrix} p11 & p12 \\ p21 & p22 \end{bmatrix} \begin{bmatrix} Vci(t) \\ Vcq(t) \end{bmatrix} + \begin{bmatrix} p1 \\ p2 \end{bmatrix} \tag{2.41}$$

or can be written as $V_q(t) = P.V_c(t) + p$

The correction circuit output compensates for errors in up-conversion when $p_i = -q_i$ and matrix P_{ii} = matrix Q_{ii}^{-1}. To keep the correction applied in the each leg independent of each other, the correction for the differential gain should be applied before the phase correction and carrier leak compensation should be applied last so that the gain and phase adjustments do not modify the DC offset correction term [20][21].

2.8.2 DDM Up-Conversion Topology

Figure 2.29 illustrates the DDM up conversion topology. In this approach, the predistorter up converts the complex baseband to a real digital IF using a digital quadrature modulator. The digital IF from the predistorter is converted to analog IF by a

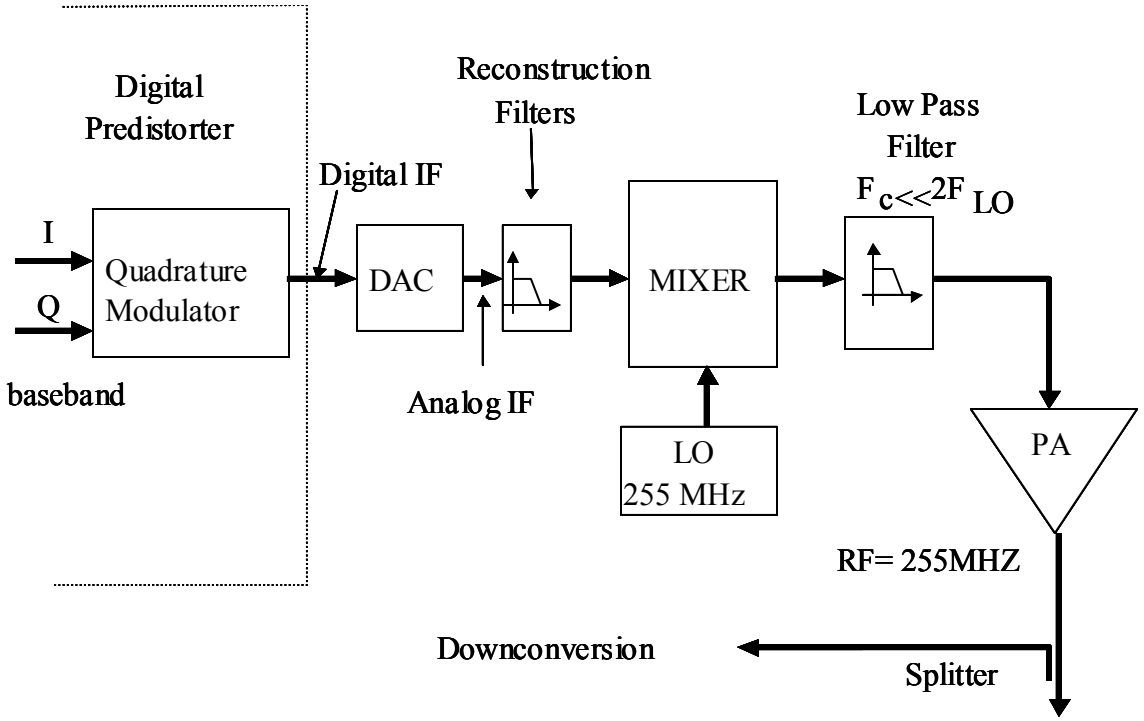

Figure 2.29 Direct Digital Modulator

single DAC. The output from the DAC is passed through lowpass reconstruction filters which remove the digital images that occur at multiples of sampling frequency (see Figure 2.26) and minimize the DAC quantization noise. The analog IF is processed by a mixer which translates the IF to required RF by a suitable choice of LO frequency.

2.8.3 Digital Up Converter

The digital quadrature modulator in predistorter is implemented as shown in Figure 2.30.

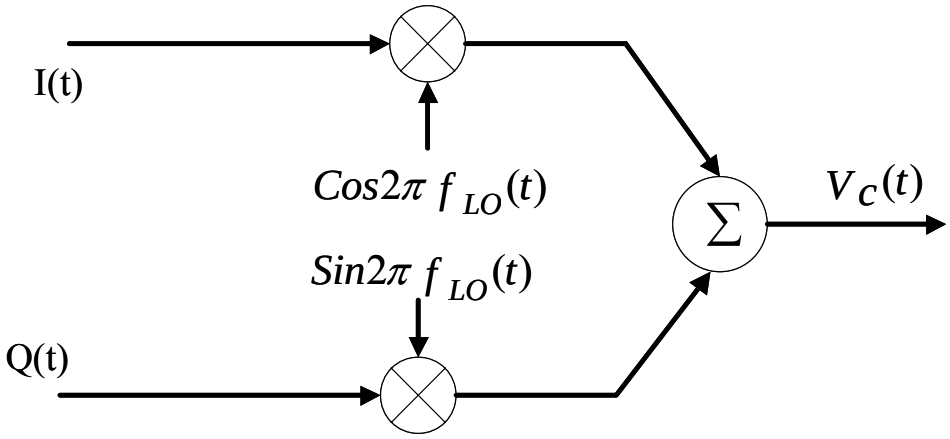

Figure 2.30 Digital Quadrature Modulator

The digital up-conversion is represented by,

$$V_c(t) = I(t)Cos[2\pi F_{LO}(t)] + Q(t)Sin[2\pi F_{LO}(t)] \qquad (2.42)$$

I(t) is the real component at baseband and Q(t) is the imaginary component.
The digital up-conversion can be performed without use of any multiplications using a quarter sampling rate translation technique in which the center of real digital IF is translated from baseband to the quarter ($f_s/4$) of the sampling frequency (f_s).

Therefore, when $f_{Lo} = f_s/4$ (as shown in Figure 2.31) the cosine mixing sequence is $t_0 = 1,\ t_1 = 0,\ t_2 = -1, t_3 = 0$ and sine mixing sequence is $t_0 = 0,\ t_1 = 1,\ t_2 = 0, t_3 = -1$ thus the spectral shifting by $f_s/4$ is achieved by applying cosine mixing sequence of 1,0,-1,0…etc to I (real) component and applying sine mixing sequence of 0,1,0,-1 … etc to the Q (imaginary) component and adding the result to obtain real IF (see Figure 2.32).

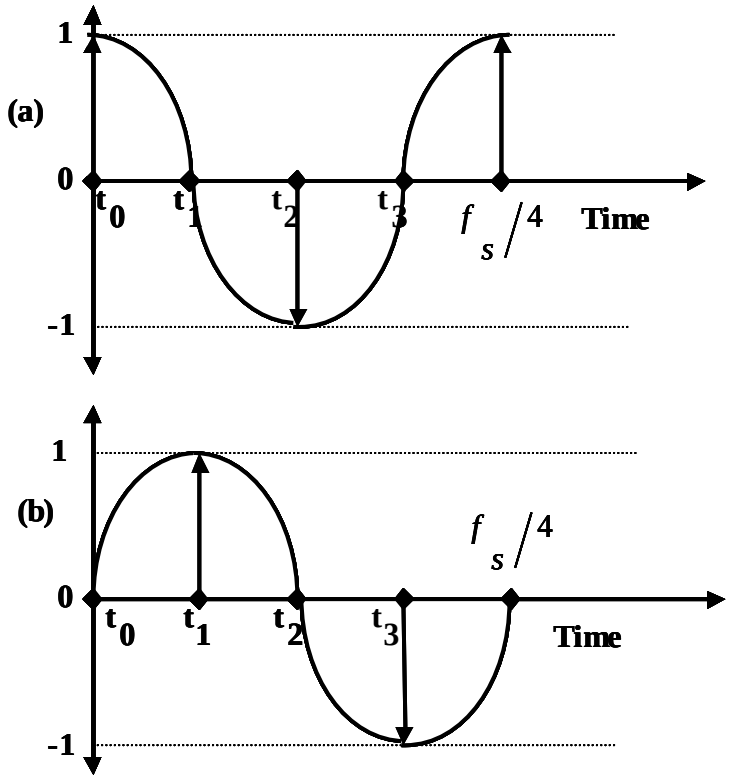

Figure 2.31 Digital Quadrature Modulator

The mixing sequence is either allowing the I/Q data to pass unaltered when the mixing sequence is 1 or inverting I/Q data when the mixing sequence is –1 and finally zeroing

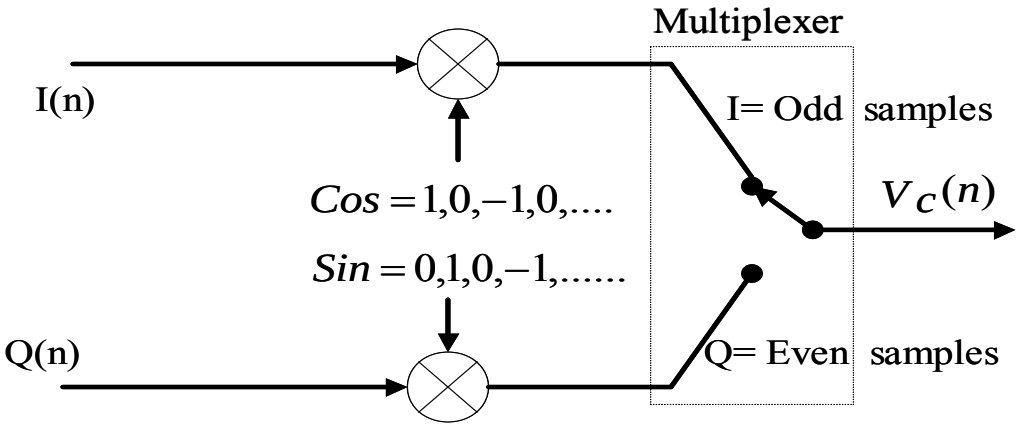

Figure 2.32 Digital Quadrature Modulator

I/Q data when the mixing sequence is zero. Further more, the addition process after mixing is only a data muxing sequence because the output of each mixing point is taken from I or Q path because when I path has valid data Q path data will be zero and vice versa.

2.8.4 Analog Mixer

Mixers operate by performing the trigonometric function of multiplying two sines as shown in Figure 2.33.

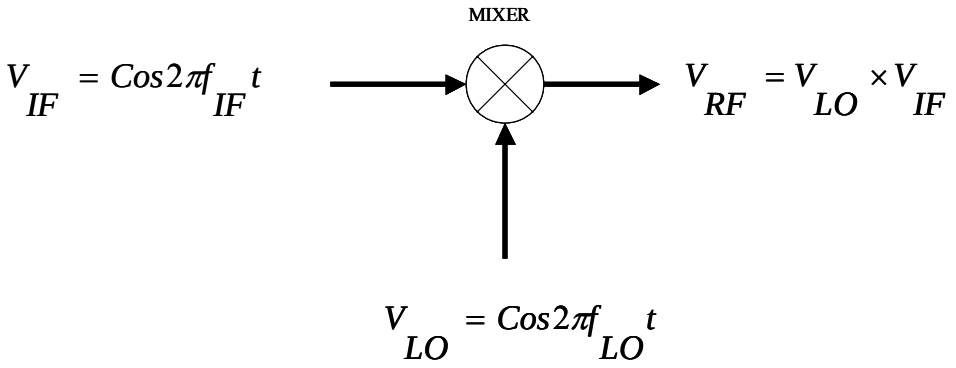

Figure 2.33 Analog Mixer

The output of an ideal mixer is given by,

$$V_{RF}(t) = V_{LO}(t).V_{IF}(t) \tag{2.43}$$

$$V_{RF}(t) = Cos[2\pi F_{LO}(t)]Sin[2\pi F_{IF}(t)] \tag{2.44}$$

simplifying gives,

$$V_{RF}(t) = \frac{1}{2}\{Cos[2\pi(F_{LO} - F_{IF})t + Cos2\pi(F_{LO} + F_{IF})t\} \tag{2.45}$$

Thus the RF output of the mixer consist of sum and difference of the input frequencies, centered at the LO frequency as shown in Figure 2.34.

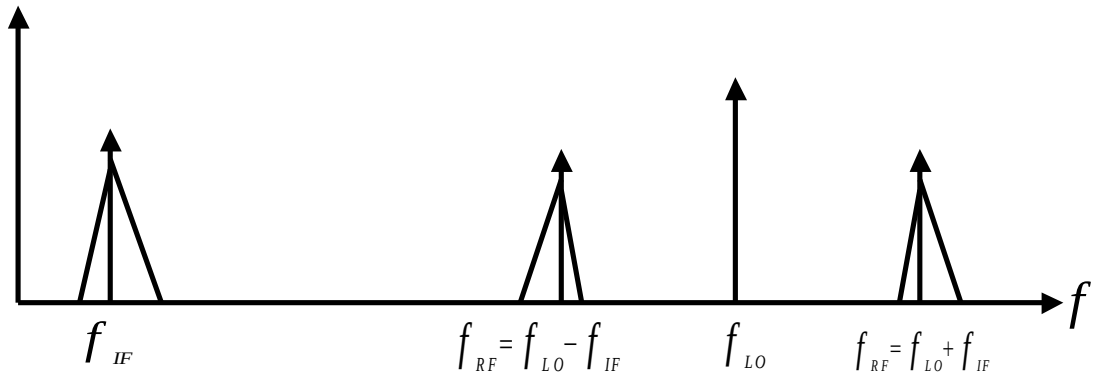

Figure 2.34 Mixer Frequency Conversion

Since the RF port of mixer generates sum and difference frequencies, the mixer can be driven by high-side LO or low-side LO as shown in Figure 2.35. A high-side LO refers to an LO frequency greater then the desired RF output and a low-side LO to refers to an LO frequency less then the desired RF output. LO selection is based on the criterion which ensures the IMD products generated by the mixing of the LO and IF fall outside frequency baseband of interest at the RF output.
For high side LO, the RF output given by

$$F_{RF} = F_{LO} - F_{IF} \tag{2.46}$$

and for low-side LO , RF output is given by

$$F_{RF} = F_{LO} + F_{IF} \tag{2.47}$$

If high-side LO is chosen, then there is spectral inversion at RF output as shown in Figure 2.35. The spectral inversion is easily corrected by swapping the baseband I and Q outputs in the predistorter.

Depending on high-side or low-side injection, the IMD products is given by,

$$F_{IMD} = F_{LO} \pm F_{RF} \tag{2.48}$$

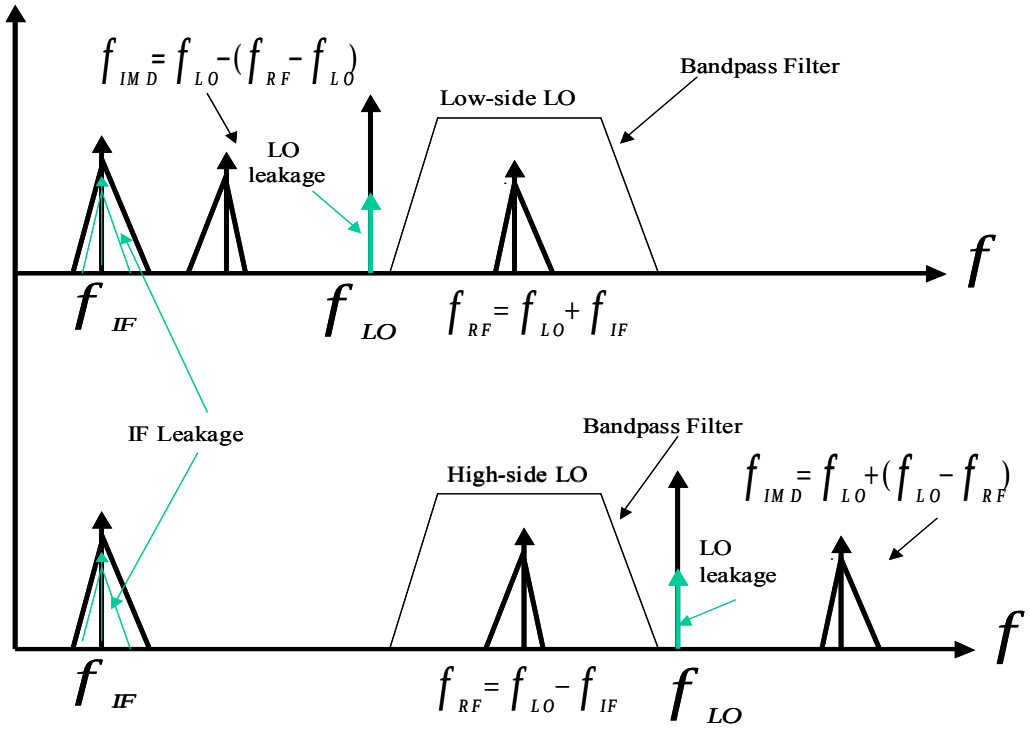

Figure 2.35 Mixer Distortion Terms

In practice, the mixers are not ideal, thus internal impedance mismatches and limitation of coupler performance results in some LO power and IF power being coupled to the RF port as shown in Figure 2.35. Therefore a bandpass filter is necessary to only allow the distortion terms generated by the predistorter to pass but rejects the IF and LO leakage, and the IMD products generated by the mixer. For optimum performance from the predistorter, the noise figure and conversion loss parameters of mixer also need to be considered.

2.8.5 Down-Conversion Topologies

There are two main types of RF down conversion topologies suitable for adaptive digital predistortion system. The first approach is using an Analog Quadrature Demodulator (AQD) with direct down conversion from RF to complex baseband and the second approach is Direct Digital Demodulator (DDD) with down-conversion from RF to Digital IF.

2.8.6 Analog Quadrature Demodulator

Figure 2.36 illustrates the AQD down conversion topology. In this approach, the RF output from the Power Amplifier is fed AQD. The I (real) and Q (imaginary) outputs from the AQD are passed through low pass filters to reject the down conversion images and then fed to two separate Analog to Digital Converters (ADC).

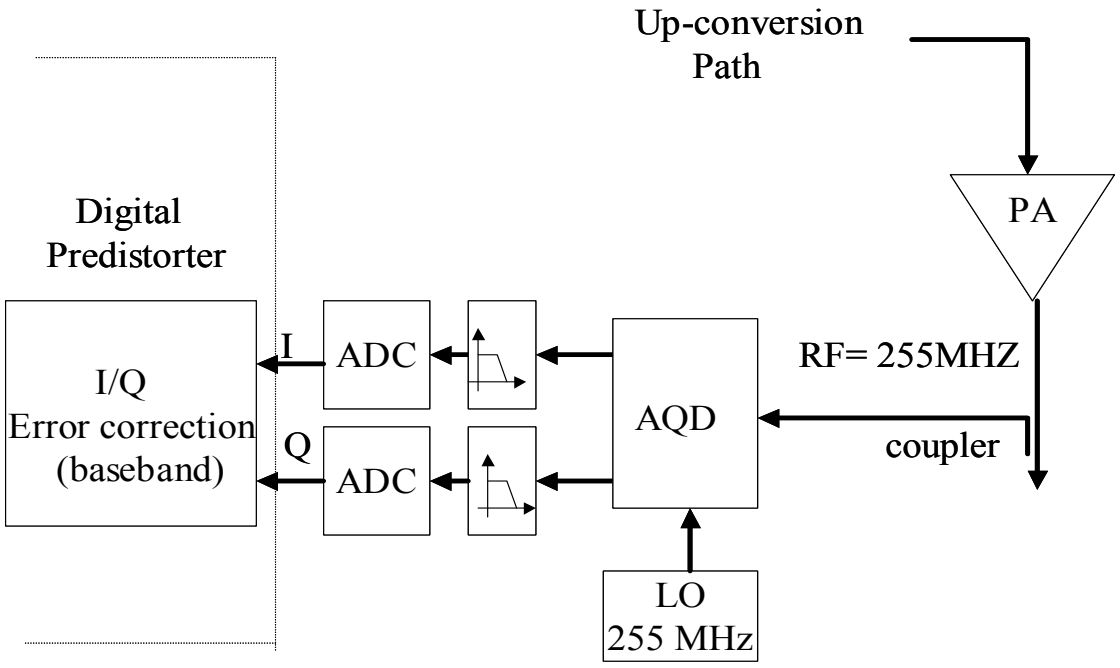

Figure 2.36 AQD Down Conversion Topology

The digital baseband output from the ADC's is fed to the predistorter which compensates for I/Q imbalances and LO leakage in the AQD. The correction techniques used for I/Q imbalances in a demodulator is the same as in AQM in the up conversion path presented in section 2.8.1.

2.8.7 Direct Digital Down-Conversion

A block diagram of the Direct Digital down conversion is given in Figure 2.37. RF signal is tapped off the power amplifier output using a coupler and attenuated and fed to wide input bandwidth ADC. The RF signal is undersampled by the ADC to produce an image of the RF signal at a convenient lower frequency so it is easier to process by the predistorter. The image is a copy of the RF signal, resulting from the sampling process. The Nyquist criteria states that to preserve all the signal information it must be sampled at a rate at least twice the signal bandwidth. The only constrained applied to absolute location of the signal frequency is that all signal bandwidth must lie within a single

Nyquist zone. Each Nyquist zone is defined as a multiple of half the sample frequency. The image of the RF signal at the 1st Nyquist Zone may have a spectral inversion if the RF signal falls in an even SyQuest zone. The spectral inversion is easily corrected in the predistorter by swapping the I and Q data at baseband.

One important selection criteria for the sampling frequency is that it should be low enough to allow the scheme to be implemented in available hardware devices and high enough that the signal bandwidth of interest does not cross the Nyquist zones, otherwise aliasing will occur across the spectrum [22].

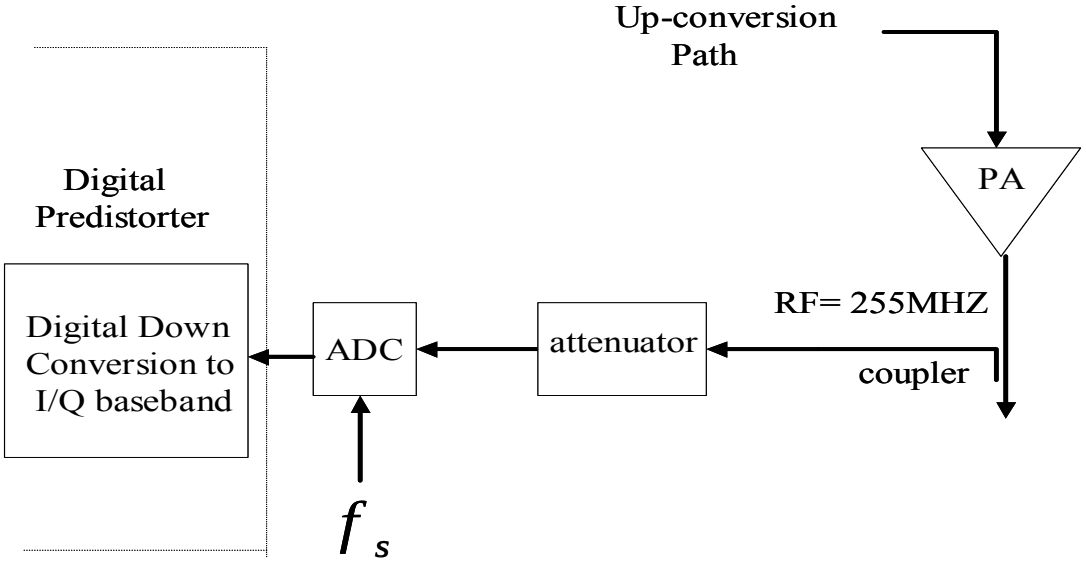

Figure 2.37 Digital Down Conversion

Figure 2.38 show that sampling a signal above the first Nyquist zones is in effect a down conversion.

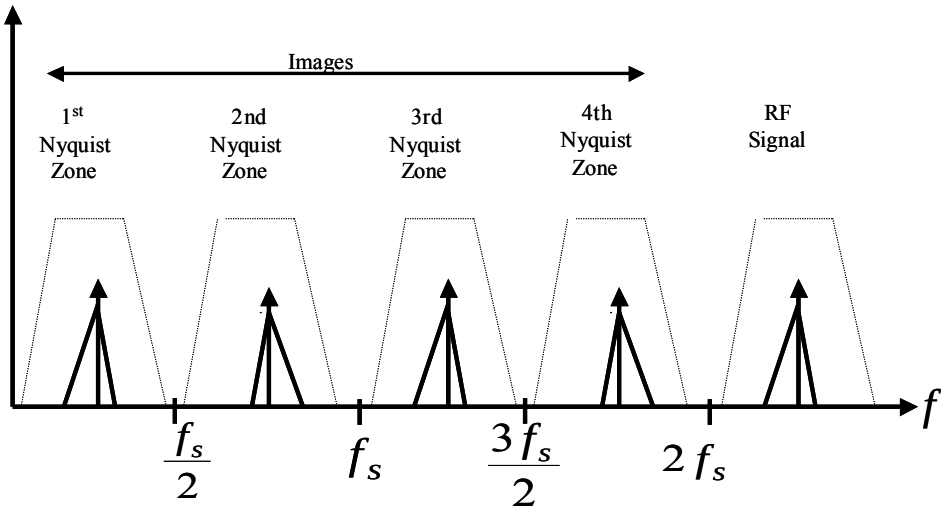

Figure 2.38 Spectral Images of RF Signal from Under Sampling

Additionally, if the sampling frequency is four times the center of RF signal in the 1st Nyquist zone. Then digital down conversion to I/Q baseband can be performed in the predistorter without the use of any multiplications using a quarter sampling rate translation technique as described in up conversion process and as shown in Figure 2.39.

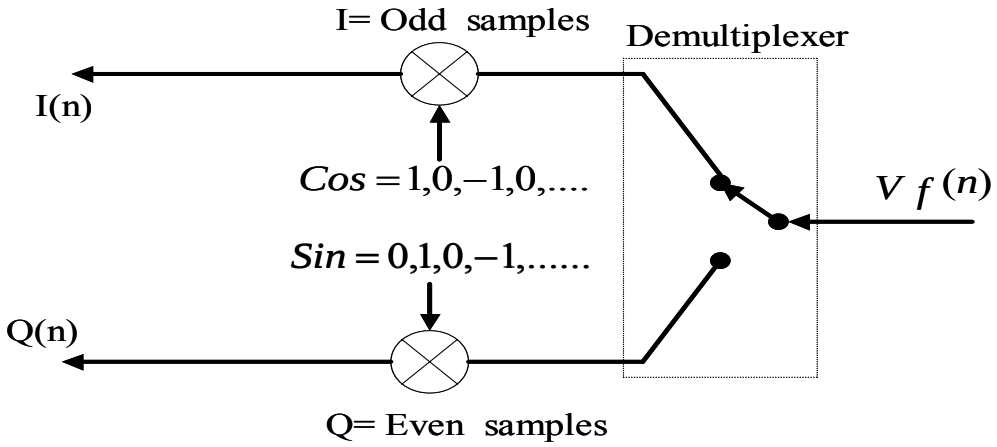

Figure 2.39 Quadrature Digital Down Conversion

Each feedback sample is clocked into the predistorter from the ADC, is either not changed, zeroed or sign change applied to generate I(real) and Q(imaginary) data stream. The data stream is then filtered to reject higher frequency images [23].

2.8.8 Discussion on AQM Approach versus DDM Approach

The advantage of the AQM approach is that it allows wider input signal bandwidth compared to DDM approach as shown in Figure 2.40. Secondly, the nearest undesired

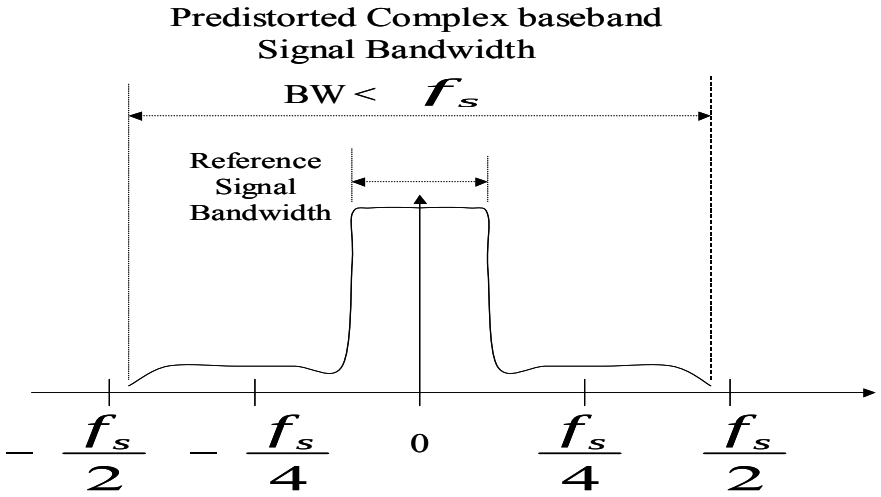

Figure 2.40 Complex Baseband Output of the Predistorter

component is the mixing image at the second harmonic of the LO frequency, so the filtering requirement is much simpler.

The disadvantage of the AQM approach is that two independent DAC's are required and also AQM suffers from I,Q imbalances and LO leakage which will result in poor image rejection and reduced dynamic range if not compensated. Therefore, reducing or eliminating the IMD correction obtained with a digital predistorter.

The advantages of the DQM approach are that only a single DAC is required and no I,Q imbalances and LO leakage compensation circuit is required. The disadvantages are that to obtained the same input bandwidth as the AQM approach the DAC sampling frequency needs to be doubled, which is not always possible because of hardware limitation. Additionally, the requirement of up conversion of digital baseband IQ to digital IF and LO canceller circuit to suppress the LO at the mixer output. The choice of cut-off frequencies for the reconstruction filters and the low pass filter for both approaches is determined by the bandwidth of the input signal and the distortion products generated by the non-linearities in the up-conversion chain and the power amplifier.

If the up-conversion chain only exhibits dominant 3^{rd} order distortion products then the predistorter will only generate 3^{rd} and up to 5^{th} order distortion products to correct for the non-linearities. Therefore up-conversion bandwidth needs to be 5 times the signal bandwidth.

3.0 DEMONSTRATION MODEL

3.1 Predistortion Demonstration Model

The literature survey indicated that the AM to AM distortion was dominant in most power amplifiers.
A breadboard hardware previously designed for OPTUS C1 UHF satellite Transponder program was used to implement a single look-up table which would correct for AM to AM distortion. The breadboard hardware consisted of a Digital Filter Module with a reconfigurable Xilinx FPGA and Personal Computer (PC) interface to reconfigure the FPGA, a two stage Up-Conversion Module and a Spacecraft Interface Module (see Figure 3.1).

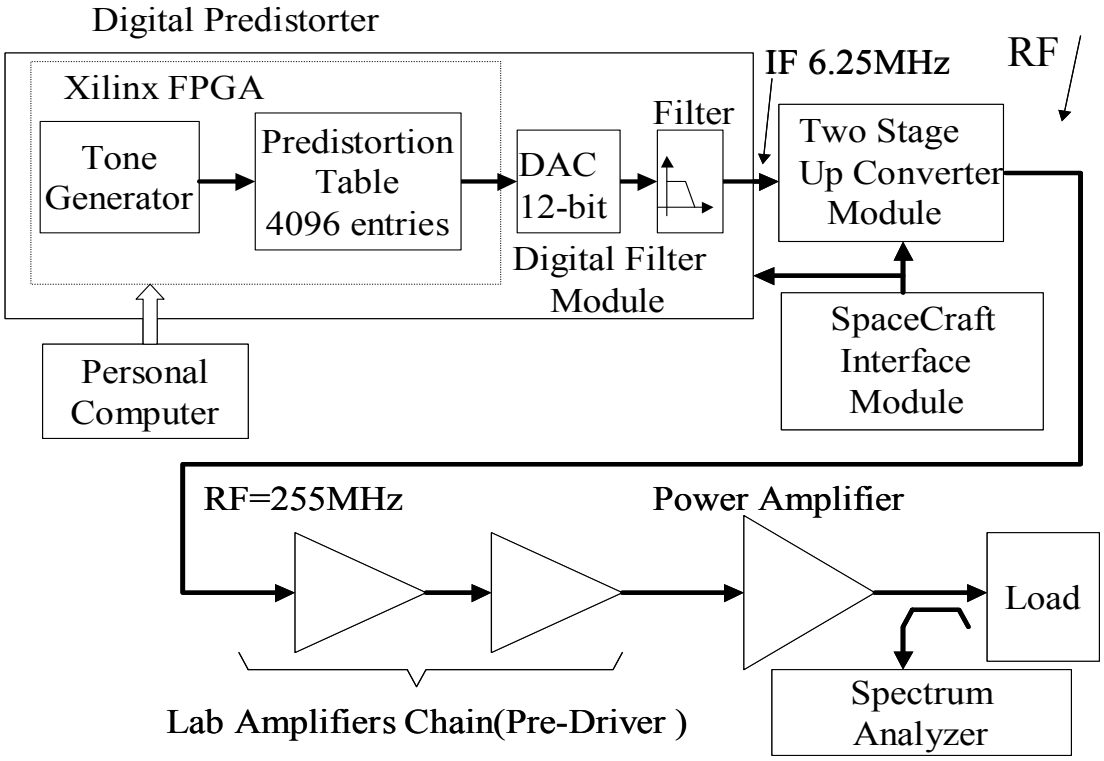

Figure 3.1 Breadboard Digital Predistorter

Digital predistorter was implemented in FPGA using VHDL. The PC was used to reconfigure the FPGA with the predistortion function. The Up-Conversion module translates the 6.25 MHz IF output from the Digital Filter Module to 255 MHz RF output. Spacecraft Interface module is used to configure the PLL's in up-conversion module to output the RF at 255 MHz. The RF output of Up-Conversion module drives a non-linear amplifier chain which was constructed from laboratory power amplifiers and attenuators, and Raytheon's dual, push-pull, class-AB, UHF power amplifier. The Digital predistorter consists of a tone generator , 4096 entry look-up table,12-bit DAC and a reconstruction filter. Five equal power tones spaced 25 KHz apart and centered at 6.25 MHz are generated by the tone generate. The composite signal of the tones is used to index into 4096 entry look-up table. The look-up table has inverse transfer characteristics of the power amplifier chain stored and therefore it predistorts the input signal to cancel effects of distortion generated by the power amplifier chain. The predistorted signal is filtered and up-converted to an RF of 255 MHz and fed to the non-linear RF power amplifier chain. The power amplifier chain is carefully set up so that the pre drivers are Class A amplifiers and are set to operate in linear region. Only Class A/B power amplifier will operate in nonlinear regions of the amplifier. Therefore most of the distortions is produced by the final stage power amplifier. A photograph of the predistorter breadboard setup is shown in Figure 3.2.

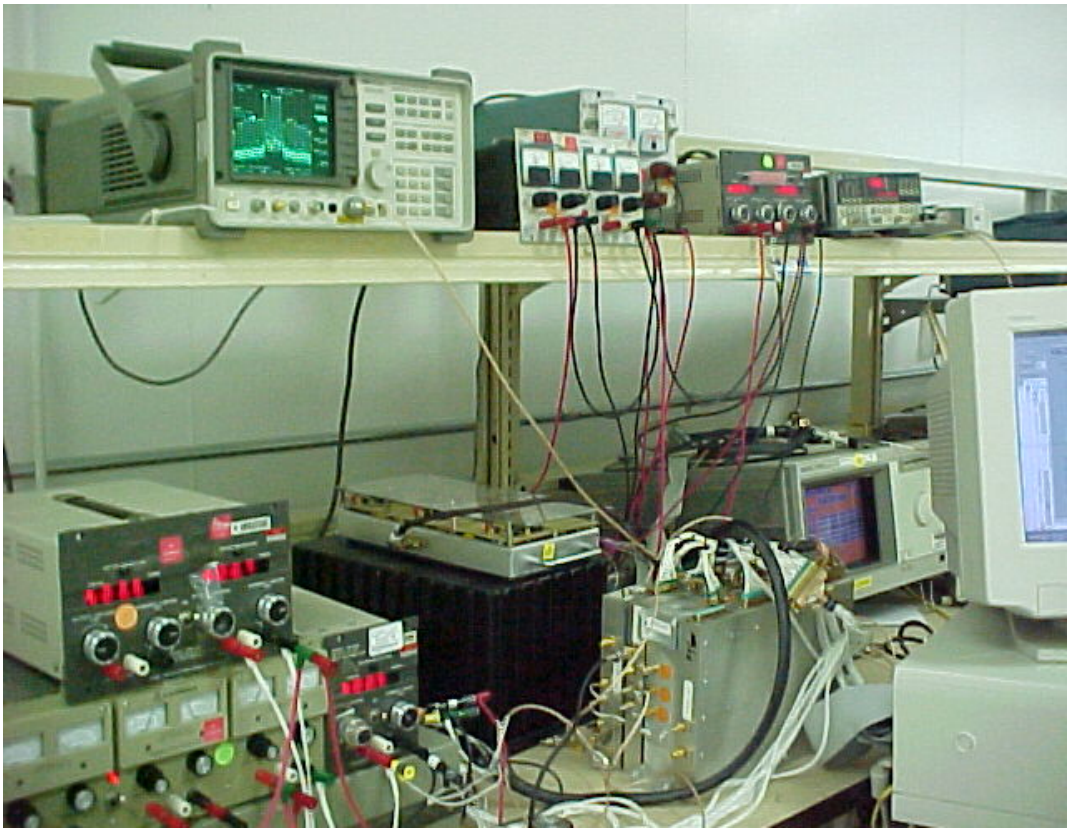

Figure 3.2 Photograph of Breadboard Digital Predistorter

To compute the look-up table entries which would represent the inverse characteristics of the power amplifier chain. Firstly, the transfer characteristics of power amplifier chain at RF of 255 MHz was measured with the input power ranging from –70 dBm to 0 dBm. Figure 3.3 shows the power amplifier chain transfer characteristic.

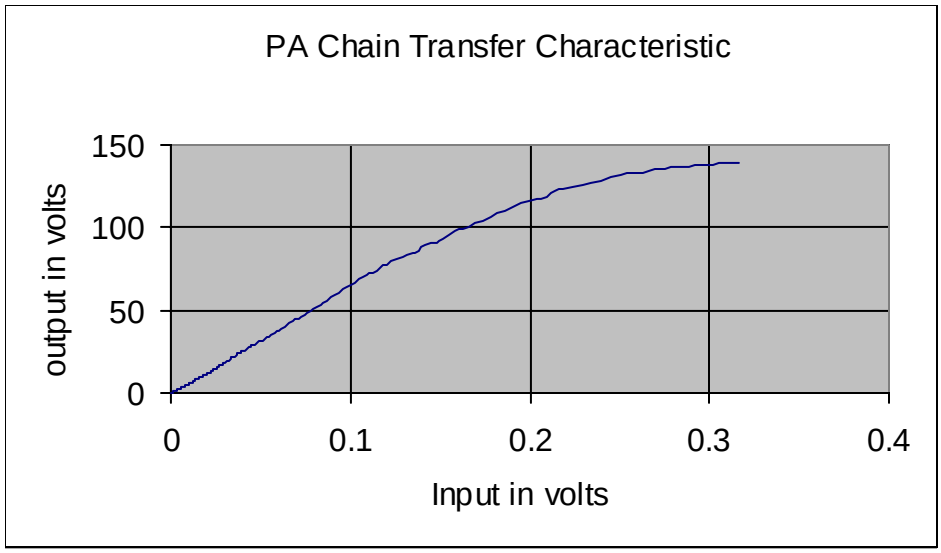

Figure 3.3 Measured PA Chain Transfer Characteristics

Using MATLAB, the measured data was used to generate polynomial to fit transfer characteristics of the power amplifier chain as shown in Figure 3.4.

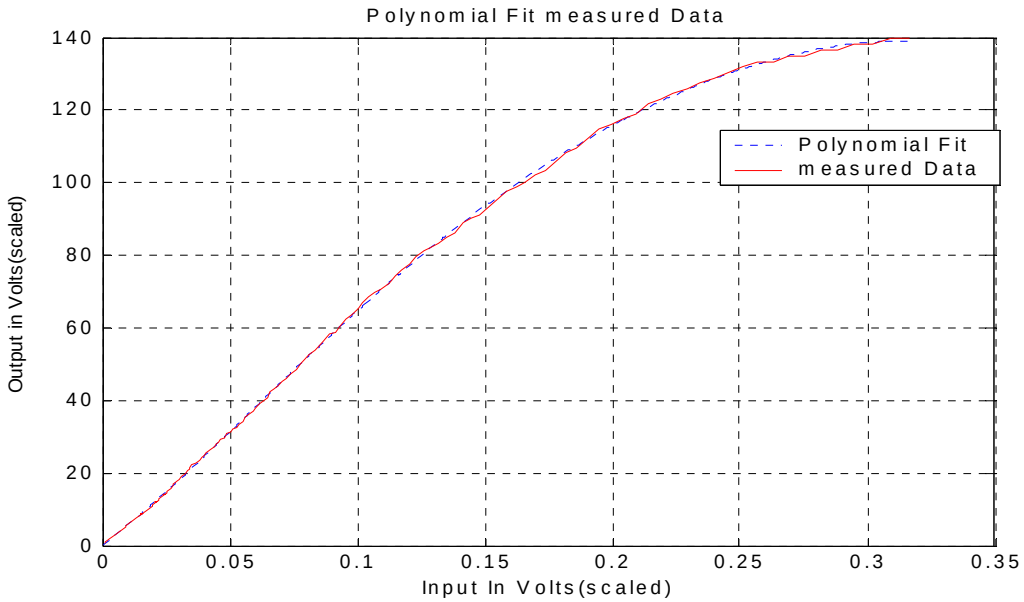

Figure 3.4 PA Chain Transfer Characteristics Polynomial Fit

The polynomial that describes the transfer characteristic is given by,

$$53.4X + 28.59X^2 - 2280.7X^3 + 6123.2X^4 - 6544.1X^5 \quad (3.1)$$

The linear gain of the chain is calculated to determine the divergence of the above polynomial from the linear gain. The divergence factor is used to compute inverse transfer characteristic polynomial which is given by,

$$72.6X - 285.9X^2 + 22807X^3 - 61232X^4 + 65441X^5 \quad (3.2)$$

Figure 3.5 shows inverse transfer characteristic which is computed from linear gain and measured transfer characteristics.

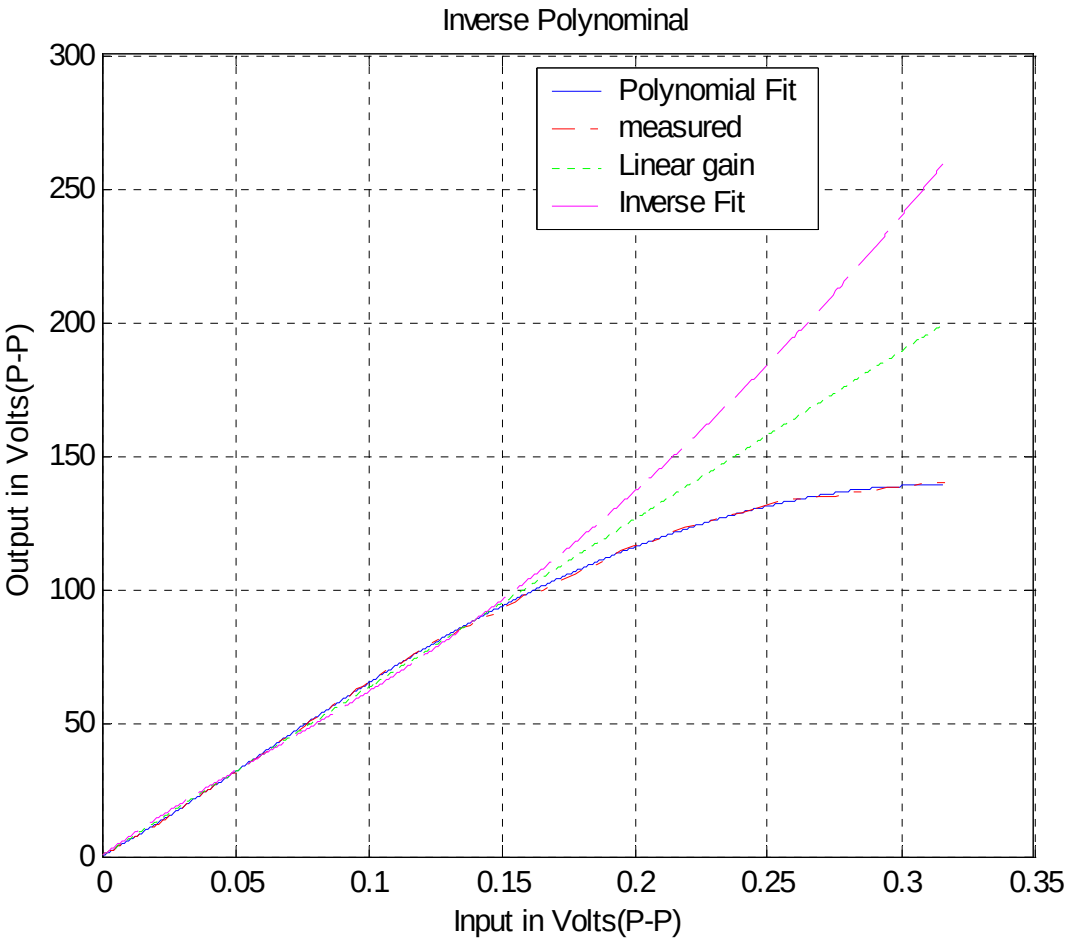

Figure 3.5 PA Chain Inverse Transfer Characteristics Polynomial Fit

The gain of the power amplifier chain is computed from polynomial in equation 3.1 and the correction gain is computed from the inverse polynomial given in equation 3.2.

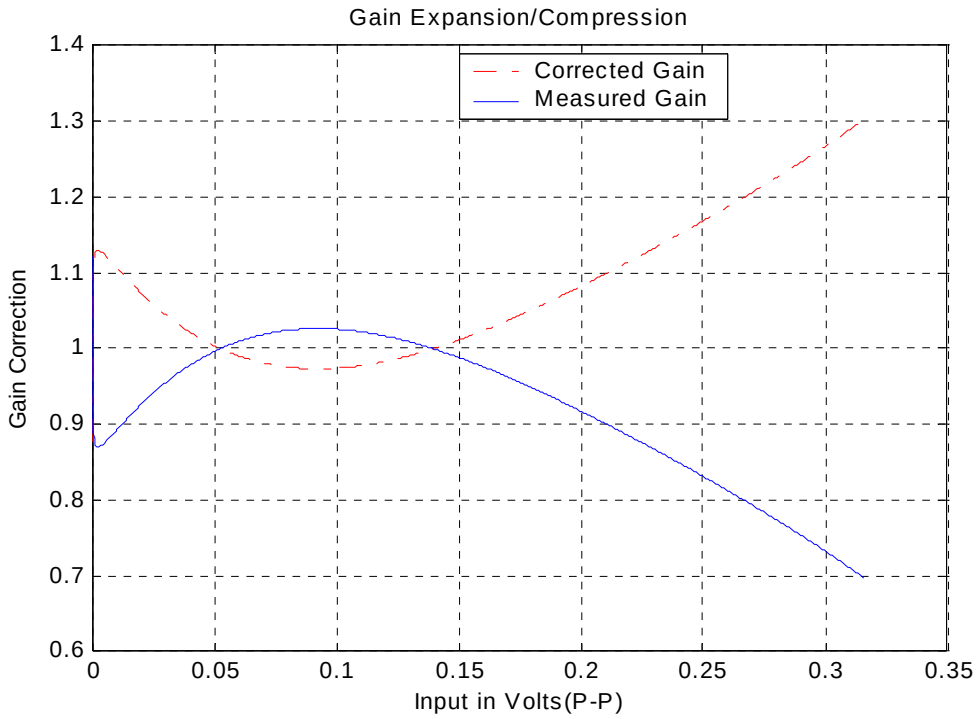

Figure 3.6 PA Gain Compression

Figure 3.6 shows that the power amplifier exhibits gain compression in the cut-off region and saturation region. The inverse gain curve shows gain expansion in the cut-off region and the saturation region to compensate for the gain compression. The inverse gain is scaled in terms of input counts and output counts to fit the look up table. For positive input values the scaled inverse gain curve is shown in Figure 3.7.

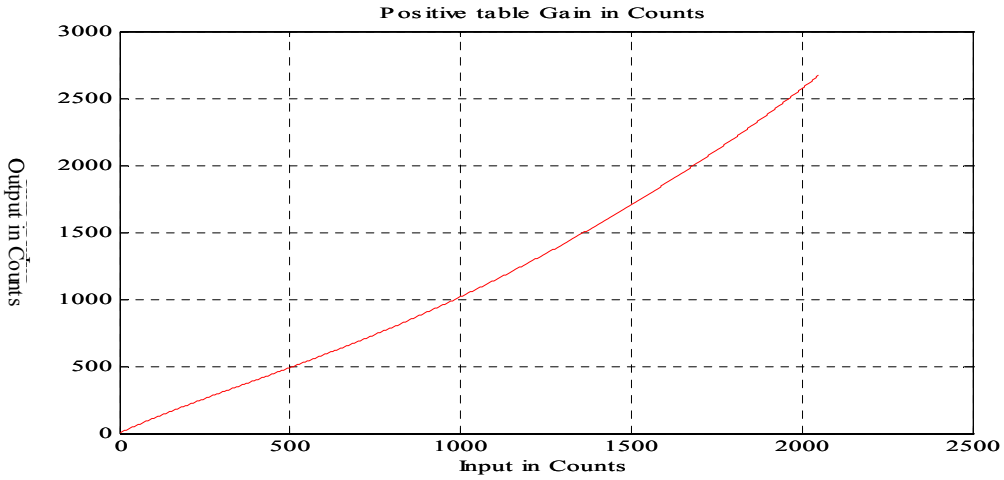

Figure 3.7 PA Gain Inverse Curve

The look-up table has 4096 entries and drives a 12-bit DAC. It has to accommodate positive and negative excursion of input signal. Since the table drives a 12-bit DAC the table entry are clamped at output of zero and 4096. This prevents entries wrapping around at the extremes of the table. Figure 3.8 shows inverse gain scaled look-up table for the predistorter.

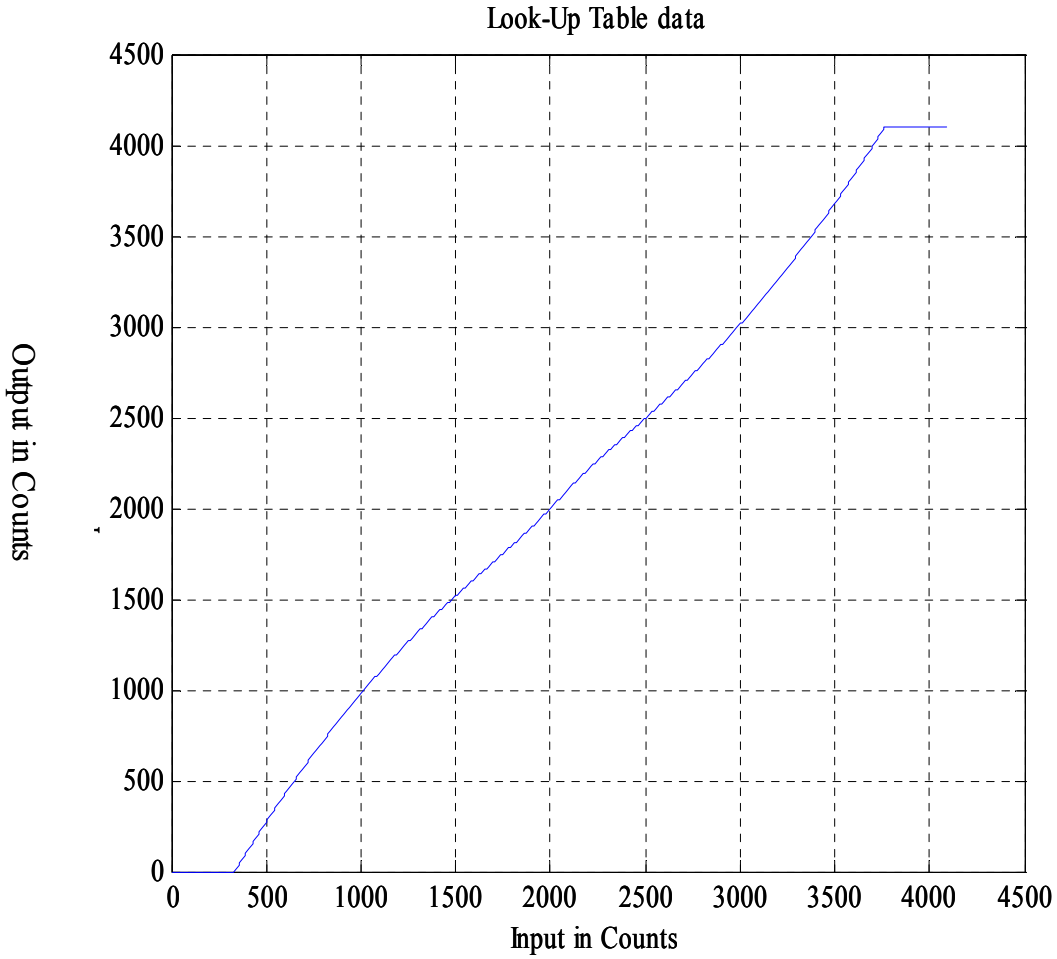

Figure 3.8 Predistorter Gain Look-Up Table

To test the performance of the predistorter the look-up table is placed in by-pass mode via PC command to the FPGA. The composite of five equal power tones centered at 6.25 MHz are feed directly to the 12-bit DAC in the digital filter module. This output is translated to 255 MHz to drive power amplifier chain to deliver an output power of 12 Watts. The output of Class A-B power amplifier is fed via coupler and attenuators to spectrum analyzers. Figure 3.9 left shows that with no correction the IMD products are 22 dB down from the carriers. The predistorter table is now activated via PC command so

the fives tones are predistorted and then feed to the power amplifier chain. Figure 3.9 right shows IMD products are now 32 dB down from the carriers. The five tone test results show that with a simple amplitude correction digital predistorter was able to achieve 10 dB of IMD correction. The results also show that there is spectral growth in the lower level IMD as a result of the correction process.

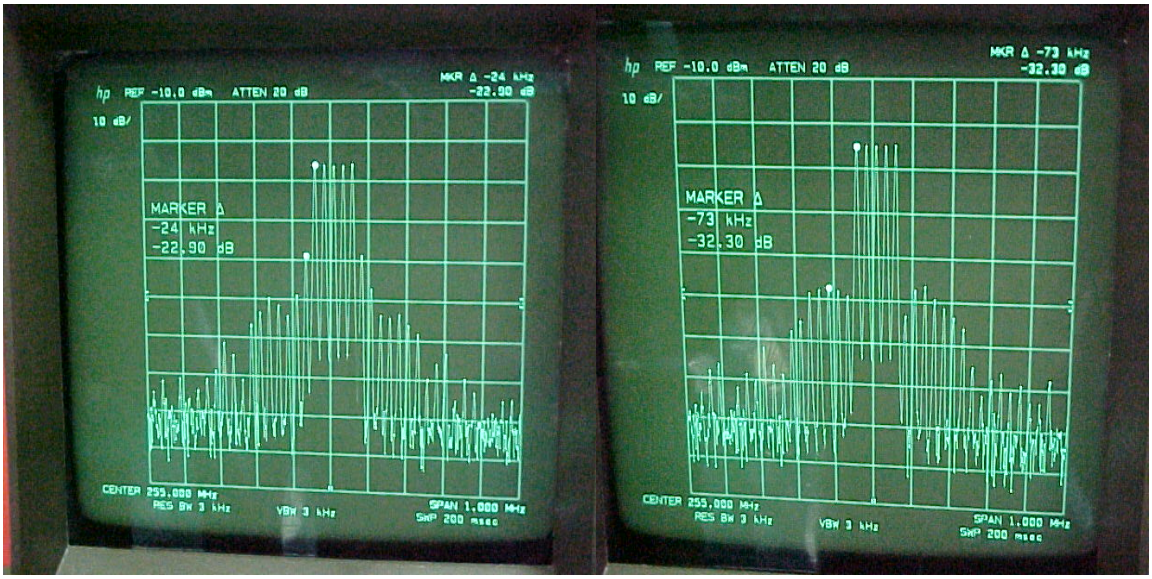

Figure 3.9 Left-PA Uncorrected, Right-PA Corrected

The next process was to add phase correction and update both tables adaptively. Before this process was started, a SIMULINK model of breadboard hardware was developed to determine what level of correction could be expected from the digital predistorter using existing hardware. Additionally, the breadboard hardware was only designed to handle 100 KHz of signal bandwidth, where as the requirement is for the digital predistorter to correct IMD distortion over 30 MHz of signal bandwidth.

4.0 SIMULINK SIMULATION MODEL AND SIMULATION RESULTS

4.1 Digital Adaptive Predistortion MATLAB SIMULINK Model

A SIMULINK model of Complex Gain Predistorter with polar tables as described in section 2.7.2 was developed. The model was based around the breadboard hardware used to demonstrate amplitude digital predistortion. The SIMULINK model consisted of seven major blocks: tone generation, address generator, delay adjustment, complex multiplier, PA model based on measured data, error correction and adaptation tables as shown in Figure 4.1.

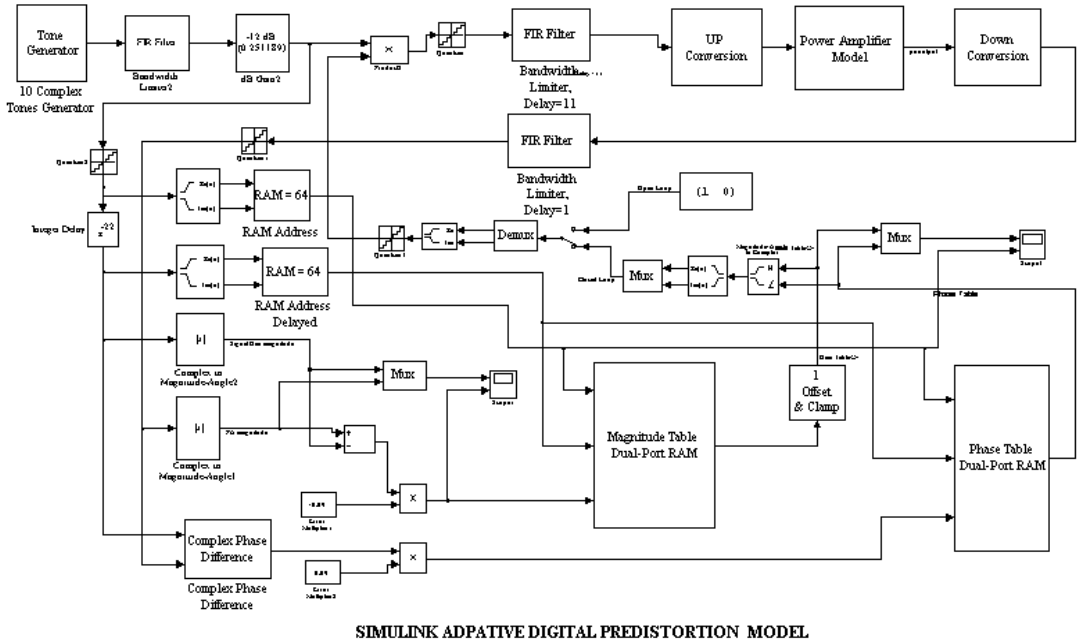

Figure 4.1 SIMULINK Model of Complex Gain based Adaptive Digital Predistorter

4.2 SIMULINK Model Description

The tone generation can be programmed to generate any number of adjustable power complex tones at baseband or offset IF. The complex tones are fed to the table address generator block, delay adjustment block, and complex multiplier block. The address

generator block computes the magnitude of the complex waveform and scales it to address the specified size of the adaptation look-up table. The delay adjust block delays the complex waveform for the required number of samples so that the error vectors are generated from time aligned input complex tones and power amplifier (PA) distorted output complex tones. The complex multiplier block multiplies the input complex tones with error vectors stored in the look-up tables. Therefore predistorting the input to the power amplifier so as to cancel the distortion generated by the power amplifier.

The baseband predistorted input is up-converted to RF and fed to the PA model block. The PA model block consists of gain and phase polynomials which are computed from the measured data (see Figure 4.2) on the Raytheon Power amplifier. The magnitude of up-converted input to the PA is computed and multiplied by the gain polynomial and the phase polynomials of the PA. Therefore, the output of the PA block represents the PA characteristics. The RF output of the PA model block is down-converted to base-band and fed to error correction block. The error correction block time aligns complex baseband input and the PA output and then converts complex signals to gain and phase components to compute error vectors. The gain and phase error vectors are scaled and stored in error table at an address corresponding to the magnitude of the time aligned complex input of each sample.

The adaptation tables consist of error table RAM and update table RAM configured to operate as dual port ram. The error RAM is addressed by the time aligned magnitude of the input complex tone and stores error vectors. The update RAM is addressed by the magnitude of the complex input tones and supplies correction vectors to the complex multipliers which pre-distorts the complex input tones fed to the PA.

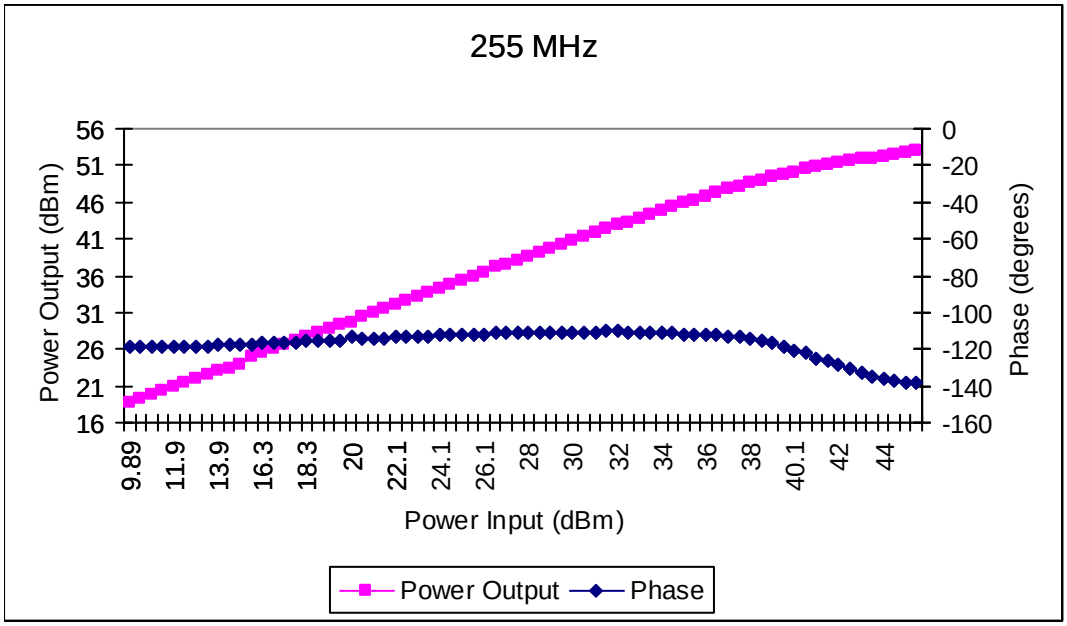

Figure 4.2 Power Amplifier Gain and Phase Characteristics

4.3 SIMULINK Model Simulation Results-100 KHz Signal Bandwidth

The tone generation is configured to generate 5 complex tones centered at 6.25 MHz occupying approximately 100Khz of bandwidth with peak to average ratio (PAR) of 7 dB. The input to the PA is scaled to operate the PA at the nominal power level of 42 dBm. The SIMULINK model is operated in open loop so that the PA is not linearized. A 2^17-point FFT at sample rate of 520 MHz is performed on the output signal of the PA. Figure 4.3 shows PA output when no correction is applied. The IMD level are approximately 20 dB down from the carriers.

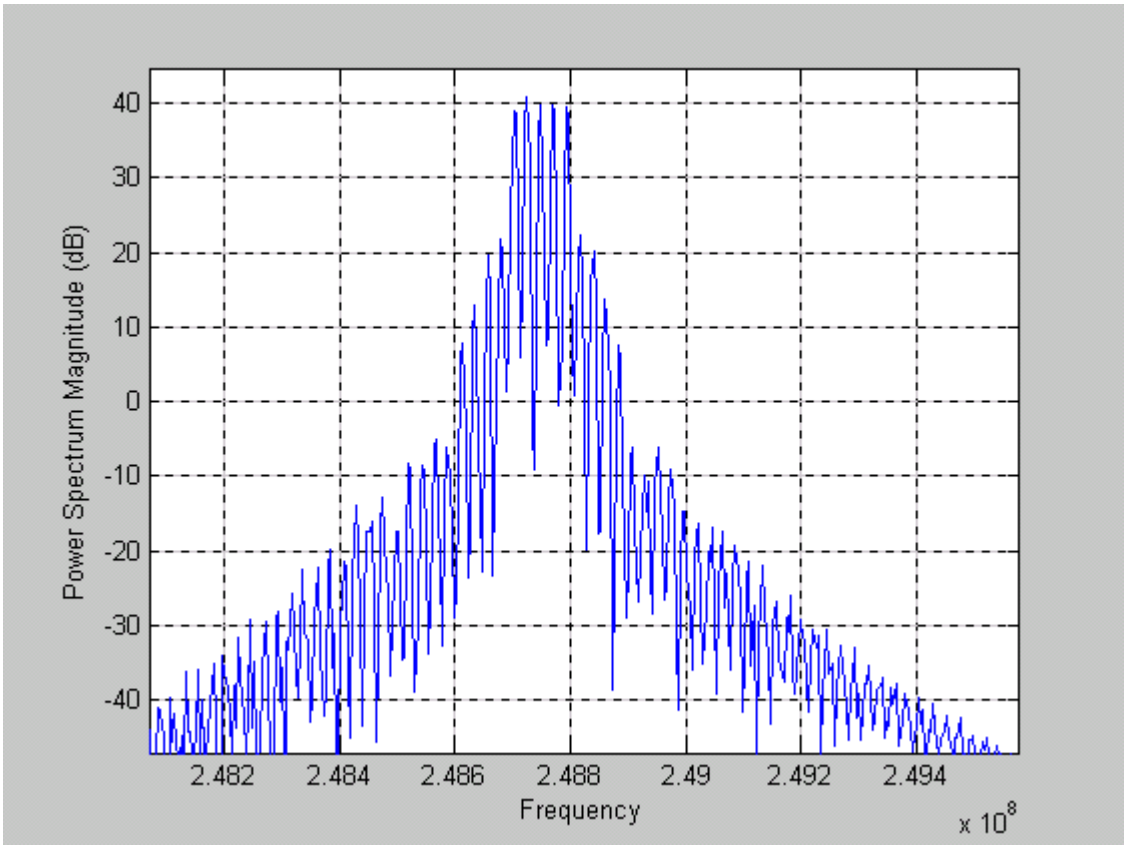

Figure 4.3 Power Amplifier Output without Correction

The SIMULINK model is now operated in closed loop and the PA is allowed to be linearized by predistorting the drive to the PA via the adaptation tables. The simulation was run for 10 seconds which took about 10 minutes to process by a 1 GHz PC. A 2^17-point FFT at sample rate of 520 MHz is performed on the output signal of the PA. Figure 4.4 shows the PA output when correction is applied. The IMD level is approximately 43 dB down from the carriers. Therefore, the linearizer improves the IMD performance of the PA by approximately 23 dB. It can also be observed from Figure 4.4 the spectral

growth occurs using digital predistortion because the adjacent channel power is spread over a wider bandwidth.

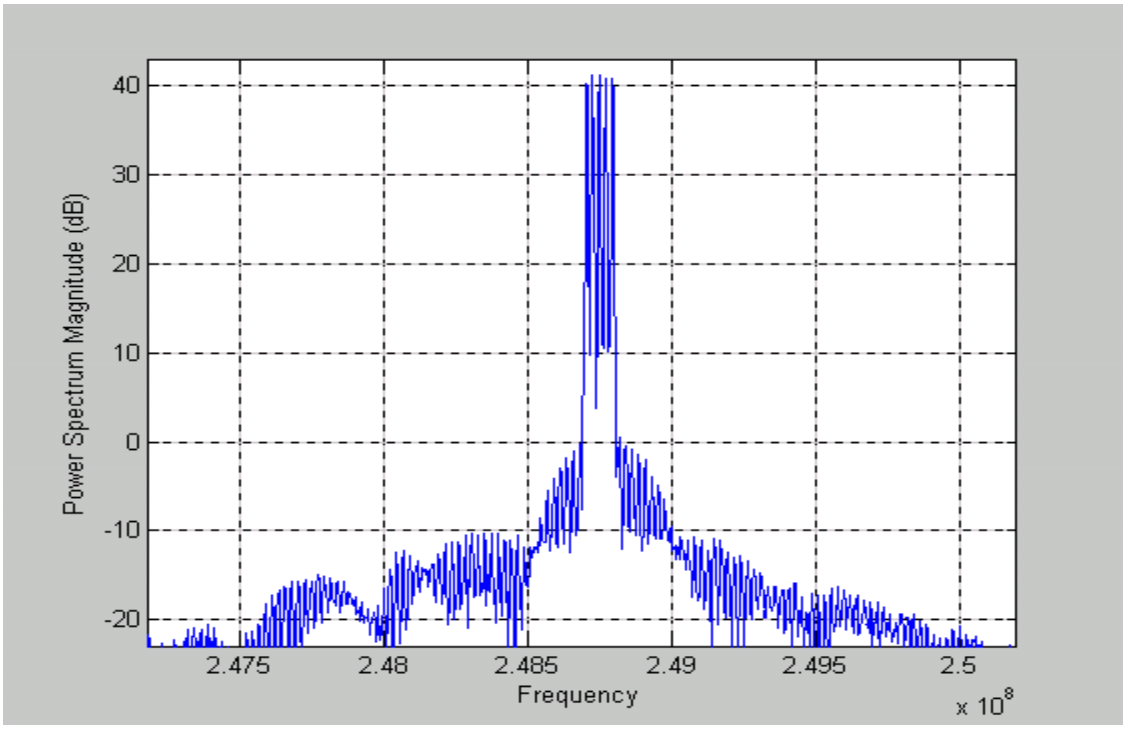

Figure 4.4 Power Amplifier Output with Correction

4.4 SIMULINK Model Simulation Results-30 MHz Signal Bandwidth

The tone generation is configured to generate 10 complex tones centered at baseband occupying approximately 30MHz of bandwidth with peak to average ratio of 10 dB. The input to the PA is scaled to operate the PA at the nominal power level of 38dBm. The SIMULINK model is operated in open loop so that the PA is not linearized. A 2^17-point FFT at sample rate of 520MHz is performed on the output signal of the PA. Figure 4.5 shows PA output with no correction applied. The IMD level are approximately 32 dB down from the carriers.

Figure 4.6 shows that when the PA is operated in the linear region the input and the output of the PA are matched. However, during peaks the input and PA output deviate as shown by the error signal, because the PA is being operated in its compression region so the PA output compressed. The distortion is also produced by the phase non-linearity in the PA as shown by Figure 4.7 the phase response of the PA. The distortion produced by this loss of gain and phase linearity is evident when FFT of the PA output is performed as shown by Figure 4.5.

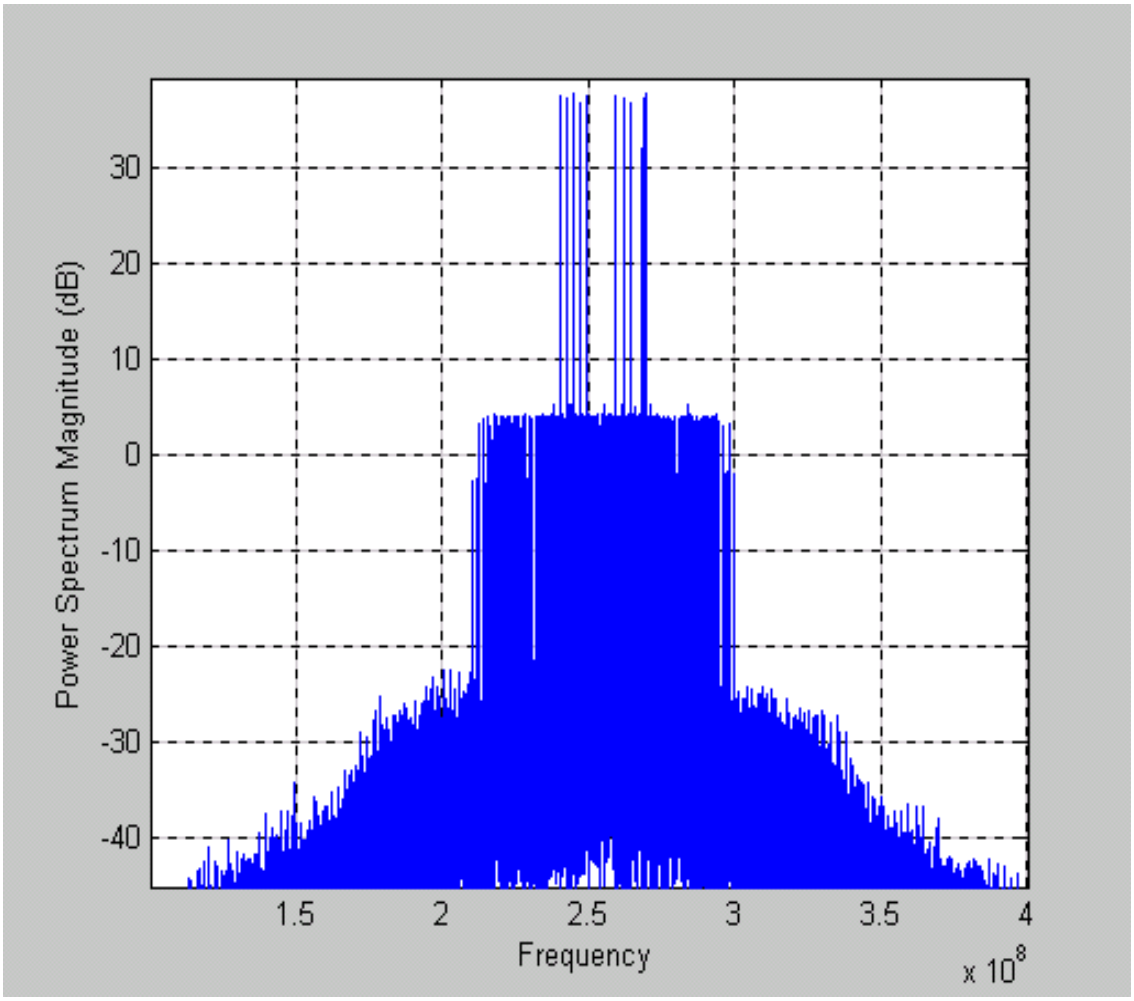

Figure 4.5 Power Amplifier Output without Correction

The SIMULINK model is now operated in closed loop and the PA is allowed to be linearized by predistorting the drive to the PA via the adaptation tables. The simulation was run for 20 seconds. A 2^17-point FFT at sample rate of 520 MHz is performed on the output signal of the PA. Figure 4.8 shows the PA output when correction is applied. The IMD level are approximately 70 dB down from the carriers. Therefore, the linearizer improves the IMD performance of the PA by approximately 40 dB. The PA is operated at lower output power because the PAR of the input signal is approximately 3dB higher, and since PA cannot be driven above hard saturation level, the input the PA has to be backed off. Thus with higher back-off the PA is operated in linear region most of the time thus the IMD level are lower. The disadvantage of operating the PA with higher back-off is that it degrades the efficiency of the PA. It can also be observed from Figure 4.8 the spectral growth occurs using digital pre-distortion because the adjacent channel power is spread over a wider bandwidth.

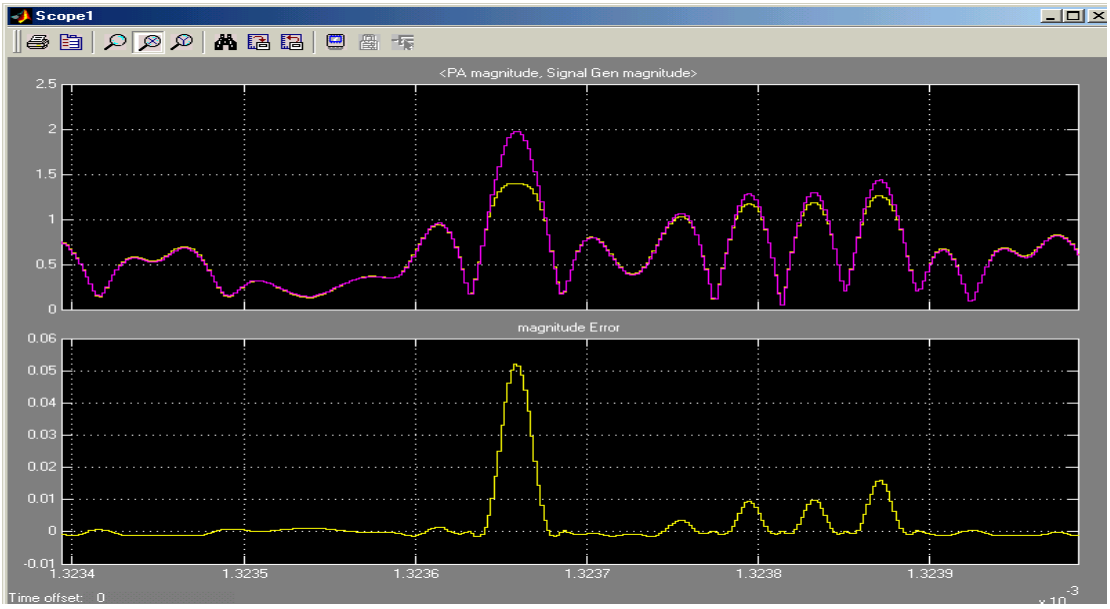

Figure 4.6 Power Amplifier Input and Output Magnitude without Correction

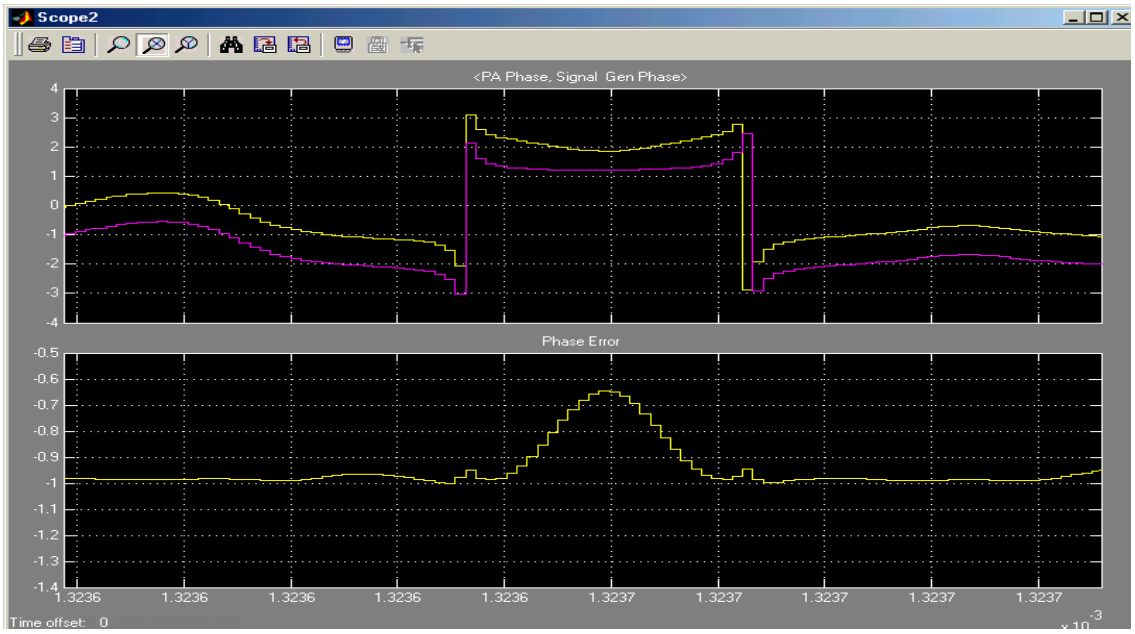

Figure 4.7 Power Amplifier Input and Output Phase without Correction

The AM/AM compression in the PA output during the peaks is compensated by gain expansion in gain table and AM/PM distortion is compensated by phase table as shown in Figure 4.10.

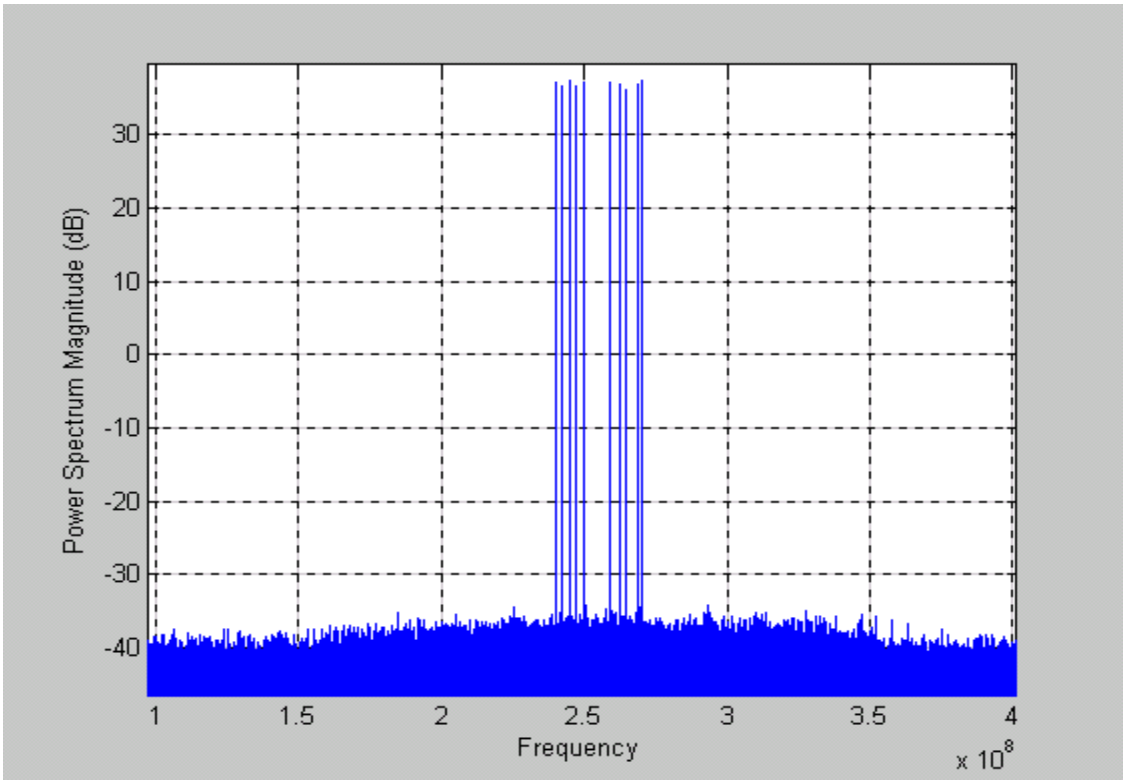

Figure 4.8 Power Amplifier Output with Correction

Figures 4.9 and 4.10 show that when the adaptation loop has converged the drive signal to the PA is distorted in manner which forces the PA magnitude and phase output to match magnitude and phase of the tone generator output. Close match between feedback and input signal results in greater improvement in the IMD performance of the PA.

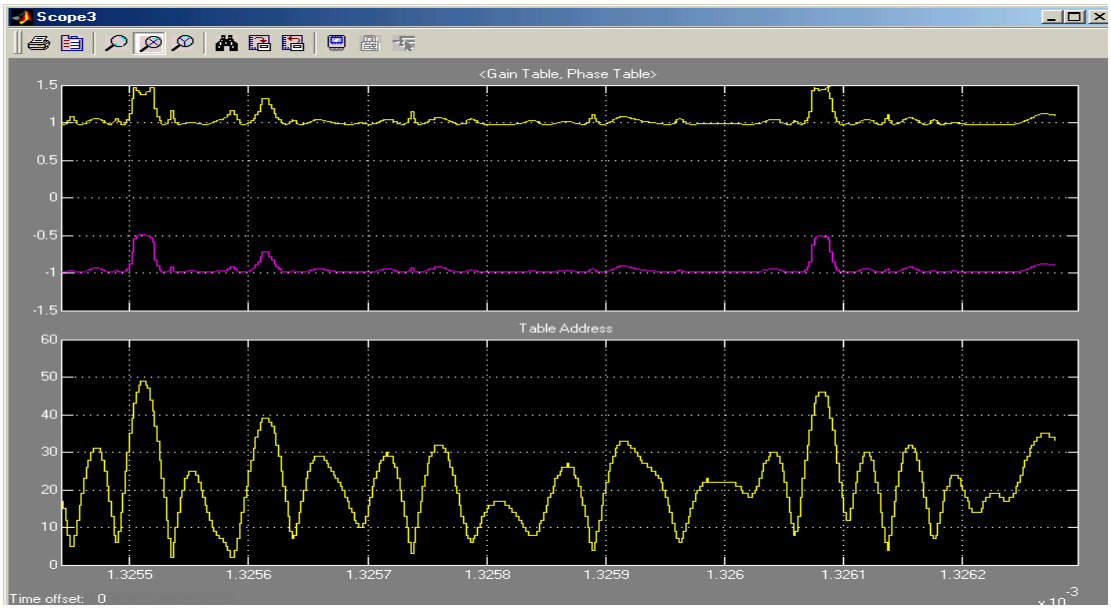

Figure 4.9 Adaptation Table Gain and Phase Entries when Loop Converges

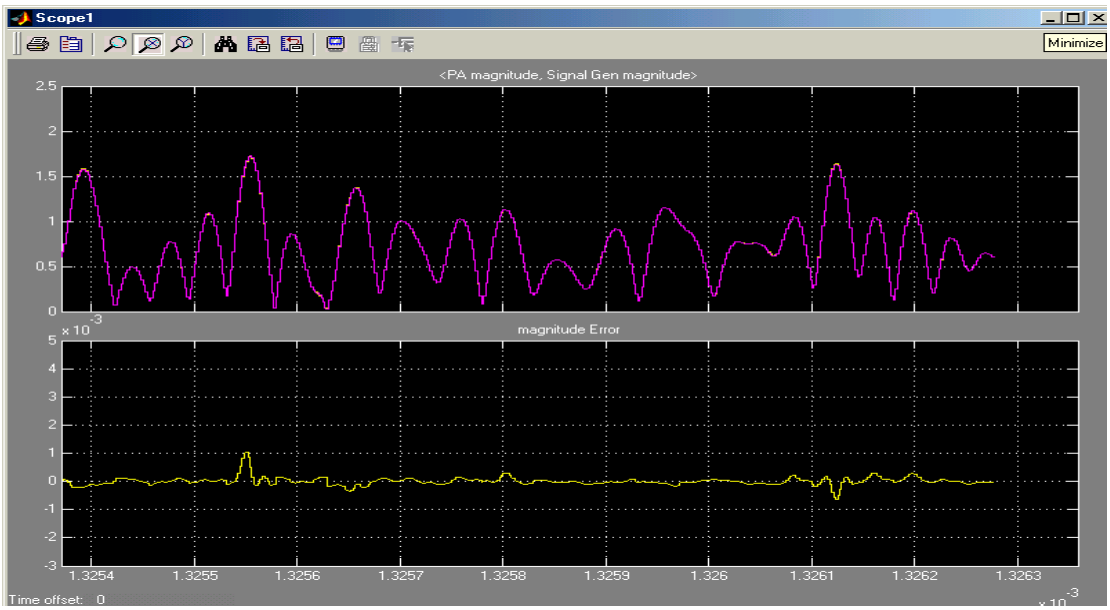

Figure 4.10 Power Amplifier Input and Output Magnitude when the Loop Converges

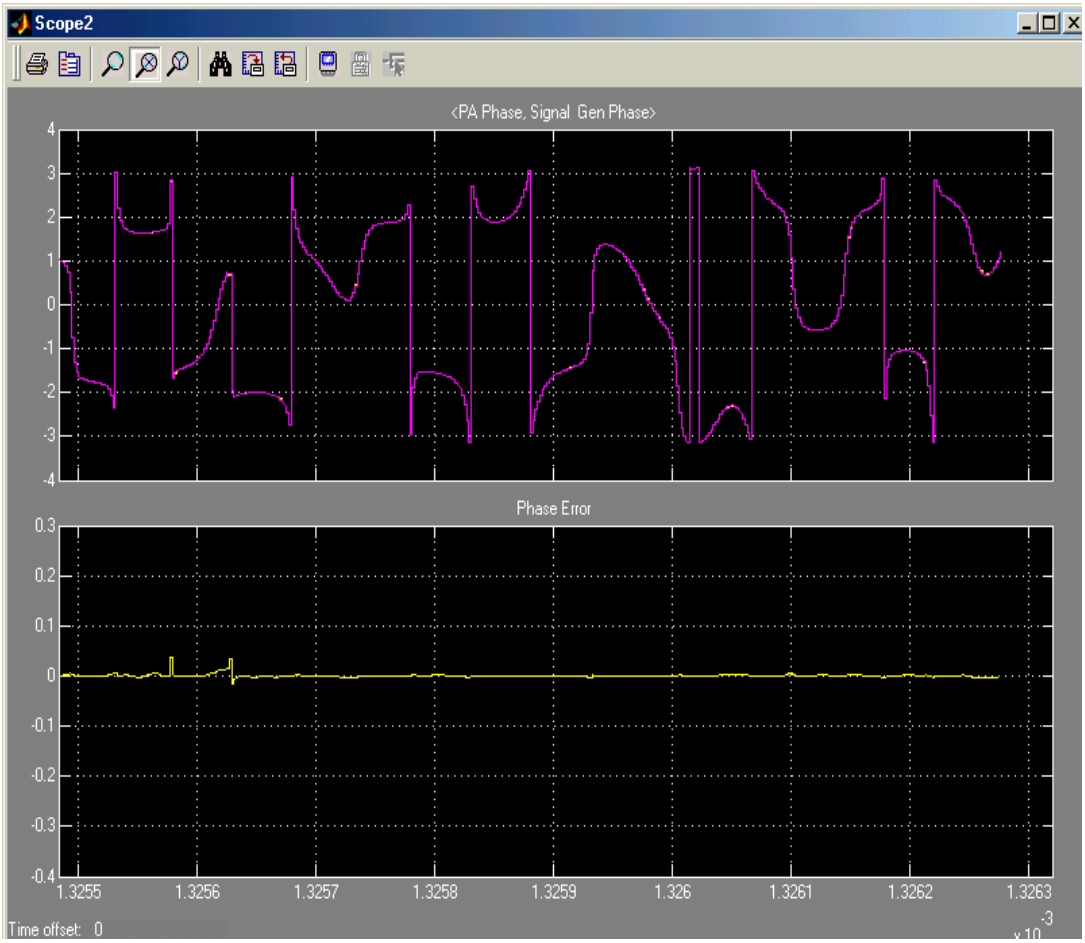

Figure 4.11 Power Amplifier Input and Output Phase when the Loop Converges

4.5 Sensitivity Analysis

Sensitivity analysis was performed to determine which parameters of the adaptive digital predistortion system improves or degrades the IMD performance of the PA [24].

4.5.1 Sensitivity to Predistortion Signal Bandwidth

The forward predistortion bandwidth (BW) is adjusted in steps of 1X signal bandwidth, 2 X signal bandwidth and 4X signal bandwidth. Figure 4.12 shows the correction achieved after 0.3 seconds of adaptation varies by more than 30 dB. The reason for the variation in correction achieved is because as wider bandwidth predistorted signal reaches the PA it

cancels more of the distortion generated by the PA, therefore greater improvement in IMD performance.

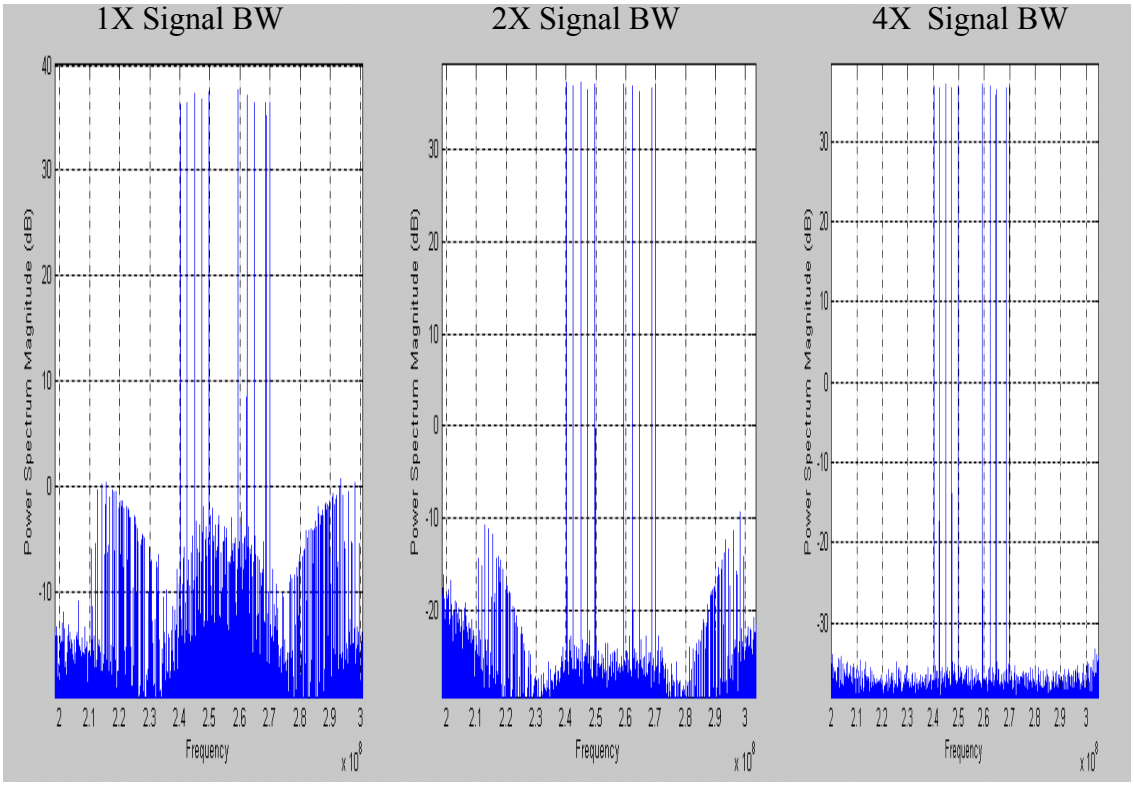

Figure 4.12 Sensitivity to Predistortion Signal Bandwidth

4.5.2 Sensitivity to Feedback Signal Bandwidth

The sensitivity to feedback signal bandwidth (BW) was tested by setting the BW to 1X signal bandwidth and 2X signal bandwidth. Figure 4.13 shows after 0.3 seconds of adaptation, an additional 10 dB of correction is achieved with feedback BW set to 2X signal BW. It should be noted that no further correction is obtained when the feedback BW is increased beyond 2X signal BW. The reason for additional correction is that the pre-distorter is able to correct for the distortion outside the signal bandwidth of interest, thereby reducing the distortion products generated in band.

Feedback BW = 1X Signal BW Feedback BW = 2X Signal BW

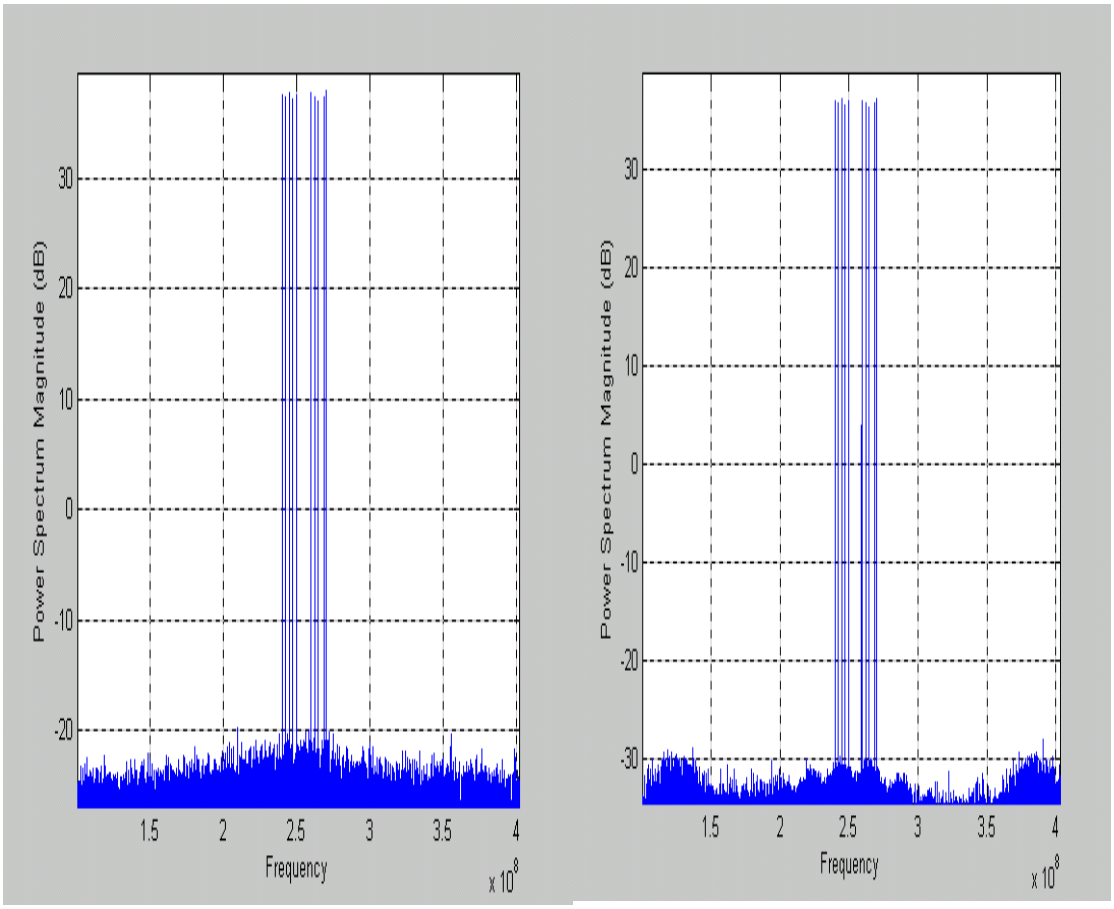

Figure 4.13 Sensitivity to Feedback Signal Bandwidth

4.5.3 Adaptation Time versus Table Size

The adaptation table size is adjusted in steps of 64 entries, 512 entries and 2048 entries. Figure 4.14 shows the correction achieved after 0.3 seconds of adaptation varies by more than 20 dB. The reason for the decrease in correction with increase in table size is because more entries need to converge therefore, longer adaptation time is required.

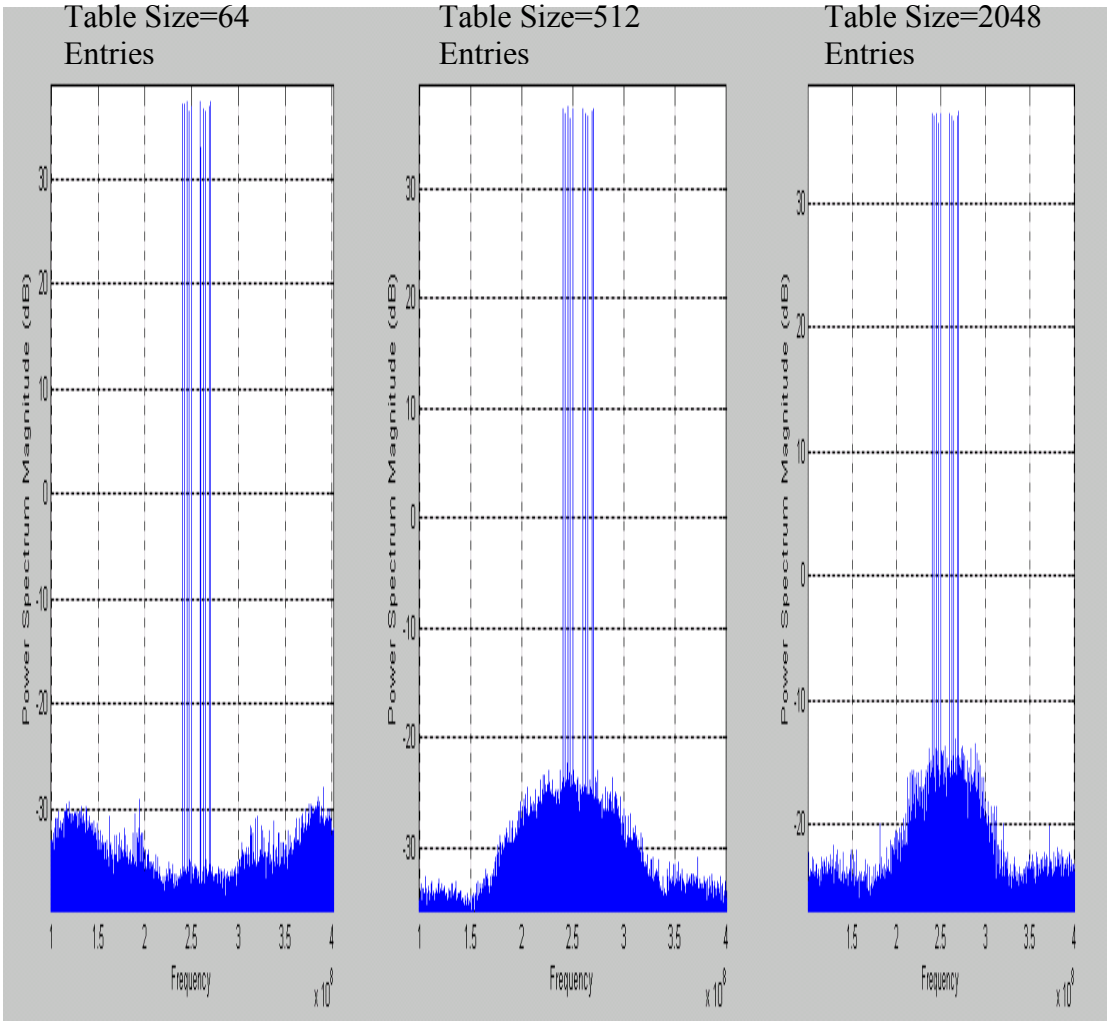

Figure 4.14 Sensitivity to Table Size

The adaptation table size is set to 512 entries and loop is allowed to adapt for 20 seconds. Figure 4.15 shows the correction achieved after 20 seconds of adaptation is similar to 64 entry adaptation table. Therefore, 64 entry appears to give the best results in terms of adaptation time and correction achieved.

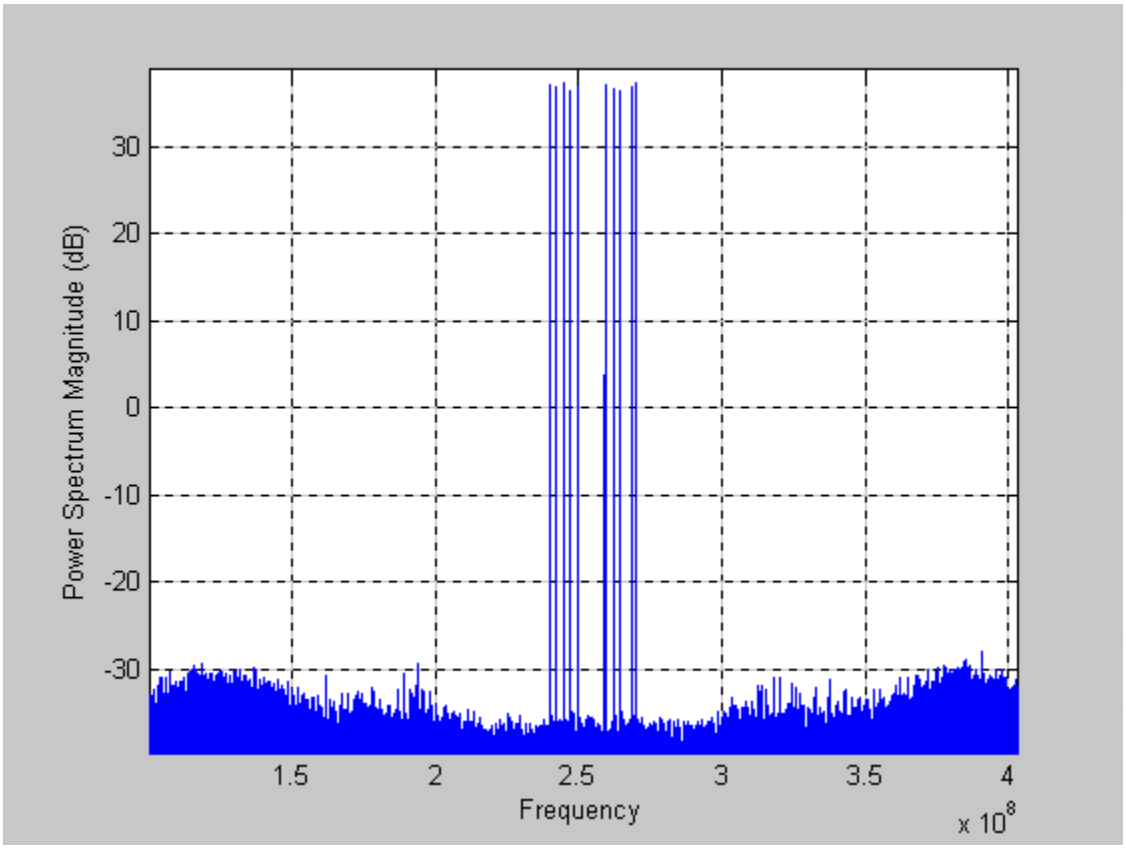

Figure 4.15 512 Entry Table Size, Adaptation Time 20 Seconds

4.5.4 Sensitivity to Time Alignment

The simulation model is a sample-based system. There is integer number of delays between the input signal from the tone generator and the feedback from the PA. In a real system delay will not be a integer number of samples. The impact on convergence if the input and feedback are misaligned by one sample is shown in Figure 4.16.

The results indicate that misalignment by one sample degrades the IMD performance by approximately 15 dB. It also found that the loop fail to converge if the misalignment was greater than one sample. The literature survey has indicated the alignment should be within 1/64 of sample period to maintain sufficient linearity improvement.

Input and Feedback Time Aligned

Input and Feedback not Aligned By 1 Sample

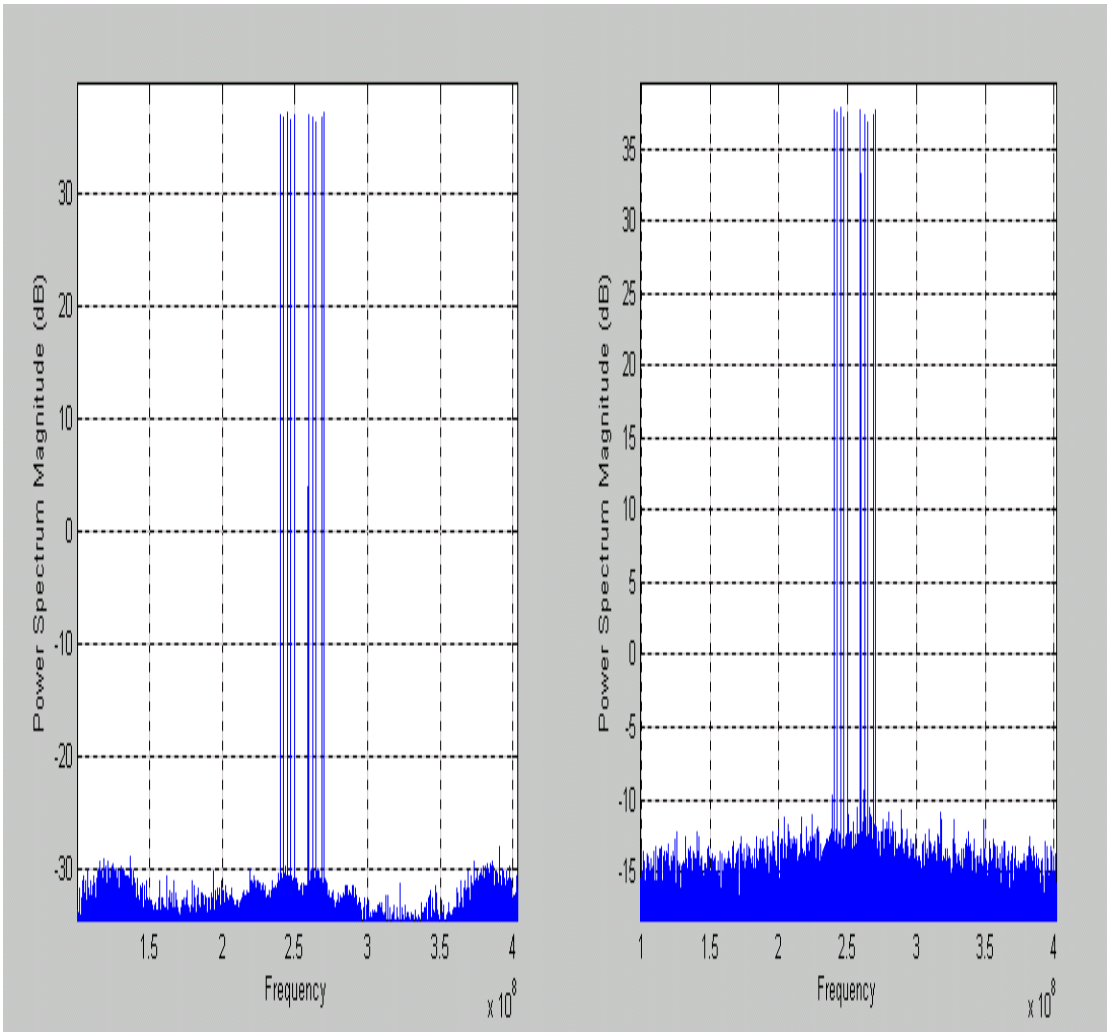

Figure 4.16 Sensitivity to Input and Feedback Alignment

4.5.5 Sensitivity to Addressing Scheme

The look table is addressed by linear method in which the magnitude of the source signal is used, so the error is distributed through out the table. However, since majority of distortion is caused when the amplifier is operated close to the compression region. Then power method of addressing can be used, which involves using the square of the input signal amplitude. This concentrates the table entries to high amplitudes thus making low amplitude coarse. Figure 4.17 shows that power method of addressing leads to an approximately 3 dB of additional improvement in the IMD performance of the PA.

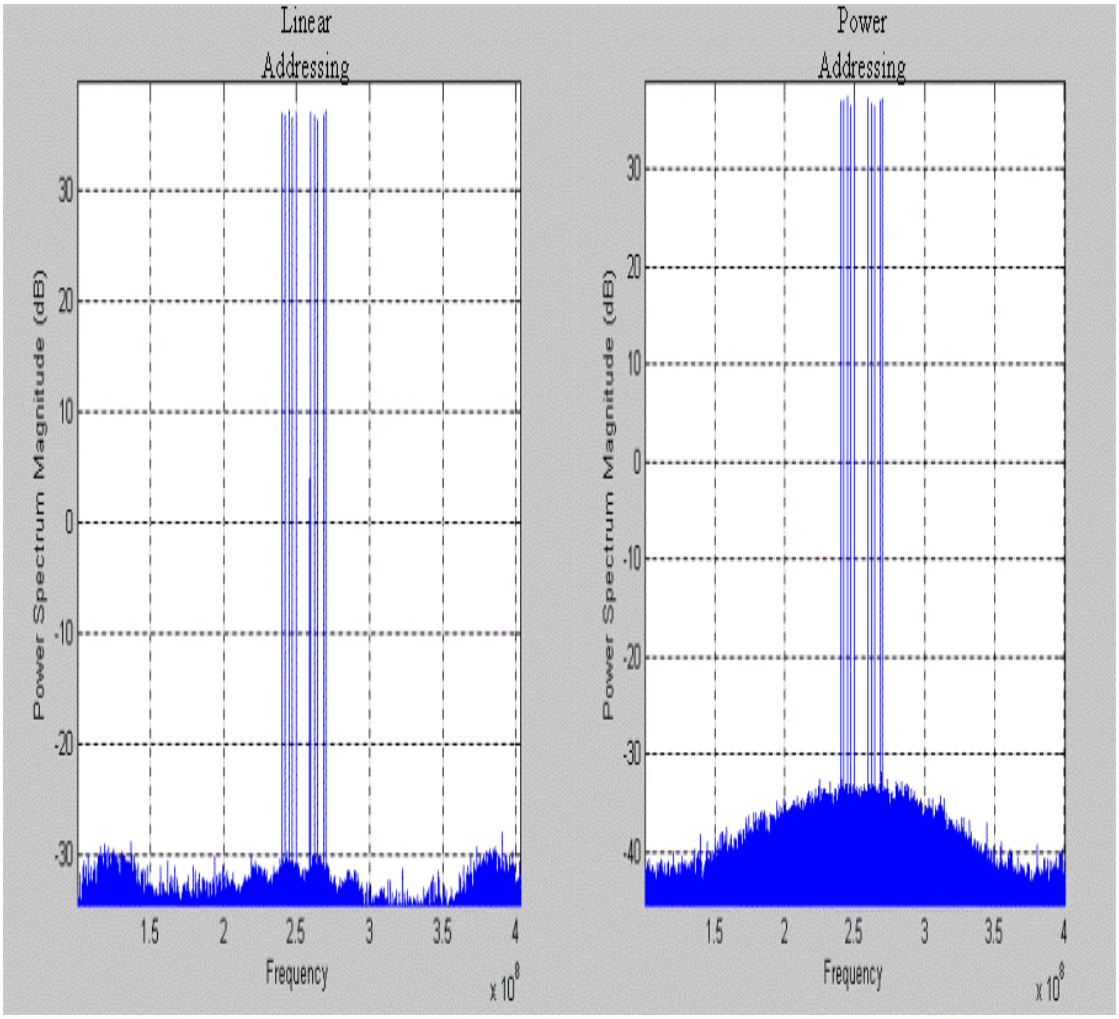

Figure 4.17 Sensitivity to Linear and Power Addressing

5.0 PREDISTORTER HARDWARE DEMONSTRATION SETUP

5.1 Adaptive Digital Predistortion Hardware Demonstration Setup

The breadboard OPTUS C1 UHF satellite Transponder hardware used for demonstration setup was reconfigured so that the adaptive digital predistortion simulation model developed in SIMULINK could be implemented in hardware.

A Down-Conversion module was added to existing setup which included Digital Filter Module, Up-Conversion Module and a Spacecraft Interface Module as shown in Figure 5.1.

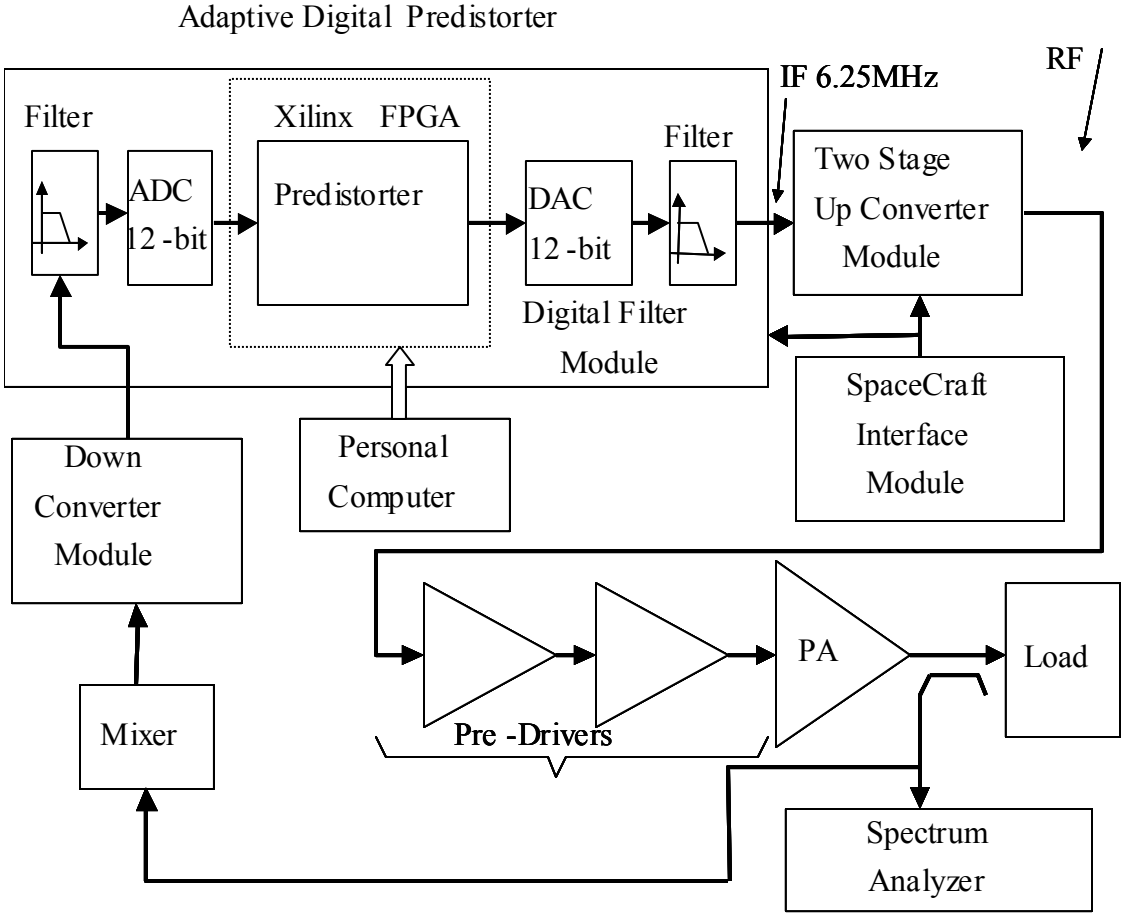

Figure 5.1 Adaptive Digital Predistorter Hardware Setup

Adaptive digital predistorter algorithm in the SIMULINK model was implemented in FPGA using VHDL. The rectangular to polar conversion was implemented using CORDIC algorithm and $\alpha Max + \beta Min$ method was used to implement the square root function required to calculate the magnitude of the input signal. The limitation in the available resources and operating speed of the FPGA meant that all the VHDL process which needed to implement CORDIC algorithm had to share this resource. The sharing of the resources meant that the table could not be updated on a sample-by-sample basis. Each point in the table took about 150 msec to update, therefore the loop failed to converge.

Since the requirement was to demonstrate correction over 30 MHz of signal bandwidth and the OPTUS hardware had bandwidth of only 100 KHz. Therefore it was decided not to expend any further effort on trying to get the adaptive loop to converge on OPTUS hardware. A new hardware demonstration setup was built to verify the simulation results and show that the digital predistorter can linearize Raytheon power amplifier over a 30 MHz of signal bandwidth and achieve greater than 20 dB of improvement in the IMD performance.

The block diagram of the hardware setup is shown in Figure 5.1. It consists of Intersil corporation's ISL5239 Predistortion Linearizer evaluation board and ISL5217 Signal Generation board, Sirenza STQ-1016 Analog Quadrature Modulator (AQM), a non-linear amplifier chain constructed from laboratory power amplifiers and attenuators, and Raytheon's dual, push-pull, class-AB, UHF power amplifier, Analog Quadrature Demodulator (AQD), Dual ADC AD1031 evaluation Board, 60MHz low pass filters and a personal computer (PC) with an USB interface to ISL5239 Pre-distortion Linearizer evaluation board and printer port interface to ISL5217 Signal Generation board. The picture of the actual hardware setup is shown in Figure 5.2.

The ISL5217 is a quad programmable up-converter (QPUC) evaluation board which is configured via PC parallel port. Stimulus pattern is loaded into external RAM and QPUC converts into modulated/frequency translated digital samples. The digital samples are fed to the ISL5239 evaluation board. The ISL5239 Pre-Distortion Linearizer is designed for linearizing memory-less Power Amplifier. This part has many features, however only the features used for the demonstration set-up will be described. The main feature of the part is that it utilizes two look-up table based algorithms for the pre-distortion correction. The table can be programmed to be addressed by input linear magnitude, input linear power or log of power. The output of the table has I/Q balance correction and DC offset correction applied to compensate for gain/phase imperfections in the external AQM. This part also has input capture memory and feedback capture memory which store input signal and PA output sample which are used by the off line processor to compute the correction coefficients for the look-up tables. In the set-up the capture memory are accessed by the PC via the USB port. The I/Q pre-distorted base-band digital outputs from the ISL5239 are fed to two 14-bits DACs. The analog outputs from the DACs are filtered and fed to an external AQM. The AQM converts the quadrature analog baseband

outputs from the evaluation board to the RF frequency set by the carrier input frequency from the signal generator.

The output of the AQM is filtered to suppress any images. Pre-amplifiers follow the filter to provide gain to boost the RF signal to sufficient levels to drive the PA. The pre-amplifiers are chosen have sufficient dynamic range and linearity so as not to distort the RF drive signal. A variable attenuator is included in the drive path for manually controlling PA operating point.

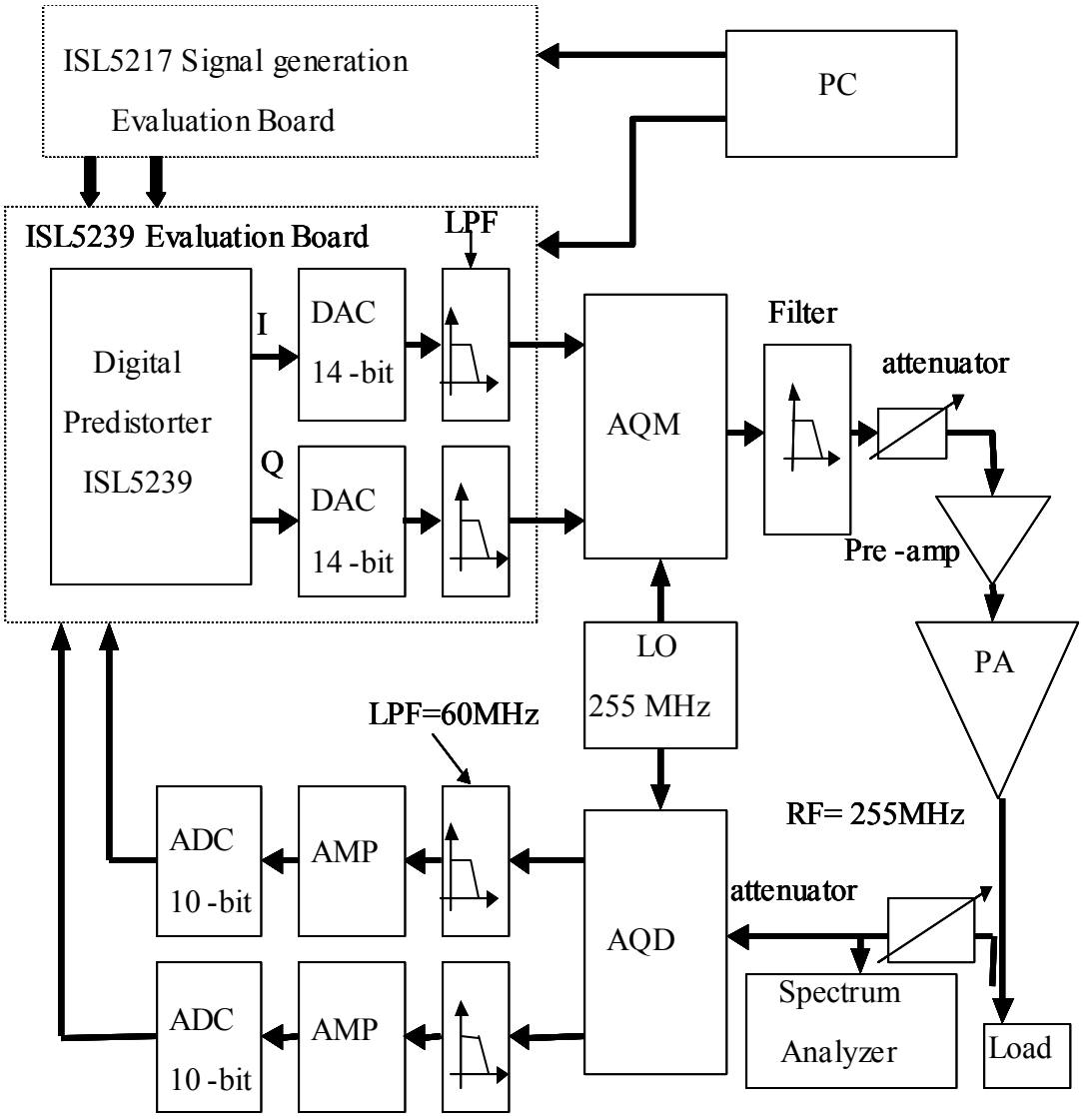

Figure 5.2 Adaptive Digital Predistorter using ISL5239

The PA output path involves a load and attenuators for attenuation of the RF output for measurement (spectrum analyzer) and driving analog quadrature demodulator (AQD). AQD down-converts the RF to I/Q base-band. The analog I/Q outputs are filtered to reject the images and fed to linear amplifiers. The amplifiers are needed to boost the baseband signals to sufficient levels to drive the ADC output to full scale. The ADC outputs are feedback to the capture memory in the ISL5239.

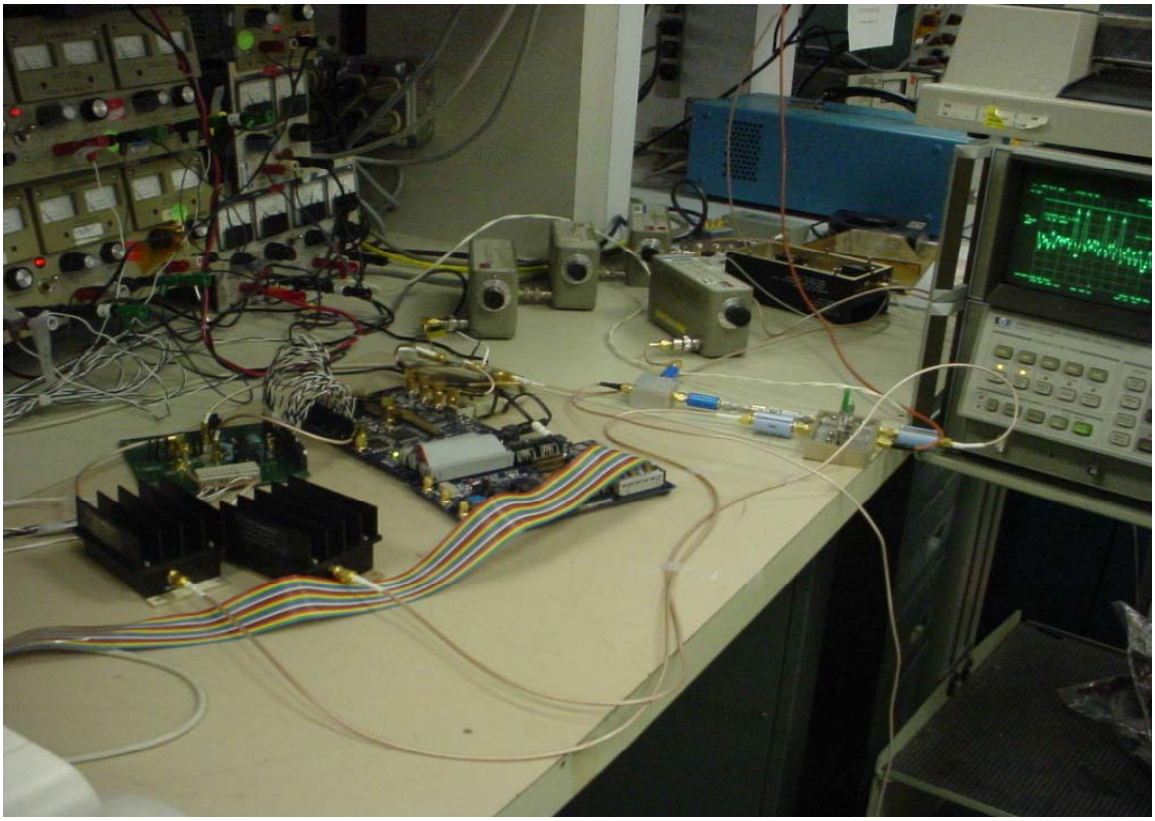

Figure 5.2 Photograph of Adaptive Digital Predistorter using ISL5239

The ISL5239 evaluation board is configured and controlled by the PC via the USB port. The MATLAB files supplied with evaluation board ran on the PC and allow PA gain and phase to be characterized and create inverse transfer function, which is loaded in the look-up tables. Prior to running the PA linearizing algorithm, the ISL5217 QPUC evaluation board is configured to output 30 MHz wide muticarrier CDMA2000 signal. The look-up table in ISL2539 is set to bypass mode and undistorted stimulus is outputted to the PA. The I/Q imbalances and DC offset circuits in the ISL5239 are adjusted via MATLAB script to compensate for imbalance in the AQM. The attenuator in the forward path is adjusted to set the operating point of the PA followed by adjusting the attenuator in the feedback path. The ADC data is retrieved from the capture memory of ISL5239

and analyzed to ensure that ADC is not saturating and that there at least 3 dB of headroom.

The adaptive algorithm in MATLAB is activated which performs the functions described below for each iteration. The input and feedback capture memories are triggered to capture input and feedback samples. The input and feedback samples are interpolated and the magnitudes are aligned in time using cross-correlation command. The aligned data is scaled to minimize the error for the samples within the linear region of the PA. Amplitude and phase error between input and output samples is calculated. A window is used to weight the error as a function of the amplitude. The new update values for the look-up table are function of previous LUT values and new calculated LUT values. To ensure all LUT addresses are updated with new correction data, a polynomial fit is applied. The process described for updating the LUT is repeated until no further correction can be observed.

5.2 Adaptive Predistorter Correction Results for 30 MHz Signal Bandwidth

Initially the PA was operated to give average power of 8 Watts with input signal having peak-to-average ratio (PAR) of approximately 0 dB. The results show (see Figure 5.3) that the adaptive digital predistorter is able to improve the IMD performance of the PA by approximately 15dB. The in-band IMD was 50dB down from the carriers. However, out of band IMD is only 40 dB down but this can be improved by having a 30 MHz band pass filter at the output of the PA.

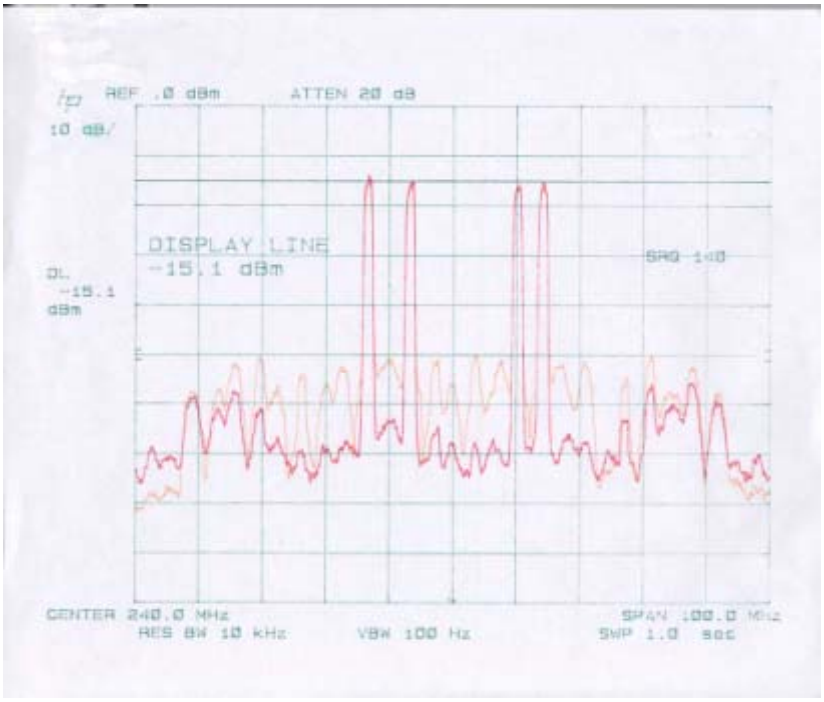

Figure 5.3 Class A/B PA Output Uncorrected and Corrected @ 8 Watts

The PA is now operated at an average power of 12 Watts and the results show (see Figure 5.4) that the predistorter was only able to improve the IMD performance of the PA by approximately 10 dB and in-band IMD were only 35 dB down from the carriers.

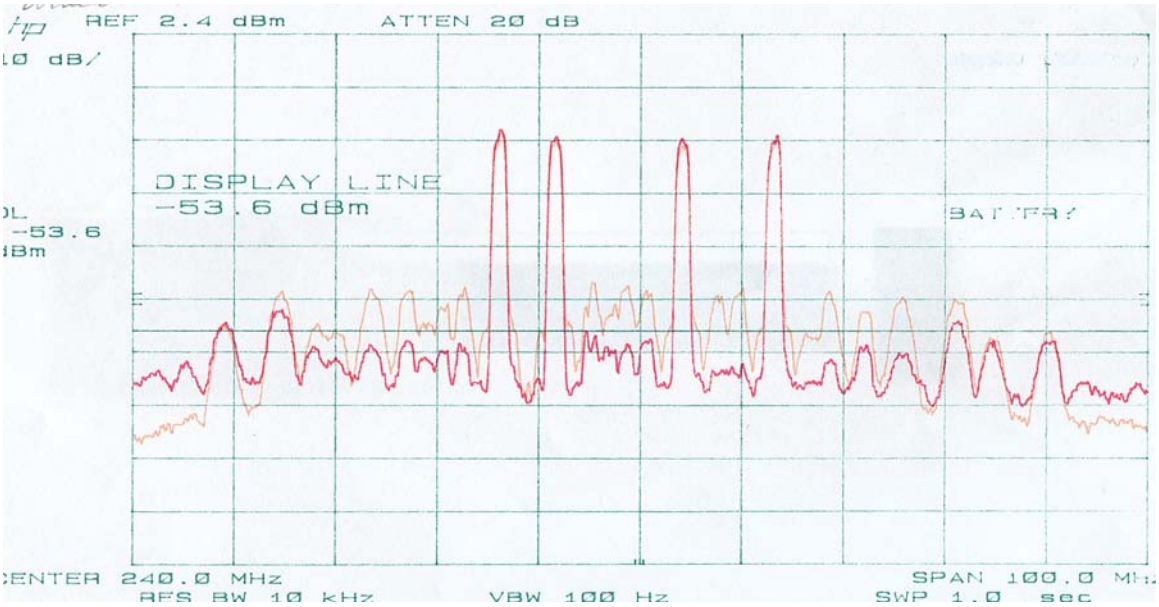

Figure 5.4 Class A/B PA Output Uncorrected and Corrected @ 12 Watts

In both cases, the amount of correction obtained did not match the simulation results. To determine the reason for poor performance of the predistorter, the bandwidth of the input signal was reduced to 7 MHz and again, it can be seen from Figure 5.5 that the predistorter was only able to reduce the IMD by 10 dB with and in-band IMD 38 dB down from the carriers.

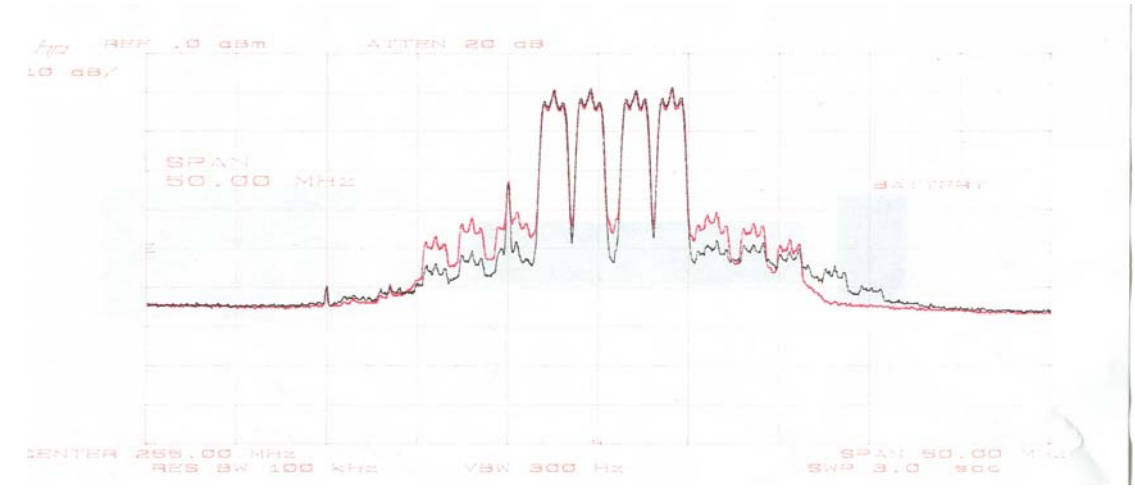

Figure 5.5 Class A/B PA Output Uncorrected and Corrected @ 7 MHz Signal BW

The next test was to substitute the Raytheon class A/B amplifier with a laboratory Class A amplifier. This time, the predistorter was able to drive the in-band IMD terms to the noise floor as shown in Figure 5.6. The in-band IMD is more than 55 dB down from the carriers. The spurs at 250/240 MHz should be ignored because they are due to the digital clock on ISL5239 evaluation board and LO leakage from the AQM.

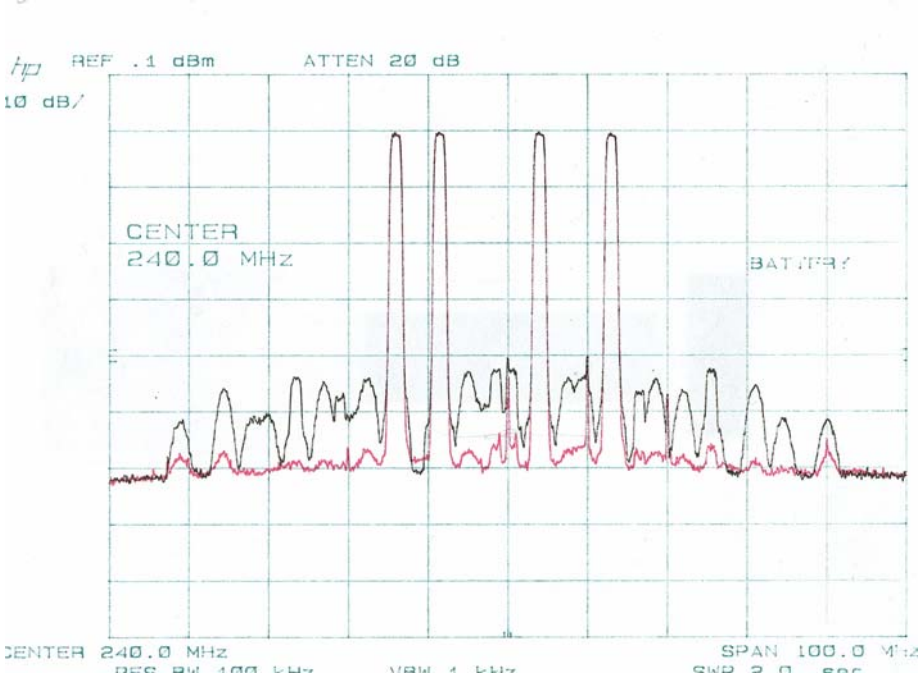

Figure 5.6 Class A PA Output Uncorrected and Corrected @ 20 Watts

The Class A power amplifier input and output amplitude and phase were checked after the adaptive loop had converged. It can be seen from Figure 5.7 that input and output amplitudes and phases are in agreement.

The input and PA output amplitude and phase for Raytheon Class A/B power amplifier were checked after the adaptive loop had converged. It can be seen from Figure 5.8 that input and output phase have not converged. Furthermore, the amplitude curve shows that when the input amplitude is increasing the power amplifier output is in slight compression and as the input is decreasing the power amplifier output has slight expansion, similarly, the unwrapped phase plot show that the power amplifier output phase is different for increasing and decreasing amplitude. Therefore, for the same input amplitude, the power amplifier distortion tables have to have different values, depending on whether amplitude is rising or falling. This hysteresis indicates that power amplifier has some type of memory effect.

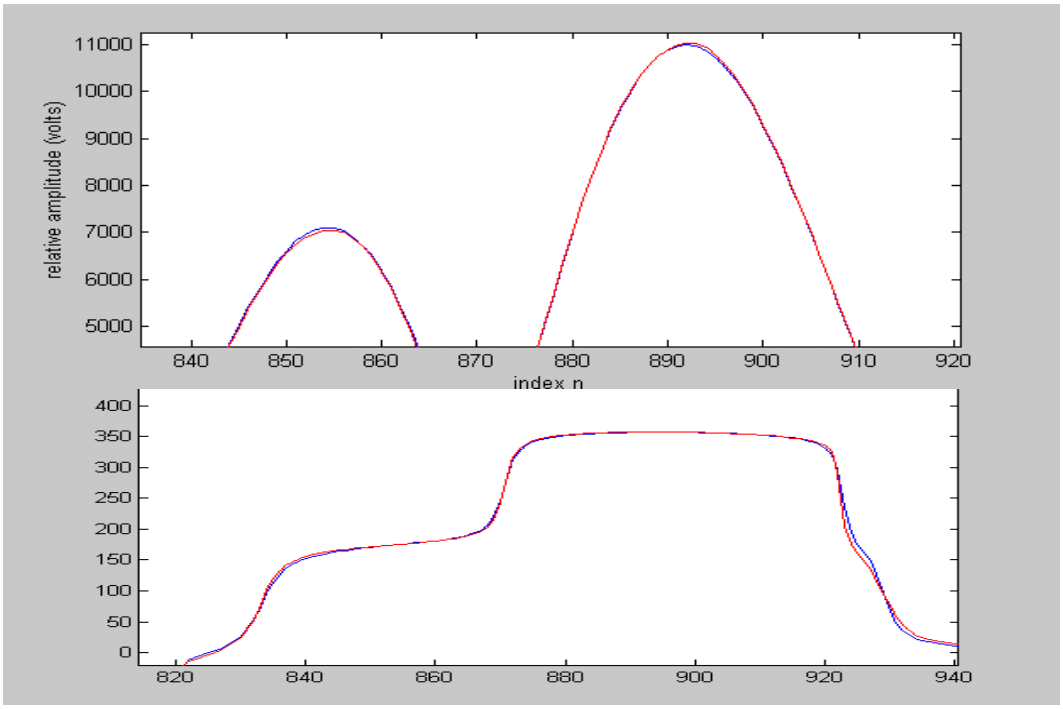

Figure 5.7 Class A PA Input/Output- Amplitude and Phase after Convergence

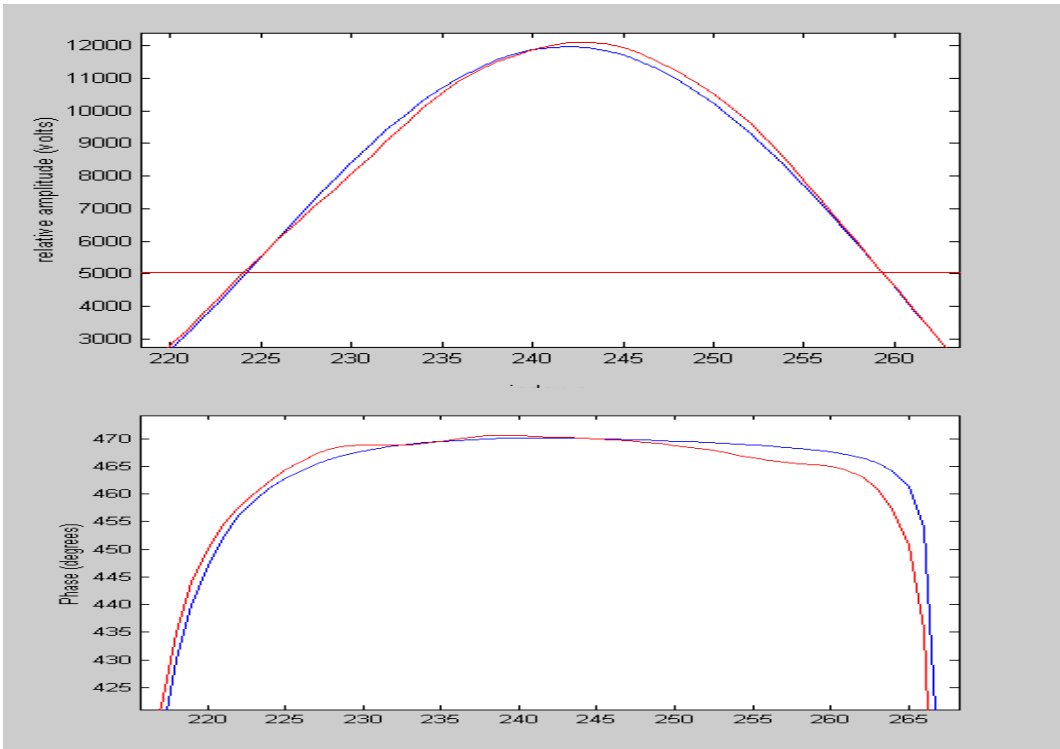

Figure 5.8 Class A/B PA Input/Output- Amplitude and Phase after Convergence

5.3 Reasons for the Poor Performance of Adaptive Predistorter

The memoryless predistorter can be viewed as canceling distorting components and the amount of IMD reduction is proportional to the accuracy of canceling components. The IMDs generated by the power amplifier are viewed as static. The literature search shows that as bandwidth of the signal and power handling capability of the power amplifier is increased, the IMD components generated by the power amplifier are not constant but vary as a function amplitude and frequency. Therefore, memoryless predistorter has insufficient cancellation as shown in Figures 5.7 and 5.8, resulting in poor IMD performance as shown in Figure 5.4. Another simple technique employed to determine if the power amplifiers has memory is to drive it with Sync pulses and measure its response. First a laboratory Class A amplifier is driven with Sync pulses and its response is shown in figure 5.9. Next, the Raytheon Class A/B amplifier is exercised with Sync pulses and its response is shown in figure 5.10.

The Class A PA response to Sync pulse shows that it is symmetrical, where as Class A/B PA's response is asymmetrical. The asymmetries in lower and upper sidebands come from memory effects in the power amplifier. The asymmetrical IMD performance of power amplifier has been a topic of several studies over the last few years. It has been reported the IMD performance of the Bipolar Junction Transistor (BJT) power amplifier is dependent on the impedance presented to its base and collector terminals, at fundamental, harmonic and baseband frequencies. Another mechanism leading to changes in IMD performance is the temperature variations at the top of the semiconductor over the modulating signal bandwidth [29-32]. Both these mechanisms are termed memory effects in power amplifier.

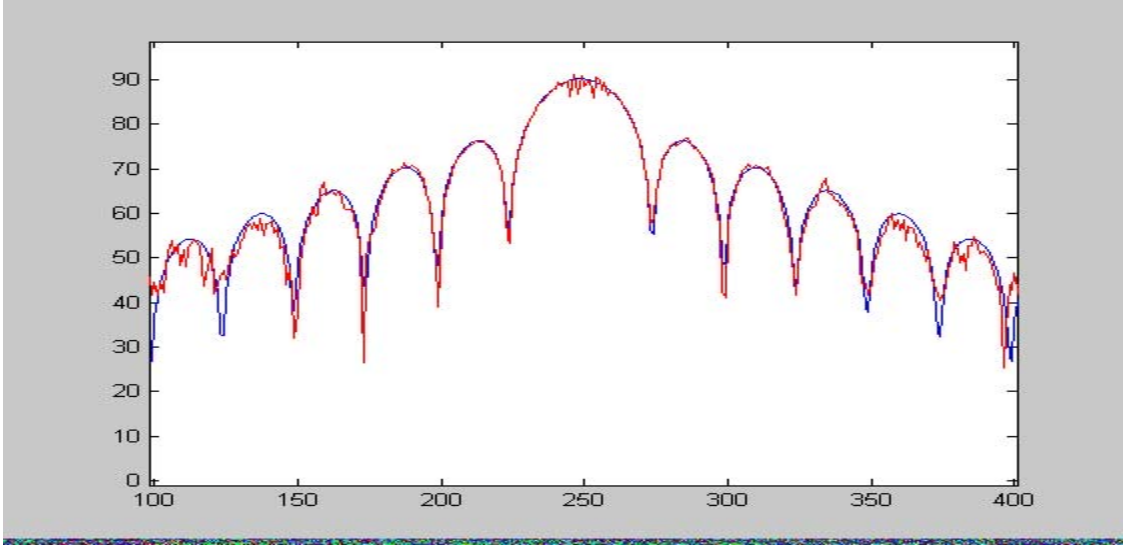

Figure 5.9 Class A PA Response to Sync Pulse

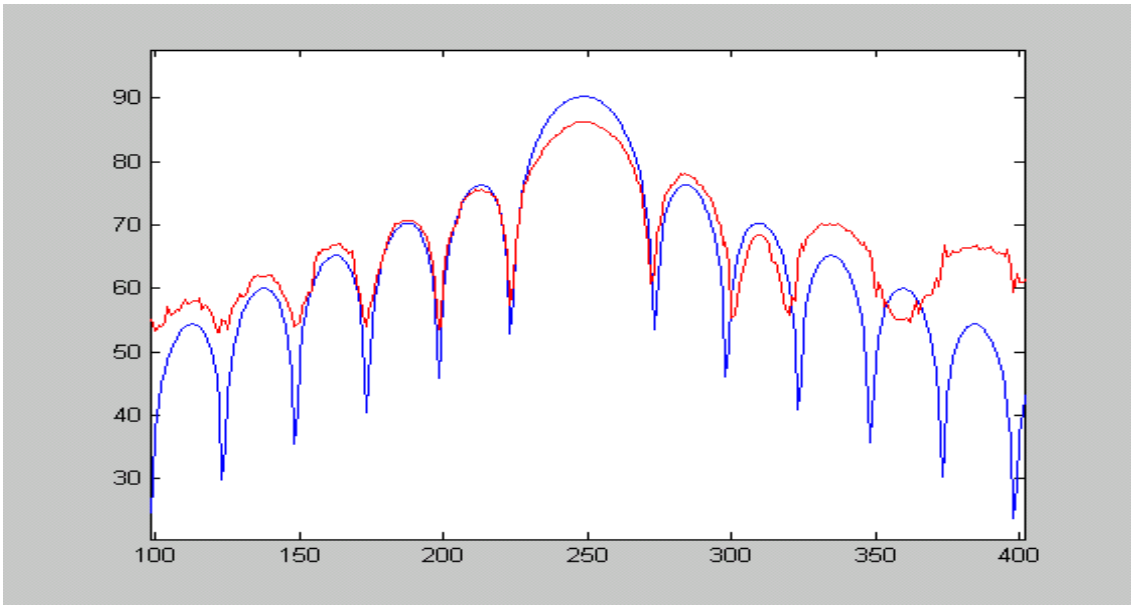

Figure 5.10 Class A/B PA Response to Sync Pulse

The memory effects not only exist in the power amplifier, but also in the RF filtering chain. Therefore, it is the total amount of memory in the system that will limit the amount correction achievable by the predistortion linearizer.

5.4 Memory Effects Classification

The memory effects are split into electrical and thermal memory. The electrical memory effects are caused by varying impedances at different modulation frequencies. The source impedance at the envelope frequency cannot be kept constant at very high modulation frequencies, therefore IMD sidebands will have different amplitude and phase distortion. Another electrical memory effect is resonance's in the source or load matching networks [31].

Thermal memory effects are caused by electro-thermal couplings which affect low modulation frequencies up to the megahertz range. The temperature variation caused by the dissipated power is determined by the thermal impedance. The thermal impedance in an active device is not just resistive, but forms a distributed lowpass filter with wide range of time constants [33].

5.4.1 Reducing Memory Effects

The memory effects in the Raytheon class A/B power amplifier were reduced by optimizing the source impedance, eliminating the resonance's, and adding additional decoupling on the power supply rails.

The predistorter was able to improve the IMD performance of the PA by approximately 10-15 dB and the in-band IMDs were now 42 dB down from the carriers. Therefore, low memory power amplifier's IMD performance was improved by an additional 4 dB, but still well short of the requirement of –52 dBc.

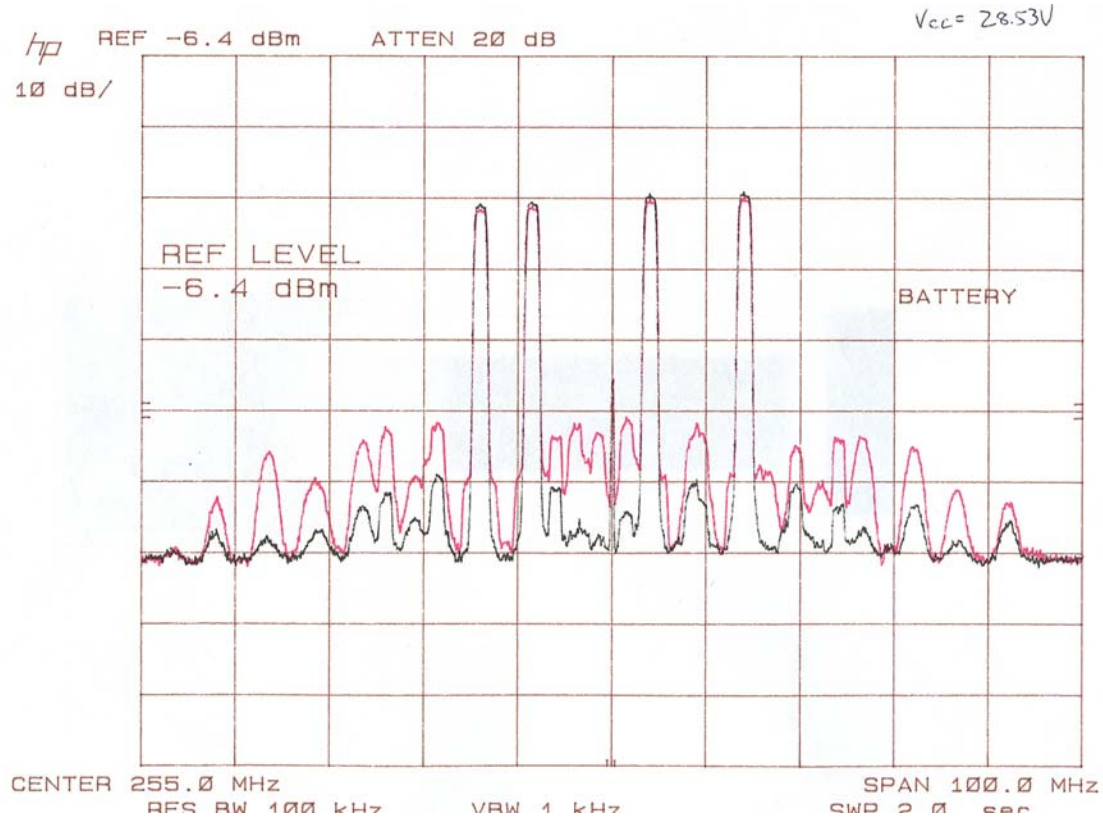

Figure 5.11 Class A/B Low Memory PA Output Uncorrected and Corrected @ 12W

Additional changes were made to the power amplifier design to reduce memory, but the memoryless digital predistorter was not able to make a noticeable improvement to the IMD performance of the power amplifier.

A two-tone setup as described by Vuolevi in [33] can be used to characterize the memory effect of the power amplifier. It was concluded that this characterization was not necessary because to have a large improvement in the IMD performance of a non-linear power amplifier with memory, its inverse must also be a non-linear system with memory.

5.5 Comparison of Hardware Model Results with SIMULINK Model Simulation Results

Table 5.1 SIMULINK Model Simulation and Memory-less Adaptive Predistorter Results

Correction Platform	Signal Bandwidth	Correction Achieved	Amplifier of Type
Non Adaptive predistortion	100 KHz	10 dB	Class AB
SIMULINK Model	100 KHz	23 dB	Class AB
Adaptive predistortion	5 MHZ	20 dB	Class A
Adaptive predistortion	5 MHZ	15 dB	Class AB
SIMULINK Model	5 MHZ	23dB	Class AB
Adaptive predistortion	30 MHZ	20 dB	Class A
Adaptive predistortion	30 MHZ	10 dB	Class AB
SIMULINK Model	30 MHz	40 dB	Class AB

The SIMULINK power amplifier model can be viewed as a memory-less model, because it is based on measured data at a single frequency. Therefore, the results from memory-less adaptive predistorter with only Class A power amplifier can be compared with the simulation results.

It can be observed from Table 5.1 that the SIMULINK model simulation results show much greater amount of correction then the correction achieved by memory-less adaptive predistorter with a Class A or a Class A/B power amplifier. However, it can be observed from Figure 5.6 that the memory-less adaptive predistorter is able cancel almost completely the IMD terms generated by Class A amplifier power. The limiting factor is the system noise floor which is masking the absolute amount of correction achievable with memory-less adaptive predistorter. Therefore, if the amount of noise in the system can be reduced, then the amount of correction achieved with memory-less predistorter with Class A power amplifier will be similar to the SIMULINK simulation results. The other major difference is that the up/down conversion paths in the actual system have imperfections which limits the amount of correction achieved. These imperfections have not included in the SIMULINK model because they are very complex to model.

6.0 PREDISTORTERS FOR POWER AMPLIFIERS WITH MEMORY

6.1 Adaptive Digital Predistorter for Power Amplifiers with Memory

The results of the memoryless predistorter indicate that memory effects in the power amplifier lead to significant decrease in IMD cancellation performance. Literature survey shows that a more complex digital predistorter can cancel the memory effects. The goal of this thesis was to show that digital predistorter could improve the linearity of the power amplifier, so that it meets the –52 dB IMD performance requirement. The ultimate goal is to design and build a power amplifier system which will not only meets the size, weight, power, efficiency and IMD performance requirements but can also be easily built. One important trade off is whether to use BJT or FET for the power amplifier. It has been shown by various researchers that FET amplifier have lower memory effects because of simpler biasing scheme [34]. Therefore, allowing a simpler adaptive memory digital predistorter to be implemented.

A nonlinear power amplifier with memory can be represented by Volterra series or linear time-invariant (LTI) system followed by a memoryless nonlinearity known as Hammerstein model or Nonlinear tapped delay line (NTDL).

6.2 Adaptive Volterra Predistorter

A truncated discrete time domain Volterra model for power amplifier has the form :

$$y(n) = h_0 + \sum_{k_i=0}^{m-1} h_i(k_i)x(n-k_i)$$

$$+ \sum_{k_i=0}^{m-1}\sum_{k_{2=0}}^{m-1} h_2(k_i,k_2)x(n-k_i)x(n-k_2) + ...$$

$$+ \sum_{k_i=0}^{m-1} ..... \sum_{k_p=0}^{m-1} h_p(k_i .....,k_p)x(n-k_i) .....x(n-k_p) \qquad (6.1)$$

where h_0 is a constant and $\{h_j(k_i,.....,k_j)$, are the set of jth-order Volterra kernel coefficients [35].

An adaptive Volterra predistorter uses an indirect learning architecture (see Figure 6.1) and consists of an estimator and a predistorter, and both are implemented using transveral

FIR filters. The estimator has an adaptive algorithm which estimates inverse nonlinear parameters of the power amplifier and updates the coefficients in the predistorter [36][37].
Literature shows that implementing Volterra predistorter is computationally intensive and in addition, an accurate inverse of Volterra system is difficult to obtain and the jth order inverse is only an approximation [38].

Zhu's [37] simulation for third order Volterra based linearizer shows about 10 dB improvements in the IMD performance of the power amplifier with the signal bandwidth of approximately 4 MHz. The reason for only a 10 dB improvement may be attributed to the fact that an exact inverse for Volterra model is difficult to attain.

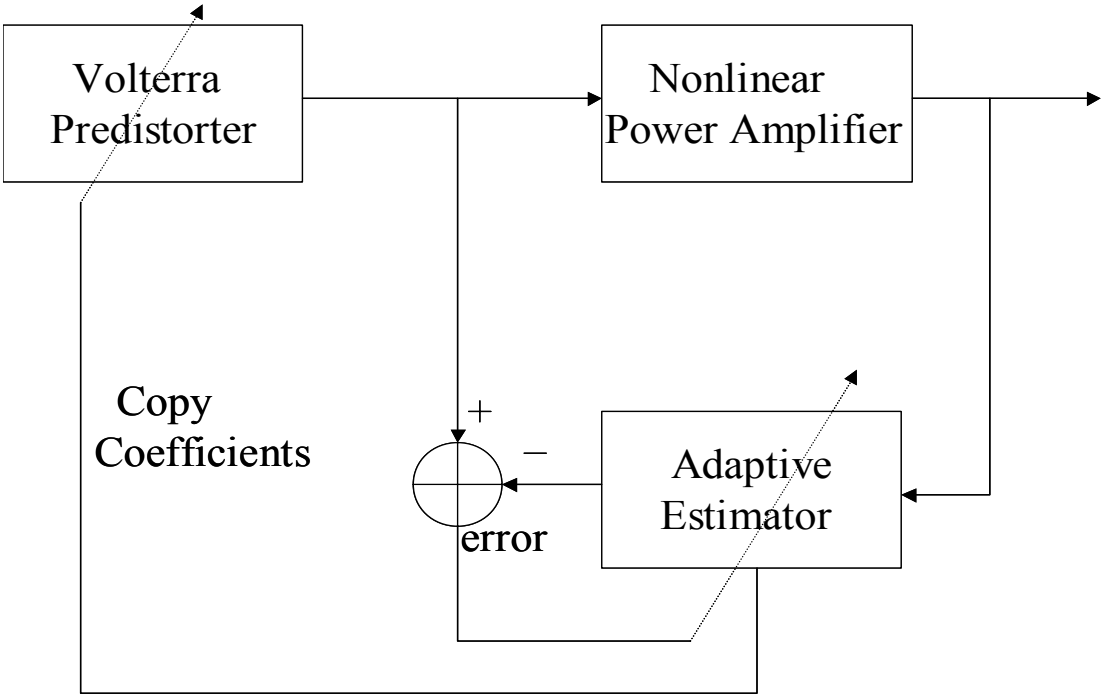

Figure 6.1 Adaptive Volterra Predistorter Architecture [37]

6.3 Hammerstein Memory Predistorter

Hammerstein predistorter model is represented by the equation in [39]:

$$z(n) = \sum_{p=1}^{p} a_p z(n-p) +$$

$$\sum_{q=0}^{Q} b_q \left(\sum_{k=0}^{(k-1)/2} c_{2k+1} y(n-p) \left| y(n-q) \right|^{2k} \right) \qquad (6.2)$$

where the y(n) is the input and z(n) is the output and the algorithm computes the a_p, b_q and c_{2k+1} coefficients. The adaptive Hammerstein predistorter uses an indirect learning architecture (see Figure 6.2) and consists of predistorter trainer and a predistorter, the LTI portion is implemented using a FIR filter. An iterative estimation algorithm in the predistorter trainer computes the inverse model of power amplifier and copies the coefficients in the predistorter in the forward path until loop converges.

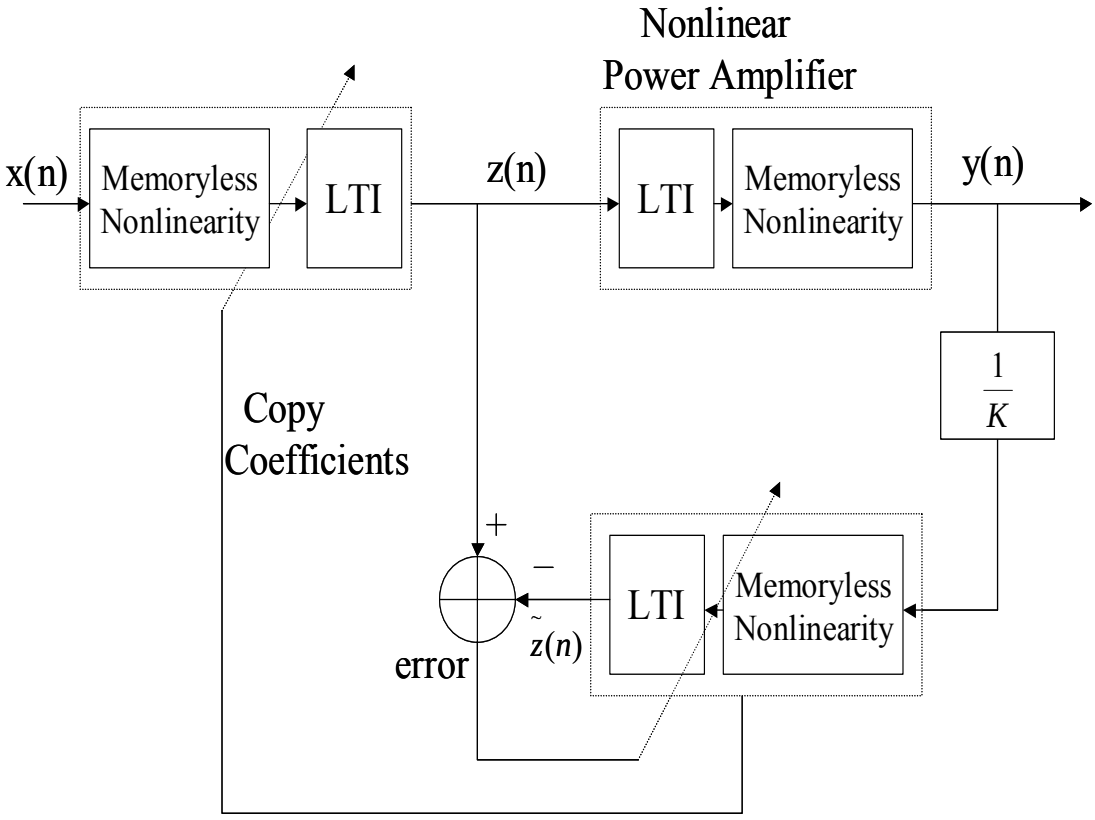

Figure 6.2 Adaptive Hammerstein Predistorter Architecture [39]

The simulation results in [39] show over 35 dB of improvement in the IMD performance of the power amplifier. The amplifier is driven with a 3-carrier Universal Mobile Telecommunications Systems (UMTS) signal.

6.4 Nonlinear Tapped Delay Line Predistorter

In [41,40], the memory is characterized in the power amplifier as hysteresis in AM/AM and AM/PM curves and can be represented by a tapped delay line polynomial as shown in Figure 6.3. The hysteresis in the power amplifier is represented by complex gain

polynomial at each tap. The polynomial at each tap is of odd order to ensure the amplifier is compressed by the same amount for both positive and negative voltages. The amplifier with memory can be represented by:

$$y(k) = \sum_{m=0}^{m=M} z_{k-m} \sum_{j=0}^{p} A_j \left| z_{k-m} \right|^{j-1} \tag{6.3}$$

The p is the order of the polynomial and A are complex coefficients.

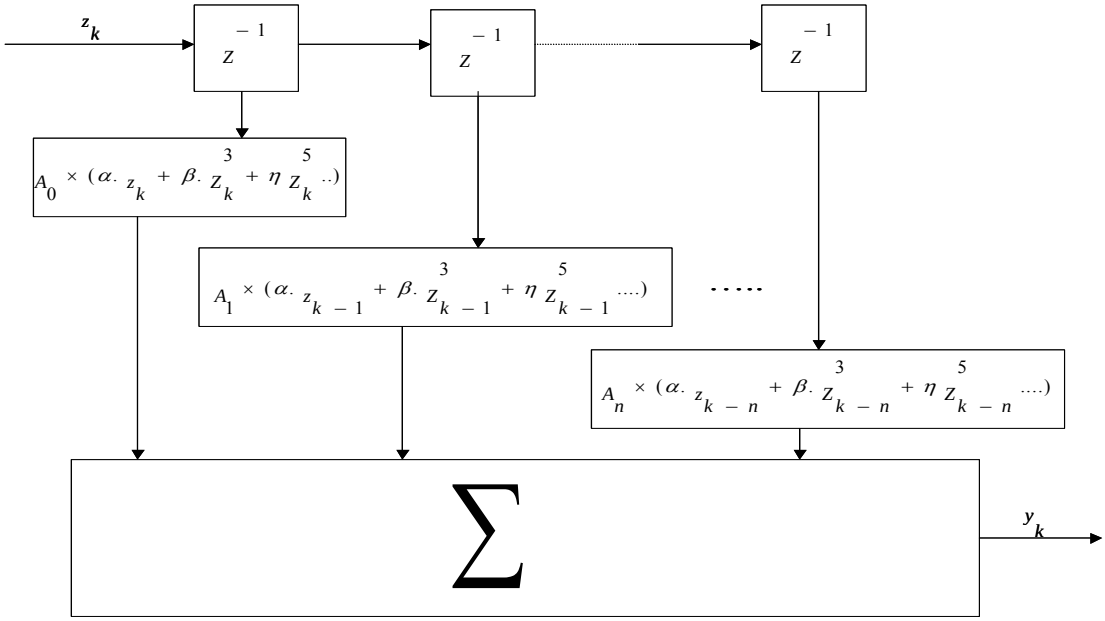

Figure 6.3 NTDL Power Amplifier Model

An adaptive NTDL predistorter uses an indirect learning architecture as shown in Figure 6.3 and consists of a trainer NTDL and a predistorter NTDL. Each tap in the NTDL predistorter is a look-up table. A polynomial fit is performed by the trainer. The trainer first estimates inverse nonlinear parameters of the power amplifier and calculates the coefficients for the polynomial in the NTDL. The trainer then fits the polynomial in the look-up table for each tap in the predistorter.

In [41], the simulation results show that for 3-tap 6th order polynomial, the IMD performance is improved by 30 dB for a 2-carrier WCDMA which has a signal bandwidth of 10MHz.

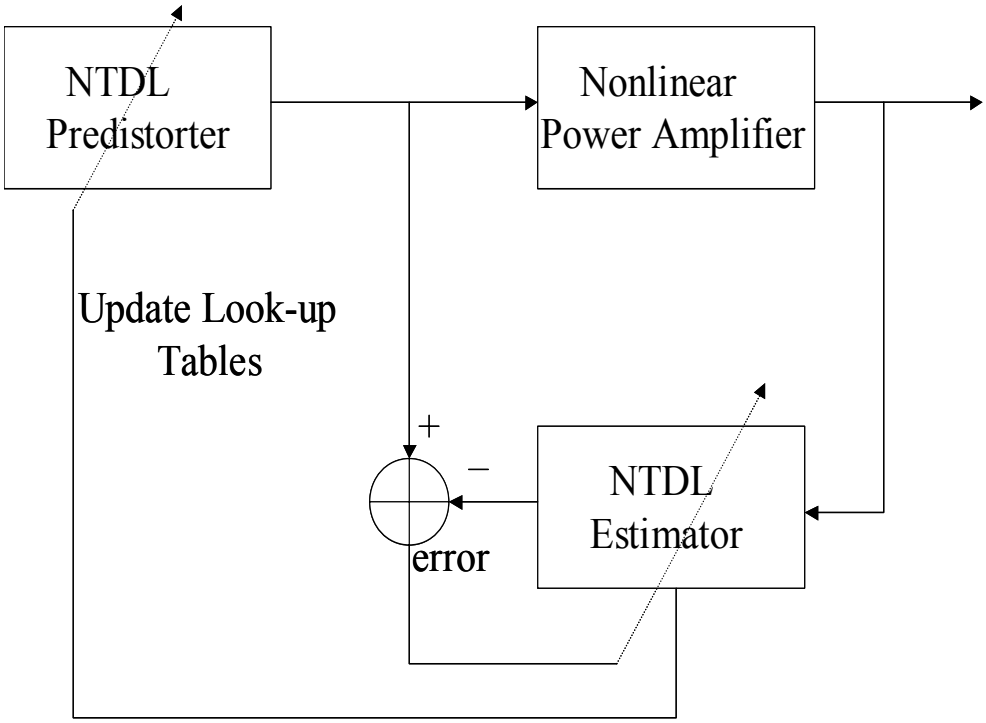

Figure 6.4 Adaptive NTDL Predistorter Architecture

6.5 Memoryless Predistorter with Feedforward for Linearizing Power Amplifiers with Memory

This technique of combining the memoryless predistorter with feedforward linearizer is a brute force solution in trying to meet stringent linearity requirements. An adaptive digital predistorter with feedforward architecture is shown in Figure 6.4.

The predistorter corrects for memoryless nonlinearity in power amplifier and the feed-forward loop corrects for nonlinearity due to memory effects. The feed-forward linearization method applies correction after the power amplifier therefore technique is immune to the memory effect in the power amplifier. This approach requires an additional amplifier which adds weight and power and also additional complexity of two converge loops.

In [42], the results from an actual power amplifier show the IMD performance is improved by 25 dB for a signal bandwidth of 10 MHz.

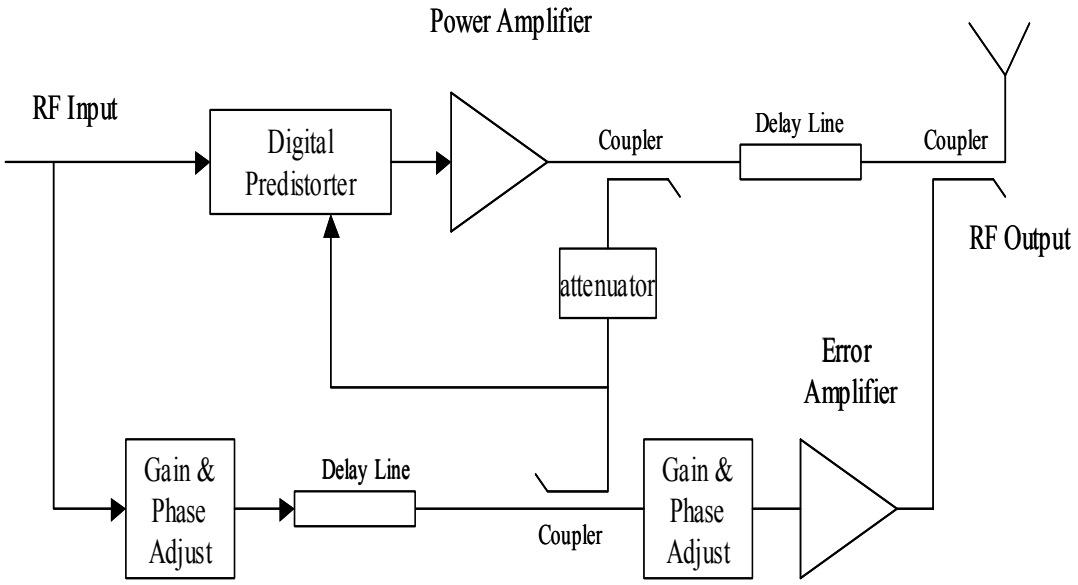

Figure 6.5 Adaptive Digital Predistorter with Feedforward Architecture

7.0 CONCLUSION AND FUTURE WORK

7.1 Conclusion

The survey of the common linearization techniques shows that the adaptive digital predistortion method was the most suitable in terms of bandwidth, correction achievable, weight and complexity for the proposed power amplifier architecture. A simulation of the memoryless adaptive digital predistorter with an actual power amplifier model has been presented and shown to provide a significant improvement in the IMD performance of a power amplifier. Sensitivity analysis of the predistorter parameters shows that the bandwidth of the canceling signal from the predistorter to power amplifier has the greatest effect on the IMD performance of the power amplifier. The simulation also shows that the size of look-up table, addressing mode for the table, time alignment of feedback with input signal and feedback signal bandwidth determine the amount of correction achieved.

The results from an actual hardware memoryless adaptive digital predistorter shows that for a Class A power amplifier, the Intersil digital predistorter was able to drive the IMD terms below –55 dB from carriers and for a Class A/B IMD terms were only -38 dB down from the carrier after correction. It was shown that the reason for only a modest amount of improvement in the IMD performance for a Class AB power amplifier was, due to memory effects. The memory effects in Class A/B power amplifier were demonstrated by the hysteresis in the gain and phase response of the power amplifier after adaptation and by asymmetrical response of the power amplifier to sync pulse. The electrical memory in the Class A/B power amplifier was minimized by optimizing the source impedance and eliminating the resonance's in bias networks and adding additional decoupling on the power supply rails. This resulted in only slight improvements in IMD performance. Therefore, it was concluded that the majority of the memory effect remaining in the power amplifier was due to thermal memory.

The comparison of the SIMULINK simulation results and the results from memory-less adaptive digital predistorter show differences which can be attributed to number of factors. The power amplifier model used in the SIMULINK model is a memory-less model, because it is based on measured data at a single frequency. Therefore, direct comparisons can only be made to the actual results with Class A power amplifier which is also memory-less. The adaptive predistorter is able to cancel almost completely the IMD terms generated by Class A power amplifier. However, the limiting factor is the system noise floor. If the noise floor of the system can be improved then the amount of

correction achieved with adaptive predistorter with Class A power amplifier will be similar to the SIMULINK simulation results. The other difference is that the up/down conversion paths in the actual system have imperfections which limits the amount of correction achieved. These imperfections have not been included in the SIMULINK model because they are difficult to model accurately.

Literature search showed that several types of adaptive digital predistorter architecture have been developed to correct for memory effects in the power amplifiers. The simulation results from various researchers show that these type of architecture were capable of improving the IMD performance of the power amplifier by greater than 30 dB over a signal bandwidth of 10 MHz.

7.2 Future Work

Future work related to this thesis should be at first, develop a Volterra series model of a power amplifier with memory and then show by simulation that an adaptive digital memory predistorter is capable of reducing the IMD terms below –52 dBc over a 30 MHz signal bandwidth. This should be followed by building an actual adaptive digital memory predistorter to verify the simulation results. To the best of the author's knowledge, no one has been able to demonstrate with real hardware a power amplifier with a linearizer able to meet the stated linearity requirements.

In addition, memory effects type of distortion is also generated by image reject filters and bandpass filters in signal path. Therefore, further work might examine how to minimize the memory effects in these components, so that the adaptive digital memory predistorter is mainly correcting for memory effects in the power amplifier. This should result in improved IMD performance. The improved IMD performance would allow the power amplifier to be operated at higher output power without violating any specifications and results in higher efficiency.

A new area of future work can be, to incorporate the techniques for reducing the peak-to-average ratio of the signal with adaptive digital predistorter. Thus producing an optimized signal processing solution for the power amplifier. This should allow the power amplifier to be operated at higher output power without the signal peaks being compressed by the power amplifier and again should result in more efficient power amplifier.

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