Impact of underfill and other physical dimensions on Silicon Lateral IGBT package reliability using computer model with discrete and continuous design variables

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ABSTRACT

An effort to design and build a prototype LED driver system which is energy efficient, highly compact and with few component count was initiated by a consortium UK universities. The prototype system will be based on silicon lateral IGBT (LIGBT) device combined with chip on board technology. Part of this effort, finite element modelling and analysis were undertaken in order to mitigate the underfill dielectric breakdown failure and solder interconnect fatigue failure of the LIGBT package structure. Electro-static analysis was undertaken to predict the extreme electric field distribution in the underfill. Based on electro-static analysis, five commercial underfill were selected for thermo-mechanical finite element analysis on solder joint fatigue failure prediction under cyclic loading. A design optimisation analysis was endeavoured to maximise the solder interconnect reliability by utilising a computer model with continuous variable (physical dimensions) and discrete variables (underfill type) and a stochastic optimiser such as multi-objective mixed discrete particle swarm optimisation. From the optimisation analysis best trade off solution are obtained.

I. INTRODUCTION

The semiconductor device design technology progression is most sophisticated. These device designs become significantly more compact in size sensitive products applications such as LED lighting, mobile phones, implantable cardioverter defibrillators (ICDs) and tablet chargers[1, 2]. These compact design devices have additional advantages due to their high current density, low power losses and reduced device footprints. These advantages have led to an increased attention toward these devices particularly in high voltage low power applications [3].

In order to utilise the advancement associated with the chip technology and exploit its full potential application level, an assembly exercise was proposed. The proposed assembly exercise targets the structural and functional integration of the design elements to enhance the reliability and also optimise the electrical / thermal management of the chip package. A consortium of UK universities is involved in this assembly exercise in order to design and build a smart energy efficient, highly compact with low component count LED driver system. The significant contribution of this assembly exercise is: it delivers a methodology for developing highly integrated, reliable and cost-effective Silicon lateral IGBTs based LED driver. This is the first time the lateral smart integrated chip together with a chip on board assembly are employed in an LED driver system.

Lateral IGBTs offer much higher current densities (5-10 times), significantly lower leakage currents and device capacitances etc., compared to the conventional vertical MOSFETs commonly used in LED driver systems. In addition, the lateral construction makes integration of other devices such as start-up MOSFETs, and temperature/current sensors feasible due to low voltage common substrate and all terminals being on the top side of the die. The higher voltage ratings (up to 1kV), high voltage interconnection between parallel IGBTs, self-isolated nature and absence of termination region unlike in a vertical MOSFET makes these devices ideal for ultra-compact, low bill of material (BOM) count LED driver system. The BOM is a hierarchical list of components used in the assembly. Chip on-board assembled LIGBTs also offer significant advantages over MOSFETs due to high ambient temperatures seen on most of the LED lamp housing.

The layout of the LIGBT package considered in this work is shown in Figure 1. The dimension of the device is 744µm x 1345µm with the deposited solder balls that has a maximum radius of around 75µm. The size of the device poses obvious challenges, which need to be analysed in order to ensure a reliable performance. The PCB package design for an effective cooling of the LIGBT is presented in Figure 1. The package was designed for

optimal thermal performance using vias. These vias link the device solder balls and top PCB copper layer to the base copper plate. The base copper plate (on the bottom of the FR4 PCB) can be used for cooling (Figure 1 (b)). An additional copper foil is used as a heatsink to extract the heat from the backside of the device. Solder layers are used to attach the copper foil to the device backside to improve thermal performance.

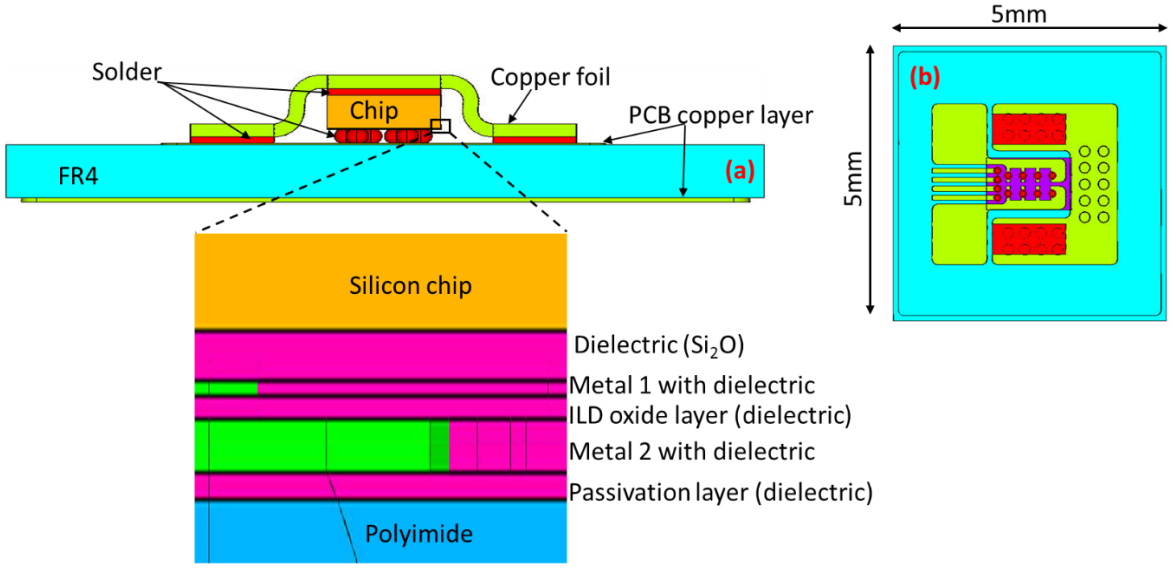

Fig 1: (a) Layers and labels of the LIGBT package, (b) top view of the package

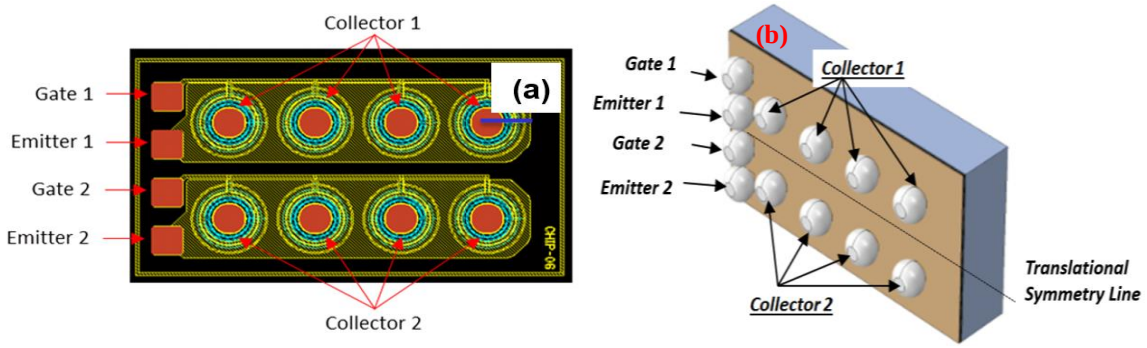

Fig.2: (a) Fabricated LIGBT layout (b) Terminal layout of two identical LIGBTs with a fully populated solder ball

The layout of the fabricated LIGBT developed by 0.6µm/5V bulk silicon CMOS process (See Trajkovic et al [3]), is shown in Figure 2(a), and 3 dimensional schematic of the LIGBT device structure is presented in Figure 2(b). The device is an 800V silicon LIGBT. The challenging aspects of the LIGBT package design in high voltage application are the underfill dielectric breakdown (DB) failure and solder fatigue failure. The underfill in chip package reduces the inelastic strain sustained by the solder and improves the thermal fatigue life of the solder joint. Furthermore underfill (UF) materials reduce and redistribute the stresses and strains in the structure by minimising the coefficient of thermal expansion (CTE) mismatch [4]. Underfill DB (and also referred as breakdown voltage) is the maximum electric field limit of an underfill material which can withstand before complete breakdown. It is desirable that the dielectric strength of an underfill should be above 20 kV/mm [5]. In high voltage application, underfill is required to withstand the extreme electric field in the region, hence its DB should be higher than the extreme electric field value in real application. In contrast, choosing an underfill with high dielectric breakdown value could compromise the solder joint reliability in comparison with the reliability of a package with an underfill which has low dielectric breakdown strength. CTE value of UF should be close to the CTE of solder material. If the CTE of the underfill differs significantly from that of solder material (20 to 30 µm /°C), thermal cycling will cause the solder and the underfill to expand and contract at different rates, exerting higher residual stresses on the solder interconnect [6].

In order to avoid the underfill dielectric breakdown failure and maximise the solder joint reliability, finite element modelling methodology was utilised for the LIGBT package structure. Finite element analysis consist of

electrostatic analysis in order to estimate the extreme electric potential distribution and thermo-mechanical analysis in order to predict the solder interconnect plastic strain distribution, hence solder interconnect reliability estimation. This paper is technically structured into five sections. Section (II) illustrates the modelling methodology of electro static analysis in order to predict the electric field distribution in the underfill layer. From the underfill layer electric potential finite element modelling prediction, five commercial underfill were selected for evaluation of the impact of these selected underfill on solder joint reliability. Section (III) illustrates the modelling methodology of thermo-mechanical analysis of the package in order to predict the solder interconnect reliability. Section (IV) composed of design of experiment (DoE) schemes of mixed continuous and discrete design variables. For all DoE design points, finite element simulations were generated and solder interconnect accumulated plastic strains were extracted, which in turn used to predict the solder reliability. Section (V) presents the computer model dependent on continuous and discrete design variables. Section (VI) discusses the multi-objective optimisation scheme for minimising the solder layer and solder bump accumulated plastic strain, hence maximising the solder interconnect reliability from multi-objective optimisation perspective. In terms of contributions of this manuscript can be listed as

- Application of a computer model with mixed discrete and continuous design variables for physics of failure based (PoF) reliability evaluation in context of power electronics applications
- Application of multi-objective mixed discrete and continuous stochastic optimisation for maximising the reliability of the LIGBT package.

II. ELECTROSTATIC MODELLING OF CHIP PACKAGE

The choice of underfill for LIGBT package assembly is also important in the context of overall reliability. In order to optimise overall package reliability detailed finite element models have been built to assess electric field distributions in the underfill for predicting underfill dielectric breakdown failure. Finite element model consists of, top to bottom, chip with thickness of 250 microns, interlayer dielectric with thickness of 2 microns, metal (Al) and dielectric layer with thickness of 0.65 micron, interlayer dielectric with thickness of one micron, metal (Al) and dielectric layer with thickness of 2.1 micron, passivation layer with thickness of 1.1 microns, polyimide layer with thickness of 5 microns, and final layer of solder bump and underfill with thickness of 103 microns as in Figure 3(a). The electro-static analysis was undertaken by solving the Poisson equation (equation (2)).

$$\nabla E = \frac{\rho}{\varepsilon} \tag{1}$$

$$\nabla \times E = 0 \;\Rightarrow\; \nabla(\nabla V) = -\frac{\rho}{\varepsilon} \tag{2}$$

$$E = -\nabla V \tag{3}$$

Where E- electric field, V-electric potential, ε – permittivity of the medium, ρ- electric charge density. The electrical properties of LIGBT package materials were sourced from public domain [7] in this study. The permittivity values of underfill, solder (Sn3.5Ag), polyimide, SiO2, aluminium, Si die are respectively 3.47, 2, 3.2, 3.9, 1.6, and 11.8. The high electric potential of 400V was applied on the collector and solder bumps and ground voltage (0V) was applied on the gate of the device. The plot in Figure 3(b) corresponds to the electric field distribution in the underfill structure from bottom view. The Figure 3(c) is the cross sectional view of electric field distribution along the cross sectional line marked in Figure 3(b). Higher electric field distribution is concentrated in the region close to polyimide/solder/underfill interface as in Figure 3(c).

The plot in Figure 4(a) is the electric field vector sum values along the cross sectional line between A and B (as marked in Figure 4(c)). The electric field vector sum values (Figure 4(a)) were extracted by Ansys 'path integral' on the polyimide/ underfill interface. The electric field intensity at the distance of 210 μm is higher than field intensity at the distance of 70 μm as in Figure 4(a) since the electric charges on the adjacent solder bumps influence the field intensity at the distance of 210 μm from A. Increase in underfill relative permittivity value decreases the extreme electric field vector sum in the underfill as in the Figure 5. If the maximum electric field is less than dielectric breakdown strength of the underfill, then underfill can withstand the breakdown related failure. Among commercially available underfill, five underfill adhesives types for their high dielectric breakdown strength value, from three leading commercial manufacturers, Henkel Loctite Corporation [8], United Adhesives

[9] and Masterbond Inc [10] were selected in this study. All these selected underfill have dielectric breakdown value in the range of 20 - 40 KV/mm and relative permittivity value in the range of 3 to 4.

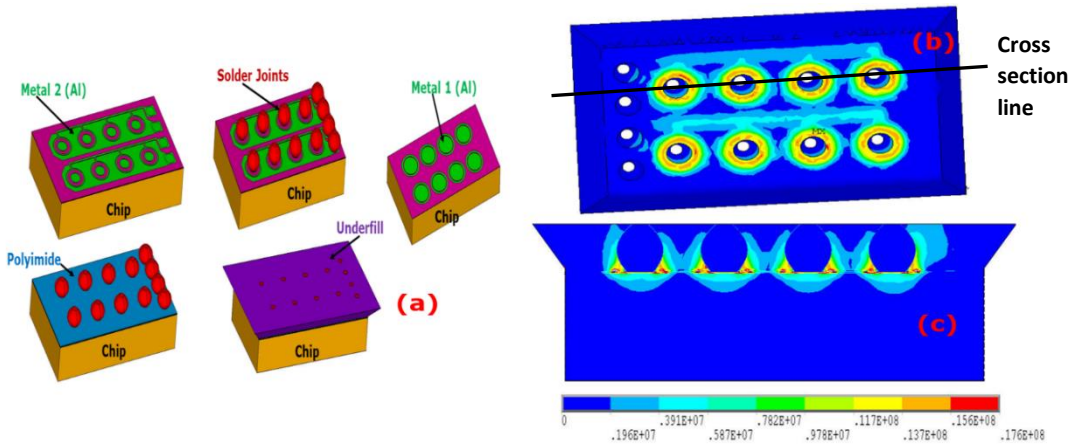

Fig 3: (a) Package model for the electro-static analysis (b) electric field vector sum distribution on the bottom of the underfill, and (c) electric field vector sum distribution on the cross section (Fig 3(b)) of the underfill

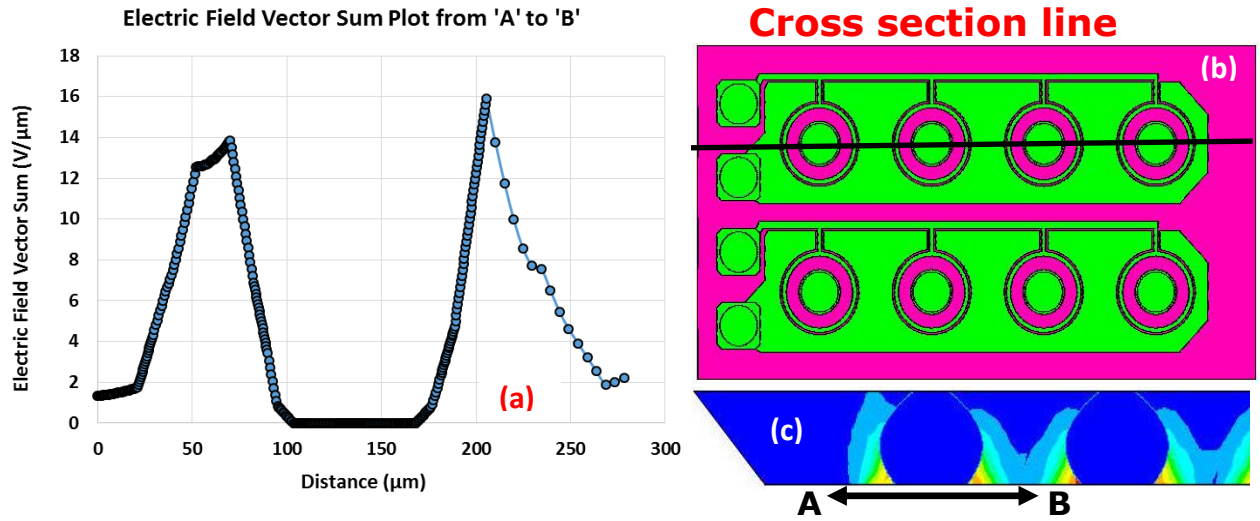

Fig 4: (a) Electric field vector sum versus distance from 'A' to 'B' across the solder bump, (b) Top view of the cross section line, (c) electric field vector sum distribution from the side view.

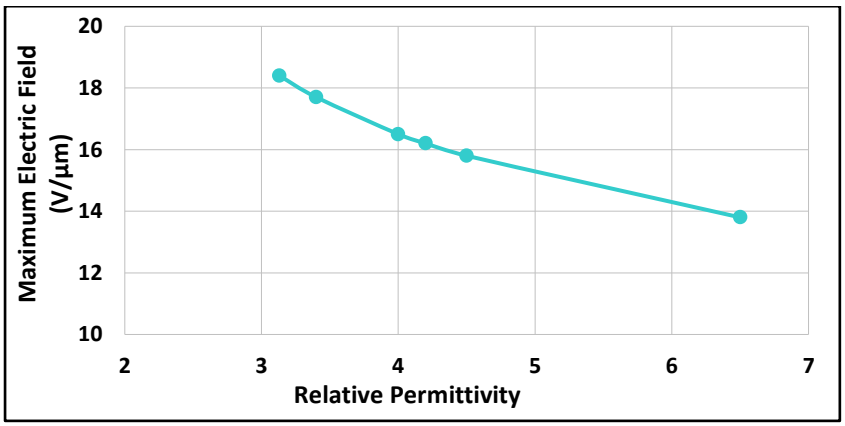

Fig 5: Extreme electric field vector sum in the underfill versus relative permittivity value of the underfill from electro-static finite element analysis.

III. THERMO-MECHANICAL MODELLING PACKAGE STRUCTURE

Thermo-mechanical finite element modelling of the package structure of LIGBT device was undertaken in order to predict the strain and stresses in the solder layers hence the prediction of the solder interconnect reliability. The package components of LIGBT device are as in Figure 6. Solder material has viscoplastic material properties. The Anand's viscoplastic model used in this study, was originally developed for high-temperature metal forming processes such as rolling, but it has been demonstrated for use in predicting the life of solder joints in electronic packaging. The flow equation of Anand model for inelastic strain rate dependence on the stress is defined as [11, 12]

$$\dot{\varepsilon_p} = Aexp\left(\frac{-Q}{RT}\right)\left(\sinh\left(\xi\frac{\sigma}{S}\right)\right)^{1/m} \tag{4}$$

Where $\dot{\varepsilon_p}$ is the inelastic strain rate, A - pre-exponential factor, Q - activation energy, R - universal gas constant, T – absolute temperature, ξ - material constant, σ is the equivalent stress and m is the strain rate sensitivity. Moreover the evolution equation for the internal variable s is of the form as

$$\dot{s} = \left(h_0\left|1-\frac{s}{s^*}\right|^a sign\left(1-\frac{s}{s^*}\right)\right)\dot{\varepsilon_p} \tag{5}$$

$$\text{with} \quad s^* = \hat{s}\left[\frac{\dot{\varepsilon_p}}{A}exp\left(\frac{Q}{RT}\right)\right]^n \tag{6}$$

where s^* - saturation value of s associated with a set of given temperature and strain rate, h_0 – hardening softening constant, n - strain rate sensitivity for the saturation value of the deformation resistance. There are nine material parameters in the viscoplastic Anand model (equations (4), (5), and (6)) A, Q, ξ, m, h_0,$\hat{S}$, n, a, and s_0. The last parameter s_0 is the initial value of the deformation resistance. These nine parameters are listed in Table 3.

A passive thermo-mechanical finite element analysis using the element SOLID185 was undertaken in Ansys mechanical APDL. In passive thermal cycling, temperatures in the whole package change simultaneously during the cycle. The parts in the model associated with critical regions of interest have finer mesh in order to ensure accurate FEA results. The structural and thermal LIGBT package material properties used in the finite element simulations are on the Table 1. The structural and thermal material properties of the selected underfill were extracted from the manufacturer's specifications as in the Table 2. The underfill can be viewed as a composite material consisting of epoxy resin and silica particles. In order to evaluate the Poisson ratio of the some of the underfill composite material which is not available from manufacturer's specification, rule of mixture approach was utilised to estimate Poisson ratio

$$\mu_{12} = v_E\mu_E + v_S\mu_S$$

where μ_E and μ_S are the Poisson ratio of epoxy and silica, respectively 0.4 and 0.19 [13]. The parameters v_E and v_S are respectively volume ratio of epoxy and silica.

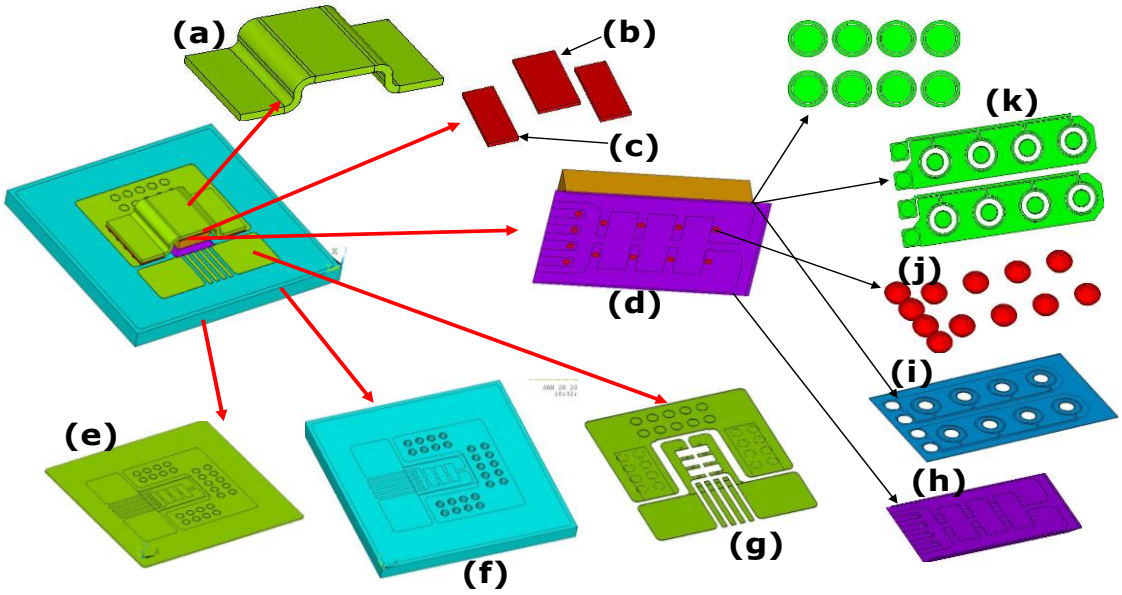

Fig.6: Components of package structure (a) Copper foil, (b) solder layer between copper foil and die, (c) solder layer between copper foil and PCB, (d) chip package, (e) copper layer on the bottom of the FR4 PCB, (f) FR4

PCB, (g) copper layer on top of the FR4, (h) underfill layer, (i) polyimide layer, (j) solder bump, and (k) aluminium metal layer (metal 1 and 2)

Table 1: Structural and thermal material properties used in the FEA

Properties / Material	Density (kg/m^3)	Coefficient of Thermal Expansion (10^{-6}/K)	Young's Modulus (GPa)	Poisson Ratio
FR4 PCB	1850	18.5	22	0.28
Polyimide	1420	13	14.5	0.34
Dielectric (SiO_2)	2200	0.54	69	0.17
Aluminium(Al)	2700	23.1	124	0.35
Silicon (Si)	2329	2.8	131	0.3
Solder (Sn3.5Ag)	7360	21.85+0.0204*T(°C)	-0.075*T(°C)+52.582	0.4
Copper (Cu)	8900	16.9	180	0.31

Table 2: Structural and thermal material properties of Underfill materials used in this study

Properties / Type	Density (kg/m^3)	Coefficient of Thermal Expansion (10^{-6}/K)	Young's Modulus (GPa)	Poisson Ratio
'A'	1670	< 75 (Above 150 °C) < 19 (Below 150 °C)	7.6	0.32
'B'	1600	< 89 (Above 125 °C) < 22 (Below 125 °C)	7	0.32
'C'	1740	< 80 (Above 155 °C) < 25 (Below 155 °C)	3.5	0.316
'D'	1520	<110 (Above 150 °C) < 35 (Below 150 °C)	2.8	0.274
'E'	1420	25	3.103	0.29

Table 3: Anand viscoplastic parameters of Sn3.5Ag solder

Anand Parameters	A (sec^{-1})	Q/R (° k)	ξ	m	$\hat{s}$ (MPa)	n	h_0 (MPa)	a	s_0 (MPa)
Value	2.23 (10^4)	8900	6	0.182	73.81	0.018	3321.15	1.82	39.09

The standard temperature cycling with ramp and dwell time of 3 and 15 minutes with the temperature range of (-25°C, 125°C) was imposed on the model. The package structure was structurally restricted with three point structural boundary restriction constraint. Plastic strain distributions of solder were extracted from the numerical simulation. Accumulated plastic strain of solder bump, solder layer between copper foil and PCB, and the solder layer between copper foil and the silicon substrate were evaluated by volume weighted averaging of thin layer (10 μm) of the total volume. To avoid the mesh singularity (singularity is the points where some aspect of the solution tends toward an unrealistic value), volume weighted averaging is commonly used to approximate physical quantity of interest on the particular region where this quantity is concentrated. A Coffin Manson fatigue model [14] was utilised for lifetime of solder. The fatigue model parameters utilised in this study is as in equation (7)

$$\Delta\varepsilon_{Pl}^{acc}\left(N_f\right)^{0.6978} = 3.921 \tag{7}$$

where N_f is the cycles to failure, and $\Delta\varepsilon_{Pl}^{acc}$ is the accumulated plastic strain in one cycle. Figure (7) is the accumulated plastic strain distribution in the LIGBT package for one cycle. The plot is extracted for the third stabilised cycle. Similarly figure (8) is the accumulated plastic strain distribution on all the solder interconnects in third cycle. The accumulated plastic strain distributions are within the range of 0.005 to 0.044. It was noted that accumulated plastic strain is higher in solder layer between copper foil and the silicon substrate than other solder interconnects. Hence that solder layer between the copper foil and the device has the worst lifetime in comparison

with lifetime of the solder bumps enclosed in the underfill. This highlights the underfills stress reduction capability in solder bump.

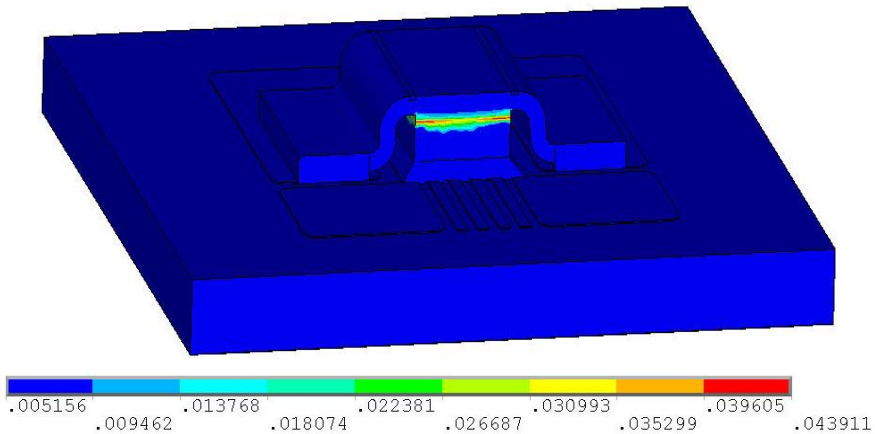

Fig 7: Accumulated plastic strain distribution in one cycle on the package

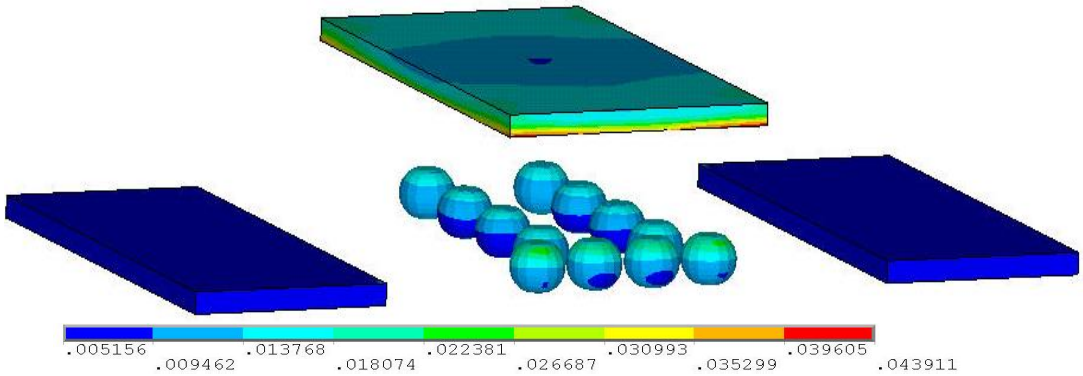

Fig 8: Accumulated plastic strain distribution in one cycle on the solder layers/bumps of the package

IV. DESIGN OF EXPERIMENT

In order to minimise the accumulated plastic strain and hence maximise the reliability of the solder layer and solder bump, a multi-objective design optimisation was endeavoured. The continuous design variables were selected based on their global influence on all solder interconnects. Table 4 lists the key design variables of interest to be optimised in order to maximise the solder reliability. The second column specifies the value of the nominal (or initial) design variable value while third column of the table provides details on some possible design variations of the assembly parameters. The fourth column of the table is the normalised design parameter variations of the continuous design variables. Fourth row correspond to the five levels of the discrete design variable 'underfill type'.

Table 4: Discrete and continuous design parameters

Design Variables	**Nominal Values**	**Un-scaled limits**	**Scaled Limits/dimensionless**
Copper foil thickness(µm)	125	100 to 150	-1 to 1
FR4 PCB Thickness(µm)	500	400 to 600	-1 to 1
Underfill Type	{'A', 'B', 'C', 'D', 'E'}		

Design of experiment (DoE) schemes were applied in the two-dimensional continuous design space of the package structure defined by the respective limits. A two level full factorial design method was applied to the continuous design space to provide four design points. In addition, two sampling points were derived by Latin Hypercube sampling scheme and the central point is also included in the continuous design space. Discrete design variable, underfill has five levels as in the Table 4. Seven continuous DoE points and the discrete design variable with five levels formed of thirty five design points combinations. For each design points, corresponding thermo-mechanical FEA model (as in Section V) was generated. The DoE points are listed in table in Appendix A. The table also shows the dimensionless scaled values of design variables over the range of -1 to 1. The fourth and fifth

columns of the table also list the finite element analysis predictions for accumulated averaged plastic strain on the 10 microns thick volume of solder layer and solder bumps. The sixth and seventh columns represents the number of cycles to failure (lifetime) of the solder layer and solder bumps.

V. COMPUTER MODEL WITH DISCRETE AND CONTINUOUS FACTORS

A Kriging model with continuous (quantitative) dependent variable such as PCB thickness as well as categorical (discrete) dependent variable such as solder type ('Sn3.5Ag') was proposed by Zhou et al [15]. The process model with discrete and continuous depend variables is defined as in equation (8)

$$y(\boldsymbol{w}) = \boldsymbol{f}^t(\boldsymbol{w})\,\beta + \varepsilon(\boldsymbol{w}) \tag{8}$$

where $\boldsymbol{w} = (\{\boldsymbol{x} = x_1, x_2, \ldots, x_i\}, \{\boldsymbol{z} = z_1, z_2, \ldots, z_j\})$ consists of i number of continuous variables and j number of discrete variables. Each discrete variables has number of levels for an example z_1 has b_1 level, hence total number of level combination factor is $m = \prod_{k=1}^{j} b_k$. For an example, 'PCB type' and 'solder type' are two discrete variable with two levels such as {'FR4', 'IMS} and {'Sn3.5Ag', 'Sn37Pb'} respectively then there are four level combinations such as {'FR4', 'Sn3.5Ag'}, {'FR4', 'Sn37Pb'}, {'IMS', 'Sn3.5Ag'}, {'IMS', 'Sn37Pb'} exists. $\boldsymbol{f}(\boldsymbol{w}) = (f_1(\boldsymbol{w}), f_2(\boldsymbol{w}), \ldots, f_p(\boldsymbol{w}))^t$ is a set of p user defined regression function, and $\beta = (\beta_1, \beta_2, \ldots, \beta_p)^t$ is the coefficient vector and $\varepsilon(\boldsymbol{w})$ is assumed to be stationary Gaussian process with zero mean and a variance. Matérn 5/2 correlation function between continuous variable vectors $\boldsymbol{x}^1$ and $\boldsymbol{x}^2$ is defined as in equation (9)

$$\phi(\boldsymbol{x}^1, \boldsymbol{x}^2, C_1, C_2) = \begin{cases} 0 & if \quad |h| = 0 \\ C_1\left(1 + \sqrt{10}\frac{|h|}{C_2} + \frac{10}{3}\frac{|h|^2}{C_2^2}\right)e^{-\sqrt{10}\frac{|h|}{\theta}} & if \quad 0 \le |h \le C_2| \\ C_1 & if \quad |h > C_2| \end{cases} \tag{9}$$

where $h = \sqrt{\sum_{k=1}^{i}\left(x_k^1 - x_k^2\right)^2}$, $x_1 = \{x_1^1, x_2^1, \cdots, x_i^1\}$ and C_1 and C_2 are coefficients of the Matérn correlation function. The correlation between $\varepsilon(\boldsymbol{w}_1)$ and $\varepsilon(\boldsymbol{w}_2)$ is defined as in equation (10)

$$Cor(\varepsilon(\boldsymbol{w}_1), \varepsilon(\boldsymbol{w}_2)) = T\,\phi(\boldsymbol{x}^1, \boldsymbol{x}^2, C_1, C_2) \tag{10}$$

where T is an $m \times m$ a positive definite with unit diagonal element (PDUDE) matrix as in equation (11) and ϕ is as in equation (9)

$$T = \begin{bmatrix} 1 & \tau_{12} & \cdots & \tau_{1m} \\ \tau_{12} & 1 & \cdots & \tau_{2m} \\ \vdots & \vdots & \ddots & \vdots \\ \tau_{1m} & \tau_{2m} & \cdots & 1 \end{bmatrix} \tag{11}$$

The unknown parameters of the Matérn correlation function C_1, C_2 and element of the PDUDE matrix (equation (11)) were extracted by optimising an objective function (equation (12))

$$\text{Min}\ \left\{nLog\left(\sigma^2\right) + Log\left(|R|\right)\right\} \tag{12}$$

where $\sigma^2 = \left(y - F\hat{\beta}\right)^t R^{-1}\left(y - F\hat{\beta}\right)/n$, $\hat{\beta} = (F^t R^{-1} F)^{-1} F^t R^{-1} y$

And $F = (\boldsymbol{f}(\boldsymbol{w}_1), \boldsymbol{f}(\boldsymbol{w}_2), \ldots \boldsymbol{f}(\boldsymbol{w}_n))^t$ is an $n \times p$ matrix and R is the correlation matrix whose $(i,j)^{\text{th}}$ entry is $Cor(\varepsilon(\boldsymbol{w}_i), \varepsilon(\boldsymbol{w}_j))$ as defined in equation (10). Hence the response of the Kriging process model with discrete and continuous factors in equation (9) becomes as equation (13)

$$y(\boldsymbol{w}_0) = \boldsymbol{f}^t(\boldsymbol{w}_0)\,\beta + r^t(\boldsymbol{w}_0)\,\alpha \tag{13}$$

where coefficient vector $\alpha = R^{-1}(y-F\beta)$ and $\{r_i = Cor\ (\varepsilon(\mathbf{w}_0), \varepsilon(\mathbf{w}_i))\}i=1,\ldots35$. A MatLab code was generated to build a Kriging process model. The Kriging process model with discrete and continuous design variables for accumulated plastic strain ($\times 10^{-3}$) of solder layer between die and copper foil in one cycle is defined as

$$y_{SolderLayer}\left(x_{CopperFoil}, x_{FR4}, z_{Underfill}\right) = 0.263\,x_{CopperFoil} - 0.064\,x_{FR4} + 21.376 + \sum_{j=1}^{35} \alpha_j^{SolderLayer} T^{SL}\left(w, w^j\right)\phi\left(x, x^j, 8.05, 19.203\right) \quad (14)$$

The elements of the PDUDE matrix T^{SL} in equation (14) is on the Table 5.

Table 5: The elements of PDUDE matrix T^{SL} for design variable vector combination of w and w^j in equation (14)

Underfill type in *w* / **Underfill type in w^j**	**'A'**	**'B'**	**'C'**	**'D'**	**'E'**
'A'	1	0.855	0.263	0.557	0.917
'B'	0.855	1	0.421	0.38	0.979
'C'	0.263	0.421	1	-0.109	0.386
'D'	0.557	0.38	-0.109	1	0.5
'E'	0.917	0.979	0.386	0.5	1

The Kriging process model with discrete and continuous variables for accumulated plastic strain ($\times 10^{-3}$) in solder bump enclosed by the underfill in one cycle is defined as

$$y_{SolderBump}\left(x_{CopperFoil}, x_{FR4}, z_{Underfill}\right) = -0.039\,x_{CopperFoil} + 0.047\,x_{FR4} + 11.803 + \sum_{j=1}^{35} \alpha_i^{SolderBump} T^{SB}\left(w, w^j\right)\phi\left(x, x^j,\ 7.551,\ 25.321\right) \quad (15)$$

The elements of the PDUDE matrix T^{SB} in equation (15) is on the Table 6. The coefficients vectors of the Kriging models $\left\{\alpha_{i=1,\cdots,35}^{Solder\ Layer}\right\}$, $\left\{\alpha_{i=1,\cdots,35}^{Solder\ Bump}\right\}$ in equation (14) and (15) are on the Table in Appendix B.

Table 6: The elements of PDUDE matrix T^{SB} for design variable combination of w and w^j in equation (15)

Underfill type in w / **Underfill type in w^j**	**'A'**	**'B'**	**'C'**	**'D'**	**'E'**
'A'	1	0.7951	0.3958	-0.21	0.7453
'B'	0.7951	1	-0.0455	-0.1129	0.9534
'C'	0.3958	-0.0455	1	0.0585	0.1082
'D'	-0.21	-0.1129	0.0585	1	-0.1892
'E'	0.7453	0.9534	0.1082	-0.1892	1

Figures (9), (10), and (11) are the plots of the computer models (equations (14) and (15) by keeping one variable constant. The models represent the accumulated plastic strain in corresponding solder interconnect as function of copper foil thickness, FR4 PCB thickness, and underfill type. Figure (9 a) & (9 b) are the plastic strain plots in the solder layer and bump respectively against the copper foil thickness and underfill type for constant value of PCB thickness. Figure (10 a) & (10 b) are the plastic strain plots in the solder layer and bump respectively against the PCB thickness and underfill type for constant value of copper foil thickness. Figure (11 a) & (11 b) are the plastic strain plots in the solder layer and bump respectively against the copper foil thickness and PCB thickness for the underfill type B.

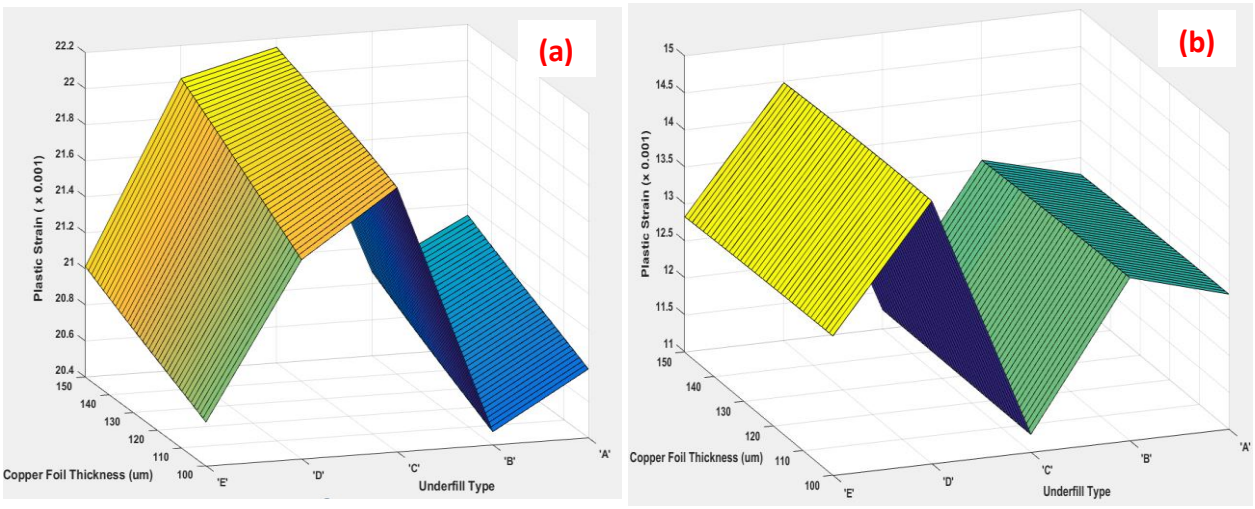

Fig 9: (a) Plastic strain (× 10^{-3}) distribution plot of solder layer against copper foil thickness (µm) and underfill type for constant FR4 thickness of 400 µm, (b) Plastic strain (× 10^{-3}) distribution plot of solder bump against copper foil thickness (µm) and underfill type for constant FR4 thickness of 400 µm.

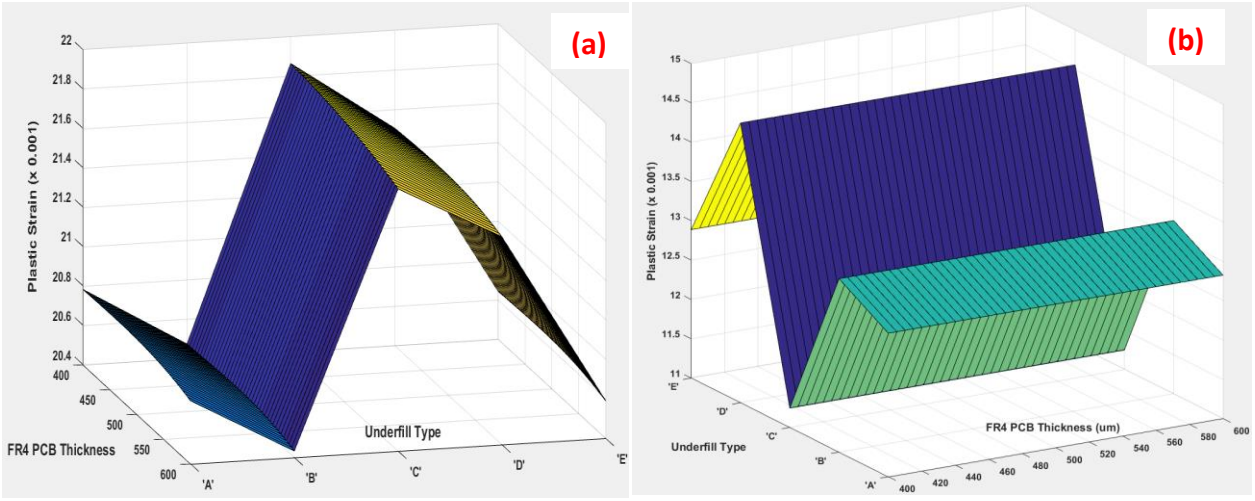

Fig 10: (a) Plastic strain (× 10^{-3}) distribution plot of solder layer against FR4 PCB thickness (µm) and underfill type for constant copper foil thickness of 100 µm, (b) Plastic strain (× 10^{-3}) distribution plot of solder bump against FR4 PCB thickness (µm) and underfill type for constant copper foil thickness of 100 µm.

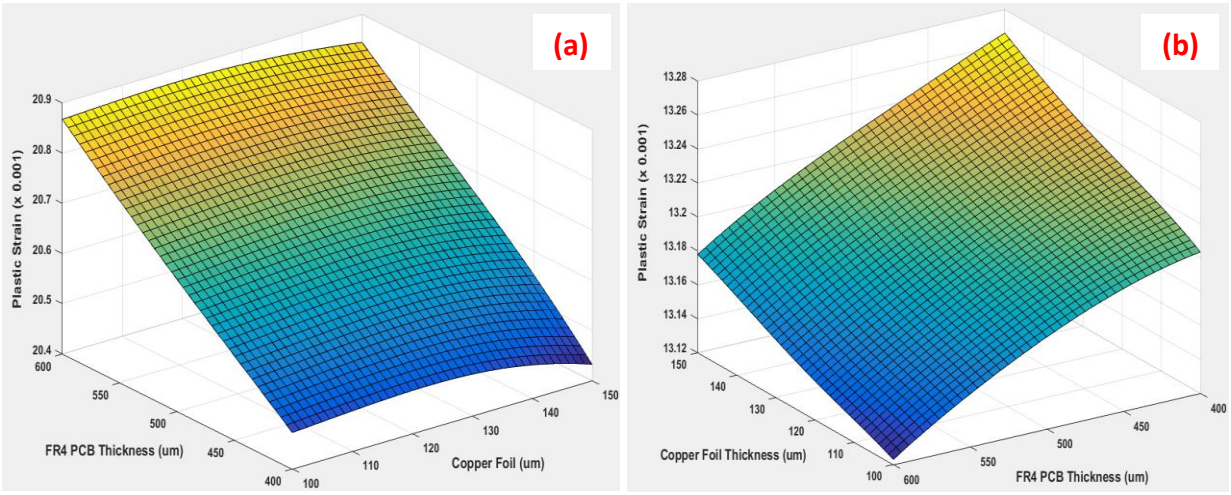

Fig 11: (a) Plastic strain (× 10^{-3}) distribution plot of solder layer vs FR4 PCB thickness (µm) and copper foil thickness for underfill type 'B', (b) Plastic strain (× 10^{-3}) distribution plot of solder bump within the underfill (type 'B') vs FR4 PCB thickness (µm) and copper foil thickness.

VI. MULTI-OBJECTIVE OPTIMISATION

In order to minimise the accumulated plastic strains in solder layer (equation (14)) and solder bump (equation (15)) simultaneously, a multi-objective optimisation (MOO) task was proposed. Multi-objective optimisation with constraints is optimising multiple objectives in a design optimisation task within a design space with additional constraints. The resulting solution of MOO is not a single optimum, rather a set of best compromise optimums called 'Pareto optimal' or 'Pareto solution'. A Pareto solution is set of optimums in which any improvement in one objective function can only possible at the expense of deterioration one or more of the other objective functions.

The form of constraint bi-objective optimisation task with mixed discrete and continuous variables can be expressed as

$$Min\ [\ y_{SolderLayer}(w), y_{SolderBump}(w)\ ]$$

$$w = \left(x_{CopperFoil}, x_{FR4}, z_{Underfill}\right)$$

s.t.
$$-1 \le x_{CopperFoil} \le 1$$
$$-1 \le x_{FR4} \le 1$$

and $z_{Underfill} \in \{'A','B','C','D','E'\}$

where $x_{CopperFoil}$ and x_{FR4} are the normalised variables within the range of -1 and 1. The non normalised variable ranges are in the Table 4. Two approaches for the MOO in the literature such as [16, 17]

- Preference based approach
- Ideal approach

Preference based approach consists of forming a composite objective function as weighted sum (scalarisation) of the objectives and ideal procedure consists of finding multiple trade off solutions with wide range of values of the objectives and then choosing one of the best solution based on the best information available (certain criteria) as in Figure 12.

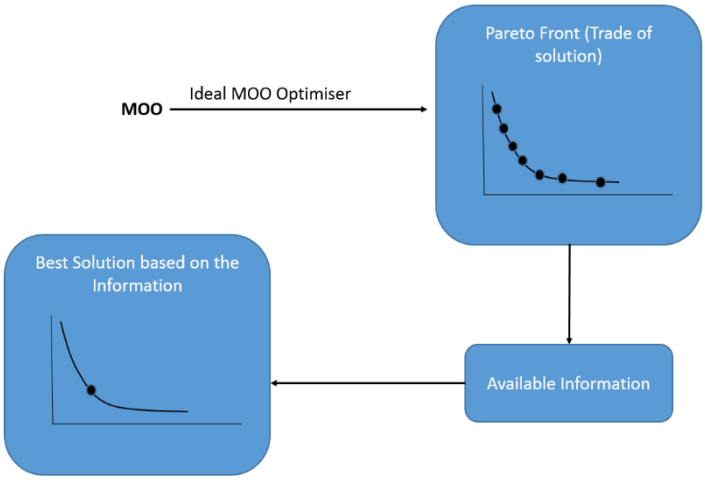

Fig 12: Ideal procedure for MOO solution

A. *Multi-Objective Mixed Discrete Particle Swarm Optimisation*

Particle swarm optimisation (PSO) scheme is based on a simplified social model that is originated from the swarming theory [18]. There are many improved versions of PSO in the literature such as co-evolutionary particle swarm [19], hybrid particle swarm optimization [20] and Quantum behaved PSO. Quantum-behaved particle swarm optimisation (QPSO) based on the quantum mechanics, can be theoretically guaranteed to find optimal solution in

search space, and it also has few control parameters [20]. Multi-objective mixed discrete particle swarm optimisation (MOO-MDPSO) is developed by Tong et al [21]. MOO-MDPSO was evolved from the single objective PSO called Mixed-Discrete PSO algorithm (MDPSO) developed by Chowdhury et al [22, 23]. In this study the MOO-MDPSO was adopted since it's capability to handle continuous as well as the discrete design variables of the bi-objective task.

The fundamental difference between the PSO and MDPSO is the additional diverging velocity vector for preserving the population diversity, hence avoiding the premature particle clustering and solution stagnation. In a MDPSO of swarm size *m*, each individual swarm is treated as a volume less particle in *n*-dimensional space, with the position vector $X_i(t)$ and velocity vector $V_i(t)$ of particle *i* at t^{th} iteration is represented as

$$V_i(t+1) = wV_i(t) + C_1 r_1 \left(P_i^l - X_{ij}(t)\right) + C_2 r_2 \left(P_i^g(t) - X_i(t)\right) + \gamma_{c,i} r_3 \left(P_i^g(t) - X_i(t)\right) \quad (16)$$

$$X_i(t+1) = X_i(t) + V_i(t+1) \quad (17)$$

where P_i^g represents the global leader of particle *i* selected from global set *G(t)*, P_i^l represents the local leader of particle *i* selected from its local set $L_i(t)$. C_1 and C_2 represent the cognitive and social parameters respectively. r_1, r_2, and r_3 are random numbers between *0* and *1*. $\gamma_{c,i}$ is the diversity preservation vector component extracted from continuous design variables hyperspace and discrete design variables hypergrid (See Chowdhury at al [23]). The eligibility criteria of current location particle *Xi(t)* to be stored in the local set *Li(t)* is defined as

$$X_i(t) \in L_i(t)$$

If

$$f^k(X_i(t)) \leq f^k(Y_i(t)) \text{ for at least one } k$$

where $\forall k = 1,2,\ldots,N$ and $\forall Y_i(t) \in L_i(t-1)$. The global solution set *G(t)* is obtained by applying the Pareto filter (see Messac et al [24]) to solutions in all of the local sets.

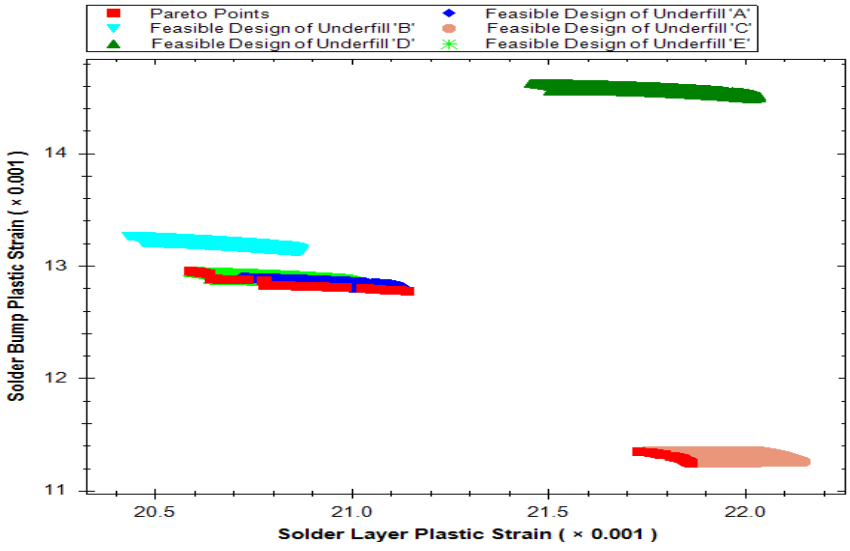

Fig 13: Pareto front plots of plastic strain ($\times 10^{-3}$) of solder bump and solder layer by MOO-MDPSO.

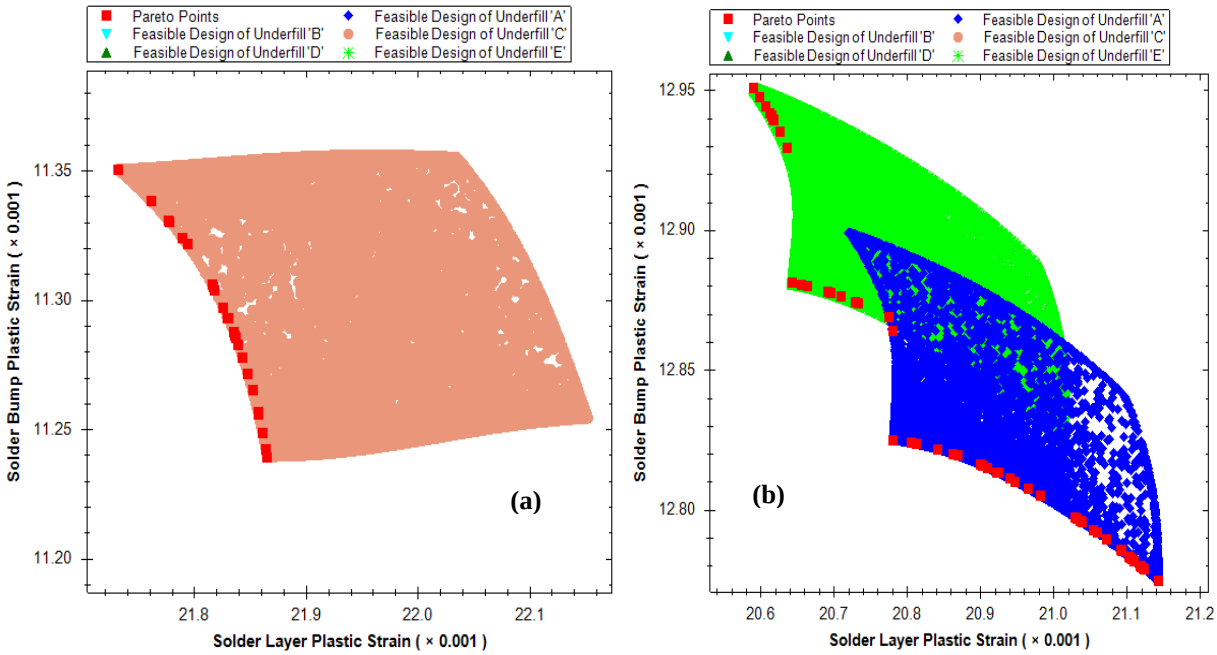

Fig 14: (a) Pareto front plots in the feasible design space of underfill C, and (b) Pareto front plots in the feasible design space of underfill A & E.

The objective function with mixed (continuous and discrete) design variables, search space of the discrete design variable was generated by relatively straightforward approach namely 'Nearest vertex approach' (NVA). In NVA, discrete domain location is approximated to the nearest vertex of the local hypercube based on the Euclidean distance between closest the discrete sets [22]. Other more computationally expensive approach for discrete domain location approximation is also reported in the literature such as 'shortest normal distance approach' (SND) [23] which was not considered in this study. A C# code was generated to implement the MOO-MDPSO algorithm. The Pareto solution of the bi-objective optimisation of solder bump plastic strain and solder layer plastic strain is in Fig 13 &14

VII. Discussion

A combination of Kriging metamodel which can handle discrete and continuous design variables and MOO-MDPSO optimiser is a suitable combination for design optimisation of discrete and continuous design space. In the MOO-MDPSO method Pareto solution does not have enough spread to capture the entire possible Pareto solutions which is a drawback since the entire design space is a group of discontinuous discrete regions. The adaptive weighted scheme (AWS) for discontinuous nonconvex design space is one of the promising technique to extract the Pareto front according to Lin et al [25]. Combining AWS and MDPSO could be one of the possible approach to extract the entire Pareto solution from a nonconvex and discontinuous design space with mixed discrete and continuous design variables.

By imposing a reliability criteria such as, minimising the overall reliability (reliability of the solder interconnect was extracted by inserting the accumulated plastic strain values into the Coffin Manson equation (equation (7)) and from the plots in Figures (9) and (11), we can conclude that, Least thickness value of the copper foil generated least accumulated average plastic strain in solder bump and solder layer. Young's modulus of copper is higher than other material in the package, hence thicker copper foil introduces more stiffness to deform of the whole package. The solder material with large CTE in comparison with other materials in the package, experience more strain. In contrast thicker copper foil dissipate more heat from the package. Other issue is the cost, increase in copper thickness will increase the cost. Hence a design engineer has to choose an optimum thickness of copper foil with two conflicting requirements such as the effective heat dissipation and the solder layer/bump reliability.

Increment in FR4 PCB thickness resulted in decrement in accumulated plastic strain in the solder layer, hence an increment in reliability of the solder layer. In contrast, FR4 thickness has positive correlation with the accumulated plastic in the solder bump, hence a negative correlation with solder bump reliability. This characteristics was observed for all the underfill materials. Hence a FR4 PCB board maximum allowable thickness could maximise the overall thermo-mechanical reliability.

VIII. CONCLUSION

An assembly exercise to design and build a smart energy efficient, compact, low BOM count LED driver using silicon based Later IGBT (LIGBT) device together with chip on board technology was proposed by consortium of UK universities. Part of the assembly exercise, finite element modelling predictions for underfill dielectric breakdown failure and solder joint fatigue failure were undertaken on the LIGBT package. Electrostatic finite element modelling was employed to estimate the electric field distribution in the underfill of the LIGBT device package. Based on the electrostatic finite element analysis, five commercial underfill were selected for their high dielectric breakdown strength values.

Thermo-mechanical finite element modelling were simulated for various combination of the design parameters (discrete and continuous) in order to predict the accumulated plastic strain in the solder layer/bump and hence the prediction of the solder reliability. A design optimisation analysis involving computer model with mixed, discrete design variable (underfill type) and continuous design variables (PCB thickness and copper foil thickness) was embarked. A multi-objective design optimisation analysis was undertaken to minimise the plastic strain in the solder interconnect (solder bump and solder layer of the LIGBT package) by utilising a computer model and multi-objective mixed discrete particle swam optimisation (MOO-MDPSO) optimiser. The Pareto front does not have a good spread on the entire possible Pareto solutions. Hence from the analysis, it was concluded that

- The model with thin copper foil layer generated lower value of accumulated plastic strain in the solder interconnect, hence higher reliability
- PCB thickness has positive correlation with the reliability of the solder layer, but it has negative correlation with the reliability of the solder bump

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APPENDIX A

Table: Design of experiments of continuous and discrete design space and the subsequent accumulated plastic strain and fatigue lifetime of the solder bump and layer

Scaled Copper Foil Thickness ($x_{Copper\ Foil}$)	**Scaled FR4 Thickness (x_{FR4})**	**Underfill Type ($z_{Underfill}$)**	**Accumulated Plastic strain of Solder Layer between die and copper foil ($\times 10^{-3}$)**	**Accumulated Plastic strain of Solder bump within the underfill ($\times 10^{-3}$)**	**Lifetime of solder layer between die and copper foil**	**Lifetime of solder bump within the underfill**
-1	-1	'A'	20.781	12.825	1825.1	3644.7
-1	-1	'B'	20.472	13.203	1864.7	3496.1
-1	-1	'C'	21.865	11.239	1696.8	4403.9
-1	-1	'D'	21.505	14.552	1737.7	3041.3
-1	-1	'E'	20.643	12.881	1842.7	3622.2
-1	1	'A'	20.720	12.899	1832.8	3614.8
-1	1	'B'	20.433	13.266	1869.9	3472.3
-1	1	'C'	21.732	11.350	1711.8	4342.2
-1	1	'D'	21.456	14.623	1743.4	3020.2
-1	1	'E'	20.591	12.951	1849.3	3594.2
1	-1	'A'	21.143	12.775	1780.5	3665.5
1	-1	'B'	20.867	13.123	1814.3	3526.8
1	-1	'C'	22.152	11.254	1665.4	4395.5
1	-1	'D'	22.018	14.484	1680.0	3061.7
1	-1	'E'	21.013	12.825	1796.3	3644.7
1	1	'A'	21.096	12.841	1786.1	3638.3
1	1	'B'	20.845	13.178	1817.1	3505.7
1	1	'C'	22.035	11.355	1678.2	4339.6
1	1	'D'	21.982	14.544	1683.9	3043.7
1	1	'E'	20.975	12.888	1801.0	3619.4
0	0	'A'	20.962	12.840	1802.6	3638.7
0	0	'B'	20.679	13.197	1838.0	3498.5
0	0	'C'	21.977	11.307	1684.5	4365.7
0	0	'D'	21.780	14.559	1706.3	3039.0
0	0	'E'	20.832	12.891	1818.8	3618.3
-0.7803	0.7583	'A'	20.793	12.885	1823.6	3620.7
-0.7803	0.7583	'B'	20.508	13.249	1860.1	3478.8
-0.7803	0.7583	'C'	21.802	11.340	1703.9	4347.7
-0.7803	0.7583	'D'	21.546	14.608	1733.0	3024.4
-0.7803	0.7583	'E'	20.664	12.936	1840.0	3600.2
0.6103	-0.4039	'A'	21.070	12.809	1789.3	3651.5
0.6103	-0.4039	'B'	20.795	13.159	1823.4	3513.0
0.6103	-0.4039	'C'	22.073	11.289	1674.0	4376.2
0.6103	-0.4039	'D'	21.940	14.519	1688.5	3051.2
0.6103	-0.4039	'E'	20.942	12.859	1805.1	3631.0

APPENDIX B

Table: Kriging process model (equations (14) and (15)) coefficients

Copper Foil Thickness ($x_{Copper\ Foil}$)	**FR4 PCB Thickness (x_{FR4})**	**Underfill Type ($z_{Underfill}$)**	$\alpha_i^{SolderLayer}$ **(Equation (7))**	$\alpha_i^{SolderBump}$ **(Equation (8))**
-1	-1	'A'	-0.055	2.032
-1	-1	'B'	-0.260	-4.552
-1	-1	'C'	0.097	-1.456
-1	-1	'D'	0.081	0.742
-1	-1	'E'	0.176	3.180

-1	1	‘A’	-2.927	12.110
-1	1	‘B’	-21.680	-26.595
-1	1	‘C’	-0.589	-8.586
-1	1	‘D’	-4.458	4.755
-1	1	‘E’	23.644	18.659
1	-1	‘A’	-0.139	6.963
1	-1	‘B’	-4.728	-15.702
1	-1	‘C’	0.093	-4.894
1	-1	‘D’	-1.213	2.610
1	-1	‘E’	4.871	10.993
1	1	‘A’	-0.043	3.373
1	1	‘B’	-0.842	-7.620
1	1	‘C’	0.049	-2.382
1	1	‘D’	-0.154	1.240
1	1	‘E’	0.741	5.332
0	0	‘A’	-1.543	6.726
0	0	‘B’	-19.470	-14.793
0	0	‘C’	-0.421	-4.708
0	0	‘D’	-4.930	2.705
0	0	‘E’	21.130	10.368
-0.7803	0.7583	‘A’	4.020	-15.776
-0.7803	0.7583	‘B’	31.490	34.625
-0.7803	0.7583	‘C’	0.903	11.170
-0.7803	0.7583	‘D’	6.754	-6.215
-0.7803	0.7583	‘E’	-34.339	-24.295
0.6103	-0.4039	‘A’	0.660	-13.505
0.6103	-0.4039	‘B’	15.155	30.322
0.6103	-0.4039	‘C’	-0.046	9.498
0.6103	-0.4039	‘D’	3.954	-5.112
0.6103	-0.4039	‘E’	-15.980	-21.213