NOVEL APPROACHES IN RF/ANALOG CMOS SPECTRUM SENSING AND ITS APPLICATIONS

A Dissertation

by

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ABSTRACT

Real time spectrum sensing refers to searching for possible signals at a specific time and location, which is applicable to cognitive radio (CR) for primary signal detection and ultra-wideband (UWB) radio for interferer detection. There are several approaches for spectrum sensing. Choosing a proper method for spectrum sensing necessitates evaluating several trade-offs among sensing time, accuracy, power consumption and simplicity of implementation.

In this dissertation several approaches for spectrum sensing along with the applications to CR and UWB receivers are presented. A novel simple spectrum sensing technique for detecting weak primary signals with negative signal-to-noise ratio (SNR) is proposed, which is called quasi-cyclostationary feature detection (QCFD) technique. Moreover, a simple, reliable, and fast real-time spectrum sensing technique based on phasers, which are dispersive delay structures (DDSs), is proposed. Lastly, a UWB receiver robust to the narrowband (NB) blockers, in the vicinity of UWB frequency, is presented. To increase the robustness of the UWB receiver towards interferers, a dynamic blocker detector, utilizing a phaser-based real time spectrum sensing technique, is employed. The proposed spectrum sensing methods provide the best solutions for the intended applications, considering the trade-offs, compared to the state-of-the-art CMOS spectrum sensors.

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Contributors

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1. INTRODUCTION AND LITERATURE REVIEW*

Current congestion of radio devices in the radio spectrum necessitates intelligent use of wireless channels to improve performance of wireless communications via reusing the licensed bands, while primary users are inactive. Spectrum sensing which is the process of detecting signals has a significant role for future usage of frequency bands. Using spectrum sensing for signal or blocker detection enables more efficient use of the currently assigned radio spectrum. For instance, cognitive radio (CR) devices use spectrum sensing for detecting unoccupied licensed frequency bands at a specific time and location [1]. Ultra-wideband (UWB) devices can also employ spectrum sensing for interferer detection.

1.1 Spectrum sensing in cognitive radio devices

CR devices are smart secondary users that detect "white space", which are frequency bands that are not being used by primary users at a specific time and location, through dynamic spectrum access (DSA) (see Fig. 1.1). They use spectrum sensing methods for white space detection to operate on these empty bands on a non-interfering basis [1, 2]. IEEE 802.22 is a standard on Wireless Regional Area Networks (WRANs) which operate in low population density areas to provide broadband access to data networks [1]. According to Federal Communications Commission (FCC), due to some restrictions [3], unlicensed use of white space, by WRAN systems, is allowed only for VHF/UHF TV broadcast bands (54-862 MHz) as low population density areas. CR devices operate in two modes [1]; sensing mode, in which no data is sent by the cognitive transmitter, however the spectrum sensor and part of the cognitive receiver (depending on the spectrum sensor structure) are active, and transmission mode, in which data is transmitted from cognitive transmitter

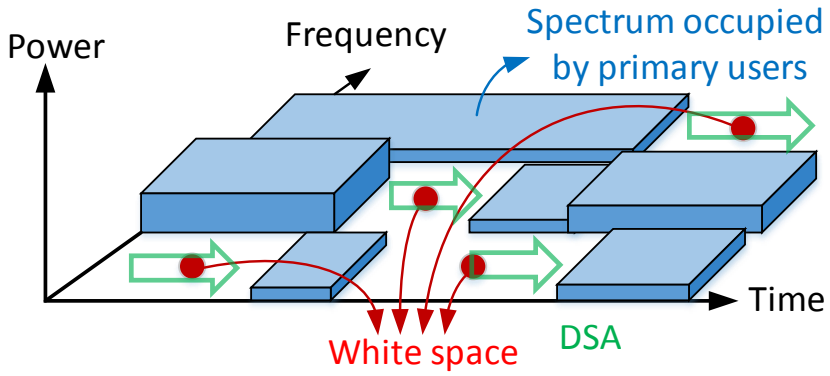

Figure 1.1: Concept of white space for CR devices.

and received by cognitive receiver, but spectrum sensing part is inactive. It is desired to minimize sensing time to increase data transmission time.

Spectrum sensing is the process of finding white spaces for CRs. The job of a spectrum sensor is detecting primary signals for a CR user. When a secondary user selects an empty primary user band, the band can be reclaimed by a primary user and it is also shared with other secondary users that selected the same band [1]. Spectrum sensing has different approaches considering trade-offs among sensing time, accuracy, power consumption and simplicity of implementation [2, 4]. One approach is non-cooperative or transmitter detection which refers to detection based on information sent from a primary transmitter to only one CR user [4]. Transmitter detection itself can be classified into three groups [4, 5]: 1) matched filter detection, 2) energy detection (ED) [6], and 3) cyclostationary feature detection (CFD) [7]. Matched filter detection, is based on correlating the unknown signal with a filter whose impulse response is the mirror and time shifted version of a reference signal. This filter maximizes the signal to noise ratio (see Fig. 1.2a). This method needs a preliminary knowledge of the primary user signal (reference signal) and should be implemented in discrete time domain. The realization of this filter in continues time domain is difficult [8]. ED measures the energy of the signal and compares it to a threshold

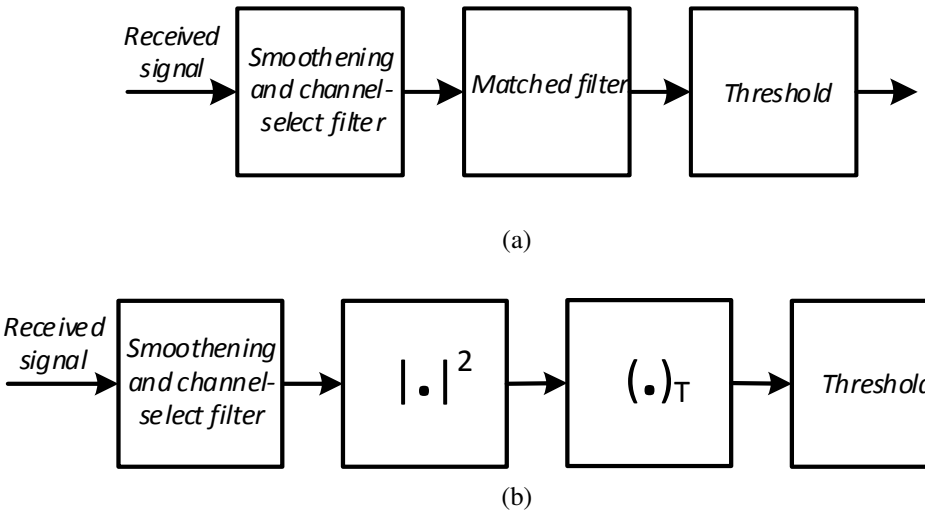

Figure 1.2: Basic block diagram for a; (a) matched filter detection technique, and (b) ED technique.

to determine if there is any primary user in the selected channel. This method is rather fast but cannot guarantee if a channel is empty for low signal to noise ratios (SNRs). For this method first a channel should be selected using filters, then a squarer and an integrator are used to find the energy of the signal (see Fig. 1.2b). CFD refers to a method in which received signals are coupled with periodic signals to make built-in periodicity and hence has the ability to differentiate between noise and modulated signal and achieve high accuracy. This is a complex and time consuming method, and can be used for those channels that have been already considered empty by ED method to reduce the sensing time. This method is further discussed in Chapter 2. Detectors based on any of the methods mentioned above can be realized either in digital or analog domains. Digital approaches commonly use a fast Fourier transform (FFT) block and they need a high bandwidth (BW) analog-to-digital converter (ADC). So while they can be more accurate (not necessarily), area, complexity, power consumption, and sensing time are increased. As a result, analog approaches are more preferable.

There have been quite a few circuit-level implementation of analog spectrum sensors for CRs reported in the literature [9, 10, 11], all use ED method and hence have the problem of low sensitivity. One structure is a digitally-assisted implementation in which digital windows are used instead of bulky tunable filters to select the channel and calculate the energy by correlation-integration to the received RF signal after down-conversion to baseband (BB) and is called multi-resolution spectrum sensing (MRSS) [9]. The decision making for the existence of the signal is performed in digital domain. The main issue with this approach is although multiplying by a window increases the signal to noise ratio, it doesn't act as a channel select filter. Windowing selects all channels with higher signal to noise ratio, it doesn't reject any of them. This means not only the desired channel has higher SNR but the non-desired channels have higher SNR without any rejection, so it does not increase the maximum interference to noise ratio (INR_{max}), which is the highest level of the signal in the adjacent channels to the level of noise that can be rejected by the detector. A more advanced MRSS technique is explored in [10] and is called spread spectrum technique. This technique correlates the received RF signal (using a mixer and an integrator) with a spread signal created by a synthesizer and is matched to the input signal. This makes a non-perfect autocorrelation (energy) of the input RF signal. The other implementation uses an adder-merged low-pass filter (LPF) followed by two cascaded second-order tunable low-pass BB filters to select the channel BW [11]. The second-order BB filters consist of four circuit units arranged in parallel and operate at optimized noise and power consumption in accordance with the desired signal level by changing the number of active circuit units. This method is based on a received signal strength indicator (RSSI) circuit; rectifiers and limiters are used as a squarer, and an RC filter is used as an integrator. The decision is made in digital unit. While this architecture covers frequencies from 30 MHz to 2.4 GHz, it can only be used as an interferer detector for frequencies above 862 MHz. It achieves higher sensitivity compared to [9] but still doesn't cover negative SNRs.

In Chapter 2, a CMOS analog spectrum sensor for a CR receiver is presented based on both energy and feature detection methods to compromise between these two methods and use the advantage of both while eliminating their downsides.

1.2 Real-time spectrum sensors

Conventional analog integrated spectrum sensing blocks use ED techniques [9, 11, 10, 12] and quasi-cyclostationary feature detection (QCFD) technique [13] for signal detection. The former calculates energy of the incoming signal and compares it to a threshold while the latter takes advantage of CFD techniques for eliminating the effect of input noise in decision making. Both methods are implemented after frequency down-conversion of the incoming RF signal to BB, which may introduce several non-linearity terms to the original signal and fill more white spaces. Impact of down-conversion on the accuracy of white space detection is studied in [14]. Besides, conventional real-time spectrum sensors usually require use of a wideband, fast-sweeping frequency synthesizer [9, 12, 15] or a wideband ADC [16, 17] along with the down-converter and spectrum sensing block, which both are complex and power hungry.

For a real-time spectrum sensor, all the channels in a frequency band need to be detected in a specific time (sensing time). As mentioned earlier, in a CR transceiver, this sensing time needs to be minimized so that the data transmission time can be maximized. Sensing process should be performed periodically to ensure accuracy of detected white space and avoid interfering with primary users.

An analog discrete real-time spectrum sensor is implemented in [18] which uses a dispersive delay structure (DDS), or "phaser", to separate channels with different frequencies in time domain. This is performed by assigning different delays to different frequencies in a time-limited modulated signal. Fig. 1.3 shows the basic architecture of this spectrum sensor. The phaser in [18] is an all-pass filter (APF) realized with an off-chip transmission

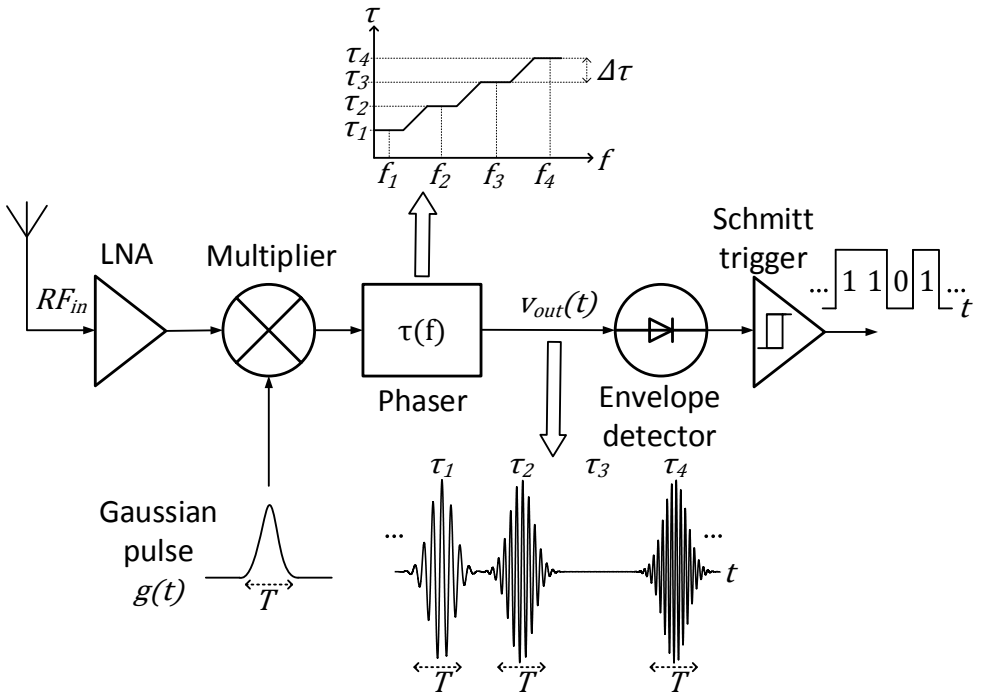

Figure 1.3: Principle of a phaser-based real-time spectrum sensor.

line with a stepped group-delay (GD) characteristic (as shown in Fig. 1.3) creating a specific delay for each frequency channel. The incoming modulated signal is time-limited by multiplication with a Gaussian pulse and then passes through the phaser for conversion of frequency difference to time difference and is finally converted to "1"-"0" pattern by an envelope detector and a Schmitt trigger, indicating the presence and absence of the signal in the corresponding channel. The reason for using Gaussian pulse instead of rectangular is to make the transitions smoother and reduce sideband power. A Gaussian pulse has also a Gaussian shape in frequency domain and achieves a small time-BW product as follows:

$$\Delta t_G \Delta \omega_G = \frac{\sigma}{\sqrt{2}} \times \frac{1}{\sqrt{2}\sigma} = \frac{1}{2} \tag{1.1}$$

where σ is the standard deviation of the Gaussian pulse. BW of the Gaussian pulse

($\Delta\omega_G = \frac{1}{\sqrt{2}\sigma}$) should be smaller than the frequency steps of the phaser.

Phaser-based spectrum sensors are simple, wideband, fast, and don't require frequency down-conversion and wideband synthesizer and operate at RF frequency. Time-frequency resolution of the conventional phasers, which is the GD difference for two consecutive channels, is determined by their GD slope in a GD vs. frequency response. However, these phasers cannot be realized on-chip for frequencies less than a few gigahertz due to large transmission lines used in these topologies. Other applications of phasers can be found in [19].

Using the idea of analog spectrum sensing with phasers which employ GD characteristics of a filter, a CMOS integrated real-time spectrum sensor is proposed, which utilizes a practical on-chip phaser, suitable for CR applications [20]. The proposed real-time spectrum sensing method simplifies measuring in a more realistic environment when more than one channel is occupied and employs a simple tunable filter with band-pass (BP) magnitude and GD response as a phaser. Chapter 3 discusses the proposed method and feasibility of on-chip phasers. The integrated spectrum sensor functionality with a decision circuit is also evaluated.

1.3 UWB receivers

According to FCC, a signal with a BW of greater than 500 MHz is considered as UWB [21]. Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) systems provide high-speed, short-range wireless communication over 3.1-10.6 GHz spectrum with fourteen 528 MHz sub-bands and support data rates of 53.3-480 Mbps [22, 23]. The FCC power spectral density emission limit for UWB transmitters is -41.3 dBm/MHz to minimize the interference with narrow-band (NB) systems operating at the same frequency band. The standard assumes a noise figure (NF) of 6.6 dB for the UWB receiver to achieve a sensitivity of -80.8 dBm (for data rate of 53.3 Mbps) to -70.4 dBm (for data

INT1 (f_{INT1} (MHz))	INT2 (f_{INT2} (MHz))	P_{INT1}/P_{INT2} (dBm)	IIP3 (dBm)
UMTS (1900)	802.11b/g (2440)	-23/-20	1.7
WiMAX (3500)	802.11b/g (2440)	-20/-20	0.6
GSM (450)	UMTS (1900)	-25/-23	0.5
GSM (450)	DCS (1800)	-25/-22	-1.6

Table 1.1: Out-of-Band IIP3 Requirements for the First UWB Band Group

INT1 (f_{INT1} (MHz))	INT2 (f_{INT2} (MHz))	P_{INT1}/P_{INT2} (dBm)	IIP2 (dBm)
DCS (1800)	DCS (1800)	-22/-22	22.4
UMTS (1900)	UMTS (1900)	-23/-23	26.6
UMTS (1900)	802.11b/g (2440)	-23/-20	23.6
802.11b/g (2440)	802.11b/g (2440)	-20/-20	23.6
HiperLAN2 (5480)	GSM (780)	-18/-30	16.3
HiperLAN2 (5480)	DCS (1800)	-18/-22	24.3
HiperLAN2 (5480)	UMTS (1900)	-18/-23	26.4
HiperLAN2 (5710)	802.11b/g (2440)	-18/-20	26.4

Table 1.2: Out-of-Band IIP2 Requirements for the First UWB Band Group

rate of 480 Mbps).

UWB devices need to function properly in the vicinity of strong NB systems. These NB interferers can saturate the UWB systems, causing desensitization and compression of the receiver. Besides, the second and third order intermodulation products (IM2 and IM3) of these blockers can fall within the UWB frequency band. Usually an off-chip band-pass filter (BPF) is placed after the antenna in the receiver path to select the desired UWB frequency band and attenuate out-of-band blockers, relaxing the linearity requirement of the receiver to some degree.

Table 1.1 and 1.2 show the out-of-band third-order input intercept point (OB-IIP3) and

out-of-band second order input intercept point (OB-IIP2) requirements for the strictest cases in the first UWB group (3.1-4.8 GHz), when the data rate is at its highest (480 Mbps) [24]. For each interferer in Table 1.1 and 1.2 and also for the UWB signal, the received power is considered to be at an antenna located at 1 m distance from a transmitter, transmitting the maximum allowable power (assuming a free space model for the path loss). Maximum power of the received UWB signal within 3.1-10.6 GHz band is -30 dBm. For the values in Table 1.1 and 1.2, it is also assumed an off-chip RF BPF [25] is employed after the antenna to attenuate the blockers outside the UWB band (3.1-10.6 GHz). The amount of each blocker power, after its attenuation by the RF filter, is also mentioned in these tables. On the other hand, the in-band IIP3, coming from two adjacent UWB channels, is much more relaxed, requiring a minimum IIP3 of only -18 dBm [24].

In addition to using off-chip BPFs, several techniques have been used to improve the UWB system robustness towards interferers including using on-chip tunable BPFs, and notch filters. Tunable BPFs enhance linearity by dividing the entire band to smaller sub-bands, alleviating the interferer issues associated with UWB systems [26, 27]. Better out-of-band linearity performance is obtained by increasing the number of smaller sub-bands, which requires using higher Q filters. Notch filters improve OB-IIP3 and OB-IIP2 by rejecting the blockers. Location of notch frequencies can be set to the possible locations of the blockers, which are known (see Table 1.1 and 1.2). Notch filters used in [28, 29] reject the interferers in 5-6 GHz frequency band using passive on-chip components. In addition to the large area, these filters suffer from low Q leading to low rejection and some attenuation in the desired band. Besides, they just target interferes in a specific band.

Using on-chip high-Q BP or notch filters surpasses using low-Q ones in terms of out-of-band linearity performance, requiring active configurations. Active high-Q filters occupy less area compared to passive ones at the cost of more power consumption. Using active, high-Q, tunable BPFs for the entire band is not practical due to large power con-

sumption. Since the possible location of blockers is known, less number of notch filters is required, making them more practical compared to BPFs. In [30], a dual-band high-Q CMOS active notch filter is used, rejecting blockers at 2.4 GHz and 5.2 GHz. However, it doesn't provide any flexibility regarding the location of the blockers and rejects two blockers at two fixed points. To add some flexibility in using high-Q notch filters and reduce the total number of required filters, tunable notch filters can be employed. However, for using tunable notch filters a dynamic system detecting the location of blockers at a specific time is required. A tunable CMOS notch filter for 5-6 GHz blockers is employed in [31], which rejects the strongest blocker in this band, assuming that the largest one is mostly responsible for the deterioration of the linearity performance [32]. Location of the strongest blocker in [31] is obtained by observing the response of a tunable RF BPF, without implementing the actual energy detector. Using a tunable notch filter and knowing the exact location of the blocker eliminates the need of having several active, high-Q notch filters, making this structure more efficient in terms of noise and power consumption. This technique doesn't address non-linearity issues from blockers which are located in other frequency bands including 802.11b/g.

In Chapter 4, a receiver front-end (RFE) plus BB filters, for MB-OFDM UWB radios operating in the first band group is proposed, utilizing three tunable active notch filters, for interferer rejection [33]. Each filter is associated with a specific frequency band corresponding to the possible interferer locations (2.35-2.75 GHz, 5.1-5.5 GHz, and 5.5-5.9 GHz). The locations of interferes are determined using a phaser-based spectrum sensor [20], which is more suitable for interferer detection than conventional spectrum sensing techniques [9, 10, 11, 12, 13]. The reason behind this is the elimination of frequency down-conversion in phaser-based spectrum sensors. Using mixers for down-converting strong blockers can lead to compression and desensitization of the system and its elimination improves linearity and reduces false detection.

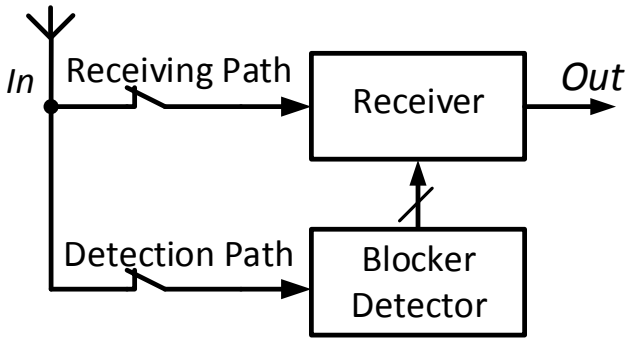

Figure 1.4: Conceptual block diagram of the proposed system.

Fig. 1.4 shows the conceptual block diagram of the proposed system. The entire system works as follows; first the blocker detector is activated, while the receiver is deactivated, and the input signal is directed to the detection path. Then the frequency locations of up to three simultaneous blockers are reported to the notch filters of the receiver, which reject the blockers in the receiving path, when the receiver is activated and the detector is disconnected.

2. QUASI-CYCLOSTATIONARY FEATURE DETECTION*

The objective of this chapter is to find the best solution for detecting weak primary signals in DVB-T band. The ultimate goal is detecting signals with negative SNR, while keeping the method simple and fast, as both sensitivity and sensing time are the key parameters in designing spectrum sensors for CR applications. The proposed QCFD method in this chapter is based on CFD techniques, which are very accurate, while avoiding their slow characteristic.

2.1 Basic idea

2.1.1 Cyclostationary feature

A signal is called to have first order periodicity if it is periodic with a specific period; $x(t) = a\cos(2\pi\alpha t + \theta)$ is periodic with period of $1/\alpha$. The power spectral density (PSD) of this signal has components at frequency of α, so detection of this signal based on its spectrum is easy. A signal is called to have second order periodicity or is cyclostationary when its autocorrelation is a periodic function of t with a period corresponding to carrier frequency [7, 34, 35]. Autocorrelation of $x(t)$, $R_x(t,\tau)$, is given by:

$$R_x(t,\tau) = E\left(x\left(t+\frac{\tau}{2}\right)x\left(t-\frac{\tau}{2}\right)^*\right) \tag{2.1}$$

Where τ is the time shift between two correlated signals. The Fourier coefficient of autocorrelation function of $x(t)$ which is called cyclic autocorrelation with the cyclic fre-

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quency of α, $R_x^\alpha(\tau)$, is defined as [7, 34, 35]:

$$R_x^\alpha(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_T x(t+\frac{\tau}{2}) x(t-\frac{\tau}{2})^* e^{-j2\pi\alpha t} dt \tag{2.2}$$

Fourier transform of a cyclic autocorrelation is called spectral correlation function (SCF) which for a cyclostationary signal has components at frequency of α, and can be used for detection of the signal:

$$S_x^\alpha(f) = F\{R_x^\alpha(\tau)\} = \int_{-\infty}^{+\infty} R_x^\alpha(\tau) e^{-j2\pi f\tau} d\tau \tag{2.3}$$

Modulated signals are cyclostationary processes while noise is not, so SCF of modulated signals has components at frequency of α while SCF of noise is zero [7, 34, 35]. This is the idea behind CFD which can detect signals with low SNRs:

$$S_y^\alpha(f) = S_x^\alpha(f) + S_w^\alpha(f) = S_x^\alpha(f), \alpha \neq 0 \tag{2.4}$$

Where x denotes pure signal, w is white noise and y is signal with noise. Energy detector operates on SCF for $\alpha = 0$, thus noise uncertainty limits the detection, while feature detector operates on SCF for $\alpha \neq 0$, where noise has no components so detection of low SNR signals is possible. Using FFT in CFD, all possible values of α for different frequencies can be considered. For a modulated signal $x(t)$ with modulation frequency of f_c, α is a non-zero integer factor of f_c ($\alpha = mf_c, m = 1, 2, ...$) [7, 34, 35]. From (2) and (3), CFD for a single frequency of α can be shown using block diagram of Fig. 2.1 [34, 35]. The smoothening filter is used to obtain a substantial reduction in random effects which results in a better SCF. Note that Fig. 2.1 is the continues time realization of the CFD method. Discrete time realization requires the use of FFT [35].

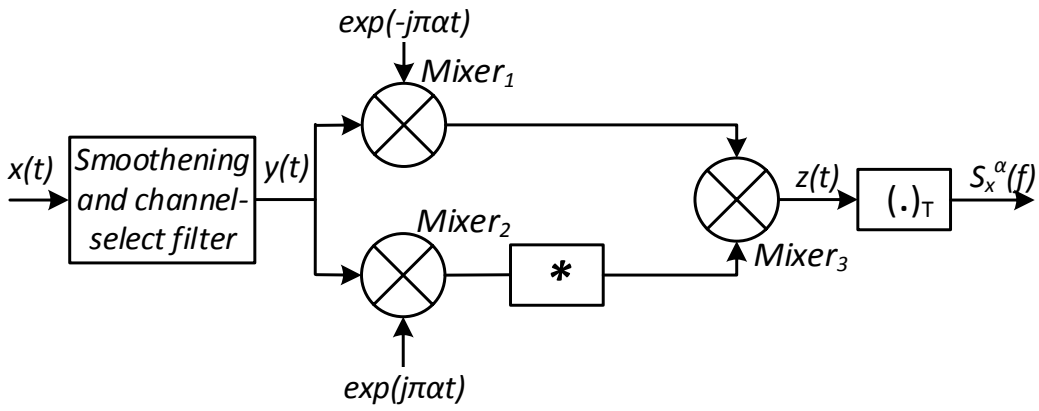


Figure 2.1: Basic block diagram for a CFD technique.

2.1.2 DVB-T signals and QCFD technique

Digital Video Broadcasting-Terrestrial (DVB-T) is a standard for the broadcast transmission of digital terrestrial television which uses Orthogonal Frequency-Division Multiplexing (OFDM) modulation [36]. Here the primary signal is assumed to be a DVB-T signal. For a BB DVB-T signal with OFDM modulation, each sub-carrier is modulated using one of B/QPSK, 16/64/256QAM modulations. In an OFDM symbol, orthogonality of the sub-carriers destroys cyclostationary feature of OFDM signals [37], so α cannot be easily an integer factor of f_c. Cyclic prefix (CP), which is inserted at the beginning of each OFDM symbol interval as a guard interval, and is the copy of the last part of the symbol (see Fig. 2.2), creates cyclostationary feature and protects DVB-T signal against inter-symbol interference (ISI) [37]. In Fig. 2.2, Δ is the timing duration of the CP, and T_U is the symbol part duration, and $T_S = T_U + \Delta$ is the total symbol duration. Considering the cyclostationary feature created by CP, the cyclic frequencies of the received signal cyclic autocorrelation are defined as: $(\alpha = m/T_S, m = 1, 2, ...)$ [38].

The pilot carriers aid the receiver in reception, demodulation, and decoding of the re-

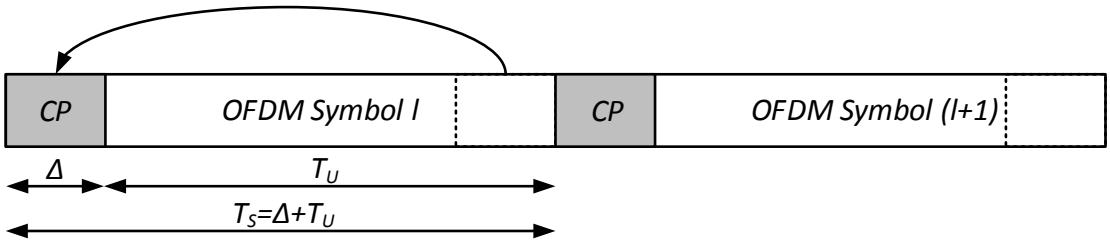


Figure 2.2: CP in an OFDM symbol.

ceived signal [37]. Two types of pilots are included in an OFDM DVB-T signal: scattered pilots and continual pilots. The scattered pilots are uniformly spaced among the carriers in any given symbol, while, the continual pilots occupy the same carrier consistently from symbol to symbol. The location of all pilots is defined by the DVB-T standard [1, 36]. Fig. 2.3 illustrates the pilot spacing for a DVB-T OFDM frame where $(k = 0, ..., K_{max})$ represent carriers and $(l = 0, ..., 67)$ represent symbols. Cyclostationary feature also exists between each two pilots. Cyclic frequency of the cyclic autocorrelation between each two pilots is defined as: $(\alpha = \Delta k/T_U)$ [38, 39], where Δk, indicates the difference between each two pilots in each symbol. For a DVB-T signal, as shown in Fig. 2.3, scattered pilots are repeated every twelve carrier in any given symbol so $(\alpha = 12m/T_U, m = 1, 2, ...)$.

Cyclostationary feature created by scattered pilots is stronger than the one created by CP [39]. So here α is chosen based on the scattered pilots. Autocorrelation of the input signal plus noise is the sum of autocorrelations of the data, pilots, and noise, and cross-correlations of the pilots, pilots and data, and signal and noise:

$$R_y(t, \tau) = AC_D + AC_P + AC_n + CC_P + CC_{P,D} + CC_{x,n} \tag{2.5}$$

Where AC denotes the autocorrelation, CC denotes the cross-correlation, P is for pilots, D is for data, n is noise, x is pure signal, and y is signal plus noise. Cyclic autocorrelation

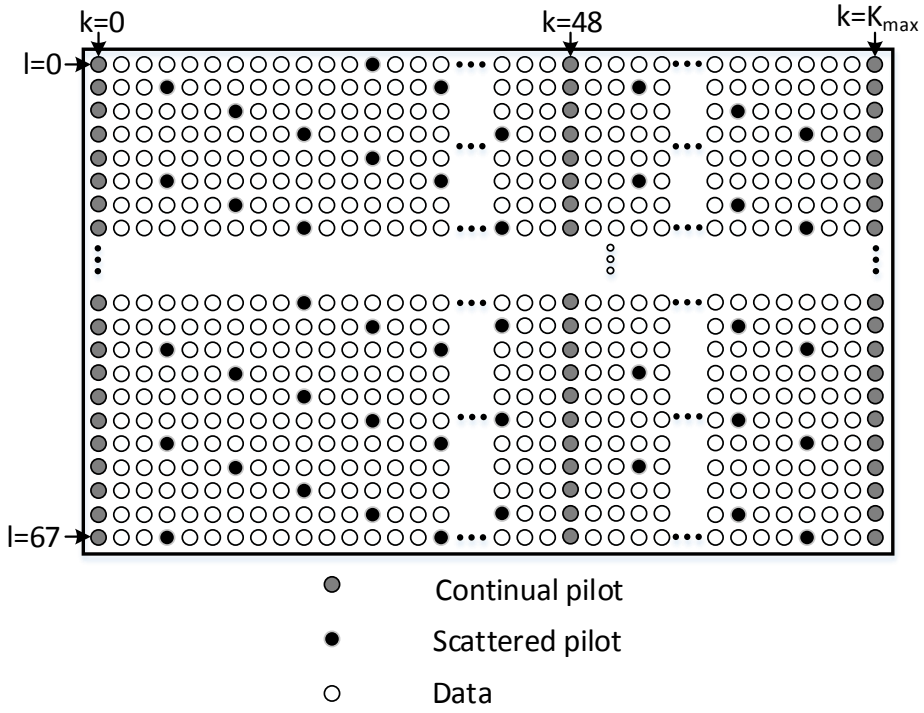


Figure 2.3: Pilot spacing for a DVB-T OFDM frame.

created by scattered pilots can be added constructively to create a strong cyclic autocorrelation. Table 2.1 shows the specifications of DVB-T OFDM symbols for two different modes; 2K and 8K. From this table scattered pilots are repeated in each symbol with a frequency of 10 kHz for 8K mode and 40 kHz for 2K mode. So α can be a factor of 10 kHz or 40 kHz for 8K or 2K mode, within the channel BW, respectively. Simulation of the system in Fig. 2.1 using SystemVue software (version 2013.08) shows that peaking of SCF at frequency of α for a BB DVB-T signal at different acceptable values of α does not change, which makes sense because the SCF of the signal is based on correlation between different carriers (see (2), (3), and (5)) and the peaking does not change with changing α which represents the location of the peaks. So there is no need to evaluate cyclic autocorrelation for different acceptable values of α if only the value of the SCF peak at α is of concern. Note that here the value of α is chosen based on the position of the scattered pi-

Parameter	8K mode				2K mode			
Number of carriers K	6817				1705			
Value of carrier number K_{min}	0				0			
Value of carrier number K_{max}	6816				1704			
Symbol part duration T_U (μs)	*1194.6*				*298.6*			
Carrier spacing $1/T_U$ (kHz)	*0.837054*				*3.348214*			
Scatter pilots repeating frequency $12/T_U$ (kHz)	*10*				*40*			
Spacing between carriers K_{min}&K_{max} $\frac{(K-1)}{T_U}$ (MHz)	*5.71*				*5.71*			
CP	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{32}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{32}$
CP duration Δ (μs)	*298.6*	*149.3*	*74.6*	*37.3*	*74.6*	*37.3*	*18.6*	*9.3*
Symbol duration T_S (μs)	*1493.3*	*1344*	*1269.3*	*1232*	*373.3*	*336*	*317.3*	*308*

Table 2.1: Specifications of OFDM Symbol for Different Modes
Note: Values in italics are approximate values.

lots in the OFDM DVB-T signal and is different if other features of the DVB-T signal such as position of continual pilots or CP is considered or if a different signal with a different modulation is employed.

In an actual feature detector, in which features of an unknown signal including its modulation, needs to be extracted, different values of α need to be considered. But here, only the presence of the OFDM DVB-T signal with the purpose of achieving weak signal detection (not feature extraction) is considered. If there is a peaking at $f = \alpha$, the signal exists and if not the signal does not exist or is lower than the achievable SNR of the detector. This detector can be converted to a conventional energy detector if α=0, which doesn't reject SCF of noise. This method can be implemented in analog domain and doesn't require an FFT and hence is much easier and faster compared to CFD itself, while it is more accurate than ED. It also doesn't need an ADC. We call this method quasi-cyclostationary feature detection or QCFD.

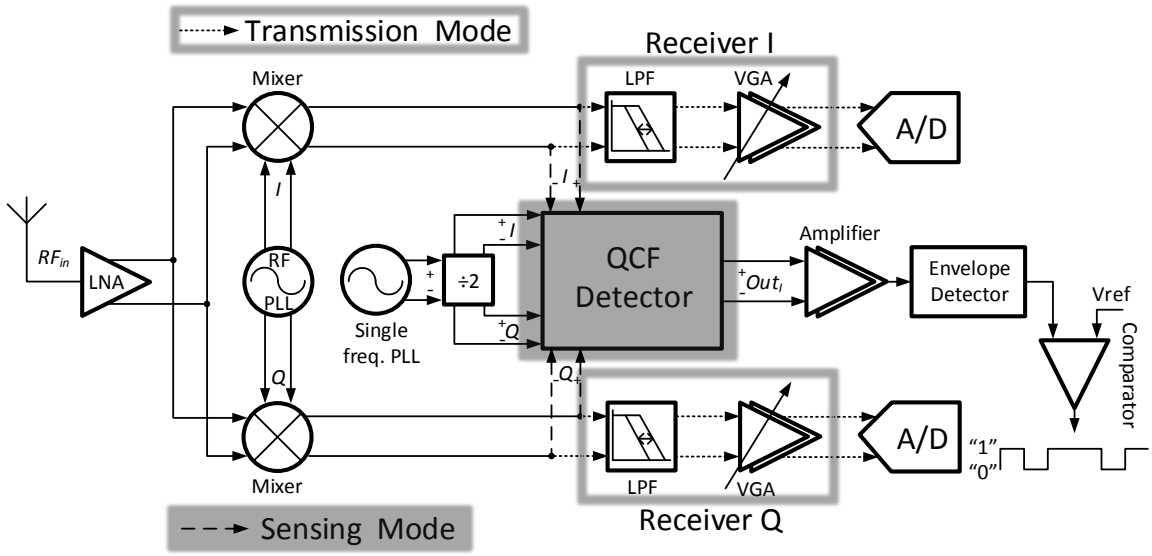


Figure 2.4: Block diagram of a CR receiver with QCF detector.

2.1.3 QCF detector architecture

Fig. 2.4 shows the block diagram of a CR receiver with QCF detector located after down-converter. As shown in Fig. 2.4, in transmission mode, the entire receiver is active and QCF detector is inactive, while, in sensing mode, the low-noise amplifier (LNA) and mixers work as well as the detector. The output of the detector passes through a voltage gain amplifier for amplification to a desired level, then using an envelope detector and a comparator as in [40] a "1"-"0" pattern can be obtained which indicates whether the signal exists or not. In order to implement a QCF detector, the CFD structure shown in Fig. 2.1 needs to be employed to build the autocorrelation function of a signal, but here there is no need to change α so the implementation of the entire system is much easier. Since the goal is to implement the system in analog domain, the multiplication of the signals given by Fig. 2.1 has to be expanded. Here, $y(t)$ is a BB quadrature signal ($y(t) = I + jQ$). So, the output signal of $Mixer_3$, $z(t)$ in Fig. 2.1, after expanding the multiplications of the

complex signals is given by:

$$
\begin{aligned}
& z(t) = \\
& [(I\cos(\pi\alpha t) + Q\sin(\pi\alpha t)) + j(Q\cos(\pi\alpha t) - I\sin(\pi\alpha t))]\times \\
& [(I\cos(\pi\alpha t) - Q\sin(\pi\alpha t)) - j(Q\cos(\pi\alpha t) + I\sin(\pi\alpha t))]
\end{aligned} \tag{2.6}
$$

Due to the similarities in the spectrum of real and imaginary parts of $z(t)$, one of them is enough in analog detection of the incoming signal. As a result, only the real part of the output is considered here. The real part of this expression is:

$$
\begin{aligned}
& Real\{z(t)\} = \\
& [\underbrace{(I\cos(\pi\alpha t) + Q\sin(\pi\alpha t))}_{\text{A}} \times \underbrace{(I\cos(\pi\alpha t) - Q\sin(\pi\alpha t))}_{\text{B}}] + \\
& [\underbrace{(Q\cos(\pi\alpha t) - I\sin(\pi\alpha t))}_{\text{C}} \times \underbrace{(Q\cos(\pi\alpha t) + I\sin(\pi\alpha t))}_{\text{D}}]
\end{aligned} \tag{2.7}
$$

and the imaginary part is:

$$
\begin{aligned}
& Imag\{z(t)\} = \\
& [(Q\cos(\pi\alpha t) - I\sin(\pi\alpha t)) \times (I\cos(\pi\alpha t) - Q\sin(\pi\alpha t))] - \\
& [(I\cos(\pi\alpha t) + Q\sin(\pi\alpha t)) \times (Q\cos(\pi\alpha t) + I\sin(\pi\alpha t))]
\end{aligned} \tag{2.8}
$$

The term, $Real\{z(t)\}$, can be represented by the system shown in Fig. 2.5 which can be implemented using integrated anaolg blocks. As shown in Fig. 2.5, two mixers are required to make each "A", "B", "C", and "D" expressions in (2.7), which can be shared for "A" and "B" expressions ($Mixer_I$ and $Mixer_{II}$), and for "C" and "D" expressions ($Mixer_{III}$ and $Mixer_{IV}$), if voltage signals are added/subtracted rather than current signals. Another

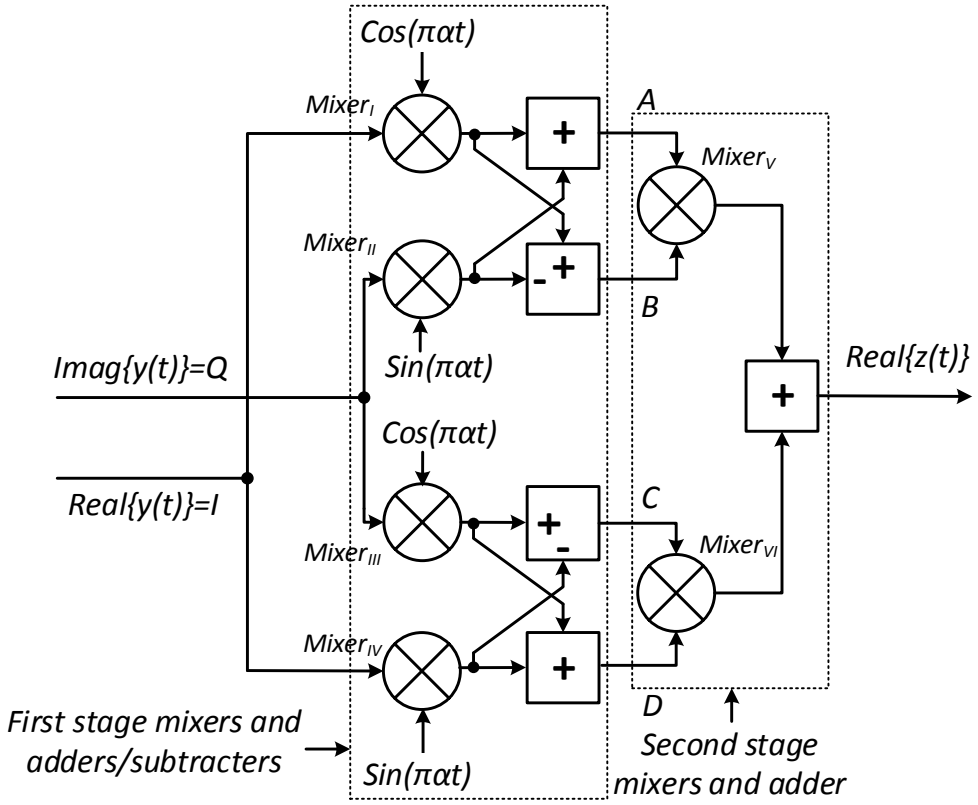


Figure 2.5: Realization of $Real\{z(t)\}$ from Fig. 2.1.

two mixers ($Mixer_V$ and $Mixer_{VI}$) are required to make "AB+CD".

2.2 Circuit implementation

Fig. 2.6 is one possible analog implementation of the QCF detector system shown in Fig. 2.5 (including the smoothening filter and integrator) which is used here. Operational amplifier-RC (Op-amp-RC) structure is used for input LPF and passive mixers are used for multiplication. In Fig. 2.6, transimpedance amplifiers (TIAs) are part of the passive mixers (Gm-Switch-TIA) which are also used as adders/subtracters. TIA_5 with RC feedback has also the role of integrator, which is required by the original system in Fig. 2.1. The imaginary part can be created by adding another TIA as adder. The LO frequency of the first four switch-pairs is $\alpha/2$.

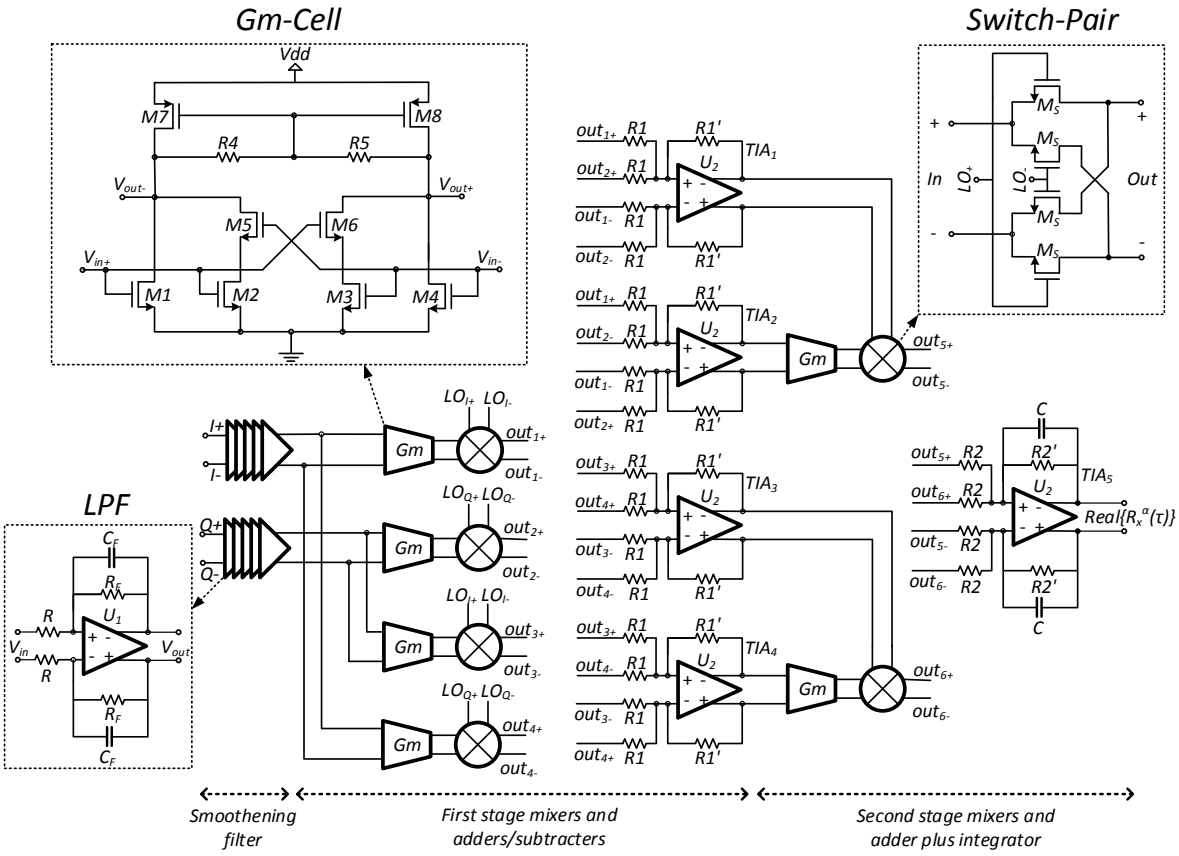


Figure 2.6: Proposed system implementation of the QCF detector.

Noise, linearity and power consumption are the key features in designing each block. For a typical spectrum sensor, noise limits the accuracy and linearity limits the dynamic range (DR) [5]. Low noise feature is required by the detector to detect low level signals and high linearity is required to detect high level signals without saturation. However, a saturated detector still indicates that a signal exists, so in a typical detector linearity is of less concern compared to noise as long as the probability of false alarm (a scenario in which the signal does not exist but the detector detects a signal) due to non-linearity is bearable.

A strong out-of-band blocker may lead to false detection by the detector in the case

of poor linearity, but it is not critical, because it is not a threat to primary users or the CR receiver, as in this scenario neither the CR user is interfering with the primary users nor the CR transceiver is working in a band close to a blocker. It only reduces the number of empty channels. Although it is always desired to have out-of-band interferer detector in addition to signal detector and remove out-of-band interferers for the CR system to increase the number of white spaces.

As mentioned in the previous section, SCF of noise is zero for $\alpha \neq 0$. This feature relaxes the low noise characteristic of each block in QCF detector to some degree. So each block of the QCF detector is designed to provide high enough linearity and low power consumption. The following sub-sections discuss the transistor-level implementation of each block.

2.2.1 Input filters

The detector is placed after the down-converter as shown in Fig. 2.4. This means that a BB LPF with a BW equal to the down-converted channel BW, 4 MHz, (half of RF channel BW) is required at the beginning of the detector to attenuate adjacent channels and decrease false alarm probability. Note that this BB LPF in sensing mode is not the same as receiver BB LPFs in transmission mode due to the fact that the detector BB LPF has a fixed BW chosen based on primary signal channel BW, while the receiver BB LPFs in the transmission mode, which are for secondary signals, are not based on the primary signal channel BW. Here, five cascade first-order op-amp-RC LPFs, which compose a fifth order LPF, are employed for each I and Q paths (LPF in Fig. 2.6) to remove the effect of adjacent channels to some degree. BW of each BB active-RC LPF is around 22 MHz, which makes a total BW of around 10 MHz to guarantee that the main channel is not attenuated much.

A fully differential folded-cascode op-amp is used in the filter [41] (U_1 in Fig. 2.6). U_1 transistor-level implementation is shown in Fig. 2.7. A continuous common mode

feedback (CMFB) circuit is adopted in order to suppress variations at the output common mode and is used with four common source transistors (M1 to M4), as voltage controlled resistors, operating in the linear region. A change in the tail current (M6) leads to the adjustment of the bias currents when the DC of output voltage is different from the desired one. There are two methods employed here to increase the gain; one is using the symmetric output branch consisting of common gate transistors (M16 to M19) with cascode current loads (M10, M11, M24, and M25), and the other is using common-source gain boosting transistors (M12 to M15, and M20 to M23). Ten op-amps are used in the filter, five in each I and Q paths, so power consumption is critical here. This structure can be designed in a way to have low power consumption considering that M1, M2, M3, and M4 operate in linear region and gain is high enough. Simulating this op-amp in 0.18-μm CMOS IBM technology results in gain-BW (GBW) product of 170 MHz for a 20 pF load, and phase margin (PM) of 72.4^o. The whole filter section (including 10 U_1 op-amps) only draws 4.3 mA from a 1 V power supply (*Vdd'*).

2.2.2 Mixers and adders/subtracters

Passive mixers are used in Fig. 2.6. They have the advantage of higher linearity compared to active mixers [42]. Besides, ten mixers are required if active structures are employed, while this number is reduced to six (with two mixers sharing one TIA) using passive structures. The reason behind this is that a passive structure can be easily modified in a way to add voltage signals rather than current signals by introducing another resistor at the output of switch-pair, compared to conventional current-driven passive mixers. Adding voltage signals has the advantage of reusing the two mixers used for building each expression in (2.7), reducing the total number of mixers. This simplifies the system and reduces power consumption. This is clarified in Fig. 2.8 in which currents are added rather than voltages in two active Gilbert cell mixers to make expression "A" in (2.7) and hence

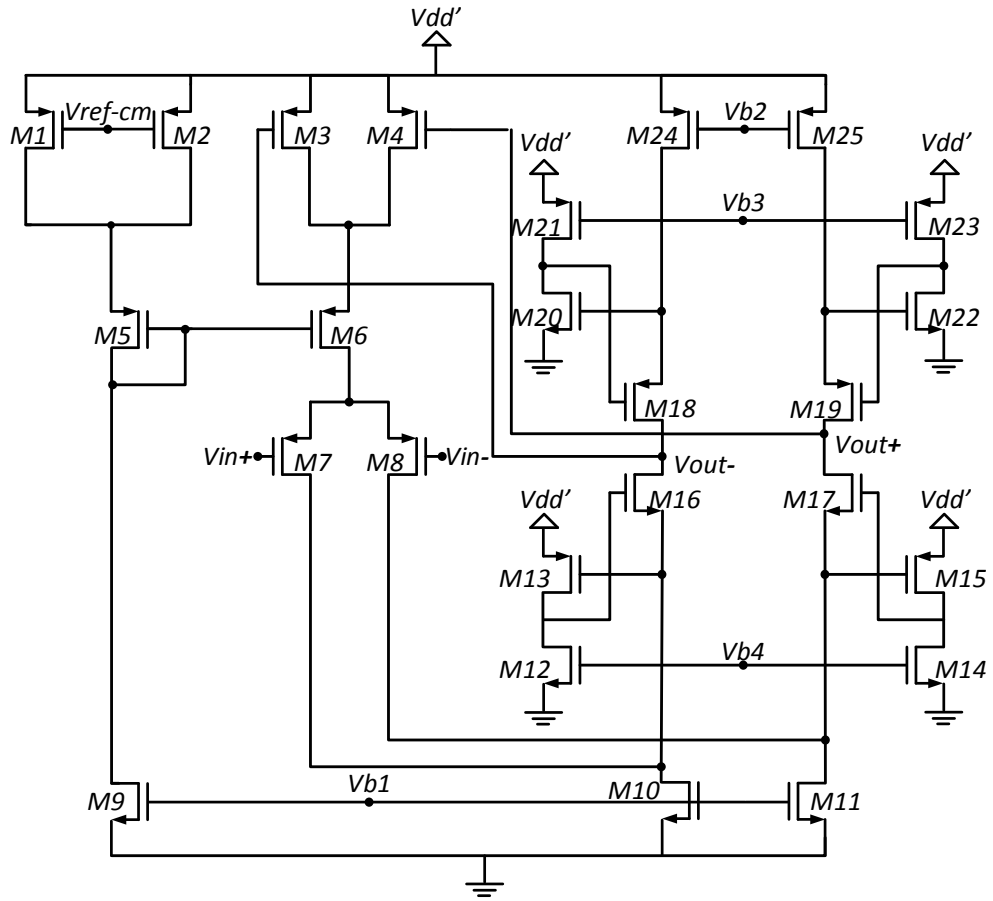


Figure 2.7: Op-amp structure of the LPF (U_1 in Fig. 2.6, $Vdd' = 1\ V$).

mixers cannot be shared.

Transcoductance (Gm-Cell in Fig. 2.6) is a simple g_m stage with active load (M7 and M8) which uses a simple linearity improvement technique called derivative superposition [43]; In this method, the third derivative of transcoductance of one transistor (G3) cancels G3 of another transistor. To realize this approach, one transistor is in saturation region (M1) with negative G3 and the other transistor (M2) is in deep-triode with positive G3. A triode FET (M2) and a stacked FET (M5) are inserted in parallel with M1 as shown in Fig. 2.6. The reason of using stacked FETs (M5 and M6) is driving gate and drain of M2 and M3 with opposite polarities and hence increasing their G3 (large variation rate of M2

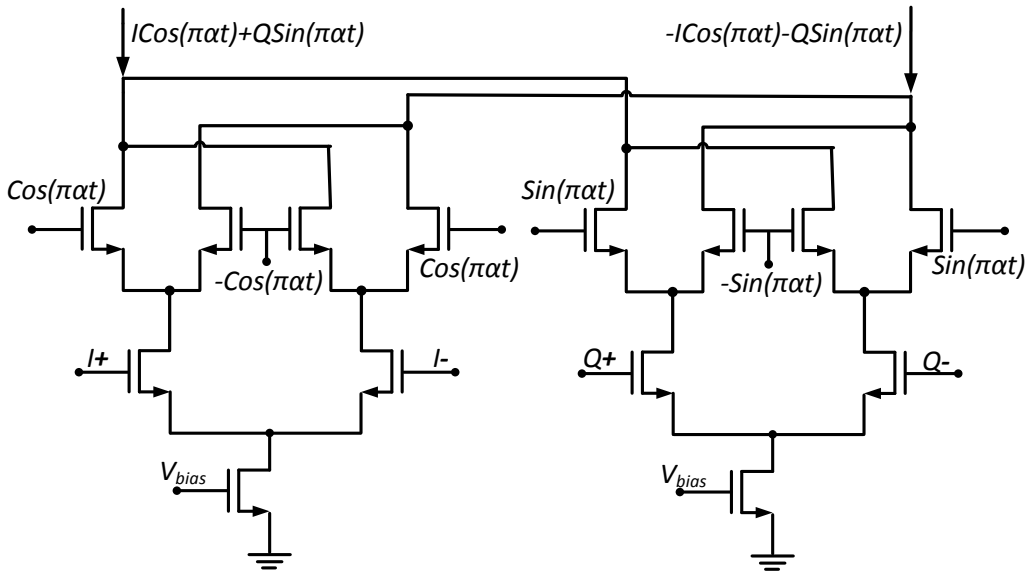


Figure 2.8: Adding currents of two active Gilbert cell mixers to make expression "A" in (2.7).

and M3 drain current in deep-triode region). So there is no need to increase M2 and M3 size to have sufficient G3 to cancel G3 of M1 and M4. Using this method the linearity improves by around 6dB compared to the conventional Gm (without M2, M3, M5, and M6) while other specs did not change much because M2 works in triode region.

Using large size MOS switch-pair (Switch-Pair in Fig. 2.6) provides better linearity performance, but with more switch parasitic capacitance which results in more noise [42]. By biasing switch transistors slightly into the OFF region, lower noise and higher IM_2 performance will be achieved. NMOS transistors are selected here for their better transmission performance.

The TIA converts the down-converted current into voltage. Normally a TIA is composed of an op-amp with a resistor in negative feedback configuration. Here resistors between switch-pairs and op-amps (R1 and R2) are also added. Using this approach, TIAs also work as voltage adders/subtracters at the same time as shown in Fig. 2.6. An op-amp

in the TIA at the output of the switch-pair in a conventional current-driven passive mixer provides low impedance node at the switch-pair output [42]. Inserting the excess resistors (R1 and R2) after the switch-pairs increases the output impedance of switch-pair, reducing the effective Gm, so this resistor should be small compared to output resistance of Gm itself. Here the main role of op-amp is for addition/subtraction. TIA_5 also works as a lossy integrator with the capacitor C added in the feedback. The op-amp employed for each TIA (U_2 in Fig. 2.6) is shown in Fig. 2.9 and is a feedforward structure which can achieve high unity GBW [44]. Because BW is not critical here the gain is increased to achieve better linearity from op-amp. Another advantage of this structure is having a left half s-plane zero which improves the PM of the op-amp which is critical here due to severe parasitic capacitances of the succeeding blocks. This structure has drawback of high power consumption and is not suitable for input LPFs. Note that U_1, used for input LPF, cannot be used here because there is no decoupling caps here to separate the DC bias from previous blocks and U_1 is too sensitive to input effects changing its bias. Although global feedback offers tighter control, which is not needed here, it has compensation and latch-up issues, so U_2 uses local CMFB.

The mixer (Gm-switch-TIA) is simulated in 0.18-μm CMOS IBM technology. It achieves NF of 33 dB to 15 dB, and relatively constant conversion gain (CG) of -1.7 dB for LO power of -30 dBm to -10 dBm, for input frequency changing from 100 kHz to 10 MHz and LO frequency of 1 MHz. Mixer IIP3 changes from 5.5 dBm to 10 dBm for a LO frequency of 1 MHz in a two tone test in which RF1 and RF2 change from 100 kHz to 10 MHz with 100 kHz separation (see Fig. 2.10). It also dissipates 4.8 mA from 1.8 V voltage source. NF is high at this low frequency due to flicker noise but is bearable by the system. U_2 which is used in the mixer has a GBW of 1.35 GHz for a 3 pF load, and PM of 60.3^o. The whole Mixers, and adders/subtracters section (including U_2 op-amps) draws 29.3 mA from a 1.8 V power supply (*Vdd*).

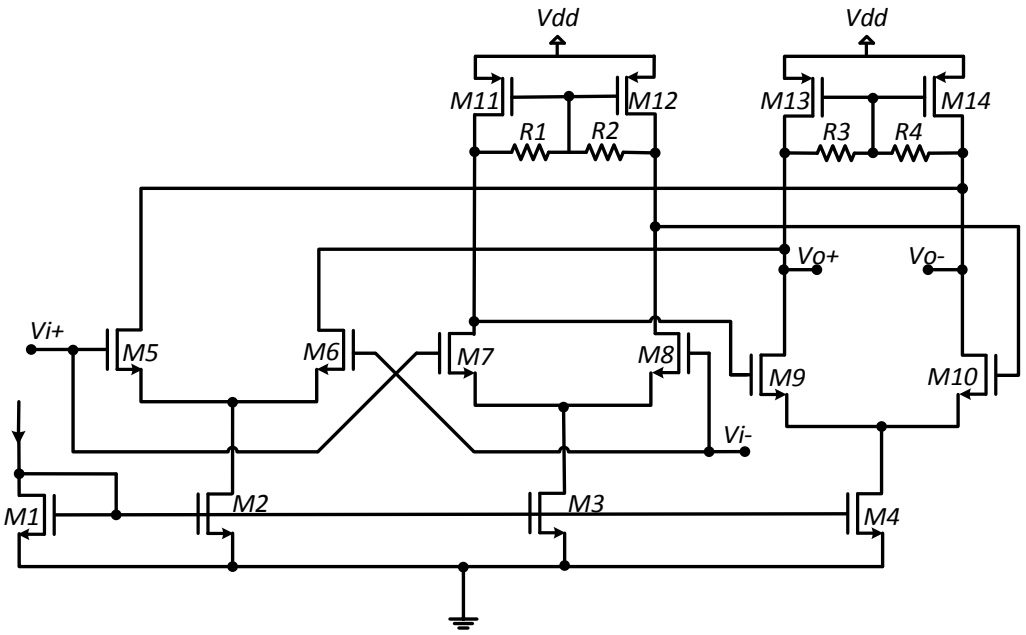


Figure 2.9: Op-amp structure for the TIA of the mixer (U_2 in Fig. 2.6, $Vdd = 1.8\ V$).

2.3 Simulation results

The QCF detector is insensitive to input noise, this means increasing the input noise power has no effects on the output of the detector. The only sources for noise are the components building the detector. This advantage means that any sensitivity can be achievable as long as enough amplification is applied to the input signal by the receiver (LNA and RF mixers).

To see the effect of input noise rejection in simulation, an IQ BB DVB-T signal with a power of -82 dBm is applied to the system, and a white noise source with different noise amplitudes is added to the OFDM signal. The input BB IQ data has extracted from SystemVue software, with the noise added in MATLAB, and the simulations are performed in Cadence for 0.18-μm CMOS IBM technology. Fig. 2.11 shows the simulated input power spectrum and the resulted SCF for signal power of -82 dBm and noise power of -105 dBm, -91 dBm, and -77 dBm. As shown in Fig. 2.11 all inputs (with similar input

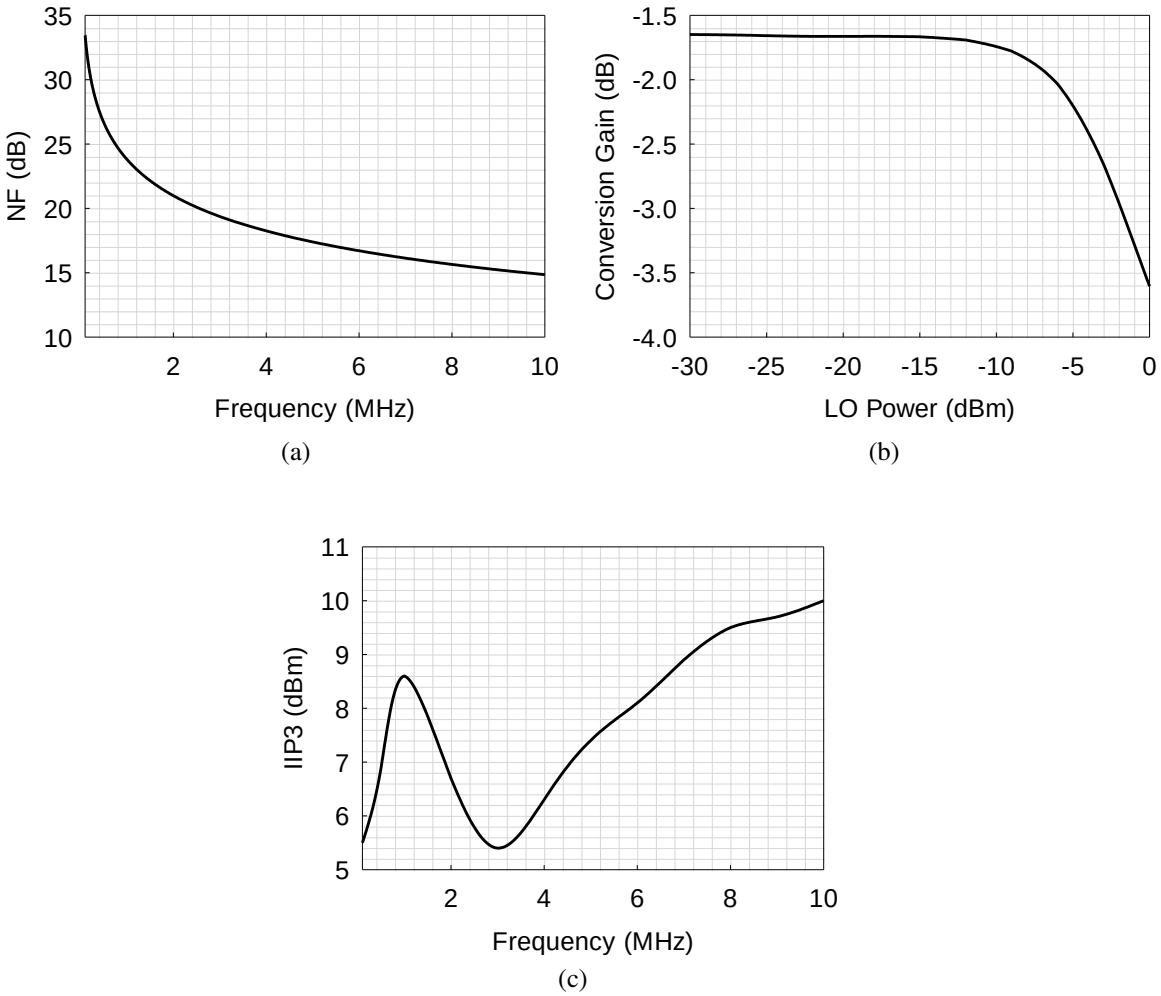


Figure 2.10: Mixer simulation results; (a) NF vs. frequency, (b) CG vs. LO power for LO frequency of 1MHz, (c) IIP3 vs. RF frequency in a two-tone test for a LO frequency of 1MHz.

signal and different noise values) result in similar SCFs and this confirms that the SCF of input noise is zero. So any SNR is achievable as long as input noise level is changing. Increasing the number of samples and simulation time reduces the variations seen in the spectrum.

Fig. 2.12 shows the simulated detected output power (peak of SCF) vs. BB input

power spectrum. As shown in Fig. 2.12 the minimum and the maximum detected input signal powers are -106 dBm and -62 dBm, respectively, which results in a DR of 44 dB. For signals higher than -62 dBm the detector saturates but it still indicates the presence of the signal.

2.4 Fabrication and measurement

The QCF detector is fabricated using 0.18-μm CMOS IBM technology. The fabricated IC microphotograph is shown in Fig. 2.13. The overall area and power consumption are 1.1 mm^2 and 57 mW respectively.

Sensitivity and sensing time are two major features for a spectrum sensor. The QCF spectrum sensor only needs to be tested for its sensitivity because of the fact that it works in frequency domain, so timing issue is addressed properly here. The sensing time for the entire RF band (54-862 MHz) is determined by the total switching times between each two adjacent channel frequencies of the synthesizer used in the down converter of the receiver, and the envelope detector and comparator in the decision circuit, which is too small (less than a micro-second) compared to digital approaches and what is required by the standard (which is in the order of milliseconds).

Testing QCF detector requires generating OFDM-modulated DVB-T signals with different SNRs. In order to generate a DVB-T signal, SystemVue software is used. Level and center frequency of the signal is set by the software. The generated RF data from SystemVue is then downloaded to a signal generator (Agilent E8267D PSG signal generator) which creates noisy RF DVB-T signal and is followed by an off-chip IQ down-converter (QD15A10 SigaTek) to create BB I/Q DVB-T signals with OFDM modulation. Here, the input signal is an 8K mode BB DVB-T signal with 8 MHz channel spacing, CP of 1/8, and 64QAM sub-carrier modulation, so frequency of α can be a non-zero integer factor of 10 kHz within the channel BW ($\alpha = m.10\text{kHz}, m = 1, 2, ...$). α is assumed to be 2 MHz,

suitable for both 2K and 8K modes, and as a result $f_{LO} = \alpha/2$ is 1 MHz. The output spectrum is obtained by a spectrum analyzer (SA) (Agilent E4446A PSA SA). Fig. 2.14 shows the measurement setup for the QCF detector.

The QCF detector checks the availability of the signal in the current down-converted channel by the IQ down-converter, so in a real scenario with considering all channels in the entire CR band (54-862 MHz), the position of the channel in the band is determined by the synthesizer of the down-converter (the channel center frequency is the same as the current LO frequency of the down-converter).

The option of changing noise level is not available in measurement when the RF signal is directly downloaded to the signal generator from SystemVue. As a result, to evaluate the input noise insensitivity of the QCF detector, some BB I/Q input data saved from SystemVue, same as the ones used previously for simulation, with signal power of -82 dBm and different noise values (-105 dBm, -91 dBm, and -77 dBm), are sent to an arbitrary wave generator (AWG) (Agilent N8241A) using MATLAB to create BB I/Q noisy DVB-T signals, which all result in similar SCFs (see Fig. 2.15).

Note that the AWG amplifies the input signal based on its resolution, so this method cannot be used for measuring the sensitivity. In other words, the AWG has a limited resolution which results in a limited minimum input signal. So to determine the sensitivity, RF data should be directly sent to the signal generator from SystemVue. Since the option of changing noise source is not available, signal level is changed. The noise level at the input spectrum is determined by the signal generator and the down-converter, while the signal level is adjusted by the software. Positive SNR values of the input spectrum can be easily calculated using the SA. To perform this task, the input spectrum is averaged by the SA, therefore the difference between the level of the signal and noise is SNR (see Fig. 2.16). This assumption is correct as long as the signal level is at least 10 times larger than the noise level. When noise level is close to signal level, both signal and noise values

should be considered in the channel BW. In this case the difference shown in Fig. 2.16 is $D = 10\log((S+N)/N)$, indicating the actual SNR is $10\log(10^{D/10}-1)$. To achieve accurate desirable negative SNR values, the signal level is adjusted by the software and the value of D is monitored by the SA for $D = 1$ (SNR=-6 dB). Then, enough number of attenuators are placed after the signal generator to precisely lower the signal level and hence SNR, below -6 dB. Fig. 2.17 shows measured input power spectrum and the resulted SCF for SNR=3 dB (D=5 dB), -15 dB, -24 dB, and -27 dB. Note that negative SNRs (lower than SNR=-6 dB for D=1) do not generate distinguishable input power spectrum so only one (SNR=-15 dB) is shown in Fig. 2.17b. As shown in Fig. 2.17e minimum detected SNR is -24 dB and after this value only noise can be seen.

Fig. 2.18 shows detected output power (peak of SCF) in dBm vs. SNR at the input of the QCF detector in dB. From Fig. 2.18, DR of the spectrum sensor is found to be 39 dB. Note that after SNR of 15 dB the SCF does not change but it still indicates the signal exists. For Fig. 2.12 the input power in simulation can be converted to SNR considering the signal generator and down-converter noise level, which results in minimum and maximum simulated SNR of -26 dB and 18 dB respectively (compared to minimum and maximum measured SNR of -24 dB and 15 dB respectively). Note that simulation is performed before circuit parasitic extraction leading to better results compared to measurement.

In Fig. 2.19 the effect of adjacent channels on detected power is shown; an INR of 25 dB (at the input of the detector) is applied to an adjacent channel (signal level in the adjacent channel is 25 dB higher than noise level) and the SCF is measured. Fig. 2.19 shows that if the input is located at the first adjacent channel, QCF detector detects a signal with the same power as if the signal was in the original channel and that is a false detection. The reason behind this is that the BW of the BB LPF (10 MHz) is greater than the down-converted channel BW (4 MHz). Although even with a lower BW enough rejection cannot be achieved with on-chip solutions. The level of the detected power is

lower for next adjacent channels and there is no false detection if the signal is at the fourth adjacent channel. An input LPF with higher rejection can reduce false alarm probability.

To check how α affects the SCF, it is changed for an SNR of 9 dB and the according SCF is measured as shown in Fig. 2.20 for four different cases (α=0.1, 1, 2, and 3 MHz). Fig. 2.21 shows α variations vs. detected power at frequency of α for SNR of 9 dB, which shows detected power doesn't change much within the channel BW (which is 4 MHz after down-conversion). The variation of detected output power vs. α is due to the mixers and output LPF frequency response variations within the BW.

As said before there is no need for an ADC for decision making, only an amplifier, an envelope detector and a comparator are enough. The amplifier is to amplify the output to a level detectable by the envelope detector. The reference voltage in the comparator should be chosen based on the QCF detector output noise level. If the level of the signal at the output of the envelope detector is more than the level of the noise, then the output of the comparator is a "1", otherwise it is a "0". To evaluate the operation of the detector with decision circuit, a decision circuit including instrumentation amplifier, envelop detector, and comparator along with the detector chip is placed on a PCB board (see Fig. 2.22).

The amplifier is a high-speed instrumentation amplifier which consists of three op-amps [two stages of ADA4817âĂŞ1 and ADA4817âĂŞ2 (Analog Devices)] with a total gain of 46 dB, and also has the role of differential to single-ended converter.

Table 2.2 shows performance summary and comparison of this work with other spectrum sensors. The spectrum sensors in [9, 11] lower the detection BW to increase the sensitivity. [45] uses a dual-mode detection technique (a software based approach after an on-chip receiver), in which two modes are employed; one is ED (coarse detection) with a short sensing time and the other is correlation detection (CD) (fine detection) with a high sensitivity (-104 dBm). The detected SNR for [45] is still positive. To have a fair comparison, minimum detected BB SNR is compared rather than the sensitivity, as the sensitivity

Parameter	This work	[9]	[11]	[17]	[45]
Detection BW (MHz)	8	0.025-0.8	0.2-30	200	6
SNR_{min} (dB)	-24[a]/-15[b]	>0	>0	-5	>0
INR_{max} (dB)	25[c]	-	-	30	-
Sensing Time (ms)	-	-	-	50[d]	0.1[e]/1[f]
Realization[g]	A	A&D	A	D	A[h]
Power Diss (mW)	57	180	30-44	7.4	28
CMOS Tech	0.18 μm	0.18 μm	90 nm	65 nm	65 nm

Table 2.2: Performance Summary and Comparison of the QCF Detector with Recently Reported Spectrum Sensors
[a] Before decision circuit.
[b] After decision circuit.
[c] Within 32 MHz BW.
[d] Is 1 ms for INR of 20 dB.
[e] ED with 1 dB noise error.
[f] CD with 1 dB noise error.
[g] "A" stands for analog and "D" is digital.
[h] Spectrum sensing after down-conversion and BB filters is performed using a software.

depends on the detection BW, SA resolution BW (RBW), and gain of receiver which are not similar in all works. This work achieves the best SNR with analog approach. As can be seen in Table 2.2,[17] uses digital approaches for spectrum sensing, and doesn't consume much power compared to analog approaches. This is because[17] assumes the signal in BB is already in digital domain and does not consider an ADC, which should have a high power dissipation for a BW of 200 MHz. The op-amp U_2 in Fig. 2.6 for the QCF detector has the main contribution to the power consumption. Using op-amps with lower power consumption in the mixers can lead to a major reduction in power consumption.

2.5 Conclusion

An integrated analog spectrum sensor has been described and fabricated in a 0.18-μm CMOS technology, which detects weak signals without increasing sensing time or de-

creasing the detection BW. It uses QCFD technique with analog realization and is designed based on knowing features of the primary DVB-T signals. It doesn't have the complexity and timing penalty of the digital CFD methods (no FFT and no ADC), while preserving their accuracy, reaching SNR of -24 dB for 8 MHz channel BW and DR of 39 dB.

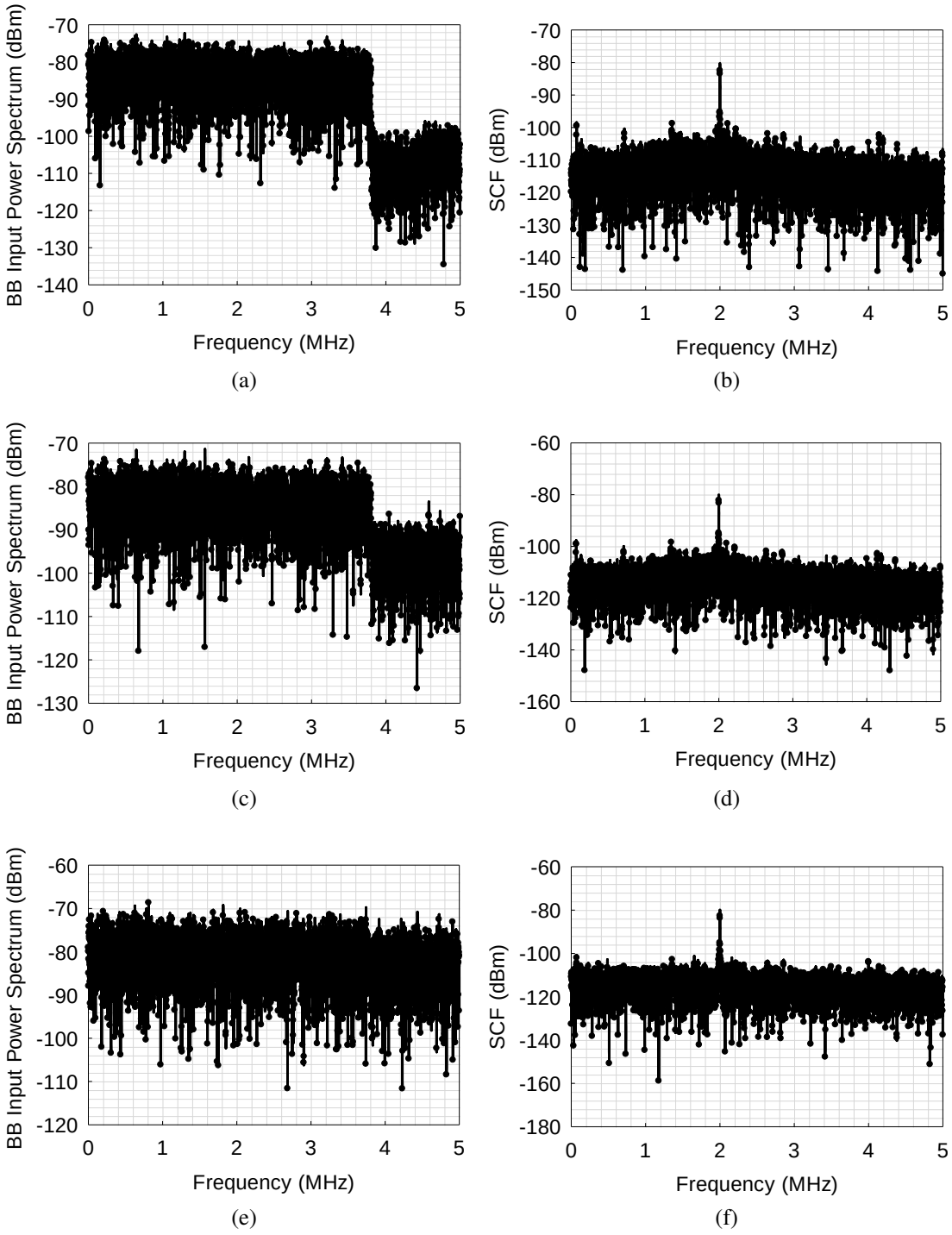


Figure 2.11: Simulated input power spectrum and SCF for signal power of -82 dBm and different noise powers; (a) input power spectrum for noise power of -105 dBm, (b) SCF for noise power of -105 dBm, (c) input power spectrum for noise power of -91 dBm, (d) SCF for noise power of -91 dBm, (e) input power spectrum for noise power of -77 dBm, and (f) SCF for noise power of -77 dBm.

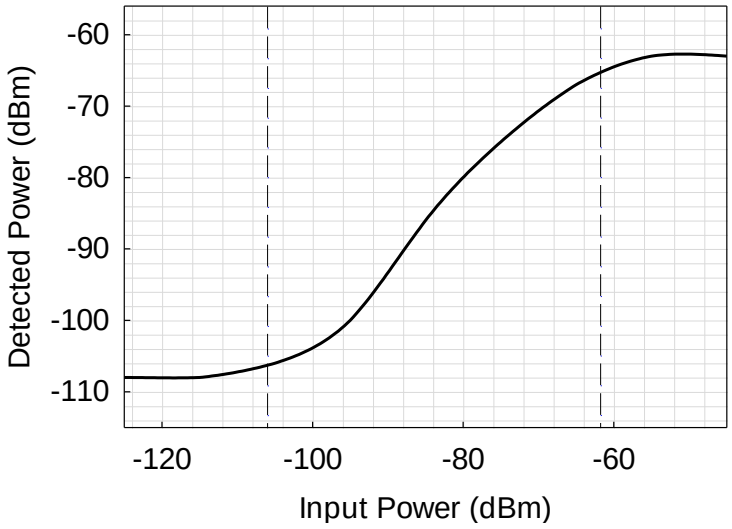


Figure 2.12: Simulated detected output power (peak of SCF) vs. input power.

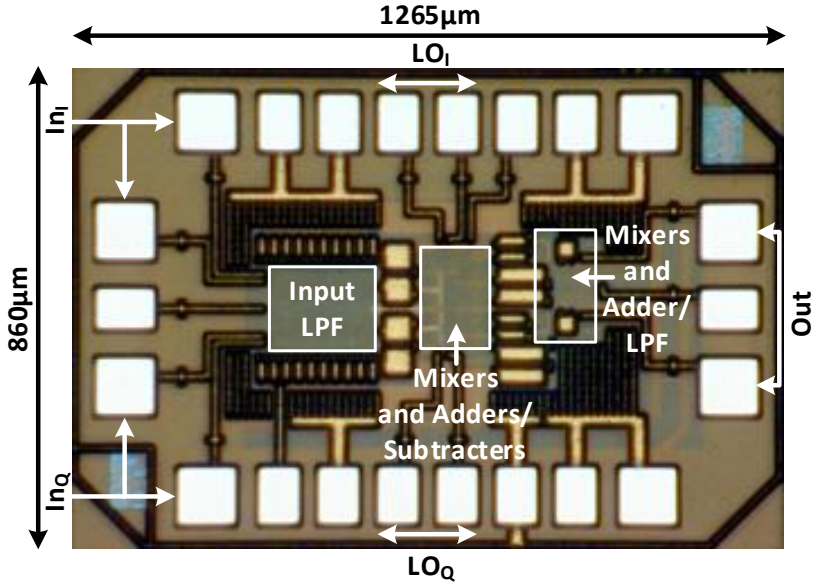


Figure 2.13: Die micrograph of the fabricated QCF detector.

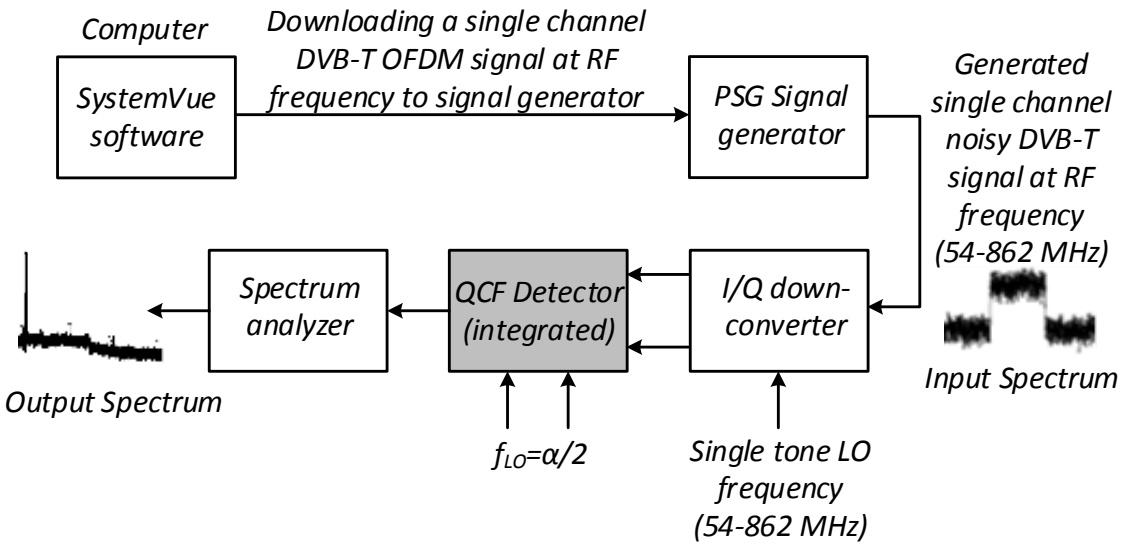


Figure 2.14: Measurement setup for the QCF detector.

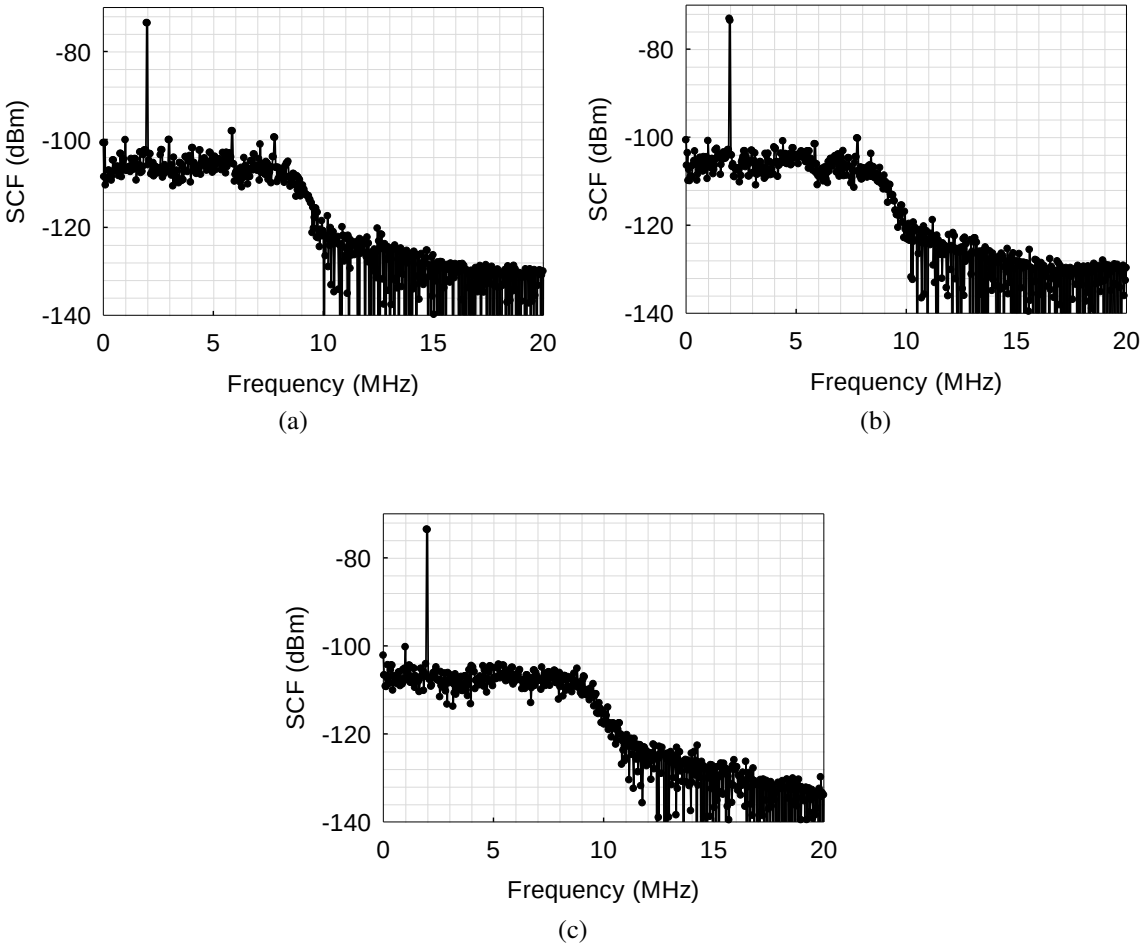


Figure 2.15: SCF for signal power of -82 dBm and noise power of; (a) -105 dBm, (b) -91 dBm, and (c) -77 dBm.

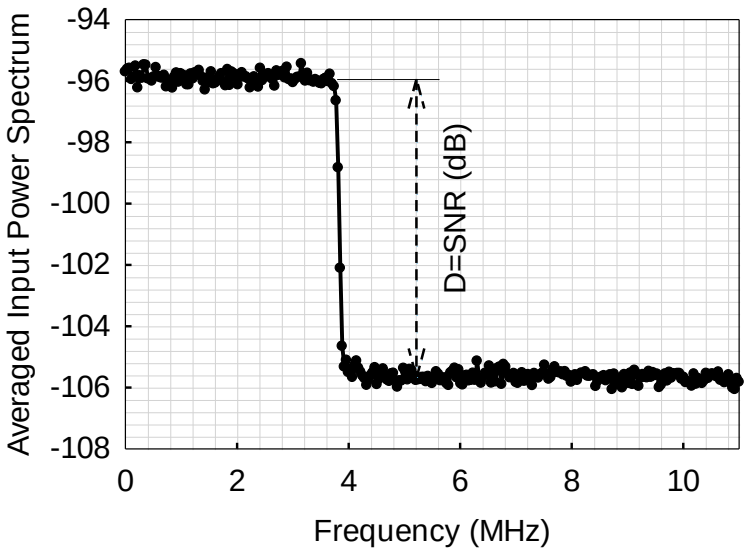


Figure 2.16: SNR calculation through power spectrum.

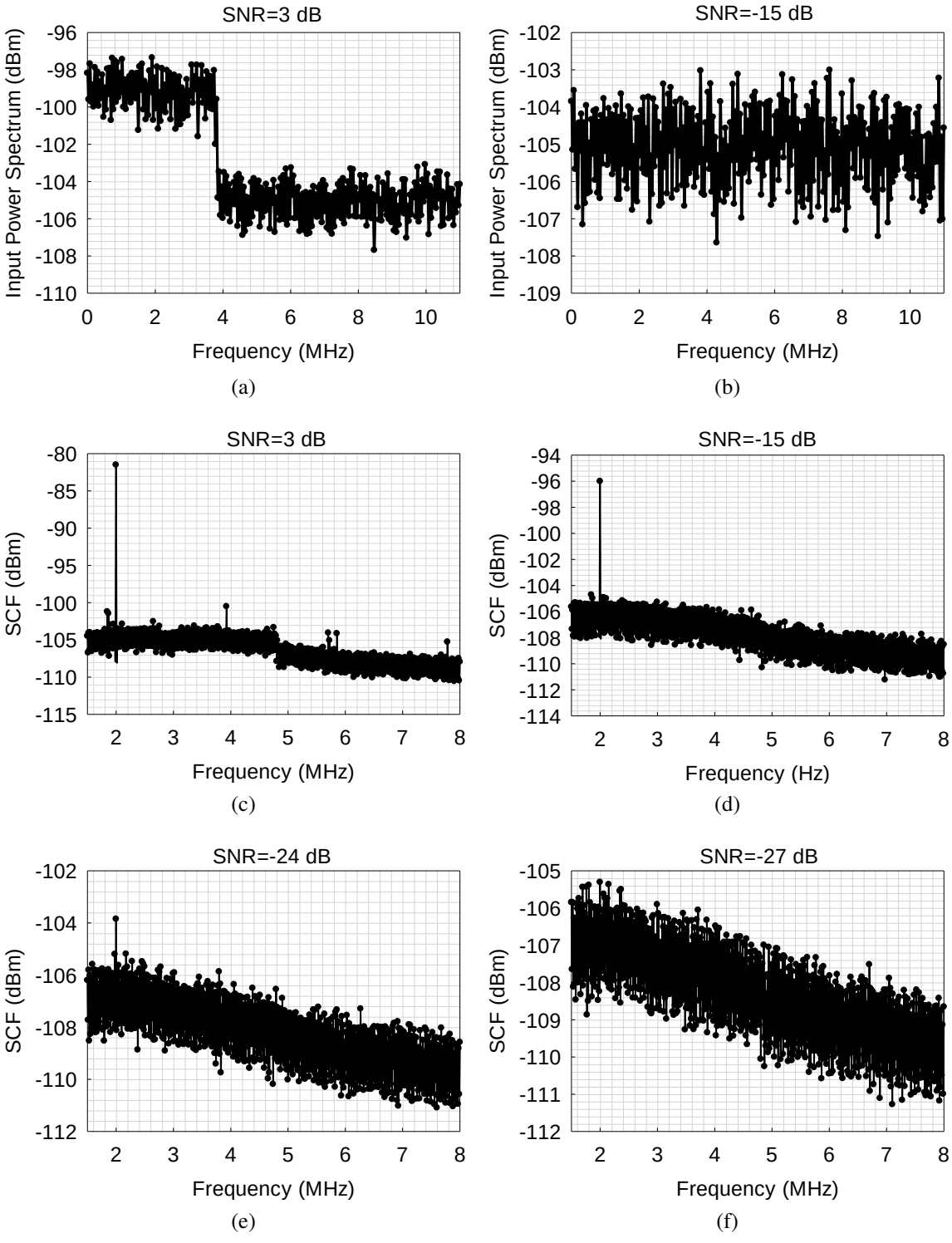


Figure 2.17: Input power spectrum and SCF for different SNRs; (a) Input power spectrum for SNR=3 dB, (b) Input power spectrum for SNR=-15 dB, (c) SCF for SNR=3 dB, (d) SCF for SNR=-15dB, (e) SCF for SNR=-24 dB, and (f) SCF for SNR=-27 dB.

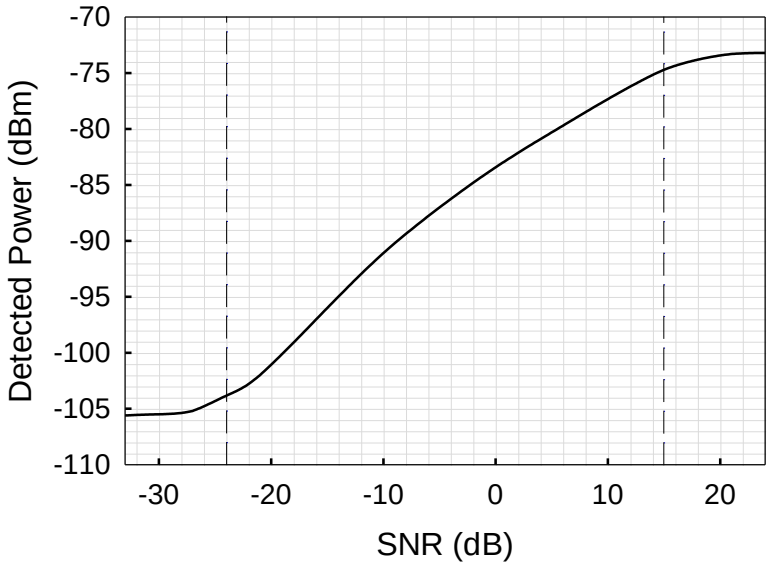


Figure 2.18: Detected output power (peak of SCF) vs. SNR at the input of the QCF detector.

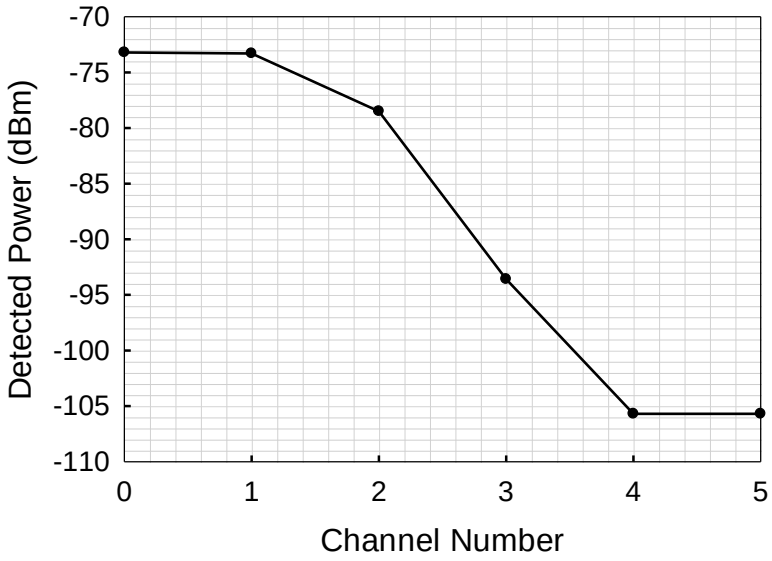


Figure 2.19: Detected power vs. channel number for INR of 25 dB (channel number=0 is the main channel, channel number=1 is the first adjacent channel, and so on).

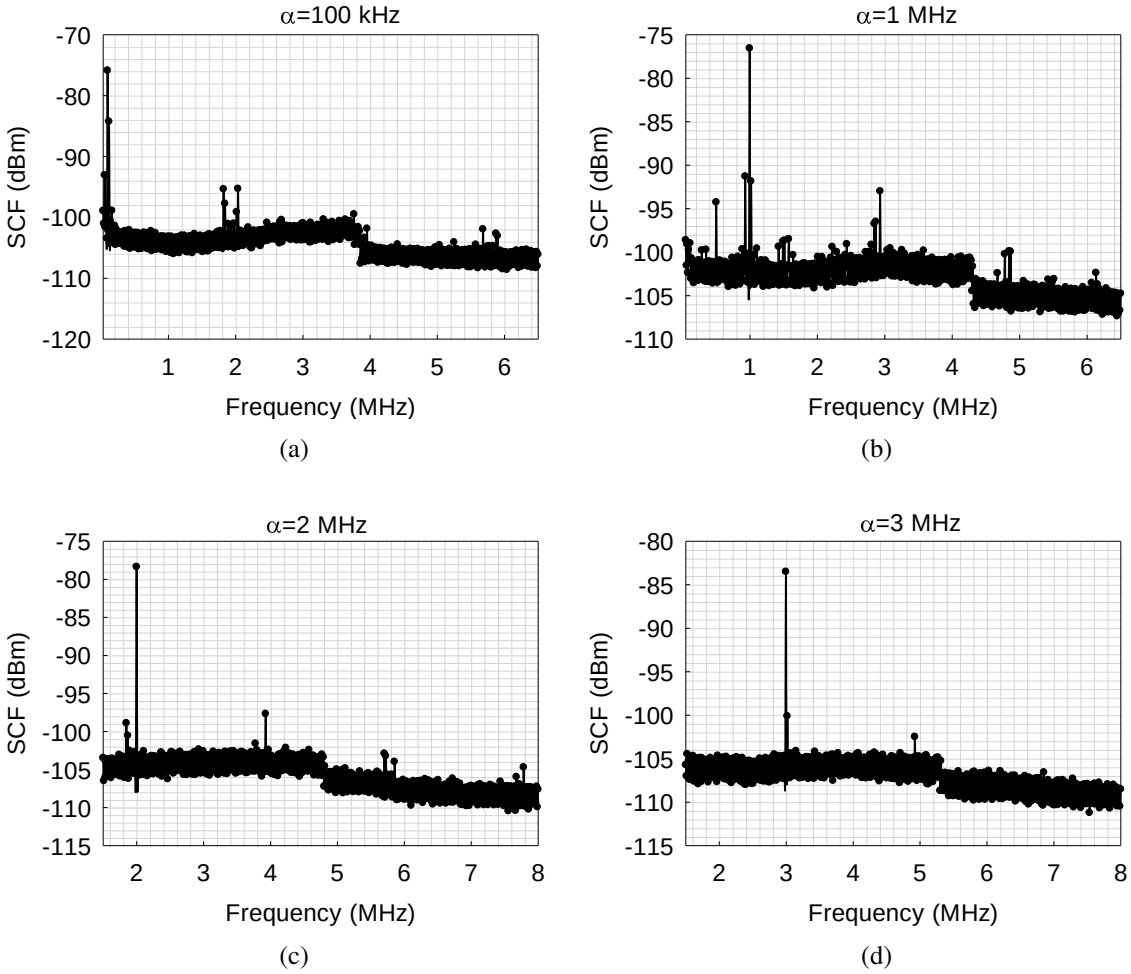


Figure 2.20: SCF for SNR of 9 dB, for different frequencies of α; (a) α=100 kHz (b) α=1 MHz (c) α=2 MHz (d) α=3 MHz.

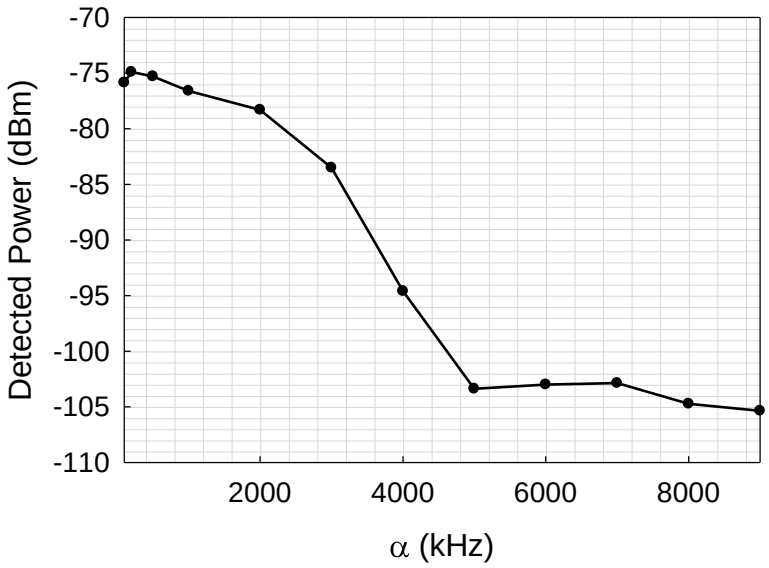


Figure 2.21: Detected power vs. α for SNR of 9 dB.

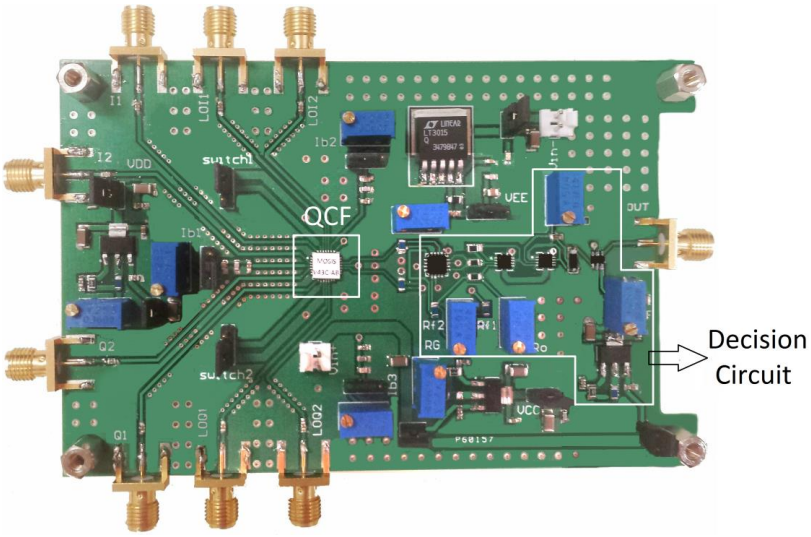


Figure 2.22: PCB showing the QCF detector chip and the decision circuit composing of instrumentation amplifier, envelope detector, and comparator with the reference volatage.

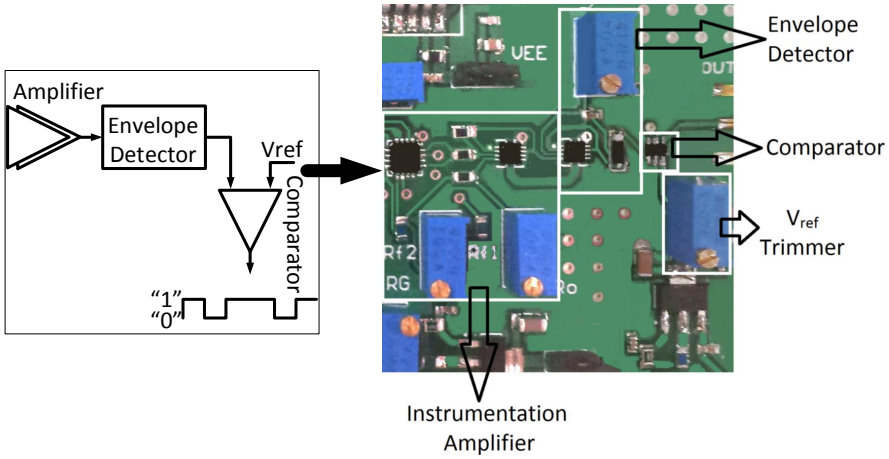


Figure 2.23: Decision circuit and the corresponding parts on PCB.

3. PHASER-BASED REAL-TIME SPECTRUM SENSORS*

The objective is to seek a simple, wideband, fast, and reliable spectrum sensor. Hence, the focus of this chapter is on finding a real-time spectrum sensing method, which has all the mentioned features. Conventional real-time spectrum sensing techniques usually require a wideband fast sweeping synthesizer or a wideband ADC in addition to the spectrum sensing block. Here, another objective is to find a real-time spectrum sensor, which doesn't require these extra circuitry, which is possible using phaser-based techniques.

3.1 Proposed architecture

As mentioned in Section 1.2, conventional phasers are APFs with linear or stepped GD characteristic realized using transmission lines [19], so ideally the incoming time-limited signal is delayed without any attenuation. Since each frequency in the signal is delayed differently, the channels are discriminated in time domain. For a proper discrimination, time-frequency resolution should be greater than the Gaussian pulse duration ($\Delta\tau_i = \tau_{i+1} - \tau_i \geq T$), assuming an ideal stepped GD with no channel spreading, as shown in Fig. 1.3. This is to avoid any overlap between two consecutive channels due to temporal dispersion caused by the phaser.

Using conventional methods, to discriminate different channels in a frequency band, each channel should have a specific GD, different from other channels, and time-frequency resolution should be enough. A CMOS APF can be designed in a way to provide such GD. A general second order APF has the frequency response of:

$$H(s) = \frac{s^2 - \frac{\omega_0}{Q}s + \omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{3.1}$$

*

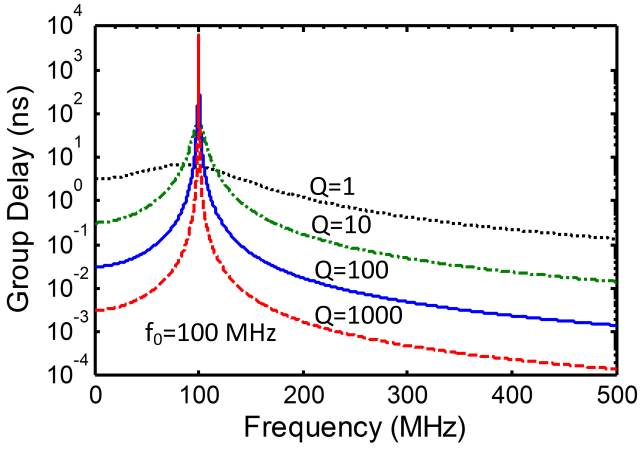
Where ω_0 is the resonance angular frequency, and Q is the quality factor. The GD response can be derived as:

$$\tau(\omega) = 2 \times \frac{\frac{\omega_0^3}{Q} + \frac{\omega_0}{Q}\omega^2}{\omega_0^4 + \omega_0^2(\frac{1}{Q^2} - 2)\omega^2 + \omega^4} \tag{3.2}$$

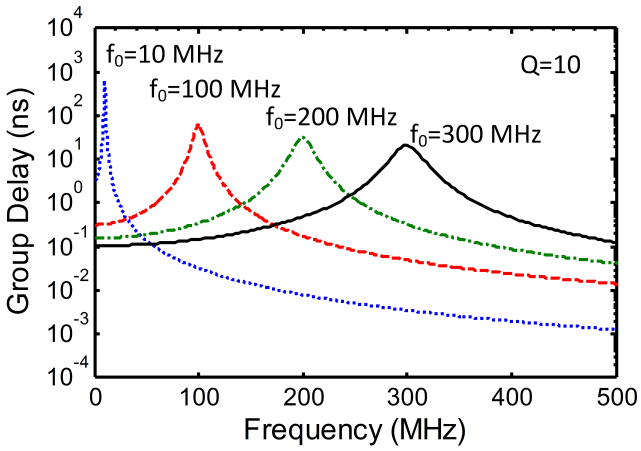
It can be shown from (3.2) that the maximum GD happens at $\omega = \omega_0$ for $Q \gg \frac{1}{\sqrt{2}}$. Fig. 3.1 shows GD for different values of f_0 and Q. To provide a specific GD for each channel, different from other channels, f_0 should be outside the desired frequency band. It means the band of interest should be either below f_0 or above f_0 but not simultaneously at both sides, to avoid similar GDs for two channels which prevents their discrimination in time domain. The closer is the frequency of operation to f_0, the more slope and hence the more resolution is obtained. From Fig. 3.1, decreasing f_0/Q enhances time-frequency resolution ($\Delta\tau$), for a smaller frequency band near f_0, however, it necessitates using a longer Gaussian pulse (higher T), which makes the condition, $\Delta\tau \geq T$, harder to achieve. For instance, consider Fig. 3.2 where $f_0 = 100$ MHz and $Q = 100$, and the purpose is separating two tones located above f_0 with 1 MHz distance (f_1=110 MHz and f_2=111 MHz). From Fig. 3.2, time-frequency resolution, $\Delta\tau$, is around 0.3 ns from frequency of 110 MHz to 111 MHz, which is not enough for separating the two single tones, f_1 and f_2; as mentioned earlier, BW of the Gaussian pulse (Δf_G) plus BW of each channel (Δf_{ch}), which is zero here, should be smaller than the frequency steps of the phaser (f_{step}):

$$\Delta f_G + \Delta f_{ch} \leq f_{step} \tag{3.3}$$

which for this example translates to: $\Delta f_G \leq 1$ MHz. From (1.1), σ should be greater than 112.5 ns, leading to a T of at least 675 ns (assuming T can be approximated as: $T \cong 6\sigma$), so time-frequency resolution condition, $\Delta\tau \geq T$, is not satisfied. Increasing order of filter doesn't sufficiently improve the resolution. Cascading N biquads results in addition of



(a)



(b)

Figure 3.1: GD of a 2^{nd}-order APF for (a) f_0=100 MHz and Q=1, 10, 100, 1000, and (b) Q=10 and f_0=10 MHz, 100 MHz, 200 MHz, 300 MHz.

their phases which multiplies the resolution by N, if the biquads are similar.

One way to deal with this issue is using a loop technique, which is used in conventional phasers [46] to improve time-frequency resolution, and requires a delay block added in the feedback of a system consisted of a DDS unit and an amplifier as shown in Fig. 3.3. This infinite loop enhances the GD slope; the channels are partially discriminated in time domain, in each transition from the delay line. Gradually at a specific time, depending on

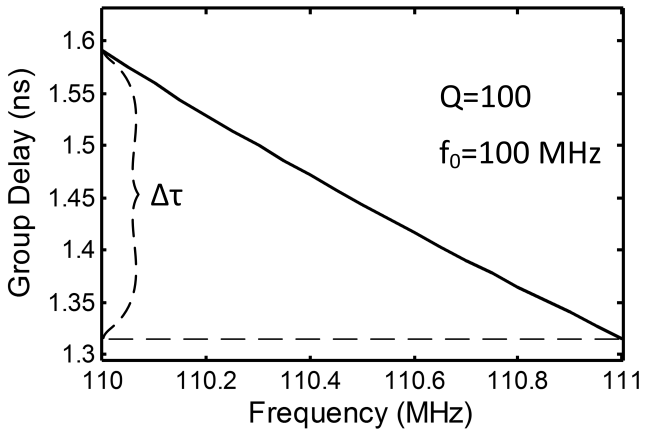


Figure 3.2: GD of a 2^{nd}-order APF for f_0=100 MHz and Q=100 from 110 MHz to 111 MHz.

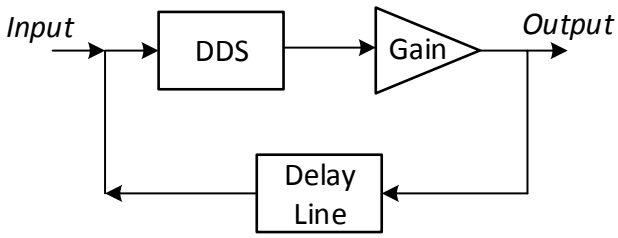


Figure 3.3: Loop technique to increase time-frequency resolution.

the lowest GD slope in the frequency band, all channels get separated. The delay amount of the delay line should be at least $T - GD_{min}$ (neglecting time spreading in each channel and assuming an ideal stepped GD characteristic for the DDS), to avoid any overlap, which T is the Gaussian pulse duration, and GD_{min} is the minimum GD of the DDS unit.

One way to realize an on-chip delay line is employing a linear-phase APF, however, considering the required delay, this method is not feasible. As an instance, consider the previous example for separating two signals located at $f_1 = 110$ MHz and $f_2 = 111$ MHz. For T=676 ns, the delay line should have a delay of at least: $676 - 1.3 = 674.7$ ns (see Fig. 3.2) to separate only two signals located at f_1 and f_2 neglecting spreading of

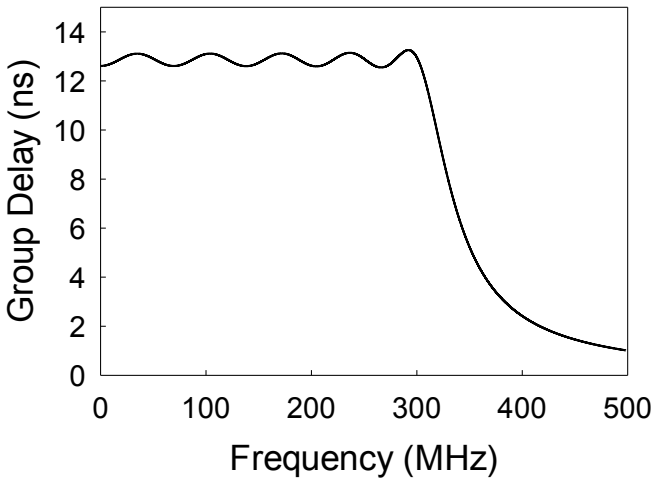


Figure 3.4: GD response of a 10^{th} order equiripple all-pass delay filter with 0.5^0 phase error and f_C of 100 MHz.

the original time-limited input. It can be shown that a 10^{th} order equiripple all-pass delay filter [47] with 0.5^0 phase error and f_C of 100 MHz has a delay of only 13 ns (see Fig. 3.4), which f_C is the -3 dB cut-off frequency of the equivalent LPF frequency response. This delay is still not sufficient for discriminating the two signals. Note that for this equiripple all-pass delay filter, a lower f_C (50 MHz) can still produce a constant GD (25 ns) at $f_1 = 110$ MHz and $f_2 = 111$ MHz which is still not sufficient. Also using a linear GD DDS for separating channels results in a significant temporal dispersion, requiring higher values for the delay line. So there is no integrated solution for the delay block.

A filter with a narrow BP shape GD as in Fig. 3.1 can separate a single channel located at f_0 if the GD is sufficient. A second order BPF has a GD of half of a second order APF. If the purpose is separating only one channel, BPF is superior to APF as both magnitude and GD have BP shapes; BP GD participates in channel discrimination, while BP magnitude rejects undesired channels. As mentioned earlier, the loop technique adds a desirable delay using a delay block to enhance time-frequency resolution. Knowing this fact along with the mentioned feature of a BPF, an alternative solution to add the desirable delay for

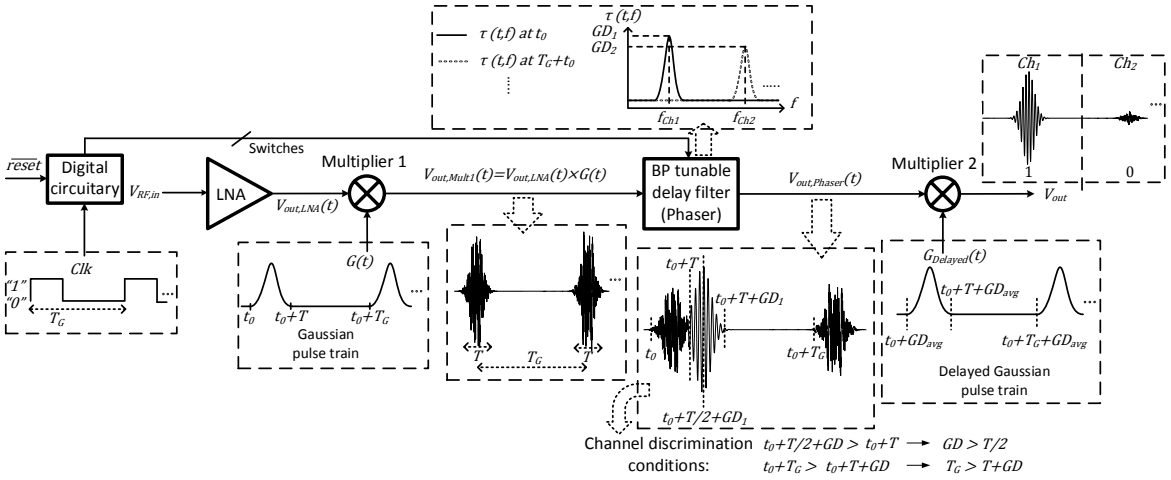


Figure 3.5: Proposed phaser-based integrated spectrum sensor.

enhancing time-frequency resolution is proposed.

Fig. 3.5 shows the proposed real-time integrated spectrum sensor architecture. In this architecture, a periodic Gaussian pulse, rather than a single one, is applied to the multiplier providing a time-limited periodic signal, $V_{out,Mult1}(t)$.

$$V_{out,Mult1}(t) = \sum_{n=0}^{\infty} V_{out,LNA}(t) \times G(t - t_0 - \frac{T}{2} - nT_G) \tag{3.4}$$

where $V_{out,LNA}(t)$ is the incoming signal after LNA, $G(t)$ is a Gaussian pulse with a duration of T, which is repeated with a period of T_G and has the following form in time and frequency domain:

$$G(t) = \frac{A_G}{\sigma\sqrt{2\pi}} e^{\frac{-t^2}{2\sigma^2}} \overset{F}{\longleftrightarrow} A_G e^{\frac{-\omega^2\sigma^2}{2}} \tag{3.5}$$

where A_G is the amplitude of the Gaussian pulse in frequency domain. The resulting periodic time-limited signal is then applied to a phaser, which is a tunable BPF with BP GD. The center frequency of this phaser is set to the center frequency of each channel periodically with the period of T_G, creating a separated channel in each period. T_G should

be chosen according to the required time-frequency resolution. Assuming that T_G is long enough and $V_{out,LNA}(t)$ is composed of N single tones with a frequency separation of $\Delta\omega$, each with an amplitude of A_k, output of the phaser in frequency domain ($V_P(\omega) = F(V_{out,Phaser}(t))$ in Fig. 3.5), when the center frequency of the BPF is set to ω_0, is as follows:

$$V_P(\omega) = \sum_{k=0}^{N-1} A_k A_G e^{-\frac{(\omega-\omega_0-k\Delta\omega)^2\sigma^2}{2}} e^{-j(t_0+\frac{T}{2})(\omega-\omega_0-k\Delta\omega)} H(\omega) \tag{3.6}$$

where $H(\omega)$ is the transfer function of the phaser when the center is set to ω_0 and for n BPF biquads (phaser) has the following polar form:

$$\begin{aligned} &H(\omega) = |H(\omega)|e^{j\Phi(\omega)}, \\ &\Phi(\omega) = n\frac{\pi}{2} - n\tan^{-1}(\frac{2Q\omega}{\omega_0} \pm \sqrt{4Q^2-1}) \end{aligned} \tag{3.7}$$

In the vicinity of ω_0, phase of $|H(\omega)|$, $\Phi(\omega)$, can be approximated as:

$$\Phi(\omega) = n\frac{\pi}{2} - n\tan^{-1}(2Q \pm \sqrt{4Q^2-1}) - \frac{2nQ}{\omega_0}(\omega-\omega_0) \tag{3.8}$$

By placing (3.8) in (3.6), $V_P(\omega)$ can be approximated as:

$$\begin{aligned} &V_P(\omega) = \\ &|H(\omega)|A_0 A_G e^{-\frac{(\omega-\omega_0)^2\sigma^2}{2}} e^{-j\left((t_0+\frac{T}{2}+\frac{2nQ}{\omega_0})(\omega-\omega_0)+\Phi_0\right)} + \\ &\sum_{k=1}^{N-1} |H(\omega)|A_k A_G e^{-\frac{(\omega-\omega_0-k\Delta\omega)^2\sigma^2}{2}} e^{-j\left((t_0+\frac{T}{2})(\omega-\omega_0-k\Delta\omega)+\Phi_k\right)} \end{aligned} \tag{3.9}$$

where Φ_k, $k = 0, 1, ..., N-1$ is:

$$\Phi_k = -n\frac{\pi}{2} + n\tan^{-1}\left(\frac{2Q(\omega_0 + k\Delta\omega)}{\omega_0} \pm \sqrt{4Q^2 - 1}\right) \tag{3.10}$$

Equation (3.9) indicates that when the center frequency of the BPF is set to ω_0, in a time duration of T_G, the phaser will shift the main signal at ω_0 in time domain with a value of $2nQ/\omega_0$, while attenuating other channels without creating any delay in them. Note that the assumption of having single tones in each channel for the incoming signal is for simplicity. The above conclusion still holds for wideband channels; however, the effective BW of the signal at input of the phaser for each channel is the BW of that channel ($\Delta\omega_{ch}$) plus BW of the Gaussian pulse ($\Delta\omega_G = 1/(\sqrt{2}\sigma)$), rather than the $\Delta\omega_G$ alone in the case of single tones. The frequency condition of (3.3) for the proposed phaser is a bit more relaxed considering the reduction in the effective BW of each channel after passing through the phaser, due to its BP shape. Considering the effect of T_G on (3.9), Gaussian shape signal at the frequency of ω_0 will be replaced by several impulses sampling it with a frequency of $1/T_G$.

This method is practical using on-chip solutions and can discriminate a wideband input signal in time-domain, since the filter can be designed to have a sufficient GD in one single channel at a time, and T_G can be chosen as long as required. Channel spreading has minimum effect on this design with a long enough T_G. The output of the filter should be multiplied by a delayed version of the Gaussian pulse train with the delay of average GDs of all channels (for simplicity), to avoid undesirable channels in each period of T_G. This delayed Gaussian pulse train selects only the delayed part of the output signal in each period (the desired channel), which is delayed by the GD response of the phaser, and rejects the part that is not delayed and is attenuated by the BP frequency response of the phaser (rest of the channels in the frequency band). To have a channel discrimination in

a frequency band consisting of N channels, N pulses in the Gaussian pulse train and N states for the filter are required, so the tuning process in the entire band takes $N \times T_G$.

The architecture in Fig. 3.5 functions properly provided that:

$$T_G > T + GD_{Max} \tag{3.11}$$

$$GD_{min} \geq \frac{T}{2} \tag{3.12}$$

Equation (3.11) is required to avoid any overlap between two states, while (3.12) is required to separate each channel in its own state (as shown in Fig. 3.5). These conditions are replacements for time-frequency resolution condition in conventional phasers [18]. While (3.11) is easy to achieve due to the term T_G, (3.12) puts some constraints on the achievable frequency resolution. From (3.11) and (3.12) and assuming $T \approx 6\sigma$, $\Delta\omega_G = 1/(\sqrt{2}\sigma)$, and $\Delta GD = GD_{Max} - GD_{min}$, the following conditions can be obtained:

$$T_G > GD_{min} + \Delta GD + \frac{6}{\sqrt{2}(\Delta\omega_G)} \tag{3.13}$$

$$GD_{min} > \frac{3}{\sqrt{2}(\Delta\omega_G)} \tag{3.14}$$

Equations (3.3) and (3.13) indicate that a lower sensing time (lower T_G) requires a lower GD with lower variation (lower GD_{min} and ΔGD) and a lower frequency resolution (higher $\Delta\omega_{step}$). Also (3.3) and (3.14) indicate that a lower frequency resolution relaxes the condition on minimum GD.

High GD variation also increases the chance of missed detection. To better understand this, consider two extreme scenarios when GD_{avg} is much smaller than GD_{Max} and much higher than GD_{min} (Fig. 3.6), which creates no overlap between the separated channel (desired channel) and the delayed Gaussian pulse train, leading to missed detection. So

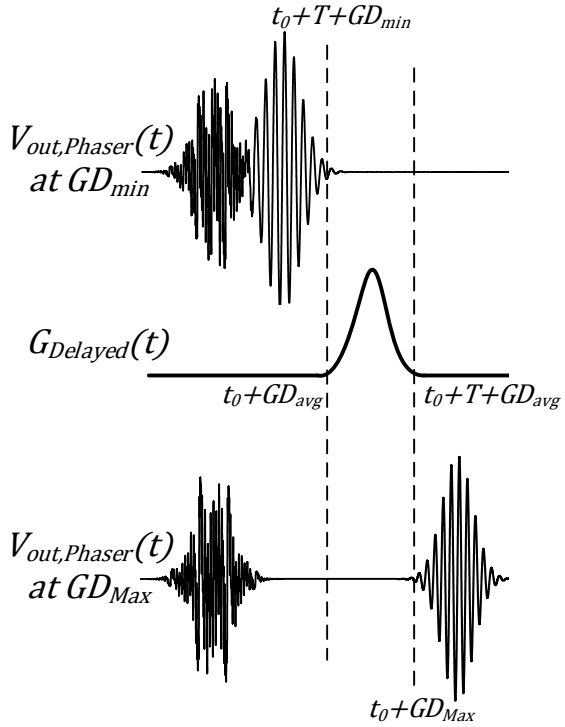


Figure 3.6: Variation of GD leading to missed detection.

the following conditions apply to the phaser GD variation:

$$GD_{min} > GD_{avg} - T,\ GD_{Max} < GD_{avg} + T \tag{3.15}$$

From (3.15) and assuming $T \approx 6\sigma$ and $\Delta\omega_G = 1/(\sqrt{2}\sigma)$, following condition is concluded for GD variation:

$$\frac{\Delta GD}{GD_{avg}} < \frac{12}{\sqrt{2}(\Delta\omega_G)(GD_{avg})} \tag{3.16}$$

Equation (3.16) indicates that with a wider BW Gaussian pulse (lower frequency resolution), the condition on GD variation is stricter, meaning GD variation should be smaller.

The conditions stated in (3.13), (3.14), and (3.16) are plotted in Fig. 3.7, with valid areas specified by small arrows. Fig. 3.7a indicates that for a Δf_G of 16 MHz, a min-

imum GD of at least 21.1 ns is required. Assuming a GD_{min} of 50 ns, Fig. 3.7b plots T_G vs. Gaussian pulse BW, for different values of ΔGD. As suggested by Fig. 3.7b, for phasers with low Δf_G and hence high frequency resolution, sensing time changes rapidly with frequency resolution variation, while sensing time of lower resolution phasers tend to change more with GD variations. For a Δf_G of 16 MHz and GD_{min} of 50 ns, T_G should be higher than 92.2-302.2 ns for a GD variation of 0-210 ns, which assuming an average GD of 70 ns, this GD variation is within 0-300$\%$. Fig. 3.7c, illustrates the valid areas for GD variation vs. Gaussian pulse BW for different values of GD_{avg}. It shows that for a 16 MHz Gaussian pulse BW and an average GD of 70 ns, up to 120$\%$ variation in GD is valid to avoid missed detection.

To better understand the functionality of the proposed system consider a scenario shown in Fig. 3.5 in which the spectrum sensor evaluates the occupancy of two consecutive channels ($Ch1$ and $Ch2$). The incoming signal is applied to "Multiplier 1" after passing through the LNA, multiplied by the Gaussian pulse train, $G(t)$, with period of T_G, creating a time-limited periodic signal, $V_{out,Mult1}$. Only two pulses in $G(t)$ are required for evaluating two consecutive channels, so only the first two time-limited signals in $V_{out,Mult1}$ are investigated. From time t_0 to $t_0 + T_G$, the phaser has a BP frequency response at the center frequency of the first channel, f_{Ch1}, with a GD of GD_1. Since $Ch1$ is occupied, the phaser shifts the signal at f_{Ch1} in time-domain with a delay of GD_1, attenuating the signal at other channels without shifting them. $V_{out,Phaser}$ from t_0 to $t_0 + T_G$ has two parts, one from t_0 to $t_0 + T$, consisting of the attenuated signal with no delay, and one from $t_0 + GD_1$ to $t_0 + T + GD_1$, consisting of the delayed, unattenuated signal at f_{Ch1}, which means $Ch1$ is occupied. The same scenario is considered for the second channel; the phaser has a BP frequency response at the center of the second channel, f_{Ch2}, and a GD of GD_2, from $t_0 + T_G$ to $t_0 + 2T_G$. $V_{out,Phaser}$ from $t_0 + T_G$ to $t_0 + 2T_G$ has only one part, consisting of the attenuated signal, from $t_0 + T_G$ to $t_0 + T_G + T$, which means $Ch2$ is unoccupied.

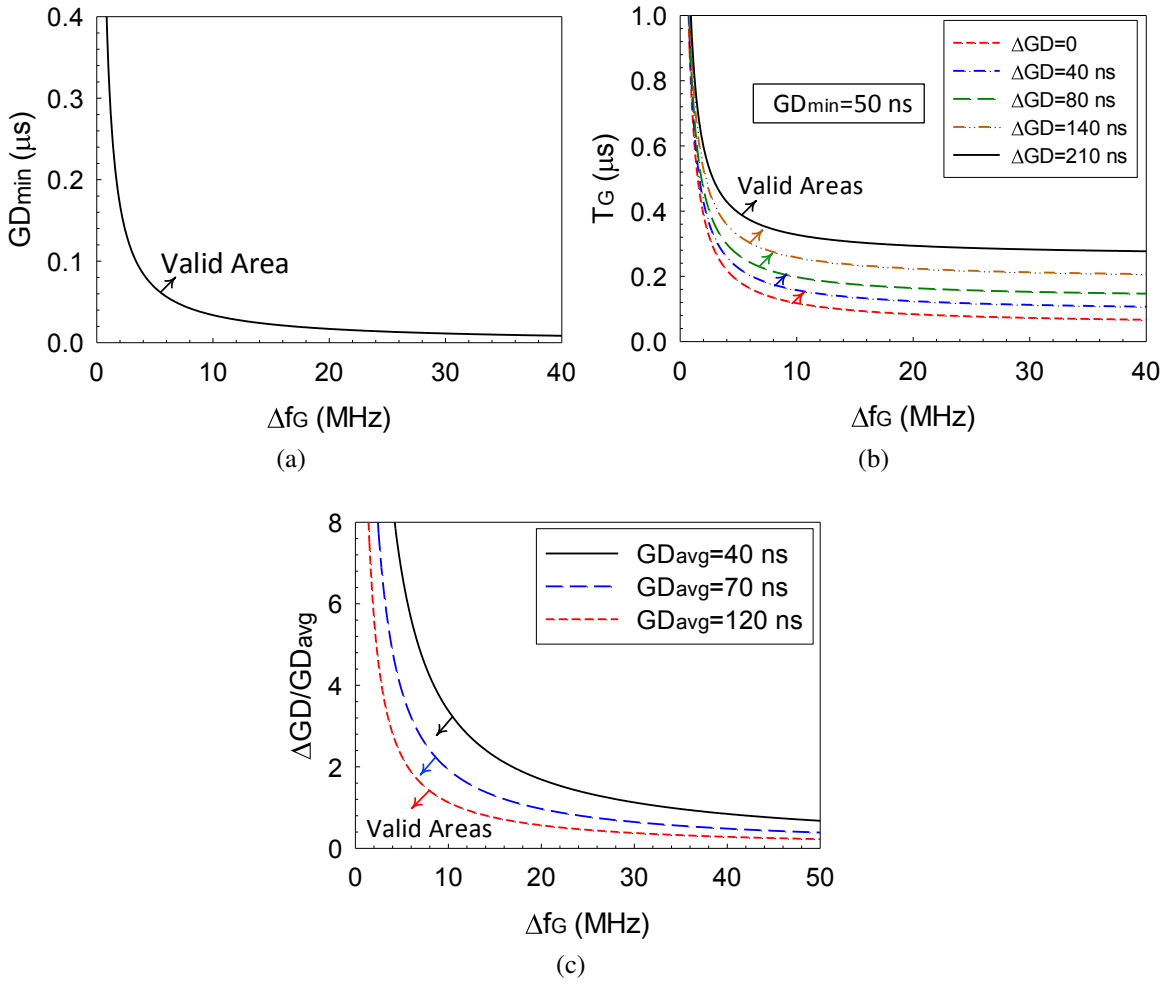


Figure 3.7: Conditions stated in (a) (3.14), (b) (3.13) with different GD variations for GD_{min} of 50 ns, and (c) (3.16) with different GD_{avg}.

Multiplication of $V_{out,Phaser}$ by a delayed Gaussian pulse train, $G_{Delayed}(t)$, with a delay of average GDs of $Ch1$ and $Ch2$, GD_{avg}, further rejects the undesired, attenuated signal. The result can be converted to a "1" and "0" for $Ch1$ and $Ch2$ respectively using an envelope detector and a comparator.

3.2 Circuit implementation

As shown in Fig. 3.5, the proposed structure is composed of an LNA, two multipliers, a tunable BPF, and a digital circuitry. For an RF input signal, LNA is required to lower the noise figure (NF) of the entire system. The first multiplier is for converting the RF signal to a time-limited periodic signal. For better linearity performance, differential structures are employed for the multipliers which necessitates use af a balun to convert the single-ended input signal to a differential one. The tunable BPF plays the role of a phaser and the second multiplier operates as a filter in time-domain which rejects the undesired channels in each period for the proposed real-time spectrum sensor. The following sub-sections further explain each block of the proposed spectrum sensor in transistor-level.

3.2.1 LNA

A balun noise and distortion canceling LNA [48] is employed in the proposed spectrum sensor as shown in Fig. 3.8, which provides a differential signal at its output. It is a CG-CS LNA where CG transistor, $M1$, provides the non-inverting path and CS transistor, $M2$, along with the cascode transistor, $M4$, provide the inverting path for the main signal. The inverted signal at the output of the inverting path is fed back to the gate of $M1$, boosting its transconductance. The resulting differential output is then applied to a multiplier.

Simulation results show that gain of the LNA in Fig. 3.8 is 23 dB, and NF and $IIP3$ change within 2.8-4 dB and 0-5 dBm respectively for the frequency range of 57-354 MHz.

3.2.2 Multipliers

Fig. 3.9 shows the multiplier used in the proposed architecture which achieves simultaneous good noise and linearity performance [49]. In Fig. 3.9, $M1-4$ operate in the linear region, while $M5-8$ operate in the saturation. Size of $M5-8$ should be chosen at least three times of size of $M1-4$ to make $M5-8$ operate as source follower transis-

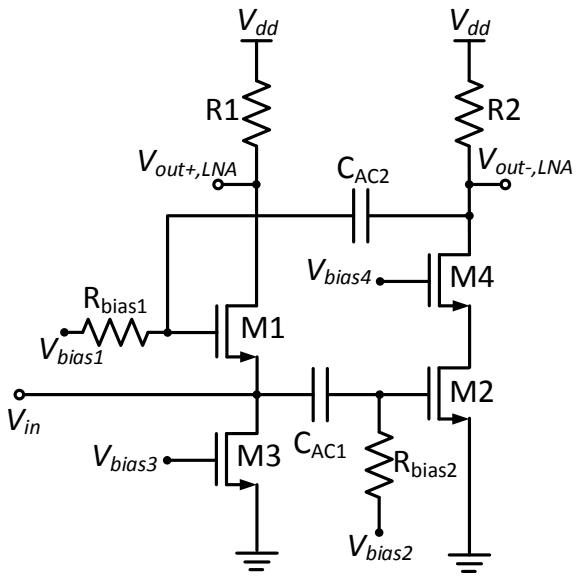


Figure 3.8: Balun-LNA used for lowering NF of the proposed spectrum sensor.

tors, providing a multiplication of the signals applied to the gate of $M1-4$ and $M5-8$ at the output of the multiplier [49]. The output of the balun-LNA is applied to the gates of $M1-4$, while the Gaussian pulse train is applied to the gates of $M5-8$, resulting a Gaussian shape periodic signal at the output of the multiplier (see Fig. 3.5).

Same structure is used for the second multiplier which multiplies the signal at the output of the phaser with a delayed version of the Gaussian pulse train.

3.2.3 Phaser

As mentioned earlier, a tunable BPF operates as a phaser in the proposed architecture. An active operational transconductance amplifier-C (OTA-C) biquad filter is preferred here based on the frequency of operation, 57-354 MHz. The structure shown in Fig. 3.10 [50] is a biquad OTA-C BPF, where ω_0, Q, and GD at the center frequency (GD_0) can be written based on the filter parameters as:

$$\omega_0 = \sqrt{\frac{Gm_1 Gm_2}{C_1 C_2}} \tag{3.17}$$

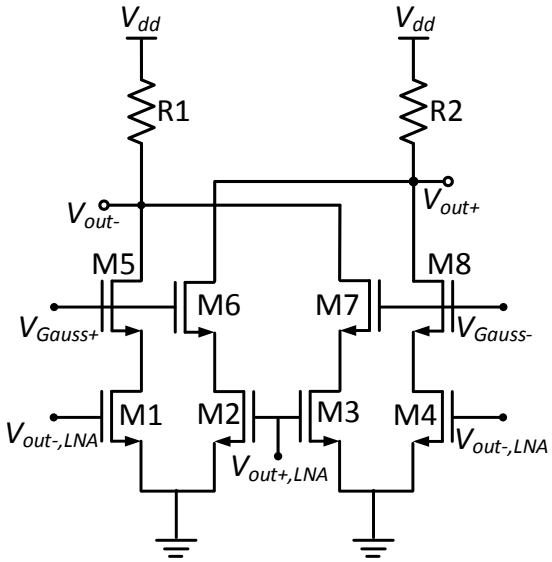


Figure 3.9: Multiplier used for time limiting the incoming signal.

$$Q = \frac{\omega_0 C_2}{Gm_3} \tag{3.18}$$

$$GD_0 = \frac{2C_2}{Gm_3} \tag{3.19}$$

where Gm_1, Gm_2, and Gm_3 are transconductances of OTA_1, OTA_2, and OTA_3 in Fig. 3.10, respectively. Existence of Gm_3 in (3.18) adds a degree of freedom in designing and tuning the filter. DC gain is OTA_4 to OTA_3 transconductance ratio (Gm_4/Gm_3).

Four biquads of Fig. 3.10 are used to create enough GD. All OTA cells have the same structure in the BPF of Fig. 3.10. Both transconductance of OTA cells and capacitors in the OTA-C filter are reconfigurable to provide the required tuning range. For simplicity Gm_1 and Gm_2 are chosen to be equal for all settings. While $Gm_{1,2}$, C_1, and C_2 affect ω_0, Gm_3 and C_2 determine GD_0. To achieve the required ω_0, the value of C_1 is minimized, for each frequency setting, to make the value of C_2 more relaxed to provide high enough GD_0 as C_2 also appears in (3.19). Gm_3 should change in the same direction of C_2 to

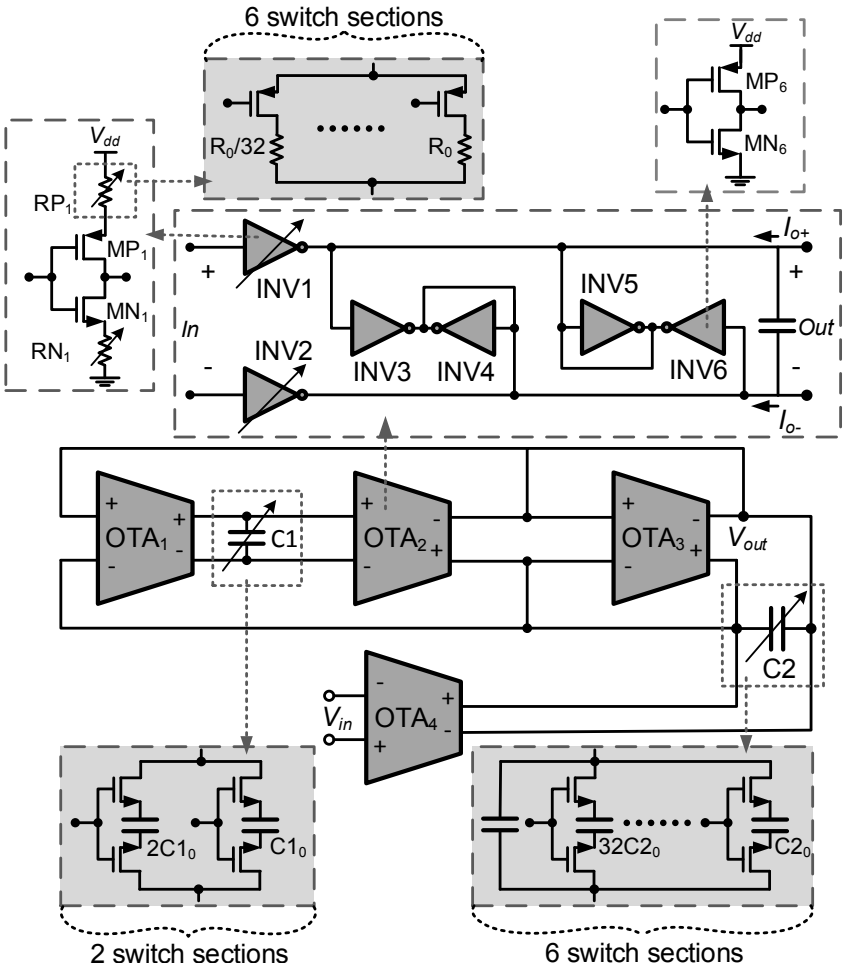


Figure 3.10: Block diagram of the proposed phaser.

compensate GD_0 variation to some degree. Since tuning range of transconductance is inherently smaller than capacitor, GD_0 cannot remain constant within the entire tuning range. Transistor sizing for OTA_4 is chosen three times higher than OTA_3 to maintain a gain of higher than one for each biquad stage. To preserve a nearly constant gain (~ 1.5) in all settings, Gm_4 is designed to track Gm_3 variations. For tuning the filter, first ω_0 is tunned by $Gm_{1,2}$, C_1, and C_2 variation, then GD_0 is tunned by Gm_3 variation. Q variation is determined by ω_0 and GD_0 variations ($Q \propto \omega_0 \times GD_0$). Fig. 3.11 shows the tuning process in a flowchart.

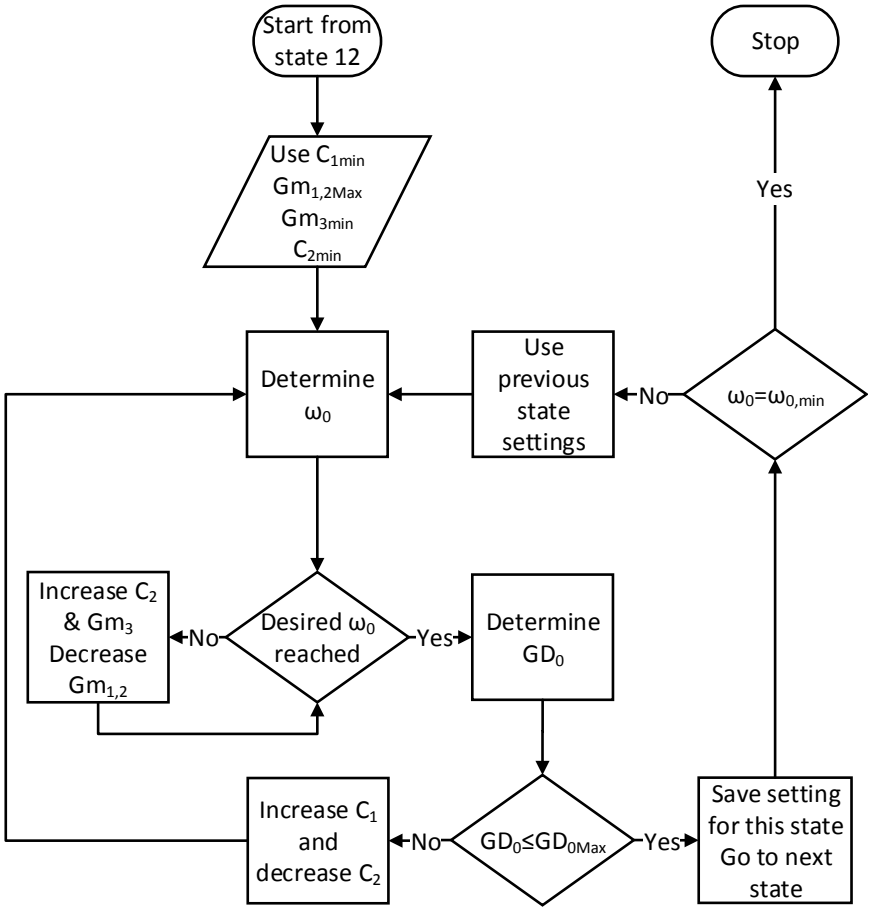


Figure 3.11: Tuning process flowchart (state 12 corresponds to the highest operating frequency).

An inverter-based structure [51] is used for the OTA cells as shown in Fig. 3.10, which has only an input and an output node making it suitable for operation in higher frequencies. $INV3-6$ make a high impedance load for differential gain ($1/(Gm_{INV4,5}-Gm_{INV3,6})$) and a low impedance load for common-mode gain ($1/(Gm_{INV4,5}+Gm_{INV3,6})$). For higher differential gain, transconductance of $INV3$ and $INV6$ are chosen slightly larger than $INV4$ and $INV5$. Transconductance of OTAs are set by changing degenerative resistors in sources of $INV1-2$ using CMOS switches.

A digital circuitry consisting of a counter and a look-up table (LUT) is employed to

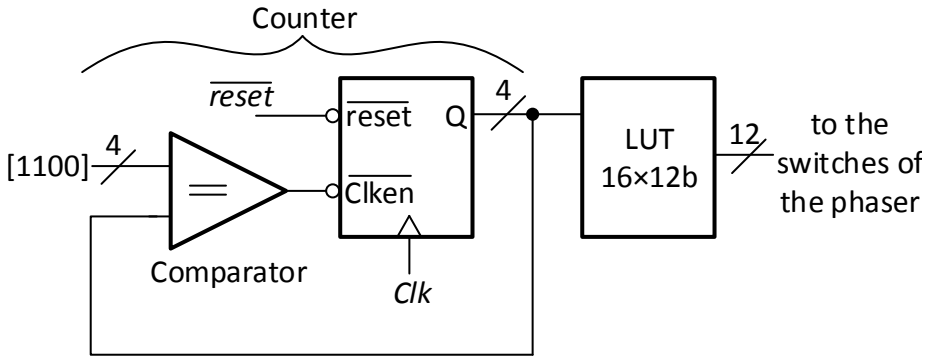
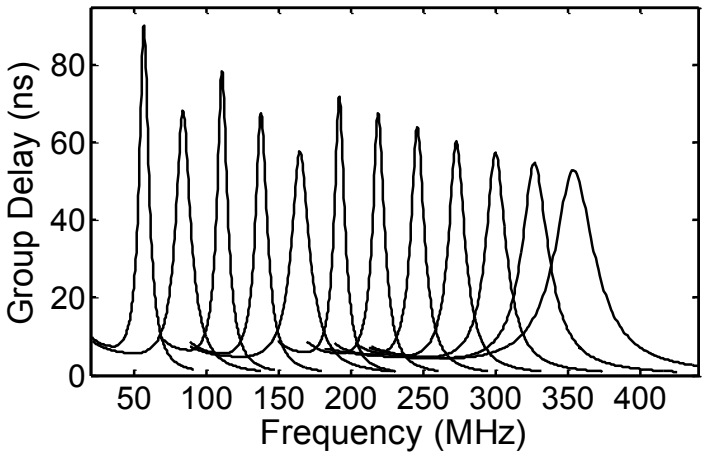


Figure 3.12: Block diagram of the digital circuitry.

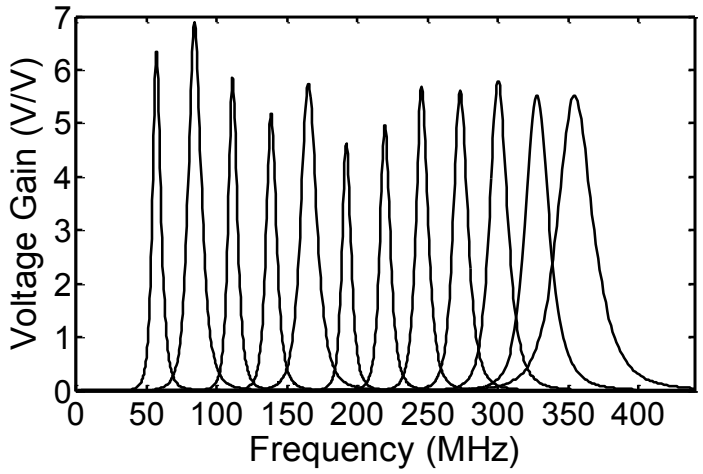
provide all the controlling signals of the phaser (Fig. 3.12). Detection process involves changing the control signals between twelve different states corresponding to twelve channels in the frequency band. State transition is performed periodically using the signal "Clk" with period of T_G, which is the same as the period of the Gaussian pulse train. In each period, phaser selects one specific channel and in twelve periods, phaser discriminates all the twelve channels in the frequency band with frequency resolution of 27 MHz. Here each defined channel is correspond to four channels in a 802.22 standard. The entire detection process can be performed periodically using the signal "$\overline{reset}$" with the period of at least $12 \times T_G$.

Fig. 3.13 shows the simulated magnitude and GD response of the phaser for all states vs. frequency. As illustrated in Fig. 3.13, GD variation is limited to 50-90 ns range, which can satisfy (3.11)-(3.16) if proper T and T_G are chosen.

Fig. 3.14 shows the transient simulation at different points of the proposed detector for a special case, evaluating the signal existence at channel three to five when $Ch3$ and $Ch5$ are occupied, while $Ch4$ is empty. In Fig. 3.14, transition of frequency difference to time difference and status of signal in each stage of transition is illustrated.



(a)



(b)

Figure 3.13: Simulated (a) GD and (b) magnitude of the phaser vs. frequency.

3.3 Fabrication and measurement

The proposed real-time spectrum sensor is fabricated using a 0.18-μm CMOS IBM technology. The overall area (including pads) and power consumption are 1.18 mm^2 and 20 mW, respectively. Fig. 3.15 shows the fabricated IC microphotograph. In Fig. 3.16 the temporal measurement setup is shown, where the gray part is the integrated chip. For simplicity a single tone for each channel rather than a wideband signal is used. Note that

multiplying a single tone with a Gaussian pulse creates a wideband signal at the center frequency of the single tone, so there is no need to create a wideband signal for each channel at the input. BW of the resulted signal from multiplication of the input and Gaussian pulse train (for each channel), which in this case is the same as the BW of the Gaussian pulse, should be smaller than the phaser frequency resolution. In Fig. 3.16, "In" is a multi-tone sinusoid coming from an Agilent E8267D PSG signal generator. It multiplies with a periodic Gaussian pulse coming from an arbitrary wave generator (AWG) (N8241A), which takes its data from a MATLAB code. The resulting signal passes through a tunable BP delay filter (phaser) with 12 states and then is multiplied by a delayed version of the Gaussian pulse. The resulted output is converted to a "1"-"0" pattern using an off-chip decision circuit, consisting of an amplifier, an envelope detector and a comparator, implemented on a PCB, along with the integrated detector. A 2 Gb/s oscilloscope (54625A Infiniium Oscilloscope) is used to observe the results. For temporal measurement, based on the AWG symbol rate, number of samples in the data coming from MATLAB, resolution of the oscilloscope, and channel spreading, period of the Gaussian pulses and clock signal, T_G, is chosen to be 0.2048 μs, which leads to a sensing time of $12\times T_G$=2.5 μs. Gaussian pulse duration is chosen to be 41 ns, which results in a BW of around 16 MHz (pulse duration is approximated by 6σ), which is less than the frequency steps of 27 MHz. This sets a margin of 12 MHz for the input signal channel BW (considering the BW of the BPF). For $GD_{Max} = 90$ ns, $GD_{min} = 50$ ns, $GD_{avg} = 70$ ns, $\Delta f_G = 16$ MHz ($T = 41$ ns), and $T_G = 0.2048$ μs, (3.11)-(3.16) are satisfied.

Fig. 3.17 shows measured output of the detector for four special cases. All channels cannot be applied simultaneously due to signal generator limitations. Input power levels in Fig. 3.17 are chosen in a way to avoid false detection, which will be explained later.

NF is measured in a conventional way and the output is connected to an spectrum analyzer (Agilent E4446A PSA), however, to measure NF for each channel, phaser needs

to operate in the state corresponding to that channel, without changing periodically, so that the frequency response of the detector doesn't change with time during measurement. Also since the noisy signal exists in part of the period, T_G, average number to the resolution BW ratio ($\frac{N_{avg}}{BW_{res}}$) in the spectrum analyzer is chosen much higher than T_G which results in a nearly static output power in the spectrum analyzer. NF of the detector changes between 3.8 dB and 5.1 dB for all channels.

For $IIP3$ measurement, output is connected to an oscilloscope and a two-tone test is used for each channel in time domain. For a conventional two-tone test, two tones are chosen within a band in a way to produce the third order intermodulation (IM3) products within the same band and the difference between the main tone and IM3 product determines $IIP3$. Here, the main tones and IM3 products cannot be measured in one single measurement and each should be measured separately; if the two tones are located in two adjacent channels and $IIP3$ is measured by looking at the output of the phaser at the adjacent channels (main tone) and main channel (IM3 product), the measured $IIP3$ would be unrealistically good. The reason behind this is that the IM3 product in the desired channel is resulted from two attenuated tones after passing through the BPF set to the center frequency of the desired channel, while each main tone in an adjacent channel shows the output of the phaser, when the BPF is set to the frequency of that channel. For measuring $IIP3$ for each channel without the attenuation effect of the BPF, the main tone and the IM3 product in the desired channel can be measured separately; for measuring the main tone in the desired channel, one single tone in that channel is applied to the system. For measuring the IM3 product in the desired channel, two tones are located out of the channel in a way to produce an IM3 product within the desired channel; however, the input power of these two tones are chosen higher than that of the first measurement to compensate for the attenuation created by the BPF (when it is set to the desired channel). Fig. 3.18 shows the method of measuring $IIP3$ in time domain for the first channel ($f_{Ch1} = 57$ MHz).

Fig. 3.18a shows the output of $Ch1$ in time domain for an input with a power of -20 dBm located at f_{Ch1}, while Fig. 3.18b shows the resulting IM3 product at f_{Ch1} from two input tones located at 178.5 MHz and 300 MHz, each with an effective power of -20 dBm (after attenuation by the BPF). After measuring voltage of both main and IM3 products, following equation is used to calculate $IIP3$:

$$IIP3 = P_{in} + 10log(\frac{v_{out}}{v_{IM3,out}}) \tag{3.20}$$

Which leads to an $IIP3$ of -3.8 dBm for the first channel. $IIP3$ changes between -3.8 dBm and 2.7 dBm for this detector over the 57-354 MHz band. Fig. 3.19 shows measured NF and $IIP3$ for each channel.

Fig. 3.20 shows the detected power and the detection error at the output of the off-chip envelope detector vs. input power for channel 7 (center frequency of 219 MHz). Note that the RC filter in the envelope detector smooths the detected power variation by averaging. Gain of the off-chip amplifier for Fig. 3.20 is set to 21 dB. As shown in Fig. 3.20, the detection dynamic range (DR) is 71.5 dB (-85.3 dBm$\sim$-13.8 dBm) within $\pm$1 dB error. Sensitivity and 1-dB compression point change between -85.9 dBm to -84.6 dBm and -17.3 dBm to -11.5 dBm, respectively, resulting in a DR of 68.6 dB to 73.1 dB from channel 1 to 12.

False detection is a scenario in which the signal doesn't exist in the intended channel but it exists in the adjacent channel and the detector falsely indicates the presence of the signal in the intended channel. For continuous time signal detection, false alarm probability (P_{FA}) is: $P_{FA} = e^{-\gamma^2/2\sigma^2}$ [52], where γ is the comparator threshold voltage and σ^2 is the estimated noise power. A 3 dB noise uncertainty is considered for σ^2 estimation [53]. For P_{FA} of %10, threshold voltage is: $\gamma = 2.146\sigma$. To have a P_{FA} of %10 and a detection probability (P_D) of better than %90, an SNR of higher than 7.2 dB is required, when a

continuous time decision circuit, based on ED is employed to test the functionality of the integrated detector [52].

Fig. 3.21 shows the minimum input power in an adjacent channel leading to a false detection (P_{FA}=%10) vs. channel number, when the input to the phaser has a channel BW of 16 MHz (signal BW+Gaussian pulse BW). For example, if the signal level in channel number "4" or "6" exceeds -23 dBm, there might be a false detection in channel number "5". The variation in Fig. 3.21 comes from different GD, frequency response, and BW of each state (see Fig. 3.13). Fig. 3.21 interprets to a tolerable INR of 72 dB to 87 dB, which is hard to achieve using conventional magnitude-based spectrum sensors (INR_{Max} is 30 dB in [16, 17]).

Table 3.1 shows the performance summary of the proposed real-time spectrum sensor in comparison to the state-of-the-art spectrum sensors. Real-time spectrum sensing in [12, 15] is performed using a wideband fast-sweeping frequency synthesizer, an RF front-end, and a wavelet-based spectrum-sensing block. In [16, 17] it is performed using a digital processor, assuming the input data is a BB signal in digital domain, and lastly in [45] it is performed using a dual-mode detection technique (ED and CD as coarse and fine tuning techniques, respectively) after an RF front-end with frequency down-conversion and BB filtering. However, [45] uses a software for spectrum-sensing blocks with no actual circuits. The method in [16, 17] requires using an RF front-end and a high BW ADC to operate with RF signals and is not applicable to very wideband applications. The needs for a wideband frequency synthesizer for conventional spectrum sensors such as [9, 11, 12, 13, 45, 15], and a wideband ADC for [17, 16], make the proposed method outperform previous methods in terms of complexity and power consumption. However, the reason of not having a high power consumption in [17, 16] is that the wideband ADC contribution is not considered in the system performance. Sensing time depends on the target BW and frequency resolution which are different for all the works in Table 3.1.

Parameter	This work	[12]	[11]	[13]	[17]	[45]	[15]
Spectrum Sensing Type	Analog/ Phaser	Analog/ Dig/ED	Analog/ ED	Analog/ QCFD	Dig/ ED	Analog/ CD/ED	Analog/ ED
Freq Range (MHz)	57∼354	400∼900	30∼ 2400	54∼862	200 in BB	300∼ 700	3100∼ 10600
Freq Res (MHz)	27	0.025∼0.8	0.2∼30	8	0.2	6	132
ST.Res/BW (μs.MHz/MHz)	0.23	57.53	-	-	50^{h}	1.5^{i}/15^{j}	7.4
NF (dB)	3.8∼5.1	-	5∼8	-	-	3.5	6.9∼7.6
IIP3 (dBm)	-3.8∼2.7	-	-11	-	-	-12	-7.9
INR (dB)	72∼87	-	-	25^{e}	30	-	-
Sensitivity/Res (dBm/MHz)	-100.2∼ -98.9	-62.5	-76	-	-	-98.8^{i}/ -111.8^{j}	-95.2
SNR_{min} (dB)	>0	>0	>0	-24	-5	>0	>0
DR (dB)	68.6∼ 73.1	32	29∼48	39	-	84	35
Power Diss (mW)	$20^{a,b}$	122^{c}	30∼ $44^{c,f}$	$57^{a,f,g}$	$7.4^{c,f,g}$	$28^{f,k}$	26.4∼ 47.9^{c}
Area (mm^2)	1.18	9.2	2.34^{d}	1.08	1.64^{d}	1.2	2.53
CMOS Tech	0.18 μm	0.18 μm	90 nm	0.18 μm	65 nm	65 nm	65 nm

Table 3.1: Performance Summary and Comparison of the Proposed Spectrum Sensor with Previously Reported Spectrum Sensors
[a] Excluding the off-chip decision circuit. [b] Excluding the external Gaussian signal generator. [c] Excluding the external ADC. [d] Active area. [e] Within 32 MHz. [f] Excluding the external LO signal generator. [g] Excluding the external RF front-end. [h] Is 1 for an INR of 20 dB. [i] ED with 1 dB noise error. [j] CD with 1 dB noise error. [k] Includes only an RF front-end and BB filters.

So a new parameter is employed in Table 3.1 to evaluate the sensing time performance as: Sensing Time.Resolution/BW. This parameter for the proposed method is far below the conventional techniques. Also the high IIP3 of the proposed technique compared to other methods shows the effect of removing frequency down-conversion in phaser-based spectrum sensing. On the other hand, phaser-based spectrum sensors cannot achieve the frequency resolution of conventional spectrum sensors, unless a high Q tunable phaser is used, to have higher GDs, leading to higher sensing time. This makes them mostly suitable for interferer detection.

3.4 Conclusion

An integrated real-time spectrum sensor has been described and fabricated in a 0.18-μm CMOS IBM technology, which achieves a low sensing time, while preserving a good noise and linearity performance. The proposed phaser-based method, which employs both magnitude and GD characteristics of BPFs, simplifies real-time spectrum sensing for a wideband signal, accomplishing a low area and power consumption. It achieves a sensing time of 2.5 μs for a frequency range of 57-354 MHz with 27 MHz resolution and a power consumption of 20 mW.

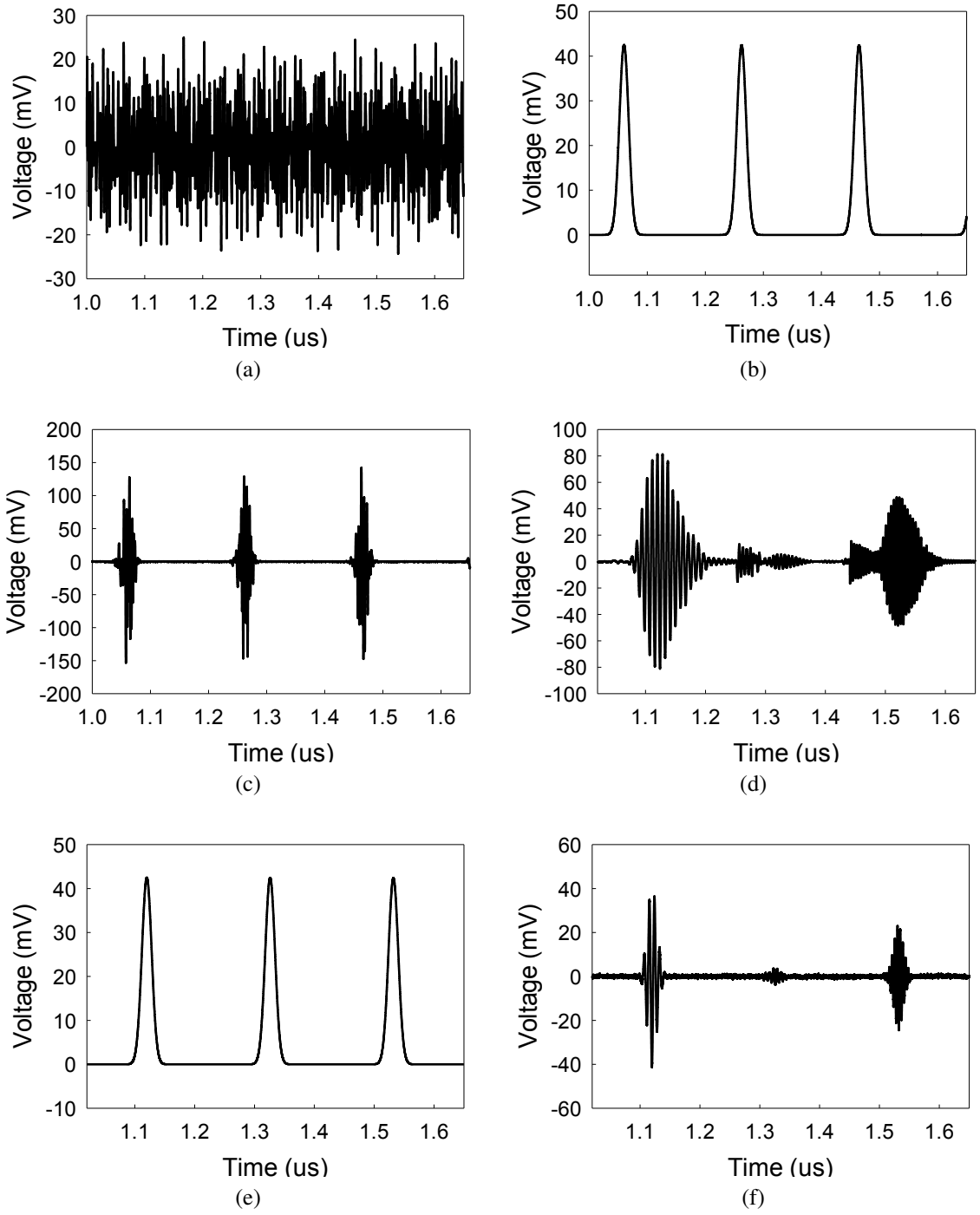


Figure 3.14: Transient simulation of the detector for an input consisting of four tones located at f_{Ch3}, f_{Ch5}, f_{Ch8}, and f_{Ch12} (each with the power of -40 dBm) and the resulting output at f_{Ch3} to f_{Ch5} for the following points; (a) input, (b) Gaussian pulse train, (c) input of the phaser, (d) output of the phaser, (e) delayed Gaussian pulse train, (f) output.

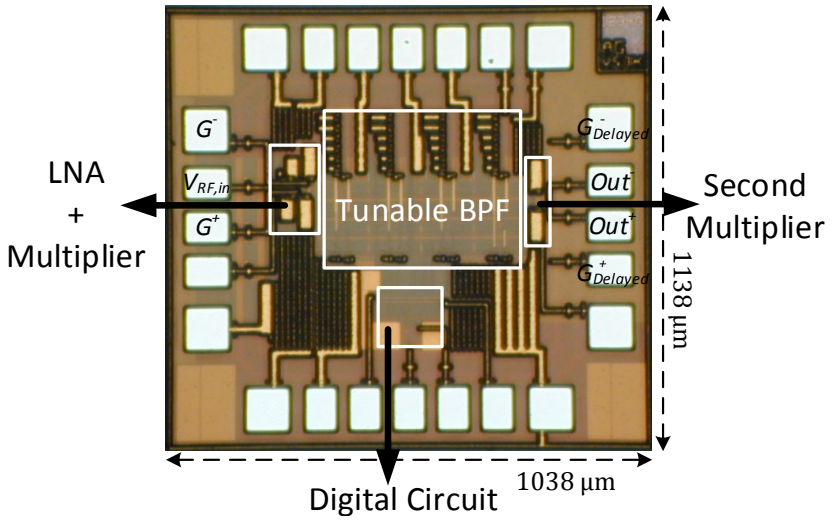


Figure 3.15: Die micrograph of the fabricated Phaser detector.

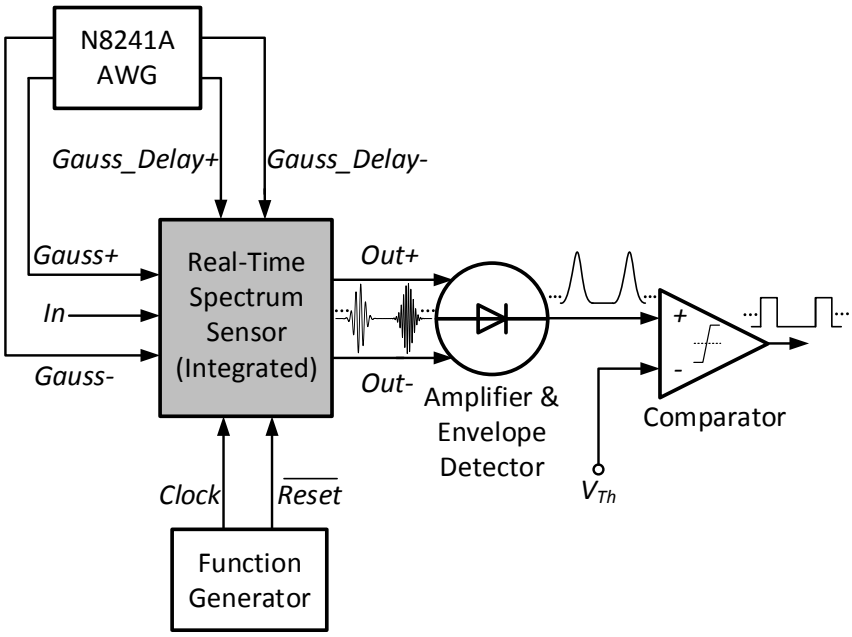


Figure 3.16: Temporal measurement setup.

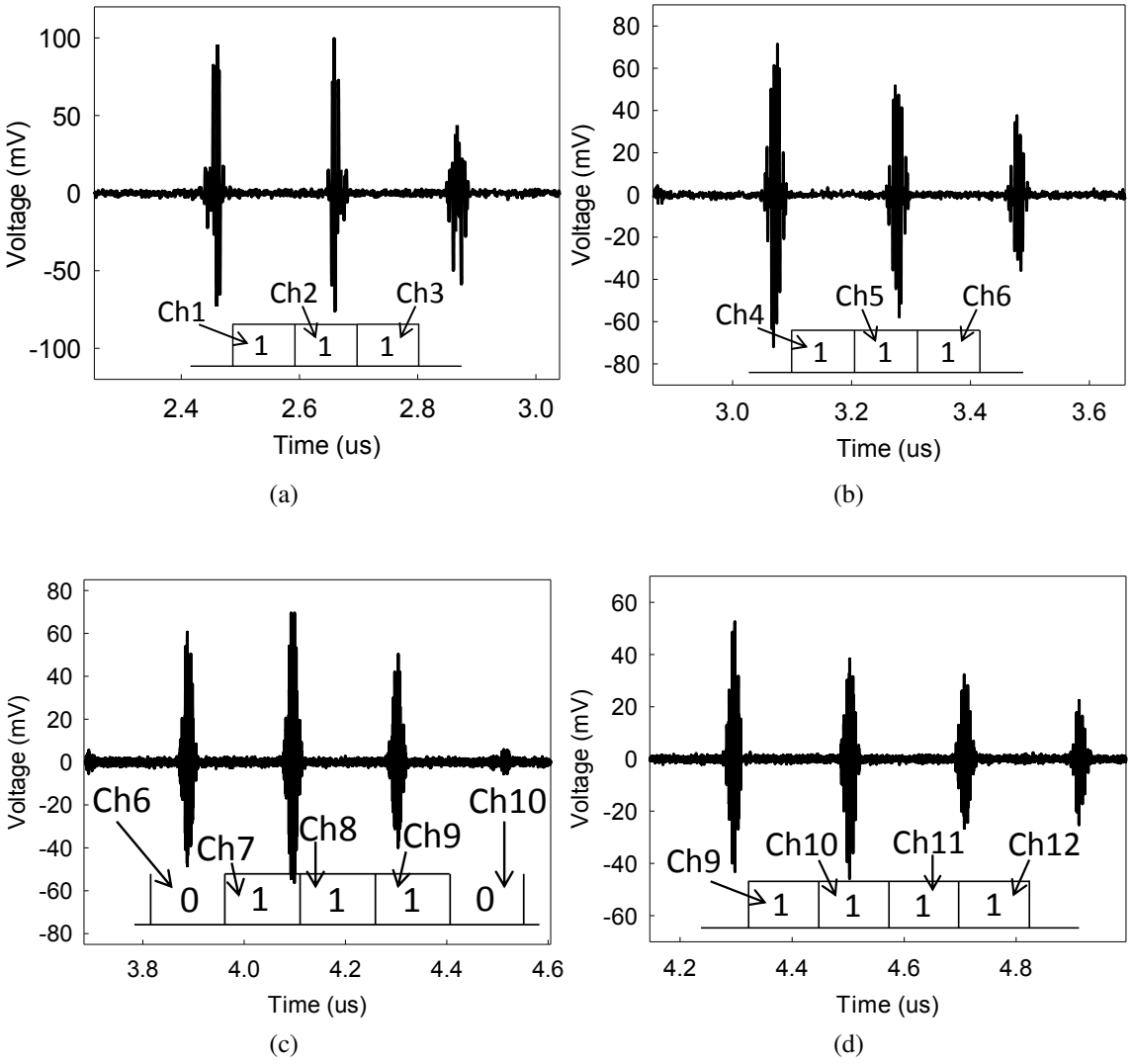
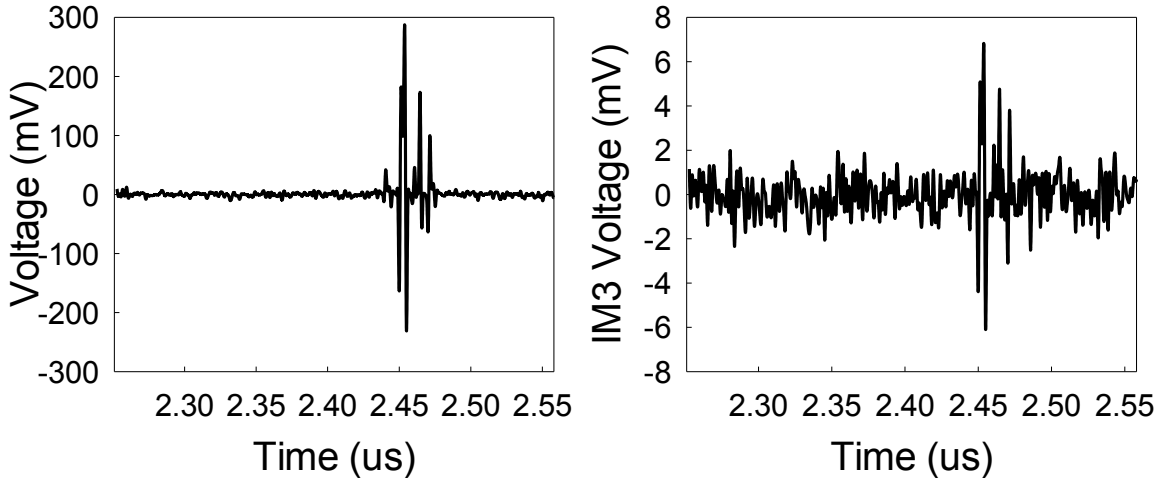
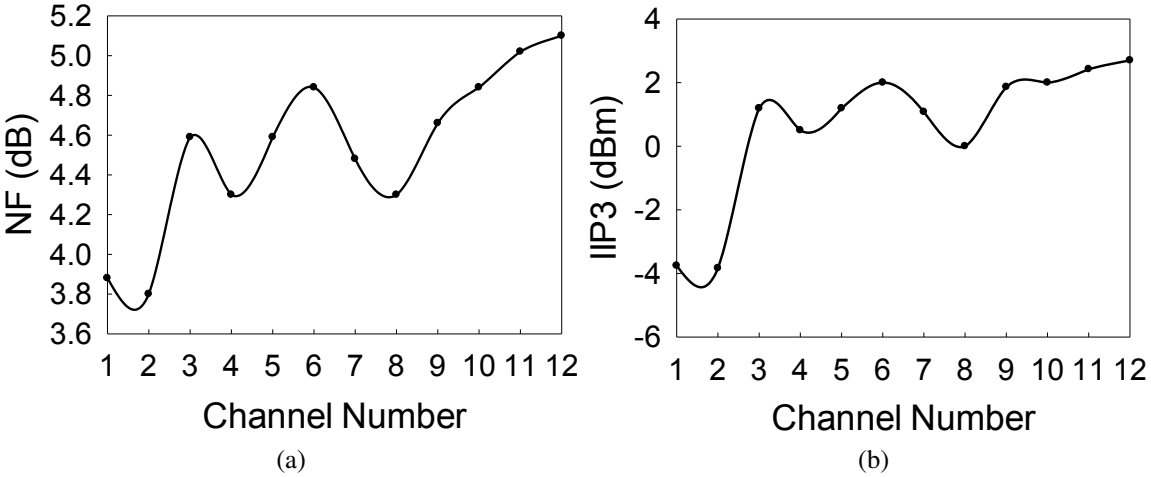


Figure 3.17: Temporal measurements at the output of the detector when input signal exists in; (a) f_{Ch1}, f_{Ch2}, and f_{Ch3}; (b) f_{Ch4}, f_{Ch5}, and f_{Ch6}; (c) f_{Ch7}, f_{Ch8}, and f_{Ch9}; (d) f_{Ch9}, f_{Ch10}, f_{Ch11}, and f_{Ch12} (P_{in}=-30 dBm for each channel, $V_{Peak,Gaussian}$=42 mV).



(a) (b)

Figure 3.18: Measured output at f_{Ch1} for; (a) an input power of -20 dBm located at 57 MHz, and (b) for two tones with the same power (after attenuation) located at 178.5 MHz and 300 MHz.



(a) (b)

Figure 3.19: Measured (a) NF vs. channel number, and (b) $IIP3$ vs. channel number.

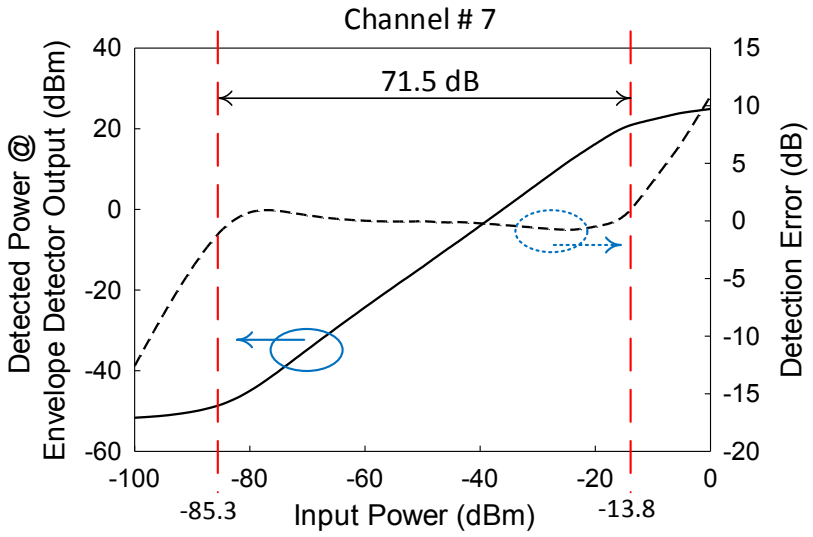


Figure 3.20: Measured detected power and the detection error at the output of the envelope detector vs. input power.

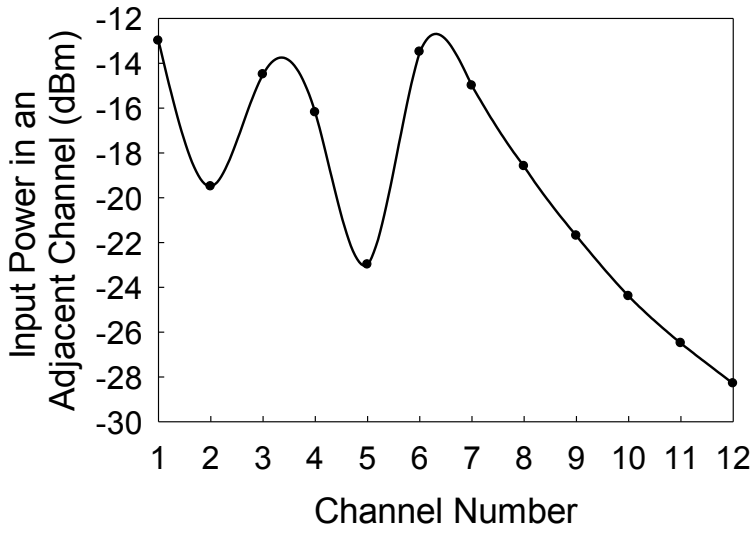


Figure 3.21: Minimum input power which leads to a false detection vs. channel number.

4. UWB RX WITH BLOCKER DETECTION AND REJECTION*

In this chapter an efficient solution for increasing robustness of UWB receivers towards NB interferers is proposed. This technique involves employing a phaser-based real-time spectrum sensor for detecting the frequency locations of interferers at a specific time. The detected blockers are removed with notch filters in the receiver.

4.1 Proposed architecture

4.1.1 UWB receiver

The target frequency band for the UWB receiver is 3.1-4.8 GHz, corresponding to the first UWB group, so in-band IIP2 is of less concern and a direct conversion architecture [24] is adequate considering its simplicity and area towards super-heterodyne [27, 54], requiring image rejection, and multi-path receiver [55], employing parallel NB paths with different LO frequencies. Note that IM2 products resulting from LNA second order nonlinearities and RF to IF feed-through, and also DC offset can cause issues for a wideband direct-conversion receiver. For LNA IIP2 issues, differential LNAs or LNAs with selectivity at their output are desired. Here, impedance transfer feature of a voltage-mode passive mixer (which is explained later in this section) is utilized for creating a BPF at the output of the LNA and removing IM2 products. It is assumed that DC offset is removed in variable gain amplifiers (VGAs) (which are not implemented here) after BB filtering. Fig. 4.1 shows the entire system including both receiver and blocker detection architectures.

Notch filters should be placed at the beginning of the receiver path, for the best out-of-band linearity performance, before the saturation of the receiver by strong blockers. Since the noise performance is also important due to weak UWB signals, notch filters are placed

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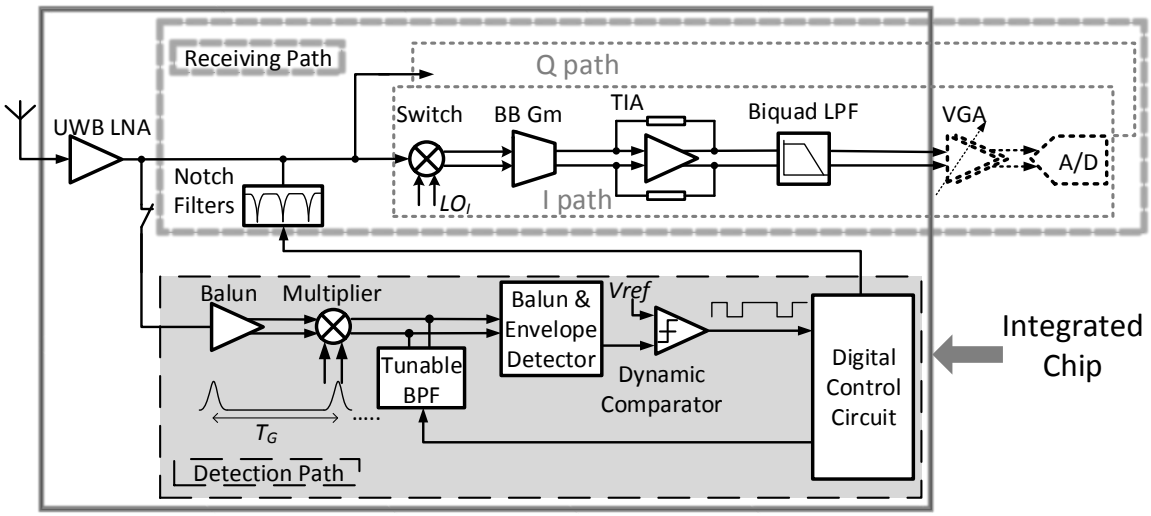
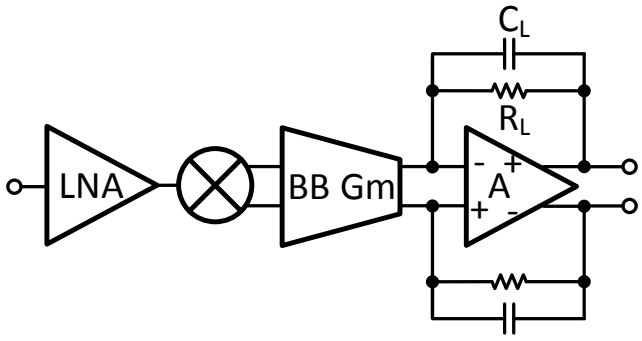


Figure 4.1: Proposed UWB receiver with blocker detection architecture.

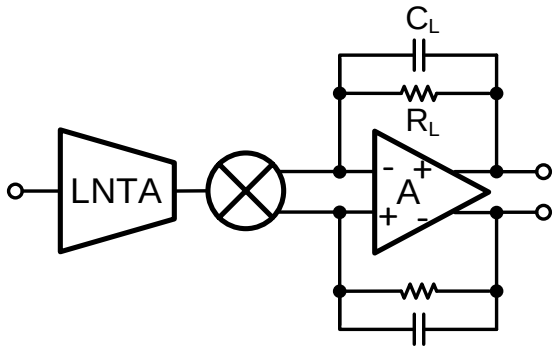
after the LNA.

Gain of the LNA is chosen to be relatively small (14 dB) to avoid signal saturation due to blockers. Further amplification of the weak UWB signal is required to preserve good NF for the entire system and needs to be performed after blocker rejection to avoid any saturation by the blockers. Passive mixers are used for better linearity considering the low supply voltage of the 65 nm CMOS process (1 V). Two types of front-ends can be implemented using passive mixers; voltage-mode or current-mode (Fig. 4.2). Voltage mode includes LNA, switch, BB Gm, and TIA, while current mode is the combination of LNA and Gm-cell (LNTA), switch, and TIA.

Fig. 4.2 can be simplified as Fig. 4.3, at the output of the LNA (LNTA), when switches of the mixer are "on" and can be modeled with an R_{on} resistance. Note that LNA in Fig. 4.3a and LNTA in Fig. 4.3b are realized with their Norton equivalent, assuming the output impedance of the LNA can be modeled with a resistor in parallel with a capacitor ($R_{o,LNA}$ and $C_{o,LNA}$), while the LNTA output impedance is approximated with a capacitor ($C_{o,LNTA}$). Also BB Gm of Fig. 4.2a is modeled as C_{i,G_m} in Fig. 4.3a.



(a)



(b)

Figure 4.2: Front-end utilizing a (a) voltage-mode passive mixer, and (b) current-mode passive mixer.

Mixing function in time domain results in a convolution in frequency domain, transferring the BB impedance to LO frequency. The voltage seen at the LNA (LNTA) output, $V_{o,LNA}$ ($V_{o,LNTA}$), is calculated by multiplying $I_{o,LNA}$ ($I_{o,LNTA}$) by the impedance seen at that point. For voltage mode, this results in a zero at

$$\omega_{Z,V} = \omega_{LO} \pm \frac{1}{R_{on} C_{i,G_m}} \tag{4.1}$$

and two poles corresponding to C_{i,G_m} and $C_{o,LNA}$. If the LNA has a high BW ($C_{o,LNA} \ll$

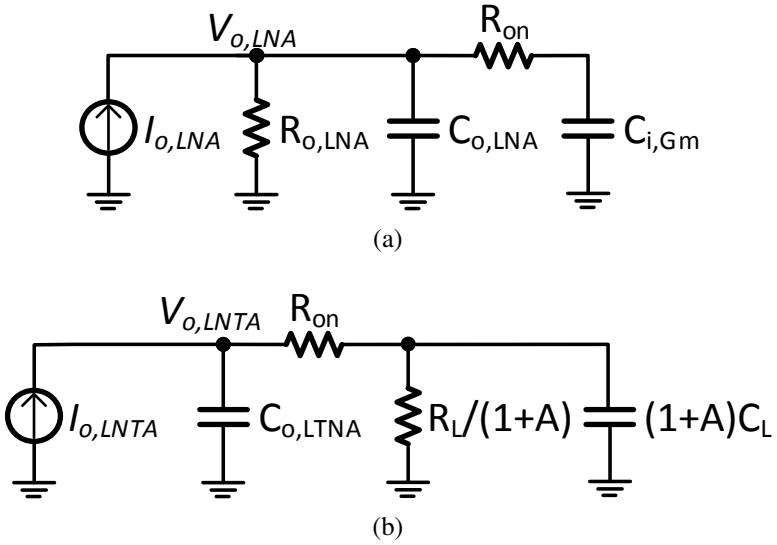


Figure 4.3: Norton simplification of Fig. 4.2 at the output of the LNA (LNTA) for (a) voltage-mode, and (b) current-mode passive mixer.

$C_{i,Gm}$), the poles can be approximated as

$$\omega_{P1,V} = \omega_{LO} \pm \frac{1}{(R_{on} + R_{o,LNA})C_{i,G_m}} \tag{4.2}$$

$$\omega_{P2,V} = \frac{1}{(R_{on}||R_{o,LNA})C_{o,LNA}} \tag{4.3}$$

where ω_{P1} is resulted from impedance transfer from BB to LO frequency. Note that using a large switch for lowering R_{on} is not desirable here as it introduces a significant parasitic capacitor to $C_{o,LNA}$, lowering BW of the LNA. Besides, $R_{o,LNA}$ cannot be very large, due to headroom and gain limitation of the LNA. So R_{on} can be comparable with $R_{o,LNA}$. Therefore, the zero reduces the rejection caused by the first pole, however its effect is reduced by the second pole ($\omega_{P2,V}$) at higher frequencies.

Now consider the current mode mixer of Fig. 4.3b, which again results in an LNTA output voltage with one zero ($\omega_{Z,I}$) and two poles ($\omega_{P1,I}$ and $\omega_{P2,I}$). As mentioned before,

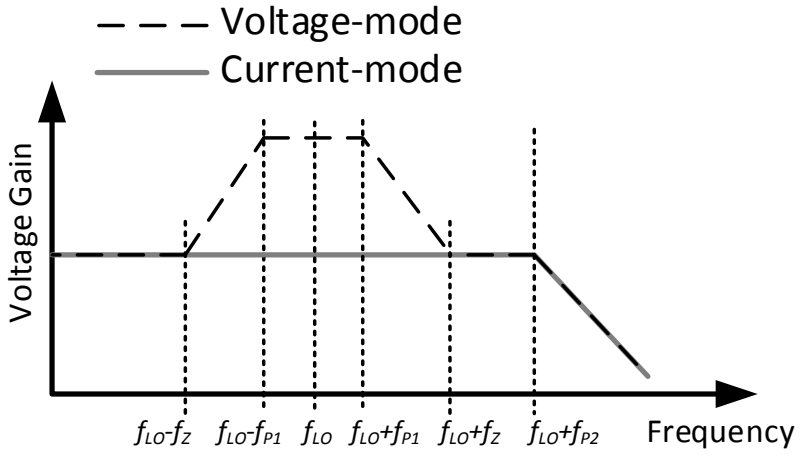


Figure 4.4: Voltage gain at the output of the LNA/LNTA.

R_{on} cannot be very small, and as a result:

$$R_{on} \gg \frac{R_L}{1+A} \tag{4.4}$$

Equation (4.4) approximates the impedance seen at the output of the LNTA with only one pole located at

$$\omega_{P2,I} = \frac{1}{R_{on}C_{o,LNTA}} \tag{4.5}$$

which is not resulted from impedance transfer and is undesirable as it limits the BW of the LNTA. In another words, with the condition mentioned in (4.4), the zero cancels out with the first pole ($\omega_{Z,I} \approx \omega_{P1,I}$). Fig. 4.4 compares the voltage-mode and current-mode voltage gain frequency response at the output of the LNA/LNTA, assuming $\omega_{Z,V} = \omega_Z$, $\omega_{P1,V} = \omega_{P1}$, $\omega_{P2,V} = \omega_{P2,I} = \omega_{P2}$, and also the DC-gain is equal in both cases. As shown in Fig. 4.4, the impedance transfer feature in not observed in current-mode for high frequency applications.

Since having a low input impedance at the input of the TIA is not critical in voltage mode, gain-BW (GBW), noise, and power consumption of the op-amp of the TIA are more

relaxed without degrading the sensitivity compared to current-mode [56, 57]. There is no superiority in terms of power consumption for the two front-ends as the power consumption of the extra Gm-cell plus TIA in the voltage-mode is comparable with the TIA in the current-mode. As a result, voltage-mode mixer topology is chosen here based on the mentioned advantages over its current-mode counterpart.

BB Gm should have a high transconductance and low noise to compensate for the low gain of the LNA to provide a reasonable NF for the entire receiver.

Further linearity improvement is performed in the TIA of the mixer and the subsequent BB LPFs. Here, a biquad active-RC LPF is used along with a TIA with an RC feedback, which overall with the BB Gm create a fourth order LPF at the output of the receiver. So BB filtering of the voltage-mode also outperforms the current-mode with similar BB LPFs, due to the extra pole created by the BB Gm.

4.1.2 Blocker detector

As mentioned earlier, out-of-band linearity performance is strict for a UWB receiver due to strong adjacent blockers. In a UWB system, while possible locations of the adjacent blockers are known, their presence is not guaranteed; this means a dynamic blocker detector which dynamically detects the location of blockers and reports them to the notch filters used in the receiver, can reduce the number of notch filters.

Here, three tunable notch filters are employed, which means up to three blockers (detected by the blocker detector) can be simultaneously rejected. Possible locations are divided to 3 sub-bands: 2.35-2.75 GHz (802.11b/g and WiMAX), 5.1-5.5 GHz, and 5.5-5.9 GHz (802.11a, HiperLAN/2, etc.). Note that WiMAX (3.3-3.7 GHz) is within the band and placing a notch filter in the band can degrade the system specs significantly, so a notch filter is avoided in this band, however its interferer effect is evaluated.

The blocker detector architecture is also shown in Fig. 4.1. LNA is a common block

between the receiver and blocker detector. After the LNA in the detection path, the signal is converted to a differential one using an active balun, then time limited (in a specific period of T_G) by a multiplier which multiplies the signal by a Gaussian pulse train with a period of T_G. The resulted signal passes through a phaser [20], which is a tunable BPF with BP GD response. The phaser converts the frequency difference in the incoming signal to time difference, discriminating the blockers in time domain.

The output of the phaser passes through a differential to single-ended buffer and then an envelope detector and a dynamic comparator, which converts the delayed signal in each period of T_G to a "1"-"0" pattern, which "1" indicates the presence of the interferer at a specific frequency. To make the detection procedure simpler, the first detected blocker in each sub-band is reported to the notch filters of the receiver. So the reference voltage of the comparator (V_{ref}) is chosen based on the interferer power. It should be lower than the received interferer power at the input of the comparator and higher than the UWB signal power and noise of the comparator, as only detection of the interferer is desired.

Using a digital circuitry, the first frequency occupied by a blocker in each mentioned sub-band is selected, so up to three blockers are located. Then this information is mapped to the notch filters of the receiver and corresponding switches in the notch filters are selected automatically.

Linearity is the most important factor for detecting strong blockers and a phaser-based detector can achieve a reliable detection. It does not require a non-linear mixer. Instead, it employs a linear multiplier. The balun after the LNA results in a more linear multiplier, while it is not necessary for the receiving path for the intended frequency band, as the noise performance is of more concern compared to second order non-linearity.

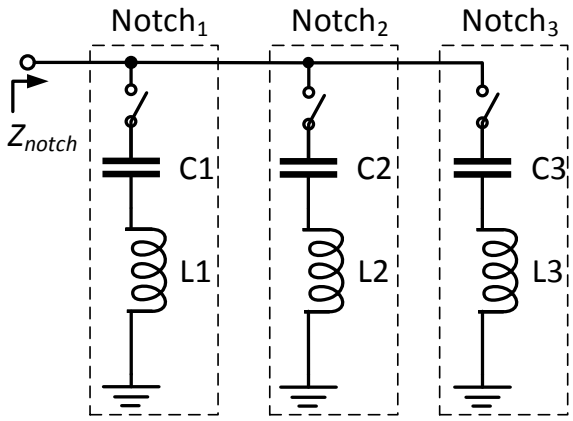


Figure 4.5: LC series notch filters.

4.2 Active filter design considerations

Three notch filters are employed as the output load of the LNA (see Fig. 4.1). To be able to disconnect the notch filters easily without much effect on the signal, series resonant LC notch filters are used (Fig. 4.5). Z_{notch} impedance in Fig. 4.5 is calculated as follows (not considering the effects of "on"/"off" switches)

$$
\begin{aligned}
&Z_{notch}(\omega) = \\
&[(1-\omega^2 C_1 L_1)(1-\omega^2 C_2 L_2)(1-\omega^2 C_3 L_3)]/ \\
&[j\omega(\omega^4 C_1 C_2 C_3 (L_1 L_2 + L_1 L_3 + L_2 L_3) - \\
&\omega^2 (C_1 L_1 (C_3 + C_2) + C_2 L_2 (C_1 + C_3) + C_3 L_3 (C_1 + C_2)) + \\
&C_1 + C_2 + C_3)]
\end{aligned} \tag{4.6}
$$

Note that (4.6) provides the impedance when all three notch filters are active. The effect of deactivating each filter can be observed by setting the corresponding inductor and capacitor to infinity and zero, respectively. The numerator zeros in (4.6) determine the notch

frequency locations and are given as follows:

$$\omega_{Zi}^2 = \frac{1}{C_i L_i}, (i = 1, 2, 3) \tag{4.7}$$

Each zero is assigned to one of the sub-bands; ω_{Z1}, ω_{Z2}, and ω_{Z3} are corresponding to 2.35-2.75 GHz, 5.1-5.5 GHz, and 5.5-5.9 GHz, respectively. Setting the denominator in (4.6) to zero provides poles of $Z_{notch}(\omega)$, which satisfy the following equations:

$$\omega_{P1}^2 \omega_{P2}^2 = \frac{C_1 + C_2 + C_3}{C_1 C_2 C_3 (L_1 L_2 + L_1 L_3 + L_2 L_3)} \tag{4.8}$$

$$\omega_{P1}^2 + \omega_{P2}^2 = \frac{C_1 L_1 (C_3 + C_2) + C_2 L_2 (C_1 + C_3) + C_3 L_3 (C_1 + C_2)}{C_1 C_2 C_3 (L_1 L_2 + L_1 L_3 + L_2 L_3)} \tag{4.9}$$

These two poles, ω_{P1} and ω_{P2}, are placed between ω_{Z1}, ω_{Z2} and ω_{Z2}, ω_{Z3}, respectively. Fig. 4.6 shows impedance Z_{notch} and the locations of zeros and poles for a specific case, when L_1^A=16 nH, $L_{2,3}^A$=8 nH, C_1^A=275 fF, C_2^A=122 fF, and C_3^A= 105 fF, resulting ω_{Z1}=2.4 GHz, ω_{Z2}=5.1 GHz, ω_{Z3}=5.5 GHz, ω_{P1}=3.2 GHz, and ω_{P2}=5.3 GHz (using ideal capacitors, inductors, and switches). Fig. 4.7 shows S_{21} of a network with the load of Z_{notch}, for three different values of inductors and capacitors, resulting the same zeros and poles; first values are the same as the ones used in Fig. 4.6, L_{1-3}^A and C_{1-3}^A, second values are L_{1-3}^B=$0.5 \times L_{1-3}^A$, C_{1-3}^B=$2 \times C_{1-3}^A$, and third values are L_{1-3}^C=$0.125 \times L_{1-3}^A$, C_{1-3}^C=$8 \times C_{1-3}^A$. As Fig. 4.7 suggests, higher values for inductors results in less in-band variations. Note that in Fig. 4.7, port resistors reduce the effect of ω_{P1} and ω_{P2}, preventing the impedance to go to infinity at the pole location. So, the impact of the poles on the gain flatness is reduced by designing the LNA with a low impedance load. Q of the inductors limits the notch rejection. Fig. 4.8 shows the $S21$ for different values of Q, when L_{1-3}^A and C_{1-3}^A values are selected for the inductors and capacitors. As shown in Fig. 4.8, a Q of at least 100 is required to achieve a rejection of 20 dB, which is not possible using on-chip passive

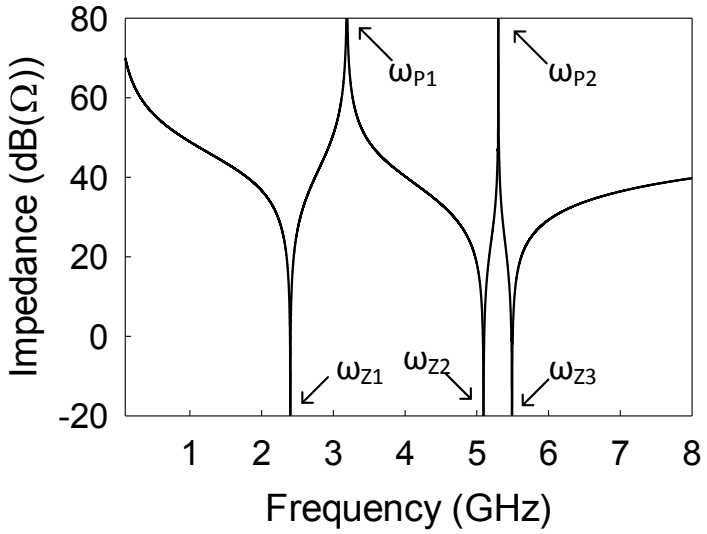


Figure 4.6: Impedance Z_{notch} and the locations of zeros and poles for, when L_1^A=16 nH, $L_{2,3}^A$=8 nH, C_1^A=275 fF, C_2^A=122 fF, and C_3^A= 105 fF.

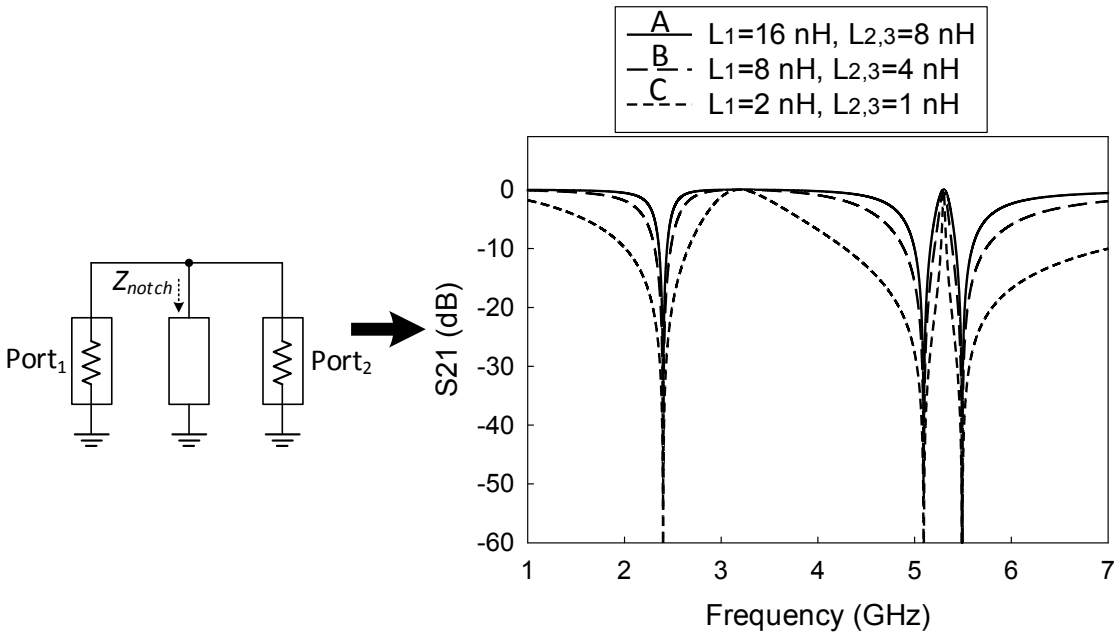


Figure 4.7: S_{21} of a network with the load of Z_{notch} for three different values of inductors and capacitors with similar pole, zero locations.

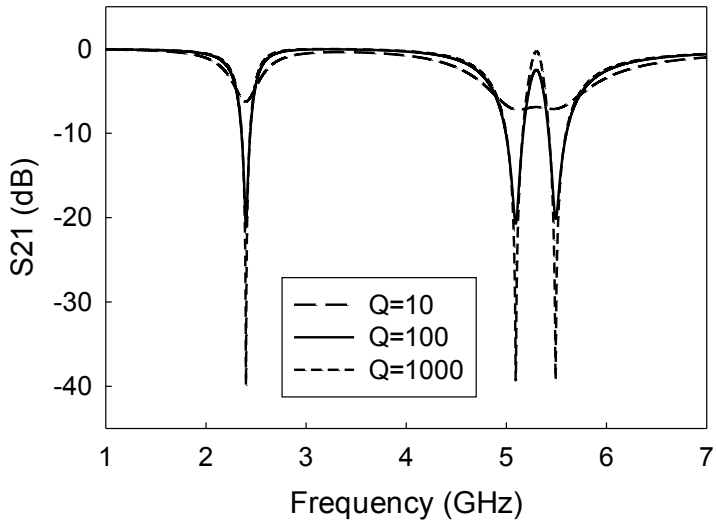


Figure 4.8: $S21$ for different values of Q, using L^A_{1-3} and C^A_{1-3}.

inductors.

The BPFs, which are used as a phaser, are placed as the output load of the multiplier, in the detection path (see Fig. 4.1). To disconnect the BPFs easily without much effect on the signal and also employ only one inductor for each filter for a differential signal, parallel resonant LC BPFs are used (Fig. 4.9). Since only one of the BPFs is active at a time (L_4 and C_4 in Fig. 4.9), the BPF impedance equation only reflects the effect of one set of inductor and capacitor, which is (not considering the effects of "on"/"off" switches)

$$Z_{BPF}(\omega) = \frac{j\omega L_4}{1 - \omega^2 C_4 L_4} \tag{4.10}$$

C_4 and L_4 create a pole corresponding to the center frequency of the BPF at:

$$\omega_P^2 = \frac{1}{C_4 L_4} \tag{4.11}$$

For an ideal inductor and capacitor and a switch resistance of zero, GD of (4.10) is infinity

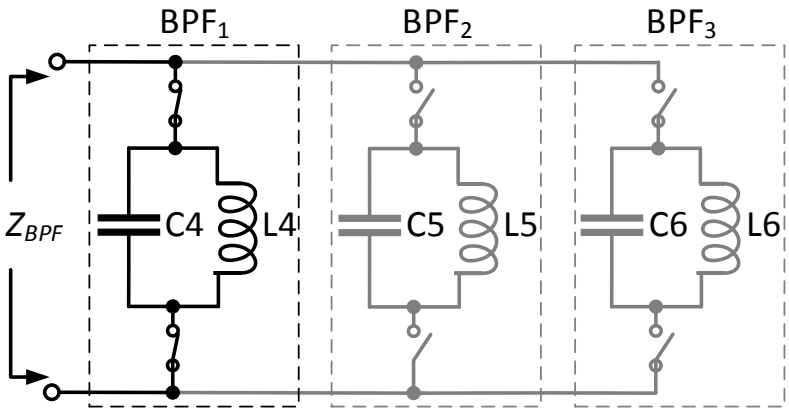


Figure 4.9: LC parallel BPFs.

at frequency of (4.11) and zero elsewhere. Placing the BPFs in a network similar to Fig. 4.7 with an overall parallel resistor of R_P, will reduce the maximum GD at frequency of (4.11) to

$$GD_{Max} = 2R_P C_4 \tag{4.12}$$

Fig. 4.10 shows the S_{21} and GD of the network with three BPF of Fig. 4.9 as load (one connected at a time), for R_P of 1 kΩ and 4 kΩ. In Fig. 4.10 capacitor values are chosen similar and inductor values change based on the center frequency ($C_{4,5,6}$=550 fF, L_4=8 nH, L_5=1.7 nH, and L_6=1.5 nH) to achieve a similar maximum GD for all three BPFs.

Passive inductors alone do not provide a high enough Q and are not area efficient, so for each inductor in filters of Fig. 4.5 and Fig. 4.9 a high-Q gyrator-based active inductor is used (Fig. 4.11), which consists of two back-to-back connected Gm-cells, and inverts the load impedance (capacitor) to its input. For the case of notch filters of Fig. 4.5, each filter can be disconnected by connecting the bias of each gyrator to zero, so there is no need for using switches in the main path of each filter for connecting/disconnecting purposes. For BPFs of Fig. 4.9, the use of switches in the main filter path is unavoidable, as the capacitors cannot be disconnected by only disconnecting the inductors using their bias.

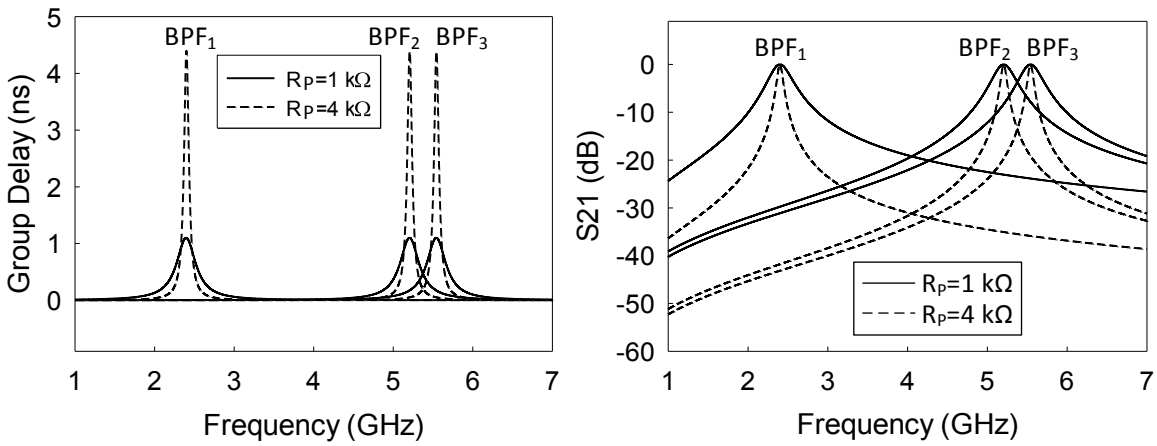


Figure 4.10: (a) GD, and (b) S_{21} of a network with three BPFs of Fig. 4.9 as load and R_P of 1 kΩ and 4 kΩ ($C_{4,5,6}$=550 fF, L_4=8 nH, L_5=1.7 nH, and L_6=1.5 nH).

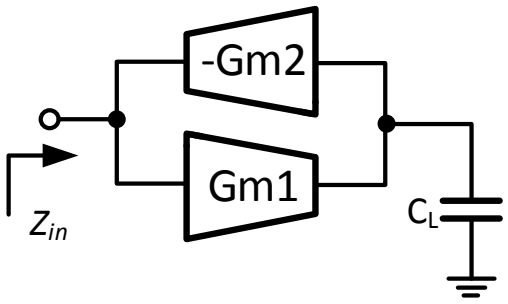


Figure 4.11: A single-ended implementation of a wideband gyrator.

Considering the effect of switch resistance, (4.12) changes to

$$GD_{Max} = 2R_P C_4 - 4R_{sw} C_4 \tag{4.13}$$

where, R_{sw} is the "on" resistance of each switch.

The inductor equation for the gyrator shown in Fig. 4.11 using ideal Gm-cells is as

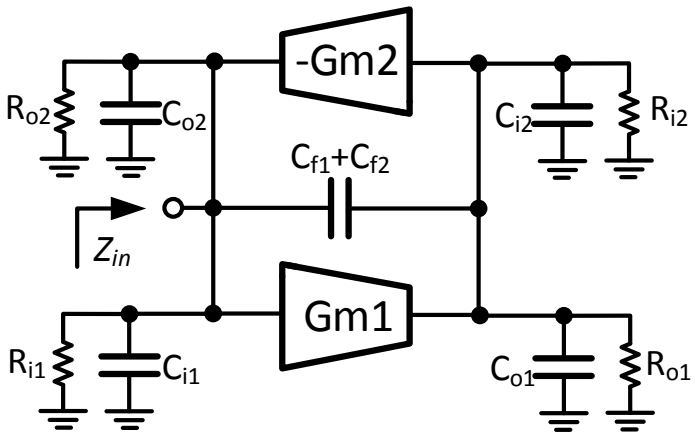


Figure 4.12: Gyrator of Fig. 4.11 with all the parasitics.

follows:

$$L_{in} = \frac{C_L}{G_{m1}G_{m2}} \tag{4.14}$$

Fig. 4.12 shows the gyrator of Fig. 4.11 with all the parasitics of the Gm-cells, assuming no internal nodes (C_L in Fig. 4.11 is considered as a parasitic capacitor).

The parasitic resistors and capacitors of Fig. 4.12 are given as

$$R_i = R_{i1} + R_{o2};\ R_o = R_{i2} + R_{o1} \tag{4.15}$$

$$C_i = C_{i1} + C_{o2};\ C_o = C_{o1} + C_{i2};\ C_f = C_{f1} + C_{f2} \tag{4.16}$$

where R_{i1} (R_{i2}) and R_{o1} (R_{o2}) are parasitic input and output resistors of G_{m1} (G_{m2}), respectively and C_{i1} (C_{i2}), C_{o1} (C_{o2}), and C_{f1} (C_{f2}) are parasitic input, output, and feedback capacitors of G_{m1} (G_{m2}), respectively. For identical Gm-cells, $C_i = C_o$ and $R_i = R_o$, so Z_{in} can be estimated as

$$Z_{in}(\omega) = \frac{R_g + j\omega L_g}{1 + j\omega\left(\frac{L_g}{R_o} + C_i R_g\right) + \left(\frac{\omega}{\omega_0}\right)^2} \tag{4.17}$$

where

$$R_g = \Big(G_{m1}G_{m2}R_o\Big)^{-1};\;\; L_g = \frac{C_i + C_f}{G_{m1}G_{m2}} \tag{4.18}$$

and

$$\omega_o = \sqrt{\frac{1}{L_g\Big(C_i + \frac{C_iC_f}{C_i+C_f}\Big)}} \tag{4.19}$$

Equation (4.17) shows that Z_{in} is a series combination of an inductor, L_g, and a resistor, R_g, as long as the frequency of operation is far below the resonance frequency, ω_0. It is desired to reduce series resistance to enhance the quality factor of the inductor, which means using Gm-cells with higher output resistance. Also increasing the resonance frequency for enhancing inductor's frequency of operation requires lowering input capacitance of the Gm-cells.

Considering a more realistic scenario and using Z_{in} of (4.17) in series with a capacitor to create a notch filter as in Fig. 4.5 will add a parasitic pole corresponding to ω_0. When three notch filters are used together, the parasitic pole of each inductor will decrease ω_{P1} and ω_{P2} in Fig. 4.6 and add another pole after ω_{Z3}, which overall has a negligible impact on the notch rejection if the parasitic capacitor of each gyrator in each notch filter (C_i) is sufficiently smaller than the filter capacitor.

Considering the gyrator of Fig. 4.12 with all the parasitics in the BPF topology of Fig. 4.9, it can be seen that the zero of the ideal BPF is increased (from frequency of zero) and the pole is decreased. Lowering switch resistance and using transconductance stages with high output resistor, in the gyrator, will reduce the zero. The effect of the gyrator on the pole is minimized by using transconductance stages with high output resistor and low parasitic capacitors.

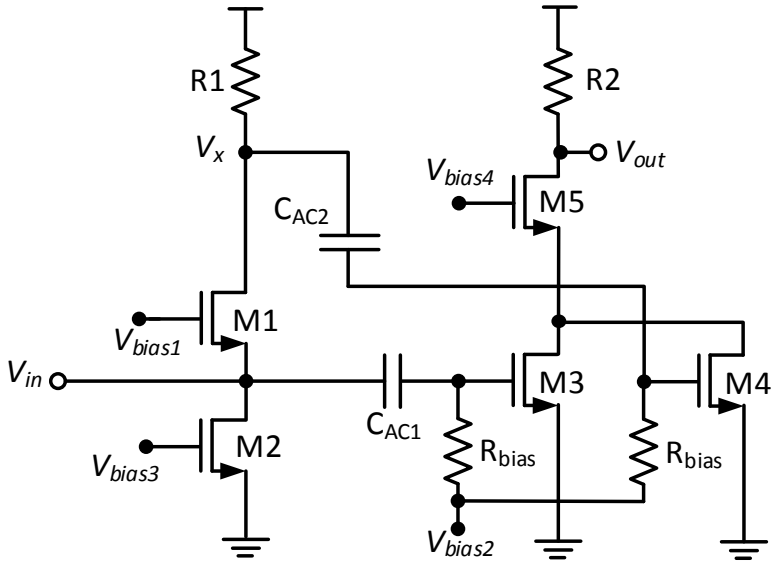


Figure 4.13: UWB LNA used at the beginning of the proposed system.

4.3 Circuit design

4.3.1 LNA

A wideband inductorless LNA, utilizing noise and distortion canceling is employed here [58]. Fig. 4.13 shows the LNA circuit. The input signal paths to the output are through transistors (M3,M5) and (M1,M4,M5), both facing similar polarity resulting an amplified signal at the output. On the other hand, noise of M1 at V_{in} and V_x have opposite polarities, which results in a reduced noise at the output. M1 third order distortion is also reduced in the same way.

There is a trade-off between noise and power consumption. Reducing F_{M1} (noise factor of M1) and F_{R_1} (noise factor of R_1), while maintaining the same input match, reduces NF while increasing current consumption. In order to reach a power efficient noise cancellation, F_{M1} is chosen to be equal to F_{R_1}, as discussed in more details in [58].

The ratio of F_{M1} to F_{R_1} is calculated as

$$\frac{F_{M1}}{F_{R_1}} = \frac{(\gamma/\alpha) g_{m1} R_1 R_T^2}{R_S^2} \delta^2 \tag{4.20}$$

where R_S is the source resistance, γ is the MOSFET noise parameter, $\alpha = g_m/g_{d0}$,

$$R_T = R_S || \frac{r_{o1}}{1 + R_1/R_S} || \frac{1}{g_{m1}} \tag{4.21}$$

and

$$\delta = \frac{R_S}{R_1} \frac{g_{m3}}{g_{m4}} - 1 \tag{4.22}$$

Equating F_{M1} and F_{R_1} results in a δ of -0.526.

From distortion analysis in [58], equations required for third-order distortion cancellation of M3 and M4 are as follows

$$\frac{g_{m3}}{g_{m4}} = \frac{R_1}{R_S} \tag{4.23}$$

$$\frac{g''_{m3}}{g''_{m4}} = \frac{R_1}{R_{in}} \tag{4.24}$$

where g''_{m3} and g''_{m4} are third order non-linearity coefficient of M3 and M4 respectively, and

$$R_{in} = \frac{R_1 + r_{o1}}{1 + g_{m1} r_{o1}} \tag{4.25}$$

Bias and sizing of M3 and M4 are chosen in a way to attain (4.23) and (4.24).

Simulation results show the LNA achieves a voltage gain of 13.4-14 dB, a NF of 3.9 dB, and an IIP3 of -3.3 dBm to -2.8 dBm within 3.1-4.8 GHz band, while drawing 4.4 mA from a 1 V supply. Fig. 4.14 shows the simulated voltage gain and NF of the LNA vs. RF frequency.

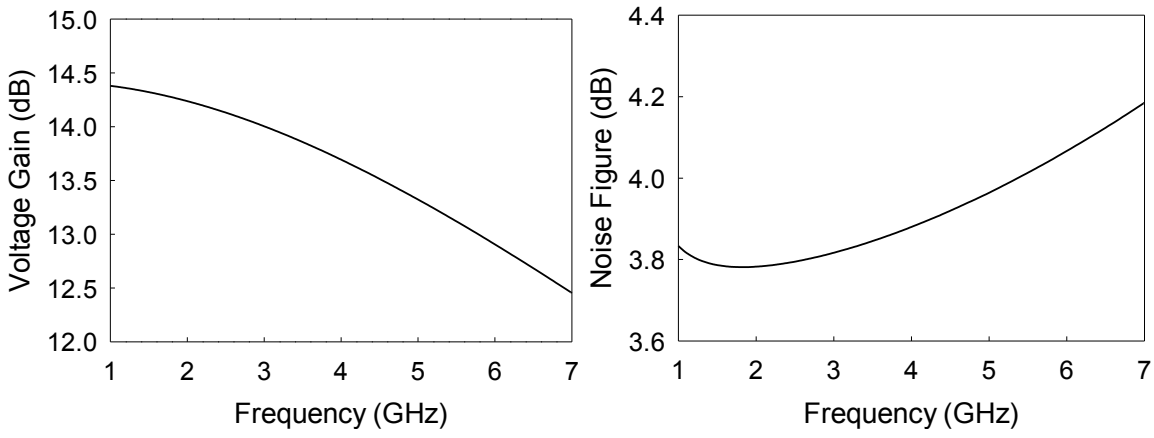


Figure 4.14: Simulated (a) voltage gain, and (b) NF of the UWB LNA.

4.3.2 Notch filters

As mentioned in section 4.2, gyrator-based active inductors are preferred here over passive ones due to the lower area and higher quality factors and are employed in the notch filters of Fig. 4.5.

Fig. 4.15 shows the implementation of each notch filter circuit. The reason of placing the active gyrator in the middle of two series capacitors, C_1 and C_2 in Fig. 4.15 is to avoid using extra decoupling capacitors at the output of G_{m2} for isolating the bias of the transconductors. An inverter-based structure [51] is used for the Gm-cells, consisting of only two nodes (In and Out) and no internal nodes, resulting in lower parasitics and hence higher frequency of operation. This structure also provides a high output resistance for differential gain using inv_{3-6}, providing a high quality factor inductor. To understand this effect, consider the differential load resistance of the inverter-based structure shown

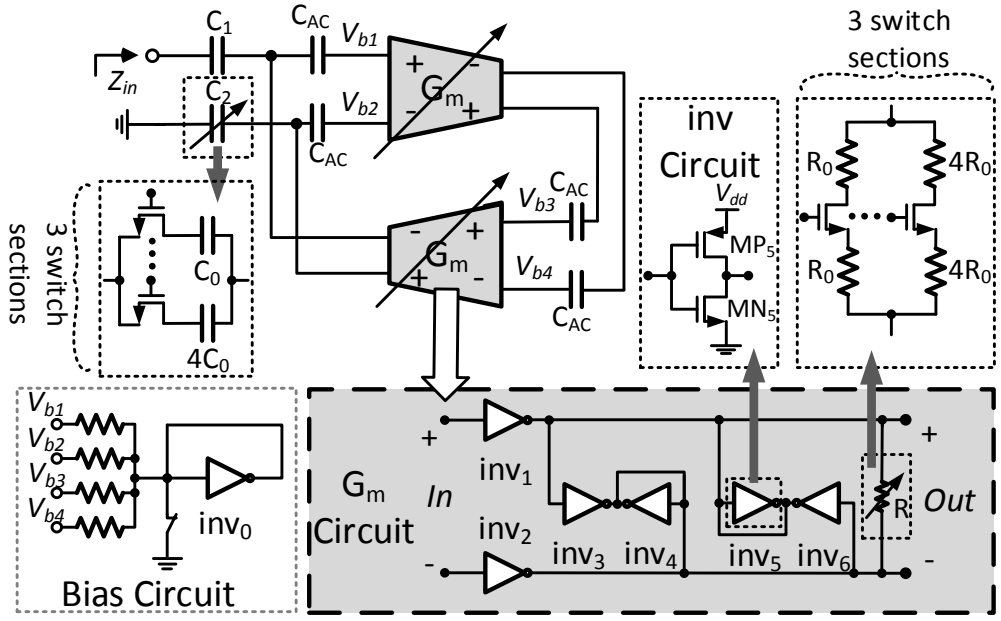


Figure 4.15: Block diagram of each notch filter.

in Fig. 4.15, which is

$$R_d = \frac{1}{\frac{1}{r_{o,inv_{1,2}}} + \frac{1}{r_{o,inv_{3,6}}} + \frac{1}{r_{o,inv_{4,5}}} + g_{m,inv_{4,5}} - g_{m,inv_{3,6}}} \tag{4.26}$$

Choosing $\frac{1}{r_{o,inv_{1,2}}} + \frac{1}{r_{o,inv_{3,6}}} + \frac{1}{r_{o,inv_{4,5}}} = g_{m,inv_{3,6}} - g_{m,inv_{4,5}}$ results in an output resistance of infinity, which in reality is a finite value due to the difference between the actual transconductance and the desired one. For common-mode resistance, $g_{m,inv_{3,6}}$ and $g_{m,inv_{4,5}}$ are added, creating a low common-mode load impedance. For higher differential gain, transconductance of inv_3 and inv_6 are chosen slightly larger than inv_4 and inv_5.

Changing the center frequency of each notch filter in Fig. 4.15 is performed by changing capacitors using three switches. For each specific frequency, the output resistor is tuned by adding a variable resistor at the output load, using three switches, to yield the maximum rejection.

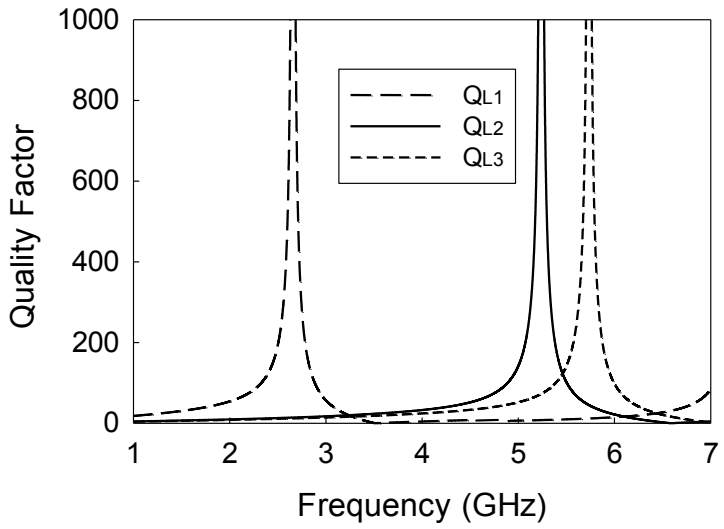
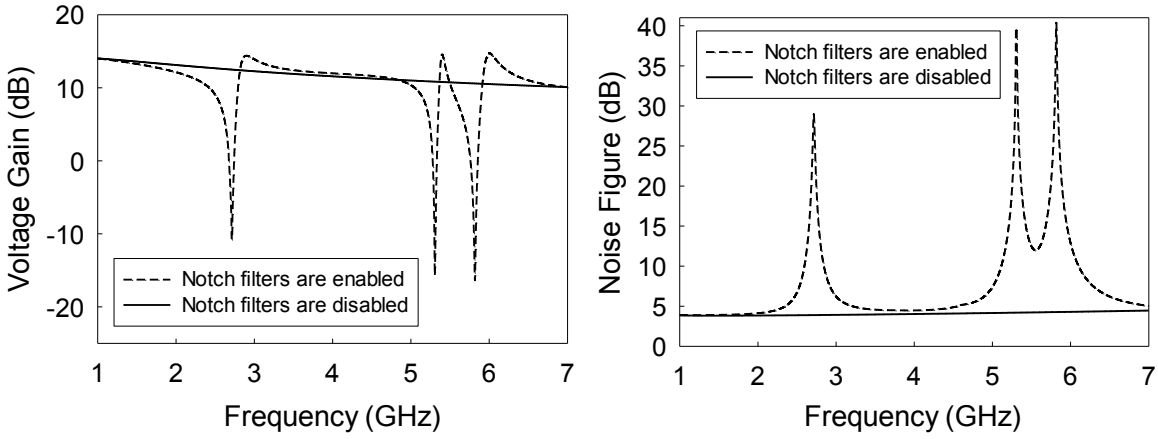


Figure 4.16: Simulated Q of each active inductor.

Fig. 4.16 shows the simulated Q for each active inductor, at a specific setting of switches, Q_{L1}, Q_{L2}, and Q_{L3} are quality factors of the active inductor used in $Notch_1$, $Notch_2$, and $Notch_3$, respectively (see Fig. 4.5). Values of inductor for Q_{L1}, Q_{L2}, and Q_{L3} in Fig. 4.16 are 20 nH, 7.7 nH, and 6.6 nH, respectively.

Fig. 4.17 shows the simulated voltage gain and NF of the LNA when the notch filters are added, for two specific cases; when all of the notch filters are enabled (for one specific set of switches), and when all of them are disabled. As Fig. 4.17 suggests, voltage gain drops to 11.1-12.2 dB within the desired band, when the notch filters are deactivated, due to the added parasitics, and it is 11.2-13.3 dB, when all three filters are activated. The NF however is similar to Fig. 4.14b (3.9 dB), when the notch filters are disabled, and it increases to 4.4-5.5 dB for the desired band, when they are enabled due to the lowered gain at the notch frequencies. IIP3 at 3.5 GHz is -2.3 dBm and -3 dBm, when all notch filters are "off" and "on", respectively. Each notch filter rejection is more than 20 dB and the BW in which each notch filter achieves a 10 dB rejection is 100 MHz. The channel



(a) (b)

Figure 4.17: Simulated (a) voltage gain, and (b) NF of the LNA, when all three notch filters are "on" and "off".

bandwidth of interferers in the proximity of UWB band (802.11b/g, WiMAX, 802.11a, and HiperLAN2) is less than 25 MHz, so the notch is wide enough to adequately attenuate an entire channel. Each Gm-cell for $Notch_1$, $Notch_2$, and $Notch_3$, consumes 0.8 mA, 1.4 mA, and 1.5 mA from a 1 V supply, respectively.

4.3.3 Mixer and BB filters

A single-balanced voltage-mode passive mixer is employed here. The mixer consists of NMOS switches, BB Gm, and TIA. A Tow-Thomas biquad active-RC LPF [50] is used after the TIA for better rejection of undesired terms. Fig. 4.18 shows the mixer along with the BB filter. Again, inverter-based structure is used for the BB Gm and also each OTA. The high DC gain of this structure makes it a good candidate to be used as an OTA as well.

Frequency response of the biquad is calculated to be

$$\frac{V_{out}}{V_{in,b}} = \frac{\frac{1}{R_d R_b C_b C_c}}{s^2 + \frac{1}{R_c C_b} s + \frac{1}{R_d R_e C_b C_c}} \tag{4.27}$$

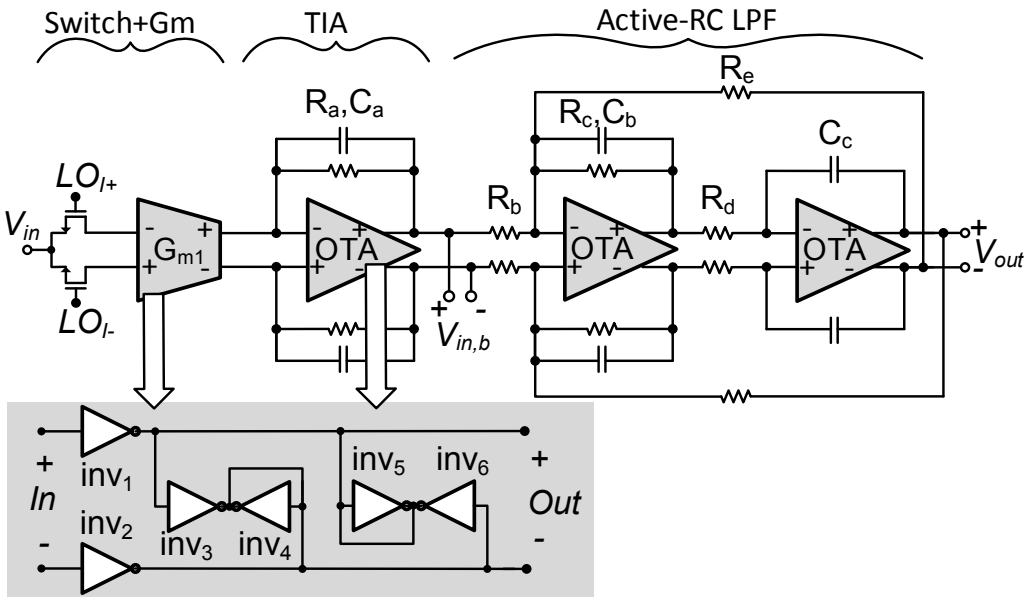
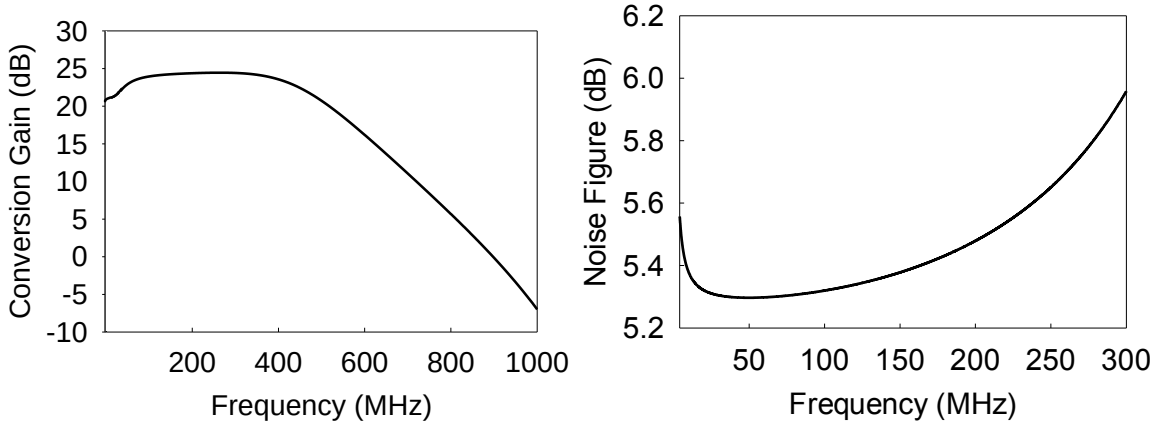


Figure 4.18: Mixer and BB filters.

For simplicity capacitor values are chosen similar ($C_b = C_c = C$) and also $R_d = R_e = R$, which leads to the following equations for ω_0, Q, and DC gain

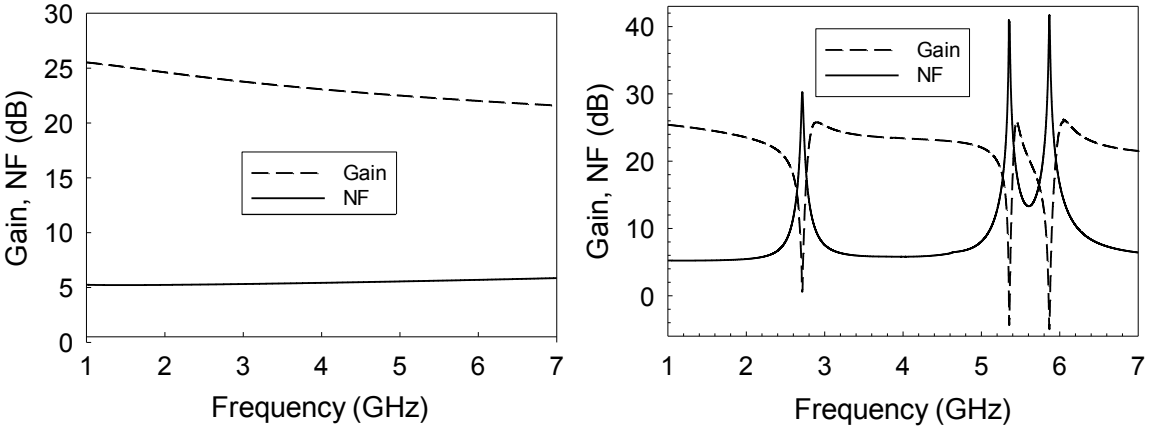
$$\omega_0 = \frac{1}{RC}, Q = \frac{R_c}{R}, G_{DC} = \frac{R}{R_b} \tag{4.28}$$

For a specific ω_0, Gain and Q of the Tow-Thomas biquad is adjusted by varying R_b and R_c, respectively. The BB Gm, TIA, and biquad filter, are cascaded, overall creating a fourth order filter at BB. Fig. 4.19 shows the simulated conversion gain and NF of the entire receiver (LNA, mixer, and BB filter) at the BB, for LO frequency of 3.9 GHz, when the notch filters are deactivated. The IIP3 for LO of 3.9 GHz is -9 dBm. Fig. 4.20 shows the simulated gain and NF of the receiver vs. RF frequency, when the notch filters are "on" (for a specific setting) and "off". G_{m1} and each OTA in Fig. 4.18 consume 2.7 mA and 3.1 mA from a 1 V supply, respectively.



(a) (b)

Figure 4.19: Simulated (a) conversion gain, and (b) NF of the receiver, at the BB, for LO frequency of 3.9 GHz.



(a) (b)

Figure 4.20: Simulated conversion gain and NF of the receiver vs RF frequency, when (a) notch filters are “off”, and (b) notch filters are “on”.

4.3.4 Balun and multiplier

Linearity is a limiting factor in the detection path as the incoming signal can include strong blockers. A linear multiplier requires to be differential and hence a balun is em-

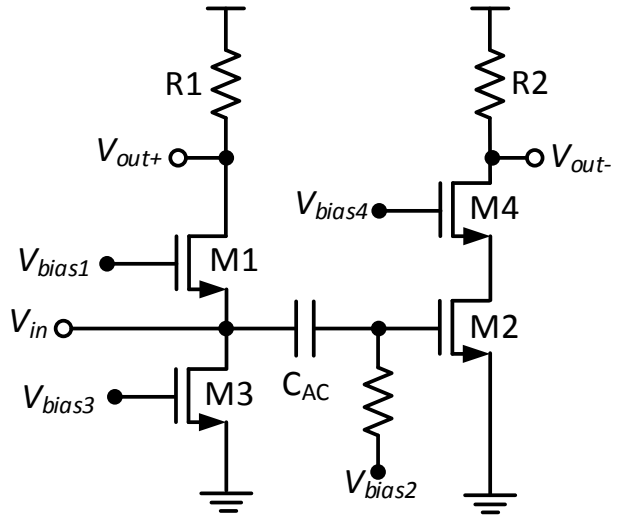


Figure 4.21: Balun LNA used after the UWB LNA in the blocker detection path.

ployed before the multiplier. An active CS-CG noise and distortion canceling balun-LNA [59] is employed due to area limitation (Fig. 4.21). Simulations show a current consumption of 1 mA from a 1 V supply, voltage gain of 6 dB, NF of 8 dB, and IIP3 of 8 dBm for the balun-LNA in the intended frequency band.

A differential four-quadrant multiplier [49] is employed after the balun-LNA (Fig. 4.22), to time limit the signal periodically by multiplying it with a Gaussian pulse train. Transistors $M1-4$ operate in linear region and the multiplication is performed using $V_{gs}V_{ds}$ term in the current equation of $M1-4$. Transistors $M5-8$ should operate as source followers to translate $V_{gs}V_{ds}$ term of $M1-4$ to multiplication of the signals applied to the gates of $M1-4$ and $M5-8$, which necessitates using larger transistor size for $M5-8$ (at least three times of size of $M1-4$ [49]). The multiplier of Fig. 4.22 is capable of a simultaneous good noise and linearity performance [49]. The output of the balun-LNA is applied to the gates of $M1-4$, while the Gaussian pulse train is applied to the gates of $M5-8$, resulting a Gaussian shape periodic signal at the output of the multiplier (see Fig. 4.22). The multiplier adds a 6 dB gain to the signal resulted from the multiplication

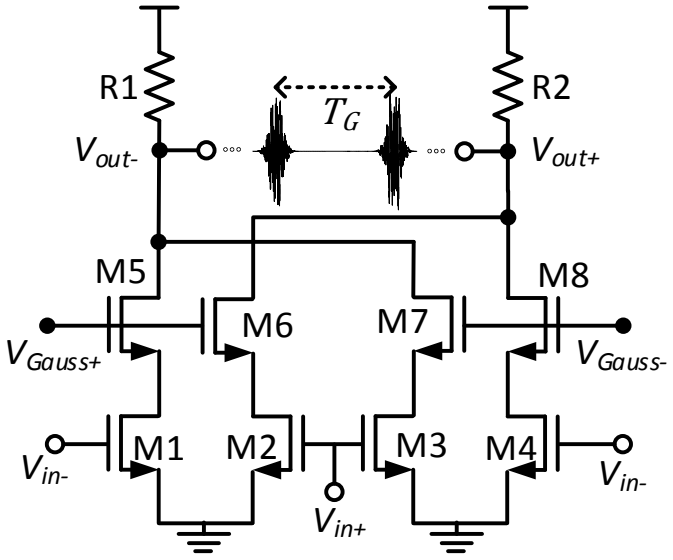


Figure 4.22: Multiplier used for time limiting the incoming signal.

of its inputs and consumes only 0.3 mA from a 1 V supply.

4.3.5 BPFs (phaser)

Phaser is a DDS, which converts the frequency difference in the incoming signal to time difference, discriminating channels in time domain. While it is superior to conventional BB blocker detectors in terms of linearity due to mixer elimination, it is also advantageous for creating separated channels in time domain and hence making an straightforward scenario for decision making.

Fig. 4.23 shows each BPF of the proposed phaser. The phaser consists of tunable LC parallel BPFs (Fig. 4.9). Since tuning for the entire interferer band (2.35-5.9 GHz) is not straightforward using only one BPF, three BPFs are employed to tune the required sub-bands. Each inductor in the BPFs is a differential active gyrator. Note that in Fig. 4.23, using of decoupling capacitors is unavoidable after the switches, S_1 and S_2, to connect the BPF to the output of the multiplier without changing the bias of the gyrator. Similar to the notch filters, for each Gm-cell, inverter-based structure is used (see Fig. 4.23). Tuning is

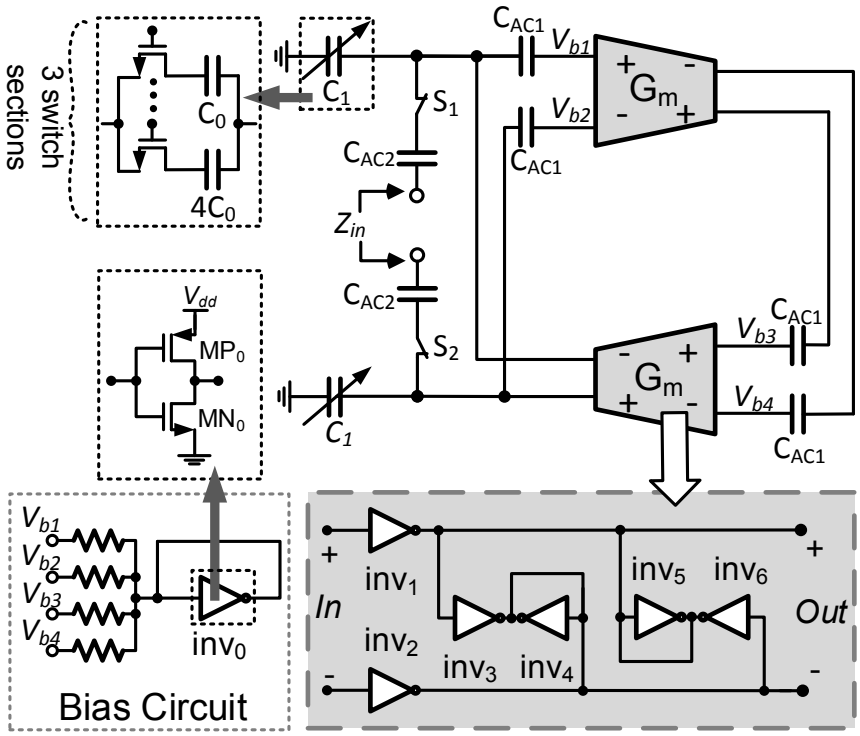
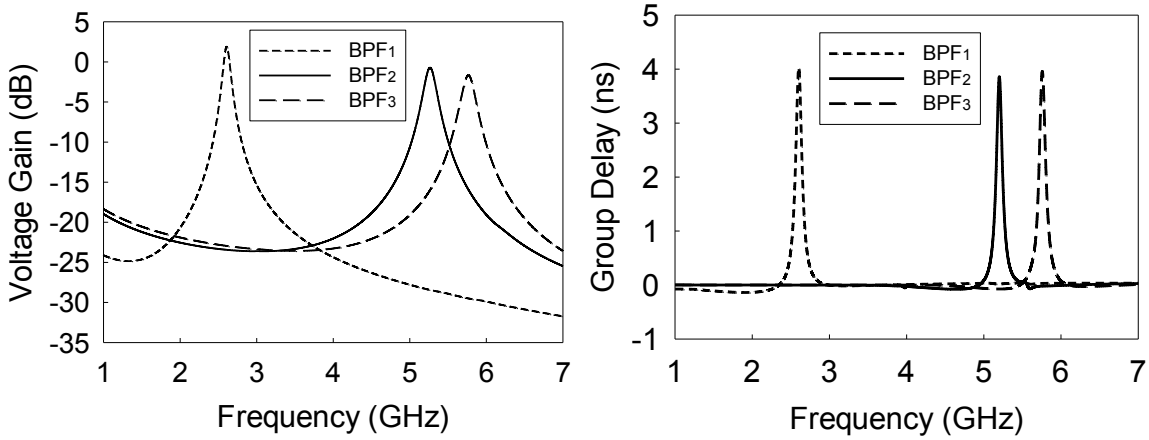


Figure 4.23: Block diagram of each BPF of the phaser.

performed by changing only the capacitors of the filter using three switches for each filter, as it is less sensitive to output resistance variations. Fig. 4.24 shows the voltage gain and GD frequency response of the blocker detector at the output of the phaser for each BPF at a specific calibration setting, when a differential voltage of 200 mV is applied to the gates of M_{5-8} in Fig. 4.22 (500 mV for M_{5-6} and 700 mV for M_{7-8}). Here, the reason of choosing the constant differential voltage of 200 mV for the gate of $M_5 - M_8$ is to obtain the voltage gain of the blocker detector, while $M_5 - M_8$ stay in saturation. Each Gm-cell in BPF_1, BPF_2 and BPF_3 draws 0.8 mA, 2 mA and 2.1 mA from a 1 V supply, respectively.

Fig. 4.25 shows the output of the phaser, when the center frequency is set to 2.6 GHz, for two cases, two tones each with the power of -20 dBm are at 2.6 GHz and 2.7 GHz



(a) (b)

Figure 4.24: Simulated (a) magnitude, and (b) GD frequency response of the blocker detector at the output of the phaser for each BPF, when a differential voltage of 200 mV is applied to the gates of $M_5 - M_8$ in Fig. 4.22.

(signal exists at the intended frequency of 2.6 GHz), and one tone with the power of -20 dBm is at 2.7 GHz (signal doesn't exist at the intended frequency of 2.6 GHz). Gaussian pulse amplitude is chosen to be 200 mV. The former shows an unattenuated, time shifted signal at the output of the phaser, corresponding to the frequency of 2.6 GHz, while the latter shows an attenuated signal at the output of the phaser, which is not shifted in time domain with respect to the input of the phaser, because the input has no component at the current center frequency of the phaser (2.6 GHz). For Fig. 4.25, σ of the Gaussian pulse is 0.8 ns. Note that in the automatic mode of the phaser, when the center frequency of the phaser changes with a frequency step of 100 MHz, BW of the Gaussian pulse should be less than the frequency step [20]. BW of a Gaussian pulse is

$$\Delta f_G = \frac{1}{2\pi\sqrt{2}\sigma} \tag{4.29}$$

which requires a σ of greater than 1.1 ns. Estimating the Gaussian pulse duration, T, as

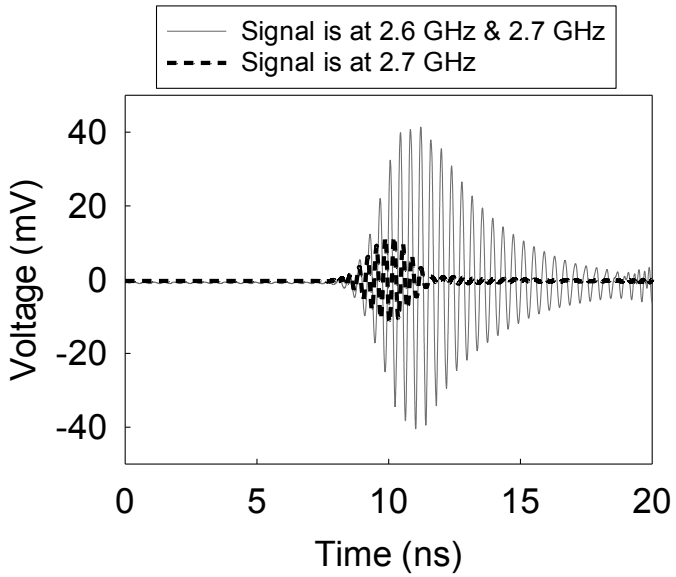


Figure 4.25: Transient output of the phaser with center frequency of 2.6 GHz, when the signal is at 2.6 GHz and 2.7 GHz, and only at 2.7 GHz (power of each tone is -20 dBm and Gaussian pulse amplitude is 200 mV).

6σ, results in a T of greater than 6.6 ns. Following conditions are mentioned in [20] for better channel discrimination in time domain

$$GD > T/2, \;\; T_G > T + GD \tag{4.30}$$

which T is the Gaussian pulse duration and T_G is the period of the Gaussian pulse train. Equation (4.30) shows that a GD of greater than 3.3 ns is required for better channel separation.

4.3.6 Decision circuits

In this section, the operation of the digital control circuit is explained. After the phaser, an active balun and a diode-RC envelope detector is placed to take the envelope of the signal (Fig. 4.26). Transistor $M8$ is biased in weak inversion region to act as a diode. The balun with envelope detector only consume 0.11 mA from a 1 V supply. The transient

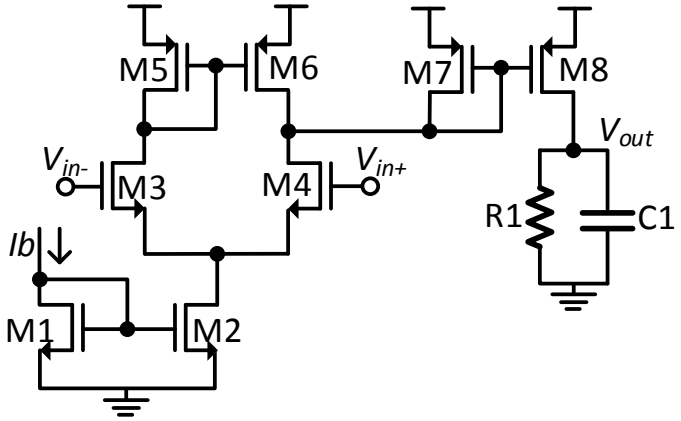


Figure 4.26: Balun and envelope detector.

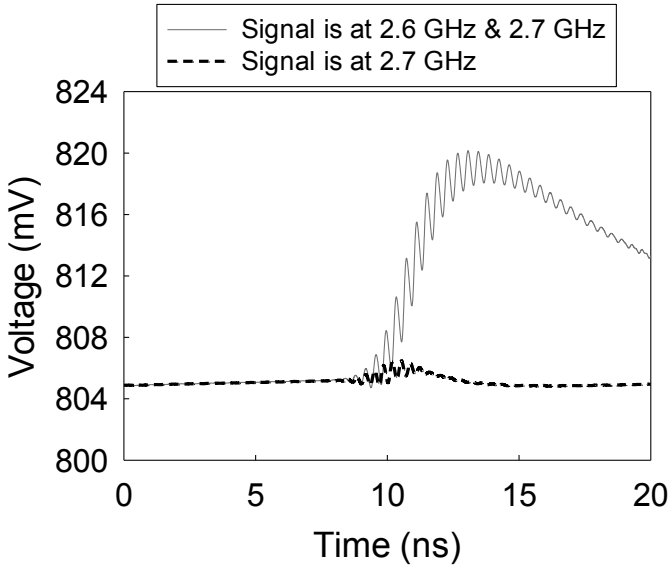


Figure 4.27: Transient output of the envelope detector with phaser center frequency of 2.6 GHz, when the signal is at 2.6 GHz and 2.7 GHz, and only at 2.7 GHz (power of each tone is -20 dBm and Gaussian pulse amplitude is 200 mV).

output of the envelope detector for the signals shown in Fig. 4.25 is shown in Fig. 4.27.

Fig. 4.28 shows the block diagram of the digital control circuit. Before the normal operation of the system both notch filters, in the receiver, and BPFs, in the detector, are

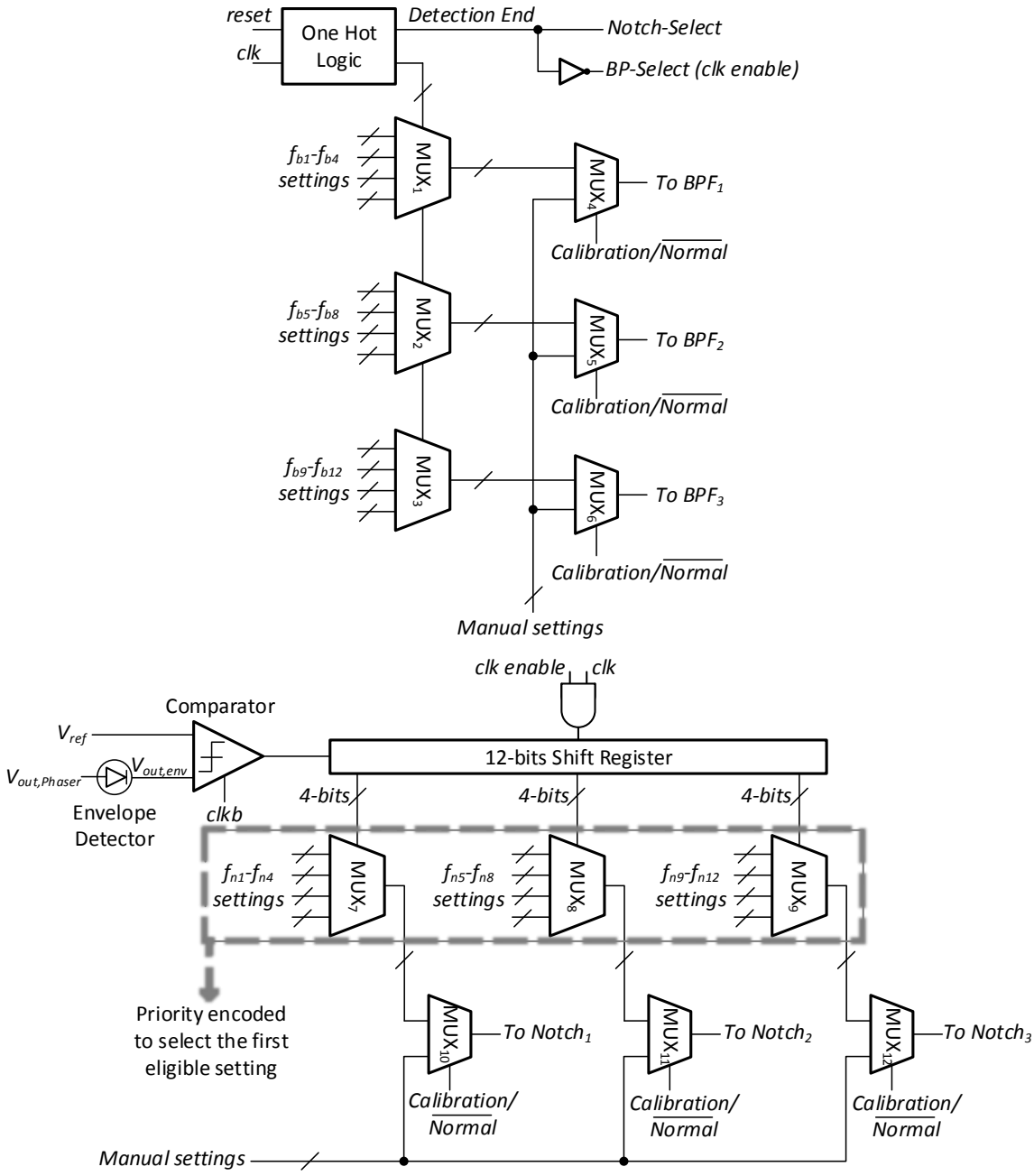


Figure 4.28: block diagram of the digital control circuit.

calibrated manually. First, the BPFs of the phaser are calibrated manually in the detection path using three switches for each BPF (see Fig. 4.23); from each BPF, four desired set-

tings are selected, determining an overall of twelve desired settings. The desired settings should result in a separation of 100 MHz between each two consecutive states for each sub-band. After calibration, the BPFs are selected automatically using "one hot logic" and $MUX_1 - MUX_3$; first BPF_1 is enabled, while BPF_2 and BPF_3 are disabled, and its center frequency varied from 2.4 GHz to 2.7 GHz ($f_{b1} - f_{b4}$ settings), then, BPF_2 is activated and varied with $f_{b5} - f_{b8}$ settings (center frequency of 5.15 GHz to 5.45 GHz), while the other two are deactivated, and finally the BPF_3 is activated, while the other two are disconnected ($f_{b9} - f_{b12}$ settings corresponding to center frequency of 5.55 GHz to 5.85 GHz). $MUX_4 - MUX_6$ determine the normal or calibrated mode of the BPFs. The output of the envelope detector, which is placed after the phaser, ($V_{out,env}$) is compared with a reference voltage (V_{ref}), using a dynamic comparator [60]. The comparator operates with a clock signal $clkb$, with a period of T_G, similar to the period of the Gaussian pulse train. Since notch filters operate in parallel, the twelve serial bits corresponding to a maximum of three interferes (one for each BPF) are placed in parallel using a 12-bits shift register. After the detection process is finished, the $Detection\ End$ signal turns from "0" to "1" and the detection path is disconnected from the LNA and the receiving path is activated. For each of the BPFs of the phaser, the first setting which results in a "1" at the output of the comparator is selected and mapped to the corresponding setting of the notch filters with the same frequency (one of f_{n1} to f_{n12} which is specified in calibration mode) using priority encoded MUXs, $MUX_7 - MUX_9$. Note that if there is no interferer in any of the sub-bands, the corresponding notch filter is deactivated. $MUX_{10} - MUX_{12}$ determine the calibration or normal operation of the notch filters. The entire detector works periodically (with a period of T_G) and in each period one interferer is discriminated. The detecting and receiving times are controlled using a reset signal. The order of system functionality is summarized as follows:

- Calibrate notch and BPFs
- Set states of switches for each frequency through scan chain (for both notch and BPFs)
- Automatic tuning of the BPFs and finding the first blockers in each sub-band using a state machine
- Automatic state mapping for selection of up to three notch filters
- Normal operation of the receiver with the selected notch filters

4.4 Fabrication and measurement

The proposed UWB receiver with blocker detection is fabricated using TSMC 65-nm CMOS technology. The overall area (including pads) is 1 mm^2 and the maximum power consumption for detecting and receiving modes are 9.6 mW and 23.8 mW, respectively. Fig. 4.29 shows the fabricated IC microphotograph.

The first step in measurement is calibration of BP and notch filters. To calibrate the BPFs, the receiving path is disabled and the detection path is enabled. For each BPF calibration the other two are deactivated. Fig. 4.30 shows the measured voltage gain and GD frequency response of the blocker detector at the output of the differential to single-ended balun placed after the phaser, for each BPF at a specific calibration setting, when a differential voltage of 200 mV is applied to the gates of M_{5-8} in Fig. 4.22 (500 mV for M_{5-6} and 700 mV for M_{7-8}). An open drain buffer is used at the output of the balun for measurement and its effect, which is only on gain, is subtracted in Fig. 4.30.

Next, the detection path is deactivated and the receiver path is activated for manual calibration of the notch filters to reach to the desired settings. Fig. 4.31 shows the measured voltage gain at the output of the LNA, when the three notch filters are all “on” or “off”,

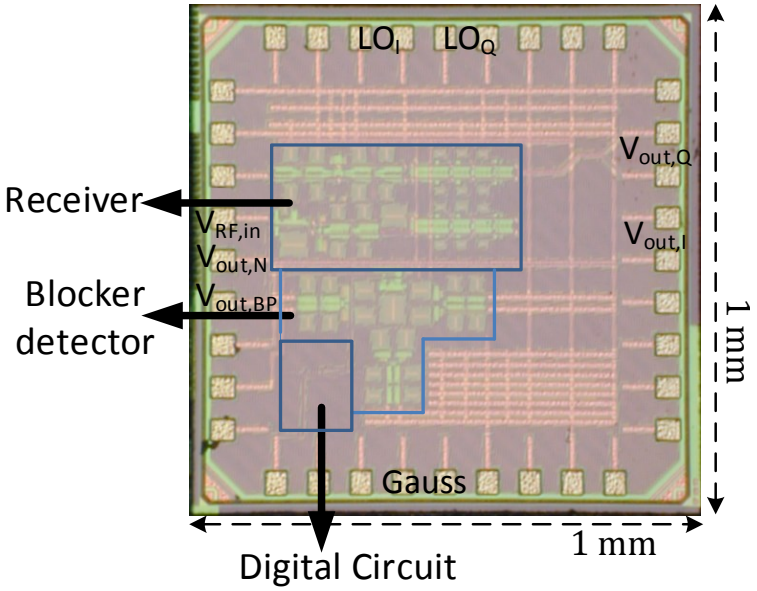


Figure 4.29: Die micrograph of the fabricated UWB receiver with blocker detection.

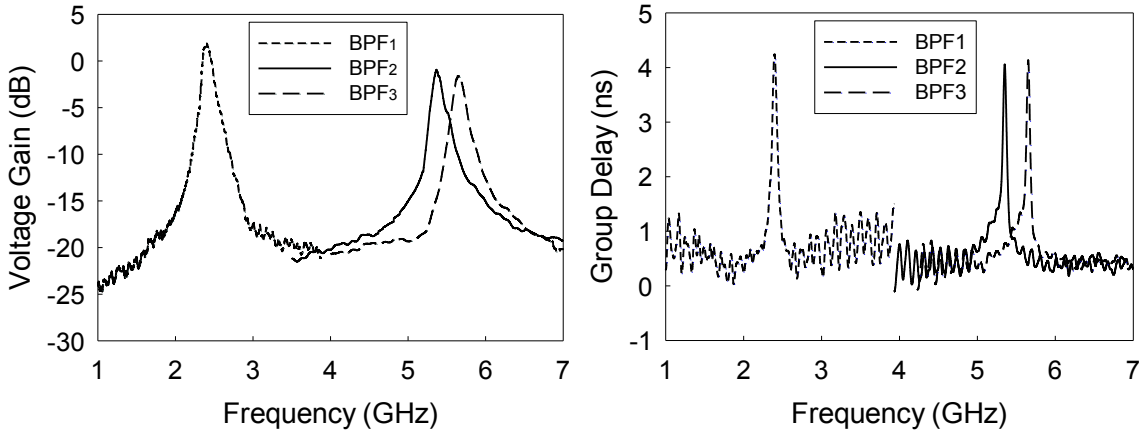


Figure 4.30: Measured (a) magnitude, and (b) GD frequency response of the blocker detector at the output of the differential to single-ended balun for each BPF, when a differential voltage of 200 mV is applied to the gates of M_{5-8} in Fig. 4.22.

for a specific setting, which is very close to simulation results in Fig. 4.17. Again, an open drain buffer is used at the output of the LNA and its effect is subtracted in Fig. 4.31.

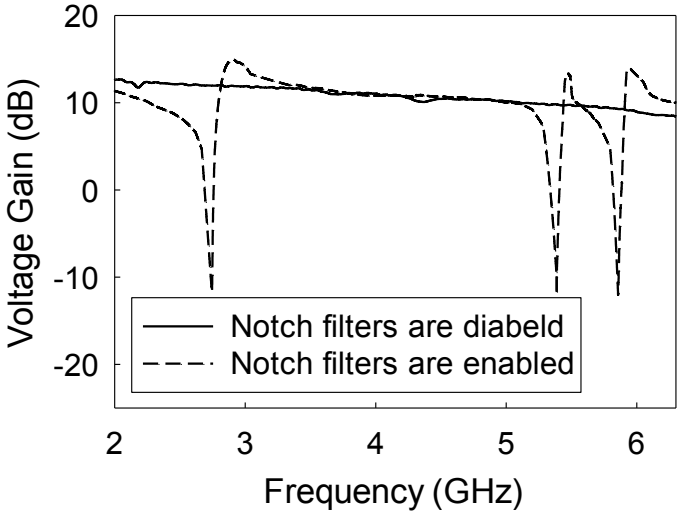


Figure 4.31: Measured voltage gain of the LNA when all three notch filters are "on" or "off".

After the calibration process, the normal operation begins; first the blocker detector is activated and the locations of the interferers are determined and mapped to the notch filters of the receiver. Then the receiver is activated and operates normally and rejects the blockers using notch filters, while the blocker detector is deactivated. Fig. 4.32 shows the comparator output for two scenarios; one, the blockers (sinusoid tones) exist at 2.4 GHz, 2.6 GHz and 2.7 GHz (not at 2.5 GHz), and two, the blockers exist at 5.45 GHz and 5.55 GHz (not at 5.35 GHz and 5.65 GHz), each with a power of -20 dBm (Gaussian pulse amplitude is 200 mV). For Fig. 4.32, σ is chosen to be 1.2 ns and T_G is 100 ns, which results in a sensing time of 1.2 μs for the twelve channels. Based on GD values (see Fig. 4.30b) and T and T_G selections, (4.30) is met.

Measured voltage conversion gain, NF, in-band IIP3, and S11 of the receiver are shown in Fig. 4.33. For Fig. 4.33a and Fig. 4.33c, all notch filters are "off", while Fig. 4.33b shows the gain and NF for a specific case when all three notch filters are "on". Fig. 4.33c shows conversion gain, NF, and IIP3 in BB for LO frequency 3.9 GHz.

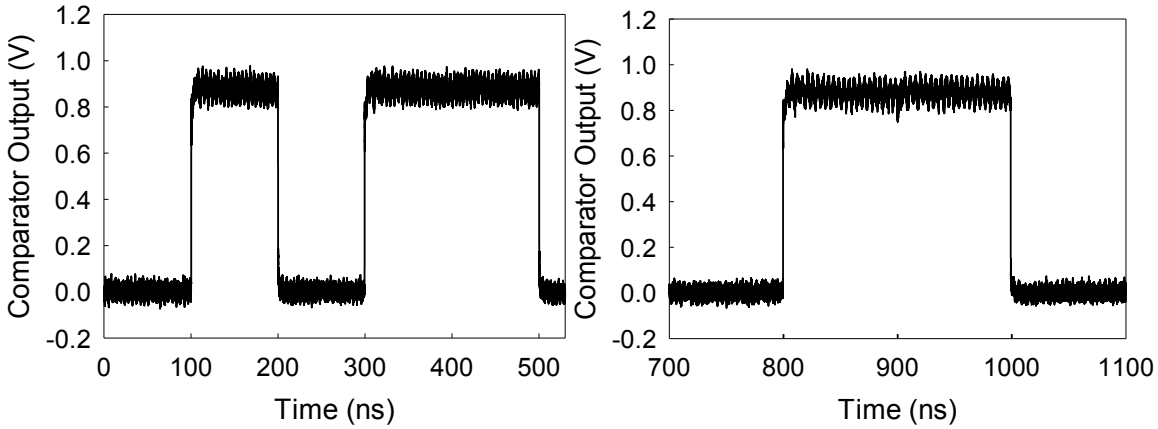


Figure 4.32: Measured comparator output evaluating the signal presence at (a) 2.35-2.75 GHz, and (b) 5.3-5.7 GHz.

For OB-IIP3 and OB-IIP2 measurements, all the cases in Table 1.1 and 1.2 including the ones with no improvement, plus some non-extreme cases are examined. So the measurement is based on the frequencies and powers mentioned in Table 1.1 and 1.2. In Fig. 4.34a (Fig. 4.34b) all pairs of interferers, which create an IM3 (IM2) product within the first UWB group, and their corresponding IIP3 (IIP2) is demonstrated, when the notch filters are both activated an deactivated. Power of 802.11a interferers, which is not mentioned in Table 1.1 and 1.2, is -24 dBm. The improved OB-IIP3/OB-IIP2 values in Fig. 4.34 are higher than the required values in Table 1.1 and 1.2. As shown in Fig. 4.34, an improvement of up to 21.7 dBm for OB-IIP3 (-2.84 dBm to 18.9 dBm for 802.11a and 802.11a) and 36.1 dBm for OB-IIP2 (8.41 dBm to 44.53 dBm for 802.11b/g and 802.11b/g) is feasible using the proposed architecture.

Table 4.1 shows the performance summary of this work and most recent state-of-the-art MB-OFDM UWB receivers. The proposed receiver excels in terms of OB-IIP3 and OB-IIP2 performance and achieves a good power consumption and acceptable NF and

Parameter	This work	[31]	[61]	[62]	[63]
System	RFE+LPF	RFE	RFE+LPF +VGA	RFE	RFE
Frequency (GHz)	3.1−4.8	3.1−4.8	3.1−10.6	3.1−10.6	0.6−10
Gain (dB)	23.2	25	73.5	20.6	14
NF_{min} (dB)	$5.5^{a}/6^{b}$	5.1	8.4	3	7
$IIP3_{avg}$ (dBm)	-9.1	1-dB CP:-30	1-dB CP:-36.8	-9.6	0
OB-IIP3 (dBm)	$2.5-18.9^{c}$	$-4.7-1.6^{d}$	-	-	-
OB-IIP2 (dBm)	$22.6-46^{e}$	$6.2-20.4^{f}$	-	-	-
Power Diss (mW)	$16.4^{g}/23.8^{h}$	32	88.74	10.8	90
area (mm^2)	1^{i}	2.25^{j}	3.23	0.91	1
CMOS Tech	65 nm	130 nm	180 nm	65 nm	45 nm

Table 4.1: Performance Summary and Comparison of the UWB Receiver with Previously Reported Receivers

[a,g] When notch filter(s) are "off".

[b,h] When notch filter(s) are "on".

[c,d,e,f] After improvement by notch filter(s).

[i,j] Area is for the entire system including the detection circuits.

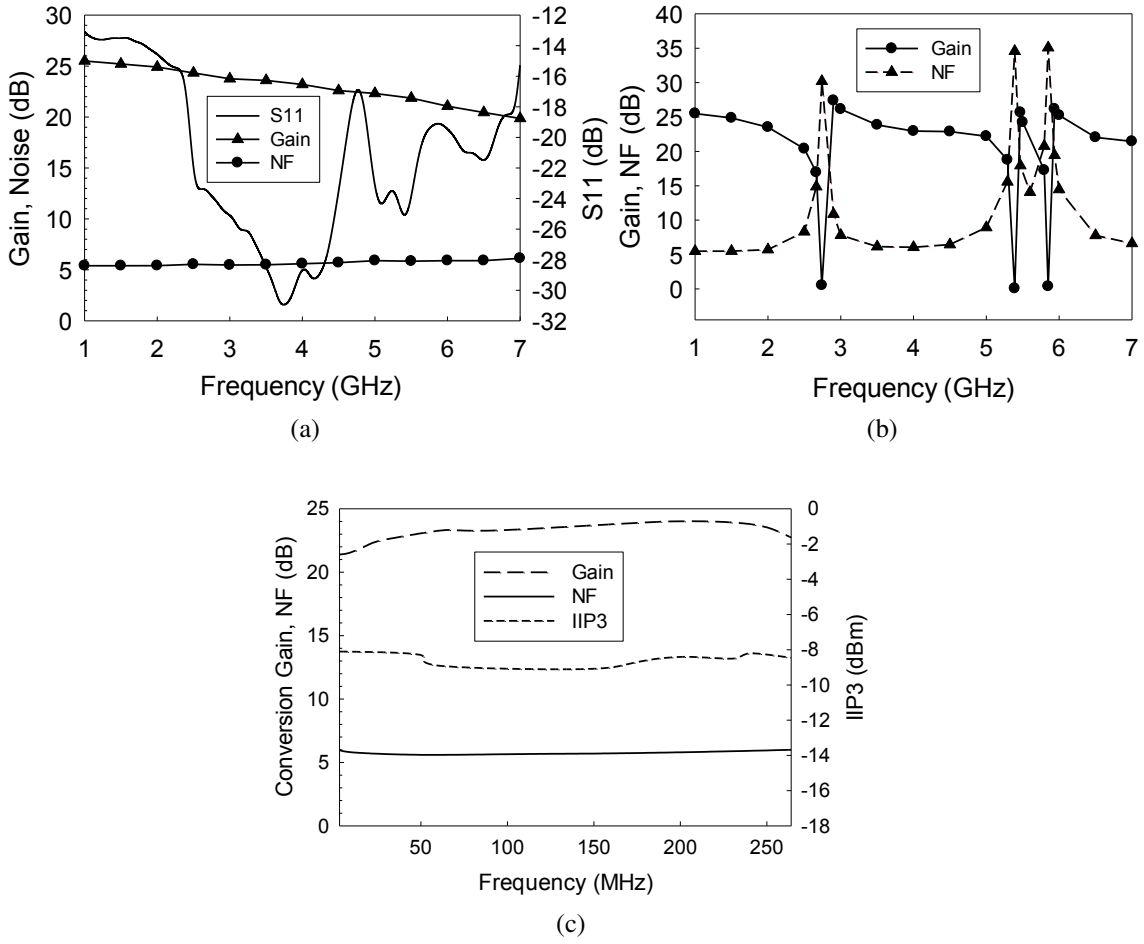


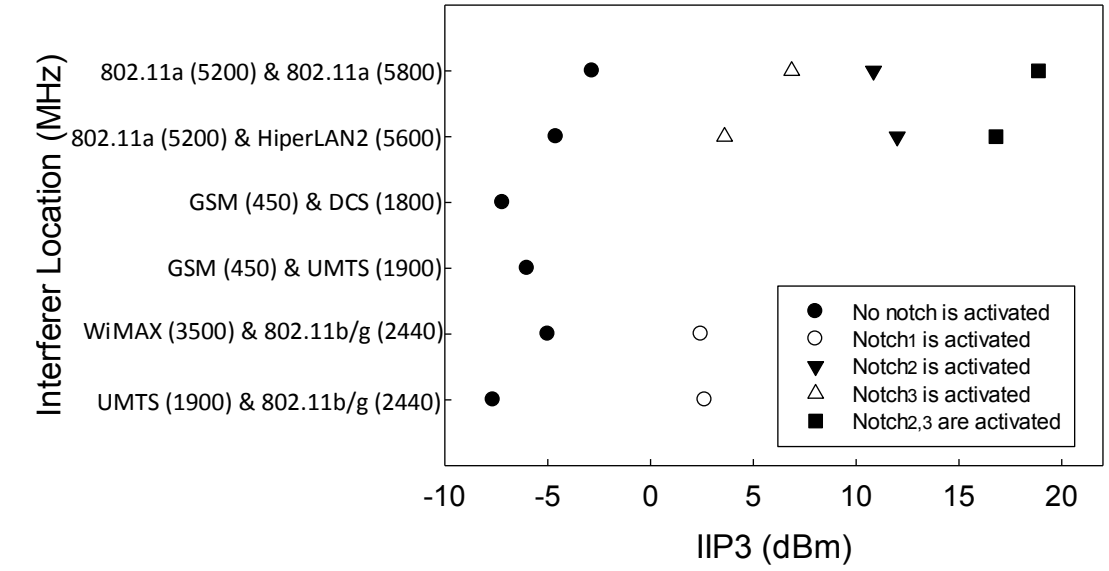
Figure 4.33: Measured (a) voltage conversion gain, NF, and S11 vs. RF frequency, when notch filters are "off", (b) voltage conversion gain, and NF vs. RF frequency, when notch filters are "on", and (c) voltage conversion gain, NF, and in-band IIP3 vs. BB frequency for LO frequency of 3.9 GHz, when notch filters are "off".

IIP3.

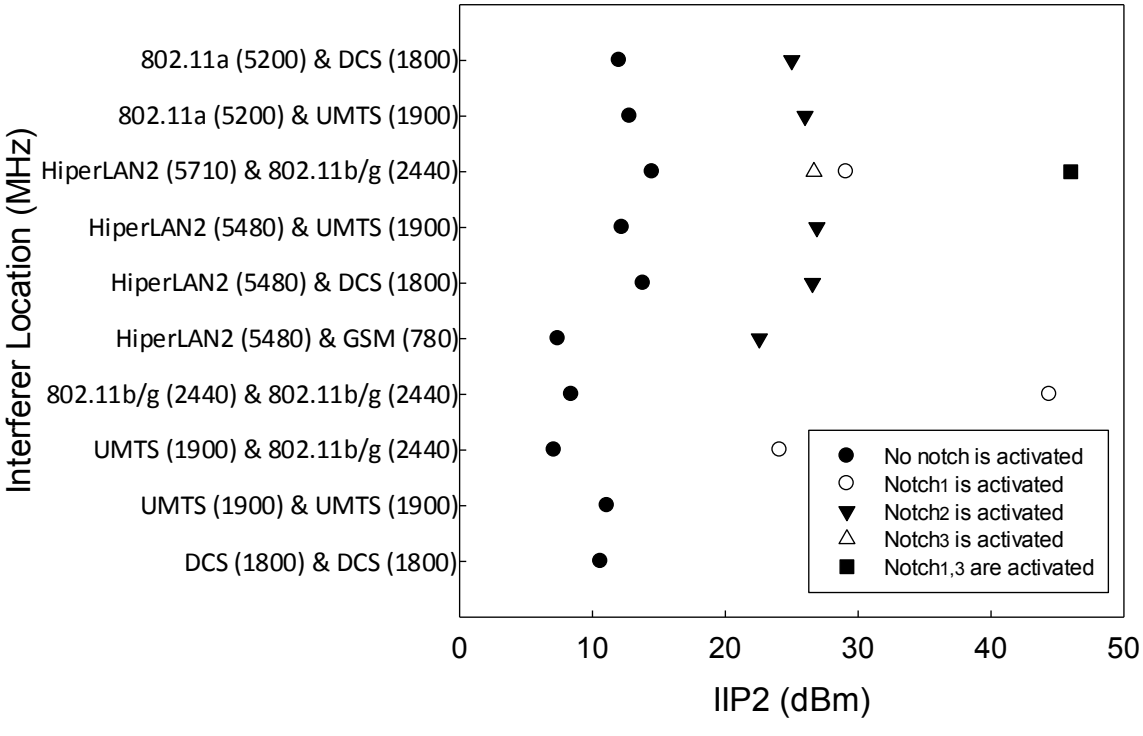
4.5 Conclusion

A UWB receiver for the first UWB group, featuring a phaser-based blocker detection has been described and fabricated in a TSMC CMOS 65-nm technology. The receiver achieves a maximum OB-IIP3 (OB-IIP2) of 18.9 dBm (46 dBm) with blocker rejection

using three tunable notch filters in the receiving path, each corresponding to 2.35-2.75 GHz, 5.1-5.5 GHz, and 5.5-5.9 GHz bands. The receiver meets the challenging OB-IIP3 and OB-IIP2 specs corresponding to the blockers located in the frequencies of the notch filters and draws 23.8 mA (16.4 mA) from a 1 V supply when the three notch filters are activated (deactivated). The phaser-based real-time blocker detector discriminates blockers located in the mentioned bands, in time domain, with a frequency resolution of 100 MHz and consumes only 9.6 mW at its worst case.



(a)



(b)

Figure 4.34: Measured (a) OB-IIP3, and (b) OB-IIP2 of different pairs of UWB blockers, which their IM3/IM2 falls within the first UWB group, when the notch filters are “on” and “off”.

5. SUMMARY AND CONCLUSIONS*

Several methods and applications of spectrum sensing are evaluated. Sections 1.1 and 1.2 provided a through background on different spectrum sensing methods for CR and UWB applications, while Section 1.3 evaluated different reported approaches for UWB receivers to overcome the NB blockers working in the proximity of the UWB devices.

As explained in Chapter 2, sensitivity and sensing time are the key features for an spectrum sensor in a CR device, which detects white space within VHF/UHF TV broadcast bands. The CR device works as a secondary user in the detected empty bands. In Chapter 2 an integrated CMOS CR spectrum sensor for a CR receiver in 54-862 MHz band is presented. A QCF detector is proposed based on both energy and feature detection methods and can take advantage of both methods to reach a fast and accurate decision without the need for an ADC for decision making. The integrated chip has been fabricated in a standard 0.18-μm CMOS IBM technology and has achieved minimum detection SNR of as low as -24 dB and DR of 39 dB. This work is published in [13].

Real-time spectrum sensing refers to searching for possible signals at a specific time and location, which is applicable to CR for primary signal detection and UWB for interferer detection. The simplicity and low sensing time of phaser-based spectrum sensors, implemented in a discrete manner previously, provided the incentive of the proposed spectrum sensor. In Chapter 3, an integrated CMOS wideband real-time spectrum sensor with a novel on-chip phaser in 57-354 MHz band, as part of VHF/UHF TV broadcast bands, is presented. The proposed approach provides a fast, simple, area efficient, analog solution for real-time spectrum sensing with low NF and power consumption. The integrated chip

*

has been fabricated in a standard 0.18-μm CMOS IBM technology and has achieved a sensing time of as low as 2.5 μs for 27 MHz frequency resolution. This work is published in [20].

In Chapter 4, an interferer-tolerant receiver for the first group of UWB (3.1-4.8 GHz) is presented. The entire system operates in two modes; detecting and receiving. In the detecting mode the interferers pass through an LNA, a multiplier, a phaser, and a decision circuit, while in the receiving mode the signal passes through the LNA, three tunable notch filters, a mixer (consisting of a switch, a BB transconductance stage, and a TIA), and a BB filter. The blocker detector detects the location of blockers and reports them to the notch filters of the receiver for rejection. The entire system is integrated in a standard TSMC CMOS 65-nm technology and consumes up to 23.8 mW and 9.6 mW, in the receiving and detecting modes, respectively, with a 1 V voltage supply. The receiver achieves a simultaneous rejection of up to three out-of-band interferers and maximum out-of-band IIP3 and out-of-band IIP2 of 18.9 dBm and 46 dBm, respectively, using a dynamic blocker detection and rejection technique. This work has been accepted for publication in [33].

5.1 Future Work

The simplicity and functionality of CMOS phaser-based spectrum sensors, which are employed in [20] and [33], for signal and interferer detection, respectively, can extend to other applications. One of the applications can be in chirp-UWB receivers to simplify the receiving process.

5.1.1 Phaser-based chirp-UWB receivers

Low data-rate impulse radio ultra-wideband (IR-UWB) transceivers [64] achieve low power consumption, but suffer from the bit-level synchronization problem at the BB. Moreover, they exhibit a high peak transmission power to maintain a sufficient average transmission power for a given link margin. Constant-envelope frequency modulated ultra-

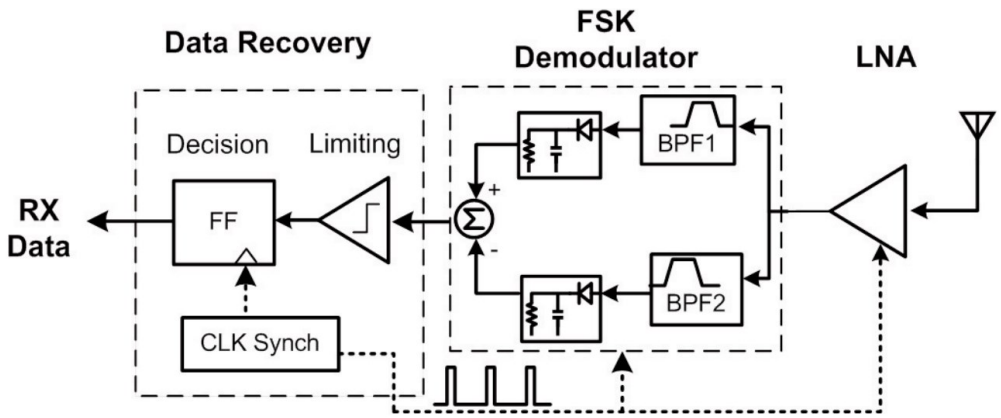


Figure 5.1: Conventional FSK-based chirp-UWB receivers.*

wideband (FM-UWB) systems [65, 66] feature a low peak voltage and a steep roll-off spectrum, but they suffer from high power consumption due to the lack of duty-cycled operation. On the other hand, frequency-shift keying-based (FSK-based) chirp-UWB transceivers [67] significantly reduce the peak transmission power with relaxed duty-cycled operation for noninvasive, energy-efficient, and fast short-range communications.

Fig. 5.1 shows the chirp-UWB receiver front-end architecture in [67]. The modulation is a 2-FSK; "1" corresponds to 8-8.25 GHz and "0" corresponds to 7.75-8 GHz. The FSK demodulator consists of two BPFs, two envelope detectors and a comparator. The upper-band BPF has a center frequency of 8.3 GHz, and the lower-band BPF has a center frequency of 7.7 GHz. The gain difference of 13 dB between the two BPFs at the high end of 8.25 GHz and at the low end of 7.75 GHz is obtained. The envelope difference between the BPFs is extracted by the envelope detectors whose output is sampled by the data slicer with the synchronized data clock. *

As mentioned before a phaser is a DDS structure with a specific GD characteristic. A phaser with an all-pass magnitude and a linear GD can easily act as an FSK demodulator, simplifying the entire procedure. Previously it was mentioned on-chip APFs cannot be

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used as phasers for signal and interferer detection for CR and UWB applications due to required resolutions. Here, a 2-FSK demodulator for a chirp-UWB signal, requires a lousy frequency resolution of 600 MHz, which is possible using on-chip APFs. It means a simple CMOS APF which has a linear GD within the required frequency can act as a phaser and a 2-FSK demodulator for a chirp-UWB signal.

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