Resistive Switching Device Technology Based on Silicon Oxide for Improved ON–OFF Ratio—Part II: Select Devices

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Abstract—**The cross-point architecture for memory arrays is widely considered as one of the most attractive solutions for storage and memory circuits thanks to simplicity, scalability, small cell size, and consequently high density and low cost. Cost-scalable vertical 3-D cross-point architectures, in particular, offer the opportunity to challenge Flash memory with comparable density and cost. To develop scalable cross-point arrays, however, select devices with sufficient ON–OFF ratio, current capability, and endurance must be available. This paper presents a select device technology based on volatile resistive switching with Cu and Ag top electrode and silicon oxide (SiO_x) switching materials. The select device displays ultrahigh resistance window and good current capability exceeding 2 $MAcm^{-2}$. Retention study shows a stochastic voltage-dependent ON–OFF transition time in the 10 μs–1 ms range, which needs to be further optimized for fast memory operation in storage class memory arrays.**

Index Terms—**Conductive bridge RAM (CBRAM), cross-point array, select device, silicon oxide, storage class memory, volatile switching.**

I. INTRODUCTION

CROSS-POINT arrays represent a promising architecture to compete with Flash memories in terms of density and bit cost. In a cross-point array, every memory element is located at the intersection between a row and a column electrode wire, therefore achieving a minimum device size of $4F^2$, where F is the minimum lithographic feature. Cross-point arrays were proposed for resistive switching (RS) memory (RRAM) [1]–[3] and phase change memory (PCM) [4], [5], both benefitting from a relatively large resistance window and

a scalable device size. Similar to Flash memory, 3-D versions of the cross-point architectures have been proposed adopting either horizontal stacking [3], [5], [6] or vertical concepts [7]–[9]. For these reasons, cross-point arrays have scalable bit cost that is required to develop storage class memories with density comparable to Flash [10].

Due to the dense crisscross structure of a cross-point circuit, read and programming operations inevitably lead to disturb effects, such as voltage disturb or sneak paths [1], [3], [11]. In the latter, application of a read/program voltage across a selected memory cell also results in unintended current contributions from half-selected cells, which share either the same row or the same column as the selected device. To mitigate those sneakpaths, each memory element must be accompanied by a select device with high nonlinear characteristic. Due to voltage division across the memory and select elements, most of the applied voltage drops across the high-resistance select device, thus inhibiting the sneak-path leakage.

To minimize sneak-path effects and maximize the available array size, the select device should display a very high ON–OFF ratio, usually estimated as the ratio of the current at the operational voltage (V) and at the half voltage (V/2). The select element should also show sufficiently large current $I(V)$ to enable set/reset operations of the memory element [3], [12], while its endurance and bandwidth should be compatible with the memory element. Also, select devices should be fabricated in the back end of line (BEOL) to enable 3-D stackable or vertical crossbar arrays [13]. To satisfy these multiple requirements, several types of select elements have been proposed, including oxide-based p-n diodes [1], [3], mixed ionic-electronic conduction devices [14], oxide-based tunnel diodes [15], insulator–metal transition layers [2], [16], chalcogenide-based threshold switching devices [5], [17], and threshold vacuum switches [18].

Most recently, novel select devices based on volatile conductive bridge RAM (CBRAM) were demonstrated with both Cu and Ag top electrode (TE) materials. CBRAM with a Cu/SiO_x structure displays both unipolar and bipolar switching [19], evidencing the capability of ultralow current operation ($I_C = 10$ pA) [20]. Most recently, volatile switching was shown in Cu/SiO_2 devices below $I_C = 500$ μA, thus supporting Cu/SiO_2 stacks for use in select devices [21], [22]. Volatile switching was also demonstrated in CBRAM with
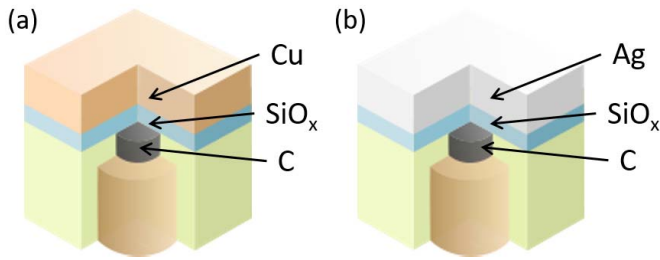
Fig. 1. Sketch of (a) Cu/SiO$_x$ select device stack and (b) Ag/SiO$_x$ select device stack.

Ag TE, and attributed to the unstable migration of Ag [21], [23]–[25]. Thanks to the extremely high ON–OFF ratio and low voltage operation, the volatile RRAM with Cu and Ag electrodes might be an excellent select device for SiO$_x$-based RRAM with high ON–OFF ratio [26].

This paper presents SiO$_x$-based (with $x \approx 1$) RRAM devices with Cu or Ag TE, exhibiting volatile switching with high ON–OFF ratio up to 10^7. The Ag/SiO$_x$ device shows bipolar switching after forming and volatile behavior for the compliance current I_C below 100 μA. The retention time has been characterized by time-resolved experiments, indicating large variability of the ON–OFF transition time in a broad range between 10 μs and 1 ms. Optimization of the retention time for fast device operation in a cross-point array is discussed.

A preliminary study of the Cu/SiO$_x$ and Ag/SiO$_x$ select devices was reported previously in [21]. Here, we provide a fully detailed report, with a deep investigation about the transition from volatile to nonvolatile switching at variable I_C, about the thickness dependence of volatile switching in Ag/SiO$_x$, and about the time evolution of the OFF-state resistance and threshold voltage after switching. This paper further elaborates about the capability of SiO$_x$-based RRAM also addressed in the companion paper about nonvolatile memory devices [26].

II. EXPERIMENTAL DEVICES AND SETUP

Fig. 1(a) shows a schematic of the select devices addressed in this paper, including Cu/SiO$_x$/C stack and Ag/SiO$_x$/C stack. Each device consists of a one-transistor/one-resistor (1T1R) structure, where the transistor was fabricated in the front end, and was connected to the BEOL select device via a W plug, similar to the RRAM devices in the companion paper [26]. The TE layer (Cu, Ag) and the SiO$_x$ switching layer were deposited by e-beam evaporation without breaking the vacuum [23]. The bottom electrode (BE) was a graphitic C pillar with a diameter of 70 nm. The metallic TE thickness was 50 nm, while SiO$_x$ was deposited with various thicknesses t_{ox} between 3 and 7 nm. A mixed DC/AC experimental setup was used to allow full electrical characterization of the select devices [26]. All devices were characterized after forming, which was carried out at positive voltage, except where noted.

III. SWITCHING CHARACTERISTICS OF Cu/SiO$_x$ DEVICES

To analyze the selector properties of our Cu/SiO$_x$ devices, we first applied a forming step with positive voltage aiming at inducing the formation of conductive filament (CF) by
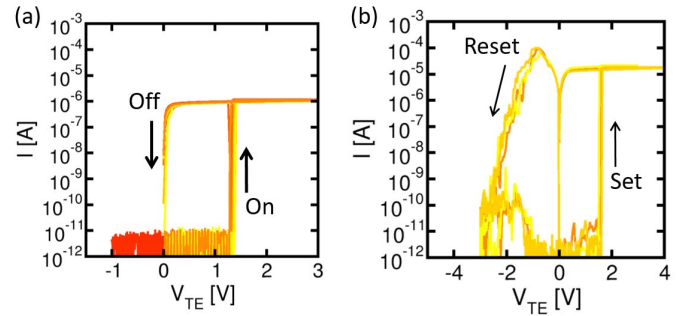

Fig. 2. (a) I–V curves for the Cu/SiO$_x$ stack for $I_C = 1$ μA. (b) I–V curves for the same device for $I_C = 20$ μA. Increasing I_C leads to a transition from unidirectional volatile switching to bipolar nonvolatile switching.

injection of Cu cations from the TE. After forming, the device was operated with the same I_C as in the forming operation, except where noted. Fig. 2(a) shows the measured I–V curves at $I_C = 1$ μA: after reducing the voltage to zero from the ON state, the device displays again OFF state during the subsequent negative and positive voltage sweeps, with constant set voltage $V_{set} = 1.2$ V. This indicates spontaneous retraction of the CF back to the TE without the need to apply any negative voltage. The spontaneous retraction is possibly due to the buildup of a compressive/tensile stress gradient inducing migration of the Cu CF back to the TE and disconnection of the CF at the BE side [27]. This, however, only occurs at zero bias, as the I–V curves clearly show the presence of an ON state during the whole voltage ramp-down, without any abrupt transition to the OFF state. Such behavior was observed for relatively low I_C, whereas for $I_C > 10$ μA, the conventional bipolar switching with nonvolatile ON state was recovered [see Fig. 2(b)]. The transition from volatile to nonvolatile switching at relatively high I_C suggests a threshold value of the CF size, possibly explained by plastic deformation of the SiO$_x$ matrix and release of the mechanical stress at the CF location, thus reducing the stress-induced instability of the LRS [27]. The ON–OFF ratio approaches 10^8 at the reset voltage $V_{reset} = -1.2$ V, namely, from the reset current $I_{reset} = 100$ μA to the HRS leakage current in the range of a few picoamperes, the latter being limited by the experimental current sensitivity. However, such a large resistance window is accompanied by extremely low endurance, in the range of a few cycles under DC operation, thus strongly limiting the feasibility of Cu/SiO$_x$ stack for nonvolatile RRAM.

IV. SWITCHING CHARACTERISTICS OF Ag/SiO$_x$ DEVICES

Fig. 3(a) shows the measured I–V curves for CBRAM devices with Ag TE shown in Fig. 1(b). In this case, the device switches to an ON state due to the formation of a Ag CF at a threshold voltage $V_T \approx 1.9$ V. A relatively high compliance current $I_C = 50$ μA was used in the experiment. As the voltage across the device decreases, the device switches back to the OFF state at a hold voltage $V_H \approx 1.3$ V, unlike the Cu-SiO$_x$ device. This suggests that the Ag CF is thinner and/or less stable compared with the Cu case, thus resulting in a more efficient CF retraction at low voltages. Also, for Ag/SiO$_x$, a
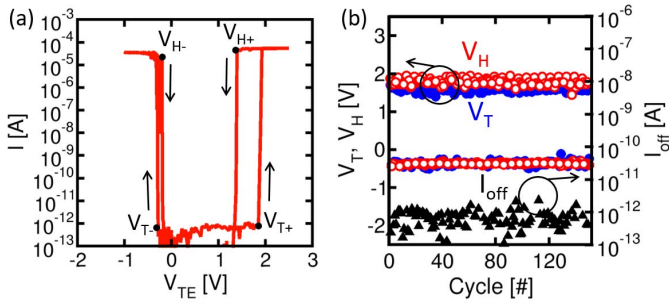
Fig. 3. (a) Measured I–V curves for the Ag/SiO$_x$ stack. (b) Measured V_T, V_H (for both positive and negative bias), and I_{OFF} as a function of the number of cycles.
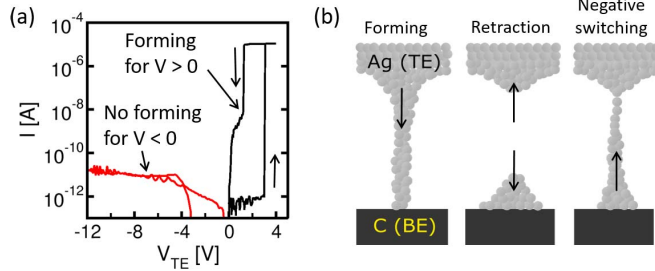

Fig. 4. (a) Measured I–V characteristics for the Ag/SiO$_x$ stack, where a negative sweep was applied first, followed by forming under positive voltage which could lead to bidirectional volatile switching. (b) Sketch of the CF structure where positive-voltage forming and successive retraction of the CF results in the formation of a BE reservoir, enabling bidirectional switching from both electrode sides.

bipolar switching behavior was observed with smaller threshold voltage at negative bias of about $V_T \approx -0.4$ V. Fig. 3(b) shows the measured V_T and V_H for 150 DC cycles for both positive and negative bias, showing the markedly asymmetric switching with smaller negative V_T and V_H. The figure also shows the subthreshold leakage current I_{OFF} at 1 V, indicating a stable leakage below 1 pA, which suggests that the whole CF was dissolved after each switching event. Data indicate an ON–OFF ratio exceeding 10^7, limited by the instrumental sensitivity of I_{OFF}.

A. Explanation of Bidirectional Switching

Given the strongly asymmetric structure of the device, similar to the Cu/SiO$_x$ stack in Section III, we investigated the origin of bipolar switching in Fig. 4. To better understand the origin of bipolar switching, we tested the possibility to form the device under negative voltage. Fig. 4(a) shows the I–V curve measured on a pristine device during a negative voltage sweep to $V_{TE} = -12$ V. In this case, no forming event was observed, thus suggesting that the BE has no active role in the switching mechanism in Ag/SiO$_x$ devices. A positive voltage sweep was then applied evidencing a forming event at $V_{TE} = 3$ V. After the forming process, application of a negative voltage revealed low voltage switching, thus demonstrating bipolar switching behavior only following positive forming.

The lack of negative forming and the onset of bidirectional switching after positive forming can be explained by the phenomena sketched in Fig. 4(b). First of all, application of a positive voltage leads to a forming process, consisting in the
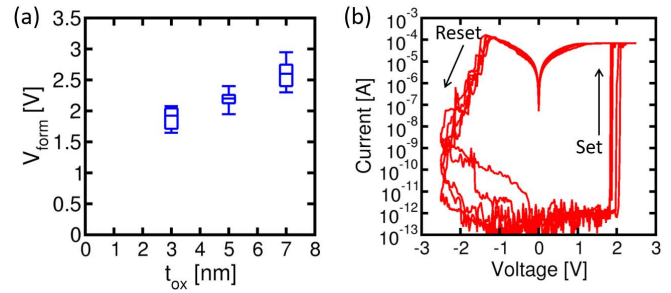

Fig. 5. (a) Forming voltage as a function of the SiO$_x$ thickness. (b) Example of RS behavior for a sample with $t_{ox} = 3$ nm.
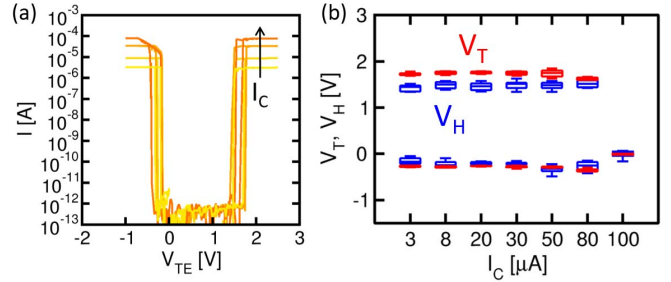

Fig. 6. (a) Measured I–V curves for the Ag/SiO$_x$ stack at increasing I_C. (b) V_T and V_H as a function of I_C, showing volatile switching for $I_C = 80$ μA and below, whereas switching at $I_C = 100$ μA led to permanent ON state ($V_T = 0$ V).

injection of Ag cations into the SiO$_x$ layer, thus creating a conductive bridge to the BE. As the bias is removed, the CF spontaneously disrupts, thus deactivating electrical connection between TE and BE. However, a significant amount of Ag atoms remain segregated at the BE side, which then can serve as a reservoir for RS upon application of a negative voltage. A similar incorporation of Ag clusters within the oxide layer in RRAM has been recently observed by high-resolution TEM [24], which supports our interpretation of bidirectional switching in Ag/SiO$_x$ devices.

B. Impact of t_{ox}

Oxide thickness plays a key role in controlling the switching characteristics of the Ag/SiO$_x$ device. Fig. 5(a) shows the forming voltage V_{form} of Ag/SiO$_x$ devices as a function of t_{ox}, ranging from 3 to 7 nm. The forming voltage increases with thickness, which is consistent with the field-driven breakdown process at the origin of forming [26]. After forming, we observed a tendency to nonvolatile switching in the case of the device with the thinnest oxide $t_{ox} = 3$ nm. This is shown in Fig. 5(b), reporting a set of switching characteristics indicating bipolar switching with positive voltage set and negative voltage reset transitions. On the other hand, devices with a thicker oxide showed bidirectional volatile switching behavior similar to data in Section IV-A. In the following, data will refer to the device with $t_{ox} = 5$ nm.

C. Impact of I_C

Volatile switching based on metallic filament formation has been previously demonstrated [18], [28], although typically at relatively low compliance current I_C which is not relevant
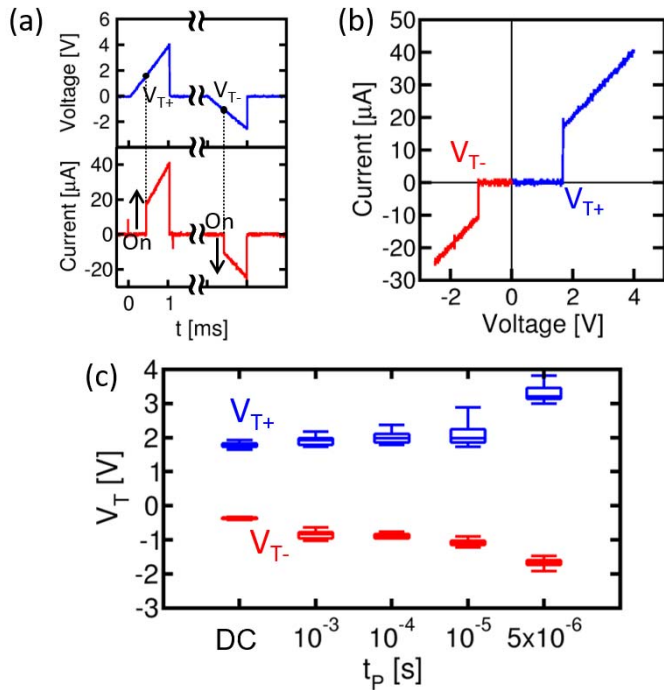
Fig. 7. (a) Measured voltage (top) and current (bottom) oscilloscope traces, (b) corresponding *I–V* curves, and (c) measured V_{T+} and V_{T-} as a function of t_P. The threshold voltage increases at decreasing t_P in agreement with the time dependence of migration dynamics in CBRAM and RRAM.

enough for practical use as select element in crossbar arrays. To study the impact of I_C on volatile switching, Fig. 6(a) shows the switching characteristics of the Ag/SiO$_x$ device for increasing I_C between 3 and 100 μA. For each value of I_C, we carried out 20 bipolar cycles (only one representative *I–V* curve is shown in the figure), and the V_T and V_H values were collected. Fig. 6(b) shows the average values of V_{T+} (positive threshold voltage), V_{T-} (negative threshold voltage), V_{H+} (positive holding voltage), and V_{H-} (negative holding voltage) as a function of I_C. Volatile switching is observed below or equal to 80 μA, whereas application of higher I_C leads to permanently ON state ($V_T = V_H = 0$ V). Different from the Cu/SiO$_x$ stack, the device could not be reset to the OFF state by negative voltage sweep. The volatile switching at $I_C \approx 80$ μA in Fig. 6 supports the use of Ag/SiO$_x$ device as select element for the Ti/SiO$_x$ RRAM [26], thus enabling all-SiO$_x$ 1S1R for crossbar arrays of nonvolatile memories.

V. PULSED CHARACTERISTICS

The pulsed characteristics of Ag/SiO$_x$ selector were studied both in terms of the switching characteristics and the pulsewidth dependence of the threshold voltage V_T. Fig. 7(a) shows the voltage and current oscilloscope traces collected with the experimental setup described in [26]. An arbitrary waveform generator was used to apply triangular voltage pulses to the 1T1R structure, while the current was monitored by measuring the voltage drop across the 50-Ω input resistance of an oscilloscope connected to the BE terminal. Triangular voltage pulses were used to monitor the threshold voltage, with a pulsewidth $t_P = 1$ ms. The threshold voltage was taken

in correspondence of the steep current rise during positive sweep to 4 V and negative sweep to −2.5 V, where the lower negative voltage is due to the asymmetric characteristics of the bipolar switching. Fig. 7(b) shows the corresponding *I–V* curve, which was obtained by combining the collected voltages and currents from the oscilloscope trace at equal times along the leading edge of the triangular pulse. Between one cycle and the other, the device was left unbiased for as long as ten times the duration of the switching pulse, to ensure that the Ag CF was completely dissolved after switching. Note the highly linear characteristic in the ON state suggesting ohmic transport in the CF. The returning *I–V* curves for decreasing voltage were not detected because of the vertical trailing edge of the voltage pulse in Fig. 7(b). The gate voltage was kept constant during both positive and negative voltage pulses.

Fig. 7(c) shows the extracted V_{T+} and V_{T-} as a function of the pulsewidth. Threshold voltages in the pulsed regime are higher than the DC counterpart and increase for decreasing pulsewidth, which is a well-known behavior in CBRAM and RRAM devices [29]. The value of V_{T+} increases from 2 V in the DC case up to more than 3 V for voltage pulses with $t_P = 5$ μs, while V_{T-} increases from −0.5 to −2 V.

VI. RETENTION TIME

Data in Fig. 7(a) show vertical OFF–ON transition indicating that the switching time was extremely fast. However, also the ON–OFF transition time is highly relevant for select devices, as all previously selected memory cells in the cross-point array must readily become unselected after access. In the Ag/SiO$_x$ device, the ON–OFF transition time is limited by the retention time of the Ag CF, which takes some time to dissolve after its formation. To study the retention time of the Ag CF, we applied an initial triangular pulse with $t_P = 1$ ms and amplitude $V_{TE} = 5$ V to switch the device in the ON state, then we monitored the resistive state of the device at increasing times by measuring the current in response to 1000 subsequent triangular pulses with $t_P = 1$ ms and $V_{TE} = 0.5$ V. This switch/read experiment was repeated 100 times on the same device to analyze the cycle-to-cycle variation of the retention time. Fig. 8 shows three representative behaviors that were observed on the same device. In Fig. 8(a), the device remains in the ON state for the whole duration of the reading pulses, while gradual dissolution of the CF and final transition to the OFF state were observed in Fig. 8(b). Immediate transition to the OFF state before the first read pulse was also detected (not shown). In the latter case, we occasionally observed a "reswitching" of the device induced by one of the read pulses, as shown in Fig. 8(c). This can be explained by a gradual disappearance of the CF, even in the case of apparent OFF state, as sketched in Fig. 9. As the CF is gradually dissolving by retraction toward the Ag TE, the application of the relatively small read voltage across the small depleted gap induces sufficient electric field to allow reformation of the CF. In this scenario, random local redistribution of Ag clusters at zero bias may play a key role in the reswitching process, as specific spatial configurations may favor Ag ions rediffusion toward the BE when a small
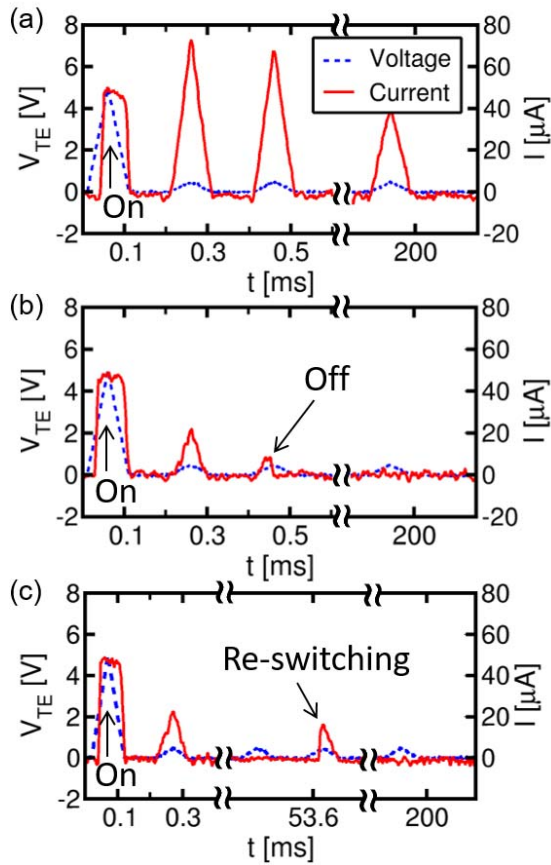
Fig. 8.   Voltage and current traces during a retention time experiment, indicating three types of behavior, namely (a) permanent ON state during the measurement, (b) gradual transition from ON to OFF state, and (c) transition to OFF state, followed by reswitching to the ON state after some time.
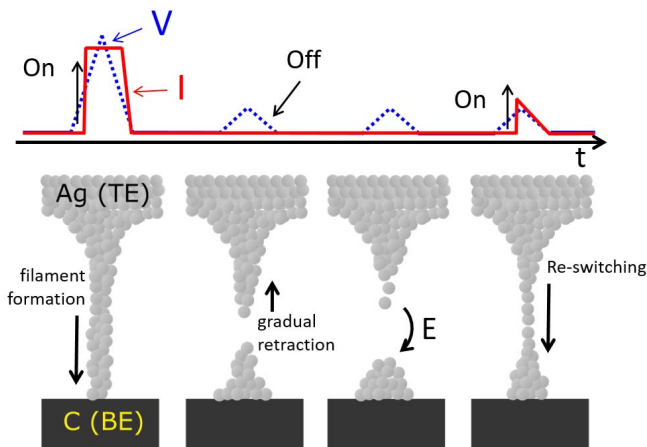

Fig. 9.   Sketch for the reswitching behavior, where the CF is first formed, then gradually dissolves, until the application of a low-voltage positive pulse causes switching to the ON state.

read voltage bias is applied. Fig. 10 summarizes the three representative behaviors by showing the measured resistance during the 1000 read pulses, including permanent ON state, gradual ON–OFF transition, and reswitching.

Given the stochastic nature of the CF dissolution, the process was studied systematically for various t_P values, as shown in Fig. 11(a). First, a triangular pulse with amplitude
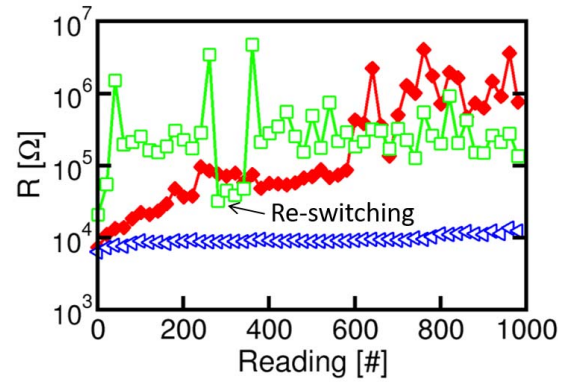

Fig. 10.   Measured R as a function of number of reading pulses for the retention experiments as the ones shown in Fig. 8, including permanent ON state, gradual transition from ON to OFF state, and reswitching behavior.
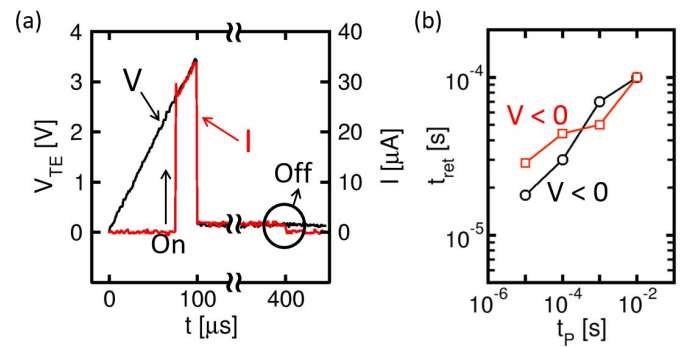

Fig. 11.   (a) Oscilloscope traces of voltage and current for measuring the retention time t_{ret}. (b) Measured t_{ret} as a function of t_P for both positive and negative switching.

$V_{TE} = 3.5$ V was applied to induce switching to the ON state, then the voltage was changed abruptly to a constant read value $V_{read} = 0.1$ V to monitor the resistive state of the device. V_{read} was chosen to prevent any additional disturb to the device and enable spontaneous switching OFF. During the first set operation, a relatively low gate voltage $V_G = 1.5$ V was used to limit the maximum current to about $I_C = 50$ μA. On the other hand, a larger gate voltage $V_G = 3$ V was used during read to minimize the series resistance of the transistor, which accounts for the read current being larger than the set current in Fig. 8(a). The read pulse was $t_{read} = 10t_P$ to include the large statistical variation of retention times. During t_{read}, the current was continuously monitored with the oscilloscope to allow for the detection of the retention time t_{ret} in correspondence of the read current dropping to zero [see Fig. 11(a)], revealing the dissolution of the CF. To improve the signal-to-noise ratio, the current was measured via a transimpedance amplifier. Fig. 11(b) shows the average t_{ret} as a function of t_P, where t_{ret} increases for increasing t_P. This is in agreement with previous observations, where the retention time was improved for increasing the set time [24], [27], which was explained as the release of the compressive stress affecting CF retention due to Joule heating during the set pulse [27]. Retention time under positive and negative switching cycles confirms the same qualitative and quantitative behaviors. Fig. 12 shows the cumulative distributions of t_{ret}
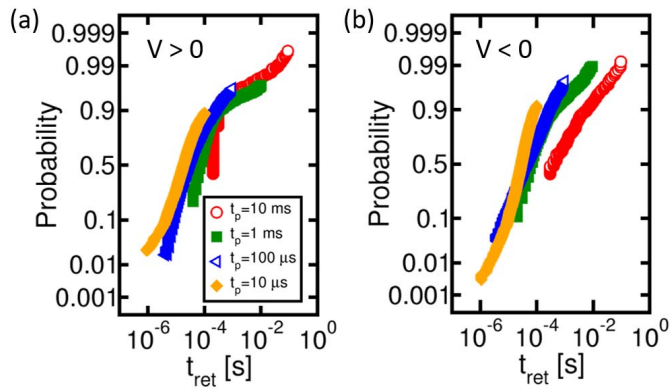
Fig. 12. Cumulative distribution of t_{ret} for (a) positive voltage switching and (b) negative voltage switching, for increasing t_P.

for increasing $t_P = 10$ μs, 100 μs, 1 ms, and 10 ms. For all values of t_P, the distributions show a large statistical spread, indicating a broad cycle-to-cycle variation of the switching OFF dynamics for the same device. Reducing the retention time and controlling its statistical variation remain vital objectives to improve the performance of Ag-based select device for implementation in the future cross-point arrays of resistive memories.

VII. CONCLUSION

This paper presents a novel volatile CBRAM device using Cu/SiO$_x$ and Ag/SiO$_x$ stacks. While Cu/SiO$_x$ stack only shows unipolar select operation at relatively low currents, Ag/SiO$_x$ indicates excellent bidirectional select operation with ON–OFF ratio exceeding 10^7 and maximum current around 80 μA, which is fully compatible with low-current Ti/SiO$_x$ RRAM. The device was characterized in pulsed regime to evaluate the threshold voltage and retention time, the latter indicating a broad distribution in the range of 1 μs–10 ms. Reducing and controlling the retention time remain a key challenge for Ag-based select devices for future crossbar array applications. More research work at the levels of materials engineering and pulse algorithm will be needed to improve the performance for practical use in memory technology.

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