Resistive Switching Device Technology Based on Silicon Oxide for Improved ON–OFF Ratio—Part I: Memory Devices

Alessandro Bricalli, *Student Member, IEEE*, Elia Ambrosi, Mario Laudato, *Student Member, IEEE*, Marcos Maestro, Rosana Rodriguez, *Senior Member, IEEE*, and Daniele Ielmini, *Senior Member, IEEE*

***Abstract*— Resistive switching memory (RRAM) is among the most mature technologies for next generation storage class memory with low power, high density, and improved performance. The biggest challenge toward industrialization of RRAM is the large variability and noise issues, causing distribution broadening which affects retention even at room temperature. Noise and variability can be addressed by enlarging the resistance window between low-resistance state and high-resistance state, which requires a proper engineering of device materials and electrodes. This paper presents an RRAM device technology based on silicon oxide (SiO_x), showing high resistance window thanks to the high bandgap in the silicon oxide. Endurance, retention, and variability show excellent performance, thus supporting SiO_x as a strong active material for developing future generation RRAMs.**

***Index Terms*— Cross point array, memory reliability, nonvolatile memory technology, resistive switching memory (RRAM), silicon oxide, storage class memory (SCM).**

I. Introduction

RESISTIVE switching memory (RRAM) devices are promising for future replacement of nonvolatile high-density memories, such as Flash and storage class memory (SCM), the latter combining the high density and low cost of Flash memory with the short latency and random bit access of RAM [1]. Although RRAM has been raising a strong interest, the reliability aspects have prevented the development of a commercial technology so far. In particular, RRAM generally suffers from programming variability [2]–[4] and noise-induced distribution broadening [3], [5], [6], which significantly limit retention in large arrays even at room temperature.

To mitigate the impact of noise on programmed distributions, the intrinsic resistance window of the RRAM device must be improved. For instance, RRAM devices based on metal cation migration, also known as conductive-bridge RAM (CBRAM) devices, have shown improved resistance window compared with the conventional metal–oxide RRAM [7], mainly thanks to a high-resistance state (HRS). Alternative schemes to improve the resistance window include the use of relatively high compliance current I_C to lower the low-resistance state (LRS) resistance, however, causing a corresponding increase of current consumption [8]. Enhancing and controlling the HRS resistance seem thus essential to improve RRAM reliability.

This paper presents a new RRAM device technology based on silicon oxide, i.e., SiO_x with $x \approx 1$. The device shows bipolar switching with high resistance window, reaching a ratio of about 10^4 between HRS and LRS despite a low compliance current $I_C = 50\ \mu A$. The device also shows excellent reliability, including high endurance (above 10^7 cycles), small variability, and good retention (1 hour at 260 °C). These data fully support SiO_x memory technology as a promising candidate for future SCM and embedded RRAM [9], [10].

A preliminary study of the SiO_x devices was previously reported in [11]. Here, we provide a fully detailed report, further exploring the thickness dependence, the voltage-controlled overshoot and endurance, and the impact of I_C scaling. While this paper addresses the switching and reliability characteristics of SiO_x memory, the companion paper presents volatile switching in SiO_x-based devices with potential application as selectors in crossbar arrays [12].

II. Experimental Devices and Setup

Fig. 1(a) shows a schematic illustration of the RRAM device studied in this paper. In the RRAM device, the switching layer consists of SiO_x as in previous RRAM works [13], [14]. The SiO_x switching layer was deposited by e-beam evaporation from a silicon monoxide source, thus $x \approx 1$. The Ti top electrode (TE) was e-beam evaporated without breaking the vacuum from the previous SiO_x deposition. Both SiO_x and Ti were deposited on the top of a confined graphitic carbon (C)

Manuscript received August 18, 2017; revised October 25, 2017 and November 20, 2017; accepted November 22, 2017. Date of current version December 27, 2017. This work was supported by the European Research Council under Grant ERC-2014-CoG-648635-RESCUE. The review of this paper was arranged by Editor U. E. Avci. *(Corresponding author: Daniele Ielmini.)*

A. Bricalli, E. Ambrosi, M. Laudato, and D. Ielmini are with the Dipartimento di Elettronica, Informazione e Bioingegneria and the Italian Universities Nanoelectronics Team, Politecnico di Milano, 20133 Milan, Italy (e-mail: alessandro.bricalli@polimi.it; elia.ambrosi@polimi.it; mario.laudato@polimi.it; daniele.ielmini@polimi.it).

M. Maestro and R. Rodriguez are with the Universitat Autònoma de Barcelona, 08193 Barcelona, Spain (e-mail: marcos.maestro@uab.cat; rosana.rodriguez@uab.cat).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2017.2777986

This work is licensed under a Creative Commons Attribution 3.0 License. For more information, see http://creativecommons.org/licenses/by/3.0/

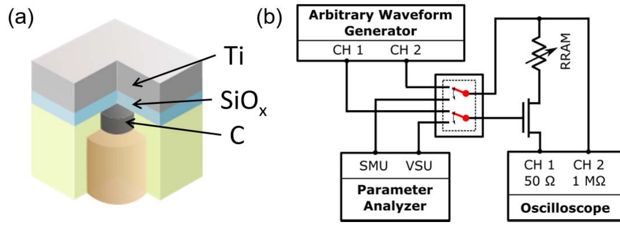

Fig. 1. (a) Sketch of the Ti/SiO_x RRAM device stack. (b) Schematic of the setup for the electrical characterization of the devices.

bottom electrode with a diameter of 70 nm. Below the C electrode, a W-plug served as via to an integrated select transistor in the front end. The availability of an integrated transistor enables independent selection of any RRAM device and control of the compliance current I_C during set transition with negligible parasitic capacitance [15], [16]. The Ti thickness was usually 50 nm, while SiO_x was deposited with various thicknesses t_{ox} between 1.5 and 6.5 nm to optimize the switching and forming characteristics. Atomic force microscopy (AFM) was used to characterize t_{ox} on control samples by measuring the AFM profile over a step obtained with a shadow mask [11].

The experimental setup sketched in Fig. 1(b) included both a semiconductor parameter analyzer for DC measurements and an arbitrary waveform generator with an oscilloscope to test the pulsed characteristics. In both cases, the one-transistor/one-resistor (1T1R) structure was characterized by controlling both the gate and the TE voltage with source grounded. The AC current was measured at the source side via the voltage drop across the 50-Ω input impedance of the oscilloscope during pulsed measurements.

III. Forming and Switching Characteristics

Devices were characterized by first applying a forming step with positive voltage aiming at inducing the injection of cations from Ti to form a conductive filament (CF). The CF was then retracted to the TE by the application of a negative voltage in the reset operation. Positive set and negative reset processes were then operated in DC or AC mode to study bipolar switching.

We attribute resistance switching in our devices to Ti cation migration originated from the TE during forming. Cation migration is usually assumed to take place in CBRAM-type devices with Ag/Cu containing TE [17], [18]. However, it was long been postulated that other metals, such as Ti, Ta, and Hf, could lead to migration in oxide-based RRAM [19], which was recently shown by experiments [20]. Moreover, our devices did not show any forming even for negative voltages up to −10 V. This is a further reason to believe that the resistance switching in our devices can be explained by Ti cation migration within a Ti-rich CF, where the lower mobility of Ti and the higher chemical interaction between Ti and SiO_x can be responsible for lower variability and improved retention with respect to more conventional Ag- and Cu-based CBRAM [18]. However, we cannot rule out that oxygen vacancy and silicon nanoinclusions contribute to the switching process in our samples, as proposed in other SiO_x-based RRAM [14].

A. Thickness Dependence

Fig. 2(a) shows the typical *I*–*V* curves of forming, set, and reset transitions for an RRAM device with SiO_x thickness $t_{ox} = 3$ nm. The forming process takes place at relatively large positive voltage V_{form}. After the forming process, the device starts to reset at a negative voltage V_{reset}. The device shows an incremental reset transition, where resistance increases at increasing voltage as a result of the increasing length of the depleted gap Δ and the decreasing density of defects within Δ [21]. The HRS resistance thus depends on the maximum negative voltage V_{stop}, which is applied during the reset transition. Application of a positive voltage to the LRS shows a set transition, consisting of an abrupt increase of current at a voltage V_{set}. Despite a large resistance window of about 10^4 in Fig. 2(a), the HRS resistance is smaller than the initial resistance of the device in the pristine state.

Fig. 2(b) shows the typical *I*–*V* curves for set and reset transitions for SiO_x thickness $t_{ox} = 1.5$, 3, and 6.5 nm, while Fig. 2(c) summarizes the forming, set, and reset voltages as a function of t_{ox}. The forming voltage increases linearly with the oxide thickness, in accordance to a field-driven oxide breakdown model, such as the E model [22] or the 1/E model [23]. The estimated breakdown electric field for the SiO_x layer is 13.1 MVcm^{-1}. On the other hand, V_{set} and V_{reset} show a slight increase with t_{ox}. The decrease of V_{set} with thickness can be attributed to the decrease of HRS resistance, which is visible in Fig. 2(b) for $t_{ox} = 1.5$ nm and might be explained by the depleted width Δ being limited by t_{ox}. For $t_{ox} = 6.5$ nm, the device tends to exhibit current overshoot, evidenced by the reset current I_{reset} being higher than I_C. Current overshoot might be due to the relatively large value of V_{set} causing fast transition to LRS before the voltage snap back in the 1T1R structure can take place [16]. The best tradeoff between HRS and LRS control was obtained at $t_{ox} = 3$ nm, which was thus taken as a reference case for the following in-depth analysis of the switching characteristics of RRAM devices.

B. Impact of V_{stop}

Fig. 3(a) shows the measured *I*–*V* curves for increasing V_{stop} in SiO_x RRAM devices with $t_{ox} = 3$ nm. A single device was cycled 20 times for each V_{stop}, starting from $V_{stop} = -4.5$ V and gradually decreasing $|V_{stop}|$ toward − 2.5 V. A compliance current $I_C = 70$ μA was used during forming and during all set processes. The resistance window can be effectively increased with V_{stop}, as shown by the measured HRS and LRS resistance values in Fig. 3(b). While HRS resistance increases, LRS resistance decreases at increasing amplitude of V_{stop}, probably due to the increasing value of V_{set} as shown in Fig. 3(c). As V_{stop} increases, the concentration of defects within the depleted gap length Δ decreases [21], and thus, the leakage current decreases and the corresponding V_{set} increases. A larger V_{set} causes moderate current overshoot with a small

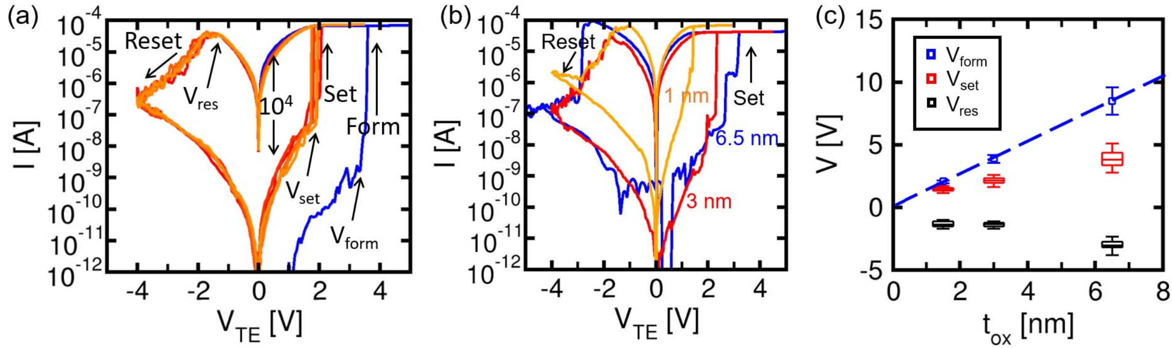

Fig. 2. (a) Typical I–V characteristics of a Ti/SiO_x RRAM device. (b) Comparison of I–V curves for RRAM devices with increasing oxide thicknesses $t_{ox} = 1.5$, 3, and 6.5 nm. (c) Summary of forming, set, and reset voltages as a function of t_{ox}. The forming voltage shows linear increase with t_{ox}.

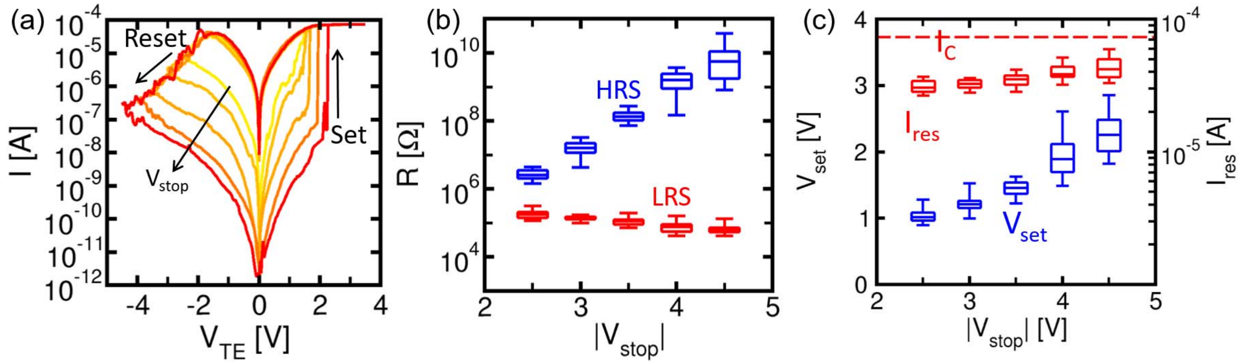

Fig. 3. (a) I–V curves of a Ti/SiO_x RRAM devices for increasing V_{stop}. (b) LRS and HRS resistance values as a function of V_{stop}. (c) V_{set} and I_{reset} as a function of V_{stop}. Increasing V_{stop} generally leads to an increase of the resistance window, still maintaining low reset current $I_{reset} < I_C$.

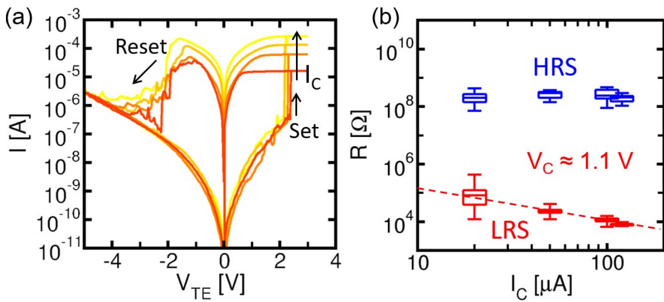

Fig. 4. (a) I–V curves of the Ti/SiO_x RRAM for increasing I_C. (b) LRS and HRS resistance as a function of I_C. Data for LRS resistance in (b) indicate a critical voltage V_C of about 1.1 V.

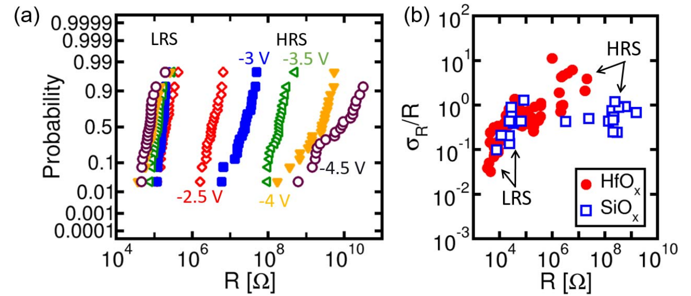

Fig. 5. (a) Cumulative distributions of measured resistance for LRS and HRS at various V_{stop} values. (b) Normalized standard deviation of R as a function of R for Ti/SiO_x RRAM and previously reported HfO_x RRAM. Data indicate similar LRS variability, whereas HRS variability was remarkably improved in the silicon oxide device.

decrease of LRS resistance, although I_{reset} never exceeds I_C by more than 20% [Fig. 3(c)].

C. Impact of I_C

Fig. 4(a) shows the measured I–V curves for increasing I_C, which was changed by varying the gate voltage V_G applied to the transistor in the 1T1R structure. Fig. 4(b) shows the measured R as a function of I_C for LRS and HRS. All devices were initially formed at $I_C = 20\ \mu$A, and then, set/reset experiments were conducted at increasing I_C. Larger values of I_C result in smaller LRS resistances in the range between 10 and 100 kΩ, revealing an increasing size of the CF, while the HRS is negligibly affected. The LRS resistance decreases as $R \approx V_C/I_C$, where the characteristic voltage V_C for ion migration is around 1.1 V, in agreement with previous results [19]. This is the voltage needed to induce ion migration in the timescale of the experiment, which was about 1 s in this paper. Interestingly, $V_C \approx 1.1$ V is very close to the absolute value of V_{reset} in Figs. 3 and 4, revealing polarity-independent ion migration in SiO_x [21].

D. LRS and HRS Variability

Fig. 5(a) shows the cumulative distributions of measured R for LRS at increasing I_C and HRS at increasing V_{stop}.

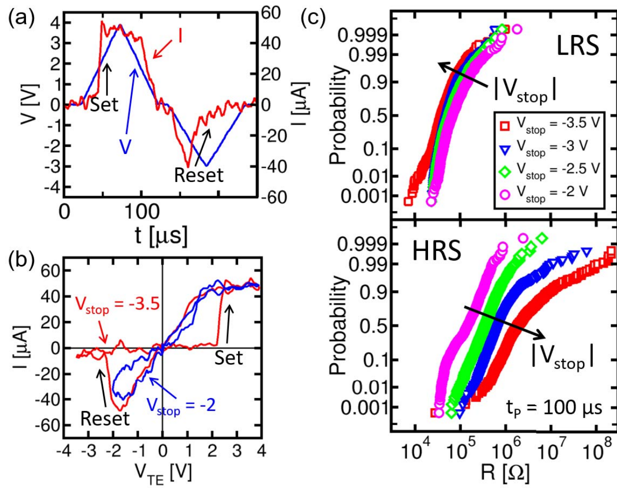

Fig. 6. (a) Measured oscilloscope traces of voltage and current during the application of a set/reset cycle with $t_P = 100\ \mu$s. (b)Corresponding I–V curves for $V_{stop} = -2$ and -3.5 V. (c) Cumulative distribution of R for LRS (top) and HRS (bottom) at increasing V_{stop} for $t_P = 100\ \mu$s. Resistance was measured by the ac setup, which accounts for the reduced HRS resistance and ON–OFF window.

Data generally show a good control of resistance levels by varying either I_C or V_{stop}, which is promising for multilevel cell operation of SiO_x-RRAM devices. However, distributions show a significant statistical spread, which can be quantified by the standard deviation σ_R. Fig. 5(b) shows the relative spread σ_R/R, which is generally considered a figure of merit for the variability of set/reset processes in RRAM [3], [4]. The relative standard deviation σ_R/R is shown as a function of R and compared with HfO_x RRAM [3]. Both LRS data at variable I_C and HRS data at variable V_{stop} are reported. LRS shows similar variability in SiO_x and HfO_x, suggesting a common origin of the CF, such as metallic-type defects, *e.g.*, Ti or Hf. In both cases, LRS variability shows a linear dependence with resistance, namely $\sigma_R/R \approx R$, which can be attributed to defect shape variation in the CF [3], [4]. On the other hand, HRS shows markedly different variabilities in the two materials, with SiO_x displaying approximately constant $\sigma_R/R \approx 1$, hence much smaller than HfO_x. Given the strong impact of HRS variability on RRAM array reliability, these data suggest that SiO_x is much more promising than HfO_x in the view of the higher resistance window and decreased variability.

IV. Pulsed Characteristics

We characterized RRAM devices in the pulsed regime by applying triangular set and reset pulses with pulsewidth $t_P = 100\ \mu$s using the setup in Fig. 1(b). Fig. 6(a) shows the typical voltage and current traces of set and reset operations. Different gate voltages were applied for the set pulse ($V_G = 1.2$ V, resulting in a compliance current $I_C = 50\ \mu$A) and the reset pulse ($V_G = 2.5$ V, thus limiting the transistor series resistance to maximize the voltage drop across the RRAM device). Peak voltages $V_+ = 4$ V and $V_{stop} = -3.5$ V were used in the two pulses. During the positive voltage pulse, an abrupt current increase can be observed, corresponding

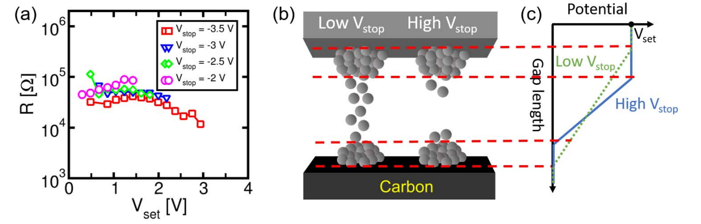

Fig. 7. (a) LRS resistance as a function of V_{set} for increasing V_{stop}. (b) Sketch of the CF structure at low and high V_{stop}. (c) Schematic profile of the electrostatic potential along the CF in the two cases shown in (b). As V_{stop} increases, the electric field increases within the depleted gap at a given V_{set}, thus resulting in larger migration and smaller LRS resistance for the same V_{set} in (a).

to the set transition to LRS. During the negative voltage pulse, before the maximum voltage V_{stop} is reached, the reset process starts occurring, resulting in a gradual decrease of current, bringing the device back to HRS. The corresponding I–V curves can be reconstructed by merging the voltage and current traces together, as shown in Fig. 6(b) [24].

The pulsed regime behavior of SiO_x devices was studied by applying pulse trains with V_{stop} varying from -2 to -3.5 V with 0.5-V steps, to characterize the resistance window opening. For each V_{stop}, 1000 set–reset cycles were applied to the memory cell. Fig. 6(c) and (d) shows the distributions of measured resistance of LRS and HRS. As for the DC case, increasing $|V_{stop}|$ causes a slight decrease of LRS resistance and a strong increase of HRS resistance, thus leading to an enlargement of the resistance window by one order of magnitude on average. In pulsed regime, however, experimental noise strongly influences the oscilloscope readout, both in terms of the maximum readable HRS value, which may be underestimated for higher values of $|V_{stop}|$, and also in terms of spreading in the HRS distributions, which is larger compared with the DC regime. Moreover, measured HRS values are inherently lower when compared with the corresponding DC readings; this is a well-known effect for resistive switching devices based on ion migration, as the maximum V_{stop} voltage needed to fully reset the devices increases by decreasing the pulsewidth [25]. Data in Fig. 6 again show that LRS resistance decreases at increasing V_{stop}, which was attributed to a moderate overshoot effect in Section III-B.

To better understand the LRS dependence on V_{stop}, Fig. 7(a) shows the measured LRS resistance as a function of V_{set} and for different $|V_{stop}|$ values, indicating that, even for a given V_{set} value, R decreases at increasing V_{stop}. This is different from usual overshoot effects, where R decreases at increasing V_{set} because of the switching time becoming shorter than the electrical RC constant [16], [26]. We attribute this new type of overshoot to the local electric field at set transition. In fact, as V_{stop} increases, the concentration of defects within the depleted gap length Δ decreases, thus causing a decrease of conductance in the depleted gap. This is schematically shown in Fig. 7(b). As a result, the electric field F across the depleted gap increases with V_{stop} [Fig. 7(c)], even for a fixed V_{set}. The high internal field induces a stronger migration at the onset of set transition, resulting in a bigger CF and a lower R, which can explain the slight overshoot effect in Fig. 7(a).

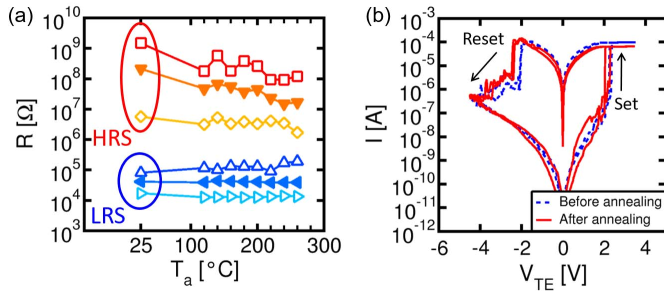

Fig. 8. (a) Resistance measured at room temperature after a 1-h annealing, as a function of the temperature of the annealing. (b) *I–V* curves of the Ti/SiO$_x$ device measured before and after a full sequence of annealing at increasing temperature. Both LRS and HRS show good stability for annealing temperatures reaching 260 °C.

V. Reliability Study

For adoption as SCM or embedded nonvolatile memory, SiO$_x$ RRAM must satisfy not only switching window, variability, and noise requirements, but also endurance and temperature-dependent retention criteria. For instance, application as embedded memory requires that the written data survive the thermal budget of the soldering reflow, typically few minutes at 260 °C [27], [28]. The reliability of SiO$_x$ RRAM devices was studied from the point of view of both data retention at high temperature and endurance.

A. High-Temperature Retention

To study data retention in SiO$_x$ RRAM, we prepared three RRAM devices in various LRSs at increasing $I_C = 10$, 25, and 60 μA, while other three devices were prepared in various HRSs at increasing $V_{\text{stop}} = -3, -4$, and -4.5 V. After this preliminary stage, the devices were annealed at constant temperature $T_a = 120$ °C for 1 h, and then, the resistance of each device was measured to check for variations. Preannealing and postannealing measurements were both done at room temperature to prevent resistance differences due to T-activation of conduction [29]. The annealing/read process was repeated eight times, each time increasing T_a by 20 °C up to a maximum value of $T_a = 260$ °C.

Fig. 8(a) shows the measured R as a function of T_a, including initial values before annealing. HRS shows a weak decrease of R toward LRS, which might be explained by redistribution of defects into the depleted gap from the top and bottom residual fractions of the CF. Even at the highest T_a in the experiments, R decreases by about one order of magnitude, thus revealing a good retention at high temperature. On the other hand, LRS shows a weak increase of resistance toward HRS, the larger drift occurring at the highest R as previously explained by size-dependent retention in RRAM [30]. Such strong retention of LRS is also very promising, given that LRS retention is regarded as particularly critical because of the filamentary nature of the RRAM device [4]. As a reference, HfO$_x$-based RRAM shows weaker LRS stability, with a drift by a factor 2 in 1 h at 250 °C for a smaller resistance $R = 5$ kΩ, corresponding to a larger CF than in this paper [31]. The better stability at high temperature might be attributed to the chemical interaction between Ti and SiO$_x$, where Ti can form both TiSi silicide and several Magneli-type compounds with oxygen [32].

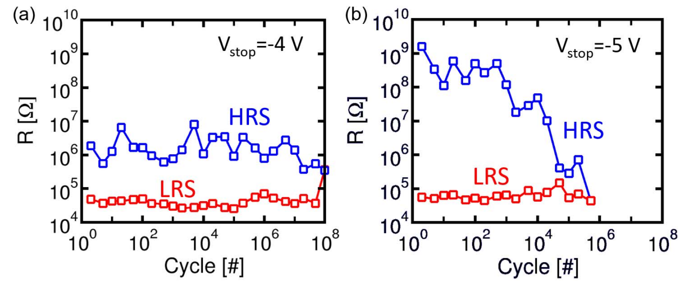

Fig. 9. LRS and HRS resistance as a function of the number of cycles for (a) $V_{\text{stop}} = -4$ V and (b) $V_{\text{stop}} = -5$ V.

Fig. 8(b) shows the *I–V* curves for the case of $V_{\text{stop}} = -4.5$ V, measured before and after the full sequence of annealing experiments in Fig. 8(a). The *I–V* curves are negligibly affected by the extensive annealing, suggesting that not only the LRS/HRS are stable over time and temperature but also the structural properties of the thin films remain unaffected.

B. Endurance Characteristics

The endurance characteristics of SiO$_x$ devices were studied by applying triangular pulses with pulsewidth $t_P = 10$ μs as described in Section IV. The resistance was measured three times over each decade of cycling by switching from DC to AC and *vice versa* via the switching matrix setup in Fig. 1(b) This allowed accurate DC measurement of HRS during cycling.

Fig. 9(a) and (b) shows the measured R for increasing cycles at $V_{\text{stop}} = -4$ V and -5 V. The first case corresponds to a relatively low resistance window of about two orders of magnitude, and resulting in a relatively high endurance in excess of 10^7 cycles, with a very clear distinction between HRS and LRS throughout the whole device lifetime. In the second experiment, V_{stop} was increased, which enhances the resistance window to about three orders of magnitude, however, causing a faster degradation and a reduced endurance of about 10^5 cycles. These results are in line with the previously observed tradeoff between resistance window and endurance controlled by V_{stop} [24]. Compared with the HfO$_x$-based RRAM, SiO$_x$ displays a much larger endurance at the optimum V_{stop}, which was around 10^6 for HfO$_x$ [24].

VI. Conclusion

This paper presents a novel Ti/SiO$_x$ resistive memory device with high resistive window of four orders of magnitude, extended endurance over 10^7, and good data retention up to 260 °C. The impact of V_{stop}, I_C, and oxide layer thickness was studied. The extremely good performance exhibited by the device distinguishes Ti/SiO$_x$ as a promising technology for future generation SCM and embedded memory application.

References

[1] G. W. Burr, B. N. Kurdi, J. C. Scott, C. H. Lam, K. Gopalakrishnan, and R. S. Shenoy, "Overview of candidate device technologies for storage-class memory," *IBM J. Res. Develop.*, vol. 52, nos. 4–5, pp. 449–464, 2008, doi: 10.1147/rd.524.0449.

[2] X. Guan, S. Yu, and H.-S. P. Wong, "On the switching parameter variation of metal-oxide RRAM—Part I: Physical modeling and simulation methodology," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1172–1182, Feb. 2012, doi: 10.1109/TED.2012.2184545.

[3] S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Statistical fluctuations in HfO_x resistive-switching memory: Part II—Random telegraph noise," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2920–2927, Aug. 2014, doi: 10.1109/TED.2014.2330202.

[4] D. Ielmini, "Resistive switching memories based on metal oxides: Mechanisms, reliability and scaling," *Semicond. Sci. Technol.*, vol. 31, p. 063002, May 2016, doi: https://doi.org/10.1088/0268-1242/31/6/063002.

[5] D. Ielmini, F. Nardi, and C. Cagli, "Resistance-dependent amplitude of random telegraph-signal noise in resistive switching memories," *Appl. Phys. Lett.*, vol. 96, p. 053503, Jan. 2010, doi: http://dx.doi.org/10.1063/1.3304167.

[6] S. Ambrogio, S. Balatti, V. McCaffrey, D. C. Wang, and D. Ielmini, "Noise-induced resistance broadening in resistive switching memory—Part II: Array statistics," *IEEE Trans. Electron Devices*, vol. 62, pp. 3812–3819, Nov. 2015, doi: 10.1109/TED.2015.2477135.

[7] A. Calderoni, S. Sills, C. Cardon, E. Faraoni, and N. Ramaswamy, "Engineering ReRAM for high-density applications," *Microelectron. Eng.*, vol. 147, pp. 145–150, Nov. 2015, doi: https://doi.org/10.1016/j.mee.2015.04.044.

[8] A. Prakash, J. Park, J. Song, J. Woo, E. J. Cha, and H. Hwang, "Demonstration of low power 3-bit multilevel cell characteristics in a TaO_x-based RRAM by stack engineering," *IEEE Electron Device Lett.*, vol. 36, no. 1, pp. 32–34, Jan. 2015, doi: 10.1109/LED.2014.2375200.

[9] M.-F. Chang *et al.*, "19.4 Embedded 1Mb ReRAM in 28 nm CMOS with 0.27-to-1 V read using swing-sample-and-couple sense amplifier and self-boost-write-termination scheme," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 332–333, doi: 10.1109/ISSCC.2014.6757457.

[10] M. Ueki *et al.*, "Low-power embedded ReRAM technology for IoT applications," in *Proc. Symp. VLSI Circuits*, Jun. 2015, pp. T108–T109, doi: 10.1109/VLSIC.2015.7231367.

[11] A. Bricalli, E. Ambrosi, M. Laudato, M. Maestro, R. Rodriguez, and D. Ielmini, "SiO_x-based resistive switching memory (RRAM) for crossbar storage/select elements with high on/off ratio," in *IEDM Tech. Dig.*, Feb. 2016, pp. 4.3.1–4.3.4, doi: 10.1109/IEDM.2016.7838344.

[12] A. Bricalli, E. Ambrosi, M. Laudato, M. Maestro, R. Rodriguez, and D. Ielmini, "Resistive switching device technology based on silicon oxide for improved on-off ratio—Part II: Select devices," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 122–128, Jan. 2018.

[13] J. Yao *et al.*, "Resistive switching in nanogap systems on SiO_2 substrates," *Small*, vol. 5, no. 24, pp. 2910–2915, 2009, doi: 10.1002/smll.200901100.

[14] A. Mehonic *et al.*, "Resistive switching in silicon suboxide films," *J. Appl. Phys.*, vol. 111, no. 7, p. 074507, 2012, doi: http://dx.doi.org/10.1063/1.3701581.

[15] K. Kinoshita *et al.*, "Reduction in the reset current in a resistive random access memory consisting of NiO_x brought about by reducing a parasitic capacitance," *Appl. Phys. Lett.*, vol. 93, no. 3, p. 033506, 2008, doi: http://dx.doi.org/10.1063/1.2959065.

[16] S. Ambrogio, V. Milo, Z. Wang, S. Balatti, and D. Ielmini, "Analytical modeling of current overshoot in oxide-based resistive switching memory (RRAM)," *IEEE Electron Device Lett.*, vol. 37, no. 10, pp. 1268–1271, Aug. 2016, doi: 10.1109/LED.2016.2600574.

[17] C. Schindler, M. Meier, R. Waser, and M. Kozicki, "Resistive switching in Ag-Ge-Se with extremely low write currents," in *Proc. Non-Volatile Memory Technol. Symp. (NVMTS)*, Dec. 2007, pp. 82–85, doi: 10.1109/NVMT.2007.4389953.

[18] S. Ambrogio, S. Balatti, S. Choi, and D. Ielmini, "Impact of the mechanical stress on switching characteristics of electrochemical resistive memory," *Adv. Mater.*, vol. 26, no. 23, pp. 3885–3892, Mar. 2014, doi: 10.1002/adma.201306250.

[19] D. Ielmini, "Modeling the universal set/reset characteristics of bipolar RRAM by field- and temperature-driven filament growth," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4309–4317, Oct. 2011, doi: 10.1109/TED.2011.2167513.

[20] A. Wedig *et al.*, "Nanoscale cation motion in TaO_x, HfO_x and TiO_x memristive systems," *Nature Nanotechnol.*, vol. 11, pp. 67–74, Sep. 2016, doi: 10.1038/nnano.2015.221.

[21] F. Nardi, S. Larentis, S. Balatti, D. C. Gilmer, and D. Ielmini, "Resistive switching by voltage-driven ion migration in bipolar RRAM—Part I: Experimental study," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2461–2467, Aug. 2012, doi: 10.1109/TED.2012.2202319.

[22] J. W. McPherson and H. C. Mogul, "Underlying physics of the thermochemical E model in describing low-field time-dependent dielectric breakdown in SiO_2 thin films," *J. Appl. Phys.*, vol. 84, pp. 1513–1523, May 1998, doi: http://dx.doi.org/10.1063/1.368217.

[23] J. W. McPherson, V. Reddy, K. Banerjee, and H. Le, "Comparison of E and 1/E TDDB models for SiO_2/under long-term/low-field test conditions," in *IEDM Tech. Dig.*, Dec. 1998, pp. 171–174, doi: 10.1109/IEDM.1998.746310.

[24] S. Balatti *et al.*, "Voltage-controlled cycling endurance of HfO_x-based resistive-switching memory," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3365–3372, Oct. 2015, doi: 10.1109/TED.2015.2463104.

[25] S. Larentis, F. Nardi, S. Balatti, D. C. Gilmer, and D. Ielmini, "Resistive switching by voltage-driven ion migration in bipolar RRAM—Part II: Modeling," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2468–2475, Sep. 2012, doi: 10.1109/TED.2012.2202320.

[26] Z. Wang *et al.*, "Postcycling degradation in metal-oxide bipolar resistive switching memory," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4279–4287, Nov. 2016, doi: 10.1109/TED.2016.2604370.

[27] H. Lung *et al.*, "A method to maintain phase-change memory pre-coding data retention after high temperature solder bonding process in embedded systems," in *Proc. Symp. VLSI Technol. (VLSIT)*, Jun. 2011, pp. 98–99.

[28] N. Ciocchini, E. Palumbo, M. Borghi, P. Zuliani, R. Annunziata, and D. Ielmini, "Modeling resistance instabilities of set and reset states in phase change memory with Ge-rich GeSbTe," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2136–2144, Jun. 2014, doi: 10.1109/TED.2014.2313889.

[29] D. Ielmini, F. Nardi, and C. Cagli, "Physical models of size-dependent nanofilament formation and rupture in NiO resistive switching memories," *Nanotechnology*, vol. 22, no. 25, p. 254022, 2011, doi: https://doi.org/10.1088/0957-4484/22/25/254022.

[30] D. Ielmini, F. Nardi, C. Cagli, and A. L. Lacaita, "Size-dependent retention time in NiO-based resistive-switching memories," *IEEE Electron Device Lett.*, vol. 31, no. 4, pp. 353–355, Apr. 2010, doi: 10.1109/LED.2010.2040799.

[31] B. Traoré *et al.*, "On the origin of low-resistance state retention failure in HfO_2-based RRAM and impact of doping/alloying," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 4029–4036, Oct. 2015, doi: 10.1109/TED.2015.2490545.

[32] D.-H. Kwon *et al.*, "Atomic structure of conducting nanofilaments in TiO_2 resistive switching memory," *Nature Nanotechnol.*, vol. 5, pp. 148–153, Jan. 2010, doi: 10.1038/nnano.2009.456.

Alessandro Bricalli (S'16) received the B.S. and M.S. degrees in engineering physics from the Politecnico di Milano, Milan, Italy, in 2013 and 2015, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering.

His current research interests include the fabrication and electrical characterization of RRAM devices for memory application and beyond-CMOS computing systems.

Elia Ambrosi received the B.S. and M.S. degrees in electrical engineering from the Politecnico di Milano, Milan, Italy, in 2013 and 2016, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering.

His current research interests include the electrical characterization and modeling of resistive switching devices for novel memory and computing architectures.

Mario Laudato (S'15) received the M.S. degree in electrical engineering from the Politecnico di Milano, Milan, Italy, in 2014, where he is currently pursuing the Ph.D. degree in electrical engineering, with a focus on nonvolatile emerging memories and select devices for high-density crosspoint memory and neuromorphic computing.

Marcos Maestro received the bachelor's degree in physics from the Universidad de Salamanca, Salamanca, Spain, in 2009, the master's degrees in physics instrumentation from the Universidad de Valladolid, Valladolid, Spain, and in micro and nanoelectronics from the Universitat Autònoma de Barcelona, Barcelona, Spain, in 2012 and 2013, respectively, and the Ph.D. degree in electronic engineering and telecommunications from the Universitat Autònoma de Barcelona in 2017.

Rosana Rodriguez (SM'13) received the Ph.D. degree in electrical engineering from the Universitat Autònoma de Barcelona (UAB), Barcelona, Spain, in 2000.

She is currently an Associate Professor with UAB. Her current research interests include the study of the resistive switching phenomenon and its applications.

Daniele Ielmini (SM'09) received the Ph.D. degree in nuclear engineering from the Politecnico di Milan, Milan, Italy, in 2000.

He joined the Dipartimento di Elettronica, Informazione, e Bioingegneria, Politecnico di Milan, in 2002, where he is currently a Professor.

Dr. Ielmini received the Intel Outstanding Researcher Award in 2013, the ERC Consolidator Grant in 2014, and the IEEE EDS Rappaport Award in 2015.