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Abstract—**Previous research on switched-capacitor DC-DC converters has focused on low-voltage and/or high-power ranges where the efficiencies are dominated by conduction loss. Switched-capacitor DC-DC converters at high-voltage (> 100 V) low-power (< 10 W) levels with high efficiency and high power density are anticipated to emerge. This paper presents a switched-capacitor converter with an input voltage up to 380 V (compatible with rectified European mains) and a maximum output power of 10 W. GaN switches and SiC diodes are analytically compared and actively combined to properly address the challenges at high-voltage low-current levels, where switching loss becomes significant. Further trade-off between conduction loss and switching loss is experimentally optimized with switching frequencies. Three variant designs of the proposed converter are implemented, and the trade-off between the efficiency and the power density is validated with measurement results. A peak efficiency of 98.6% and a power density of 7.5 W/cm^3 are achieved without heatsink or airflow. The characteristic impedance level of the switched-capacitor converter is an order of magnitude higher than previously published ones. The converter is intended for LED drivers.**

Index Terms—**DC-DC power converters, Gallium nitride, Silicon carbide, Switched capacitor circuits, Wide band gap semiconductors.**

I. INTRODUCTION

The demand for high efficiency and high power density power converters has progressed along with advances in industrial and consumer electronics, power conversion architectures, converter circuit topologies, and wide band gap semiconductor technologies. The size, weight, cost reduction demands of power supplies are the major drivers in the continuing miniaturization trend [1]. However, the decrease in volume could be attained only by simultaneous increase of the efficiency to maintain thermal limits for the maximum losses [2]. Therefore, increasing the efficiency is the primary development goal and the premise of the realization of smaller and lighter power supplies.

The applications such as light-emitting diode (LED) drivers for intelligent lighting systems and miniature chargers

for internet of things (IoT) are examples driving a continuous demand of reduction in volume of power converters. The converters driving LEDs are typically inductor-based converters, with operation ranges in voltage from a few volts [3] to tens of volts [4]. The power density of these converters can potentially be increased by integrating power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET) on integrated circuits (IC) [5]. For the LED drivers interfacing with rectified AC mains in the range of hundreds of volts, voltage conversion is needed to step-down the high-voltage level to a suitable level, with which the LED drivers can properly work. A possible way of achieving the voltage conversion is by stacking power converters or stacking certain parts of power converters, e.g. the inverter stages [6]. This paper is to present another approach, i.e. the voltage conversion is achieved with a high-voltage low-power switched-capacitor converter, which has not been previously demonstrated in the voltage and power level under consideration.

The switched-capacitor approach has been shown as an alternative way with respect to the inductor-based converters [7]. State-of-the-art switched-capacitor DC-DC converters that are implemented on IC chips are either limited by input voltages (≤ 12 V) or limited by output powers (≤ 2 W) [7]–[10]. To be simultaneously above both practical limits, low-voltage (≥ 12 V) high-power (≥ 100 W) switched-capacitor converters are commonly implemented with discrete components [11], [12]. However, at high-voltage (> 100 V) low-power (< 10 W) levels, design challenges are not the same as low-voltage designs, and high performance implementation remains a challenge. The conventional modelling of switched-capacitor converters [13] focuses only on conduction loss and is not adequate to analyse switched-capacitor converters at high-voltage levels [14], where switching loss related to charging and discharging the output capacitances of the switches becomes significant compared to charge transfer loss related to charging and discharging the energy transfer capacitors. Recent research shows switched-capacitor converters with input voltages up to 200 V and output powers in the range of 30–53 W [14], [15]. Switched-capacitor converters at even further higher characteristic impedance levels (higher voltage and lower current) with high efficiency and high power density are to be

demonstrated for potential applications such as LED drivers that are globally compatible with AC mains.

This paper presents a high input voltage (up to 380 V, e.g. compatible with European 220-240 Vrms AC operation with ±10 % tolerance) and low output power (up to 10 W) switched-capacitor DC-DC converter. To address the aforementioned challenges, wide band gap semiconductor devices, i.e. Gallium Nitride (GaN) switches and Silicon Carbide (SiC) diodes are combined and utilized to achieve high power density while obtaining high efficiency by trade-off between conduction loss and switching loss at high characteristic impedance (high-voltage and low-current) levels. Section II presents the proposed switched-capacitor DC-DC converter and its operation principle. Section III presents the design procedure and considerations. Section IV presents the experimental results of the converter with three variant designs, i.e. a high power density design, a high efficiency design, and a trade-off design between the other two. The optimization of the switching frequencies and the trade-off between the efficiency and the power density are experimentally validated. Section V concludes the paper.

II. SWITCHED-CAPACITOR DC-DC CONVERTER

The proposed high-voltage low-power switched-capacitor DC-DC converter is shown in Fig. 1. The converter has a voltage conversion ratio of 2:1 from the input to the output. The power stage of the converter consists of only eight components, i.e. two switches (Q1, Q2), two diodes (D1, D2), and four capacitors (C1–C4).

The operation of the switched-capacitor converter is distinguished in four states (S1–S4), as shown in Fig. 2. The contribution of this analysis is that the conventional 2-states analysis is not adequate to analyse the behaviour of the output voltage ripple, and the 4-states analysis clearly reveal that the output voltage ripple is at the double-frequency of the switching frequency with detailed charge and discharge transfer behaviour of the energy transfer capacitor C2.

The switching waveforms are shown in Fig. 3. The two switch/diode pairs Q1/D1 and Q2/D2 are in complementary operation with fixed 50% duty cycle. In general, the load current is primarily supplied by either charging or discharging the energy transfer capacitor C2. The sum of the voltages of the capacitors C1 and C3 equals to the input voltage, as a result, the capacitors C1 and C3 are always charged and discharged in the opposite directions.
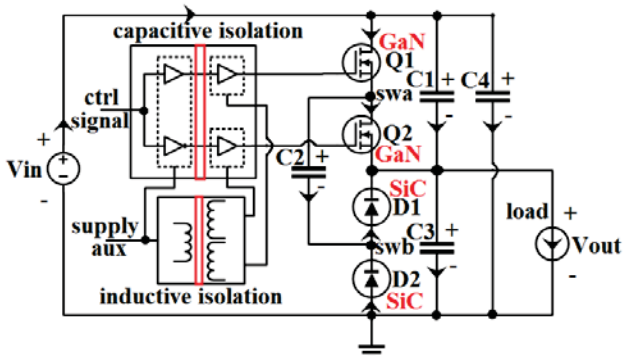

Fig. 1. Proposed switched-capacitor DC-DC converter, for high voltage low power applications with high efficiency and high power density.
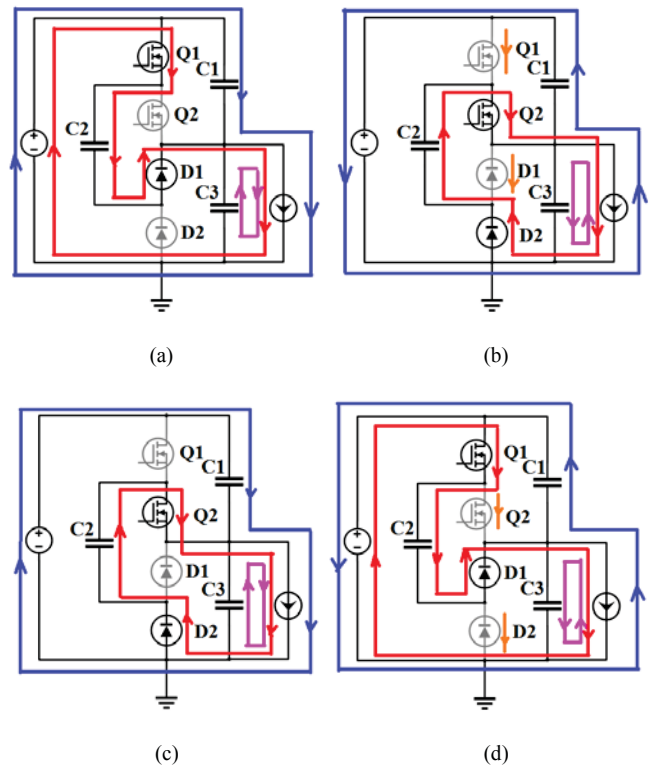

Fig. 2. Four operation states of the switched-capacitor DC-DC converter. (a) State S1. (b) State S2. (c) State S3. (d) State S4.
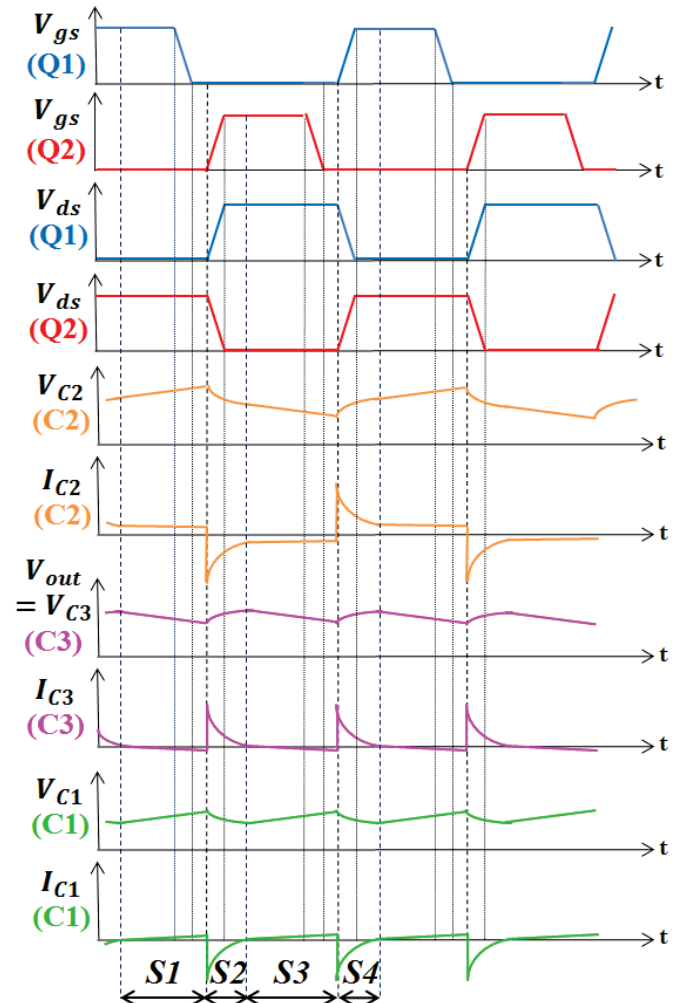

Fig. 3. Switching waveforms of the switched-capacitor converter (four operation states are indicated with S1-S4).

The operation principle of the four states (S1-S4) is elaborated as follows:

State S1: The switch/diode pair Q1/D1 is on. The input current mainly charges C2 and also charges C1, and C3 is discharged, thus the output voltage decreases.

State S2: The switch/diode pair Q2/D2 starts turning on. Small amount of current is needed to charge the parasitic output capacitances of Q1/D1. C2 is discharged to provide the load current and also charges C3, and C1 is discharged, thus the output voltage increases.

Stage S3: The switch/diode pair Q2/D2 is on. The load current mainly discharges C2 and also discharges C3, and C1 is charged, thus the output voltage reduces.

Stage S4: The switch/diode pair Q1/D1 starts turning on. Small amount of current is needed to charge the parasitic output capacitances of Q2/D2. C2 is charged while providing the load current and also charges C3, and C1 is discharged, thus the output voltage rises. Then next cycle begins.

The output voltage of the converter increases and then decreases for each of the 50% switching cycle when either Q1/D1 or Q2/D2 starts turning on. Therefore, the output voltage ripple has a frequency that is twice of the switching frequency f_{sw} of the control signals for driving Q1 and Q2.

$$f_{Vout\_ripple} = 2 \times f_{sw} \qquad (1)$$

For the energy transfer capacitor C2, in steady state, the average current of C2 is zero. However, the average of the absolute current of C2 equals the output DC current. These two currents are distinguished in (2) and (3), where T_s is the period of the control signals, i.e. $1/f_{sw}$.

$$I_{C2} = \frac{1}{T_s} \int_0^{T_s} i_{C2} \cdot dt = 0 \qquad (2)$$

$$|I_{C2}|_{avg} = \frac{1}{T_s} \int_0^{T_s} |i_{C2}| \cdot dt = I_{out} \qquad (3)$$

This is because the current of C2 is in opposite directions for each of the 50 % duty cycle, i.e. in one 50 % duty cycle, C2 is discharged to provide the load current, and in the other 50 % duty cycle, C2 is charged while providing the load current, as discussed above. To reduce conduction loss, it is the root mean square (RMS) current of C2 to be minimized, while the average of the absolute current of C2 is kept constant as the DC load current.

$$I_{C2\_RMS} = \sqrt{\frac{1}{T_s} \int_0^{T_s} |i_{C2}|^2 \cdot dt} \qquad (4)$$

The peak-to-peak voltage ripple of C2 can be calculated, and it is reversely proportional to the capacitance of C2 and the switching frequency f_{sw} of the control signals [16]. The capacitance and the switching frequency are the two major design parameters of the switched-capacitor converter, and it is to be discussed in more details in the next section.

$$\Delta V_{C2} = \frac{I_{out}}{2 \times C2 \times f_{sw}} \qquad (5)$$

From a generalized DC model of switched-capacitor converters [13], [17], [18], the output voltage of the converter can be expressed as follows.

$$V_{out} = \frac{V_{in}}{2} - I_{out} \times R_{out} \qquad (6)$$

TABLE I. SPECIFICATIONS OF THE CONVERTER.

Parameters	Specifications
Input voltage	300–374 V
Voltage conversion ratio	2:1
Maximum output power	10 W
Output voltage ripple	< 5 %
Efficiency	> 95 % above half rated power
Power density	> 4 W/cm^3

Therefore, the output voltage directly depends on the output load current. R_{out} is the equivalent (resistive) output impedance of the converter (only taking conduction loss into account), which also depends on the two major design parameters, i.e. the capacitance and the switching frequency.

III. DESIGN CONSIDERATIONS

A. Converter Specifications

The specifications of the DC-DC converter are shown in Table I. From the specifications, the characteristic impedance of the converter is considerably high (high-voltage low-current), which is proportionally to the square of the voltage for a given power. Note that both high efficiency and high power density are required for the converter. As previously discussed, a high efficiency is the primary development goal and the premise of a high power density. However, the requirement of the power density needs to be kept in mind through the development process. This is because higher efficiencies are fundamentally always possible by increasing the volume of the converter [2]. A good practice is to design with components and architectures that can address high efficiency and high power density at the same time. It should be mentioned that the characteristic impedance level of the converter is an order of magnitude higher than those of previously published switched-capacitor DC-DC converters with high efficiency and high power density.

B. GaN switches and SiC diodes

The emerging wide band gap semiconductors have superior properties, which have the potentials to enable both high efficiency and high power density. The components considered here are GaN switches and SiC diodes, for the specified voltage range.

First, the purpose of the diodes is to replace some of the transistor-switches in the switched-capacitor converter. This is theoretically analysed, i.e. by analysing the direction of the current flow in an all-transistor-switches switched-capacitor converter, a general switching-device that conducts negative current and blocks positive voltage may be suitable for diode implementation [13].

Second, the need of using both GaN switches and SiC diodes becomes clear when the comparison of the two devices is demonstrated with conduction loss, switching loss, gating loss, land pattern and total footprint area. The SiC diodes are non-controlled devices, and a fictitious all-diode-switches switched-capacitor converter is not feasible. Therefore, to implement the converter, it only needs to compare the two cases of either using all-transistor-switches or using the combination of switches and diodes. The comparison of GaN switch and SiC diode is summarized in Table II. The comparison mainly contains four parts: conduction loss,

switching loss, gating loss, and footprint area. The detailed comparison is described as follows.

Conduction loss: for low-voltage high-power applications, where conduction loss is the dominated loss, diodes may be considered to be replaced by synchronous rectification (SR) actively-controlled transistors to reduce the conduction loss and thus improve the total efficiency. However, the converter under discussion is for high-voltage low-power applications, and switching loss and gating loss are the major concerns. From Table II, a SiC diode indeed incurs higher conduction loss compared to a GaN switch, but under high-voltage (> 100 V) and low-current (< 100 mA) operation conditions, the conduction loss introduced by the forward voltage drop of the diode can be constrained at a minimal level. The loss of the converter under discussion is not conduction loss dominated.

Switching loss: from the datasheets, the GaN switch has an output charge of 10 nC and an output capacitance of 64 pF at 100 V, whereas the SiC diode exhibits a total capacitive charge of only 1.8 nC and a total capacitance of 10 pF at 100 V. Further calculated and estimated comparison is shown in Table II. SiC diodes largely reduce the output capacitance related switching loss, and facilitate fast switching transients, compared to the case if the converter is implemented solely with GaN switches, taking into account that SiC diodes as majority carrier devices need close-to-zero reverse recovery charge.

Gating loss: the SiC diode implementation eliminates the driver circuits (and the associated supply circuits) needed for driving GaN switches, thus the gating loss and the power consumption of the driver circuits are saved, and high power density can also be achieved.

Footprint area: at the component level, as shown in Table II, the SiC diode occupies more footprint area than the GaN switch. However, the development goal is to achieve a high power density of the total converter, not a single component. In fact, the GaN switch together with its driver circuits takes much larger footprint area than the SiC diode, which does not need any driving circuits. From a total converter point of view, the SiC diode can greatly save the footprint area and thus improve the overall power density.

As a result of the comparison of the GaN switch and the SiC diode, the combination of using both GaN switches and SiC diodes is preferred and proposed to achieve high efficiency and high power density of the switched-capacitor converter for high-voltage low-power applications.

The peak current handling capability of the GaN switches and the SiC diodes may be of concern and is briefly discussed here. From analysis and simulations, high peak currents conduct through the switches (and the corresponding diodes) to and from the energy transfer capacitor right after each switching event. The high peak currents get worse when low equivalent on-resistance devices such as the GaN switches and the SiC diodes are employed to reduce conduction loss. For this reason, the selected GaN and SiC devices have high ratios of peak-current to continuous-current ratings. The high forward surge current handling capability of the SiC diodes is enhanced by the Merged PIN Schottky (MPS) structure [19], evolved from the Junction Barrier Schottky (JBS) design.

TABLE II. COMPARISON OF GAN SWITCH AND SIC DIODE.

Parameters	GaN switch	SiC diode
Manufacturer	Efficient Power Conversion	Wolfspeed (Cree)
Part Number	EPC2012C	C3D1P7060Q
On-Resistance (Equivalent)	70 mΩ (at 5 V V_{GS})	260–880 mΩ (estimated)
Conduction Loss	$I_{RMS}^2 \times R_{on}$	$I_{RMS}^2 \times R_{on}$
Conduction Loss (Calculated)	0.11 mW* (at 40 mA I_{RMS})	0.42–1.41 mW* (at 40 mA I_{RMS})
Output Capacitance	50 pF (at 200 V V_{DS})	7 pF (at 200 V V_R)
Output Charge	15.7 nC (at 200 V V_{DS})	2.7 nC (at 200 V V_R)
Switching Loss (Capacitance Loss)	$Q_{OSS} \times \left(V_{in}/2\right) \times f_{sw}$	Zero (assume zero reverse leakage current)
Switching Loss (Calculated)	7.46 mW** (at 2.5 kHz f_{sw})	Zero (assume zero reverse leakage current)
Gate Charge	1.1 nC (at 200 V V_{DS})	Zero (no gate terminal)
Gating Loss	$Q_G \times V_{DRIVE} \times f_{sw}$	Zero (no gate terminal)
Gating Loss (Calculated)	0.01 mW** (at 2.5 kHz f_{sw})	Zero (no gate terminal)
Driver and Isolated Supply Loss	78.79 mW* (average value of measured prototype)	Zero (no driver or isolated supply needed)
Reverse Recovery Charge	Zero (no body diode)	Zero (majority carrier diode)
Total Loss (without Driver)	7.58 mW*	0.42–1.41 mW*
Total Loss (with Driver and Isolated Supply)	86.37 mW* (each GaN switch)	0.42–1.41 mW* (no driver or isolated supply needed)
Package Dimensions	1.711 mm × 0.919 mm = 1.57 mm^2	3.3 mm × 3.3 mm = 10.89 mm^2
Land Pattern (without Driver)	1.711 mm × 0.919 mm = 1.57 mm^2	3.6 mm × 3.6 mm = 12.96 mm^2
Land Pattern (with Driver and Isolated Supply)	1.57 + 5.00 × 5.00/2 + 15.24 × 12.00/2 mm^2 = 105.51 mm^2 ***	12.96 mm^2 (no driver or isolated supply needed)

*Depends on frequency, capacitance, load current, input voltage, output power, and parasitic resistances and inductances of packages and layout.
**Depends on frequency (to be experimentally optimized in next section).
***Half of driver and isolated supply land pattern is counted for each GaN switch for fair comparison, but additional footprint is further needed for local decoupling capacitors and dead time circuits for driving GaN switches.

C. Switching Frequency and Dead Time

As shown in Table II, the conduction loss, the switching loss, the gating loss, and hence the total loss of the converter depend on the switching frequency. The calculations and estimations in Table II serve as the initial design guide of the converter, and the switching frequency is to be experimentally optimized in the next section. The conduction loss is considered as frequency dependent here. This is because from the RMS current point of view, the RMS currents through the switches and the diodes depend on the switching frequency. In the frequency range of interest (about a few kilohertz), the switched-capacitor converter is insensitive to the dead time between the complementary control signals for driving the GaN switches. Therefore, the dead time may firstly be optimized, and then the optimization of the switching frequency is performed afterwards.

D. Capacitors Design

The design of the capacitors of the switched-capacitor converter starts with the capacitors C1 and C3. The voltage ratings of C1 and C3 need to be higher than the maximum input voltage, rather than the steady-state operation voltages. During the initial start-up phase, C3 may be fully discharged and/or not properly charged, and then C1 has to withstand the input voltage. By doing further failure analysis, if either the switch Q1 or Q2 breaks down as a short circuit, C3 has to withstand the input voltage, instead of the output voltage. C1 and C3 are firstly chosen to have a 450 V rating with a nominal capacitance value of 1 µF. The total capacitance of C1 and C3 needs to be designed high enough to keep the output voltage ripple at low levels, while considering that the effective capacitance of the 450V ceramic capacitors operating at 200 V is about the half of the nominal capacitance at zero DC bias voltage.

The design of C2 is to be shown as a trade-off between the efficiency and the power density, and its capacitance value is chosen to be several times larger than those of C1 and C3 to achieve high efficiency. To demonstrate the trade-off, C2 is designed with three capacitance values, i.e. 3 µF (high power density), 9 µF (high efficiency), and 6 µF (trade-off between the other two), all of which has a voltage rating of 250 V. In addition, C4 is a 0.22 µF 450 V capacitor to filter out higher-frequency noise of the input supply than the decoupling capability partly provided by C1 and C3.

After the voltage ratings and the capacitance values are determined, the quality factor and the energy density of the ceramic capacitors may be further improved by trade-off with temperature specifications [20], e.g. X7R (+125 °C ±15 %) may be relaxed to X6S (+105 °C ±22 %) or X7T (+125 °C +22/-33 %). All capacitors C1–C4 are chosen to be X7T type.

E. Driver and Isolated Supply

The power state design is now completed. However, driving the GaN switches in the proposed high-voltage converter is another challenge. From simulation results, the highest peak dv/dt of the switching transients may research 100 V/ns level. High dv/dt immunity is required for the high-side gate drivers of the GaN switches, to prevent the control signals from losing signal integrity and/or unexpectedly changing logic states. For a GaN switch above 100 V, more than 50 V/ns immunity is typically needed [21]. The state-of-the-art junction-coupled drivers, opto-coupled drivers, and transformer-coupled drivers have Common Mode Transient Immunity (CMTI) specified up to 50 V/ns (minimum) [22]. Therefore, the capacitive-coupled gate driver (Si8274GB1) with a CMTI of 150 V/ns (minimum) is selected. The capacitive isolation is achieved with semiconductor-based isolation barrier of the three-die architecture, and the control signals are transmitted in the form of RF on/off keying modulated signals [23]. Because the isolated output drivers are actually located on individual dies, independent supplies are needed for these driver outputs, and the inductive-isolated supply with dual independent outputs (R1DA) is used to fulfil this purpose. The comparison of different driver circuit topologies is analysed in [16]. The gate driver circuitry can be viewed as a floating half-bridge gate driver that is superposed on the converter output voltage.

IV. EXPERIMENTAL RESULTS

The prototype of the proposed converter is implemented with 2-layers PCB, which has 1 mm PCB-thickness and 2 oz copper-thickness. The PCB is designed complying with industry standard specifications such as track widths, spacing distances, and through-hole diameters. The components are located on both sides of the PCB, as shown in Fig. 4, to minimize the charge transfer loops and the power loops. The measurement test bench is shown in Fig. 5. The digital multimeter (34401A) and the power analyzer (PPA5530) are compared by calculating the sum of the reading error and the range error. For an input at 300 V and 20 mA, the total error of 34401A is ±12 mV, ±6 µA, ±0.034 % ($\Delta P/P$), and the total error of PPA5530 is ±136 mV, ±11.6 µA, ±0.103 % ($\Delta P/P$). For an output at 150 V and 40 mA, the total error of 34401A is ±9 mV, ±8 µA, ±0.026 % ($\Delta P/P$), and the total error of PPA5530 is ±106 mV, ±30.8 µA, ±0.148 % ($\Delta P/P$). The maximum absolute error of the efficiency measurement can then be calculated [2].

$$\Delta \eta = \eta \times \left(\frac{\Delta P_{out}}{P_{out}} + \frac{\Delta P_{in}}{P_{in}} \right) \qquad (7)$$

Assume an expected efficiency of 98 %, the maximum absolute errors of the efficiencies measured using 34401A and PPA5530 are 0.059 % and 0.246 %, respectively. Therefore, 34401A digital multimeters are used for the efficiency measurements. For the highest accuracy, the full 6½ digits resolution and the manual ranging of 34401A are used. For the low-power converter with high efficiencies, the measurement results are sensitive to the surrounding airflow. All efficiencies are measured at the room ambient temperature without any heatsink or airflow. The measurements are repeated for multiple times under the same conditions, and the measurement results are only counted when the data are reasonably repeatable.

Three variant designs with different nominal capacitance values of C2 are experimentally optimized for switching frequencies. The measured efficiencies versus switching frequencies with an input voltage of 374 V and the maximum output power of 10W are shown in Fig. 6. The optimization of switching frequencies is essentially the trade-off between the conduction loss and the switching loss (mainly the output capacitance related loss of the GaN switches), as discussed in the previous section.

After the switching frequencies are optimized for each design, the efficiencies of the power stage (without driver losses) are measured versus output powers and input voltages, as shown in Fig. 7. The efficiencies are generally higher with higher capacitance values. However, higher capacitance values mean larger volumes, and this fundamentally results in a trade-off between the efficiency and the power density.

The voltage conversion ratios are measured versus output powers and input voltages, and the results are shown in Fig. 8. The measurements are under the same conditions as the efficiency measurements in Fig. 7. The voltage conversion ratios are close to 2:1, as expected. The voltage conversion ratios increase with the output power and it is because the output voltages decrease with the output load current for given capacitance values and fixed switching frequencies. The theoretical relation is (6) in the previous section.

(a)

(b)

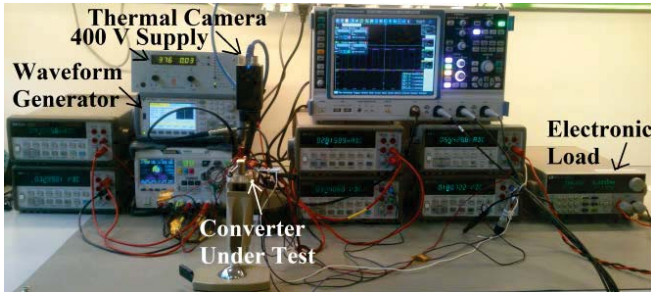Fig. 4. Prototype converter. Power stage components are highlighted. (a) Top side. (b) Bottom side.

Fig. 5. Measurement test bench. Keysight 33622A waveform generator is used for generating control signals. Delta Elektronika SM400-AR-4 power supply is used for input voltages. ITECH IT8812B Electronic load is used for load currents. FLIR A35 thermal imaging temperature sensor is used for taking thermal images of the prototype converter.
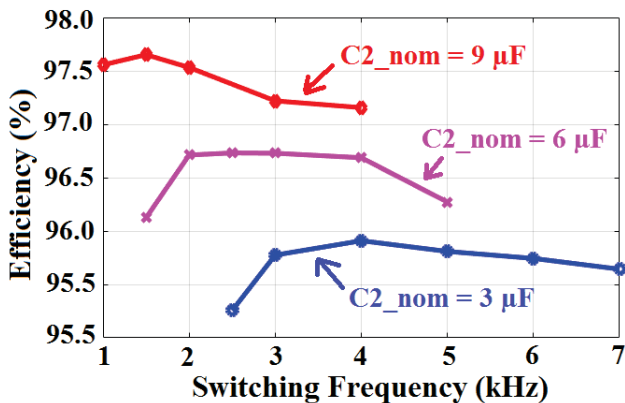

Fig. 6. Experimental optimization of switching frequency (trade-off between conduction loss and switching loss). Test conditions are 374 V input voltage and 10 W output power.
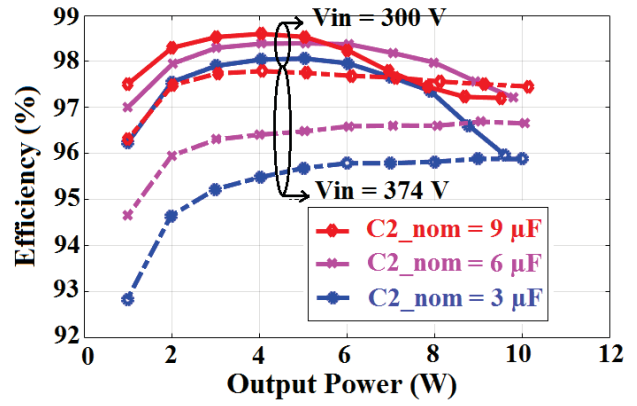

Fig. 7. Measured efficiency vs. output power (three variant designs with optimized switching frequencies: 3 µF/4 kHz, 6 µF/2.5 kHz, 9 µF/1.5 kHz).
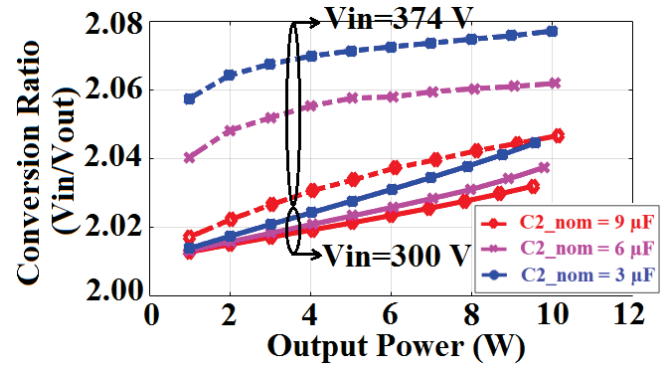

Fig. 8. Measured voltage conversion ratio vs. output power (three variant designs and the legends are the same as Fig. 7).
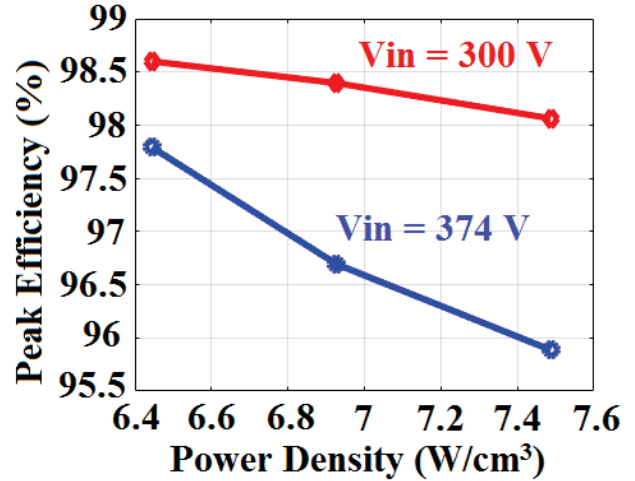

Fig. 9. Peak efficiency vs. power density (three variant designs).

TABLE III. PEAK-TO-PEAK OUTPUT VOTLAGE RIPPLE (MEASURED ABSOLUTE VOLTAGE AND CALCULATED PERCENTAGE).

| Output Power 10 W (Worst-Case)	Vin	Switching Frequency		
		1.5 kHz	2.5 kHz	4 kHz
C2_nom = 9 µF	300 V	3.085 V (2.06 %)	1.835 V (1.22 %)	0.896 V (0.60 %)
	374 V	2.030 V (1.09 %)	0.922 V (0.49 %)	0.371 V (0.20 %)
C2_nom = 6 µF	300 V	4.180 V (2.79 %)	2.325 V (1.55 %)	1.955 V (1.30 %)
	374 V	2.840 V (1.52 %)	1.420 V (0.76)	0.806 V (0.43 %)
C2_nom = 3 µF	300 V	5.630 V (3.75 %)	3.580 V (2.39 %)	2.125 V (1.42 %)
	374 V	4.400 V (2.35 %)	2.295 V (1.23 %)	1.056 V (0.56 %)
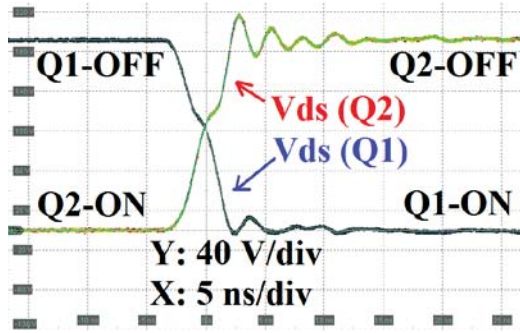
(a)
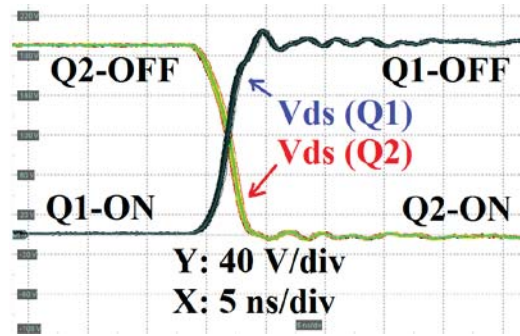
(b)

Fig. 10. Measured waveforms. Input voltage of the converter is 380 V. Both Q1 and Q2 are high-side switches. The ringing is partly reduced by the custom-made local ground connections for the oscilloscope probes. Due to the high density of the converter and double-side mounted components, the ringing is not completely removed when differential signals are measured with interactive signal-ground loops. The ringing is mainly parasitic effect and the ringing does not show up when single-ended signals are separately measured. (a) Q1-turn-on/Q2-turn-off transient. (b) Q2-turn-on/Q1-turn-off transient.
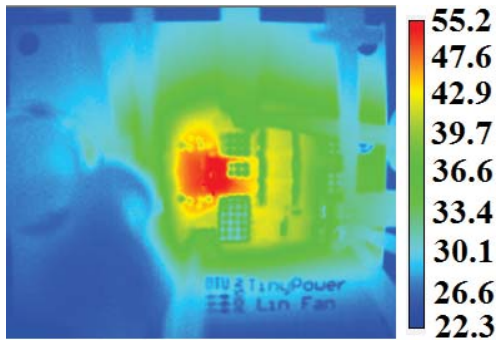
(a)
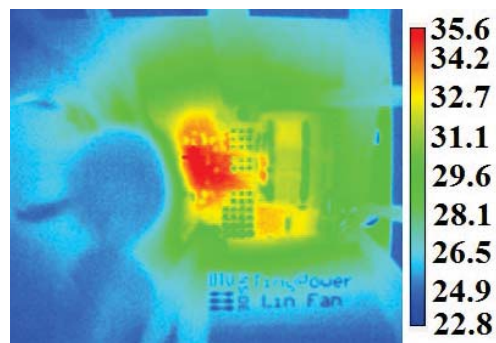
(b)

Fig. 11. Thermal images (°C) measured after one hour full-power operation, no heatsink, no airflow (annotated with output power, input voltage, nominal capacitance of C2, and switching frequency). (a) 10 W, 374 V, 3 µF, 4 kHz. (b) 10 W, 300 V, 9 µF, 1.5 kHz.

The peak efficiency versus the power density of the power stage is summarized in Fig. 9 for the three variant designs. The peak efficiencies of the high efficiency design (C2, 9 µF) are 98.6% and 97.8% at 300 V and 374 V input voltages, respectively. The high power density design (C2, 3 µF) reaches a power density of 7.5 W/cm^3 (123 W/inch^3), which is based on the boxed volume of the power stage (the white-boxes as shown in Fig. 4).

The peak-to-peak output voltage ripples are measured at the worst-case condition of the maximum output power of 10 W, for the three variant designs with different input voltages and switching frequencies. The results are summarized in Table III, and the bold numbers in green colour are measured when the designs are operated with the optimized switching frequencies. The worst-case peak-to-peak output voltage ripples are between 0.56 % and 2.06 % at the full load conditions. For a given design, the peak-to-peak output voltage ripples are higher with the input voltage of 300 V compared with the input voltage of 374 V, and it is because the load current is higher in the case of 300 V input voltage for a given output power of 10 W.

For the measured waveforms shown in Fig. 10, the Rohde & Schwarz RTO-1024 2-GHz oscilloscope and the RT-ZP10 500-MHz single-ended passive probes are used for the measurements. The measured average slew rates of the high-side GaN switches (Q1 and Q2) are about 40–50 V/ns.

The thermal images of the prototype converter are shown in Fig. 11, at the maximum output power of 10 W after one hour operation without heatsink or airflow. The heat density is high around the GaN switches due to the limited available copper area connecting the small land patterns of the devices to conduct currents and heat.

V. CONCLUSIONS

A high-voltage low-power switched-capacitor DC-DC converter is designed, implemented and validated with experimental results. The GaN switches and the SiC diodes are analysed, combined and utilized to properly address the challenges at high-voltage and low-power levels. The trade-off between the conduction loss and the switching loss is optimized with switching frequencies. Three variant designs with the trade-off between the efficiency and the power density are experimentally validated. A peak efficiency of 98.6% and a power density of 7.5 W/cm^3 (123 W/inch^3) are achieved, without any heatsink or airflow. The converter is intended for applications such as LED drivers.

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