Hardware-in-the-Loop Test for Automatic Voltage Regulator of Synchronous Condenser

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Hardware-in-the-Loop Test for Automatic Voltage Regulator of Synchronous Condenser

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Abstract—Automatic voltage regulator (AVR) plays an important role in volt/var control of synchronous condenser (SC) in power systems. Test AVR performance in steady-state and dynamic conditions in real grid is expensive, low efficiency, and hard to achieve. To address this issue, we implement hardware-in-the-loop (HiL) test for the AVR of SC to test the steady-state and dynamic performances of AVR in different operating conditions. Startup procedure of the system and voltage set point changes are studied to evaluate the AVR hardware response. Overexcitation, underexcitation, and AVR set point loss are tested to compare the performance of SC with the AVR hardware and that of simulation. The comparative results demonstrate how AVR will work in a real system. The results show HiL test is an effective approach for testing devices before deployment and is able to parameterize the controller with lower cost, higher efficiency, and more flexibility.

Keywords—Automatic voltage regulator, hardware-in-the-loop, synchronous condenser, real time digital simulator.

I. Introduction

WITH continuously increasing penetration of converter-based generation and the simultaneously reduced system inertia, the system dynamic characteristics significantly change. The challenges brought about calls for high reliability and functionality of the equipment and their control systems. As a consequence, verification and testing of those elements are becoming more important. Synchronous condenser is seen as viable solution to smooth the transition from synchronous plant to renewable generation plant in use of massive power converters [1], [2]. The automatic voltage regulator (AVR) is concerned as a core control component of SC to fulfill the reactive power support functions. AVR test on real SC plants before running real-world diagnostics on the complete system is highly costly and inefficient. Off-line test for AVR performance in steady-state and dynamic conditions is limited to the system conditions.

Hardware-in-the-loop (HiL) test represents a bridge between pure simulation and complete system construction by providing an efficient real-time and safe environment. Tests can focus on the functionality of the controller and verify all dynamic conditions of the system. HiL is recognized as an effective approach for testing devices before deployment, which is able to solve the issue of physical controller test with lower cost, higher efficiency, and more flexibility. HiL allows the implementer to conveniently implement complicated control algorithms, system conditions and safely modify them.

In recent years, HiL technology has been applied to develop controls and components with healthy and faulty conditions in power grid, automotive industry, transportation, and other sectors to overcome the drawback of low accuracy in a pure simulation. In general, it can be classified into two main categories. The first HiL called control HiL (CHiL) that allows the physical control device can be connected in closed-loop with the power system model [3]–[9]. The closed-loop interaction of CHiL system and the grid model provides insight on both the performance of the control strategy and its effect on the network. The interfaced signals between the CHiL and the simulator are low-power control signals that are often within the range of ± 10 V, 0-100 mA, and commercial digital/analog converters. The second one namely power HiL (PHiL) is an extension of CHiL which is capable of exchange current and voltage signals according to the power of an external equipment [10], [11].

In [3], a photovoltaic (PV) control system is implemented CHiL test to evaluate the control method in dynamic conditions. Using dSPACE real-time simulation for verifying the field oriented control approach of permanent magnet synchronous motor is studied in [4]. In [5], CHiL test for an excitation control system of a synchronous generator using external stabilizing signals to improve oscillation damping is investigated. CHiL test of a complete control and protection system for a modular multilevel converter-based unified power flow controller coupled with Opal real-time simulator is studied in [6]. Furthermore, an application of CHiL test for AVR of synchronous generator based on identification model interfaced with real-time LAB is implemented in [7]. A maximum power point tracking control based on a polynomial fuzzy model is investigated in [8] to evaluate the performance and efficiency of the control strategy in the PV generation. A CHiL simulation of a permanent magnet synchronous motor under healthy and faulty conditions is proposed in [9] which proves that CHiL is a safe and relatively inexpensive environment for developing fault detection and diagnostic algorithms.

A PHiL application for a dynamic electric PV model integrated to a five-layer thermal model is investigated to verify the dynamic condition during various load changes [10]. In addition, a PHiL simulation for the megawatt-scale motor drives is implemented in [11] to validate the device during different disturbances.

In this paper, a CHiL is implemented for testing AVR systems of SC in steady-state and dynamic conditions. The

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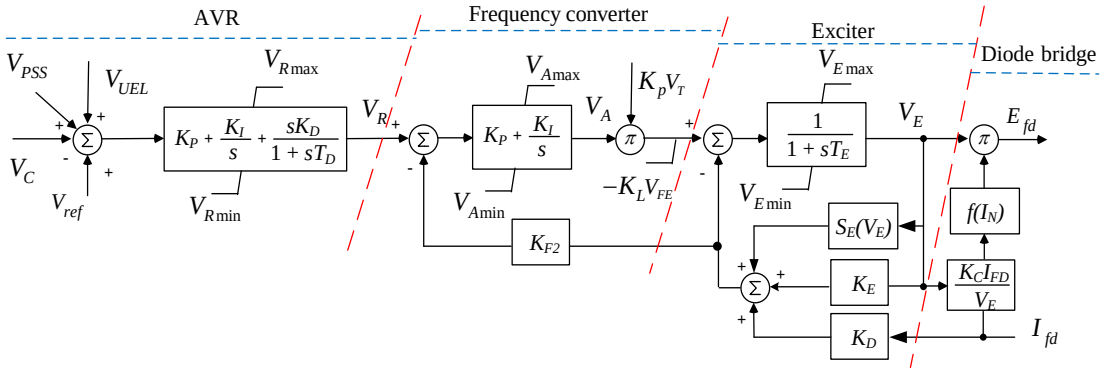


Fig. 1. IEEE AC7B excitation system [3].

grid and SC are modeled in real time digital simulator (RTDS) interfaced with AVR hardware platform under different operating conditions to examine and compare how the actual and simulated AVR systems react. The overexcitation, underexcitation, and AVR set point loss are implemented to evaluate the control function of AVR system satisfying requirements that are difficult and complicated to implement in the real machines.

The rest of the paper is organized as follows. Section II presents the configurations of AVR model that is implemented in hardware. The system configuration and HiL setup are investigated in section III. In section IV, the comparative results between the actual AVR system response and that of simulation under different scenarios are discussed and analyzed. Some important conclusions are finally drawn in section V.

II. AVR MODEL

The AVR system is modified based on PID controller of AVR model of IEEE AC7B excitation system model as shown in Fig. 1) [12]. AVR detects the terminal voltage of SC through voltage compensator and transforms the signal to V_C, and then compare with the reference voltage V_{ref}. The deviation e between these two values works as the input for PID control to create the AVR output V_R:

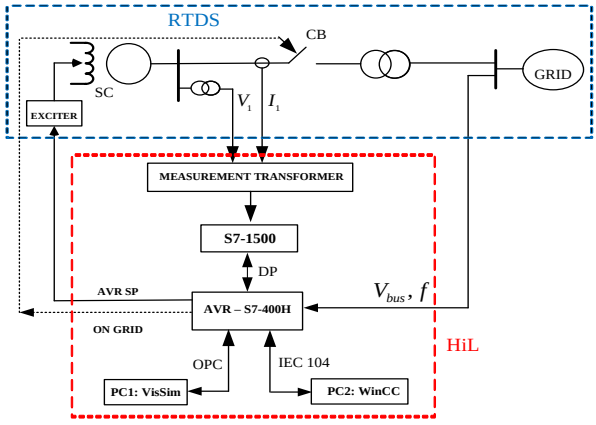
$$V_R = K_P e + K_I \int_0^t e + K_D \frac{\mathrm{d}e}{\mathrm{d}t} \tag{1}$$

where K_P, K_I, and K_D are the proportion, integral, and differential gains of the PID control, respectively.

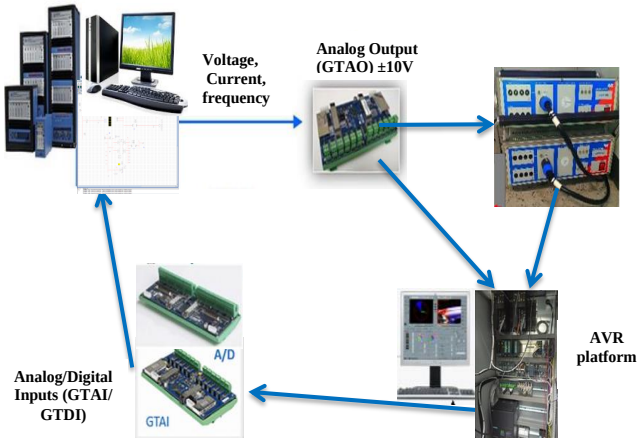
When there is a difference between V_C and V_{ref}, PID control immediately react to correct the deviation. The higher the K_P is, the faster the correction is. However, a large K_P can cause a large oscillation in the output. The static error of terminal voltage is eliminated by the integral function. The lower K_I is, the smaller overshoot the output obtains, however, the system may experience more oscillations during the dynamic period. The differential function improves the disturbance rejection ability, but it may bring the noise of the input to the output. A low-pass filter ($\frac{1}{1+sT_D}$) is usually added for the derivative term to cancel the noise.

The value of V_R is converted to a percentage as the AVR set point sending to the frequency converter of the excitation system as shown in Fig. 1. The overexcitation, underexcitation, and V/Hz limiters are implemented HiL as well. The frequency converter, exciter, and diode bridge parts are implemented in RTDS with SC and the grid models.

III. SYSTEM CONFIGURATION AND HIL SETUP



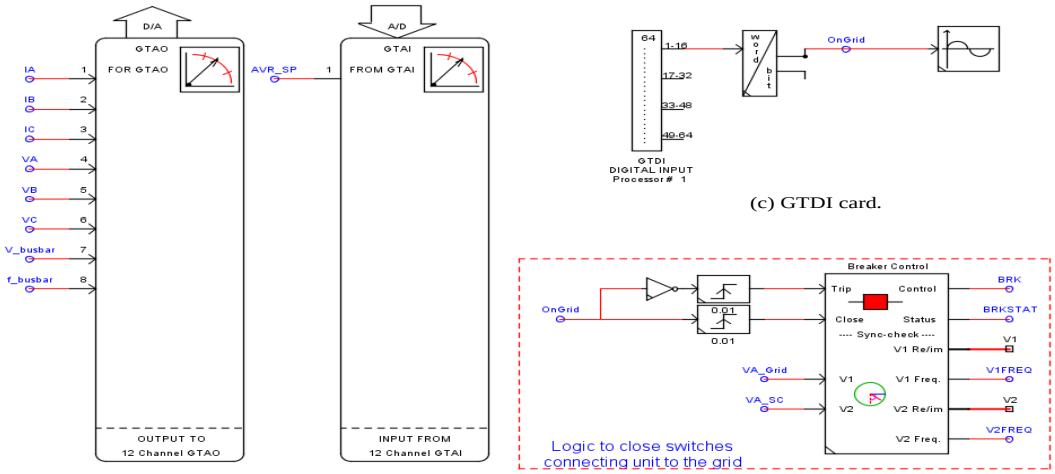
(a) The system diagram with AVR HiL.



(b) AVR hardware testing setup.

Fig. 2. Hardware in the loop testing setup for AVR system.

Figure 2 presents the configuration diagram of system interfaced with hardware-in-the-loop test of AVR. The entire



(a) GTAO card. (b) GTAI card. (c) GTDI card. (d) Circuit Breaker logic.

Fig. 3. Sending and receiving signal setup for GTAO, GTAI, GTDI, and circuit breaker in RTDS. (a) Sending signals to GTAO card. (b) Receiving signals from GTAI card. (c) Receiving signals from GTDI card. (d) Circuit breaker logic.

grid and SC model is simulated in RTDS with the dash blue bound, while AVR system is implemented HiL with the dash red one. RTDS sends three-phase current and voltage of the generator side, and busbar frequency and voltage of the grid side to HiL, whereas HiL transfers AVR set point (AVR SP) and ON GRID signal to RTDS.

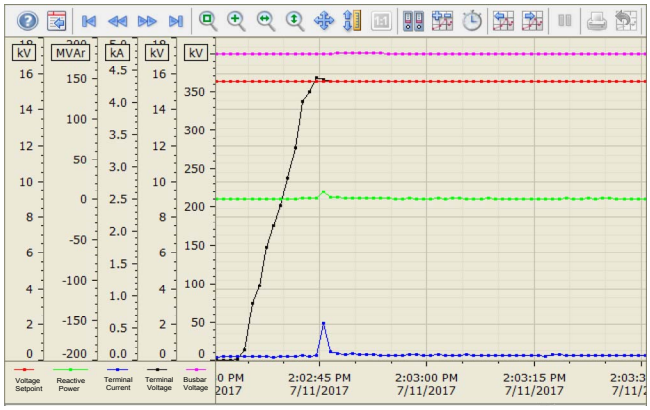


Fig. 4. SC response with AVR hardware during the startup period.

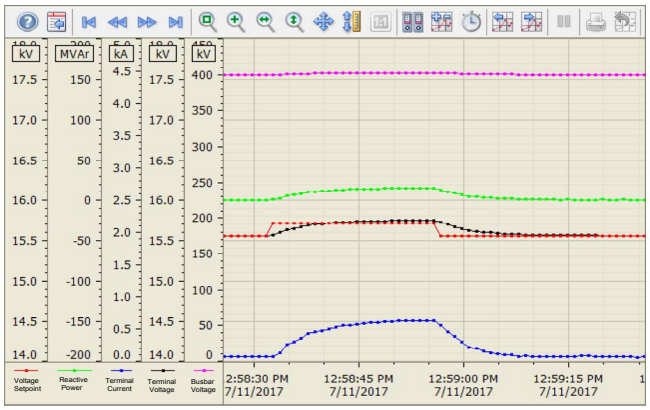


Fig. 5. SC response with AVR hardware during the voltage set point changes.

RTDS receives and sends their analog and digital signals to HiL through Giga Transceiver I/O cards (GTIO) that include Giga Transceiver Analog Input/Output cards (GTAI/GTAO) and Giga Transceiver Digital Input/Output cards (GTDI/GTDO) [13]. The GTAO/GTAI cards include twelve analog output/input channels with an output/input range of $\pm$10V. The GTDO/GTDI cards include 64 optically isolated digital output/input channels which are arranged into two banks of 32 channels each. Each bank of 32 channels may be operated at a voltage level in the range of +5V DC, if the external device output signal is out of the range, a variable resistor must be used to get the proper voltage value. The simulation time step of SC and grid in RTDS is set equal to 60 μs.

The sending and receiving analog and digital signals of RTDS and AVR hardware are shown in Fig. 3. With terminal voltage and current outputs of SC from RTDS after through measurement transformers are 115 V and 5 A which are out of acceptable range of GTAO card. Consequently, a scaling ratio is implemented inside of GTAO card to get the proper value send out through the card as shown in Fig. 3(a). However, the analog input of external device requires other ranges which are 1 A for the current and 100 V for the voltage corresponding to their nominal values. A power amplifier is therefore used to satisfy the HiL required values as shown in Fig. 2(b). On the contrary, the frequency and voltage of busbar through scaling ratios inside of GTAO card are sent directly to the hardware. The ON GRID signal with 24 VDC sending to RTDS is out of range of GTDI card, a resistor works as a voltage divider is implemented to get a 5 VDC signal for GTDI card. Furthermore, AVR set point operates at a range from 0 to 150 % corresponding to 0 to 10 VAC is sent to RTDS via GTAI as shown in Fig. 3(b).

The AVR system based on the AVR model of IEEE AC7B excitation system model is programmed in VisSim software in PC1 and then transferred to PLC S7-400 through OLE for Process Control (OPC) standard. PC2 using WinCC communicate to S7-400 via IEC 104 standard for supervisory control

and data acquisition purpose.

The main components of HiL consist of two programmable logic controller (PLC) S7-1500 and S7-400H, and two measurement transformers. Three-phase 100 VAC voltage and 1 AAC current outputs from the OMICRON power amplifier is sent directly to the measurement transformers, these voltage and current outputs transfer to S7-1500, after storing and processing these signals, S7-1500 communicates with S7-400H where AVR programmed via Profibus Decentralized Periphery (DP) protocol sends the terminal voltage and current of SC.

IV. Test results

In order to verify the performance of AVR, different tests are implemented in this section. Firstly, a start-up procedure of AVR hardware is described step by step. After that, underexcitation and overexcitation tests are studied. Finally, an AVR SP loss incident is investigated. Comparison is provided on the responses of the AVR in hardware and the simulation.

A. AVR start-up procedure

To start up the system, real time simulation is first start in RTDS without the SC connection, after that the voltage and frequency of the busbar at the grid side are sent to the AVR. The starting up process of SC is modelled in the hardware platform, where a virtual SC is turned and accelerated to its full speed. When the virtual SC reaches the full speed, the excitation is on and AVR SP is sent from the AVR to the RTDS model that is proportional to the corresponding busbar voltage of the grid side. When the terminal voltage of the generator hits the set point, an ON GRID digital signal is sent to the circuit breaker (CB) of the RTDS. CB checks the synchronization by checking the voltage magnitude and phase differences of the SC side (VA_SC) and the grid side (VA_Grid) as shown in Fig. 3(d). When their differences are within a certain level CB is closed and the SC model in RTDS is connected to the grid.

Figure 4 shows the busbar voltage (pink), the reactive power (green), the terminal current (blue), the voltage set point (red) and the terminal voltage (black) of SC responses during the startup period. The terminal voltage of SC increases gradually for 0 to its voltage set point (red) within 10 s when the excitation system activates. It is worth to mention that thank to the synchronization check of CB, the reactive power and the terminal current experience a small overshoot during the SC synchronization.

B. Voltage set point change

To verify the response of AVR hardware, a manual change of SC voltage set point is implemented to see how the actual terminal voltage track to its set point in dynamic conditions. Figure 5 shows the SC responses and busbar voltage during a 0.045 pu step increase and decrease of SC voltage set point (red). It can be seen clearly that when the set point increases/decreases, the terminal voltage tracks quite well to its set point with no overshoot during transient periods. It takes approximately 7s to settle down when the set point changes. Furthermore, the reactive power (green), the current (blue) of SC and the busbar voltage (pink) respond quickly and very smoothly during the set point changes.

C. Underexcitation test

In this test, the voltage of the grid side suddenly increases from 1 pu to 1.1 pu at t = 1.7 s, SC tries to absorb reactive power from the grid side to lower the voltage. The comparative results between AVR controller of HiL and that of simulation are shown in Fig. 6 with blue curves for hardware and orange ones for simulation.

As can be seen in Fig. 6, the reactive power of AVR simulation has a smoother response and shorter settling time than that of hardware: approximately 15.3 s and 4 s, respectively. However, with AVR hardware, SC can absorb more reactive power which reaches -142 Mvar instead of -126 Mvar in simulation with the same underexcitation limit setting. As a result, the voltage of SC and the grid have a longer recovery time and higher overshoot but lower over-voltage value after the incident with hardware results. It can be explained that with hardware test, it takes time to transfer the measurement signals from RTDS to the hardware platform and the reversed direction while there are almost no either time delay or sending/receiving time for that of simulation.

It is noteworthy that the active power responses of AVR hardware and simulation are almost similar because the AVR controller seems insensitive to electric power.

D. Overexcitation test

A sudden decrease of the grid voltage from 1 pu to 0.9 pu occurs at t = 1.7 s, as shown in Fig. 7. From the comparative results with simulation and hardware of AVR, the reactive power support of AVR hardware is slower but higher than that of simulation which makes SC terminal voltage and the grid voltage hit lower minimum magnitudes during the transient period but higher recovery values after the incident.

The reactive power of AVR simulation increases from around 2 Mvar at the initial value to nearly 125 Mvar within 1.5 s, whereas that of hardware with the same interval is within 7 s and increases further to reach approximately 150 Mvar after about 18 s. The settling time of AVR hardware for reactive power and voltage is approximately 18 s much longer than that of AVR simulation around 2 s.

The active power responses are almost similar in terms of magnitude and settling time for both of two approaches.

E. AVR set point loss

An AVR set point loss incident occurs at t = 1.7 s, SC loses excitation and it tries to draw the reactive power from the grid to operate at the synchronous speed and maintain its terminal voltage. Figure 8 shows how HiL and simulation of AVR respond during the incident. The voltage and reactive power responses are similar for AVR hardware and simulation while there is a difference in the active power response. The reactive powers of both of them reach -123 Mvar within 10 s.

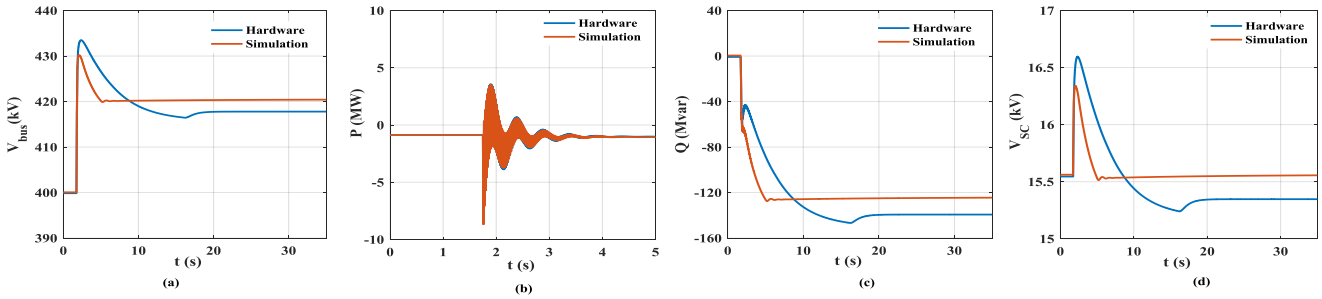


Fig. 6. Underexcitation responses. (a) High-level voltage of SC side. (b) Active power of SC. (c) Reactive power of SC. (d) Terminal voltage of SC.

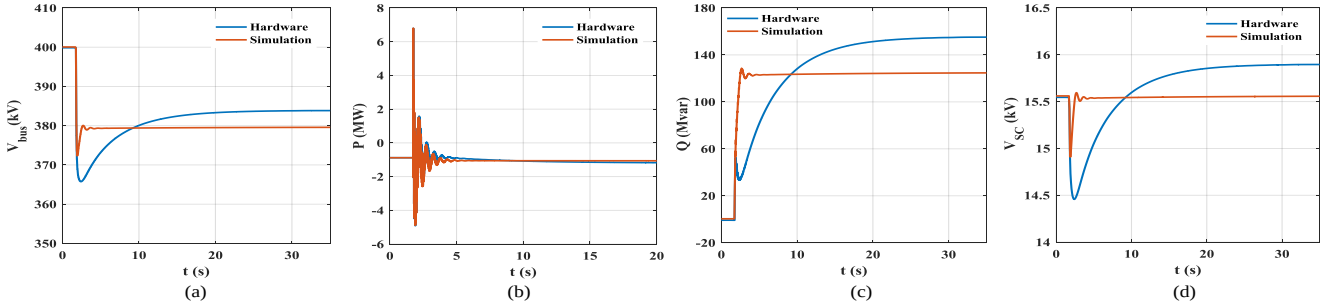


Fig. 7. Overexcitation responses of SC. (a) High-level voltage of SC side. (b) Active power of SC. (c) Reactive power of SC. (d) Terminal voltage of SC.

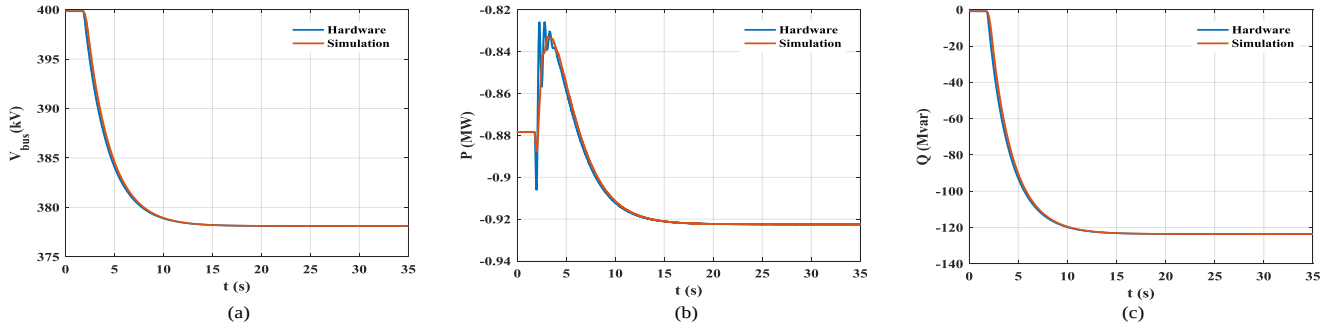


Fig. 8. Dynamic responses of SC during AVR SP loss. (a) High-level voltage of SC side. (b) Active power of SC. (c) Reactive power of SC.

The active power of AVR hardware undergoes more oscillation than that of simulation but settle down at almost the same time during the incident.

V. Conclusion

The paper reports an implementation of the hardware-in-the-loop test for AVR that is one of core components of SC for keep voltage stability purpose. An interface of AVR hardware with SC and the grid models in RTDS and HiL setup is presented. Startup procedure of the system, AVR hardware test, and voltage set point changes are studied to evaluate how the simulation responds to the AVR hardware. Furthermore, underexcitation, overexcitation, and AVR set point loss are implemented as tests to compare the different responses in terms of the overshoot and settling time of AVR hardware and simulation. The comparative results provide a good experience to test and evaluate the AVR control before working in reality. It also demonstrates the possible applications of HiL to validate and adjust the control function of the equipment in steady state and dynamics conditions before final construction implementation with lower cost, higher efficiency, and more flexibility.

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