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### Very High Frequency Galvanic Isolated Offline Power Supply

Pedersen, Jeppe Arnsdorf; Knott, Arnold; Andersen, Michael A. E.

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Jeppe Arnsdorf Pedersen

# Very High Frequency Galvanic Isolated Offline Power Supply

Ph.D. Dissertation, January 2017

**DTU Electrical Engineering** Department of Electrical Engineering

Jeppe Arnsdorf Pedersen

# Very High Frequency Galvanic Isolated Offline Power Supply

Ph.D. Dissertation, January 2017

#### Author:

Jeppe Arnsdorf Pedersen

### Supervisors:

Arnold Knott	—	DTU Elektro, Electronics Group
Michael A. E. Andersen		DTU Elektro, Electronics Group
Thomas Andersen		Nordic Power Converters

Department of Electrical Engineering Electronics Group Technical University of Denmark Elektrovej building 325 DK-2800 Kgs. Lyngby Denmark

www.ele.elektro.dtu.dk Tel: (+45) 45 25 38 00 Fax: (+45) 45 88 01 17 E-mail: hw@elektro.dtu.dk

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# **Preface and Acknowledgment**

This thesis is submitted in partial fulfilment of the requirements for obtaining the Ph.D. degree from the Technical University of Denmark. The research has been carried out at the Electronics group, Department of Electrical Engineering between the December 2013 and January 2017, under the supervision of associate prof. Arnold Knott, prof. Michael A.E. Andersen and Thomas Andersen.

The Ph.D. project titled Very High Frequency Galvanic Isolated Offline Power Supply was funded by Technical university of Denmark (DTU). The research was conducted in close collaboration between DTU Electrical Engineering and Nordic Power Converters.

During the project, a 3.5 month external research stay was conducted at the Electronic and Electrical Engineering department, at the University of Sheffield, England.

The last three years as a Ph.D. student have been filled with good experiences and have introduces me to many interesting people. I wish to thank all who shared their technical knowledge and in any way helped me along the way.

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During the last decades many researchers have turned their attention to raising the operation frequency of power converters to the very high frequency (VHF) range going from 30 MHz to 300 MHz. Increasing the operating frequency of a power converter leads to smaller energy storing components and hence smaller volume. The smaller volume comes from the passive components that scales inversely with frequency, and thereby decrease in value and size as the frequency is increased. Air-core magnetics are the preferred choice for VHF converters as there is no core losses and the selection of magnetic materials are still very limited. Ceramic capacitors are very suitable for VHF converters and with new semiconductor materials, this area will only grow in the near future.

Increasing the frequency to the VHF range also increases the switching losses, therefore soft switching techniques are used to eliminate the switching losses. The topologies used, are inspired by radio frequency amplifiers, which are used to generate high frequency current for an antenna. In VHF converters this antenna is replaced by a rectifier to generate a DC voltage. Driving these type of converters can be a challenge as hard gating of traditional silicon MOSFETs generates losses that are frequency depended. Several soft gating solutions have been presented that limit the losses at these frequencies. In this thesis, one gate drive solution is described and used for multiple implemented converters. The gate drive is self-oscillating and consists of a few passive components ensuring a low cost. This gate drive is used as both a low side gate driver for an inverter and a synchronous rectifier in a bidirectional converter achieving a peak efficiency of 80% at 37 MHz. This gate drive is also implemented with a coupled inductor to drive a half-bridge based converter achieving 81% efficiency at an input voltage of 80 V.

The subject of this thesis is off line VHF converters, which means input voltages of several hundred volts. As most VHF topologies have relatively high voltage stresses with peak voltages reaching multiple times the input voltage, the resonant currents needed to achieve soft switching will generate high AC losses. A solution to this problem is presented in this thesis where several inverters have their input connected in series to split the high input voltage. An off-line converter build for the US mains is presented build with three inverters with a single combined rectifier. The converter designed to deliver 9 W to a 60 V LED load and is achieving an efficiency of 89.4% and a power density of 2.14  $\frac{W}{cm^3}$ . The development of this converter proof that offline VHF converter can be implemented with high efficiencies even for low power applications.

VHF converters are also subject to EMC regulations and the need for galvanic isolation as well as other standards. Galvanic isolation is usually implemented with transformers, however as mentioned earlier there are only limited magnetic materials for the VHF range. In this thesis PCB transformers are described together with the possibility of using capacitors as the power galvanic isolation, both methods of creating galvanic isolation are implemented in converters. Regarding EMC a series of converters with different filter implementations are examined. The results from the conducted measurement from 150 kHz to 30 MHz shows no peaks as the switching frequency is above the measured range. However, the radiated measurement shows high peaks with no filter, these peaks are reduced to 6 dB below the limits from EN 55022 with filtering and a EMC shield. The filter component scales with frequency, and therefore the implemented filter were still small compared to a traditional EMC filter.

Due to the high frequencies of VHF converters it is difficult to use traditional pulse width modulation (PWM) control, instead the most used are burst mode (on/off) control which can be implemented with commercial available controllers. A new implementation of burst mode together with a self-oscillating gate drive is presented.

Another approach is frequency control where the switching frequency is controlled in respect to the output or input. A converter topology is analyzed with the first harmonic approach to evaluate the operation, and to create a new frequency control method to ensure a good power factor (PF). A prototype is implemented with the frequency control method, which achieves a PF of 0.99 and a THD of 5.68%. This is for a converter, switching at traditional frequencies, however the same method can be used for VHF converters.

During this Ph.D. thesis, different areas of an offline VHF converters are described, during the project different areas have been investigated such as, gate drive, synchronous rectifiers, PCB transformers, control of a resonant converter, galvanic isolation, EMC performance, power factor and stacking of converters. I løbet af de sidste årtier er interessen for at øge skifte frekvensen af strømforsyninger til det "meget høje frekvens" (VHF) område steget markant, VHF frekvensområdet spænder fra 30 MHz til 300 MHz. En øget skiftefrekvens medføre at mindre energi skal lagers i hver periode og derved mindskes værdierne af de passive komponenter. De lavere værdier resulterer i mindre volumen af de passive komponenter. Reduktionen skalerer inverst med frekvensen, hvorved man opnår en reduktion i størrelse hvis frekvensen øges. De passive komponenter består bl.a. af luftspoler. Luftspoler er det foretrukne valg for VHF konvertere, da man undgår kerne tab, ydermere er udvalget af magnetiske materialer der virker ved høje frekvenser meget begrænset. Keramiske kondensatorer er meget velegnet til VHF konvertere, og de er også at fortrække til VHF konvertere, grundet deres høje selvresonans. Med komponenter lavet af nye halvledermaterialer, hvis udvikling stadig er i tidlige stadier, vil forskningen i VHF konvertere kun vokse i den nærmeste fremtid.

Ved at øge skifte frekvensen til VHF området øges skiftetabene også, derfor benyttes "soft switching" teknikker der reducere skiftetabene betydeligt. De anvendte topologier er inspireret af radioforstærkere, som anvendes til at generere et højfrekvent signal til en antenne. I VHF strømforsvninger er antennen erstattet af en ensretter der genererer en DC spænding. Denne type konvertere kan ikke drives med traditionelle gate drivere da gate tabene bliver for store. Derfor benyttes resonante gate drive hvis tab ikke er frekvensafhængige. I denne afhandling præsenteres en ny gate drive løsning til VHFkonvertere, denne løsning blev brugt i alle de implementerede VHF strømforsyninger. Dette gate drive er selvsvingende og består udelukkende af passive komponenter, hvilket sikrer en lav pris. Gate driveret blev igennem denne afhandling brugt i flere invertere, heriblandt en resonant halvbro inverter. Det blev yderligere brugt til at lave en tovejs-konverter med synkron ensretter. Denne konverter opnåede en effektivitet på 80% med en skiftefrekvens på 37 MHz. Dette gate drev blev også implementeret med en koblet luftspole til at drive en halvbro baseret konverter. Denne konverter opnåede en effektivitet på 81% ved en indgangsspænding på 80 V. I afhandlingen er muligheden for udvikle VHF strømforsyninger til lysnettet blevet undersøgt. De fleste VHF topologier har relativt høje spændingsbelastninger på de aktive komponenter, som regel med maks spændinger på flere gange indgangsspændingen. De nødvendige resonante strømme for at opretholde "soft switching" vil derfor generere store AC tab, hvilket vil resultere i lav effektivitet for lave udgangseffekter. I afhandlingen er en løsning på dette problem er præsenteret, hvor flere invertere har deres indgang forbundet i serie for at opdele den høje indgangsspænding. En strømforsyning bygget til amerikanske AC spændinger præsenteres, den er opbygget af tre invertere og en enkelt ensretter. Strømforsyningen er designet til at levere 9 W til en 60 V LED. Forsyningen opnår en effektivitet på 89,4% og en effekttæthed på 2,14  $\frac{W}{cm^3}$ . VHF konvertere er omfattet af en række standarder inklusiv "Electromagnetic Compatibility" (EMC) regulativerne og behovet for galvanisk isolation. Galvanisk isolation bliver normalt implementeret med transformatorer, men som tidligere nævnt er der få magnetiske materialer til rådighed det virker i VHF området. I denne afhandling bliver "Printed Circuit Board" (PCB) transformatorer samt muligheden for at bruge kondensatorer som galvanisk isolation beskrevet. Begge metoder til at skabe galvanisk isolation er også blevet implementeret i forskellige strømforsyninger. For at undersøge VHF konvertere i forhold til EMC kravene er en række konvertere blevet målt med forskellige filter implementeringer. Resultaterne viste at der ikke er nogen problemer i "conducted" målingerne. Men ved måling af den udstrålede støj ses høje peak værdier uden filter. Disse er reduceret til 6 dB under grænseværdierne fra CISPR 22 med filtrering og et EMC-skjold. På grund af de høje frekvenser i VHF konvertere er det vanskeligt at anvende pulsbreddemodulation (PWM) til kontrol, i stedet benyttes burst mode (tænd/sluk) kontrol, som kan implementeres med kommercielt tilgængelige controllere. Et alternativ til dette er er frekvensstyring hvor skiftefrekvensen styres på baggrund af indgangs eller udgangs spændingen. En konverter topologi blev analyseret ved hjælp af "the first harmonic approach" (FHA) for at få en matematisk model af operationen. Denne matematiske model blev brugt til at lave en frekvensstyringsmetode for at sikre en god power faktor (PF). En prototype blev implementeret for at eftervise denne skiftefrekvens kontrol. Prototypen opnåede en til PF på 0,99, samt en "Total Harmonic Distortion" (THD) af indgangsstrømmen på 5,68%. Denne strømforsyning har en traditionel skiftefrekvens, men den samme fremgangsmåde kan anvendes til VHF konvertere. Overordnet belyser denne Ph.D. afhandling forskellige områder der skal tages højde for ved design af en VHF konverter forbundet til lysnettet. Gennem projektet er følgende områder blevet undersøgt: gate driver, synkroniserede ensrettere, PCB transformatorer, burst mode kontrol, frekvenskontrol af en resonantkonverter, galvanisk isolation, EMC, power factor og serieforbundne forsyninger.

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1

# Introduction

## 1.1 Background

Electronics has become vital for our every day life, and we often use it without noticing it. As a consumer we use both battery powered devises, household appliances and lighting equipment all being powered or charged from a mains connected power supply. In resent years the electronic market has been growing rapidly with smart devices, internet of things and other electronic appliances, which have increased the demand for power supplies. Today most power supplies are Switch Mode Power Supplies (SMPS) that combine high efficiency and small size. The size is limited by the passive components that occupy most of the volume [2]. The passive components scale inversely with frequency and hence increasing the operating frequency reduces the physical size of the power supply. Increasing the frequency is not a new idea, this has been done since the early days of of SMPS [3], however there are some limitations when doing, so such as increased switching losses in the active devices and increased core losses in the magnetic. The switching frequency is typically limited to a few MHz due these losses.

Research within power electronics focuses on increasing the efficiency, lowering the cost and reducing the size. We have seen small incremental steps during the last decades as magnetic materials and semiconductors have been improved. Most magnetic materials are still limited to around a MHz and the few materials that goes above have a very low permeability [4, 5]. Therefore to go higher in frequency, air core inductors have been used, however the relative permeability of 1 have forced a jump to frequencies around 30 MHz. The reason for this jump in frequency is the size benefit gained by using air cores inductors starts at this frequency. The 30 MHz limit is known as the lower boundary of the Very High Frequency (VHF) range going from 30 to 300 MHz.

Research in VHF power converters started in the early 2000s at Massachusetts Institute of Technology (MIT) and have since then continuously published papers on this topic [2, 4–29]. Since MIT started investigating VHF converters other universities have followed including the Technical University of Denmark (DTU). DTU published there first paper in 2011 [30] and have since then frequently been publishing within this area [16, 31–51].

The first publications from both MIT and DTU [6, 30] was inspired by Radio Frequency (RF) amplifiers that were already used for this frequency range. They used the same active components specially designed for RF amplifiers which is very costly (the transistors in [6, 30] cost more than 20 USD each). The first VHF converters showed great promise however failed to deliver on high efficiencies. Since the first publications commercial available MOSFETs have shown to be a viable alternative and can lower the cost significantly while achieving a high efficiency. New wide band-gab devices, such as Gallium Nitride GaN and Silicon Carbide SiC transistors, is starting to be used in VHF converters [52] and it will be interesting to follow the results of these, especially as the price of these devices drops over the coming years.

When this Ph.D. project started in 2013 most publications on VHF converters focused on DC-DC or DC-AC conversion. The technology showed promising results and the ability of reducing the physical size of the power converter. On the basis on previous results the idea to implement AC-DC converters with switching frequencies in the VHF range seemed promising. As the AC-DC offline application for consumer electronics include many portable products, this market would benefit from the size reduction offered by the VHF converters. Many consumer products are by law required to have galvanic isolation to protect the consumer, therefore the main field of this Ph.D. became galvanic isolated offline VHF converters.

### 1.2 Thesis scope

The objective of this Ph.D. thesis is to investigate the different blocks of a VHF offline power converter with galvanic isolation. Offline meaning a power converter connected to the AC grid. The goal is to achieve efficiencies comparable with existing commercial products, which are above 85%, fulfilling the standard regarding electromagnetic compatibility (EMC). The focus has been to achieve all this while using off the shelf low price components. To cover all the parts that makes a complete offline power converter several different research topics have been investigated. The research topics directly related to offline VHF converters has been galvanic isolation, EMC performance, power factor, stacking of converters. In addition to this more general topics have also been investigated during this Ph.D., such as synchronous rectifiers, PCB transformers, control of a resonant converter, and new gate drive implementations. These different parts have been published in 7 peer reviewed conference and journal papers. The publications create the basis for this thesis and are all included in the Appendix A-I. The Appendix also include a patent and a draft journal paper, which is soon to be submitted. This Ph.D. project has been performed in close collaboration with the DTU spinout company "Nordic Power Converters". Therefore, there has been a strong focus on commercialization of this technology.

### **1.3** Structure and content

The structure and content of the Ph.D. thesis are visualized in Figure 1.1.

Chapter 1: Covers the background and motivation for this Ph.D. project, it describes the scope of the thesis and gives an overview of the content in the thesis.

Chapter 2: Describes the state of the art within VHF resonant power converters. Here different topologies are presented, the general control strategies are presented together with galvanic isolation methods and applications.

Chapter 3: The passive components and the effect of parasitic components in VHF converters are described in this chapter. The main focus is on a self oscillation gate drive and the galvanic isolation of VHF converters.

Chapter 4: Describes stacking of converters placing converters in series to increase the input voltage span. An offline VHF converters for the US mains using the stacking technique is presented.

Chapter 5: Control of VHF converters are described in this chapter. A burst mode control method based on the gate drive from chapter 3 is presented and described. Furthermore a frequency control of an offline resonant converter is described together with the mathematical model behind the control.

Chapter 6: This chapter describes the EMC properties of a VHF converter regarding conducted and radiated emissions.

Chapter 7: Summarises the experimental results, conclude on the material presented in this thesis and describes future work.



Figure 1.1: Content overview of this thesis together with a list of the publications placed in the appendix, and a visual overview of where the content from the publications is used.

2

# State of the art

In this chapter different resonant topologies will be presented and discussed. An overview of state of the art solutions within offline resonant converters and within VHF converters is presented. VHF converters are still a new topic and the general advantages and limitations will be discussed.

## 2.1 High frequency resonant converters

Switch mode power supplies (SMPS) dominate the market for offline power supplies. Traditional SMPSs, described in [53], mainly use hard switching topologies which limits operating frequency as a result of switching losses. Nevertheless, increased switching frequencies permit reduced volume and therefore alternative topologies which overcome this limitation are of great interest. Resonant converter topologies are a prime example as they use soft switching frequency limit. For consumer electronics some of most common resonant topologies are the LLC and LCC [54–56] or variants of these. These topologies can be operated at a load independent point with a fixed input to output voltage ratio which makes them well suited for DC-DC applications. In respect to offline applications the LLC and LCC are usually used as a second stage DC-DC converter as mentioned in [57, 58]. There have been a few papers on topologies inspired by the LLC converter working as a single stage offline converter with high Power Factor (PF) [59–61].

# 2.2 Very High Frequency Resonant Converters

One of the main reasons to move the switching frequency to the VHF range is to minimize the size of the passive components and eliminate the use of electrolytic capacitors, which has a limited lifespan. New topologies have been presented [62, 63] to eliminate the use of electrolytic capacitors.

### 2.2.1 Topologies

Most topologies for VHF converter have been inspired by the radio amplifier topologies, connected together with a rectifier. These topologies were first presented in [64, 65]. The Class-E converter is one of the most used topologies, it is shown in Figure 2.1. The Class-E topology has one low side MOSFET which only requires a low side gate drive. This topology is well documented with specified design methods [66–70]. The

drawbacks with this topology is the high peak voltage across the MOSFET which at 50% duty cycle is approximately 3.6 times the input voltage.



Figure 2.1: Schematic of a Class-E converter, based on a Class-E inverter and rectifier.

The Class- $\phi_2$  topology is similar to the Class-E with the addition of an LC branch in parallel with the MOSFET. By adding an LC circuit with a resonance at the 2. harmonic the maximum voltage across the MOSFET can be reduced to approximately 2 times the input voltage at 50% duty cycle. This topology was developed at MIT and first presented in [8, 9]. The Class- $\phi_2$  are frequently used both as an amplifier and as a full converter, and is used for wireless power transfer applications [71–73].



Figure 2.2: Schematic of a Class- $\phi_2$  converter, based on a Class- $\phi_2$  inverter and a Class-E rectifier.

The Sepic converter is a known topology from traditional power electronics and it is described in [53, 74, 75]. This topology is shown in Figure 2.3 and have also been used for VHF converters [11, 32, 41, 48, 49]. The benefit of the Sepic converter compared to the Class-E is that it only has two inductors in a full converter, which can help reduce the AC losses in the inductors and improve the efficiency of the converter. The Sepic converter used in [49] reaches 87% efficiency with a switching frequency of 48.7 MHz.



Figure 2.3: Schematic of a Sepic converter.

The Class-DE converter shown in Figure 2.4 is a half bridge topology described in [76, 77]. The peak voltage across MOSFETs for this topology is equal to the input voltage, which makes this topology suited for higher input voltages. This topology

however needs a high side gate driver, which is the main limitation for implementing the Class-DE with VHF switching frequencies. The only implemented VHF Class-DE converters are presented in [36, 37] (Appendix D) using the gate drive described in [31, 78] (Appendix B,C).



Figure 2.4: Schematic of a Class-DE converter, based on a Class-DE inverter and a Class-E rectifier.

### 2.2.2 Galvanic isolation

Galvanic isolation is used to isolate two different part of a system, galvanic isolation means that there is no direct conductive path across the barrier. Transferring energy across the isolation barrier can be done in different ways such as capacitive, magnetic, optical or mechanical. The most used isolation type in power converters is the magnetic using coupled inductors or transformers. Galvanic isolation is used in almost all chargers for consumer electronics such as a laptop charger. Safety regulations require galvanic isolation if the costumer can touch the power connector. Transformers have been used for many years. They are made with different materials depending on the frequency. high frequency magnetic materials are investigated in [2, 4, 5, 21–23]. An alternative to using ferrite materials are air core magnetics, especially in the VHF range were they can be superior in performance [79, 80]. By use of air core inductors and transformers the magnetics can be implemented directly into the Printed Circuit Board (PCB), PCB embedded inductors are described in [35, 38, 44, 51] and PCB embedded transformers in [33, 37, 40]. PCB embedded transformer can be made with spiral, toroidal and solenoid geometries. Figure 2.5 shows different implementations of solenoid PCB transformers, they are described [37] (Appendix D). The figure shows one of the drawbacks with air core transformers, as there is no magnetic material to guide the flux the windings have to share a common area for the flux to pass through.

Mechanical isolation can be implemented with piezoelectric transformers described in [81], this type of transformers can be made in a small package and can be used in a magnetic less converter [82–86]. The piezoelectric transformers are made of ceramics and can be cheap to manufacture in large quantities. They can achieve high power density and efficiencies and their topologies are in many ways similar to VHF converters. They produce little Electromagnetic Interference (EMI) as they have no changing magnetic fields, this enables them to work in high flux environment like with Magnetic Resonance Imaging (MRI) scanners.

Capacitive isolation can be used to transfer power or signals across an isolation barrier. A power converter with capacitive isolation is described in [35, 48, 87], An application were capacitive isolation are well suited in in wireless power transfer [88–90]. Wireless



Figure 2.5: Different approaches to implement solenoid PCB transformers, primary is solid and secondary is crossed.

power transfer have become a great application for VHF and multi megahertz converters [71–73, 91].

Optical isolation is mostly used for transmitting signals as in optocouplers or through optical cables, and it is not important for this project.

### 2.2.3 Control methods

Control of power converters is essential for most commercial products as it keeps the converter operating optimal under different conditions. The typical control method for conventional power electronics are Pulse Width Modulation (PWM) which is simple and easy to implement. It does however not work for resonant converters with a fixed duty cycle ratio, here alternative solutions are used such as frequency control [92–95].

Frequency control changes the frequency depending on the conditions, this changes the transfer function of the converter. By changing the transfer function the converter can maintain a constant output voltage or current, or compensate for a varying supply voltage. To implement frequency control a good understanding of the topology is needed. For LLC converter there is now off the shelf IC-drivers with frequency control. For other topologies the process is not so straight forward, especially when the frequency is increased. Therefore frequency control on VHF converters is very difficult. Frequency control is further discussed in section 5.2, where a frequency control method is derived for an offline converter.

An alternative to frequency control is burst mode control, this control method is also refereed to as on/off control. Burst mode control works by turning the converter on and off at a frequency much lower than the switching frequency. In this way a low frequency PWM signal can control if the converter is on or off and thereby control the output. The benefits of burst mode control are the linear response and easy feedback implementation. The drawbacks are the introduction of low frequency content, which can lead to higher EMI. This control method is used for traditional SMPS for light load conditions where the converter is powered down to save energy. This make the converter achieve a higher efficiency at light load. Burst mode control is one of the most used control methods for VHF converters. This is used in [11, 13, 15, 20, 41, 96, 97]. One reason for using burst mode control for VHF converters is the simplicity as they can otherwise be difficult to control. As mentioned, burst mode create lower frequency content. However, the burst frequency can be implemented at the same or higher frequencies than traditional SMPS are switching.

Another method of controlling VHF converters is out phasing control, this requires multiple inverters and strict control of the phase. Out phasing control works by controlling the phase difference between two or more inverters. Their output is then combined through a passive network so that the outputs are either added or subtracted. Examples of out phasing control are described in [16, 17]

### 2.2.4 Challenges and limitations with VHF converters

When increasing the switching frequency to the VHF the traditional hard switched topologies cannot operate due to losses. This is primarily due to the switching losses which in simplified form can be calculated by:

$$P_{sw} = \frac{1}{2} \cdot C_{oss} \cdot V^2 \cdot f_s \tag{2.1}$$

Where  $C_{oss}$  is the output capacitance, V is the voltage across the MOSFET and  $f_s$  is the switching frequency. From the equation it is evident that the voltage is the dominant part, and this is why it is much easier to increase the switching frequency for low voltage applications. This thesis is operating towards offline VHF converters and therefore the voltages and frequencies will he high, this would result in high losses for traditional hard switched converters. For resonant converters the switching losses can be neglected, however this does not mean that the MOSFETs don't have any losses. The conduction losses are still present which is the loss in the MOSFET when it is turned on. The conduction loss is found by:

$$P_{con} = R_{DS} \cdot I^2 \tag{2.2}$$

Where  $R_{DS}$  is the on resistance of the MOSFET and I is the RMS current through the device. For traditional frequencies this equation is usually sufficient. When increasing the frequency to the VHF range additional conduction losses appear, as illustrated in Figure 2.6. The conduction loss element  $R_{DS}$  is shown together with two other loss elements the gate resistance  $R_{gate}$  and the Equivalent Series Resistance (ESR)  $R_{C_{DS}}$  of the drain-source capacitance  $C_{DS}$ . The losses related to  $R_{C_{DS}}$  is the off-state conduction loss and can be a significant part of the total MOSFET loss. This effect will be described in chapter 3.2.



Figure 2.6: Loss model of a MOSFET.

The gate drive for traditional SMPS provide the gate with a square wave signal to ensure a fast transition between on and off and to ensure a low on resistance  $R_{DS}$ . A traditional gate driver produces a loss each time the gate is discharged corresponding to the energy stored in the input capacitance  $C_{iss} = C_{GS} + C_{GD}$ . For most MOSFETs this will lead to a large loss when they switch in the VHF range. To avoid this resonant gate drives, where a sinusoidal current is driving the MOSFET, is often used. Resonant gate drives use a resonant network to circulate the energy stored in the input capacitor  $C_{iss}$ . Thereby the loss is minimised to the AC loss in the gate resistor  $R_{gate}$  and the ESR of the network.

One of the challenges when operating in the VHF range is the charging current needed to charge the output capacitance of the MOSFET. The current needed to charge a capacitor is:

$$I_C = C \cdot \frac{dV}{dt} \tag{2.3}$$

When designing an offline converter with switching frequencies in the VHF range equation (2.3) is a good place to start. The current will increase as the voltage across the MOSFET or the frequency increases. A VHF Class-E converter with an input voltage of 200 V switching at 30 MHz will need to charge the output capacitor of the MOSFET to 720 V in 8.33 ns. Assuming an output capacitance of 50 pF the current becomes 4.32 A. The waveforms of a Class-E converter is shown in Figure 2.7. These 4.32 A is the average resonant current for the first 8.33 ns after the switch turns off, and the output capacitor is charged to the peak voltage. This is the minimum resonant current for the Class-E converter to operate regardless of the output power. For low power systems this can be a real challenge, since the AC losses in the converter will become to high.



Figure 2.7: Waveforms in a Class-E converter.

### 2.2.5 Applications

The majority of VHF converters consist of an inverter and a rectifier, the inverter topologies are inspired by RF amplifiers generate outputs an AC current. The AC output current is then passed through the rectifier to the load, because the output is a rectified AC current this type of converter is suited as a DC-DC converter with constant output current. Many of the topologies used for VHF converters have tight tolerances to the load impedance, usually the rectifier is designed for a given load and then the inverter is designed to match the input impedance of the rectifier. Most publications of VHF converters are working with resistive loads and are not mentioning a specific application, however there are a few operating as LED drivers [36, 41, 44, 47]. The LED driver is a very suitable application for this type of converters as they have a constant output current. The LED are naturally limiting the output voltage ensuring that the rectifier diodes are not exceeding its maximum reverse voltage. The same holds for battery charging applications, where the battery clamps the output voltage. To operate a VHF converter with a fixed output voltage for varying loads control methods have to be implemented, as mentioned there are different options and two of these will be presented in Section 5. For a VHF converter to be commercialized they will in most applications need some sort of control. At the time of writing this Ph.D. thesis their are two companies are working on brining VHF converters to the market. These two being Finsix a spinout company from MIT working with laptop chargers and Nordic Power Converters a spinout of DTU working with LED lighting.

3

# Passive and parasitic components

Passive components are essential for power converters and the parasitic components are well known for traditional SMPS. However when the switching frequency is increased, the parasitics have a larger impact on the circuit. In this section passive components and the impact of parasitic components will be discussed in connection to VHF converters, and the parasitic components will be used to implement a self-oscillation gate drive. Different ways of implementing galvanic isolation will also be described.

## 3.1 Passive components

Passive components are a vital part of power electronics. Inductors and capacitors are used to store energy and resistors are used to control the energy flow, however introduces losses. The energy storing components are accountable for most of the physical volume in a traditional SMPS, and can be the limiting factor when making a compact power converter. The energy storing components consists of two different groups the electrical field components being the capacitors and the magnetic field components consisting of inductors, coupled inductors and transformers.

There are three different parts of a power converter where the passive components take up most volume. The input filter reduces the input current ripple and can remove differential and common mode signals. It usually consists of a large capacitor and a common mode choke inductor. In the power stage, passive components are used to store and transfer the energy each switching cycle. In galvanic isolated power converters transformers are used which can take up a large area together with the isolation barrier. The output filter reduces ripple on the output and removes unwanted differential and common mode signals. This filter also consists of a large capacitor and a common mode choke inductor. Increasing the switching frequency to the VHF range reduces the amount of energy transfer within the power stage in each cycle. This reduces the value of the passive components, which also reduces the physical size of the component. This reduction of component values is not only within the power stage. By increasing the switching frequency the the input and output filters can be implemented with higher cut-off frequencies, which will lead to a reduction in size.

Increasing the frequency to the VHF range also changes the component selection. For magnetic components there is limited magnetic materials that can operate above 10 MHz, this is investigated in [2, 4, 5, 21–23]. High frequency magnetics have low permeability and can have high core losses at VHF, because of this air core magnetics are used. Today there are a good selection of air core inductors on the market, most of which are solenoid based. Furthermore, they can be implemented into the PCB. PCB

air core inductors can be implemented as spiral, solenoid and toroidal inductors as described in [51]. Solenoid PCB air core inductors are used in [31, 35] (Appendix B,E). Another interesting approach of implementing air core inductors are the 3-D printed inductors described in [79, 80].

The capacitor selection is also limited for VHF converters. An electrolytic capacitor has a high energy density. However it also has a large parasitic inductance and thereby a low self-resonance frequency. It can be used in the input/output filters to maintain a constant DC voltage, however it has to high impedance at 30 MHz to work inside the power stage. Film capacitors in general have a higher self-resonance than the electrolytic and they can thereby be used for higher frequency operation. However, they are still not the preferred choice in the power stage of a VHF converter as there is a limited selection when working with Surface Mounted Devices (SMD). Therefore, the preferred capacitor for VHF converters are the ceramic capacitors because they have a high self-resonance. Ceramic capacitors come in different materials, shapes and voltage ratings. Listed below are a few guide lines for choosing a capacitor for a VHF converter.

- Smaller footprint means lower self-inductance and thereby higher self-resonance.
- C0G and NP0 de-rates very little over voltage and temperature. However, they only come in relatively low capacitance values.
- Smaller footprint also means higher voltage de-rating (not for COG and NP0), in some cases the capacitance is reduced by 80% at the rated DC voltage.
- X5R, X7R, CoG, NP0 and so on is only a temperature marking, therefore check the datasheet for voltage properties and series resistance.
- If there is no good datasheet available then measure the component in an impedance analyser.
- Electrolytic and film capacitors are good for DC voltages just parallel a ceramic capacitor that can handle the operating frequency.

## **3.2** Parasitic components

When increasing the frequency to the VHF range the values of the passive components decreases significantly, this also means that the parasitic components have a larger influence on the design. This section will focus on the parasitic components of the active devices in a VHF converter. The parasitic inductance is usually package dependent, long legs or big package results in larger parasitic inductance where flip-chip and small packages have low parasitic inductance. Parasitic inductance is unwanted and can result in ringing above the switching frequency generating EMI. Therefore small packages SMD devices are preferred for VHF converters. Parasitic capacitance is however mostly depending on the device parameters, for low power Shottky diodes (below 100 V and 2 A) the capacitance is usually around tens of pico farad. The junction capacitance varies with the reverse voltage of the diode and is found in most datasheets. Parasitic capacitance is also an important part of the MOSFET. As shown in Figure 3.1 there is



Figure 3.1: Loss model of a MOSFET.

several capacitances in the MOSFET. The capacitances are inversely proportional to the on resistance  $R_{DS}$  and is also depending on the voltage rating of the MOSFET.

The output capacitance listed in the MOSFET datasheet is defined as  $C_{oss} = C_{DS} + C_{GD}$ , this capacitance changes as the drain-source voltage changes. In most topologies used for VHF converters there is a capacitance connected between drain and source of the MOSFET, the output capacitance of the MOSFET therefore sets the lower limit for this capacitor value. In some cases it can be beneficial to choose a MOSFET where the output capacitance matches the needed capacitance, in this case the MOSFET will also have a lower on resistance ( $R_{DS}$ ) which reduces the conduction losses. This is the same as using the figure of merit (FOM), except FOM is dependent on the on resistance and the gate charge and not the energy stored in the output capacitor.

The second capacitance shown in a datasheet is the input capacitance  $C_{iss} = C_{GS} + C_{GD}$ , this capacitance determines the current needed to drive the MOSFET. It also determines the gate losses in traditional gate drives, driving the gate with a square signal result in a loss defined as:

$$P_{gate,HS} = f_s \cdot Q_G \cdot V_{GS} \tag{3.1}$$

Where  $Q_G$  is the gate charge  $f_s$  is the switching frequency and  $V_{GS}$  are the gate drive voltage. Another approach is to use the input capacitance  $C_{iss}$ , However this capacitance is non linear and is only used to approximate the gate loss.

$$P_{gate,HS} \approx f_s \cdot C_{ISS} \cdot V_{GS}^2 \tag{3.2}$$

The last capacitance found in a datasheet is  $C_{rss} = C_{GD}$ , this capacitance is the smallest of the three and is unwanted in traditional hard gated converters. However, in VHF

converters it can be used to transfer energy to a self-oscillating gate drive which will be described in the next section.

Together with the parasitic capacitances of the MOSFET there are three parasitic resistances, the first is the drain-source resistance  $R_{DS}$  which is used to calculate the conduction loss.

$$P_{DS} = R_{DS} \cdot I_{DS}^2 \tag{3.3}$$

The second resistance is the gate resistance  $R_{gate}$  which is used to calculated the peak current when driving the MOSFET with a square wave voltage. The gate resistance is also used to calculate the gate loss in a resonant gate drive, this loss is calculated by:

$$P_{gate,RE} = R_{gate} \cdot I_{gate}^2 \tag{3.4}$$

As seen the resonant gate loss is not frequency depended as the traditional gate drive in 3.1.

The two resistances  $R_{DS}$  and  $R_{gate}$  are usually listed in the datasheet. However, there is a third resistance, connected in series with the capacitance  $C_{DS}$ . This resistance is named  $R_{C_{DS}}$  and is the ESR of the capacitance. In traditional hard-switched converters there is only passed current though the output capacitance when the voltage over the MOSFET changes, this current results in a loss which at frequencies below 1 MHz is low compared to the other losses in the MOSFET and therefore neglected. However, when increasing the frequency to the VHF range the current passing through the capacitance  $C_{DS}$ , when the MOSFET is turned off, can be equal to the current in the on period. Therefore, if the resistance  $R_{C_{DS}}$  is comparable to  $R_{DS}$  so is the loss. This resistance is not given in the datasheet, so it have to be measured frequency depending and also dependent on the drain-source voltage.

$$P_{C_{DS}} = R_{C_{DS}} \cdot I_{C_{DS}}^2 \tag{3.5}$$

The intrinsic resistance of  $R_{C_{DS}}$  can be extracted from some IC process spice models, however this is not available for discrete devises. Therefore it is useful to measure the resistance of the output capacitor  $C_{oss}$  using an impedance analyser. To measure the  $C_{oss}$  the gate and source are connected together, and the measurement are then done from drain to source. The resistance  $R_{C_{DS}}$  and  $R_{C_{oss}}$  can be assumed to be close to each other as long as  $C_{DS} >> C_{GD}$ .

Parasitics can have a great influence on the design of the converter and on the gate drive. The parasitic components influence both traditional hard-gated and also the resonant gate drives. In the next section a gate drive for VHF converters using the two capacitors  $C_{GS}$  and  $C_{GD}$  and the gate resistor  $R_{gate}$  is described.

### 3.3 Gate drive

There are several resonant gate drive solutions for VHF converters, some of which are self-oscillation as described in [41, 44, 45]. In this section a VHF gate drive consist-



Figure 3.2: The simple gate drive, the dotted line represent the devise including the parasitic capacitors.



Figure 3.3: Different gate drive implementations.

ing of only passive components is presented. The gate drive is published in [31, 78] (Appendix B,C). This gate drive utilizes the parasitics together with a few external passive components to create a transfer function from drain to gate with 180 degree phase shift. The gate drive in its simple version is shown in Figure 3.2. Where the only external component is an inductor connected between the gate and a bias voltage.

The simple gate drive has some limitations as the only variable component is the external inductor, and the bias voltage which can be raised and lowered to adjust the duty cycle of the MOSFET. To expand the flexibility of the gate drive there can be added additional components on the gate as shown in Figure 3.3. The first extension is adding a capacitor from gate to source or gate to drain, which can help adjusting the gain and phase of the transfer function. The transfer functions can be seen in Figure 3.4 where the colors are matched to Figure 3.3. The capacitor between gate and source (Brown) reduces the gain and increases the phase slightly at 30MHz compared to the simple gate drive (Black), where the capacitor between gate and drain (Green) increases the gain with a slight reduction in phase compared to the (Brown). The gate drive can also be implemented with LC circuit connected from gate to either source (Blue) or drain (Red), this can eliminate the second harmonic and boost the third harmonic creating a gate voltage closer to a square wave. However, adding these extra parts also increases the complexity and cost of the circuit.

The transfer functions from drain to gate are shown for the different implementation in Figure 3.4. The different implementations have different gain around the fundamental,


Figure 3.4: Transfer functions of the different implementations of the gate drive shown in Figure 3.3.

which in this case are 30 MHz. The gain can be adjusted by changing the component values, in general placing capacitance between gate and drain will increase the gain and placing capacitance from gate to source decreases the gain. It is seen that they all have a phase shift close to 180 degrees at and the fundamental frequency which is essential for this gate drive, as the gate must go high when the drain-source voltage is low. The blue line shown an LC circuit tuned to the second harmonic placed between gate and source, this removes the second harmonic and create a gain on the third. By doing this the gate voltage can either be more square shaped or have a peak depending on the phase, the square shaped is good for limiting the peak voltage and having a short peak results in a low duty cycle.

This gate drive has the advantage that it can be implemented as a high side gate drive. Since it is only composed of passive components the circuit just need a transient to start oscillating. The half bridge gate drive implementation is shown in Figure 3.5. Here the simple gate drive is connected on the low side MOSFET and the high side have an additional inductor  $(L_H)$  and capacitor  $(C_{G1})$ . The inductor  $L_H$  is used to set the bias voltage for the high side gate drive form  $V_{Bias1}$  which would be  $V_{Bias1} = \frac{V_{IN}}{2} + V_{Bias2}$ . The capacitor  $C_{G1}$  are used to create a low impedance path at high frequency between the gate and source of the high side MOSFET.

The gate drive shown in Figure 3.5 has been used for half bridge converters in [36, 37] (Appendix D), where it has achieved above 80 % efficiency at 30 MHz. In [37] the two inductors  $L_{G1}$  and  $L_{G2}$  are implemented as coupled inductors which will be discussed in section 3.4.

This gate drive is also suitable for use in synchronous rectifiers, where the gate drive is driving a single low side switch or a half bridge rectifier. Synchronous rectifiers are used for low voltage or high current applications where the forward voltage drop across the diodes results in high losses. The conduction loss in a diode are calculated by:

$$P_{con,D} = V_{forward} \cdot I_{average} \tag{3.6}$$



Figure 3.5: Class-DE schematic with the self-oscillating gate drive on high and low side MOS-FET.



Figure 3.6: Class-E converter with synchronous rectifier, both inverter and rectifier is implemented with the self-oscillating gate drive.

By replacing the diodes in the rectifier with MOSFETs the conduction losses becomes:

$$P_{con,M} = R_{DS} \cdot I_{DS_{RMS}}^2 \tag{3.7}$$

If  $P_{diode} >> P_{DS} + P_{gate}$  and the engineer can justify the addition of a gate dirve and an control signa, then the diode should be replaced by a MOSFET to reduce the total losses. This holds for traditional switching frequencies and also for VHF converters. A synchronous rectifier also have switching losses, switching losses is depending on the output voltage and will in most synchronous rectifiers not be the dominant. A synchronous rectifier will increases the complexity and price of the circuit. The selfoscillating gate drive is used in synchronous rectifiers in [31, 35, 44] (Appendix B,E,A). The gate drive of in rectifier is designed to start oscillating when the inverter is activated, and then just follow follow the same frequency. Using a synchronous rectifier improved the efficiency of 2.5% in [35] (Appendix E) where the converter reached a peak efficiency of 80%.

Another reason for having a synchronous rectifier is to make the converter bidirectional. A schematic of a bidirectional Class-E converter is shown in Figure 3.6. The Class-E schematic shows symmetry around the resonant tank, which here consists of a capacitor and an inductor, and this makes it appear ideal for bidirectional use.



(a) Bidirectional converter with discrete inductors.



(b) Bidirectional converter with PCB embedded inductors.

Figure 3.7: Bidirectional converters from Appendix E.

In [35] (Appendix E) a bidirectional Class-E converter is implemented operating at 35.6 MHz. The converter was implemented on two separate PCBs one with discrete air core inductors and one with PCB embedded inductors. The two converters are shown in Figure 3.7. The converter with discrete components achieved efficiencies of 80/70% in forward/reverse conduction mode, and the converter with PCB embedded inductors achieved efficiencies of 74/65%. This difference was due to the higher Q values of the discrete inductors, as the converter with the PCB embedded inductors was limited to the same size, the inductors reach lower Q values.

#### 3.4 Galvanic isolation

Galvanic isolation means no direct conducting path across a isolation barrier. The galvanic isolation can be made as a functional or a safety isolation barrier, the safety isolation is used in applications where it is required by the law. The isolation requirements are depending on the application and also on the voltages in the circuit. An isolation barrier can be a limiting factor when decreasing the size of a power converter as there is strict demands on clearance and creepage. To use capacitors as galvanic isolation they have to be Class-Y rated capacitors. The class system together with isolation voltages is stated in the standard DS/EN 60384-14:2013 [98]. Class-Y rated capacitors can be made with different materials, including ceramic materials. However, Class-Y rated ceramic capacitors come in large packages and tend to be very expensive.

When implementing functional galvanic isolation the capacitor should only be rated for the maximum voltage across it, and in this case regular capacitors can be used. functional galvanic isolation was implemented in [35] (Appendix E), where a Class-E converter is galvanic isolated. This was done by splitting the resonant capacitor into two as shown in Figure 3.8. By making a functional galvanic isolation the input and output can be connected in different ways, and several converters can be connected with the input or output in series and parallel. An example could be three converters with series connected input and a parallel output, in this way three 5 W converters boosting 5 V to 12 V could become one 15 W converter boosting 5 V to 36 V. This technique will be further discussed in section 4. Several converters have been implemented with galvanic isolation during this Ph.D. project. All of these was implemented with functional galvanic isolation [35, 43, 46, 48] (Appendix E,G,I,F).



Figure 3.8: Schematic of a bidirectional Class-E with galvanic isolation.



Figure 3.9: Solenoid transformer in the nested configuration.

Galvanic isolation can also be implemented with transformers. This is the most common way of achieving galvanic isolation in traditional SMPS. Most transformers use a magnetic core to guide the flux between the primary and secondary windings, and thereby achieve a good coupling. High frequency magnetic materials are investigated in [4, 5, 22, 23]. However, very few materials are suitable for VHF converters. Air core magnetics described in [21, 79, 80] are a good alternative as they do not have any core losses or risk going in saturation. Air core transformers are limited to structures that guide the flux through a common winding area, since there is no core to help guiding the flux. Spiral and toroid PCB embedded air core transformers are described in [40, 99]. In [37] (Appendix D) a solenoid PCB embedded air core transformer is described and verified in a half bridge VHF converter. The transformer is in this case used to couple the gate drive inductors ( $L_{G1}$  and  $L_{G2}$  in Figure 3.5) of the two MOSFETs forcing them to be out of phase. The paper [37] (Appendix D) describes and tests different configurations of the solenoid transformer as shown in Figure 2.5. The converter is implemented with the nested configuration which is shown in Figure 3.9. By using this PCB air core transformer the efficiency was improved by 2.2% reaching 81.09% with an output power of 9.12 W.

PCB embedded air core transformers are easy and cheap to make and consistent PCB production makes these a good solution for air core magnetics. In general air core magnetics are considered a good solution for VHF converters since they have no core losses, which is a problem for normal core based transformers [2, 4]. The disadvantages are the low inductance, coupling and a larger external magnetic field, due to the missing magnetic material [51].

Transformers can also be used to make galvanic isolation in VHF converters from input to the output. Examples of this are described in [21, 100, 101]. The transformers



(a) Isolated Class-φ<sub>2</sub> converter with Class-E rectifier [101].



(b) Isolated Class- $\phi_2$  converter [21].



(c) Push-pull Class- $\phi_2$  converter with full wave Class-E rectifier [100].

Figure 3.10: Different approaches to implement solenoid PCB transformers.

is either connected in series with the input or as a part of the resonant tank. The topologies from the three papers are shown in Figure 3.10. The topology in Figure 3.10a has the transformer as part of the resonant tank, this is also the case for the topology shown in Figure 3.10c. The topology shown in Figure 3.10b has a transformer connected in series with the input inductor. All these three converter topologies are based on the Class- $\phi_2$ . However all configurations could also be implemented as Class-E or Sepic converters. If a Class-DE converter should use a transformer it would be in the resonant tank. This would make the converter similar to the LLC converter.



# Stacking

One of the challenges within VHF converters is to increase the input voltage, as most VHF topologies have a high voltage stress on the active components due to their resonant behaviour. The most suited topology for high input voltage is the Class-DE which limits the peak voltage of the MOSFETs to the input voltage. As an alternative to the Class-DE topology several converters can be connected in series. If the converters are galvanic isolated from input to output their outputs can either be connected in series or parallel. This idea is described in [48] (Appendix F) where an isolated converter shown in Figure 4.1 is used in different configurations.



Figure 4.1: Galvanic isolated converter, the dotted line represents the isolation barrier.

#### 4.1 Connection of several converters

One of these configurations is shown in Figure 4.2, where two converters have their input in series and output in parallel. By doing this they can operate form twice the input voltage and double the output power. For the two converters to split the input voltage equally they will need to have the same input current. If one converters draws more current the voltage will decrease on its input and increase on the other. The converters therefore need to draw more current when the input voltage is increased. If this is the case, the two converters will be self-regulating and split the input voltage. This form of stacking can be done for all isolated converters and is in [48] (Appendix F) done for both a traditional DC-DC converter and a VHF converter. For resonant VHF converters with high voltage stresses this can increase the operating input voltage.

Another way to increase the input voltage for a converter is to use the step-up configuration shown in Figure 4.3. Here the load is connected in series with the input of the converter. This system can then be operated at the input voltage of the converter and the load voltage. The step-up configuration not only increases the input voltage of the system it also increases the output power and the efficiency. The input current in the converter flows through the load together with the output current from the converter,



Figure 4.2: Two galvanic isolated converters with there inputs connected in series and outputs in parallel.



Figure 4.3: A galvanic isolated converter connected in step-up configuration.

The input current is therefore added to the output power "for free". In [48] (Appendix F) this technique was used to increase the efficiency by approximately 5% and to increase the output power by 50%. Even so the converter by itself is galvanic isolated, this configuration creates a direct current path from input to output and thereby the system is not galvanic isolated.

#### 4.2 US mains converter

The techniques described in [48] (Appendix F) were used to implement a US mains VHF converter in [43] (Appendix G), where three Class-E inverters were connected in series as shown in Figure 4.2. The stacking of three inverters reduces the peak voltage across the MOSFET in each Class-E inverter to one third, this means that lower voltage devices can be used. To decrease the input voltage of the three inverters further, the load was placed in series with the input of the inverters as shown in Figure 4.3 and used



Figure 4.4: The build up of the US mains VHF converter.



Figure 4.5: The Class-DE rectifier used in the US mains converter.

in [36]. To decrease the component count the three inverters share a single rectifier and have a combined resonant tank. The configuration of the inverters, rectifier and load is shown in Figure 4.4.

The converter is implemented with a single rectifier to reduce component count. Because the rectifier is connected in parallel with all three inverters the input impedance of the single rectifier should be three times higher than a rectifier for a single inverter stage. This converter uses a Class-DE rectifier which is shown in 4.5 and described in [66, 102], the input impedance of a Class-DE rectifier with D = 0.25 is:

$$Z_{IN} = \frac{1}{2 \cdot \pi} \cdot \frac{2 \cdot \pi}{\omega \cdot (C_{D1} + C_{D2})} \tag{4.1}$$

As shown the capacitances  $C_{D1}$  and  $C_{D2}$  define the input impedance of the rectifier. For this converter this impedance have to be three times a single rectifier meaning that



Figure 4.6: The US mains VHF converter with size measurements.

the junction capacitance of the diodes have to be three times a large. This enables a selection of a bigger diode with lower forward voltage resulting in a higher efficiency. As shown in Figure 4.4 there is only one resonant inductor instead of three inductors. The value of the single resonant inductor is equal to a parallel connection of the three resonant inductors. So by using only one inductor a higher Q can be achieved which increases the efficiency and reduces component count. Another advantage of using a single resonant inductor is that the switching frequency of the three inverters is forced to synchronize as they share the same resonant current.

The converter was designed to operate from the US mains delivering 9 W to a 60 V LED. Each inverter was implemented with the self-oscillating gate drive described in [31, 78] and in section 3.3. A picture of the converter is shown in Figure 4.4. If the PCB is divided into two box volumes one is to the left of the large resonant inductor and one with the large resonant inductor, the power density of the converter becomes 2.14  $\frac{W}{cm^3}$ . The converter is achieving an efficiency of 89.4% with an AC input voltage of 120 V RMS.

The converter is designed to run from the US mains and high PF is often a requirement for offline converters. To achieve a good PF there is no large DC capacitor placed on the input and the converter is operated in most of the period. Each inverter needs an input voltage of 23 V for the gate drive to start, once started they keep operating until the input voltage becomes too low for the self-oscillating gate drive to maintain oscillations. This converter type works as a voltage controlled current source and the output power follows the input voltage, which means that the current drawn from the mains follows the mains voltage. The input voltage and input/output currents are shown in Figure 4.7. It is evident that the input current is in phase with the voltage. The converter reaches a PF = 0.96, which is sufficient for an offline LED driver in this power range. To implement this into a product there is still a few things that need addressing. First the converter shuts down twice every 60 Hz period which results in a 120 Hz flicker at the output. To reduce this low frequency flicker an energy storage is needed. This could be a large capacitor at the output, however this would reduce the power density. Second is the input harmonics on the input current that might need additional filtering



Figure 4.7: Measurements of the input voltage (yellow), input current (green) and output current through the LED (blue).

as there is a steep flank when the converter starts every cycle.

# 5

# Control

Control of power converters is essential for most commercial products as it keeps the controlled variables within their specified limits. Most power converters use PWM to control the output voltage or current. The control scheme can be implemented in many different ways depending on the application. In traditional SMPS the control can be a simple PI regulator controlling the PWM. However, this control does not work for resonant converters with fixed duty cycles. In this chapter two new control methods for fixed duty cycle converters are described. A new burst mode control implementation of a Class-E converter and a new frequency control method for a half bridge resonant converter.

## 5.1 Burst mode

Burst mode control works by turning the converter on and off at a frequency much lower than the switching frequency, a PWM signal can in this way control the output of the converter. Burst mode control has a linear response, and works with standard control IC's. Burst mode control is one of the most used control methods for VHF converters. It is used in [11, 13, 15, 20, 41, 96, 97]. In [41] burst mode is used to control an interleaved Sepic converter. This converter achieved an efficiency above 81% for most of the operating range. However, this implementation of burst mode control relies on an RC constant that introduces a delay of 500 ns from the rising edge of the PWM signal to the converter starts operating. To reduce this delay the burst mode control can be implemented as shown in Figure 5.1. This implementation works for most single switch topologies, using the gate drive described in section 3.3.

The new burst mode circuit consists of two MOSFETs, an N-MOS (N) and a P-MOS



Figure 5.1: Burst mode control implemented with the self-oscillating gate drive, the dotted line represent the devise including the parasitic capacitors.

(P) with their gates connected to the PWM signal. When the PWM signal is low the P-MOS turns on while the N-MOS turns off, this raises the gate voltage of the large MOSFET to  $V_{Bias}$ . If  $V_{Bias}$  is high enough the MOSFET turns on and the oscillations starts. When the PWM signal goes high the P-MOS turns off and the N-MOS turns on draining all the energy stored in the gate drive circuit. The diode  $D_1$  is added to enable the gate voltage to go below the source voltage. This circuit is easy to implement and only contribute with small losses, mostly the additional conduction losses in the P-MOS. The PWM signal needs steep flanks to ensure that the N-MOS and P-MOS is not both conducting and hereby creating a short from  $V_{Bias}$  to  $V_S$ . If  $V_{bias}$  is just above the threshold of the MOSFET the gate drive will be operating with 50% duty cycle. The circuit was simulated with the converter used in [46] (Appendix I). The results from the simulation are shown in Figure 5.2. With a zoom on the turn on and the turn off in figure 5.3. The circuit starts approximately 50 ns after it is turned on, and is effective at turning off the converter. The drain voltage  $V_{drain}$  reaches 90 V under operation and settles around the input voltage when the converter is off. The gate voltage operates around the bias voltage which is 4 V in this simulation. The PWM voltage clearly demonstrates that the converter is running when  $V_{PWM}$  is low and off when  $V_{PWM}$  is high. The output power shows that the burst mode generate low frequency content. The flanks on the output power is due to the output capacitor, this low frequency content could be filtered out with a bigger output filter.



Figure 5.2: Burst mode operation of a class-E converter, blue is the drain voltage, gray is the gate voltage, green is the PWM signal, and red is the output power.

This design of a burst mode control could be implemented in a stacked converter as described in section 4. To achieve this each inverter would need a PWM signal which would require a level shifter for each stage. Therefore burst mode is best suited for single stage converters as in DC-DC converters. Implementing burst mode on VHF converters



Figure 5.3: A zoom of the burst mode operation at turn on and turn off. Blue is the drain voltage, gray is the gate voltage and green is the PWM signal.

creates EMI at the burst frequency and the harmonics. To minimize the EMI generated by burst mode large EMC filters are needed. This will limit the size reduction gained by operating in the VHF range. With burst mode control only the passive components within the power stage of a VHF converter helps with a size reduction. In general burst mode control is easy to implement on VHF converters, and will be a good solution for many applications.

#### 5.2 Frequency control

For consumer electronics some of the most common resonant topologies are the LLC and LCC [53, 103–105]. These topologies can be operated at a load independent point with a fixed input to output voltage ratio which makes them well suited for applications with a varying load. Another approach is controlling the switching frequency and hereby changing the transfer function of the converter. Frequency control is used to track changes in the load and maintain a constant output voltage. It can also be used compensate for input voltage variations. With proper design, resonant converters can work at different input voltages and loads within certain limits.

To use frequency control, it is necessary to understand the behaviour of the converter, such as knowing the transfer function. In Appendix H the first harmonic approach (FHA) is used to characterise the charge pump topology reported in [106] and shown in Figure 5.4. The converter is a mains connected half bridge topology with a "charge pump" capacitor  $C_{in}$  ensuring a high PF. The resonant tank is implemented with an inductor  $L_{res}$  and three capacitors  $C_{res}$ ,  $C_b$  and  $C_{in}$ . The resonant current in  $L_{res}$ ensures that the MOSFETs achieve soft switching with a prober dead-time.  $C_b$  is a DC blocking capacitor, where  $C_{res}$  and  $C_{in}$  ensures a high frequency AC voltage at  $V_A$ . If the voltage  $V_A$  is reaching from 0 to  $V_{C_{DC}}$  each period, then  $C_{in}$  draws a high frequency current from the mains proportional to the mains voltage. The two components before



Figure 5.4: The half bridge "charge pump" topology described in appendix H.



Figure 5.5: The simplified model of the circuit shown in Figure 5.4.

the diode bridge  $L_{AC}$  and  $C_{AC}$  are filter components, and they are used to filter the high frequency current, creating a sinusoidal input current. The voltage across  $C_{DC}$ is kept larger than the peak voltage of the rectified AC mains, to avoid a direct path from the mains to the  $C_{DC}$ .

If the voltage in  $V_A$  has a minimum voltage of 0 and and a maximum voltage equal to the voltage  $V_{C_{DC}}$  each cycle, then ideally the converter will have a PF of 1. However the impedance of the resonant circuit changes across a mains cycle which will change the voltage  $V_A$ . To understand the high frequency behaviour of the topology the FHA is used. The FHA is a method for analysing and understanding the operation of resonant converters, through harmonic approximation of a piecewise analytical circuit model [103, 107]. To use FHA on the circuit shown in Figure 5.4 has to be simplified. The resonant inductor is assumed to have a sinusoidal current and the diodes are assumed lossless. The simplified circuit is shown in Figure 5.5, and is only analysed at the fundamental frequency.

The circuit shown in Figure 5.5 is used to described the voltage  $V_A$  across one period assuming a sinusoidal resonant current. This process is described in Appendix H. The final piecewise equation for the voltage  $V_A$  is:

$$V_{A} = \begin{cases} -\frac{I_{in} \cos\left(\theta\right)}{\omega C_{x}} + I_{in} \sin\left(\theta\right) R_{x} + V_{1}, & \theta_{2} - \pi < \theta \le \theta_{1} \\ \frac{|X| I_{in} \cos\left(\theta + \angle X\right)}{\omega C_{x}} \\ + |X| I_{in} \sin\left(\theta + \angle X\right) R_{x} + V_{2}, & \theta_{1} < \theta \le \theta_{2} \\ -\frac{I_{in} \cos\left(\theta\right)}{\omega C_{x}} + I_{in} \sin\left(\theta\right) R_{x} + V_{3}, & \theta_{2} < \theta \le \theta_{1} + \pi \\ -\frac{|X| I_{in} \cos\left(\theta + \angle X\right)}{\omega C_{x}} \\ + |X| I_{in} \sin\left(\theta + \angle X\right) R_{x} + V_{4}, & \theta_{1} + \pi < \theta \le \theta_{2} + \pi \end{cases}$$
(5.1)

Where |X| and  $\angle X$  are the magnitude and phase of a complex impedance defined in H. The initial voltages  $V_1$  to  $V_4$  across  $C_x$  are found to be:

$$V_1 = -\frac{I_{in} \left(-C_x \sin\left(\angle IN\right) R_x \,\omega - \cos\left(\angle IN\right)\right)}{\omega \, C_x} \tag{5.2}$$

$$V_2 = -\frac{|X| I_{in} \left( \sin \left( \angle IN - \angle X \right) R_x \,\omega \, C_x + \cos \left( \angle IN - \angle X \right) \right) - V_{in} \,\omega \, C_x}{\omega \, C_x} \tag{5.3}$$

$$V_3 = -\frac{I_{in} \sin\left(\angle IN\right) R_x \,\omega \,C_x - V_{in} \,\omega \,C_x + I_{in} \cos\left(\angle IN\right)}{\omega \,C_x} \tag{5.4}$$

$$V_4 = -\frac{I_{in} |X| (-C_x \sin (\angle IN - \angle X) R_x \omega - \cos (\angle IN - \angle X))}{\omega C_x}$$
(5.5)

Where |IN| and  $\angle IN$  are the magnitude and phase of a second complex impedance defined in H. With voltage and the current known Fourier analysis is used to simplify the impedance of the resonant circuit to a series connected RC circuit. The resonant circuit is then reduced to the series connected LCR circuit shown in Figure 5.6. As the analysis did not include the resonant inductor  $L_{res}$  it is a fixed value.

The equivalent capacitor and resistor changes across the AC input voltage and at different switching frequencies. The equivalent capacitance of  $C_{eq}$  is shown in Figure 5.7. The capacitance increases with an increase in input voltage, this is because the capacitor  $C_{in}$  is conducting for a larger part of the period.

The equivalent resistance of  $R_{eq}$  is shown in Figure 5.8. The resistance increases at low AC voltages as the load resistor  $R_{load}$  and the DC blocking capacitor  $C_b$  becomes



Figure 5.6: The FHA model of the circuit.



Figure 5.7: The equivalent capacitor  $C_{eq}$ .



Figure 5.8: The equivalent resistor  $R_{eq}$ .



Figure 5.9: Frequency vs. AC voltage plot for different resonant inductor  $L_{res}$  values.

a larger part of the resonant impedance. The equivalent resistor  $R_{eq}$  increases at lower frequencies this is because the load resistor draws a constant power independent on frequency.

Both the resistor and the capacitor changes over frequency and input AC voltage, however the inductor shown in Figure 5.6 has a fixed value. As part of the model the amplitude of the resonant current is found. The amplitude is used to generate a frequency control depended on the AC input voltage. The control curves for different inductor values are shown in Figure 5.9. The plot shows, the frequency vs. AC voltage control curves for different inductor values. So if the the converter was implemented with a 150  $\mu$ H inductor, then the converter should follow that curve to achieve a high PF.

To verify the FHA model the frequency control was implemented in a prototype. The AC mains voltage was measured by a differential amplifier before the input filter, and an Analog to Digital Converter (ADC) converted the voltage to a digital signal. A micro controller with a lookup table based on the FHA model control a Digital to Analog Converter (DAC) to set a DC voltage. This DC voltage is connected to a voltage controlled oscillator (VCO), which controls the frequency of the power stage.

The implemented converter was tested with and without frequency control, both with an output power of 5 W. The AC voltage and input currents with and without control are shown in Figure 5.10. In both cases, the input current is in phase with the voltage. The current with frequency control resembles a sinusoidal waveform, with a small zero crossing error. The input current for the fixed frequency operation has a considerable discontinuity around the zero crossing and a spike in current at the peak AC voltage. A steep flank around the zero crossing will cause a rise in harmonics, and the spike illustrates that the voltage of  $C_{DC}$  drops below the AC peak voltage.

The converter achieved a PF of 0.990 with frequency control, which is sufficient for most applications. The PF without control was measured to be 0.955, which is a lower but sill acceptable. Regulations regarding mains connected power converters are not limited to the PF value, limits for the harmonic content on the input current is also specified. The



Figure 5.10: The measured AC input voltage  $V_{AC}$  and the input current  $I_{in}$  with and without control.



Figure 5.11: The measured input current harmonics and standard limits from IEC 61000-3-2 [1].

measured harmonics and the limits from IEC 61000-3-2 [1] are shown in Figure 5.11. The harmonics with control are much lower than the limits and only have a small peak at the third harmonic. Whereas without control the harmonics are above the limits at the 5th, 7th and 13th harmonic. The Total Harmonic Content (THD) measured on the input current was 5.68% with control and 26.1% without control. This also confirms that the control improves the operation in relations to the regulations 61000-3-2.

The output power of the converter is plotted in Figure 5.12. The control maintains a constant voltage in  $V_A$  which directly relates to a more constant output power. There is a little third harmonic ripple on the output with control, which might originate from the same place as the third harmonic measured on the input current. The output power without control fluctuates much more during a line cycle.

Overall the model is fitting well with the measured results, and it gives a good description on the behaviour of this topology. And even though this model is used for a converter switching around 300 kHz the model still holds for higher frequencies. The



Figure 5.12: The measured output power of the implemented converter.

biggest difference when increasing the frequency is that the voltage between the two MOSFETs in the half bridge is assumed to be a square wave for traditional switching frequencies, whereas for VHF frequencies it would be a trapezoidal waveform.

6

## Electromagnetic compatibility

This section focuses on the EMC for VHF converters. In [46] (Appendix I) a Class-E VHF converter is implemented, to test how a VHF converter performs regarding electromagnetic emissions. The converter used is a single Class-E inverter, similar to the one used for the US mains converter in section 4, with a Class-DE rectifier. To test the performance of different filters and cable orientations, 9 different converters were implemented. All the different implementations are described in Appendix I. In this chapter, 3 implementations will be presented and discussed.

#### 6.1 Starting point

The converter for the EMC test was implemented as a Class-E inverter with a Class-DE rectifier as shown in 6.1. The converter is galvanic isolated with the two capacitors  $C_{RES1}$  and  $C_{RES2}$  as discussed in section 3.4. In this implementation  $C_{RES2} >> C_{RES1}$ making  $C_{RES2}$  acts as a DC blocking cap, this reduces the common mode. With a large  $C_{RES2}$  fluctuations on the potential between the ground on primary and secondary side are reduced. The output power is 3 W and the load is a 60 V LED. The switching frequency is 37 MHz which is above the limits regarding conducted emissions. The converter uses the self-oscillating gate drive described in section 3.3 and achieves an efficiency of 80%. All the converters were implemented with small connectors to be able to change between the PCBs without changing the position of cables and the converter it self. This is mainly important in regards to radiated emissions where the position can influence the measurement.

The first converter to be tested is shown in Figure 6.2. This converter were a implemented with a single decoupling capacitor. This capacitor is necessary to remove



Figure 6.1: Schematic of the converter used for EMC test, it consists of a Class-E inverter and a Class-DE rectifier.



Figure 6.2: Class-E converter with a Class-DE rectifier without input/output filters.



Figure 6.3: The conducted measurement on the converter without any input/output filter.

the influence of the cable inductance. A line impedance stabilization network (LISN) network was used to to test the converters conducted emissions. The result of this measurement is shown in Figure 6.3. It is clear from the measurement that there are no conducted emissions op to 30 MHz.

The switching frequency of the converter was placed above the conducted regulations and therefore it was not expected to show any conducted emission. However if burst mode control was implemented there would be emissions at the burst frequency, and these emissions would require larger filters to suppress. To reduce the size of the filters for burst mode control, the burst frequency can be changed constantly within given fre-



Figure 6.4: Radiated measurement without input/output filters.

quency range and hereby spread the emissions across multiple frequencies lowering the peak values. Frequency control generates emissions at the switching frequencies, therefore if a VHF converter is implemented with frequency control it would not generate any emissions below 30 MHz.

With the conducted measurement showing no emissions, the attention can be focused on the radiated emissions. All the radiated measurements have been made inside an EMC chamber with an antenna placed 3 m from the converter. The radiated measurements of the converter without filters is shown in Figure 6.4.

As seen in the figure there is a large peak at the switching frequency followed by all the harmonic content. The radiated emission shows that additional filtering is necessary. The PCB is a few cm in length and width and would by itself not be a good antenna. For a frequency of 37 MHz the wavelength is  $\lambda = 8.1 \text{ m}$ , a good antenna is then  $\lambda_2 = 4.05 \text{ m}$  or  $\lambda_4 = 2 \text{ m}$ . Therefore the cables are expected to be responsible for the emissions.

### 6.2 With filters

To reduce the radiated emissions input and output filters were implemented. The converters were also implemented with a ground plane on the bottom of the PCB. Two converters with EMC filters are shown in Fig. 6.5. One of these also have an EMC shield that covers the most of the PCB. By adding filters the power density is reduced,





(a) Class-E converter with a Class-DE rectifier with input/output EMC filters.

(b) Class-E converter with a Class-DE rectifier with input/output EMC filters and shield.

Figure 6.5: Two VHF converters used in Appendix I, one without EMC filter and one with EMC filter and shield.



Figure 6.6: Schematic of the input/output filter implementation used in the two converters,  $V_{IN/OUT}$  is placed towards the VHF converters power stage.

however this is also the case for traditional switching frequencies. As a rough estimation the ratio between the size of the power stage and the filters should remain the same for VHF converters and traditional converters.

A EMC filter is usually implemented to filter both differential and common mode signals. Differential mode emissions in a SMPS are created when the converter draws power from the source or delivers power to the load. This makes the differential signals easy to track down, whereas the origin of the common mode emissions is more difficult to find, as they can depend on several things. The EMC filter implemented on the two converters is shown in Figure 6.6. This filter is both filtering differential and common mode signals.

The filters are implemented with 1008AF inductors from Coilcraft and ceramic capacitors, all component values for the filters are shown in table 6.1. As seen on the schematic, the two inductors are not coupled, and they therefore filter differential mode and common mode signals. The capacitors  $C_{f1}$  and  $C_{f6}$  are only filtering differential mode signals. Whereas the four capacitors  $C_{f2}$ - $C_{f5}$  are connected to the ground plane to filter the common mode signals. By connecting them to the ground plane they create a low impedance path for the signals at high frequencies. This keeps the signals within the PCB and reduces the emissions. The EMC shield is connected to the ground plane with vias all around the edge of the shield. This reduces any electric field coupling

Component	Value	Type
$L_{f1}$	3.3 µH	Ferrite
$L_{f2}$	3.3 µH	Ferrite
$C_{f1}$	1 μF	X5R
$C_{f2}$	680  pF	C0G
$C_{f3}$	680  pF	C0G
$C_{f4}$	680  pF	C0G
$C_{f5}$	680  pF	C0G
$C_{f6}$	1 µF	X5R

 Table 6.1: Component values for the input and output filter.



Figure 6.7: Radiated measurement on the converter with input/output EMC filters.

across the filter and to the outside.

The radiated measurement of the converter with filters is shown in Figure 6.7. The filters placed on the input and output reduces the radiated emission with 20-25 dB $\mu$ V across the frequency range. However there is still a few harmonics which are above the limit.

The radiated measurements for the converter with an EMC shield is shown in Figure 6.8. Adding the EMC shield reduces the radiated emissions significant and only the fundamental and first harmonics are present. By adding the EMC shield the capacitive coupling across the filter is limited and most of the radiated emissions are eliminated. The radiated emission are with the addition of the EMC shield below the limits of EN



Figure 6.8: Radiated measurement on the converter with input/output EMC filters and shield.

55022 [108].

#### 6.3 Summary

The conducted EMC measurement demonstrated that the converter had no problem with conducted emissions from 150 kHz to 30 MHz. The challenge when increasing the switching frequency to the VHF range is to lower the radiated emissions between 30 MHz and 1 GHz. The radiated emissions still originate from the cables and can be reduced with filtering and by adding an EMC shield to stay within the limits of EN 55022 [108].



# Conclusion and future work

## 7.1 Summary of experimental work

During the Ph.D. project several converters have been implemented. In this section a brief overview of the implemented converters is presented. I have designed and implemented the converters presented in the first part of this section. In the second part of the section converters designed in collaboration with Nordic Power Converters is presented.



Figure 7.1: Class-E converter with synchronous rectifier.

The first converter implemented during my Ph.D project is shown in Figure 7.1. It consists of a Class-E inverter and a Class-E rectifier. The converter was designed to test the feasibility of a synchronous rectifier. The efficiency of this converter was 70% with a switching frequency of 30 MHz. The converter is described in [31, 44] (Appendix A and B).



Figure 7.2: Bidirectional Class-E converter with discrete PCB embedded inductors, together with unidirectional converter with diode rectifiers.

The second converter to be implemented is shown in Figure 7.2, it is a bidirectional Class-E converter with capacitive galvanic isolation. The converter was implemented

with discrete and with PCB embedded inductors. Two converters with diode rectifiers was implemented to test the efficiency gained by using synchronous rectifiers. The converter reached a peak efficiency of 80% with a switching frequency of 35.6 MHz. This converter is described in [35] (Appendix E).



Figure 7.3: Class-E inverter with Class-DE rectifier, the converter has PCB embedded inductors and one PCB embedded capacitor.

Shown in Figure 7.3 is the third converter. This converter was made to investigate the possibility of implementing all the passives components in the PCB. The converter was implemented with PCB embedded inductors and one PCB embedded capacitor. The capacitor seen in the middle of the PCB, as the metallic part. It has a capacitance of 56 pF. The converter is the same as those used for the EMC investigation in section 6. This converter showed that even with a switching frequency of 37 MHz implementing the passive components on the PCB is possible but not practical. This converter reached a peak efficiency of 83%.



Figure 7.4: Several converters implemented with a Class-E inverter and a Class-DE rectifier. These were used for EMC investigation.

The converters shown in Figure 7.4 was implemented to investigate EMC on VHF converters. All converter were implemented with a Class-E inverter and a Class-DE rectifier. And all of them were galvanic isolated with capacitors. The converters showed no emissions in the conducted measurement from 150 kHz to 30 MHz, however the radiated measurement from 30 MHz to 1 GHz showed that filtering is necessary. The converter with filters and a EMC shield was able to reduce the emissions below the limits given in EN 55022 [108]. The EMC results are described in section 6 and published in [46] (Appendix I). The efficiency of this converter reached a peak efficiency of 83% with a switching frequency of 37 MHz.

The fifth converter I have implemented is shown in Figure 7.5. It is an offline VHF converter for the US mains (120  $V_{RMS} @ 60 Hz$ ). The converter is implemented with three Class-E inverters in series and a single Class-DE rectifier. The converter is designed to



Figure 7.5: An offline VHF converter for the US mains.

deliver 9 W to a 60 V LED, and the three inverters were designed to have a switching frequency of 37 MHz. As described in section 4 the output of the rectifier was placed in series with the inverters input boosting the efficiency to 89.4%. The converter had a power density of 2.14  $\frac{W}{cm^3}$ , and was achieving a PF of 0.96. The converter is published in [43] (Appendix G).



Figure 7.6: A half bridge charge pump prototype, implemented to verify a new frequency control method.

The last converter to be implemented is shown in Figure 7.6. It is an offline half bridge charge pump converter. The converter was implemented to verify a mathematical model based on the first harmonic approach (FHA). The converter was implemented with a new frequency control method which improved the PF to 0.99 and reduced the harmonics on the input current significant. The switching frequency was around 300 kHz which made it the only converter not switching in the VHF range. The converter is described in 5.2 and it will be published in the near future. The draft paper is shown in Appendix H.

In connection with my collaboration with Nordic Power Converters, I have been involved in the development of several converters. The first of these converters are shown in Figure 7.7. The figure shows three different implementations of the same converter. The converter is designed as an LED driver, delivering 20 W to a 60 V LED load. It consists of three Class-E inverter and three Class-DE rectifiers. The converter was implemented with either an electrolytic capacitor or several ceramic capacitors as shown in Figure 7.7a and 7.7b. These two converters reached a power density above 3  $\frac{W}{cm^3}$ . The converter shown in Figure 7.7c was implemented with EMC filters and EMC shield. It was tested at a certified test facility and it fulfilled the standard EMC regulations.

Another project performed in collaboration with Nordic Power Converters is shown in 7.8. This was also a 20 W offline LED driver for the US mains. This time implemented with a Class-DE inverter and Class-DE rectifier. This converter was implemented with



(a) US mains converter with a electrolytic capacitor.



(b) US mains converter with ceramic capacitors.



(c) US mains converter with a electrolytic capacitor and EMC filter and shield.

Figure 7.7: US mains offline Class-E converters developed together with Nordic Power Converters.

burst mode, enabling the output power to be controlled from 1% to 100%. I was involved in the development of this converter and was in charge of a small batch production of 20 pieces.



Figure 7.8: US mains offline Class-DE converter developed together with Nordic Power Converters.

## 7.2 Conclusion

The Ph.D. project documented in this thesis has focused on the main topic "A VHF offline power converter with galvanic isolation". During this project different research

areas within VHF power converters have been investigated and published.

A new self-oscillating resonant gate drive along with several examples of its implementations in complete circuits have been presented. The described gate drive is a simple, compact, low cost and reliable solution composed only of passive components. The gate drive is used for all the VHF converters presented in this thesis. The gate drive has been used as low side gate drive, a high side drive and to control a bidirectional converter with a synchronous rectifier.

Several converters has been implemented with capacitive galvanic isolation, that have worked as functional isolation and not safety isolation. The capacitor in the resonant tank can easily be split into two capacitor placed across a isolation barrier. The magnetic isolation barrier have been investigated with new structures for PCB embedded air-core transformers. The transformers were based on a rectangular solenoid structure and an analytic two-port model for the structure was developed and verified by measurements. The structure of two solenoids nested inside each other, was found to be the most promising. This structure was used to couple the gate inductors in a Class-DE converter increasing the efficiency by 2.5%.

Different stacking techniques were presented, which can be used to reduce the voltage stress for isolated DC-DC converters in applications where galvanic isolation is not a requirement. The stacking technique can provide higher efficiency compared to a conventional single converter. The obtained benefits are considered very appealing for certain non-isolated applications, such as LED lighting. The experimental results shows twice the power handling capabilities and 5-10% higher efficiency compared to single converters without stacking.

The stacking technique was used to implement a US mains VHF converter delivering 9 W to a 60 V LED load. The converter consisted of three Class-E inverters and one Class-DE rectifier. The converter had a switching frequency of 37 MHz and an efficiency of 89.4%. Increasing the switching frequency to the VHF range reduced the size of the passive components and thereby the size of the converter. The size reduction resulted in a high power density of 2.14  $\frac{W}{cm^3}$ . The converter was implemented without a DC energy storage on the input, and reached a PF of 0.96.

A simple burst mode control circuit was presented, which together with the selfoscillating gate drive provides easy control for VHF converters with low side switches. Burst mode control can in many cases be a good solution, where the low frequency content is acceptable or can be filtered out. As an alternative to burst mode control a new frequency control method was presented for an offline half bridge topology. The frequency control was build on a mathematical model found from FHA. And it was implemented in a prototype where the power factor was improved to 0.99. Furthermore the harmonic content of the input current was lowered significantly. The prototype was implemented with a switching frequency around 300 kHz. However, the mathematical model is also valid for a VHF converter.

If VHF converters is to be commercialised they have to fulfill standard regulations such as EMC requirements. Therefore EMC measurements on VHF converters have been presented. The EMC measurements shows that the main challenge for VHF converters is the radiated emissions above 30 MHz. My work demonstrated that the radiated emissions can be lowered with filtering and by adding an EMC shield.

#### 7.3 Future work

This Ph.D. thesis have covered the broad topic of offline VHF converters, and though great effort have been put in covering everything. There are still topics within "offline VHF converters" worth investigating, together with VHF converter in general. Some ideas for future work is listed here

- The possibilities of implementing a galvanic isolated VHF converter with an air core transformer that will fulfill the safety requirements. And compare the performance of this with a capacitively isolated converter.
- Implementation of a VHF converter operating from the European mains 230  $V_{RMS}$ . This could be achieved by stacking several inverters in series, similar to the US mains converter presented in this thesis. An alternative is to use GaN devices with voltage ratings of 600 V, these devices could be used in a single stage Class-DE converter for the EU mains.
- Implementation of burst mode control with increased frequency will increase the bandwidth of the control loop. Increasing the burst frequency will allow for the filter components to be reduced in size. As part of the size reduction an integration of the control circuitry with an IC process could also be investigated.
- The possibilities of frequency control for VHF converters, as this would enable control without increasing the size of the filters. Implementing a VHF converter with frequency control will require specially designed controllers. The controller IC could be implemented on the same die as the power MOSFETs to minimize the parasitics.
- Development of VHF specific MOSFETs either in silicon or gallium nitride. VHF specific MOSFET could be optimized to have low parasitic inductance, low gate resistance and low output capacitance. Hereby improving the performance together with minimizing power losses.

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# Evolution of Very High Frequency Power Supplies

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# Evolution of Very High Frequency Power Supplies

Arnold Knott, Member, IEEE, Toke M. Andersen, Student Member, IEEE, Peter Kamby, Jeppe A. Pedersen, Mickey P. Madsen, Student Member, IEEE, Milovan Kovacevic, Student Member, IEEE, and Michael A. E. Andersen, Member, IEEE

Abstract—The ongoing demand for smaller and lighter power supplies is driving the motivation to increase the switching frequencies of power converters. Drastic increases however, come along with new challenges, namely the increase of switching losses in all components. The application of power circuits used in radio frequency transmission equipment helps to overcome those. However, those circuits were not designed to meet the same requirements as power converters. This paper summarizes the contributions in the recent years in the application of very high frequency (VHF) technologies in power electronics, which show the results of the recent advances and describes the remaining challenges. The presented results include a self-oscillating gate drive, air-core inductor optimizations, an offline LED driver with a power density of 8.9 W/cm<sup>3</sup>, and a 120-MHz, 9-W dc powered LED driver with 89% efficiency as well as a bidirectional VHF converter. The challenges to be solved before VHF converters can be used effectively in industrial products are within those three categories: 1) components; 2) circuit architectures; and 3) reliability testing.

*Index Terms*—DC–DC power converters, power conversion, resonant inverters, very high frequency (VHF) circuits, zero-voltage switching (ZVS).

#### I. INTRODUCTION

THE continuing trend of miniaturization in industrial and consumer electronics is continuously driving a demand for smaller power supplies. Weight and cost reduction demands accompany this trend. Within power supplies, the major size, weight, and cost drivers are typically the passive components. Increasing the switching frequency of power converters can reduce the size, weight, and therefore the cost of those. For substantial size and weight reduction, the switching frequencies are increased up to the very high frequency (VHF) band (30–300 MHz), which leads to a merge in circuit technologies used in radio frequency transmitters [1]–[6] and the classical power electronics circuits.

The VHF amplifiers are designed for dc–ac conversion, where the ac simultaneously is the switching frequency. Generally, those circuits [1], [2] drive a known load impedance, typically a  $50 - \Omega$  antenna. Traditionally, the topologies used for those circuits have been characterized as classes with running

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The authors are with the Technical University of Denmark, Kgs, Lyngby 2800, Denmark (e-mail: akn@elektro.dtu.dk; andersen@lem.ee.ethz.ch; peter@kamby.dk; jarpe@elektro.dtu.dk; mpma@elektro.dtu.dk; mikov@elektro.dtu.dk).

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labels following the alphabet. Class-A, B, and C are described in [7] and [2]. These classes are characterized through the relative amount of time; the power transistor is conducting the load current with respect to the period of the VHF signal. For class-A, the transistor conducts the load current 50% of the time. Class-B operates between 25% and 50% and class-C between 0% and 25%. This leads to theoretical maximum achievable efficiencies of 50%, up to 78.5%, and up to 100% for class-A, B, and C, respectively. Their power electronics counter parts are linear regulators. Class-D is described in [8] and the first power circuit topology, which allows for theoretical 100% efficiency under all operating conditions. The equivalent is strictly all hard-switched power converters. Class-E, as described in [3] and [4], and class-F, as demonstrated in [5] and [6], correspond to all power converters, that apply zero-voltage switching (ZVS) and zero-current switching (ZCS) techniques, respectively.

Similar to switch-mode power supplies, those VHF amplifiers convert the constant supply voltages into a high-frequent voltage by operating power semiconductors in the triode region only. The major difference is that VHF amplifiers do not convert the energy back into a constant voltage or current level.

Numerous research works have been published [9]–[20], filling this gap and making VHF technologies available for power electronics. This paper describes the individual contributions of those in greater detail. However, there are still some challenges left, before VHF switch-mode power supplies can relieve their advantages for products in industrial and consumer electronics.

This paper elaborates on the most recent advances, showing prototypes and measurement results in Section II. Section III describes the remaining challenges based on previous work and characterizes them. Section IV concludes this paper.

#### **II. RECENT ADVANCES**

Recent research results enhanced the state of the art in VHF converters. Most of the works in the recent years have focused on class-E derived topologies.

#### A. Optimal Operation

The class-E-based power circuits allow for a second degree of soft switching. Despite turning the power switches on, when the voltage across them is zero (ZVS), also the derivatives of these signals are considered. This is called ZdVS and ZdCS, respectively. The technique has been applied to power converters in [19]. The schematic diagram in Fig. 1 shows the

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Fig. 1. Schematic diagram of a self-oscillating VHF converter  $\left[ 24\right]$  with LED load.



Fig. 2. Simulated waveforms for an ZVS and ZdVS class-E-based converter from [19].

adoption of the principles of a class-E oscillator, e.g., shown in [21]–[23], to a class-E-based power self-oscillating VHF converter (dc–dc) [19], [24]. A converter achieving both ZVS and ZdVS at all times operates in optimal mode.

Other implementation replaced either the resonant tank [25], [26] or the input inductor [11], [27] with a transmission line. The resulting waveforms of this circuit have been reported in, e.g., [28]–[33] and Fig. 2 shows the simulated waveforms of this converter, where  $v_s$  and  $i_s$  are the voltage and the current across and through the switch and  $v_D$  and  $i_D$  are voltage and current across and through the rectifier diode.  $v_G$  is the control signal of the power switch and  $V_o$  and  $V_i$  are input and output voltages of the converter. The top graph  $v_s$  shows the optimization of the converter for both ZVS and ZdVS.



Fig. 3. Photograph of the self-oscillating VHF converter from [24].

Fig. 3 shows a photograph of the implementation of this converter. The overall efficiency of the 97-MHz converter is 55%.

The advantage of this converter is that it is based on a widely documented circuit topology from the communication electronics applications. As implemented here, it also provides means of output regulation. The downside is the voltage stress across the power switch, 3.6 times higher as in hard-switched converters.

#### B. Suboptimal Operation

Due to the tight adjustment of the turn-on instance of the power switch for achieving ZVS and ZdVS the degrees of freedom in this converter are low. That limits the input and output voltage ranges. Furthermore, the efficiency is not acceptable. In this case, the majority of the losses are due to conduction losses in the power semiconductors, which are due to the on-resistance of the power switch. As the gate voltage is not significantly higher than the threshold voltage, the devices minimum on-resistance could not be achieved.

Suboptimal operation of class-E converters, as described in [4], opened for higher degrees of freedom in the design of class-E-based dc–dc converters. This means that the ZdVS condition is only fulfilled under nominal load conditions and only ZVS is fulfilled otherwise. The resulting converter waveform in the optimal and suboptimal operating regions is shown in Fig. 4. The effects of these operation mode, as described in [34], have been extended in [20] to LED lighting applications.

Note that the body diode of the MOSFET is conducting in the beginning of the MOSFETs conduction period. This is due to wrong timing in the turn-on of the power device. The energy lost in the body diode ruins the efficiency of this particular converter.

Furthermore, [20] provides a detailed analysis of the power components parasitics and the effect of their nonlinearities. The basis for this analysis has been, among others, laid in [35] and [36] for the analysis of class-E amplifiers, which is fully applicable to class-E-based power converters when



Fig. 4. Measurements of gate-source and drain-source voltages  $V_{\rm gs}$  and  $V_{\rm ds}$  of the power switch and the turn-on instances. Note that the drain-source voltage has an offset of -0.5 V, due to the oscilloscopes offset. (a) Optimal operation. (b) Suboptimal operation.

tuning the rectifier to act as an ohmic load. The most relevant parasitics of the power switch are the input and output capacitances. The later is the most critical for the design of the converter. Simultaneously, the output capacitance is highly nonlinear, which was considered in the analysis in [20]. There, the nonlinearity of the output capacitance  $C_{\rm ds}$  is modeled with

$$C_{\rm ds}(V_c) = \frac{C_{j0}}{\left(1 + \frac{V_c}{V_{\rm bi}}\right)^{\gamma}}$$
(1)

where  $C_{j0}$  is the junction capacitance at 0 V,  $V_{bi}$  is the built-in junction potential, typically 0.5–0.9 V [29], and  $\gamma$  is the junction sensitivity or gradual coefficient. Typically,  $\gamma = 1/3$  for gradient junctions, while  $\gamma = 0.5$  for abrupt junctions [1] hence junction diodes [29], and v is the junction voltage.

This results in a voltage waveform  $V_c$  of the power switch as a function of the converters input current  $I_{in}$  and the above



Fig. 5. Voltage waveform of the power switch in relation to dc input voltage for a nonlinear output capacitance from [20].  $V_{bi}$  is the junction potential of the process.

output capacitances parameters as

ı

$$V_c = V_{\rm bi} \left( \left[ \frac{I_{\rm in}(1-\gamma)}{\omega C_{j0} V_{\rm bi}} \times \left( \omega t - \frac{3\pi}{2} - \frac{\pi}{2} \cos \omega t - \sin \omega t \right) + 1 \right]^{\frac{1}{1-\gamma}} - 1 \right).$$
(2)

Fig. 5 shows the relative voltage waveform of the power switch as a function of time and junction potential  $V_{\rm bi}$  for a junction sensitivity of  $\gamma = 0.5$ .

The remaining components of the power stage have been investigated in [20] as well. Thereby, most focus is on the inductors, as these are the most volume-consuming parts, have the biggest weight and typically a big impact on the overall price of the converter. Therefore, the inductors have been integrated as toroids into the printed circuit board (PCB). This process is described in [37] and Fig. 6 shows the principle.

A power stage has been designed to operate in suboptimal mode under the consideration of the power switches nonlinear output capacitance. The converters efficiency is in the same area as the one presented in Section II-A and again limited by a high on-resistance, which is due to a low gate drive voltage. While giving up on the single operating point operation in optimal operation mode, the suboptimal operating converters theoretically allow for different conduction angle operation on the cost of tighter timing to operate in ZVS.

### C. Class-E-Based SEPIC Converter

For dealing with the efficiency challenge, [38] compared a number of power switches both in simulation and experiment. Furthermore, multiple air-core inductors where calculated, designed, and implemented. An extraction is shown in Fig. 8. The prototypes reach Q-values beyond 100 and resonance frequencies up to 340 MHz. Fig. 9 shows a photograph of the implemented converters. On top of that, an effective line and load regulation scheme was realized in those. The designs where verified in a SEPIC converter (Fig. 7) [39], based on



Fig. 6. PCB integrated inductor from [37]. The cross section of the PCB toroid and the resulting flux arrows are shown.



Fig. 7. Schematic diagram of a class-E-based SEPIC VHF converter [39].



Fig. 8. Photograph of various air-core inductors [38].

the topologies presented in [40], achieving a power density of 8.9 W/cm<sup>3</sup> (146 W/in<sup>3</sup>) by switching at 51 MHz for offline LED applications.

Fig. 10 shows the implementation of the final prototype with 70-MHz switching frequency. The voltage step-down ratio of the converters is 10 and the output power range is between 1 and 4 W at an efficiency within this range beyond 70%.

Compared with the above-reported converters, the SEPIC converter is not based on an inverter that delivers a sinusoidal output. The later is crucial in telecommunication applications, when using the class-E inverter as a transmitter, but completely unnecessary demand as an intermediate VHF link within a dc/dc power converter. Relaxing this requirement removes the resonant tank inductor, and therefore the resonant tanks bandpass behavior. On the other hand, the rectifier can no longer freely be chosen between several topologies, but has to



Fig. 9. Photograph of numerous prototypes for comparing measured efficiency with simulations [38].



Fig. 10. Photograph of a closed loop low-power VHF converter with an efficiency beyond 70% from [38]. The TO220 components in the upper left corner are the dummy load resistance.



Fig. 11. Full schematic view of the open-loop interleaved class-E converter from [43].

be implemented with a diode, not referenced to ground, which is a disadvantage in some implementation technologies, such as integrated circuits.

## D. Interleaved VHF Converters

In addition, the self-oscillating principle from [19] and [24] was combined with the interleave principle from [41] and [42] in [43], resulting into a significant efficiency improvement. Interleaving two converter legs allows furthermore to use the ripple cancelation, as described in [44] and applied in [41]. The complete schematic diagram of the open-loop implementation is shown in Fig. 11. The realized converter



Fig. 12. Drain-source waveforms of the two power switches in the interleaved converter from [43]. (a) Simulated waveforms. (b) Measured waveforms.

is switching at 120 MHz, i.e., beyond the FM band, converts an input voltage between 6 and 9 V into an output current between 0.4 and 0.5 A and has an efficiency between 80 and 89% within this operation range. The output power range is 3–9 W, corresponding to an output voltage range between 7 and 20 V. The converter is designed to drive LEDs. Fig. 12 shows both a SPICE-based simulation and the measurement of the power switches voltage waveforms. Fig. 13 shows the efficiency graph of this converter.

Interleaved converters allow for input and/or output ripple cancellation, segmented power stages, which enables higher power levels [45]. However, those converters suffer from different optimal frequencies due to tolerances for each leg, which either might result in beat tones, when operating each of them at its own optimal resonant frequencies, or a nonoptimal operation point with respect to efficiency for all legs, when operating all legs at the same frequency.

#### E. Bidirectional VHF Converter

Replacing the diode in Fig. 1 with a transistor, the class-E amplifier and the class-E synchronous rectifier form a symmetric schematic view, as shown in Fig. 14. This was realized in [46] and resulted in a bidirectional converter with the same conversion ration from both sides. Operating in the forward mode, the transistor  $M_1$  is the power switch, operating in class-E mode, and  $M_2$  is used as synchronous rectifier in class-E operation. In the reverse operating mode, the voltage



Fig. 13. Efficiency of a battery driven LED driver switching at 120 MHz [43].



Fig. 14. Schematic diagram of a VHF converter with class-E inverter and synchronous class-E rectifier [46].



Fig. 15. Photograph of a bidirectional VHF converter [46].

designated  $V_{out}$  is acting as the input voltage and  $M_2$  becomes the inverter switch, while  $M_1$  turns into the synchronous rectifier. The maximum achieved efficiency with this topology was 70% switching at 30 MHz. A photograph of the prototype and thermal pictures of the converter are shown in Figs. 15 and 16, respectively. The bidirectional converter allows for lower conduction losses in the rectifier and allows for two-quadrant operation at the cost of an extra gate, which needs a control signal.

#### III. CHALLENGES OF VHF CONVERTERS

Lately, remaining research challenges have been described in [47] and [48]. This section summarizes the remaining challenges common in all above-described converters with respect to implementation in products. It is dividing the major remaining show stoppers into three categories and describes those afterward with respect to the existing products on the power supply market, with switching frequencies below the VHF range.





Fig. 16. Thermal photographs of bidirectional VHF converter in thermal equilibrium [46]. (a) Class-E inverter. (b) Class-E synchronous rectifier.

VHF operation of power supplies differs from submegahertz operated power supplies (here called traditional power converters) mainly by the following subjects:

- 1) electronic components, both active and passive;
- 2) circuit architectures for power stages and control parts;
- 3) adjacent behavior, such as electromagnetic compatibility (EMC), mechanics, and other reliability tests.

#### A. Components

Especially, inductive components are size, weight, and cost optimization limitations in nowadays power circuits. Simultaneously, VHF converters provide a major opportunity to overcome those.

Among the challenges are core losses, skin, and proximity effect [27], [49]–[54]. For driving further miniaturization of VHF power supplies, an obvious next step is to integrate the whole converter in a package (power supply in package) or even on a single chip (power supply on chip). The most challenging part for this goal is the integration of the inductors. Great progress has been made and summarized lately in [55], [56]. However, realizations of integrated inductors with Q-values beyond 100 in the relevant frequency ranges remain to be seen. Hybrid concepts, as shown in [57], might be applicable. Another challenge within passive components for VHF is the creation of a galvanic isolation barrier [58]–[60].

Despite passive components also active components, i.e., the power semiconductors, need to fulfill other requirements than in usual power supplies [61]–[63]. The parasitic components have a big influence on the design of the overall converter, as they are a part of the design parameters. Unlike traditional power stages, the parasitic elements are therefore not considered undesired, but form an integral part of the stage. An example is the output capacitance  $C_{oss}$  of the power semiconductor in a class-E-based power supply. According to [19], it is dependent on output power  $P_{out}$ , input voltage  $V_{in}$ , and switching frequency  $f_{sw}$ , as

$$P_{\rm out} = 2\pi^2 f_{\rm sw} C_{\rm oss} V_{\rm in}^2. \tag{3}$$

This means that the output capacitance  $C_{oss}$  limits the maximum switching frequency for a given application, which specifies  $P_{out}$  and  $V_{in}$ .

### B. Architectures

Where traditional power electronics circuits use squarewave gate drive signals, the presented VHF converters so far used sinusoidal gate drive [18], [24], [64], [65]. This is mainly due to the input capacitance  $C_{iss}$  of VHF power semiconductors, which require a high peak current at extremely high speed. To consider the drive voltage trapezoidal, its rise and fall times have to be less than 1 ns [65]. A trapezoidal or square-wave drive would minimize the time of the power switch in linear operation and therefore decreases the losses. The degrees of freedom in terms of modulation principles are less for VHF converters. Whereas power electronic circuits usually use pulsewidth modulation or phase modulation, the VHF converter efficiency is dependent on those parameters. Therefore, they need to be adjusted statically to avoid losses by leaving the ZVS (or ZCS) range. A way to get around this is to apply burst mode control [17], [64], [66]. This method, however, introduces another low-frequency component in the spectrum, which has to be buffered or filtered at both the in and output of the converter. A requirement that enforces the use of bulky components and therefore is counterproductive to the intended advantages of VHF converters in the first place. While the VHF converters offer good possibilities for fast transient regulations, their low-frequency control performance is limited by intrinsic bandpass behaviors through serial capacitors. Even though some rectifiers are available with parallel capacitances and impedance transformation [19], [67], more suitable architectures are missing. Thereby, it needs to be considered that the original VHF power circuits are designed to match a defined load (typically the impedance of the antenna), and therefore impedance transformation circuits can be realized in a passive way. Power converters however, are connected to highly varying loads, i.e., load circuit in idle-drawing no energy from the supply and full loaddemanding the maximum output from the supply. Therefore, active and lossless impedance matching circuits are required.

Having such circuits at hand opens for the utilization of the high gain bandwidth in VHF converters for line and load regulation.

#### C. Adjacencies

Finally, the interaction of VHF converters with its physical environment is different than the one of traditional power converters.

On the one hand, the electromagnetic interaction between circuits increases, the higher the relevant frequencies are [68]–[71]. Fields are distributed easier both inside the converter and to its surroundings. The electrical behavior also becomes highly dependent on electromechanical interfaces, such as cooling and housing. However, the harmonics of the resonant waveforms are falling faster than the harmonics in hard switched traditional power converters [20]. In addition, the harmonics of the fundamental switching frequency are spaced wider. That means the distance can be used to place strategically important EMC bands, dependent on the application.

On the other hand, the carefully adjusted operating points of VHF converters (for efficiency purposes) are highly dependent on temperature [19], [20]. Adaptive mechanisms for ensuring optimal operation over industry standard temperature ranges are yet to come.

#### IV. CONCLUSION

The merge of techniques used in radio communication electronics and power electronics was pointed out. The development through the previous decades has been revisited and the recent developments were summarized. Remaining challenges and the latest advances were described. The implementations of numerous VHF converters were presented. Among them are low-power, high-step-down converters with a switching frequency of 70 MHz and an efficiency beyond 70% as well as a 120-MHz, 9-W LED driver with an efficiency up to 89%. Both converters maintain high efficiencies over a wide load range.

The remaining challenges that require solutions before VHF converters can be implemented in numerous industrial applications were found to be within the categorizes components, circuit architectures, and reliability testing.

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Arnold Knott (M<sup>1</sup>10) received the Diplom-Ingenieur degree from the University of Applied Sciences, Deggendorf, Germany, in 2004, and the Ph.D. degree from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2010.

He has been with Harman/Becker Automotive Systems GmbH in Germany and USA, from 2004 to 2009, designing switch-mode audio power amplifiers and power supplies for automotive applications. He is involved in a research project under the title "Improvement of out-of-band Behaviour in Switch-

Mode Amplifiers and Power Supplies by their Modulation Topology." From 2010 to 2013, he was an Assistant Professor and an Associate Professor with the Technical University of Denmark since 2013. His current research interests include switch-mode audio power amplifiers, power supplies, active and passive components, integrated circuit design, acoustics, radio frequency electronics, electromagnetic compatibility, and communication systems.

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technologies.

Toke M. Andersen (S'10) received the B.Sc. and M.Sc. degrees from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2008 and 2010, respectively. He is currently pursuing the Ph.D. degree with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology Zürich, Zürich, Switzerland, in collaboration with IBM Research Zurich, Rüschlikon, Switzerland.

His current research interests include analysis, design, implementation, and optimization of on-chip power converters in deep submicrometer CMOS



Mickey P. Madsen (S'12) received the B.Sc.E.E. and M.Sc.E.E. degrees from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2009 and 2012, respectively. He is currently pursuing the Ph.D. degree in power electronics under the title "Very High Frequency Switch Mode Power Supplies."

His current research interests include switch-mode power supplies, resonant inverters/converters, wide band gab semiconductors, solid state (LED) lighting, and radio frequency electronics.



Peter Kamby received the B.Sc. and M.Sc. degrees from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2009 and 2012, respectively. His current research interests include very high frequency switch-mode power supplies, high current power conversion, and pulsed power.



Milovan Kovacevic (S'13) received the B.Sc. and M.Sc. degrees from the University of Belgrade, Belgrade, Serbia, in 2008 and 2010, respectively. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, Technical University of Denmark, Kongens Lyngby, Denmark. His current research interests include highfrequency power electronics, resonant and softswitching techniques, analog and mixed-signal circuit design, and control of power converters.



Jeppe A. Pedersen received the B.Sc. and M.Sc. degrees from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2010 and 2013, respectively.

He is currently a Research Assistant with the Technical University of Denmark. His current research interests include very high frequency switch-mode power supplies, bidirectional power conversion, and light-emitting diode drivers.



Michael A. E. Andersen (M'88) received the M.Sc.E.E. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1987 and 1990, respectively.

He is currently a Professor of power electronics with the Technical University of Denmark. Since 2009, he has been the Deputy Director with the Department of Electrical Engineering. He is the author or coauthor of more than 200 publications. His current research interests include switch-mode power supplies, piezoelectric transformers, power

factor correction, and switch-mode audio power amplifiers.

В

# Self-Oscillating Resonant Gate Drive for Resonant Inverters and Rectifiers Composed Solely of Passive Components

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# Self-Oscillating Resonant Gate Drive for Resonant Inverters and Rectifiers Composed Solely of Passive Components

Mickey P. Madsen\*, Jeppe A. Pedersen\*, Arnold Knott\*, Michael A. E. Andersen\* \*Technical University of Denmark

Ørsteds Plads, building 349 2800 Kongens Lyngby

Denmark

Email: {mpma, jarpe, akn, ma}@elektro.dtu.dk

Abstract—This paper presents a new self-oscillating resonant gate drive composed solely of passive components. The gate drive can be used in various resonant converters and inverters and can be used for both low and high side gate drive. The paper presents examples of how higher order harmonics can be used to improve the performance of the gate drive and how the gate drive can be implemented in a class E inverter, a class DE inverter and in class E inverter with a synchronous class E rectifier. The paper shows practical implementations of all the proposed inverters and converters operating in the Very High Frequency (VHF) range, all showing good results with peak efficiency up to 82% and output regulation from 70% to full load without bursting.

#### I. INTRODUCTION

In the early 70s the constant strive for small, cheap and efficient power supplies lead to the development of Switch-Mode Power Supplies (SMPS) [1]. As the size of modern power supplies are mainly governed by the passive energy storing elements, which scales inversely with the switching frequency, this strive has lead to constantly increasing switching frequencies ever since. Commercially available converters today switch at frequencies up to several megahertz and can have efficiencies of more than 95% (e.g. [2]).

The reason not to increase the switching frequency further and thereby reaching even higher power densities is the switching losses. For the last two decades (since 1988 [3]) research has been done in order to enable the use of resonant RF amplifiers (inverters) combined with a rectifier for dc/dc converters in order to avoid switching losses. With this type of converters SMPSs with switching frequencies in the Very High Frequency range (VHF, 30-300MHz) have been designed with efficiencies up to approx. 90%, [4], [5].

Several of the benefits and challenges of the increased switching frequency are described in [6], [7]. One of the big challenges is to drive the MOSFET without too high gating losses and so far resonant gate drives have shown to be the best solution for this [8], [9]. Control of these converters is also a challenge due to their resonant behavior and burst mode control has been used to overcome this challenge [10], [11], but it introduces spectral components at the bursting frequency. The compact, low cost converters that can be designed with these resonant converters are very well suited for LED lighting. Price, efficiency and reliability are key parameters in this market and with the presented gate drive the price can be reduced to a minimum without compromising the reliability or efficiency.

In section II of this paper a new type of resonant gate drive and several ways of designing it will be shown. Section III shows how the gate drive can be implemented in a complete circuit, both as low and high side gate drivers and used for synchronous rectification and bidirectional power conversion. Section IV shows results from various prototypes utilizing this gate drive and finally section V concludes the paper.

#### II. SELF-OSCILLATING GATE DRIVE

For a converter switching in the VHF range, hard gating leads to gating losses which are unacceptably high, at least for the semiconductors available today and for low to medium power levels [12], [13]. Several researchers have therefore used resonant gating to reduce the gating losses and drive the gate in an efficient way [14], [15]. All of these circuits need either a transformer, switching semiconductor, adjustable passives and/or feedback from other nodes in the circuit [16], [17].



Fig. 1. Schematic of the basic self-oscillating gate drive. The gate resistance and the body diode has been left out for simplicity.

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All these things adds to both price, size and complexity of the complete design.

This paper presents a new resonant gate drive solely constituted by passives around the main semiconductor. This leads to a robust and very simple and low cost gate drive.

The simplest implementation of the gate drive is shown in Fig. 1, the only thing added is an inductor at the gate of the semiconductor and a dc bias voltage. If the  $V_D$  is seen as input and  $V_G$  as output, the inductor and the parasitic capacitances composes a high pass filter with a capacitive load.

If this high pass filter is designed to have a gain,  $G = V_{GS,pp}/V_{DS,pp}$ , and have a phase shift close to  $180^{\circ}$  at the resonance frequency of the power stage, it will create a sine wave at the gate with a peak to peak voltage swing of  $V_{GS,pp}$  and a DC offset equal to  $V_{Bias}$ .

This dc offset can be used to control the switching frequency and the duty cycle of the power stage and thereby to regulate the output power. In some situations the parasitic capacitances of the MOSFET will lead to too high or too low gain at the desired frequency and additional capacitors,  $C_{GDext}$  and  $C_{GSext}$ , can be added to adjust this gain.

In order to improve the turn on speed of the MOSFET, and thereby lower the drain to source resistance, higher order harmonics can be added to the fundamental sine wave leading to a more trapezoidal gate signal. This can be achieved by adding small LC circuits between the gate and drain or source of the MOSFET (see Fig. 2). LC circuits connected to drain will cause the higher harmonics to be in phase with  $V_{DS}$  and LCs circuit connected to the source will cause the harmonics to be out of phase with  $V_{DS}$  (see Fig. 3).

The number of harmonics to include in a given design will depend on several parameters as price, complexity, efficiency etc. Adding higher order harmonics will in general increase the performance of the converter, but it is important to consider which harmonics to include and the magnitude of those harmonics compared to the fundamental. Fig. 4 shows the fundamental and the 3rd and 5th harmonics in and out of phase with the drain signal. It is clear that it is desirable to have the fundamental out of phase with the drain signal, but for the 3rd and 5th harmonic it depends on the duty cycle and the current waveform. From the figure it can be seen that it is desirable to have the 3rd harmonic out of phase for a duty cycle of 50%, but for a duty cycle of 25% it has to be in phase and will only add to the center part of the conducting period where the current usually is the smallest [18], [19]. The gate signals that can be achieved by adding harmonics are shown in Fig. 5.

#### III. USE IN RESONANT CIRCUITS

As the resonant gate drive is only relying on the resonance of the power stage and is floating between the drain and source of the MOSFET, it can be used in all resonant circuits. It can for instance be used in the class E inverter [20], [21], a class EF<sub>2</sub> ( $\phi_2$ ) inverter [22], [23], a resonant SEPIC [24], [25], a resonant boost converter [26], [27] or a class DE inverter (including high side gate drive) [28], [29], but it can also



Fig. 2. Schematic of the self-oscillating gate drive with the 2nd and 4th harmonic to source and drain.



Fig. 3. Examples of transfer functions from drain to source for different implementations of the resonant gate drive.



Fig. 4. The 1st, 3rd and 5th harmonics in and out of phase with the drain signal.



Fig. 5. Gate signals with higher order harmonics for 25% and 50% duty cycle (\*=signal in phase with  $V_{DS}$ ).

be used for synchronous rectification and bidirectional power flow.

#### A. In a class E inverter

The simple version of the gate drive implemented in a class E inverter is shown in Fig. 6. As the gate drive relies on the resonance of the inverter the switching frequency will automatically adjust for any tolerances in the passives,  $L_{IN}$ ,  $L_R$  and  $C_R$ . Furthermore the dependency on the resonance of the power stage gives and inherent open load protection as an open load situation will remove the resonance of the circuit.

When designing a class E inverter with the proposed gate drive, the design procedure will be first to design the power stage according to the specifications for the inverter, then select a proper MOSFET and finally design the gate drive for the selected MOSFET. An inverter with the specifications in table I will be designed in the following to give an example.

# TABLE I DESIGN SPECIFICATION FOR THE CLASS E INVERTER

$$\begin{array}{c|cccc} f_S & V_{IN} & P_{OUT} & R_L \\ \hline 50 \text{ MHz} & 45 \text{ V} & 5 \text{ W} & 25 \Omega \end{array}$$

The first step is to design the power stage and this can be done as described in [8]. The drain source voltage of the MOSFET is assumed to be a half wave rectified sine wave, hence the peak voltage is:

$$V_{IN} = \int V_{DS} = V_{DS,peak} \frac{2 \cdot (1 - D)}{\pi}$$

$$\Leftrightarrow$$

$$V_{DS,peak} = V_{IN} \frac{\pi}{2 \cdot (1 - D)}$$
(1)

The rms value of a half wave rectified sine wave is:

$$V_{DS,rms} = V_{DS,peak} \sqrt{\frac{D}{2}} \tag{2}$$

And the rms value of the output voltage is:

$$V_{OUT,rms} = \sqrt{P_{OUT} \cdot R_L} \tag{3}$$

According to [10] the reactance of the resonance circuit can now be determined by:

$$X_{RC} = R_L \cdot \sqrt{\left(\frac{V_{DS,rms}}{V_{OUT,rms}}\right)^2 - 1} \tag{4}$$

By combining equation 1, 2, 3, and 4, an expression for the needed reactance as function of input voltage, duty cycle, output power, and load is obtained:

$$X_{RC} = R_L \cdot \sqrt{\frac{V_{IN}^2 \cdot \pi^2 \cdot D}{2 \cdot (2 \cdot D - 2)^2 \cdot P_{OUT} \cdot R_L} - 1}$$
 (5)

From equation 1 it is found that a duty cycle of 45% will give a peak voltage of 128 V, leaving approximately 20% headroom if a 150 V MOSFET is used. Substituting this and the values from table I into equation 5 gives a reactance of 134



Fig. 6. Schematic of a class E inverter with self oscillating gate drive.



Fig. 7. Bodeplot of the transferfunction from drain to source for different gate inductors.



Fig. 8. Simulated class E inverter waveforms with the simple resonant gate drive.

 $\Omega.$  If a capacitor of 100 pF is used, the value of the inductor becomes 528 nH.

When designing low power inverters switching at VHF it is important to select a MOSFET with low  $C_{OSS}$  [8]. For this reason Fairchilds FDT86256 is selected and the values in table II are extracted from the datasheet.

TABLE II PARASITIC COMPONENTS OF FAIRCHILDS MOSFET FDT86256. PARASITIC CAPACITANCES TAKEN FOR  $V_{DS} = V_{IN}$ .

$$C_{DS}$$
 $C_{GS}$ 
 $C_{GD}$ 
 $R_{ON}$ 
 $R_G$ 

 15.3 pF
 55 pF
 1.2 pF
 1 Ω
 1.3 Ω

The effective output capacitance is  $C_{DS,eff} = \frac{C_{DS}}{1-D} = 30$  pF, hence the total inductance of the resonance circuit and the input inductor should be:

$$L_{total} = \frac{1}{\omega_R^2 \cdot C_{S,eff}}$$

Where  $\omega_R$  is given by:

$$\omega_R = \frac{\omega_S}{2 \cdot (1 - D)}$$

Knowing the values of  $X_{RC}$ , the input inductance can be calculated according to:

$$\begin{split} L_{total} &= \frac{1}{\frac{1}{L_{IN}} + \frac{\omega_R}{X_{RC}}} \\ & \uparrow \\ L_{IN} &= \frac{1}{\frac{1}{\frac{1}{L_{total}} - \frac{\omega_R}{X_{RC}}}} = 1.62 \ \mu \mathrm{H} \end{split}$$

The values of all the components in the power stages have now been calculated and the only thing remaining is the gate inductor. The gate signal should have an amplitude of 10  $V_{PP}$  and a phase shift as close to 180° as possible. The transferfunction from drain to source for different gate inductors is shown in Fig. 7.

From the plot it can be seen that the phase shift is around 175° for all the values of  $L_G$  at 40 MHz, but starts to decrease for the two largest inductors around the switching frequency. As the peak to peak voltage across the drain and source of the MOSFET is 128 V, a gain of  $20 \cdot log(10V/128V) = -22$  dB is needed to get a gate signal with an amplitude of 10  $V_{PP}$ . This is almost exactly what is achieved with the 140 nH inductor and as the phase shift is still 170° at the switching frequency this value is chosen for this design. Simulated waveforms of the designed inverter can be seen in Fig. 8.

The class E inverter (as most resonant circuits) behaves as a voltage controlled current source in open-loop situations; hence the output power increases with the input voltage. As the amplitude of the gate signal is a fixed ratio of the input voltage, a change in input voltage will lead to a change in amplitude of the gate signal. Hence the gate signal will be small at low input voltages, giving low gating losses at low power levels, and be large at high power, levels leading to lower conduction losses in the MOSFET.

#### B. Used for synchronous rectification in a class E rectifier



Fig. 9. Schematic of a class E dc/dc converter with synchronous rectification.

The self oscillating gate drive is very well suited for synchronous rectification as it doesn't require a control signal to control the phase between the two gate signals. The two gate signals will automaticly oscillate out of phase with the drainsource voltage of the MOSFET they are controling, hence the gate drive on the inverters side will act as a master drive and the rectifier drive act as a slave drive following the frequency set by the master drive. This principle automatically takes component tolerances and temperature variations of critical design parameters into account. If used in an isolated converter this will further more benefit from not having a control signal and hence no need for communication across the isolation barier. Fig. 8 shows how a dc/dc converter with synchronous rectification can be made with this gate drive. As it can be seen the converter is completely symmetric across the resonant tank,  $C_R$  and  $L_R$ , hence operation in both directions is possible allowing for bidirectional power flow.

#### C. Used for high side gate drive in a class DE inverter

An implementation of the self-oscillating resonant gate drive in a half bridge is shown in Fig. 7. Here the two MOSFETs have equally sized inductors at the gates, the only difference is that the other node of  $L_{G1}$  is connected to  $V_{bias}$  through  $L_H$ and to the switch node through  $C_{G1}$ . In this way the voltage at this node will follow the switch node but have a dc offset set by  $V_{Bias1}$ . As the phase of gate signals of the MOSFETs are directly coupled to drain source voltages, which are 180°



Fig. 10. Schematic of the class DE inverter with self oscillating gate drive.



Fig. 11. Picture of a SEPIC converter with the simple version of the gate drive.



Fig. 12. Measured waveforms of the SEPIC converter with the simple gate drive.

shifted, the gate signals will automatically be phase shifted and shoot through is avoided.

The simple version of the gate drive has been used for simplicity, but all the implementations can be used.

#### **IV. PRACTICAL IMPLEMENTATIONS**

A resonant SEPIC converter switching at 51MHz showing efficiency of 84% with the simple version of the gate drive has been implemented. A picture of the prototype is shown in Fig. 11 and the measured waveforms are shown in Fig. 12. By varying the bias voltage it is possible to regulate the output power from 4.3 W to 6.2 W. The efficiency is above 80% in the range 5-6.2 W but drops to 77% at the lowest output power. A plot of the power and efficiency for varying bias voltages is shown in Fig. 13.



Fig. 13. Measured efficiency and output power for varying bias voltages.



(a) Top



(b) Bottom

Fig. 14. A SEPIC converter with the gate inductor embedded in the PCB.

The three air core inductors takes up around half of the PCB footprint and they are the tallest components. In order to decrease the size further it is hence necessary to use another type of inductors. As the skin depth is very small and the maximum inductance 160 nH embedding the inductors in the PCB becomes a viable solution. A prototype of the same converter with the inductors embedded in the PCB has therefore been made [30] (see Fig. 14). Doing so the efficiency drops 2% but the power density increases approximately 4 times and the price becomes significantly lower.

The converter shown in Fig. 9 has also been implemented showing that the synchronous rectification works even without synchronization of  $M_1$  and  $M_2$  and allows for bidirectional power flow as well. The bidirectional converter is implemented as a class E inverter and a synchronous class E rectifier both using the simple self-oscillating gate drive.



Fig. 15. Picture of a class E inverter and a synchronous class E rectifier both with the simple version of the gate drive.



Fig. 16. Measured waveforms of the Class E converter with synchronous rectifier.



Fig. 17. Measured gate voltage of the SEPIC converter implemented with the gate drive with a 2.harmonic LC circuit connected to ground.

The reason for using a synchronous rectification is to minimize losses in the diode when dealing with low voltages and high currents; it also enables the converter to be used as a bidirectional converter. The converter with the synchronous rectifier is shown in Fig. 15. The converter reaches a maximum efficiency of 67% with the synchronous rectifier compared to 66.5% with a standard rectifier. The waveforms measured on the class E converter are shown in Fig. 16. It is evident that the inverter dictates the switching frequency. The simple gate drive in the rectifier is designed with an  $180^\circ$  phase shift from drain to gate at the switching frequency. This ensures that the rectifiers gate drive follows the same frequency as the inverter. Since the converter is implemented with a synchronous rectifier it could be used as a bidirectional converter with a load connected to the input of the inverter and a power source connected to the output of the rectifier. The transfer ratio  $\frac{V_{in}}{2A}$  was roughly the same in both directions  $\frac{14V}{2A} \approx \frac{5V}{730mA} \approx 7$ . The efficiency was kept above 50% when driven in reverse direction. The switching frequency was in this case dictated by the rectifier and the inverter just followed. With this self-oscillating gate drive it is possible to implement a small and cheap bi-directional converter using only a few passive components for driving the MOSFETs.

One of the more advance self-oscillating gate dives described earlier with a 2. harmonic LC circuit connected to ground is used with the SEPIC converter shown in Fig. 11. The transfer function is showed in Fig 3 is designed to remove the 2. harmonic and adding a 3. harmonic in phase with the fundamental. To ensure that the two peaks of the gate drives transfer function is placed above the fundamental frequency and the 3. harmonic the value of  $L_G$  is reduced and a small value for  $L_{2HS}$  is used. The total value of the inductances is reduced compared to the simple gate drive, in this case the total inductance was reduced by 45% which will free up more space when using PCB inductors.

The waveform of the gate voltage are shown in Fig. 17, it is evident that the gate signal generated by the more advance self-oscillating gate drive is more like a square wave than in 12. The peak-peak voltage is however twice of the simple gate drive and these increases the gate losses and in this case resulting in the efficiency reduction of a few % compared to the simple gate drive.

A implementation of a class DE inverter showing the function of the high side gate drive is shown in [31]. This is the first implementation of an off chip high side gate drive for operation in the VHF range.

#### V. CONCLUSIONS

This paper has presented several ways of designing a new self-oscillating resonant gate drive along with several examples of implementations in complete circuits. The presented gate drive is a simple, compact, low cost and reliable solution composed only of passive components. The gate drive is floating between the drain and source of the MOSFET and is directly coupled to the resonance frequency of the power stage. Due to this the gate drive can be used in all resonant circuits, also for high side drive and synchronous rectification. The gate drive offers an inherent open load protection and allows for synchronous rectification in isolated converters without synchronization across the isolation barrier. Finally the gate drive allows for output control without the low frequency ripple seen when utilizing burst mode control.

The paper has shown practical implementations of a low side gate drive, a high side gate drive and synchronous rectification and efficiencies up to 84% has been achieved.

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# Self-Oscillating Resonant Power Converter

Patent

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- (71) Applicant: DANMARKS TEKNISKE UNIVERSITET [DK/DK]; Anker Engelundsvej 1, Bygning 101A, 2. sal, DK-2800 Kgs. Lyngby (DK).
- (72) Inventors: MADSEN, Mickey P; Kollegiebakken 15A, st. 63, DK-2800 Kgs. Lyngby (DK). PEDERSEN, Jeppe Arnsdorf; Jagtvej 109E, DK-2200 Copenhagen N (DK).
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(57) Abstract: The present invention relates to resonant power converters and inverters comprising a self-oscillating feedback loop coupled from a switch output to a control input of a switching network comprising one or more semiconductor switches. The self-oscillating feedback loop sets a switching frequency of the power converter and comprises a first intrinsic switch capacitance coupled between a switch output and a control input of the switching network and a first inductor. The first inductor is coupled in-between a first bias voltage source and the control input of the switching network and has a substantially fixed inductance. The first bias voltage source is configured to generate an adjustable bias voltage applied to the first inductor. The output voltage of the power converter is controlled in a flexible and rapid manner by controlling the adjustable bias voltage.

## SELF-OSCILLATING RESONANT POWER CONVERTER

The present invention relates to resonant power converters and inverters comprising a self-oscillating feedback loop coupled from a switch output to a control input of a switching network comprising one or more semiconductor switches. The self-

- 5 oscillating feedback loop sets a switching frequency of the power converter and comprises a first intrinsic switch capacitance coupled between a switch output and a control input of the switching network and a first inductor. The first inductor is coupled in-between a first bias voltage source and the control input of the switching network and has a substantially fixed inductance. The first bias voltage source is
- 10 configured to generate an adjustable bias voltage applied to the first inductor. The output voltage of the power converter is controlled in a flexible and rapid manner by controlling the adjustable bias voltage.

# BACKGROUND OF THE INVENTION

- 15 Power density is always a key performance metric of a power supply circuit such as AC-DC, DC-AC and DC-DC power converters to provide the smallest possible physical size for a given output power specification. Resonant power converter topologies are well-known types of DC-DC/switched mode power supplies or converters (SMPS) in the art. Resonant power converters are particularly useful for high switch-
- 20 ing frequencies such as above 1 MHz where switching losses of standard SMPS topologies (Buck, Boost etc.) tend to be unacceptable for conversion efficiency reasons. High switching frequencies are generally desirable because of the resulting decrease of the electrical and physical size of circuit components of the power converter like inductors and capacitors. The smaller components allow increase of the
- 25 power density of the SMPS. In a resonant power converter an input "chopper" semiconductor switch (often MOSFET or IGBT) of the standard SMPS is replaced with a "resonant" semiconductor switch. The resonant semiconductor switch relies on the resonances of circuit capacitances and inductances to shape the waveform of either the current or the voltage across the switching element such that, when switching
- 30 takes place, there is no current through or voltage across the switching element. Hence power dissipation is largely eliminated in at least some of the intrinsic capacitances of the input switching element such that a dramatic increase of the switching frequency becomes feasible for example to values above 10 MHz. This concept is known in the art under designations like zero voltage and/or current switching (ZVS)

and/or ZCS) operation. Commonly used switched mode power converters operating under ZVS and/or ZCS are often described as class E, class F or class DE inverters or power converters.

5 However, fast and accurate control of the output voltage of the resonant power converter remains a challenge. Prior art power converters described in the references below propose to utilize a self-oscillating feedback loop around the input switching element and driven by the intrinsic or inherent drain-to-source capacitance of a MOSFET switch in combination with a variable series inductance coupled to the gate terminal of the MOSFET switch.

U.S. 4,605,999 discloses a self-oscillating power converter comprising a selfoscillating inverter circuit build around a single MOSFET switch. The inherent drainto-source capacitance of the MOSFET switch supplies a feedback path sufficient to

15 sustain self-oscillation of the inverter circuit if the frequency of operation is sufficiently high. The power converter is voltage regulated by a feedback loop deriving the control signal from a DC output voltage of the converter and applying the control signal to a variable inductance network comprising an inductor and a pair of nonlinear capacitances.

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U.S. 5,430,632 discloses a self-oscillating power converter utilizing a pair of MOSFET transistor switches in a half bridge configuration wherein the junction of the two MOSFET transistors is coupled to a reactive network which in turn is connected to an output rectifier. Intrinsic gate-to-drain inter-electrode capacitances of

25 the switching transistors serve as the sole means of sustaining oscillations. Oscillations are initiated at the gate-to-source terminals of the MOSFET transistor switches by a start-up circuit. The frequency of oscillation is determined by the gate-to-source capacitance of the MOSFET transistor switches and the inductance of an isolated gate drive transformer. The frequency of oscillation is controlled by varying induct-

30 ance of the isolated gate drive transformer coupled to the gate terminals of the MOSFET transistor switches through a pair of control windings.

However, the possible regulation range of adjustable inductances and/or capacitances tend to be very narrow due to physical component limitations and the accu-

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racy may also be limited. Furthermore, adjustable inductances and/or capacitances are difficult to integrate on semiconductor substrates or on ordinary circuit carriers like printed circuit boards. Finally, the maximum regulation speed of the inductance or capacitance may be limited due to the reactive nature of the component leading

5 to an undesirable limitation of the speed of the regulation of the converter output voltage. This is of course particularly undesirable in view of the advantages of moving to higher converter switching frequencies for the reasons discussed above.

Consequently, it would be advantageous to provide a control mechanism for the oscillation frequency that eliminates the need of variable reactive components like inductors and capacitors such that the converter output voltage can be controlled by appropriately controlling a level of a circuit voltage or circuit current for example in the form of an adjustable bias voltage

# 15 SUMMARY OF THE INVENTION

A first aspect of the invention relates to a resonant power converter or inverter comprising an input terminal for receipt of an input voltage and a switching network comprising one or more semiconductor switches controlled by respective control inputs. The switching network comprises a switch input operatively coupled to the

- 20 input terminal for receipt of the input voltage and a switch output operatively coupled to an input of a resonant network of the resonant power converter. The resonant network comprises a predetermined resonance frequency (f<sub>R</sub>) and an output operatively coupled to a converter output terminal. A self-oscillating feedback loop is coupled from the switch output to a control input of the switching network to set a
- 25 switching frequency of the power converter. The self-oscillating feedback loop comprises a first intrinsic switch capacitance coupled between the switch output and the control input of the switching network,

a first bias voltage source configured to generate a first adjustable bias voltage, a first inductor with substantially fixed inductance coupled in-between the first bias

30 voltage source and the control input of the switching network. A voltage regulation loop of the resonant power converter is configured to control an output voltage of the power converter by controlling the first adjustable bias voltage applied to the first inductor. The present resonant power converter allows flexible, rapid and accurate control of the converter output voltage by controlling the adjustable bias voltage applied to the first inductor coupled to the control input of the switching network. By adjusting a level of the adjustable bias voltage, an oscillation frequency of the self-oscillating

- 5 feedback loop coupled around the switching network can be controlled so as to set a switching frequency of the resonant power converter. The adjustment of the oscillation frequency of the self-oscillating feedback loop is achieved without making any adjustment of the inductance of the first inductor which therefore has a substantially fixed inductance independent of the level of the adjustable bias voltage. The skilled
- 10 person will understand that the term "substantially fixed" characterizing the inductance of the first inductor includes an inductance that vary slightly over temperature depending on electrical characteristics of a particular material of the selected inductor type. Furthermore, the application of the first adjustable bias voltage to the first inductor is preferably carried out without any adjustment of an inductive or capaci-
- 15 tive reactance of a component coupled in series with the first inductor in the voltage regulation loop. Hence, the first adjustable bias voltage generated by the voltage regulation loop is preferably applied to the first inductor without any transformer, tuneable inductor or tuneable capacitor in series with the first inductor.
- 20 The ability of adjusting the switching frequency of the present resonant power converter by adjusting the level of the first adjustable bias voltage enables a wide and accurate control range of the switching frequency and eliminates or circumvents the previously discussed disadvantages of relying on adjustable inductances and/or capacitances to adjust the switching frequency of the resonant power converter.
- 25 Power losses in intrinsic or parasitic capacitances such as the first intrinsic switch capacitance of the one or more semiconductor switches are furthermore reduced to a low level by the presence of first inductor because energy stored in these parasitic capacitances during charging is discharged to, and temporarily stored in, the first inductor. The stored energy in the first inductor is subsequently returned to parasitic
- 30 or intrinsic capacitances of the one or more semiconductor switches. The parasitic or intrinsic capacitances may comprise gate-source, gate-drain and drain-source capacitances of a MOSFET switch.

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While the present invention is described in detail in the following with reference to implementations in resonant power converters/inverters and corresponding DC-DC power converters of Class E or DE type or topology, the skilled person will understand that the invention is equally applicable to other types of resonant power inverters, rectifiers and converters such as class E, F, DE and  $\pi_2$  inverters and rectifiers and rectifiers and resonant boost, buck, SEPIC, LCC, LLC converters etc.

The voltage regulation loop may comprise a reference voltage generator supplying a DC or AC reference voltage to a first input of a comparator or error amplifier. A second input of the comparator may be coupled to the converter output voltage and an output of the comparator may be operatively coupled to a control input of the first bias voltage source. In this manner, the comparator or error amplifier may be configured to generate a suitable error signal as control signal for the first bias voltage source by a comparison of the output voltage of the converter with the DC or AC reference voltage. The error signal or signals applied to the first bias voltage source increases or decreases the first adjustable bias voltage in an appropriate direction to adjust the converter output voltage to the target output voltage indicated by the DC or AC reference voltage as explained in additional detail below in connection with the accompanying drawings.

The skilled person will appreciate that the switching network can comprise numerous types of switch topologies such as single switch topology, half-bridge or fullbridge switch topologies. According to a preferred embodiment, the switching network comprises a first semiconductor switch with a control terminal coupled to the control input of the switching network and an output terminal coupled to the switch input and to the switch output. An input inductor is coupled between the input voltage and the switch input. This embodiment may comprise a basic class E power inverter or converter wherein the switching network comprises a single semiconduc-

tor switch with its output terminal, e.g. a drain terminal of a MOSFET, coupled both

30 to the input and output of the switching network. The input inductor forms part of the resonant network to control the setting of the predetermined resonance frequency (f<sub>R</sub>). The control terminal, e.g. a gate or base terminal, of the single semiconductor switch is coupled to the control input of the switching network.

The input inductor and the first inductor may be magnetically coupled with a predetermined magnetic coupling coefficient, preferably a magnetic coupling coefficient larger than 0.1 or even more preferably larger than 0.4. The magnetic coupling provides a number of advantages relative to the case of uncoupled input and first induc-

- 5 tors such as improved phase response between the signal at the control input of the switching network and the switch output and larger and more constant gain. The magnetic coupling ensures that the inductor currents of the input inductor and first inductor are out of phase. Consequently, a phase shift between the control input signal, e.g. a gate voltage of the MOSFET switch, of the switching network and the
- 10 switch output is very close to 180 degrees. Furthermore, the magnetic coupling is preferably substantially constant across a wide frequency range to provide a more constant level of the first adjustable bias voltage when the output voltage V<sub>OUT</sub> of the power converter is regulated.

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Another preferred embodiment of the present resonant power converter comprises a half-bridge based switching network. The switching network comprises a first semiconductor switch coupled between the switch output and a voltage supply rail of the resonant power converter and having a control terminal coupled to the control input

- 20 of the switching network. The switching network additionally comprises a second semiconductor switch coupled between the switch output and the input terminal. A control terminal of the second semiconductor switch is coupled to a second bias voltage source through a cascade of a second inductor with substantially fixed inductance and a third inductor with substantially fixed inductance. A feedback
- 25 capacitor of the switching network is coupled between the switch output and an intermediate node between the second and third inductors. This embodiment of the present resonant power converter may comprise a class DE power converter, invertor or form part of a class DE based DC-DC power converter.
- 30 The feedback capacitor serves as a bootstrap device which raises a voltage level supplied to the control terminal of the second semiconductor switch and thereby facilitates use of a N-channel MOSFET transistor as semiconductor switch device. The second inductor serves as a high impedance signal path at the oscillation frequency allowing passage of a relatively slowly varying bias voltage component gen-
erated by the second bias voltage source, but blocking passage of a relatively high frequency voltage component supplied through the feedback capacitor. Consequently, by combining bias voltage components supplied through the second inductor and the feedback capacitor, the control voltage at the second switch is level

- shifted and referred to the switch output instead of the voltage supply rail of the first semiconductor switch such as ground or a negative power supply voltage if the input voltage is a positive DC voltage. The self-oscillation loop may be configured to ensure that each of the semiconductor switches S<sub>1</sub> and S<sub>2</sub> is alternately switched between conducting and non-conducting states. The semiconductor switches S<sub>1</sub> and S<sub>2</sub> are also switched in opposite phase according to a non-overlapping scheme.
  - The first inductor and the third inductor may be magnetically coupled with a predetermined magnetic coupling coefficient, preferably a magnetic coupling coefficient
- larger than 0.1 or even more preferably larger than 0.4. The magnetic coupling will
  force a phase shift that is substantially 180 degrees between the control input signals, e.g. gate signals or voltages, of the first and second semiconductor switches.
  To provide a large magnetic coupling coefficient between the input inductor and the first inductor these may be wound around a common magnetically permeable member or core. For the same reason, the first inductor and the third inductor may be
- 20 wound around a common magnetically permeable member or core.

The first bias voltage source may be configured in various ways. In one embodiment, the first bias voltage source may be coupled between a suitable DC bias or reference voltage of the resonant power converter and a ground potential or nega-

- 25 tive supply rail thereof. The first adjustable bias voltage may be derived from the DC bias or reference voltage by suitable voltage division or regulation circuitry. In one embodiment, the first bias voltage source comprises a capacitor coupled from the first adjustable bias voltage to a fixed electric potential of the resonant power converter such as ground. A first adjustable resistor is coupled between the first adjust-
- 30 able bias voltage and a first DC reference voltage and a second adjustable resistor is coupled between the first adjustable bias voltage and a second DC reference voltage. The first DC reference voltage may possess a DC voltage higher than a maximum peak voltage of the first adjustable bias voltage. The second DC reference voltage may possess a DC voltage lower than an expected minimum voltage

of the first adjustable bias voltage such that the first adjustable bias voltage can be varied through a suitable voltage regulation range by adjusting a resistance ratio between the first and second adjustable resistances. Each of the first and second adjustable resistors preferably comprises a MOS transistor allowing the respective

5 resistances to be controlled from a high impedance gate terminal of the MOS transistor.

The first inductor may have an inductance between 1 nH and 10  $\mu$ H such as between 1 nH and 50 nH. The latter inductance range makes it possible to form the

10 first inductor as an electrical trace pattern of a printed circuit board or as an integrated passive semiconductor component leading to considerable size reduction and reliability advantages of the resonant power converter.

The substantially fixed inductance of the first inductor is preferably determined ex-

- 15 perimentally for example by adjusting its value until a suitable voltage swing is obtained at the control input of the switching network as explained below in additional detail. Preferably, the substantially fixed inductance is set such that a peak voltage at the control input of the switching network exceeds a threshold voltage of at least one of the semiconductor switches of the switching network. This threshold voltage
- 20 may for example lie between 5 and 10 V for an N-channel power MOSFET, but the skilled person will appreciate that other types of semiconductor switches may have different threshold voltages depending on characteristics of the semiconductor technology in question.
- In one embodiment, the substantially fixed inductance of the first inductor is selected such that a peak-peak voltage swing at the control input of the switching network is approximately equal to a numerical value of the threshold voltage of the at least one of the semiconductor switches of the switching network. In the above-mentioned example in respect of the N-channel power MOSFET, the peak-peak voltage swing would accordingly be adjusted to a value between 5 and 10 V in accordance with
- the threshold voltage.

In another embodiment, the self-oscillating feedback loop comprises a series resonant circuit coupled in-between the control input of the first semiconductor switch

and a fixed electric potential of the converter. The series resonant circuit preferably comprises a cascade of capacitor and an inductor connected between the control input of the semiconductor switch and a negative power supply rail e.g. ground. The series resonant circuit functions to introduce additional uneven frequency compo-

5 nents, by attenuating one or more even harmonic frequency components, to a fundamental frequency component of the oscillating voltage waveform at the control input of the switching network, e.g. the gate of the first semiconductor switch. This leads to a trapezoidal waveform shape of the oscillating voltage waveform and results in faster switch turn-on and turn-off times.

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A useful embodiment of the present resonant power converter comprises a DC-DC power converter. The DC-DC power converter is preferably constructed or derived by coupling a rectifier between the output of the resonant network and the inverter or converter output terminal to generate a rectified DC output voltage. The rectifier may

- 15 comprise one or more diodes to provide passive rectification of the DC output voltage. The rectifier of an alternative embodiment of the resonant power converter comprises a synchronous rectifier which may comprise one or more semiconductor switches. According to one such embodiment the synchronous rectifier comprises: a rectification semiconductor switch configured to rectify an output voltage of the
- 20 resonant network in accordance with a rectifier control input of the rectification semiconductor switch. A first rectification inductor with a substantially fixed inductance is coupled in-between a fixed or adjustable rectifier bias voltage and the rectifier control input. It is a significant advantage of this embodiment that the fixed or adjustable rectifier bias voltage of the rectifier may be left decoupled or unconnected to the first
- 25 bias voltage source generating the first adjustable bias voltage for the switching network on the input side of the resonant power converter for the reasons discussed in detail below with reference to FIG. 8 of the appended drawings. The fixed or adjustable rectifier bias voltage may for example be coupled to a fixed DC bias voltage source of the resonance power converter or to the rectified DC output voltage
- 30 through a resistive or capacitive voltage divider.

The skilled person will appreciate that numerous types of semiconductor transistors may be used to implement each of the first and second semiconductor switches depending on requirements such as threshold voltage, gate source break-down voltage, drain source break-down voltage etc., imposed by any particular resonant power converter. Each of the first and second semiconductor switches may for example comprise a MOSFET or IGBT such as a Gallium Nitride (GaN) or Silicon Carbide (SiC) MOSFET.

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A second aspect of the invention relates to a resonant power converter assembly comprising a resonant power converter according to any of the above described embodiments thereof and a carrier substrate having at least the switching network and the resonant circuit integrated thereon wherein an electrical trace pattern of the

10 carrier substrate is forming the first inductor. The carrier substrate may comprise a single-layer or multi-layer printed circuit board with integrally formed electrical wiring patterns interconnecting various electronic components of the resonant power converter. The relative small inductance required for the first inductance for achieving VHF switching frequencies of the power converter, e.g. in the order of tens of nH,

15 facilitates an advantageous integration of the first inductor, and potentially other inductors of the power converter of suitable size, directly in the wiring pattern of carrier substrates like printed circuit boards. This type of integration leads to several advantages such as saving component costs, reducing assembly time and costs and possibly improving reliability of the power converter assembly.

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A particularly advantageous embodiment of the carrier substrate comprises a semiconductor die, such as a CMOS based integrated circuit, integrating all active and passive components of the present resonant power converter thereon.

## 25 BRIEF DESCRIPTION OF THE DRAWINGS

A preferred embodiment of the invention will be described in more detail in connection with the appended drawings, in which:

FIG. 1A) is an electrical circuit diagram of a class E resonant power converter in accordance with a first embodiment of the invention,

30 FIG. 1B) is an electrical circuit diagram of a class E resonant power converter comprising a pair of magnetically inductors in accordance with a second embodiment of the invention, FIG. 2A) is an electrical circuit diagram of a class E resonant power converter comprising a series resonant circuit in accordance with a third embodiment of the invention,

FIG. 2B) is an electrical circuit diagram of a class E resonant power converter com-

5 prising a series resonant circuit in accordance with a fourth embodiment of the invention,

FIG. 2C) is an electrical circuit diagram of a gate drive circuit for class E and DE resonant power converters comprising a plurality of series resonant circuits, FIG. 2D) shows a plurality of magnitude and phase response curves of transfer

- 10 functions of a MOSFET switch of the class E resonant power converter in accordance with the third embodiment of the invention, FIG. 2E) shows a plurality of control input signal waveforms of the MOSFET switch of the class E resonant power converter in accordance with the third embodiment of the invention,
- 15 FIG. 3A) is an electrical circuit diagram of a class DE resonant power converter in accordance with a fifth embodiment of the invention, FIG. 3B) is an electrical circuit diagram of a class DE resonant power converter comprising a pair of magnetically coupled inductors in accordance with a sixth embodiment of the invention,
- 20 FIG. 4 is an electrical circuit diagram of an exemplary DC-DC power converter based on the class E resonant power converter in accordance with the first embodiment of the invention,

FIG. 5 shows a series of graphs illustrating voltage waveforms at the output of a switching network of the class E resonant power converter of the first embodiment

- 25 for different bias voltage levels applied to the control input of the switching network, FIG. 6 is a circuit simulation model of a second exemplary DC-DC power converter based on the first embodiment of the class E resonant power converter, FIG. 7 shows a series of graphs illustrating various simulated voltage waveforms of the second DC-DC power converter for four different DC bias voltage levels of an
- 30 adjustable bias voltage; and FIG. 8 is an electrical circuit diagram of a third DC-DC power converter with synchronous rectification on the output side based on the class E resonant power converter in accordance with the first embodiment of the invention

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. 1A) is a simplified electrical circuit diagram of a class E resonant power converter 100 in accordance with a first embodiment of the invention. The present class E resonant power converter is particularly well-adapted for operation in the VHF

- 5 frequency range for example at switching frequencies above 10 MHz or even higher such as between 30 and 300 MHz due to, amongst other factors, low switching losses in connection with the operation of a self-oscillating feedback loop connected around a transistor switch element S<sub>1</sub> as explained in further detail below. The class E resonant power inverter or converter 100 comprises an input pad or
- 10 terminal 102 for receipt of a DC input voltage V<sub>IN</sub> from a DC power supply 104. The DC voltage level may vary considerably according to requirements of any particular conversion application such as lying between 1 V and 500 V for example between 10 V and 230 V. A switching network comprises a single switch transistor S<sub>1</sub>. The skilled person will understand that the switch transistor S<sub>1</sub> can comprise different
- 15 types of semiconductor transistors such as MOSFETs and IGBTs. The skilled person will likewise understand that the switch transistor S<sub>1</sub> in practice can be formed by a plurality of parallel separate transistors e.g. to distribute operational currents between multiple devices. In one embodiment of the invention, S<sub>1</sub> is formed by an IRF5802 power MOSFET available from the manufacturer International Rectifier. A
- 20 gate terminal  $V_{GS}$  of the switch transistor  $S_1$  forms a control input of the switching network allowing  $S_1$  to be switched between a conducting state or on-state with low resistance between the drain and source terminals and a non-conducting state or off-state with very large resistance between the drain and source terminals. A drain terminal  $V_{DS}$  of the switch transistor  $S_1$  forms both a switch input and a switch output
- 25 of the switching network in the present embodiment based on a single switch transistor. The drain terminal  $V_{DS}$  is at one side coupled to the DC input voltage through an input inductor  $L_{IN}$  (108). The drain terminal  $V_{DS}$  is also coupled to a first side of a series resonant network comprising resonant capacitor  $C_R$  and resonant inductor  $L_R$ . The input inductor  $L_{IN}$  resonant capacitor  $C_R$ , an intrinsic drain-source capacitance
- 30 C<sub>DS</sub> of the MOSFET S<sub>1</sub> and the resonant inductor L<sub>R</sub> (112) form in conjunction a resonant network of the power converter 100. A second and opposite side of the series resonant network is operatively coupled to an output terminal 114 or node of the class E resonant power converter 100 either directly as illustrated or through a suitable rectification circuit as illustrated in detail below. An inverter load is schematical-

Iy indicated by a load resistor  $R_{LOAD}$  connected to the converter at the output terminal 114 and may generally exhibit inductive, capacitive or resistive impedance. The resonant network is designed with a resonance frequency ( $f_R$ ) of about 50 MHz in the present implementation, but the resonance frequency may vary depending on

- requirements of the application in question. In practice, the respective values of the resonant capacitor C<sub>R</sub> and resonant inductor L<sub>R</sub> may be selected such that a target output power at the converter output is reached for a particular load impedance. Thereafter, the value of the input inductor L<sub>IN</sub> is selected such that a desired or target value of the predetermined resonance frequency (f<sub>R</sub>) is reached in view of the intrinsic drain-source capacitance C<sub>DS</sub> for the selected switch transistor.
  - The present class E resonant power converter 100 comprises a self-oscillating feedback loop arranged around the transistor switch S<sub>1</sub> such that the oscillation frequency of the loop sets the switching or operational frequency of the power convert-
- 15 er 100 as briefly mentioned above. The self-oscillating feedback loop comprises an intrinsic gate-drain capacitance  $C_{GD}$  of the transistor switch  $S_1$  which transmits a 180 degree phase shifted portion of the switch output signal at the drain terminal  $V_{DS}$ back to the gate terminal of the transistor switch  $S_1$ . Additional loop phase shift is introduced by the gate inductor  $L_G$  which preferably comprises a substantially fixed
- 20 inductance. The gate inductor  $L_G$  is coupled in-between a variable bias voltage  $V_{Bias}$ and the gate terminal of the transistor switch  $S_1$ . The variable bias voltage  $V_{Bias}$  is generated by a bias voltage generator or source with a design explained in further detail below in connection with FIG. 4. However, the adjustable bias voltage  $V_{Bias}$ applied to the gate terminal of transistor switch  $S_1$  through the gate inductor  $L_G$  pro-
- vides an advantageous mechanism for controlling the converter output voltage V<sub>OUT</sub>. This mechanism exploits that the time period of the cycle time, the cycle time being the reciprocal of the oscillation frequency of the feedback loop, during which S<sub>1</sub> remains in a non-conducting state is controlled by the previously mentioned components of the resonant network defining the resonance frequency (f<sub>R</sub>). The latter fre-
- 30 quency controls when the voltage at the switch output at V<sub>DS</sub> reaches ground or zero volts, being the lower power supply rail of the converter in the present embodiment, and thereby allowing S<sub>1</sub> to be turned on again without introducing switching losses to discharge the intrinsic drain-source capacitance C<sub>DS</sub>. This operation mechanism where the resonant circuit is used to discharge the intrinsic semiconductor switch

capacitance until the voltage across the semiconductor switch reaches approximately zero is normally denoted zero voltage switching (ZVS) operation.

Conversely, the time period of the cycle time during which S1 remains conducting, or

- 5 in its on-state, can be controlled by the level of the adjustable bias voltage. This property allows a duty cycle, and hence the oscillation frequency of the self-oscillating loop, to be adjusted. This is explained in further detail in connection with FIG. 5 below. Since the switch output at  $V_{DS}$  is coupled directly to the DC input voltage through the input inductor  $L_{IN}$  the average voltage at the switch output  $V_{DS}$  is
- 10 forced to equal the DC input voltage. The integral of a half-period sine waveform of frequency (f<sub>R</sub>) equals the sine amplitude divided by pi times the resonance frequency (f<sub>R</sub>). Furthermore, when S<sub>1</sub> is conducting the voltage across S<sub>1</sub> is essentially zero such that the voltage at the switch output V<sub>DS</sub> becomes substantially zero. These circumstances lead to the following equation for a peak voltage, V<sub>DS,PEAK</sub>, across S<sub>1</sub>:

$$V_{DS,PEAK} = \frac{V_{IN} * \pi * f_R}{f_S} \qquad (1);$$

wherein  $f_S$  = The oscillation frequency of the self-oscillation loop which equals the switching frequency of the power converter.

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Equation (1) reveals that a decreasing oscillation frequency leads to increasing switch output voltage  $V_{DS}$  as illustrated below by switch output voltages  $V_{DS}$  of FIG. 5.

- 25 The voltage waveforms, duty cycle control and oscillation frequency control discussed above are illustrated on the graphs 500, 510 and 520 of FIG. 5 for three different levels of the adjustable bias voltage V<sub>Bias</sub> applied to the substantially fixed inductance gate inductor L<sub>G</sub>. The scale on the y-axis of all graphs indicates voltage in volts while the x-axis scale indicates time in steps of 10 ns such that the entire x-
- 30 axis spans over about 100 ns. As mentioned above,  $L_G$  is coupled to the control input or gate  $V_{GS}$  of the transistor switch  $S_1$ . In graph 500, the adjustable bias voltage  $V_{Bias}$  has been adjusted to a level which results in a duty cycle of approximately 0.5 in the switch output voltage  $V_{DS}$ . Waveform 501 shows the switch output voltage  $V_{DS}$

while waveform 503 shows the corresponding gate-source voltage applied to the gate  $V_{GS}$  of  $S_1$ . It is evident that the cycle time of the switch output voltage  $V_{DS}$  is about 10 s corresponding to an oscillation frequency of about 100 MHz.

- 5 In practice, the substantially fixed inductance of the gate inductor L<sub>G</sub> may be selected such that a desired voltage amplitude of the (oscillating) gate-source voltage waveform is achieved. The voltage amplitude is preferably adjusted such that a suitable peak voltage at the gate terminal of MOSFET switch S<sub>1</sub> is reached in view of its threshold voltage and its gate break-down voltage. This means that the peak voltage
- 10 at the gate terminal should be sufficiently large to exceed the threshold voltage of the chosen semiconductor switch, e.g.  $V_{TH}$  of MOSFET switch  $S_1$ . The oscillation frequency  $f_S$  of the self-oscillation loop will inherently lie close to the resonance frequency ( $f_R$ ) of the resonant network if the bias voltage is adjusted approximately to the threshold voltage of the MOSFET switch  $S_1$ . If the adjustable bias voltage  $V_{Bias}$  is
- 15 increased above the threshold voltage, the on-period of the MOSFET switch S<sub>1</sub> increases and leads to increase of the duty cycle of the oscillating switch output voltage waveform. This leads to a decreasing oscillation frequency or switching frequency of the power converter. The decrease of the oscillation frequency leads to an increase of the peak voltage V<sub>DS,PEAK</sub> at the switch output as explained above in
- 20 connection with equation (1), and a corresponding increase of the peak voltage across the series resonant network comprising resonant capacitor C<sub>R</sub> and resonant inductor L<sub>R</sub> due to its coupling to the switch output voltage V<sub>DS</sub>. Furthermore, because the series resonant network exhibits inductive impedance, the decreasing oscillation frequency of the switch output voltage waveform leads to a decrease of
- 25 the impedance of the series resonant network. The decrease of impedance leads in turn to increasing current and power through the series resonant network and through the load resistor  $R_{LOAD}$  in effect increasing the converter output voltage  $V_{OUT}$ .
- 30 Consequently, the converter output voltage  $V_{OUT}$  can be controlled by appropriately controlling the adjustable bias voltage  $V_{Bias}$  applied to the substantially fixed inductance gate inductor L<sub>G</sub>. This feature provides a highly flexible and fast way of controlling the converter output voltage  $V_{OUT}$  compared to prior art mechanism based on adjustable inductances and/or capacitances. In particular, the range of

adjustment of the adjustable bias voltage  $V_{\text{Bias}}$  can be very wide compared to the possible regulation range of the adjustable inductances and/or capacitances.

In graph 510, the adjustable bias voltage  $V_{\mbox{\tiny Bias}}$  has been increased to a level which

- 5 results in a duty cycle of approximately 0.7 in the switch output voltage  $V_{DS}$ . Waveform 511 shows the switch output voltage  $V_{DS}$  while waveform 513 shows the corresponding gate-source voltage applied to the gate  $V_{GS}$  of S<sub>1</sub>. As illustrated, the switch output voltage  $V_{DS}$  has increased from a peak level of approximately 30 volt for the 0.5 duty cycle condition depicted above to approximately 50 volt. It is evident that
- 10 the cycle time of the switch output voltage V<sub>DS</sub> has decreased to about 18 ns corresponding to an oscillation frequency of about 55 MHz. Finally, in graph 520, the adjustable bias voltage V<sub>Bias</sub> has been further increased to a level which results in a duty cycle of approximately 0.9 in the switch output voltage V<sub>DS</sub>. Waveform 521 shows the switch output voltage V<sub>DS</sub> while waveform 523 shows the corresponding
- 15 gate-source voltage applied to the gate  $V_{GS}$  of  $S_1$ . As illustrated, the switch output voltage  $V_{DS}$  has further increased from a peak level of approximately 50 volt for the 0.7 duty cycle condition depicted above to approximately 150 volt. It is evident that the cycle time of the switch output voltage  $V_{DS}$  has further decreased to about 50 ns corresponding to an oscillation frequency of about 20 MHz.

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FIG. 1B) is an electrical circuit diagram of a class E resonant power converter 100b comprising a pair of magnetically coupled inductors in accordance with a second embodiment of the invention. The skilled person will appreciate that the above discussed features, functions and components of the first embodiment of the class E resonant power converter 100 may apply to the present embodiment as well. Likewise, corresponding components in the first and second embodiments of the present class E resonant power converter have been provided with corresponding reference numerals to ease comparison. The main difference between the first and second embodiments is that the previously discussed separate and substantially uncoupled input inductor L<sub>IN</sub> and gate inductor L<sub>G</sub> have been replaced by the pair of magneti-

cally coupled inductors  $L_{In}$  and  $L_G$  where the respective functions in the present class E resonant power converter 100b are similar to those of the first embodiment. The skilled person will appreciate that magnetic coupling between the input inductor  $L_{In}$  and gate inductor  $L_G$  may be achieved in numerous ways for example by a close-

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ly spaced arrangement of the inductors e.g. coaxially arranged. The magnetic coupling provides a number of advantages over the first embodiment such as improved phase response between the control input and switch output of the MOSFET switch  $S_1$  and larger and more constant gain. The magnetic coupling ensures that the re-

- 5 spective inductor currents of the input inductor L<sub>in</sub> and gate inductor L<sub>G</sub> are out of phase. Consequently, the phase shift between control input of the switch S<sub>1</sub> and the switch output is very close to 180 degrees. Furthermore, the magnetically coupled input inductor L<sub>in</sub> and gate inductor L<sub>G</sub> may be configured such that the magnetic coupling is substantially constant across a wide frequency range to provide a more
- 10 constant level of the first adjustable bias voltage when the output voltage V<sub>OUT</sub> of the power converter is regulated.

The magnetic coupling between the magnetically coupled input inductor  $L_{in}$  and gate inductor  $L_G$  may also be accomplished by a transformer structure as schematically indicated on FIG. 1B). The input inductor  $L_{in}$  and gate inductor  $L_G$  may for example

be wound around a common magnetically permeable member or core. The latter embodiment has the advantage of a stronger coupling of magnetic fields between the input inductor  $L_{in}$  and gate inductor  $L_G$ . This forces a phase shift even closer to 180 degrees between the control input of the switch  $S_1$  (i.e. gate voltage of switch

 $S_1$ ) and the switch output (i.e. drain voltage of the switch  $S_1$ ).

The magnetically coupled input inductor  $L_{in}$  and gate inductor  $L_G$  may be configured to possess a magnetic coupling which is sufficient to ensure that inductor current forced in  $L_G$  by  $L_{iN}$  is sufficiently large to drive the control input of the switch  $S_1$ . In this case the gate drive can also be used to drive cascode coupled transistors where the intrinsic capacitance  $C_{GD}$  is small or non-existent.

FIG. 2A) is a simplified electrical circuit diagram of a class E resonant power converter 200 in accordance with a third embodiment of the invention. The present
power converter is of similar topology to the above discussed power converter based on a single switch transistor S<sub>1</sub>. The skilled person will appreciate that the above discussed features, functions and components of the first embodiment may apply to the present embodiment as well. Likewise, corresponding components in the first and second embodiments of the present class E resonant power converter

have been provided with corresponding reference numerals to ease comparison. The main difference between the first and second embodiments lies in an addition of a series resonant circuit, comprising a cascade of capacitor  $C_{MR}$  and inductor  $L_{MR}$ , connected between the gate node or terminal  $V_{GS}$  of switch transistor  $S_1$  and the

- 5 negative supply rail e.g. ground. The function of the series resonant circuit is to introduce additional uneven frequency components, by attenuating one or more even harmonic frequency components, to the fundamental frequency component of the oscillating gate voltage waveform of the switch transistor S<sub>1</sub>. This leads to a trapezoidal waveform shape of the gate voltage of switch transistor S<sub>1</sub> leading to faster
- 10 switch turn-on and turn-off times. This is beneficial because it reduces the conduction losses, as the switch MOSFET S<sub>1</sub> will have relatively high resistance when the gate voltage is just above the threshold voltage. FIG. 2C) shows generally applicable embodiments of a series resonant network 201a coupled to the control input, e.g. a gate terminal, of a switch transistor or a switching network of a class E or DE
- 15 resonant power converter such as the class E and DE resonant power converters depicted on FIGS. 1A)-1B), FIG. 2A), FIGS. 3A)-3B), FIG. 4 and FIG. 8. The series resonant network 201 comprises a plurality of series resonant circuits of which one or more may be included in particular design of the class E or DE resonant power converter.

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If a transistor switch like a MOSFET is driven by a sine wave the gate signal will be right above the threshold voltage of the MOSFET in a beginning and end of a conduction period of the MOSFET. This causes the on resistance to be very high in these periods as the MOSFET is only fully turned on when the gate signal is larger

- 25 than around twice the threshold voltage. In many resonant power converters these time periods are also where the largest currents are running through the MOSFET. Hence a lot of power is dissipated in these time periods. In order to improve the turn on speed of the MOSFET, higher order harmonics can be added to the fundamental sine wave leading to a more trapezoidal gate signal as mentioned above. This can
- 30 be achieved by adding one or more series resonant circuits, each preferably comprising an LC circuit, between the control input, i.e. the gate of the present MOSFET switch, and a drain or source of the MOSFET as illustrated on FIG. 2C). Here the capacitor, C<sub>GDext</sub>, is optional and may be used to increase overall gain of the gate signal as shown in FIG. 2D). In the same way capacitor, C<sub>GSext</sub>, can optionally be

used to lower the gain. The first and second LC based series resonant circuits  $C_{4HI}$  and  $L_{4HI}$  and  $C_{2HI}$  and  $L_{2HI}$ , respectively, are both connected to drain of MOSSFET switch  $S_1$  and will cause higher harmonics to be in phase with the switch output voltage at the switch output,  $V_{DS}$ . The third and fourth LC based series resonant

- 5 circuits  $C_{4HO}$  and  $L_{4HO}$  and  $C_{2HO}$  and  $L_{2HO}$ , respectively, connected to the ground will cause the harmonics to be out of phase with  $V_{DS}$  as illustrated in FIG. 2D). The magnitude response curve 250 of graph 245 of FIG. 2D) illustrates how a LC circuit with a resonance at the second harmonic of the switching frequency of the power converter causes a peak in the gain at the third harmonic and that it is in phase with
- 10 the switch output V<sub>DS</sub>. It can be shown that a 3<sup>rd</sup> harmonic in phase will be desirable for a duty cycle of 25%, but for a duty cycle of 50% it would be more desirable to have the signal out of phase as this would increase the signal right after and turn on of the MOSFET and just before turn off of the MOSFET. This feature can be achieved by setting a LC series resonant circuit with resonant frequency at the 2<sup>nd</sup>
- 15 harmonic to ground instead as indicated by the third and fourth series resonant circuits  $C_{4HO}$  and  $L_{4HO}$  and  $C_{2HO}$  and  $L_{2HO}$ , respectively, of FIG. 2C). By this connection, the magnitude response curve 252 of FIG. 2D) is achieved. Here a zero is seen at the 2<sup>nd</sup> harmonic of the switching frequency and again a peak at the 3<sup>rd</sup> harmonic, but this time with a phase shift of nearly 180 degrees (please refer to curve 252 of
- 20 the phase graph 246). The skilled person will understand that the number of harmonics to include in a given power converter design will depend on several parameters as price, complexity, efficiency etc. Adding higher order harmonics will in general increase the performance of the power converter, but it is important to consider which harmonics to include and the magnitude of those harmonics compared to the
- fundamental. Graphs 247 and 248 of FIG. 2E) show the fundamental and the 3<sup>rd</sup> and 5<sup>th</sup> harmonics of the switching frequency are in and out of phase with the switch output signal for the duty cycle D set to 25 % and 50 %. Note that the symbol \* indicates that the depicted signal is in phase with the switch output signal V<sub>DS</sub>. By comparing, the gate drive signal waveforms with the indicated ideal (rectangular) wave-
- 30 form shape of the same, it is clear that it is desirable to place the fundamental out of phase with the switch output signal, but for the 3<sup>rd</sup> and 5<sup>th</sup> harmonic it depends on the duty cycle and the current waveform. Exemplary gate drive waveforms that can be achieved by adding harmonics by the above-described series resonant networks are shown in the graphs 247 and 248 of FIG. 2E).

FIG. 2B) is an electrical circuit diagram of a class E resonant power converter 200b comprising a series resonant circuit in accordance with a fourth embodiment of the invention. The skilled person will appreciate that the above discussed features, func-

- 5 tions and components of the third embodiment of the class E resonant power converter 200 may apply to the present embodiment as well. Likewise, corresponding components in the third and fourth embodiments of the present class E resonant power converter have been provided with corresponding reference numerals to ease comparison. The main difference between the third and fourth embodiments is that
- 10 the previously discussed a series resonant circuit, comprising the cascade of capacitor  $C_{MR}$  and inductor  $L_{MR}$ , connected between the gate node or terminal  $V_{GS}$  of switch transistor  $S_1$  and ground have been replaced by another type of resonant circuit comprising the parallelly coupled capacitor  $C_{MR}$  and inductor  $L_{MR}$ . The parallelly coupled capacitor  $C_{MR}$  and inductor  $L_{MR}$  are connected between the adjustable
- 15 bias voltage  $V_{Bias}$  and the gate inductor  $L_g$ . This connection with the parallelly coupled capacitor  $C_{MR}$  and inductor  $L_{MR}$  provides the same advantages as the series resonant circuit employed in the third embodiment, but with much smaller inductances of inductors  $L_g$  and  $L_{MR}$  leading to a significant reduction in costs and size.
- FIG. 3A) is a simplified electrical circuit diagram of a class DE resonant power converter or inverter 300 in accordance with a fifth embodiment of the invention. The present resonant power inverter 300 is based on a switching network which comprises a half-bridge semiconductor topology. The present DE resonant power converter 300 provides several important advantages. One of the biggest challenges
- 25 when designing resonant power converters is a huge voltage stress imposed on the switch element in the single switch power converter topology described above in connection with the first, second, third and fourth embodiments of the invention. This voltage stress may reach 3-4 times the level of the DC input voltage. Using a half bridge switch topology instead limits a peak voltage across the each of the semi-
- 30 conductor switches S<sub>1</sub> and S<sub>2</sub> to a level of the input voltage. However, this requires a fast and efficient high side driver which can pose a significant advantage if an operating frequency or switching frequency above approximately 5 MHz is desired. The present generation of the first adjustable bias voltage solves this problem as it can also be used as a high side drive (V<sub>Bias1</sub>) at several tens of megahertz. The half-

bridge comprises a cascade of the first semiconductor switch  $S_1$  coupled between a switch output terminal 311 and ground and a second semiconductor switch  $S_2$  coupled between the switch output terminal 311 and a DC input voltage rail supplied through power input terminal 302 from an external DC voltage source or generator

- 5 304. A coupling or mid-point node interconnecting the first and second semiconductor switches  $S_1$  and  $S_2$  form the switch output terminal 311. This switch output terminal 311 is the drain terminal of the first semiconductor switch S1. This switch output terminal or node 311 is coupled to a first side of a series resonant network comprising resonant capacitor  $C_R$  and resonant inductor  $L_R$ . A drain node of the transistor
- 10 switch S<sub>2</sub> coupled to the DC input voltage, comprises the switch input terminal of the present half-bridge switch. Each of semiconductor switches S<sub>1</sub> and S<sub>2</sub> may comprise a NMOS power transistor as illustrated by the switch symbol. Intrinsic drain-gate, gate-source and drain-source capacitances of the first NMOS transistor switch S<sub>1</sub> are depicted as C<sub>GD2</sub>, C<sub>GS2</sub> and C<sub>DS2</sub> and likewise as C<sub>GD1</sub>, C<sub>GS1</sub> and C<sub>DS1</sub> for NMOS
- 15 transistor switch S<sub>2</sub>.

The resonant capacitor  $C_R$ , intrinsic drain-source capacitances of switches  $S_1$  and  $S_2$ ,  $C_{DS1}$  and  $C_{DS2}$ , respectively, and the resonant inductor  $L_R$  in conjunction form a resonant network of the power converter 300. A second and opposite side of the

- 20 series resonant network is coupled to an output terminal 314 or node of the power converter 300. A converter load is schematically illustrated by a load resistor R<sub>LOAD</sub> connected to the converter at the output terminal 314 and may generally exhibit inductive, capacitive or resistive impedance. The class DE resonant power inverter 300 furthermore includes a self-oscillating feedback loop arranged around the tran-
- 25 sistor switch S<sub>1</sub> such that an oscillation frequency of the loop sets the switching or operational frequency of the power converter in a manner similar to the one discussed in detail above in connection with the first embodiment of the invention. The self-oscillating feedback loop comprises an intrinsic gate-drain capacitance C<sub>GD2</sub> of the transistor switch S<sub>1</sub> and a first gate inductor L<sub>G2</sub> which preferably comprises a
- 30 substantially fixed inductance as discussed above. The gate inductor L<sub>G2</sub> is coupled in-between a variable bias voltage V<sub>Bias2</sub> and the gate terminal V<sub>GS2</sub> of the transistor switch S<sub>1</sub>. The variable bias voltage V<sub>Bias2</sub> may be generated in numerous ways by a suitably configured bias voltage generator or source for example as explained in further detail below in connection with FIG. 4. In addition to the circuitry forming the

self-oscillating feedback loop arranged around transistor switch S<sub>1</sub>, the current power inverter 300 comprises a second or high side adjustable bias voltage  $V_{Bias1}$  that is coupled to the gate terminal of the second semiconductor switch S<sub>2</sub> through a cascade of a second substantially fixed inductance L<sub>H</sub> and a third substantially fixed

- 5 inductance  $L_{G1}$ . The inductances of the gate inductors  $L_{G2}$  and  $L_{G1}$  may be substantially identical. A feedback capacitor  $C_{G1}$  is coupled between the switch output node 311 and an intermediate node between the second and third substantially fixed inductances  $L_H$  and  $L_{G1}$ . The feedback capacitor  $C_{G1}$  serves as a bootstrap device which raises the voltage level supplied to the upper transistor switch  $S_2$  and facili-
- 10 tates use of a N-channel MOSFET transistor as switch device. The inductor L<sub>H</sub> serves as a high impedance signal path at the oscillation frequency allowing passage of a relatively slowly varying bias voltage component generated by the second adjustable bias voltage V<sub>Bias1</sub>, but blocking passage of a relatively high frequency voltage component supplied through the bootstrap capacitor or feedback capacitor
- 15 C<sub>G1</sub>. Consequently, combining the bias voltage components from L<sub>H</sub> and C<sub>G1</sub>, the gate control voltage at the gate terminal of the second switch S<sub>2</sub> is level shifted. In this manner, the gate control voltage is referred to the switch output node 311 instead of ground. The self-oscillation loop ensures that each of the semiconductor switches S<sub>1</sub> and S<sub>2</sub> is alternately switched between conducting and non-conducting
- 20 states in opposite phase in a non-overlapping manner. Thereby, the switch output node 311 becomes alternatingly clamped to the DC input voltage  $V_{IN}$  and ground through the semiconductor switches  $S_1$  and  $S_2$  at a frequency defined by the oscillation frequency of the self-oscillating loop.
- 25 The duty cycle of the switch output voltage waveforms and hence the converter output voltage at  $V_{out}$  can once again be controlled by synchronously controlling the respective bias voltages supplied by the first and second adjustable bias voltages  $V_{Bias2}$  and  $V_{Bias1}$ .
- 30 FIG. 3B) is an electrical circuit diagram of a class DE resonant power converter 300b comprising a pair of magnetically coupled inductors L<sub>G1</sub> and L<sub>G2</sub> in accordance with a sixth embodiment of the invention. The skilled person will appreciate that the above discussed features, functions and components of the first embodiment of the class DE resonant power converter 300 may apply to the present embodiment as

well. Likewise, corresponding components in the fifth and sixth embodiments of the present resonant power converters have been provided with corresponding reference numerals to ease comparison. The main difference between the fifth and sixth embodiments is that the previously discussed separate and substantially uncoupled

- 5 gate inductors L<sub>G1</sub> and L<sub>G2</sub> have been replaced by the pair of magnetically coupled inductors L<sub>G1</sub> and L<sub>G2</sub> where their respective functions in the present class E resonant power converter 300b are similar to those of the first embodiment. The skilled person will appreciate that magnetic coupling between the gate inductors L<sub>G1</sub> and L<sub>G2</sub> may be achieved in numerous ways for example by a closely spaced arrange-
- 10 ment of the inductors e.g. coaxially arranged. The magnetic coupling provides a number of advantages over the above-described first embodiment of the class DE resonant power converter 300 such as improved phase response between the respective gate signals at the gate terminals, or control inputs, of the inductors L<sub>G1</sub> and L<sub>G2</sub> and larger gain. The magnetic coupling ensures that the respective inductor cur-
- 15 rents in the inductors L<sub>G1</sub> and L<sub>G2</sub> are out of phase. Hence, forcing a phase shift that is substantially 180 degrees between the gate signals of the inductors L<sub>G1</sub> and L<sub>G2</sub>.

The magnetic coupling between the inductors may also be accomplished by a transformer structure as schematically indicated on FIG. 3B) wherein the inductors  $L_{G1}$ 

20 and L<sub>G2</sub> are wound around a common magnetically permeable core. The latter embodiment has the advantage that a larger magnetic coupling between the inductors L<sub>G1</sub> and L<sub>G2</sub> can be achieved and the relative phase shift of substantially 180 degrees between the respective gate signals or voltages of the MOSFET switches S<sub>1</sub> and S<sub>2</sub> is enforced even stronger.

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FIG. 4 is a schematic electrical circuit diagram of a DC-DC or switched mode power converter/supply (SMPS) 400 which is based on the class E resonant power converter or inverter 100 disclosed above in a first embodiment of the invention. The DC-DC power converter 400 comprises, in addition to the circuitry of the class E resonant power converter 100, a voltage control loop controlling the level of a DC output voltage  $V_{OUT}$  of the DC-DC converter and a rectifier 413 schematically illus-

series inductor coupled between the illustrated diode and the output voltage terminal  $V_{OUT}$ . The skilled person will appreciate that the illustrated diode(s) based rectifier

trated by a storage capacitor and a diode. The rectifier 413 preferably includes a

413 may be replaced by a synchronous rectifier based on one or more actively controlled semiconductor switches rather than diodes as described in additional detail below with reference to FIG. 8. The voltage control loop regulates respective resistances of a pair of pull-up and pull-down MOSFET resistors M<sub>1</sub> and M<sub>2</sub> forming

- 5 part of bias voltage source or generator supplying the adjustable bias voltage V<sub>Bias</sub>. The adjustable bias voltage V<sub>Bias</sub> is applied to the gate terminal of transistor switch S<sub>1</sub> through the gate inductor L<sub>G</sub> as explained in connection with FIG. 1A) above. The voltage control loop comprises a comparator or error amplifier 414 which has a first input coupled to a DC or AC reference voltage V<sub>BEF</sub> and a second input coupled to
- 10 the DC output voltage V<sub>OUT</sub> of the converter. A resulting error signal V<sub>ERR</sub> reflecting whether the output voltage is lower or higher than the reference voltage is fed to an optional level converter 414. The level converter 414 is configured to provide appropriate gate control signals V<sub>C1</sub> and V<sub>C2</sub> for the pair of pull-up and pull-down MOSFET resistors M<sub>1</sub> and M<sub>2</sub> to either increase or decrease the adjustable bias voltage V<sub>Bias</sub>.
- 15 The bias voltage source or generator comprises the MOSFET resistors M<sub>1</sub> and M<sub>2</sub> coupled between the DC input voltage and ground. Hence, the adjustable bias voltage V<sub>Bias</sub> can either be pulled towards the DC input voltage or ground depending on the adjustable on-resistances of the MOSFET resistors M<sub>1</sub> and M<sub>2</sub>. The skilled person will appreciate that the voltage control loop can be configured in numerous ways
- 20 to provide appropriate control signals to the MOSFET resistors M<sub>1</sub> and M<sub>2</sub> for example by proportional voltage control or by purely binary voltage control, i.e. up/down.

FIG. 6 is a circuit simulation model of a second DC-DC power converter based on the first embodiment of the class E resonant power converter. The DC-DC converter
comprises a rectifier coupled between an output of the series resonant circuit, including C1 and L4, and a load resistance R6 coupled to an output voltage of the converter. The rectifier comprises components C3, D, L2 and C5. Inductor and capacitor component values of the second DC-DC power converter are listed on the figure in Henry and Farad, respectively. Accordingly, the inductance of the gate in-

30 ductor Lg is set to a substantially fixed value of 68 nH. The semiconductor switch is modelled by an ideal switch ISW with the listed parameters, i.e. an on-state resistance of 1.0  $\Omega$  off-state resistance of 1M $\Omega$  and threshold voltage of 4.5 V.

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FIG. 7 shows a series of graphs 600, 610, 620, 630 and 640 illustrating various simulated voltage waveforms of the simulation model of the second DC-DC power converter for four different fixed DC bias voltage levels of the adjustable bias voltage  $V_{bias}$ .  $V_{bias}$  is stepped through fixed DC voltage levels of -7.0, -2.0, 3.0 and 8.0 volt as illustrated by waveforms 607, 605, 603, 601, respectively, of graph 600 showing the DC bias voltage level. The DC input voltage V2 (Vin) is kept constant at 50 volts for all simulations.

- The scale on the y-axis of all graphs indicates voltage in volts while the x-axis scale indicates time in steps of 0.01  $\mu$ s such that the entire x-axis spans over about 0.05  $\mu$ s.
- Graph 610 illustrates the corresponding oscillating control input voltage waveforms
   617, 615, 613, 611 at the indicated gate node (refer to FIG. 6) for the four different
   levels of the DC bias voltage. The higher average level of the oscillating control input voltage waveforms for the highest DC bias voltage of 8.0 V is evident. Graph
   620 illustrates the corresponding switch output voltage waveforms 627, 625, 623,
   621 at the switch output node i.e. at the indicated drain node (refer to FIG. 6). The
   longer conducting states or on-states of the switch ISW for the highest DC bias voltage of 8.0 V is evident leading to a lower oscillation frequency or switching frequency of the converter.
- Graph 640 illustrates the corresponding load power waveforms 627, 625, 623, 621
  for the power delivered the load resistor R6 through the converter output. The gradually increasing load power from about 1.5 W at the lowest DC bias voltage of -7.0 V to about 3.5 W at the highest DC bias voltage of 8.0 V is evident. Hence, converter output power and therefore converter output voltage can be controlled by adjusting the voltage supplied by the adjustable bias voltage V<sub>bias</sub>.
- 30 FIG. 8 is a schematic electrical circuit diagram of a DC-DC or switched mode power converter/supply (SMPS) 800 based on the class E resonant power converter or inverter 100 according to the first embodiment of the invention discussed above. The DC-DC power converter 800 comprises, in addition to the circuitry of the class E resonant power converter 100, a synchronous rectifier building around transistor

switch  $S_{R1}$  and comprising additional passive components  $L_{G2}$  and  $L_{OUT}$ . The skilled person will understand that the DC-DC power converter 800 may comprise an output capacitor coupled from  $V_{OUT}$  to the negative supply rail (e.g. ground) and a voltage control loop similar to the one discussed above in connection with FIG. 4 in the

- 5 fourth embodiment of the invention. The voltage control loop being configured to control the output voltage at  $V_{OUT}$  of the power converter 800 as defined by a DC or AC reference voltage. The transistor switch element  $S_{R1}$  and inductors  $L_{G2}$  and  $L_{OUT}$ provide a synchronous rectifier in the DC-DC power converter 800 and replaces the diode based asynchronous rectifier circuit 413 discussed above. Since the control
- 10 input, e.g. the gate drive signal, of the switching network of the present class E and DE resonant power converters does not need a traditional PWM or PDM type of control signal (but only the two adjustable bias voltage V<sub>Bias1</sub> and V<sub>Bias2</sub>), the resonant power converters in accordance with the present embodiments are generally very well suited for synchronous rectification as illustrated on FIG. 8 for this particu-
- 15 lar embodiment. The traditional PWM or PDM type of control signals are not required because is not necessary to control a phase between the respective control input signals of the first transistor switch S<sub>1</sub> and the rectification transistor switch S<sub>R1</sub>. The rectification transistor switch S<sub>R1</sub> may for example be coupled to a suitable fixed rectifier DC bias voltage V<sub>Bias2</sub> applied to the inductor L<sub>G2</sub> coupled to the gate
- (i.e. control input) of S<sub>R1</sub>. For rectification purposes, the gate terminal of S<sub>R1</sub> is driven by an oscillation output voltage, i.e. the drain voltage V<sub>DS</sub>, of the first semiconductor switch S<sub>1</sub> to automatically maintain synchronous operation between S<sub>1</sub> and SR1. This absence of the traditional PWM or PDM type of control signals on the respective gate terminals of the first transistor switch S<sub>1</sub> and rectification transistor switch
- S<sub>R1</sub> is a significant advantage leading to simplified power converter design and smaller component count. In isolated power converter applications, the present diode based asynchronous rectifier circuit 413 possess an additional advantage because it eliminates the need for transmitting or communicating the traditional PWM or PDM type control signal or signals across a voltage isolation barrier of the reso-
- 30 nant power converter. This type of voltage isolation barrier will typically require expensive and space consuming components like optocouplers or fast transformers in traditional power converter topologies. As illustrated by FIG. 8, the present DC-DC power converter with synchronous rectification may be completely symmetrical in terms of circuit topology across a series resonant network comprising resonant ca-

pacitor  $C_R$  and resonant inductor  $L_R$  allowing for bidirectional power flow between the DC input power source  $V_{IN}$  804 and the output voltage at  $V_{OUT}$ . The skilled person will appreciate that the input transistor switch  $S_1$  and rectifier transistor switch  $S_{R1}$  may be substantially identical or different components and the same applies to the

5 fixed inductance inductors L<sub>G2</sub> and L<sub>G1</sub> depending on factors such as the voltage conversion ratio of the resonant power converter.

The skilled person will appreciate that the above-described synchronous rectifier may be added to each of the above discussed class E and DE resonant power con-

10 verter embodiments depicted above on FIG. 1B), FIGS. 2A)-2B) and FIGS. 3A)-3B).

## <u>CLAIMS</u>

1. A resonant power converter comprising:

an input terminal for receipt of an input voltage,

- 5 a switching network comprising one or more semiconductor switches controlled by respective control inputs, the switching network comprising a switch input operatively coupled to the input
- terminal for receipt of the input voltage and a switch output operatively coupled to an input of a resonant network of the resonant power converter,
- the resonant network comprising a predetermined resonance frequency  $(f_R)$  and an output operatively coupled to a converter output terminal,

a self-oscillating feedback loop coupled from the switch output to a control input of the switching network to set a switching frequency of the power converter;

- the self-oscillating feedback loop comprising:
  - a first intrinsic switch capacitance coupled between the switch output and the control input of the switching network,

a first bias voltage source configured to generate a first adjustable bias voltage, a first inductor with substantially fixed inductance coupled in-between the first bias voltage source and the control input of the switching network,

a voltage regulation loop configured to control an output voltage of the power converter by controlling the first adjustable bias voltage applied to the first inductor.

2. A resonant power converter according to claim 1, comprising:

an input inductor coupled between the input terminal and the switch input,

- 25 the switching network comprising a first semiconductor switch with a control terminal coupled to the control input of the switching network and an output terminal coupled to the switch input and to the switch output.
- 3. A resonant power converter according to claim 2, wherein the input inductor and
   the first inductor are magnetically coupled with a predetermined magnetic coupling
   coefficient, preferably a magnetic coupling coefficient larger than 0.1 or even more
   preferably larger than 0.4.

4. A resonant power converter according to claim 1, wherein the switching network comprises:

a first semiconductor switch coupled between the switch output and a voltage supply rail of the resonant power converter and having a control terminal coupled to the

control input of the switching network,
 a second semiconductor switch coupled between the switch output and the input terminal; and

wherein a control terminal of the second semiconductor switch is coupled to a second bias voltage source through a cascade of a second inductor with substantially

10 fixed inductance and a third inductor with substantially fixed inductance, and wherein a feedback capacitor is coupled between the switch output and an intermediate node between the second and third inductors.

5. A resonant power converter according to claim 4, wherein the first inductor and

- 15 the third inductor are magnetically coupled with a predetermined magnetic coupling coefficient, preferably a magnetic coupling coefficient larger than 0.1 or even more preferably larger than 0.4.
- 6. A resonant power converter according to claim 3 or 5, wherein the input inductorand the first inductor are wound around a common magnetically permeable member of core; or

the first inductor and the third inductor are wound around a common magnetically permeable member or core.

- 7. A resonant power converter according to any of the preceding claims, wherein the first bias voltage source comprises:
   a capacitor coupled from the first adjustable bias voltage and a fixed electric potential of the resonant power converter such as ground,
   a first adjustable resistor coupled between the first adjustable bias voltage and a first
   DC reference voltage.
- a second adjustable resistor coupled between the first adjustable bias voltage and a second DC reference voltage.

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8. A resonant power converter according to any of the preceding claims, wherein the voltage regulation loop comprises:

a reference voltage generator supplying a reference DC or AC voltage to a first input of a comparator,

a second input of the comparator being coupled to the converter output voltage, an output of the of the comparator operatively coupled to a control input of the first bias voltage source.

9. A resonant power converter according to any of the preceding claims, wherein the
10 first inductor has an inductance between 1 nH and 10 μH such as between 1 nH and
50 nH.

10. A resonant power converter according to any of the preceding claims, wherein the substantially fixed inductance of the first inductor is set such that a peak voltage at the control input of the switching network exceeds a threshold voltage of at a

15 at the control input of the switching network exceeds a threshold voltage of at a semiconductor switch of the switching network.

11. A resonant power converter according to claim 10, wherein the substantially fixed inductance of the first inductor is selected such that a peak-peak voltage swing
at the control input of the switching network is approximately equal to a numerical value of the threshold voltage of the at least one of the semiconductor switches of the switching network.

12. A resonant power converter according to any of the preceding claims, wherein
the self-oscillating feedback loop further comprises:
a series resonant circuit coupled in-between the control input of the switching network and a fixed electric potential of the power converter.

13. A resonant power converter according to claim 12, wherein the self-oscillating feedback loop further comprises:

a first series resonant circuit coupled in-between the control input of the first semiconductor switch and fixed electric potential of the converter such as a positive or negative DC supply voltage or a ground voltage,

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a second series resonant circuit coupled in-between the control input of the first semiconductor switch and the switch output.

14. A resonant power converter according to any of the claims 1-11, wherein the self-oscillating feedback loop further comprises:

a parallel resonant circuit coupled in series with the first inductor in-between the first adjustable bias voltage and the first inductor.

15. A resonant power converter according to any of the preceding claims, furthercomprising:

a rectifier coupled between the output of the resonant network and the converter output terminal to provide a rectified DC output voltage.

16. A resonant power converter according to claim 15, wherein the rectifier compris-es a synchronous rectifier.

17. A resonant power converter according to claim 16, wherein the synchronous rectifier comprises:

a rectification semiconductor switch configured to rectify an output voltage of the resonant network in accordance with a rectifier control input of the rectification semi-

conductor switch,

a first rectification inductor with a substantially fixed inductance coupled in-between a fixed or adjustable rectifier bias voltage and the rectifier control input.

- 25 18. A resonant power converter according to claim 17, wherein the fixed or adjustable rectifier bias voltage is coupled to a fixed DC bias voltage source or to the rectified DC output voltage through a resistive or capacitive voltage divider.
- 19. A resonant power converter according to any of claims 2-18, wherein one of the
  first and second semiconductor switches comprises a MOSFET or IGBT such as a
  Gallium Nitride (GaN) or Silicon Carbide (SiC) MOSFET.

20. A resonant power converter assembly comprising: a resonant power converter according to any of the preceding claims, a carrier substrate having at least the switching network and the resonant circuit integrated thereon,

an electrical trace pattern of the carrier substrate forming the first inductor.

5 21. A resonant power converter assembly according to claim 16, wherein the carrier substrate comprises a semiconductor die.







FIGS. 1A, B







FIGS. 2A, B















FIGS. 2D, E







FIGS. 3A, B

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FIG. 5

## FIG. 6

.param Vin=50 .param Lin 1u .param Cds 26p .param Cds 10p .param Cgs 80p .param Rg 1.5 .param Rg 1.5 .param Ct 1n .param Lt 250n .param Lg 68n .param Lr 30n .param Cr 80p

.tran 0 50u .step param Vbias LIST -7 -2 3 8 .model ISW SW(Ron=1 Roff=1Meg Vt=4.5 Vh=-0.5)

.model D D



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FIG. 7

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FIG. 8
D

# Investigation, development and verification of printed circuit board embedded air-core solenoid transformers

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## Investigation, development and verification of printed circuit board embedded air-core solenoid transformers

Jakob D. Mønster, Mickey P. Madsen, Jeppe A. Pedersen and Arnold Knott

DTU Elektro Technical University of Denmark Denmark, Kongens Lyngby 2800 Email: {jdomo,mpma,jarpe,akn}@elektro.dtu.dk

Abstract—A new printed circuit board embedded air-core transformer/coupled inductor is proposed and presented. The transformer is intended for use in power converter applications operating at very high frequency between 30 MHz to 300 MHz. The transformer is based on two or more solenoid structures in different configurations. The different configurations are compared for usefulness as a transformer solution, and an analytical model of the inductive parameters for the most suitable configuration is derived for design purpose. The analytical model is verified by comparing calculations and measurements of prototypes. The analytical model shows good agreement with the measured results. The model can predict the inductive parameters of the transformer with a deviation range of approximately 3% to 22%. Lastly a prototype is used in a VHF converter to achieve a rise of 2.2% points in efficiency.

#### I. INTRODUCTION

The increasing demand from consumers and industry for high power density converters is leading to continuous work on resonant switch-mode power supplies (SMPS) switching in the very high frequency (VHF) range between 30 MHz to 300 MHz [1], with designs achieving efficiencies up to approximately 90% [2], [3]. VHF power converters reduces the requirements for inductance and capacitance for a desired output power as the need for energy storing per switching cycle is inversely coupled to the frequency [4]. Galvanic isolation in traditional high-frequency SMPS is usually implemented with an isolation transformer, that utilize a magnetic core. This approach is not suitable for VHF-SMPS as the core-losses will be significant at VHF [5]. Air-core magnetics with the lack of magnetic core removes the core-losses and the possibility of saturation, making them a suitable solution for VHF operation with the converters low inductance requirements. Air-core magnetic design can be implemented into a printed circuit board (PCB) [6]–[14], and can be implemented with different structures. This paper propose an implementation and analytic inductance model of a PCB embedded rectangular solenoid air-core transformer. First the concept of PCB embedded solenoid transformers is introduced, followed

by an evaluation of different winding configurations. An analytic model of the inductive parameters is developed for the most promising configuration and finally the model is verified by measurement of implemented prototypes, together with the use of a coupled inductor in a VHF resonant converter, showing improved efficiency.

#### II. TRANSFORMERS

Transformers in general exist in a vast number of designs, most focused on versions with a core to guide the flux to achieve a good coupling between the primary and secondary side. Air-core transformers can also be made in many designs, but are for practical purposes limited to structures that in it self will guide the flux through a common winding area, since there is no core to help guiding the flux. Spiral and toroid PCB embedded air-core transformer structures have previously been proposed [10], [13]. In this paper the solenoid PCB embedded air-core transformer is proposed.

#### A. Printed circuit board embedded air-core transformers

The idea behind PCB embedded air-core transformers is to utilize the easy, cheap and consistent production method of PCBs with air-core magnetics. In general aircore magnetics are considered a viable solution for magnetic components in converters operating in the VHF range since they do not have any core losses, which in a normal core based transformer would be very high [5]. The disadvantages are the low inductance, coupling and typically a larger external magnetic field, due to the missing magnetic material [8]. The 3D transformer structures are created in the PCB by using areas of copper in a two or more layer PCB as horizontal wires and by using vias as vertical wires.

1) Solenoid transformers: The PCB embedded rectangular air-core solenoid transformer can be designed in different configurations, where two main configurations are investigated here. The solenoid transformer is either built up by having a solenoid winding structure nested inside a slightly larger solenoid structure, embedded in a minimum four layer PCB, giving the transformer a rectangular cross section as seen in Figure 1a, or built up by having two or more windings in an interleaved pattern on the same layers. The interleaved configurations ranges from the bifilar configuration to the end-to-end configuration as seen in Figures 1b to 1d. The interleaved configurations can be implemented in a two layer PCB.



(c) Sections (4:4)



(d) End-to-end

Fig. 1. Different winding configurations of rectangular PCB embedded air-core solenoid transformers

#### III. Comparison

In this section different configurations similar to each of the configurations shown in Figure 1 is evaluated for their inductive parameters and coupling. A good transformer will have a high coupling to efficiently transfer energy from the primary side to the secondary.

#### A. Transformer parameters

The inductive model of a transformer can be defined as a two-port passive device and is described by the inductance matrix [15] in (1). The inductance matrix consists of the self-inductance for each winding  $L_{pp}$  and  $L_{ss}$ .  $L_{ps}$  and  $L_{sp}$ are the mutual inductance, and is determined by the flux that flows through the mutual area of the transformer. Note that  $L_{ps}$  and  $L_{sp}$  are equal since the transformer is a passive device.

$$\begin{bmatrix} v_p(t) \\ v_s(t) \end{bmatrix} = \begin{bmatrix} L_{pp} & L_{ps} \\ L_{sp} & L_{ss} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_p(t) \\ i_s(t) \end{bmatrix}$$
(1)

The coupling ratio is defined as (2), and is a ratio of how much flux couples between the primary and secondary windings. In regular transformers wound around a core, the coupling is in the range of k = 0.99 for the best [15].

$$k = \frac{L_{ps}}{\sqrt{L_{pp}L_{ss}}} \tag{2}$$

The measurement of the inductance matrix defined in (1) was carried out by measuring the S-parameters [13] on a Agilent 4396B, set up as a vector network analyzer. The S-parameter measurements are converted to Z-parameters [16] and then inductances by (3).

$$L = \frac{\Im(Z)}{\omega} \tag{3}$$

#### B. Evaluation of configurations

Prototypes in each of the configurations similar to the ones shown in Figure 1 were produced and measured. The prototypes are shown in Figure 2. The resulting inductances, in Table I, used for comparison are mean values from 1 MHz to 10 MHz, to remove any small measurement noise. The impedances measurements of the prototype transformers, are shown in Figure 3.

#### TABLE I

#### INDUCTANCES OF DIFFERENT CONFIGURATIONS OF PCB EMBEDDED SOLENOID TRANSFORMERS

Variable	Lpp	$L_{ps}$	$L_{ss}$	k	
Measured [nH]	67.40	17.62	9.58	0.70	
(a) Nested configuration					
Variable	$L_{pp}$	$L_{ps}$	$L_{ss}$	k	
Measured [nH]	42.25	18.95	41.87	0.45	
(b) Bifilar					
Variable	$L_{pp}$	Lps	Lss	k	
Variable Measured [nH]	$\frac{L_{pp}}{40.95}$	$\frac{L_{ps}}{10.52}$	$L_{ss}$ 38.81	k 0.26	
Variable Measured [nH] (c) Interle	$L_{pp}$ 40.95 eaved in	$\frac{L_{ps}}{10.52}$ sections	$\frac{L_{ss}}{38.81}$ (2:2)	$\frac{k}{0.26}$	
Variable Measured [nH] (c) Interle Variable	$L_{pp}$ $40.95$ eaved in $L_{pp}$	$\frac{L_{ps}}{10.52}$ sections $L_{ps}$	$ \frac{L_{ss}}{38.81} $ (2:2) $ L_{ss}$	k 0.26 k	
Variable Measured [nH] (c) Interle Variable Measured [nH]	$ \begin{array}{c} L_{pp} \\ 40.95 \\ \text{eaved in} \\ \hline L_{pp} \\ 41.00 \end{array} $	$\frac{L_{ps}}{10.52}$ sections $\frac{L_{ps}}{3.22}$	$L_{ss}$ 38.81 (2:2) $L_{ss}$ 39.45	k 0.26 k 0.08	

The interleaved configurations shows coupling in the range from k = 0.08 to k = 0.45. The more intertwined the primary and secondary side is, the higher the coupling. The coupling is in general limited by the clearance between the traces / sections on the PCB, leaving the end-to-end configuration with very bad coupling for a transformer. The sections configuration shows better properties with the bifilar configuration as the optimum of the interleaved with a coupling of k = 0.45. Compared to the nested configuration, the interleaved configurations are inferior, as the coupling is k = 0.7 for the nested configuration. This coupling coefficient is suitable for a VHF converter as the leakage inductance can be used in the design of the converter. As the nested configuration is the most promising, the inductance formulas for inductance matrix will be derived and evaluated.



Fig. 2. Examples of PCB embedded air-core solenoid transformers with different winding configurations. Scale 1:1



Fig. 3. Impedances of different winding configurations of the PCB embedded air-core solenoid transformer

#### IV. ANALYTIC MODEL

In this section the nested configuration is analytically analyzed. The cylindrical solenoid transformer is a classic textbook example in the magnetic literature, with relatively simple equations [17]. The general equations for a solenoid inductor with a rectangular cross section was derived in [18], the short version given in [19]. The formula is valid as long as the width is greater than the height of the inductor, which, for all practical purposes, is the case for PCB embedded solenoids. There are no equations in the literature for solenoid transformers with rectangular cross sections, so the model will be deduced here. The following assumptions are made to simplify the model

#### expression:

- The lengths of each solenoid structure are equal
- The flux is evenly distributed inside the solenoid.

The assumption that the flux is evenly distributed inside the the solenoid is an approximation, and will be a source of error. The approximation is made on basis of 3D finite element simulations made in COMSOL of a single inductor. An example of the strength of the magnetic field is shown in Figure 4. The flux is slightly concentrated where there is a wire or a via, but is on average close to an evenly distribution.

1) Inductance formula: For the self-inductance  $L_{pp}$  and  $L_{ss}$  the equation is given in (5) [19], with the respective



Fig. 4. Flux distribution in a PCB solenoid inductor

heights h, widths w and numbers of turns N for the primary and secondary side respectively. The dimensions can be seen in Figure 5. For reference the inner structure of windings is denoted the primary side and the outer the secondary. g is given by (4).

$$g^2 = w^2 + h^2 \tag{4}$$

The mutual inductance,  $L_{ps}$  or  $L_{ps}$ , is determined by the shared flux, which will pass through the windings mutual area inside the transformer. The mutual inductance must therefore be the same inductance formula (5) as the inner solenoid with respect to the width and height but with the number of turns as  $N^2 = N_p N_s$ .

$$\begin{split} L &= 8 \cdot 10^{-9} N^2 \frac{hw}{l} \\ &\left[ \frac{1}{2} \frac{l}{h} \sinh^{-1} \left( \frac{w}{l} \right) + \frac{1}{2} \frac{l}{w} \sinh^{-1} \left( \frac{h}{l} \right) \\ &- \frac{1}{2} \left( 1 - \frac{h^2}{l^2} \right) \frac{l}{h} \sinh^{-1} \left( \frac{w}{l\sqrt{1 + \frac{h^2}{l^2}}} \right) \\ &- \frac{1}{2} \left( 1 - \frac{w^2}{l^2} \right) \frac{l}{w} \sinh^{-1} \left( \frac{h}{l\sqrt{1 + \frac{w^2}{l^2}}} \right) \\ &- \frac{1}{2} \frac{h}{l} \sinh \left( \frac{w}{h} \right) - \frac{1}{2} \frac{w}{l} \sinh^{-1} \left( \frac{h}{l} \right) \\ &+ \left( \frac{\pi}{2} - \tan^{-1} \left( \frac{wh}{l^2 \sqrt{1 + \frac{g^2}{l^2}}} \right) \right) \\ &+ \frac{1}{3} \frac{l^2}{wh} \sqrt{1 + \frac{g^2}{l^2}} \left( 1 - \frac{1}{2} \frac{g^2}{l^2} \right) + \frac{1}{3} \frac{l^2}{wh} \\ &- \frac{1}{3} \frac{l^2}{wh} \sqrt{1 + \frac{w^2}{l^2}} \left( 1 - \frac{1}{2} \frac{h^2}{l^2} \right) \\ &+ \frac{1}{6} \frac{l}{wh} \left( \frac{g^3 - w^3 - h^3}{l^2} \right) \end{split} \end{split}$$
(5)

#### A. Verification

The nested configuration is produced in different windings ratios, sizes, and coupling ratios to validate the formulas. The transformers are produced in a standard 4 layer PCB configuration. The full configuration of the prototypes is listed in Table II. A prototype transformer is shown in Figure 2a.

 TABLE II

 PARAMETERS OF THE NESTED CONFIGURATION SOLENOIDS

	Dimensions [mm]					Tu	rns
Prototype	$w_p$	$h_p$	$w_s$	$h_s$	l	$N_p$	$N_s$
1	23.2	1.24	25	1.6	10.3	19	19
2	6.6	1.24	8.2	1.6	6.5	7	2
3	16.1	1.24	17.7	1.6	7.4	15	2
4	5.2	1.24	6.8	1.6	5.7	7	2

The measured inductances shown in Table III fit closely to the calculated with the highest deviation between calculated and measured being 18.7%. The coupling has a higher deviation than the inductances, since it is a combination of the deviations of the inductances, but still with a maximum deviation of 21.8%, which is comparable to formulas for other structures [20]. The inductance equations is in general good enough to use for design of transformers or coupled inductors.

TABLE III Comparison of analytic model and measurements

Variable	$L_{pp}$	$L_{ps}$	$L_{ss}$	k
Calculated [nH]	1119.17	1119.17	1499.16	0.86
Measured [nH]	1154.33	1104.82	1506.57	0.84
$\Delta$ [%]	3.05	1.30	0.49	2.89

(a) Solenoid transformer

Variable	$L_{pp}$	$L_{ps}$	$L_{ss}$	k
Calculated [nH]	65.98	20.91	9.17	0.85
Measured [nH]	67.40	17.62	9.58	0.70
$\Delta$ [%]	2.11	18.71	4.21	21.78
(1) ~ .				

(b) Solenoid transformer - 2

Variable	Lpp	$L_{ns}$	$L_{ss}$	k
Calculated [nH]	596.30	86.45	15.77	0.89
Measured [nH]	592.14	76.84	18.54	0.74
$\Delta$ [%]	0.70	12.50	14.95	20.54

(c) Solenoid transformer - 3

Variable	$L_{pp}$	$L_{ps}$	$L_{ss}$	k
Calculated [nH]	52.47	16.64	7.68	0.83
Measured [nH]	53.40	14.17	8.22	0.68
$\Delta$ [%]	1.75	17.42	6.63	21.83

(d) Solenoid transformer - 4



Fig. 5. Dimensions of the PCB embedded solenoid transformer (nested configuration)

#### V. Applied design

The nested configuration is used in an half-bridge VHF resonant power converter presented in [21]. The converter is a class-DE type, with a passive gate drive [22] for both the high-side and low-side. Each gate drive circuit has an inductor  $L_{G(1,2)}$  in series with the MOSFETs gate. For the class-DE converter to work properly in the VHF area, the switch timing between the high-side and lowside is critical. The two separate inductors can be made by a coupled inductor instead, which will force the gate currents to be 180° phase-shifted, and ensure a better timing, resulting in higher efficiency. As the gate drive circuit should see the same inductance as when the gate inductors are not coupled, the primary  $L_{pp}$  and secondary inductances  $L_{ss}$  values should be chosen so the leakage inductance corresponds to the original  $L_G$ , leading to (6). If the coupling is close to one, the inductances would go to infinity, hence large couplings are for any applied purpose unpractical, as the coupled inductor will be very large. A coupling of k = 0.6 is chosen as a good compromise, leading to an inductance matrix of (7).

$$L_{pp,ss} = \frac{L_G}{1-k} \tag{6}$$

$$\begin{bmatrix} L_{pp} & L_{ps} \\ L_{sp} & L_{ss} \end{bmatrix} = \begin{bmatrix} 375\text{nH} & 225\text{nH} \\ 225\text{nH} & 375\text{nH} \end{bmatrix}$$
(7)

#### A. Coupled inductor design

The coupled inductor is designed with the formulas presented in Section IV, with the simplifications implemented. The length of the inductors are matched (as close as possible) and the widths  $w_p$  and  $w_h$  are set as close as possible. The PCB production sets certain limits on the inductors, e.g. as the width of each trace can be no smaller than the minimum via hole size, the clearance between the traces, as well as the width of the inner inductor must have a minimum clearance to the outer inductor, etc. All the restrictions does that not all combination of  $L_{pp}$ ,  $L_{ss}$  and  $L_{ps}$  can be obtained. The specific design is found using a genetic algorithm to optimize the transformer to the given inductance matrix. The algorithm has been set to favorite the leakage inductance to ensure the high-side and low-side gate-drive are matched.

#### B. Experimental

The class-DE converter from [21] is used as base performance. The schematic is shown in Figure 6, with the corresponding component values in Table IV.



Fig. 6. Converter schematic of the class-DE inverter with coupled inductors in the self-oscillating gate drive

TABLE IV

Component values for class-DE converter

Component	Value
$C_{in}$	4.7nF
$C_s$	14pF
$C_{GD}$	6pF
$C_{GS}$	82pF
$C_{GDext}$	39pF
$L_G$	150nH
$C_{G1}$	100nF
$L_H$	3.3µH
$C_T$	500 pF
$L_T$	360nH
$C_R$	$40 \mathrm{pF}$
$C_{OUT}$	14nF

TABLE V

Comparison of the class-DE converter with different gate drive inductors

Converter	$L_{pp}$	$L_{ps}$	$L_{ss}$	k	$L_{pp,leak}$	$L_{ss,leak}$	$P_{in}$	$P_{out}$	n
Base configuration	150 nH	-	150 nH	-	-	-	12.21W	9.57W	78.87%
Leakage based	120nH	-	100nH	-	-	-	10.25W	6.44W	63.1%
Coupled inductor	238.5 nH	165 nH	333.5 nH	0.58	120.5	102.8	11.32W	9.12W	81.09%

The converter performance is tested at 80V input, and the efficiency is measured with a Yokogawa WT1600. The converter, shown in Figure 7, is tested with three different  $L_G$  configurations:

- 1) The original inductors
- 2) Inductors with the value of the leakage inductance
- 3) The coupled inductor

The leakage inductor value, are two separate inductors with the value of the leakage inductance of the coupled inductor. This is to check whether it is the coupling or the slight change in inductance that causes any effect in the circuit. The inductor measurement and efficiencies are shown in Table V. The base efficiency is 78.87%, and with the leakage-valued inductors the efficiency is at 63.1%. The coupled inductor increase the efficiency by 2.2% points from the base value to 81.09%.



(b) Coupled PCB embedded gate driver inductors

Fig. 7. Class-DE converters used for efficiency comparison

#### VI. CONCLUSION

New structures for PCB embedded air-core transformers was proposed based on the rectangular solenoid structure, for use in VHF converters. The structures were evaluated for the use as a transformer, by comparing the coupling of the transformers. The structure of two solenoids nested inside each other, was found to be the most promising. An analytic two-port model for the structure was developed and verified by measurements on prototypes of the configuration. The formula shows a good consistency between the calculated and measured inductances, with a deviation range of approximately 3 % to 22 %. The proposed analytical model is suitable to predict the inductive parameters of the nested configuration of the PCB embedded air-core solenoid transformers.

The use of a coupled inductor in the self-oscillating gate drive in a class-DE converter shows that PCB embedded air-core solenoid inductor are suitable for using in VHF converters.

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# Self-oscillating Galvanic Isolated Bidirectional Very High Frequency DC-DC Converter

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## Self-oscillating Galvanic Isolated Bidirectional Very High Frequency DC-DC Converter

Jeppe A. Pedersen\*, Mickey P. Madsen\*, Arnold Knott\*, Michael A. E. Andersen\* \*Technical University of Denmark Ørsteds Plads, building 349

2800 Kongens Lyngby

Denmark

Email: {jarpe, mpma, akn, ma}@elektro.dtu.dk

Abstract—This paper describes a galvanic isolated bidirectional Very High Frequency (VHF = 30 MHz - 300MHz) Class-E converter. The reason for increasing the switching frequency is to minimize the passive components in the converter. To make the converter topology bidirectional the rectifier has to be synchronous. This increases the complexity of the gate drives, which in this paper is solved by using a self-oscillating gate drive. A bidirectional converter has been implemented and is described in this paper; the converter reaches efficiencies above 80% in forward conduction mode and 73.5% in reverse conduction mode. The designed converter operates at a switching frequency of 35.6 MHz, which is well within the VHF range. The same converter is also implemented with PCB embedded inductors to minimize cost and the physical volume of the total converter.

#### I. INTRODUCTION

In traditional Switch Mode Power Supplies (SMPS) small physical size is often a priority. The passive components usually take up most of the space and scale inversely with frequency and therefore increasing the switching frequency reduces the physical size of the overall converter. The switching frequency is typically limited to a few megahertz, this is where the switching losses become dominant as they increase linearly with frequency. Using resonant converters the switching losses can be significantly reduced, these types of converters are used in [1]-[5]. Increasing the switching frequency into the Very High Frequency (VHF = 30 MHz - 300 MHz) reduces the value as well as the physical size of passive components significantly, not just the energy storing components inside the converter also the EMI filter can be greatly reduced [6], [7]. The Class-E DC-DC converter topology, presented in [8] inspired by [9], is made with an inverter and a rectifier that both uses a resonant circuit to enable soft switching. This paper describes how the Class-E topology can be used for bidirectional VHF converters; this topology has two switching devises placed on each side of a resonant tank made with a capacitor in series with an inductor, to make this converter galvanic isolated the resonant capacitor is split into two capacitors where one is placed in series with the resonant inductor and one in the ground return path from the rectifier. Then an input and output filter which also helps to achieve soft switching in the inverter and rectifier. The symmetry around the resonant tank make the topology ideal for bidirectional operation. The schematic of the converter is seen in figure 1. The synchronous Class-E rectifier has been described in [10] and [11], and a bidirectional full-bridge class-E converter is implemented in [12] running at several hundred kilohertz. Bidirectional LLC converter have been used in different setups and shown that resonant converters are very suitable as bidirectional converter [13]-[15]. The bidirectional Class-E converter topology described in this paper could be suitable for many applications were size and price is a key consideration. One application for this converter is a single converter to charge a battery and then deliver the power from the battery to a load when it is not charging. This could be charging a battery from a PV panel during the day and delivering the power to an LED during the night. Another use of such a converter could be voltage sharing of batteries were two batteries need to have the same voltage. In future prospects this type of converter could also be integrated inside a chip, which can have two different transfer ratios depending on which way the chip is placed. This would cut the production cost for such a converter. Since this converter is galvanic isolated it is suitable for auxiliary supplies on the secondary side of an isolated converter. The converter is designed with a self-oscillating gate drive described in [10] that drives the MOSFET both in the inverter and the rectifier. This gate drive has shown great potential for normal VHF converters and in this paper it is used for driving a bidirectional converter.

#### II. THEORY

The converter is made as a standard Class-E converter in both directions, this is done by calculating the component values of the converter in forward direction, then afterward the reverse direction from the given resonant tank. To enable bidirectional power flow in a Class-E converter the rectifier needs to be implemented with a MOSFET and thereby becoming a synchronous rectifier as shown in figure 1. The use of VHF converters with synchronous rectification is a challenge due to the gate signals timing. The gate signals amplitude and duty cycle needs to be tightly controlled to ensure ZVS on the MOSFET in the rectifier and to keep the gate losses to a minimum. The design for the inverter is inspired from the method used in [16], made for a Class- $\phi_2$  converter which is described in [17]. Where the impeadance of the circuit is matched to create a half sine on the drain of the MOSFET at the frequency needed to ensure ZVS in the inverter. The design method is changed to fit a Class-E inverter as described in [10]. This method is not ensuring a perfect sinusoidal current through the resonant tank but only that the ZVS of the MOSFET is achieved.



Fig. 1. Schematic of a bidirectional Class-E converter

#### A. Forward conduction mode

The forward conduction mode is when power is drawn from  $V_{IN}$  and delivered to  $V_{OUT}$  and the reverse conduction mode is the other way. The first step when designing the power stage is to make the rectifier. For a rectifier with a duty cycle D = 50%, the inductor  $L_{OUT}$  and the capacitor  $C_{S2}$  is chosen so they resonate at the switching frequency, and the output capacitor  $C_{OUT}$  is chosen to be large enough to limit the output ripple. The input impedance of a Class-E rectifier at different duty cycles can be found in [18], for D = 50% the input impedance of the rectifier is:

$$Z_{IN} = 0.5760 \cdot R_L \tag{1}$$

When the rectifier and its input impedance is found the inverter can be calculated. First the drain source voltage of the MOSFET is assumed to be a half wave rectified sine, hence the peak voltage is:

The peak voltage is used to find the rms value of a half wave rectified sine:

$$V_{DS,rms} = V_{DS,peak} \sqrt{\frac{D}{2}} \tag{3}$$

The rms value of the output voltage is found from:

$$V_{OUT,rms} = \sqrt{P_{OUT} \cdot Z_{IN}} \tag{4}$$

The needed reactance of the resonance circuit can now be determined by [10]:

$$X_{RC} = Z_{IN} \cdot \sqrt{\left(\frac{V_{DS,rms}}{V_{OUT,rms}}\right)^2 - 1}$$
(5)

By combining equation 2, 3, 4, and 5, an expression for the needed reactance as function of input voltage, duty cycle, output power, and load is obtained:

$$X_{RC} = Z_{IN} \cdot \sqrt{\frac{V_{IN}^2 \cdot \pi^2 \cdot D}{2 \cdot (2 \cdot D - 2)^2 \cdot P_{OUT} \cdot Z_{IN}}} - 1 \quad (6)$$

The reactance of the resonant tank has to match the calculated reactance for the given design, if the capacitor  $C_{RES2}$  is chosen to be much bigger than the  $C_{RES1}$  it can be neglected in the calculations, and hence the reactance of the resonant tank is:

$$X_{RC} = 2 \cdot \pi \cdot f_r \cdot L_{RES} - \frac{1}{2 \cdot \pi \cdot f_r \cdot C_{RES1}}$$
(7)

Where  $f_r = \frac{f_s}{2 \cdot (1-D)}$  is the frequency of the half wave sine. Last the input inductor is found this helps ensuring soft switching in the inverter, this is found by:

$$L_{IN} = \frac{1}{4 \cdot C_S \cdot f_r^2 \cdot \pi^2 - \frac{2 \cdot \pi \cdot f_r}{X_{RC}}}$$
(8)

Where  $C_S = \frac{C_{S1}}{1-D}$  is the effective capacitance of  $C_{S1}$ . When the converter is designed in the forward direction the component values is fixed this limits the possibilities of optimizing the circuit in reverse direction. However there is still some degree of freedom such as the choice of load impedance or change of switching frequency.

#### B. Reverse conduction mode

When designing the bidirectional converter in the reverse conduction mode the first thing is to calculate the resonance of  $L_{IN}$  and  $C_{S1}$ , this limits the frequencies of the converter in this direction, and if the same frequency is maintained as in forward operation the load options is limited. In this section the switching frequency is set to be the same as in forward direction to simplify the calculations. The values of  $L_{IN}$ and  $C_{S1}$  determines the duty cycle of the rectifier in reverse conduction mode and this affects the input impedance of the rectifier. When this is found the equations 6, 7 and 8 described in the forward conduction mode can be used to determining the duty cycle of the inverter. Most VHF converter have a resonant gate drive driving the MOSFETs with a sinusoidal current, when using such a gate drive, the duty cycle can easily be changed by a varying DC offset. By doing this the duty cycle can be changed and there by also changing the output power of the converter.

#### III. BIDIRECTIONAL CONVERTER

To test the circuit a bidirectional converter has been designed. The converter is operating at low voltages were the benefit of having a synchronous rectifier is highest. This circuit is intended to operate from 14 V to 7 V in the forward conduction mode and from 7 V to 3.5 V in the reverse conduction mode. All specifications are shown in table I. The switching frequency is set just inside the VHF range. The power level is intended for charging of a battery in the forward conduction mode and delivering power from the battery to an LED in the reverse conduction mode. The circuit can either be connected to the charger or the LED.

TABLE I.	DESIGN SPECIFICATION FOR THE CLASS-E CONVERTER
----------	------------------------------------------------

Power flow	$V_{IN}$	$V_{OUT}$	$f_s$	$P_{OUT}$	$R_L$
Forward	14	7 V	37 MHz	5 W	10 Ω
Reverse	7	3.5 V	37 MHz	1.5 W	10 Ω

#### A. Gate drive

One of the main reasons to keep the switching frequency constant in both directions is to make the gate drive implementation easier. For the prototypes in this paper the gate drive is implemented with the self-oscillating passive gate drive described in [10]. The benefit of this gate drive is that it is controlled by the drain voltage so when the inverter starts sending power through the resonant tank the voltage across the MOSFET in the rectifier will rise and start the oscillation on the gate. For simplicity the gate drives for the MOSFETs are the same in the inverter and rectifier, the schematic is shown in figure 2.



Fig. 2. Schematic of a basic self-oscillating gate drive were  $L_G$  and  $C_G$  is external components

To be able to simulate the converter the gate drive has to be found. Both MOSFETs  $(M_1 \text{ and } M_2)$  are chosen to be the FDC8601 from Fairchild as they have relatively low parasitic capacitance. Because they are both the same MOSFETs the external components in the gate drive can be the same for simplicity. First the gate drive for the inverter in the forward direction are designed to have gain of -10 dB and a phase shift close to  $180^{\circ}$  from drain to gate. This ensures that the MOSFET is soft switching and that the gate signal is large



Fig. 3. Waveforms from simulation of the converter in forward conduction mode,  $V_{M1}$  and  $V_{M1}$  are the voltage across the MOSFETs

enough to fully turn on the MOSFET. The gate drive in the rectifier is implemented with the same external components but here the gain of the gate dive are -4 dB as the parasitic capacitances are higher at lower drain-source voltages. The higher gain in the gate drive is beneficial since the drain voltage in the rectifier is smaller.

#### B. Simulation

With the gate drive, the converter was simulated in LTspice. The drain voltages of the two MOSFETs in forward conduction mode is shown in figure 3 and for the reverse conduction mode in figure 4. It is evident that the peak voltages are much higher than the in/output voltages, at 50% duty cycle the peak voltage across the MOSFET in a Class-E converter are 3.6 times the in/output for the inverter and rectifier respectively. The body diode is conduction a small period of time before the MOSFET turns on, this can be avoided by increasing the bias voltage seen in figure 2, the simulation are made with the components values stated in table II.

TABLE II. COMPONENT VALUES USED IN THE CLASS-E CONVERTER

Component	Value
$C_{IN}$	100nF
$L_{IN}$	350nH
$C_{S1}$	165 pF
$C_{RES1}$	1nF
$C_{RES2}$	100nF
$L_{RES}$	110nH
$C_{S2}$	160pF
LOUT	156nH
$C_{OUT}$	100nF
$L_G$	68µH
$C_G$	40pF

#### C. Implemented converter

The converter was implemented with discrete inductors from Coilcraft as shown in figure 5. The waveforms measured in the forward conduction mode resembles the simulations as shown in figure 6. The switching frequency of the converter is measured to be 35.6 MHz. This is close the desired 37 MHz, the shift in frequency is reasonable since the gate drive is selfoscillating and is not externally controlled. The converter has been measured in reverse conduction mode and the waveforms



Fig. 4. Waveforms from simulation of the converter in reverse conduction mode



Fig. 5. Prototype with discrete inductors and synchronous rectifier

is shown in figure 7. The voltage across  $M_1$  in reverse direction does not reach as high a voltage level as in the simulation, this could be due to the parasitics of the MOSFET which are more dominant at lower voltages. The efficiency of the converter in both directions is shown in figure 8, the efficiency is 80% for output powers above 1.5 W. In the forward conduction mode and above 70 %. The output power is changing over input voltage as shown in figure 9.

Implementing the magnetics as part of the PCB is widely used in traditional converters as described in [19], [20]. For VHF converters there is limited selection of magnetic materials since most materials does not operate well at these frequencies and therefore air core inductors are used. One form of air core inductors used for VHF converters is the PCB embedded inductors described in [21], [22]. A second identical prototype is made with PCB embedded inductors and compared to the



Fig. 6. Measured waveforms of the converter in forward direction



Fig. 7. Measured waveforms of the converter in reverse direction



Fig. 8. Measured efficiency vs. output power

first converter. The converter with PCB embedded inductors, is seen in figure 10. It only reach 74% efficiency in the forward conduction mode and 65% in reverse conduction mode. The reason for the lower efficiency is the low Q values for the PCB embedded inductors. The Q values of the PCB embedded inductors varies from 80 to 110 which is lower than what can be achieved with larger air core inductors. The volume of this converter with PCB inductors is significantly reduced as the PCB area remains the same where as the hight of the converter is significantly reduced. This can be very useful in many applications were size is an issue. The PCB embedded inductors has the benefit of being cheap and has a low spread in production. Both the converter with discrete inductors and the one with PCB embedded inductors is implemented as unidirectional converter with a diode rectifier operating in the forward conduction mode see figure 11. In this configuration the efficiency is roughly 2.5% lower than with the synchronous



Fig. 9. Measured output power vs. input voltage



Fig. 10. Prototype with PCB inductors and synchronous rectifier



Fig. 11. Unidirectional converter prototypes with diode rectifier, (a) with discreate inductors and (b) with PCB enbedded inductors

rectifier due to higher conduction losses in the diodes. This proves that the use synchronous rectifiers are very suitable for low voltage high current applications also in the VHF range.

#### IV. CONCLUSIONS AND FUTURE WORK

In this paper a VHF bidirectional converter has been implemented and presented, it has been proven that the Class-E converter topology it is able to operate as a bidirectional converter in the VHF range. The implemented converter achieves high efficiency in both operating modes over varying input voltages and output powers. This type of converter can be used in various applications where a small bidirectional converter is needed. The price of this type of converter is relatively low since it only uses ceramic capacitors, air core inductors and two MOSFETs. By using PCB embedded inductors the price and the physical size of the converter can be reduced further however in this case it does decrease the efficiency.

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## Input-Output Rearrangement of Isolated Converters

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### Input-Output Rearrangement of Isolated Converters

Mickey P. Madsen\*, Milovan Kovacevic\*, Jakob D. Mønster\*, Jeppe A. Pedersen\*, Arnold Knott\*, Michael A. E. Andersen\* \*Technical University of Denmark Ørsteds Plads, building 349 2800 Kongens Lyngby Denmark Email: {mpma, mikov, jdomo, jarpe, akn, ma}@elektro.dtu.dk

Abstract— This paper presents a new way of rearranging the input and output of isolated converters. The new arrangement posses several advantages, as increased voltage range, higher power handling capabilities, reduced voltage stress and improved efficiency, for applications where galvanic isolation is not a requirement. The proposed technique is particularly valuable in power conversion at very high frequencies, and may be combined with other stress reduction methods. Finally, the new arrangements are experimentally verified both on off the shelf converters and on a VHF resonant SEPIC converter. All results are in good agreement with the theory and twice the power handling capabilities and 5-10% higher efficiencies are shown.

#### I. INTRODUCTION

Constant strive for cost and size reduction of power converters, as well as better performance, results in higher and higher switching frequencies. From the size and cost perspective, higher frequencies are desirable since energy storage requirements drop linearly with frequency, even though the components size and price do not typically scale at the same rate. An added benefit is cost and size reduction of filtering components. Recent advances in switching devices technology [1] and magnetic materials [2], [3] allowed converter operation in low-MHz range with high efficiencies [4]–[7]. If the switching frequency is pushed beyond 30 MHz, class E derived topologies - class E, resonant boost, resonant SEPIC, etc. - made it possible to use air-core magnetics, which eliminates core loss mechanism entirely [8], [9].

However, loss mechanisms in the switches start to dominate the total loss budget at higher frequencies. In low-MHz range, switching loss already gives incentive for use of resonant transition or quasi square-wave converter topologies (boost [10], inverted buck [6], flyback [11]). For operation above 30 MHz, switching losses impact converter efficiency so severely that only ZVS (zero voltage switching) topologies become practical. Even then, gating loss needs to be accounted for, regardless of the gating technique: hard-gating, singleresonant, or multi-resonant [12]. Needless to say, proper utilization of the switching components, especially in pricesensitive applications, is a must.

Class E derived converters exhibit voltage stress on the inverter switch of typically between 2.5 and 3.6 times input voltage, depending on the switch duty cycle [13]. As a consequence, devices with high voltage ratings are required.

These devices typically perform worse compared to their lower voltage counterparts, as voltage rating comes at the expense of increase in  $R_{DS,on}$  with all other parameters held the same. It is therefore of interest to reduce switch voltage blocking requirement in order to improve performance.

Voltage stress in these converters can be reduced by employing multi-resonant networks, either transmission line [14] or discrete with limited number of harmonics [15]-[17]. By implementing these techniques, switch voltage stress in VHF converters can be reduced to 2-2.5 times input voltage for the same duty cycle, but this technique requires extra resonant elements. Another approach infers single switch quasi squarewave converter topologies. The downside of quasi square-wave converters is limited converter transformation ratio (inverted buck, boost), or excessive ringing on the primary switch due to leakage inductance (flyback). In [18] a self-oscillating drive method was used to obtain a VHF self-oscillating DE inverter, in which the switch voltage stress is limited to input voltage. Finally, converter cell stacking [19], [20] reduces the switch voltage stress by N compared to a single cell case, where N is the number of converter cells. However, control becomes more complicated since it is required to balance voltages across the cells, and certain start-up issues may occur.

This paper presents a voltage stress reduction method, which may be used in either step-up or step-down applications where galvanic isolation is not a requirement. In addition to voltage stress reduction, it results in higher converter efficiency with minimum adjustments to the original circuit. Section II describes the method in detail. Section III shows experimental results when the principle is applied to conventional offthe-shelf design and a VHF prototype, respectively. Finally, Section IV concludes the paper.

#### II. THE BASIC PRINCIPLE

Fig. 1 shows the conventional input-output configuration of an isolated dc/dc converter. If two isolated converters have their inputs connected in parallel and outputs connected in series, we obtain the structure in Fig. 2 (top). Similarly, if the inputs are connected in series and outputs in parallel, the structure in Fig. 3 (top) is obtained. Let us assume that one of the converters in each configuration is with 1:1 voltage transformation ratio. In such case, it is possible to connect its input to its output directly and remove 1:1 converter from the circuit, without effecting the rest of the system. In doing so, part of the delivered power flows directly from input to the output, and is not processed by the converter. As a consequence, higher converter efficiency is achieved. Moreover, compared to the single cell design, voltage and/or current stresses on the switches are reduced. The only difference is that the input is not galvanic isolated from the load. Fig. 2 and 3 (bottom) demonstrate the final connection rearrangement to obtain step-up and step-down configuration, respectively.

To quantify the benefits from the proposed configurations, we analyze the case where input voltage  $V_{in}$  and output voltage  $V_{out}$  are held constant across all configurations. Moreover, output current  $I_{out}$  and output power  $P_{out}$  are held constant as well. A distinction is made between the power processed by the converter  $P_C$ , and  $P_{out}$ .

Voltage transformation ratio of the conventional converter is

$$M = \frac{V_{out}}{V_{in}} \tag{1}$$

In step-up and step-down configurations, transformation ratio of the converter cell only becomes

$$M_{up} = \frac{V_{out} - V_{in}}{V_{in}} \tag{2}$$

$$M_{down} = \frac{V_{out}}{V_{in} - V_{out}} \tag{3}$$

In general, switch voltage stress is a function of both input and output voltages. In step-up configuration, output voltage stress contribution is reduced by a factor of  $(1 - V_{in}/V_{out})$ . In step-down configuration, input voltage stress contribution is reduced by  $(1 - V_{out}/V_{in})$ .

Output power of all three configurations is the same:

$$P_{out} = V_{out} I_{out} \tag{4}$$

The power processed by the converter  $P_C$  in the conventional structure is equal to  $P_{out}$ . In the step-up and step-down cases, this power is given as

$$P_{C,up} = P_{out} \left( 1 - \frac{V_{in}}{V_{out}} \right) \tag{5}$$

$$P_{C,down} = P_{out} \left( 1 - \frac{V_{out}}{V_{in}} \right) \tag{6}$$



Fig. 1. Conventional isolated dc/dc converter topology. Dashed line represents galvanic isolation.



Fig. 2. Step-up configuration: two converter cells with inputs in parallel and outputs in series (top) and a single cell equivalent (bottom).



Fig. 3. Step-down configuration: two converter cells with inputs in series and outputs in parallel (top) and a single cell equivalent (bottom).



Fig. 4. Power processed by the converter and efficiency improvement by rearranging.

 $P_{C,up}$  and  $P_{C,down}$  are smaller than  $P_{out}$ , and the remaining power is delivered through the DC path. Efficiency of that power transfer is very close to 100%. Assuming that  $P_C$ ,  $P_{C,up}$ , and  $P_{C,down}$  are transfered with the same efficiency  $\eta$ , effective efficiencies of the step-up and step-down configurations can be expressed in terms of  $\eta$ ,  $P_{out}$ , and  $P_{C,up/down}$ :

$$\eta_{up/down} = \eta \; \frac{P_{C,up/down}}{P_{out}} + \frac{P_{out} - P_{C,up/down}}{P_{out}} \tag{7}$$

Equations 5-7 are illustrated in Fig. 4. The plot clearly shows that for limited step-up or step-down ratios, the percentage of the output power processed by the converter is small and hence the efficiency improvement becomes significant. For a step-up converter with 330V input and 400V output only 17.5% of the output power would be processed by the converter and if the converter efficiency were 80%, the rearranged efficiency would be 96.5%. The converter would in that case have to be designed as an galvanic isolated converter with 330V input, 70V output and a peak output power equal to 17.5% of the required power. Hence a high power boost converter with high efficiency could be replaced by a low power flyback or SEPIC converter with moderate efficiency while achieving the same overall system performance.

Adaptations shown in Fig. 2 and 3 can be used for any type of isolated converter, regardless of the isolation type (inductive or capacitive). In Fig. 5, a flyback converter is used in a step-up configuration, along with simulated waveforms. Fig. 6 presents



Fig. 5. Flyback converter in step-up configuration (top) and simulated waveforms of a quasi square-wave 1:2 flyback converter in conventional (solid black) and step-up (dashed red) configuration. Diode voltage and switch current stresses are reduced by a factor of 2. Output capacitance is formed by series connected  $C_{out}$  and  $C_{in}$ .

a class DE converter (DE inverter and DE rectifier) in stepdown configuration.

The proposed technique may be used together with multicell stacked designs, as shown in Fig. 7. This also adds complexity to control circuitry since it needs to monitor and balance voltages across the cells.



Fig. 6. Class DE converter in step-down configuration with output referenced to the inverter input. Parasitic capacitances of the switching devices are included implicitly.



Fig. 7. Two stacked converters in step-down configuration.

#### **III. EXPERIMENTAL RESULTS**

#### A. Off the shelf converter

In order to experimentally verify equation 5-7 a test setup with two isolated 12-12V DC/DC converters (Murata NTE1212MC and CUI Inc PDS1-S12-S12-S) has been made. The setup is made with five jumpers allowing the setup to be changed between normal configuration (12-12V), step down (24-12V) and step up (12-24V).

The measured efficiency as function of output power is shown in Fig. 9. The increased efficiency and power handling capability in the new configurations are clearly seen. With a 1-2 or 2-1 step ratio the converter only handles 50% of the output power (see equation 5-6). The power handling capability is hence doubled while the efficiency is increased across the entire load range with half the loss at full load.

#### B. Resonant SEPIC converter

As mentioned in Section I, the input and output voltage and the subsequent voltage stress on the semiconductors is of high importance in resonant converters. The availability of



(a) Schematic



(b) PCB

Fig. 8. Test board for evaluation of the principle.



Fig. 9. Measured performance improvements of two rearranged converters.



Fig. 10. Resonant SEPIC converter with capacitive galvanic isolation.

suitable semiconductors is reduced significantly as the break down voltage requirement gets above 100 V. Furthermore the amount of resonating current needed in order to achieve zero voltage switching scales with the voltage squared, hence a reduction in input and output voltage will lead to significantly lower currents and thereby also reduced losses due to ESR in the components.

As the switching loss in resonant converters with ZVS is reduced to a minimum, these converters are operable at several tens of MHz [12], [15]–[19], [21]–[32]. At these frequencies, galvanic isolation can be achieved simply by adding a small capacitor in the return path between the inverter and rectifier.

The proposed rearrangement is hence extremely well suited for non-isolated converters where very high frequency resonant converters can be used to achieve high power density, low cost and weight and still keep the efficiency high. In order to show the benefit in these type of converters a resonant SEPIC converter (see Fig. 10) switching at 50 MHz has been implemented and tested on the test board in Fig. 8.

Figure 11 shows the performance improvements measured with this setup. From the plot it is clearly seen that both the efficiency and the voltage and power handling capability are increased. The measurements and theoretical values for the step down version fits well as the loading conditions as well as the input voltage are the same. For the step-up version the output voltage from the converter changes quite dramatically as the input voltage is increased and becomes close to zero towards the end.

In [18] the same principle is shown for a capacitively isolated VHF class DE converter. Here the rearangement increases the efficiency by 5-10% across a wide input voltage range. At the same time the input voltage and output power is increased by approx 50%.

#### IV. CONCLUSION

The paper presents a voltage and/or current stress reduction technique for isolated dc-dc converters in applications where isolation is not a requirement. The technique provides higher efficiency compared to a conventional single cell design, and it can be combined with other methods of voltage stress reduction, as long as the initial converter provides capacitive or inductive isolation. Obtained benefits are considered very appealing for certain non-isolated applications, such as LED



Fig. 11. Measured performance improvement of a VHF resonant SEPIC.

lighting. Theoretical analysis and experimental results are provided and are in good agreement. Twice the power handling capabilities and 5-10% higher efficiencies are shown for the tested converters.

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# US Mains Stacked Very High Frequency Self-oscillating Resonant Power Converter with Unified Rectifier

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## US Mains Stacked Very High Frequency Self-oscillating Resonant Power Converter with Unified Rectifier

Jeppe A. Pedersen\*, Mickey P. Madsen\*, Jakob D. Mønster\*, Thomas Andersen\*, Arnold Knott\*, Michael A. E. Andersen\* \*Technical University of Denmark Richard Petersens Plads, building 325 2800 Kongens Lyngby Denmark Email: {jarpe, akn, ma}@elektro.dtu.dk

Abstract—This paper describes a Very High Frequency (VHF) converter made with three Class-E inverters and a single Class-DE rectifier. The converter is designed for the US mains (120 V, 60 Hz) and can deliver 9 W to a 60 V LED. The converter has a switching frequency of 37 MHz and achieves an efficiency of 89.4%. With VHF converters the power density can be improved and the converter described in this paper has a power density of 2.14 W/cm3. The power factor (PF) requrements of mains connected equepment is fulfilled with a power factor of 0.96.

#### I. INTRODUCTION

In traditional Switch Mode Power Supplies (SMPS) the passive components occupies most of the volume. Increasing the switching frequency reduces the physical size of the power supply since the passive components scale inversely with frequency. The switching frequency of hard switching converters is typically limited to a few megahertz due to switching losses and limited selection of commercial available gate drivers operating at higher frequencies. In resonant converters using soft switching the switching losses can be neglected and is therefore not limiting the frequency. Therefore when increasing the switching frequency to the Very High Frequency (VHF) range (30 MHz - 300 MHz) resonant converter topologies are used [1]-[5]. Most VHF converters consist of an inverter and a rectifier. The VHF converter described in this paper consists of three Class-E inverters [6], [7], and one Class-DE rectifier described in [8]-[12]. One of the challenges with the Class-E resonant inverter when using a high input voltage is the peak voltage across the MOSFET which theoretically is  $V_{peak} \approx 3.6 \cdot V_{in}$  when the duty cycle is 50% [8]. If a single Class-E inverter were to operate from the US mains (120 V, 60 Hz) the MOSFET should be at least 650 V devise to withstand the voltage peak. As there do not exist 650 V devises with good characteristics, three inverters is connected in series to divide the input voltage as in [13]. This reduces the peak voltage across the MOSFET in each Class-E inverter to one third. To decrease the input voltage of the three inverters further, the load is placed in series with the input of the inverters as described in [14]. The three inverters



Fig. 1. Configuration of the converter, each box has input on the left and output on the right side. The resonant tank is shown between the inverters and the rectifier.

share a single rectifier and has a combined resonant tank made with six capacitors and one inductor. The configuration of the inverters, rectifier and load is shown in Fig. 1. Each inverter is implemented with the self-oscillating gate drive described in [15] and used in [16], [17].

The schematic of the converter is seen in Fig. 2 where the dotted line shows the separation between the inverter, resonant tank and the rectifier. In this configuration each inverter's output is galvanic isolated from the rectifier by the two resonant capacitors, this is necessary because of the series connection of the inverters and the load. The converter is however not galvanicly isolated since the load is directly connected to the input diode bridge as seen in Fig. 1.

The converter described in this paper is designed to run from the US-mains delivering 9 W to a 60 V LED. The full specifications are shown in Table I. The LED market



Fig. 2. Schematic of the converter topologi used in this paper, the dotted line shows separation between the Class-E inverter, Resonant tank and the Class-DE rectifier. In the final converter three inverters are combined to a single rectifier.

 $\begin{array}{c|c} \mbox{TABLE I} \\ \mbox{Specifications} \end{array}$ 

is growing rapidly both with replacement bulbs and new LED fixtures. In this market a small size, high efficiency, and increased regulations regarding power factor (PF) is a challenge. This paper shows how this can be achieved by use of VHF converters.

#### II. THEORY

The converter consists of three Class-E inverters and a single Class-DE rectifier which is connected as shown in Fig. 1. When designing a resonant converter the rectifier is usually designed first. Then the inverter is designed to match the input impedance of the rectifier. The load is a 60 V LED and due to the high output voltage the Class-DE rectifier topology is chosen. The Class-DE rectifier has the advantage that the peak voltage across the diode is equal to the output voltage, which makes is suitable for high voltage applications. The design of a Class-DE rectifier is described in [8], [11]. The capacitances  $C_{D1}$  and  $C_{D2}$  is found by:

$$R_L = \frac{V_{out}}{I_{out}} = \frac{2 \cdot \pi}{\omega \cdot (C_{D1} + C_{D2})} \tag{1}$$

The input impedance of the Class-DE rectifier with D = 0.25 is:

$$Z_{IN} = \frac{1}{2 \cdot \pi} \cdot R_L \tag{2}$$

The design for the Class-E inverter is described in [16]. Each inverter is designed to work with a third of the rectifiers input impedance. The resonant inductor is designed as three separate inductors and then combined into one inductor. The resonant inductor can be combined since the output of the three inverters is in parallel. The value of the combined resonant inductor is equal to a parallel connection of the three separately calculated resonant inductors. With a combined inductor a



Fig. 3. Schematic of the gate drive with MOSFET parasitics.

higher Q can be achieved. This increases the efficiency and reduces component count. Another advantage of using a single resonant inductor is that the switching frequency of the three inverters is forced to synchronize.

The gate drive used in the inverters is shown in Fig. 3. This is a simple passive gate drive described in [15] where  $C_{GD}$ ,  $C_{GS}$  and  $R_{gate}$  is the parasitic components of the MOSFET. The gate drive creates a phase shift of 180° from drain to gate and maintains a sinusoidal gate voltage. The bias voltage is kept around the threshold voltage of the MOSFET to achieve 50% duty cycle.

#### **III. DESIGN AND SIMULATIONS**

The converter is designed to deliver 9 W from US mains (120 V at 60 Hz) with a 60 V LED as load. The converter is designed with a switching frequency of 37 MHz this frequency is chosen to place the second harmonic below the FM band (87.5 - 108 MHz) and the third harmonic above. The power balance design of the converter is described in this section. One of the three Class-E inverter is simulated together with a Class-DE rectifier designed for a single stage as a DC-DC converter as shown in Fig. 2. To speed-up the simulation process. The 37 Mhz converter is evaluated at different DC input voltages to equivalent the quasi stationary behaviour of the slow 60 Hz AC mains input. LT-Spice is used to simulate the converter with a simple model of the MOSFET including the parasitic capacitances and gate resistor.

When designing a resonant inverter it is important that the converter can operate in the desired voltage range. The converter is designed to deliver 2.5 W at  $V_{IN} = 30$  which is



Fig. 4. The input voltage after the rectification with markings for when the full converter are running.

a reasonable starting point. As each inverter will deliver less than a third of the total power to the load. The first simulation is used to find the minimum stable voltage. It shows that the converter start at 20 V where the gate drive has enough gain to maintain the resonating gate voltage. In case all three inverters are not perfectly sharing the input voltage the minimum turn on voltage is raised to 23 V. The maximum voltage can be found by (3).

$$V_{inv,peak} = \frac{V_{IN,peak} - V_{out}}{3} \tag{3}$$

When  $V_{IN,peak} = V_{IN,RMS} \cdot \sqrt{2} = 120 \text{V} \cdot \sqrt{2} \approx 170 \text{V}$  the maximum voltage for each inverter is 37 V.

With the minimum and maximum voltage for each inverter found and assuming the output voltage is a constant 60 V the converters ON period can be defined. The ON period of the rectified 60 Hz period is shown in Fig. 4.

When the operating voltage and the ON period is found the average input current  $I_{IN,AVG}$  in the ON period of the total converter can be found from (4).

$$P_{IN} = \frac{T_{ON}}{T_{Period}} \cdot \int_{t_1}^{t_2} V_{IN,peak} \cdot \sin(t) \cdot I_{IN,avg} \,\mathrm{d}t \qquad (4)$$

The input power is  $P_{IN} = \frac{P_{OUT}}{0.9} = 10 \text{ W}$  assuming an efficiency of 90%. The integral is found from  $t_1$  to  $t_2$  to integrate over the total ON perriod  $T_{ON}$ . By solving (4) for the average input current the result is  $I_{IN,avg} \approx 100 \text{ mA}$ .

When connecting the load in series with the inverters the output power can be split up into two different parts. The  $P_{INcurrent}$  is the part coming from the input current that runs through the inputs of the inverters. The  $P_{REC}$  is the part coming from the rectifier.

$$P_{OUT} = P_{INcurrent} + P_{REC}.$$
 (5)

 $P_{INcurrent}$  is found to be  $P_{INcurrent} = I_{IN,avg} \cdot V_{Load} \cdot \frac{t_{ON}}{t_{Period}} = 2.71 \text{ W}$ .  $P_{REC}$  is the total power from the rectifier and therefore each inverter need to deliver a third of this  $\frac{P_{REC}}{3} \approx 2.1 \text{ W}$ . The single converter is now simulated at



Fig. 5. Simulated output power vs. input voltage.

different input voltages where the output power is measured, this is done to avoid long simulations of the half sine at 60 Hz. The result of the simulations is shown in Fig. 5.

By making a linear approximation of the measurements shown in Fig. 5 a relationship between the input voltage and the output is defined (6).

$$Pout = 0.16 \cdot V_{Inv} - 1.8 \tag{6}$$

This can then be used to see how much power each converter delivers to the load over one period. The voltage across each inverter follows the form described in (7).

$$V_{Inv} = \frac{V_{IN,peak} \cdot sin(t) - V_{OUT}}{3} \tag{7}$$

When combining (6) and (7) the output power can be integtrated over an ON period which is used to verify the output power of a single inverter stage is reaching 2.1 W.

$$P_{out} = \frac{t_{ON}}{t_{Period}} \cdot \int_{t_1}^{t_2} 0.16 \cdot \frac{V_{IN, peak} \cdot sin(t) - V_{OUT}}{3} - 1.8 \, \mathrm{d}t$$
(8)

The single converter is delevering 2.13 W in a full period. The components used in a single converer stage is described in Table II. The component values will change in the resonant tank and the rectifier when all three inverters shares one single rectifier.

 TABLE II

 COMPONENT VALUES FOR A SIGLE INVERTER AND RECTIFIER.

Component	Value
$C_{IN}$	1 µF
$L_{IN}$	1 µH
$C_{S1}$	18 pF
$C_{RES1}$	39 pF
$C_{RES2}$	4.7 nF
$L_{RES}$	1.24 µH
$C_{D1}$	7 pF
$C_{D2}$	7 pF
$C_{OUT}$	1 µF
$L_G$	82 nH
$C_G$	39 pF



Fig. 6. Drain waveforms from simulation of the inverter at the mimimum and maximum input voltages.

To verify the behavior of the converter within the full voltage range simulations are performed. The converter is operating in the full voltage range. The drain waveforms from simulation at minimum and maximum input voltage are shown in Fig. 6, the converter is ZVS at both input voltage. The selfoscilating gatedrive causes the switching frequency to change depending on the input voltage. The frequency change comes from the nonlinear parasitic capacitances of the MOSFETs. The change in frequency are relativly small is in not a problem regarding the FM-band.

#### IV. EXPERIMENTAL RESULTS

The converter is implemented with a single rectifier to reduce component count. Because the rectifier is connected in parallel with all three inverter the input impedance should be three times higher that for a single inverter stage. By looking at (1) that means that the two capacitances is getting 3 times as large. The three resonant tank inductors can also be combined into a single resonant inductor. A single resonant inductor will only be a third on the value and can have a higher Q which means higher efficiency. The component list is shown in Table III. The inductors used as input inductor's  $(L_{IN})$ is the 1812CS series from Coilcraft and the gate inductor's  $(L_G)$  is the 1008CS series. The common resonant inductor is chosen to be a 2929SQ air inductor because this have a high O at 37 MHz. The MOSFET used in the inverters is IRF5802, which is a 150 V silicon MOSFET from International Rectifier. The diodes used in the rectifier is the 60 V schottky diode PMEG6010AED from NXP. The input bridge rectifier is the MBS2 which is rated for 200 V.

A picture of the converter is shown in Fig. 7. It measures 20.2mm x 38.2mm. The PCB is devided into two box volumes one is to the left of the large resonant inductor and one with the large resonant inductor. The distance from the left side of the PCB to the resonant inductor is 22.7 mm and the height in this part is 2.7 mm, the part with the resonant inductor is 9.3 mm in height. The converter is achieving an efficiency of 89.4% and a power density of 2.14  $\frac{W}{cm^3}$ . The temperature of the converter in steady state is shown in Fig. 8 were the warmest spot is the MOSFETs in the middle of the PCB reaching  $T_{max} = 58$  °C. The temperature test was performed

TABLE III Component values for the implemented VHF converter.

Component	Value	PCS
$C_{IN}$	1 μF	3
$L_{IN}$	1 µH	3
$C_{S1}$	18 pF	3
$C_{RES1}$	39 pF	3
$C_{RES2}$	4.7 nF	3
$L_{RES}$	430 nH	1
$C_{D1}$	21 pF	1
$C_{D2}$	21 pF	1
$C_{OUT}$	1 µF	1
$L_G$	82 nH	3
$C_G$	39 pF	3



38.2 mm

Fig. 7. The converter with three inverters and one rectifier.

with the PCB placed horisontal in a vise with 21 °C ambient temperature.

The converter is designed to run from the US mains and high PF is often a requrement for offline converters. This means that the converter starts once each inverter's input voltage reaches 23 V on the input and runs until the input voltage becomes too low for the self-oscillating gate drive to operate. This converter



Fig. 8. Image of the converter in steady state. The temperatures are shown in  $^\circ\mathrm{C}.$ 



Fig. 9. Measurements of the input voltage (yellow), input current (green) and output current through the LED (blue).

type works as a voltage controlled current source. The input voltage and input/output currents are shown in Fig. 9. It is evident that the input current is in phase with the voltage which is needed to achieve a high PF. The converter reaches a PF = 0.96, which is high for an offline LED driver in this power range. The converter achieves a high PF, this makes it suitable as a power factor correction (PFC) converter if prober contols is implemented. The converter shuts down twice every 60 Hz period which results in a 120Hz flicker at the output. To reduce this low frequency flicker an energy storage is needed. This could be a large capacitor at the output, however this would reduce the power density.

#### V. CONCLUSION

This paper describes a VHF converter driving a 60 V LED from the US mains. The converter consists of three Class-E inverters and one Class-DE rectifier. The converter has a switching frequency of 37 MHz and an efficiency of 89.4%. Increasing the switching frequency to the VHF range reduces the size of the passive components and thereby the size of the converter. This size reduction results in a high power density of  $2.14 \frac{W}{cm^3}$ . The input current is in phase and proportional to the input voltage which results in a PF of 0.96.

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# Offline Half Bridge "Charge Pump" Resonant Power Factor Correcting Converter with Frequency Control

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# Offline Half Bridge "Charge Pump" Resonant Power Factor Correcting Converter with Frequency Control

Jeppe Arnsdorf Pedersen, Jonathan N Davidson, and Martin P Foster

Abstract—This paper presents a mathematical model of a charge pump half- bridge resonant converter. The model is derived using the first harmonic approach. The model describes the impedance of the resonant tank network as a series connection of an equivalent capacitor and resistor. To validate the model, a frequency control method was developed. The frequency control method was used to achieve a power factor of 0.99 and reduce the input harmonics compared to fixed frequency operation. The converter was simulated and implemented and the performance of the converter with and without control were presented and compared.

### I. INTRODUCTION

Switch mode power supplies (SMPS) dominate the market for off-line power supplies. Traditional SMPSs, described in [1], use mainly hard switching topologies which limits operating frequency as a result of switching losses. Nevertheless, increased switching frequencies permit reduced volume and therefore alternative topologies which overcome this limitation are required. Resonant converter topologies are a prime example as they reduce the switching losses significantly and increases the maximum switching frequency limit. For consumer electronics some of most common resonant topologies are the LLC and LCC [1]-[4]. These topologies can be operated at a load independent point with a fixed input to output voltage ratio which makes them well suited for applications with a varying load. Other resonant topologies used today are the Class-E, Class-DE, and resonant Sepic [5]-[8] inspired by high frequency amplifiers connected to rectifiers. These converter topologies are suitable for applications with a constant output current. The simplest implementation of a resonant converter is a DC to DC converter with at a fixed output power which works very well for a single operating point. The resonant converters can have problems if ether the input voltage or load is changing, some topologies can be designed with a fixed voltage transfer function which makes it possible to change the load without changing the output voltage.

Resonant converters with a changing input voltage or a changing load need control to ensure soft switching, correct output power or to control the input current for maximum power-point tracking purposes. There are several control methods such as burst mode, phase shift and frequency control [8]–[12]. Changing the switching frequency allows the behaviour of the converter and its transfer function to be controlled. Frequency control is used to track changes in the load maintaining a constant output voltage or change the voltage transfer function with input voltage variations. With proper design, resonant converters can work at different input voltages and loads within certain limits. This technique is often seen in LLC

and LCC converters when they are used as the second stage after a AC-DC power factor correction (PFC) converter [13].

Single stage solutions for lighting applications are gaining impetus with light emitting diodes (LED) applications gaining prominence. For low power applications there are several appropriate topologies including traditional hard-switched topologies such as the flyback and newer resonant topologies which are described in [14]–[16]. These single stage solutions have also been investigated for fluorescent lighting [17]. Another approach to operate with varying input voltage for off-line applications is reported in [14]–[17], which achieves mains operation while maintaining high power factor (PF). These topologies are used in industry for fluorescent and LED lighting.

In this paper the first harmonic approach (FHA) is used to characterise the charge pump topology reported in [17] and shown in Figure 1. The FHA is a general way of analysing and understanding the operation of resonant converters [2], [18] through harmonic approximation of a piecewise analytical circuit model. The FHA analysis is described in detail in section III. The FHA model is verified using a novel frequency control method based on the input AC voltage. The control method was simulated and verified in hardware. Both the simulation and the measurement results are presented with and without the frequency control in section V and VI.

### II. ANALYSIS OF OPERATION

The converter in Figure 1 uses a resonant half-bridge topology. The resonant tank consists of inductor  $L_{res}$ , three capacitors  $C_{res}$ ,  $C_b$  and  $C_{in}$  and load resistor  $R_{load}$ . The converter operates at 50% duty cycle with extended dead time to enable the resonant current in  $L_{res}$  to charge or discharge the output capacitance of the MOSFETs until they reach the appropriate rail voltage thereby ensuring zero voltage switching. The purpose of the three capacitors are as follows: the resonant capacitor  $C_{res}$ . The capacitor  $C_b$  works as a DC blocking capacitor for the load.  $C_{in}$  is the charge pump capacitor which draws current from the mains and delivers it to the DC capacitor  $C_{DC}$ . The capacitor  $C_{in}$  is charged and discharged with  $|V_{AC}|$  each period, in steady state the current drawn from the mains tracks the AC voltage and leads to a good PF.

When analysing the high frequency operation of the converter, the AC input voltage is at such a low frequency that it can be treated as DC (therefore  $V_{AC}$  is constant over a few cycles). The converter operates in four different stages during a full cycle. The voltage,  $V_A$ , over the cycle is shown in Figure



Fig. 1. Schematic of the charge pump topology used.



Fig. 2. Normalized voltage at point  $V_A$  over a switching cycle.

2. The first stage from  $\theta_2 - \pi$  to  $\theta_1$  the resonant current passing through  $L_{res}$  goes into  $C_{res}$  and  $C_b$  and no current is flowing in  $C_{in}$ .

The second stage from  $\theta_1$  to  $\theta_2$  starts when  $C_{in}$  starts conducting, the resonant current now flows into  $C_{res}$ ,  $C_b$  and  $C_{in}$ . In  $S_2$  the current flowing through  $C_{in}$  is also flowing through  $D_5$  and into  $C_{DC}$ ,  $S_2$  stop when the current in  $C_{in}$  is  $I_{C_{in}} = 0$ .

The third stages is similar to the first where the resonant current is only flowing in  $C_{res}$  and  $C_b$ .

In stage fourth the capacitor  $C_{in}$  is active again. In this stage, the current is flowing from the AC mains through the diode bridge  $(D_1 \text{ to } D_4)$  and into  $C_{in}$ . Since  $V_{AC}$  is constant over the cycle, the energy stored in  $S_4$  must be equal to the energy discharged in  $S_2$ . The length of the four stages will change depending on  $V_{AC}$ . When the AC voltage is close to 0, the converter will operate mainly in  $S_1$  and  $S_3$ , whereas, when  $V_{AC}$  is high, the converter will operate mainly in  $S_2$  and  $S_4$ . The initial voltages for each stage is given in (1).

$$V_A = \begin{cases} V_{C_{DC}} - V_{ac}, & \theta = \theta_1 \\ V_{C_{DC}}, & \theta = \theta_2 \\ V_{ac}, & \theta = \pi + \theta_1 \\ 0, & \theta = \pi + \theta_2 \end{cases}$$
(1)

The voltage across the capacitor  $C_{in}$  does not change during  $S_1$  or  $S_3$  because no current flows through the capacitor, therefore the  $V_{Cin}$  is equal at the beginning of  $S_1$  and  $S_4$  and also  $S_2$  or  $S_3$ . The voltage across the capacitor  $C_{in}$  in  $S_2$  and  $S_4$  changes from 0 to the AC voltage. The initial voltage for capacitor  $C_{in}$  is listed in (2).

$$V_{C_{in}} = \begin{cases} V_{ac}, & \theta = \theta_1 \\ 0, & \theta = \theta_2 \\ 0, & \theta = \pi + \theta_1 \\ V_{ac}, & \theta = \pi + \theta_2 \end{cases}$$
(2)

Because the topology is drawing high frequency current from the mains it is necessary to filter the input current due to EMI, this filtering is done with  $L_{AC}$  and  $C_{AC}$ . For the converter to operate correctly the voltage across  $C_{DC}$  needs to be larger than the peak of the AC mains voltage to avoid a direct path from the mains to the  $C_{DC}$ . If this is achieved the only input current will be the high frequency current drawn from  $C_{in}$ . If the peak to peak voltage in  $V_A$  is kept at  $V_{C_{DC}}$ through a mains cycle the energy charged in the capacitor  $C_{in}$  is  $\frac{1}{2}C_{in} \cdot |V_{AC}|^2$ , the energy drawn from the mains are  $I_{AC} \cdot |V_{AC}|$  this leads to the relationship of

$$I_{AC} = \frac{1}{2}C_{in} \cdot |V_{AC}| \tag{3}$$

As seen the input current should be linearly proportional to the AC voltage ensuring a high power factor with low harmonics.

### III. THE FIRST HARMONIC APPROACH

In this section the circuit is analysed with the first harmonic approach. The goal is simplify the resonant circuit into a series connected LCR filter of the type shown in Figure 3. This simplified circuit will reduce modelling complexity and allow easier control. To analyse the resonant circuit with the FHA model, the charge pump circuit in Figure 1 must be simplified. The simplification is achieved in three steps

- 1) For a high-Q resonant tank, the input current is sinusoidal and therefore  $L_{res}$  can be replaced by an ideal sinusoidal current source of some unknown value,  $I_{in}$ .
- 2) For analysis at the first harmonic, the combination of  $C_{res}$ ,  $C_b$  and  $R_{load}$  can be combined into a single complex impedance. By splitting into real and imaginary parts, the impedance may be drawn as series-connected resistor,  $R_x$ , and capacitor,  $C_x$ .
- 3) The rectifier and half bridge at the input stage can be simplified to two diodes if bipolar  $V_{AC}$  is replaced with unipolar  $|V_{AC}|$ . To ease the math the input AC voltage will be written as  $V_{AC}$  in the rest of the paper and assumed positive.

The result of this simplification is shown in Figure 4. Since we are only concerned with the first harmonic and not DC effects,  $V_{AC}$  can be subtracted from each branch without affecting the RC branch for a further simplification shown in Figure 6.

In the analysis, all components are taken as ideal, the voltage  $V_A$  is defined to be minimum 0 V and maximum  $V_{ACpeak}$  (i.e.  $V_A$  min is taken as reference).

The resonant current  $I_{in}$  is defined in Equation 4, where Iin is the amplitude and  $\theta$  is the phase going in the range 0 to  $2\pi$  over a full cycle. The voltages in the four stages will be analysed on the basis of this resonant current.



Fig. 3. The final equivalent circuit model.



Fig. 4. Simplification of the circuit for the FHA model.

$$I_{in} = Iin \cdot \sin(\theta) \tag{4}$$

Now the voltages in the four stages will be analysed on the basis of this resonant current.

### A. First stage $(\theta_2 - \pi \le \theta < \theta_1)$

In the first stage, the charge pump capacitor,  $C_{in}$ , is not active and therefore the circuit can be simplified to that shown in Figure 5. The voltage  $V_A$  is defined as the voltage across  $C_x$  and  $R_x$ .

$$V_A = V_{Cx} + V_{Bx} \tag{5}$$

which can be found from Ohms law as

$$V_A = I_{in} \left( R_x + \frac{1}{sC_x} \right) = I_{in} \sin\left(\theta\right) R_x - \frac{I_{in} \cos\left(\theta\right)}{\omega C_x} + V_{in}$$
(6)

The initial voltage V1 can be found from (1) at either  $\theta_1$  or  $\theta_2$  and is shown here for  $\theta_2$ 



Fig. 5. The active resonant circuit in stage 1 and 3.



Fig. 6. The active resonant circuit in stage 2 and 4.

$$V1 = -\frac{Iin \left(-C_x \sin\left(\theta_2\right) R_x \omega + \cos\left(\theta_2\right)\right)}{\omega C_x} \tag{7}$$

### B. Second stage $(\theta_1 \leq \theta < \theta_2)$

In the second stage, the resonant current is divided into two parts: a current  $(I_1)$  through  $C_x$  and  $R_x$  and another through  $C_{in}$ . The latter is essential for the power factor capabilities of this topology. The two currents are shown in Figure 6. The resonant current  $I_{in}$  is found from

$$I_{in} = Iin \sin(\theta) = I_1(\theta) + I_2(\theta)$$
(8)

The voltage  $V_A$  is still defined as

$$V_A = V_{Cx} + V_{Rx} \tag{9}$$

The voltage  $V_A$  is then

$$V_A = I_1(\theta)R_x - \frac{\int I_1(\theta) \,\mathrm{d}\theta}{\omega \,C_x} + V2 \tag{10}$$

And the voltage across  $C_{in}$  is dependent on the current  $I_2$  and is defined as

$$V_{Cin} = \frac{\int I_2(\theta) \, \mathrm{d}\theta}{\omega \, C_{in}} + V_{Cin0} \tag{11}$$

The resonant current divides into the two currents  $I_1$  and  $I_2$  whose amplitude and phases may be calculated with referee to the impedance ratios X and IN.

$$X = \frac{Z_{Cin}}{Z_x + Z_{Cin}} = \frac{\frac{1}{j \cdot \omega \cdot C_{in}}}{R_x + \frac{1}{j \cdot \omega \cdot C_x} + \frac{1}{j \cdot \omega \cdot C_{in}}} \qquad (12)$$
$$= \frac{C_x}{j \omega C_{in} C_x R_x + C_{in} + C_x}$$

$$IN = \frac{Z_x}{Z_x + Z_{Cin}} = \frac{R_x + \frac{1}{j \cdot \omega \cdot C_x}}{R_x + \frac{1}{j \cdot \omega \cdot C_x} + \frac{1}{j \cdot \omega \cdot C_{in}}}$$
(13)
$$= \frac{C_{in}(j\omega C_x R_x + 1)}{j\omega C_{in} C_x R_x + C_{in} + C_x}$$

These are then used to calculate  $I_1$  and  $I_2$ 

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$$I_{1}(\theta) = |X| \operatorname{Iin} \sin\left(\theta + \arctan\left(\frac{\Im(X)}{\Re(X)}\right)\right) \qquad (14)$$
$$= |X| \operatorname{Iin} \sin(\theta + \angle X)$$

Where  $\Im(X)$  is the imaginary part of X and  $\Re(X)$  is the real part of X. As seen the equation is rewritten with angle  $\angle X$  which is the argument of X.

Having found  $I_1$ , we can now calculate  $V_A$  from (10).

$$V_A = |X| \operatorname{Iin} \sin(\theta + \angle X) R_x + \frac{|X| \operatorname{Iin} \cos(\theta + \angle X)}{\omega C_x} + V2$$
(15)

Where the initial voltage V2 found at  $\theta_2$  is

$$V2 = -\frac{|X| \operatorname{Iin} (\sin (\theta_2 + \angle X) R_x \omega C_x - \cos (\theta_2 + \angle X)) - V_{in} \omega C_x}{\omega C_x}$$
(16)

Likewise, the current  $I_2$  flowing through  $C_{in}$  is:

$$I_{2}(\theta) = |IN| Iin \sin\left(\theta + \arctan\left(\frac{\Im(IN)}{\Re(IN)}\right)\right)$$
(17)  
= |IN| Iin \sin(\theta + \alpha IN)

The phase  $\theta_2$  is found when the diode  $D_5$  stops conducting. The current in  $D_5$  is  $I_2$  and by solving for when the current reaches 0, the phase  $\theta_2$  is found

$$\theta_2 = -\arctan\left(\frac{\Im\left(IN\right)}{\Re\left(IN\right)}\right) + \pi = -\angle IN + \pi \qquad (18)$$

### C. The piecewise equation

Repeating this analysis for  $S_3$  and  $S_4$ , voltage  $V_A$  can be found for the complete cycle. The piecewise equation for  $V_A$ is hence given in 19

$$v_{A} = \begin{cases} -\frac{Iin \cos\left(\theta\right)}{\omega C_{x}} + V1 + Iin \sin\left(\theta\right) R_{x}, & \theta_{2} - \pi < \theta \le \theta_{1} \\ \frac{|X| Iin \cos\left(\theta + \Delta X\right)}{\omega C_{x}} + V2 \\ + |X| Iin \sin\left(\theta + \Delta X\right) R_{x}, & \theta_{1} < \theta \le \theta_{2} \\ -\frac{Iin \cos\left(\theta\right)}{\omega C_{x}} + V3 + Iin \sin\left(\theta\right) R_{x}, & \theta_{2} < \theta \le \theta_{1} + \pi \\ -\frac{|X| Iin \cos\left(\theta + \Delta X\right)}{\omega C_{x}} + V4 \\ + |X| Iin \sin\left(\theta + \Delta X\right) R_{x}, & \theta_{1} + \pi < \theta \le \theta_{2} + \pi \end{cases}$$
(19)

The initial voltages  $V_1$  to  $V_4$  are

$$V_{1} = -\frac{Iin\left(-C_{x}\sin\left(\angle IN\right)R_{x}\omega - \cos\left(\angle IN\right)\right)}{\omega C_{x}}$$
(20)

$$V2 = -\frac{|X| \operatorname{Iin} \left( \sin \left( \angle IN - \angle X \right) R_x \ \omega \ C_x + \cos \left( \angle IN - \angle X \right) \right) - V_{in} \ \omega \ C_x}{\omega \ C_x}$$
(21)

$$V3 = -\frac{Iin\,\sin\left(\angle IN\right)R_x\,\omega\,C_x - V_{in}\,\omega\,C_x + Iin\,\cos\left(\angle IN\right)}{\omega\,C_x} \tag{22}$$

$$V4 = -\frac{Iin |X| \left(-C_x \sin\left(\angle IN - \angle X\right) R_x \omega - \cos\left(\angle IN - \angle X\right)\right)}{\omega C_x}$$
(23)

Having developed this describing function, it is necessary to calculate the amplitude of the resonant current Iin needed to ensure steady state That is, the exact current needed to ensure  $V_A$  goes from 0 to  $V_{DC}$  each cycle. Since  $V_A$  is a continuous waveform with no discontinuities,  $V_A$  must be equal at the boundaries between stages. The describing function shown in 19 have the initial voltages V1 to V4 defined from  $\theta_2$ . therefore, By equating the function of stage 1 and 2 and the phase  $\theta = \theta_1$  one gets

$$V_{A_{S1}}(\theta 1) = V_{A_{S2}}(\theta 1)$$
(24)

where  $\theta_1$  are

$$\theta_1 = -\angle IN + \arccos\left(\frac{V_{AC}\,\omega\,C_{in} - |IN|\,Iin}{|IN|\,Iin}\right) \quad (25)$$

The amplitude of the resonant current Iin can then be found by solving equation 24, as this is the current needed for the describing function a continuous waveform.

An FHA approach is used to convert these describing functions into the equivalent capacitor  $C_{eq}$  and resistor  $R_{eq}$  shown in Figure 3. To calculate these values, the first term in the Fourier series of the voltage  $V_A$  is used. The resistance can be calculated from

$$R_{eq} = \frac{a}{I_{in}} \tag{26}$$

And the capacitance is

$$C_{eq} = \frac{I_{in}}{\omega \cdot b} \tag{27}$$

Where a and b for a periodic signal are defined from Fourier analysis as

$$a = \frac{1}{\pi} \cdot \int_0^{2 \cdot \pi} V_A \cdot \sin(\theta) d\theta \tag{28}$$

$$b = \frac{1}{\pi} \cdot \int_0^{2 \cdot \pi} V_A \cdot \cos(\theta) d\theta \tag{29}$$

The resonant current and the equivalent resistor  $R_{eq}$  and capacitor  $C_{eq}$  are functions of the AC and switching frequency and therefore change across a mains cycle. Thus, in order to use the model, the amplitude of the resonant current, *Iin*, is calculated for each small step in voltage or frequency. In the next section the model for the Resistor  $R_{eq}$  and capacitor  $C_{eq}$ will be used to calculate a frequency control method.



Fig. 7. The equivalent resistor  $R_{eq}$  over frequency and AC voltage.



Fig. 8. The equivalent capacitor  $C_{eq}$  over frequency and AC voltage.

### **IV. FREQUENCY CONTROL**

The model developed in the previous section makes is possible to calculate the equivalent resistance  $R_{eq}$  and capacitance  $C_{eq}$  for a range of  $V_{AC}$  values. Figure 7 shows  $R_{eq}$  over partial ranges of  $V_{AC}$  and frequency.

 $R_{eq}$  drops when  $V_{AC}$  increases because more energy is passed into the charge pump capacitor  $C_{in}$ .  $R_{eq}$  also drops as frequency increases because the output power is constant and each switching cycle transfers a set amount of power. The equivalent capacitance  $C_{eq}$  is shown in Figure 8 and varies over the AC input voltage range. This is due to the capacitor  $C_{in}$  conducting current for a larger part of the period as the AC voltage increases. The change in  $C_{eq}$  with frequency is less pronounced.

When the equivalent resistance and capacitance are found, the resonant inductor  $L_{res}$  value can be calculated. Using this value allows the circuit to achieve the correct resonant current. The resonant inductor can be found from 30.

$$L_{res} = \frac{|I_{res}| + \sqrt{-C_{eq}^{2}R_{eq}^{2}\omega^{2}I_{res}^{2} + (V_{DC} \cdot \frac{2}{\pi})^{2}\omega^{2}C_{eq}^{2}}}{|I_{res}|\,\omega^{2}C_{eq}}$$
(30)

The inductance calculated across the AC voltages and frequencies are shown as contours in Figure 9. The inductance decreases with an increase in frequency, a common attribute of SMPSs. As the AC input voltage increases,  $C_{eq}$  increases and the inductance  $L_{res}$  drops. This demonstrates that single





Fig. 9. Calculated inductance values across frequency and AC voltage.



Fig. 10. Selected inductance value of 115 µH.

frequency operation is not suited for this topology as the inductance cannot easily be changed during operation.

In order to verify the results, a 115  $\mu$ H inductor was selected. The ideal frequency of operation for this inductor value is shown in Figure 10 against the input AC voltage. Remaining on this curve will ensure good PF and constant output power.

### V. SIMULATION

To verify the frequency control found from the FHA model, the circuit was simulated in LTspice with the control implemented as shown in Figure 11. The square wave signal for the half bridge is generated by a voltage controlled oscillator (VCO) in this case the LTC6990 from Linear Technologies. The VCO is controlled by a voltage source that tracks the ideal frequency for a given AC voltage as given in Figure 10.

The input voltage and currents generated by the simulation are compared to simulated operation at a fixed frequency (255



Fig. 11. Frequency control implementation in simulation.



Fig. 12. Simulated input voltage and current with and without frequency control.



Fig. 13. Average output power with and without frequency control.

kHz) and shown in Figure 12. Both cases are simulated with the same output power to enable a fair comparison. It can be seen that both input currents is in phase with the voltage. The current with control is close to sinusoidal which indicates that it has low harmonic content. The sinusoidal input current with control indicates than the control scheme works as intended. The input current for a fixed frequency has a discontinuity around the zero crossing which will result in high harmonic distortion.

The output power regulation of the circuit is improved by the proposed control arrangement. The output power was measured and low pass filtered to identify fluctuations over a mains cycle. The measured output power can be seen in Figure 13. The output power changes over a cycle for fixed frequency operation and stays more constant with control. The remaining variations in output power are likely due to FHA only considering the fundamental frequency.

### VI. IMPLEMENTATION

To verify the results from the simulation, a prototype was implemented. The half bridge is built with two IPD50R650CE MOSFETs from Infinion driven with a SI8244 gate driver, which has adjustable dead time to aid soft switching. The prototype was implemented using the same frequency control as the simulation here implemented as shown in Figure 14. To enable this control method, the AC mains voltage is measured before the input filter by an attenuating differential amplifier which drives a discrete analogue to digital converter. The digital output is fed through an ATMega microprocessor which makes the calculations and control the frequency using a



Fig. 15. Measured AC voltage and input current with and without control.

## LTC6990 VCO. The LTC6990 delivers a square wave signal with 50% duty.

As before, the converter was tested with frequency control and at fixed frequency. To get the desired output power, the control function used was for a slightly larger inductor value than used in simulation to account for losses in the system and the non-linearity of the inductor. The AC voltage and input current are shown in Figure 15. In both cases, the input current is in phase with the voltage. The current with frequency control resembles a sinusoidal waveform with few harmonics, where the input current for the fixed frequency test has a discontinuity around the zero crossing and a spike in current at the peak AC voltage. This spike is caused by the charge pump capacitor  $C_{in}$ not being sufficiently charged and discharged across a mains cycle. This results in the voltage across the DC capacitor,  $C_{DC}$ , dropping below the mains peak voltage and thereby making a direct path from the mains to the DC capacitor through the diodes. The PF and harmonics was measured with a N4L PPA5530 power analyser: the converter achieved a PF of 0.990 with frequency control and a PF of 0.955 with a fixed frequency. The measured harmonics with control together with the standard limits defined in IEC 61000-2-3 for Class-C equipment are shown in Figure 16. Measurements shows that the control method is working as intended lowering the harmonic content of the input current. The third harmonic is clearly the largest of the harmonics however well below the limit that is given by  $30 \cdot \lambda$  in % where  $\lambda$  is the power factor of the converter. The THD measured on the input current are 5.68% with control and 26.1% without control.

The harmonics for the fixed frequency are shown in Figure 16. Several of the harmonics are above the limits. The third harmonic only a little larger than with frequency control. However, the fifth, ninth, and thirteenth are above the limits. This is mainly due to the zero crossing discontinuity and the spike when the AC input voltage exceeds  $V_{DC}$ . The capacitor  $C_{in}$  could have been made bigger to accommodate the spike at additional expense and volume for the converter.

The output power was measured and low pass filtered as



Fig. 16. The measured harmonics of the converter with control at 110  ${\rm V}_{AC},$  together with the limits from IEC 61000-3-2



Fig. 17. Output power with and without control.

shown in Figure 17. Both the output power with control and at fixed frequency agree with the simulation. There is a third harmonic ripple seen on the output power with frequency control, however the control maintains a more flat output power. This third harmonic ripple on the output could originate from the same limitation with the FHA as the the third harmonic measured on the input current.

### VII. CONCLUSION

This paper has presented a model based on the first harmonic approach of a charge pump half bridge resonant converter. The model transforms the resonant tank network to a series-connected LCR network for frequency in a range of operating frequencies. The model is used to developed a frequency control methodology which is both simulated and implemented practically. The frequency control method proven to achieve a good power factor of 0.99 with frequency control. The frequency control also keeps the input harmonics well below the limits for class-C equipment while reducing ripple on the output power compared to fixed frequency operation.

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# EMC Investigation of a Very High Frequency Self-oscillating Resonant Power Converter

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# EMC Investigation of a Very High Frequency Self-oscillating Resonant Power Converter

Jeppe A. Pedersen\*, Arnold Knott\*, Michael A. E. Andersen\* \*Technical University of Denmark Richard Petersens Plads, building 325 2800 Kongens Lyngby Denmark

Email: {jarpe, akn, ma}@elektro.dtu.dk

Abstract—This paper focuses on the electromagnetic compatibility (EMC) performance of a Very High Frequency (VHF) converter and how to lower the emissions. To test the EMC performance a VHF converter is implemented with a Class-E inverter and a Class-DE rectifier. The converter is designed to deliver 3 W to a 60 V LED, it has a switching frequency of 37 MHz and achieves an efficiency of 80%. For an LED driver to be used on the consumer market it has to fulfil the standard regarding EMC emissions. The conducted emission is often used as a reason to increase the switching frequency to the VHF range to avoid the regulations. This converter shows to be well below the levels for conducted emission even without filtering. For the radiated emissions the converter is above the limits without input and output filters. Several designs with different ways to lower the emissions are implemented and the different layouts and filtering are compared and discussed.

### I. INTRODUCTION

In most Switch Mode Power Supplies (SMPS) the passive components set the limit for the minimum physical size. The passive components scale inversely with frequency and hence increasing the switching frequency reduces the physical size of the power supply. The switching frequency is typically limited to a few megahertz due to switching losses that increase linearly with frequency. In resonant converters that utilize soft switching the switching losses can be neglected. When increasing the switching frequency to the Very High Frequency (VHF) range (30 MHz - 300 MHz) resonant converters are used [1]-[5]. Converter operating in the VHF range often consists of an inverter and a rectifier. This paper describes the electromagnetic compatibility (EMC) performance of a DC-DC converter with a Class-E Inverter described in [6], [7] and with a Class-DE rectifier described in [8]-[12]. The converter is galvanic isolated by two resonant capacitors ( $C_{res1}$  and  $C_{res2}$ ) placed in series with the resonant inductor and in the ground return path separating the inverter from the rectifier. The schematic of the full converter is seen in Fig. 1. The converter uses a self-oscillating gate drive [13] shown in Fig. 2. This gate drive is also used for VHF converters in [14], [15].

VHF converters have been a hot topic in recent years and with the development of wide bandgap devices this field will grow. There has not been any documentation of soft switching VHF resonant converters EMC performance. Only the EMC performance of a hard switched VHF converter is described in [16]. This subject is of great importance for industrial applications since products must comply with the standard for EMC emissions both in radiated and conducted mode. The standard for conducted emissions stops at 30 MHz which makes VHF converter attractive since the switching frequency is no longer within the measured frequency range. The radiated emissions is measured from 30 MHz and up and the presented converter shows that the radiated emissions needs attention when designing VHF converters.

### II. THEORY

The converter described in this paper is made with a Class-E inverter and a Class-DE rectifier. When designing resonant converters the rectifier [11] is designed first. Then the inverter [14] is designed to match the input impedance of the rectifier. The load is a 60 V LED and due to the high output voltage a Class-DE rectifier is chosen since the peak voltage of the diode is equal to the output voltage. The design of a Class-DE rectifier is described in [11] and the input impedance of the Class-DE rectifier for D = 0.25 is:

$$Z_{IN} = \frac{1}{2 \cdot \pi} \cdot R_L \tag{1}$$

The design for the Class-E inverter is described in [14] where the circuit components needed to obtain zero voltage switch (ZVS) is found from the load impedance. Ideally the Class-E inverter and Class-DE rectifier have no rapid transients since they are soft switching. Soft switching is known to have less harmonic content at the switch node and hence better EMC performance [17].

In power electronics the current loops are kept small to avoid large magnetic fields on the PCB, it also ensures that the ground return inductance is kept as small as possible. Ground bounce can create common mode emissions because it has a capacitive coupling to other parts of the circuit. The impedance of the traces in the circuit is usually considered inductive [18] and therefore the impedance increase with frequency which again increases ground bounce. For the PCB itself to become a good antenna at a given frequency it has to be above a quarter of a wavelength and since the PCB is usually smaller than this within the VHF range it is the cables that contribute most to the radiation. One of the means to reduce the radiated emissions is to use an image plane as described in [19]. The image plane can be used to lower the impedance for traces in the circuit



Fig. 1. Schematic of the converter used in this paper, with a Class-E inverter and a Class-DE rectifier.



Fig. 2. Schematic of the gate drive with MOSFET parasitics.

and together with proper filtering it can create a low impedance return path. If the PCB layout is not enough to suppress the emissions input and output filtering can be implemented on the PCB. Filtering can be used to create a low impedance path for differential and common mode signals and a high impedance path to the cables ensuring that the high frequency signals stays within the PCB.

### **III. IMPLEMENTED CONVERTERS**

The converter used in this paper is designed to deliver 3 W for a 60 V LED with a switching frequency of 37 MHz and the input voltage is 30 V DC. The component list is found in Table II. The MOSFET used in this design is a IRF5802. This is a 150 V device and was chosen due to its low parasitic capacitances. The diodes used in the rectifier is a MBR0560 which is a 60 V schottky diode. The converter is achieving an efficiency of 80% at 30 V input.

Different versions of the converter are implemented as shown in Fig. 3 to test the EMC performance of different layouts. The PCBs are made with different input and output orientation on the PCB, converter A-C is made with input and

TABLE I. COMPONENT VALUES FOR THE VHF CONVERTER.

Component	Value
$C_{IN}$	1 µF
LIN	1 µH
$C_{S1}$	18 pF
$C_{RES1}$	100 pF
$C_{RES2}$	4.7 nF
$L_{RES}$	1.2 µH
$C_{D1}$	7 pF
$C_{D2}$	7 pF
Cout	1 μF
$L_G$	82 nH
$C_G$	33 pF



Fig. 3. Picture of the converters labeled from A-I.



Fig. 4. PCB layout with small traces.

output is in each end of the PCB and converter D-I are made with input and output close together on one side of the PCB. Converter B-C and F-I is made with image plane. Input and output filters are implemented on H-I and in addition to this I is implemented with an EMC shield connected to the image plane.

There is also made a comparison between having narrow traces between the components as shown in Fig. 4 and having polygons fill up the PCB with copper as shown in Fig. 5. The PCBs with small traces will add inductance to the wires and this increases ground bounce and can create resonances in the circuit. The PCB with large polygon traces will have less inductance in the traces and better thermal cooling of the components as the copper helps spread the heat. However due to the larger copper planes the capacitive coupling within the circuits and to the surroundings increases.

The converters H and I have an input and output filter which is shown in Fig. 6, the filters is connected on both the input and output to minimize the emissions from the board. The filter is made with 1008AF inductors from Coilcraft and capacitors with the values shown in table II. The two inductors is placed to filter both common mode and differential mode signals. The capacitors  $C_{f1}$  and  $C_{f6}$  are only filtering differential mode signals,  $C_{f6}$  is also shown in Fig. 1 as the input  $(C_{IN})$  and output  $(C_{OUT})$  capacitors. The capacitors



Fig. 5. PCB layout with large copper polygons.



Fig. 6. Schematic of the filter used, the  $V_{IN-OUT}$  is placed at the input and output of the VHF converter.

 $C_{f2}$ - $C_{f5}$  are connected to the image plane to filter the common mode signals. By connecting them to the image plane they create a low impedance path for the signals at high frequencies. In this way the signals is kept within the PCB and hereby minimise the emissions. For the last converter I the EMC shield is also connected to the image plane with vias all around the edge of the shield.

### IV. EMC PERFORMANCE

The converter implemented is designed for an LED therefore the Cispr 15 standard should be followed. This standard however refers to the limits from Cispr 22 (EN 55022) so these limits are used in this paper. One of the reasons for increasing the frequency into the VHF range is to avoid the conducted EMC requirements that only goes to 30 MHz. Conducted measurements using a LISN network have been made on the converters and the results without filter is shown in Fig. 7. It is clear from the measurements that the noise floor is increased at the lower frequencies. This is caused by the self-oscillating gate drive drifting a little up and down in frequency. The measurement indicates that the conducted emission is not an issue for VHF converters.

The radiated emissions is more interesting and radiated measurements have been made inside an EMC chamber with an antenna placed 3 m from the converter. The chamber and

TABLE II. COMPONENT VALUES FOR THE INPUT AND OUTPUT FILTER.

Component	Value	Туре
$L_{f1}$	3.3 µH	Ferrite
$L_{f2}$	3.3 µH	Ferrite
$C_{f1}$	1 µF	X5R
$C_{f2}$	680 pF	C0G
$C_{f3}$	680 pF	C0G
$C_{f4}$	680 pF	C0G
$C_{f5}$	680 pF	C0G
$C_{f6}$	1 µF	X5R



(a) Conducted emission reference.



(b) Conducted emission of a converter without filter (converter E).

Fig. 7. Conducted measurements with limits from EN 55022 (blue is peak and green is average).

antenna is not fully calibrated however it can be used to compare the performance of different layouts. All measurements are done with the same setup and at same voltages. A reference measurement is shown in Fig. 8(a) and is compared to the basic converter A that is expected to have the highest emission. The measurement of converter A is shown in Fig. 8(b). The converter is clearly radiating at the fundamental and all the harmonic frequencies. The drain voltage in this converter is going from 0 V to a peak voltage of  $V_{DSpeak} = 3.6 \cdot V_{in} = 108$ V in a quarter of a period which at 37 MHz is 6.75 ns. This results in a high  $\frac{\delta V}{\delta t}$  which can generates high radiated emissions if not filtered proberly.

As mentioned before an image plane is one of the methods used to reduce radiated emissions. Two identical boards one with and one without an image plane is tested. The image plane is connected to ground on the primary side with a via placed next to the input connector. As seen in Fig. 9 the image plane is damping the radiated emissions as expected, the only filter components used in this setup is the input and output capacitors  $C_{IN}$  and  $C_{OUT}$  so some radiation is expected. It seems that the image plane is working well and reduces the





(b) Radiated emmissions, the converter has input and output in each end of the PCB and no image plane (converter A).

### emissions.

The standard recommendation is to place the input and output in the same side of the PCB. The measurements on two converters with different placement of input and output are shown in Fig. 10. It is clear from the measurement that having the input and output next to each other helps lowering the emissions. In this case it keeps the current loop smaller in the power stage which seems to have a positive effect on the fundamental and second harmonic.

The two types of trace layouts shown in Fig. 4 and 5 is measured. First on converter D and E that is both implemented without an image plane, the results are shown in Fig. 11. Here there is only a small difference between the two PCB layouts. Only at frequencies above 400 MHz the polygons are performing better which indicates that it lowers the trace inductance. The same test was performed on two PCB's implemented with an image plane. The emissions from the PCB with thin traces (converter F) is shown in Fig. 10(b) and the emissions with large polygons (converter G) is shown in Fig.



(a) Radiated emissions, the converter has input and output in the same end of the PCB and no image plane (converter E).



(b) Radiated emissions, the converter has input and output in the same end of the PCB and an image plane (converter G).

Fig. 9. Radiated emissions measured on converters with and without image plane.

9(b). The polygon implementation seems to lower inductance in the traces thereby reducing the radiated emissions when there is an image plane. Because of the better performance all the converters with additional filtering have been implemented with polygon traces. Placing two large copper areas closely above each other can add capacitance to the circuit. This is not considered a problem in this implementation as the areas are relatively small.

Measurement was performed on a converter with filters on the input and output this is shown in Fig. 12(a). The filters placed on the input and output of the converter is reducing the radiated emission at the high frequencies. However there is still much harmonic content at the frequencies below 400 MHz. In figure 12(b) the measurements on a converter with the same filters and an EMC shield is shown. The EMC shield is surrounding the converter to minimize the capacitive coupling to the cables and surroundings. Adding the EMC

Fig. 8. Radiated emmisions reference and basic converter.



(a) Radiated emmissions, the converter has input and output in each end of the PCB and an image plane (converter B).



(b) Radiated emmissions, the converter has input and output in the same end of the PCB and an image plane(converter F).

Fig. 10. Radiated emmisions for converters with different input and output layout.

shield reduces the radiated emissions significant and only the fundamental and first harmonics are present. By adding the EMC shield the capacitive coupling across the filter is limited and most of the radiated emissions are eliminated.

To summarize the EMC performance of this VHF converter seems to have no problems with the conducted EMC, and therefore the main focus is on the radiated emissions. As for the radiated part the converter has a high level of radiation if left without any filtering besides the input and output capacitor. By implementing the image plane the emissions are lowered. Placing the input and output connecters on the same side also helps reducing the emissions. The polygon layout on the PCB seems to have a positive effect together with an image plane. By adding additional filtering on the input and output the emissions are reduced further. The EMC shield prevents the electric field from coupling across the filters.



(a) Radiated emmisions, the converter has input and output in the same end of the PCB, no image plane and the thin traces (converter D).



(b) Radiated emmissions, the converter has input and output in the same end of the PCB, no image plane and polygon traces (converter E).

Fig. 11. Radiated emmisions for thin vs polygons traces and no image plane.)

### V. CONCLUSION

This paper describes a VHF converter implemented with different layouts to investigate the EMC challenges when increasing the switching frequency to the VHF range. The converter has a switching frequency of 37 MHz and an efficiency of 80%. The conducted EMC test shows that the converter has no problem in the frequency range from 150 kHz to 30 MHz. The challenge with VHF converters is to lower the radiated emissions. This paper shows that the image plane can be used to reduce the radiated emission to some extent and filtering and proper shielding can be used to lower the emissions.

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(a) Radiated emmisions, the converter has input and output in the same end of the PCB, no image plane, polygon traces and filters on the input and output (converter H).



(b) Radiated emmisions, the converter has input and output in the same end of the PCB, no image plane, polygon traces, filters on the input and output and an EMC sield (converter I).

Fig. 12. Radiated emmisions for converters with filters, and with and without EMC shield.

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Technical University of Denmark Department of Electrical Engineering Elektrovej building 325 DK-2800 Kgs. Lyngby Denmark Tel: (+45) 45 25 38 00 Fax: (+45) 45 88 01 17 Email: hw@elektro.dtu.dk