ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUPHA117

UPGRADE OF THE LLRF CONTROL SYSTEM AT LNL

D. Bortolato*, S. Pavinato, INFN, Laboratori Nazionali di Legnaro, Legnaro,Italy
M. Bellato[2], F. Gelain[1], R. Isocrate[2], D. Marcato[1], E. Munaron[1], D. Pedretti[1]
[1]INFN, Laboratori Nazionali di Legnaro, Legnaro,Italy
[2]INFN, Sezione di Padova, Padova, Italy

Abstract

For the SPES project at Legnaro National Laboratories (LNL), a Low-Level Radio Frequency (LLRF) has been designed to have flexibility, reusability and an high precision. It is an FPGA-based digital feedback control systemusing RF ADCs for the direct undersampling and it can control at the same time eight different cavities. The LLRF system was tested on the field with an accelerated beam. In the last year some improvements on the firmware, software and hardware of the control system have been done. In this paper the results carried out in the more recent tests, the future works and the upgrades of the system will be detailed.

INTRODUCTION

SPES (Selective Production of Exotic Species) [1] is a new facility under construction at LNL. The main goal is the production of neutron-rich exotic beams to perform research in nuclear structure and in interdisciplinary fields like medical and biological. Then the Radioactive Ion Beam (RIB) from SPES can be boost through the linear accelerator ALPI [2] and sent to the three experimental halls. Some upgrades which would make ALPI suitable as an RIB accelerator are in commissioning [3]. ALPI is a superconducting linear formed by 96 QWR cavities. The first group of cavities resonate at 80 MHz, while that of a second group resonate at 160 MHz. In order to boost also the RIB coming from SPES, ALPI must be modernized. Besides the resonators themselves, all their ancillary components need to be modernized: RF controllers, RF control system, RF power amplifiers, and couplers, pickup and tuners. The RF control system upgrade are here detailed. In particular this paper is focused on the digitalization of the signals, how this process is related to the control performance and on the firmware/software modifications done during the last year.

RF CONTROLLER

Each RF controller [4], [5] controls up to eight cavities. The RF signals picked-up from the cavities are undersampled by RF ADCs. The digitized signals are elaborated by a field programmable gate array (FPGA) which implements a proportional-integral controller. The signals processed by the FPGA are up-converted by DACs, hence the harmonic of interest is filtered-out and sent to power amplifiers and then to the cavities.

A block diagram of the LLRF controller for the cavities is shown in Fig. 1. It is based essentially on three boards:

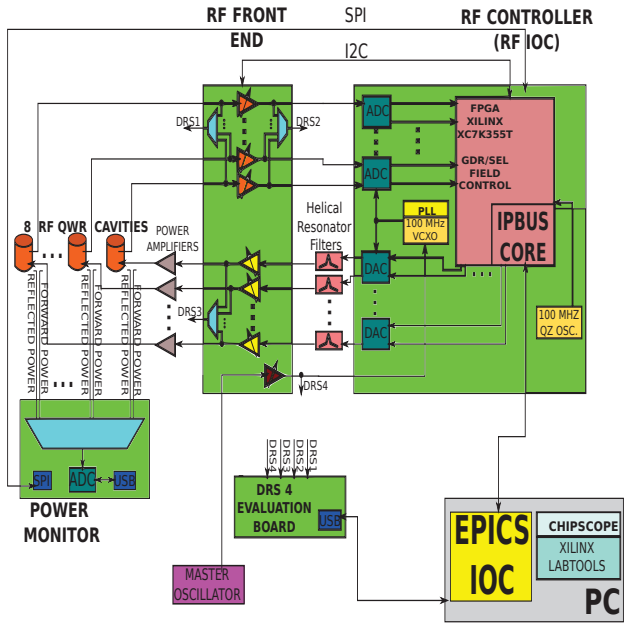

Figure 1: Block diagram of the LLRF system

the RF input-output controller (RF IOC), the RF front end (RFFE) and the power monitor (PM) [4]. The RF IOC implement the control law. The RFFE board adapts the amplitude level of the RF signals from the cavities to the ADCs of the RF IOC and from the DACs of the RF IOC to the power amplifiers. The PM board measures the reflected powers and the forward powers of the eight controlled cavities.

One of the most critical point next analyzed is the digitalization of the signals.

ADC

In order to simplify the hardware design the direct down conversion(DDC) was adopted. The signals picked up from cavities have frequencies that lie in the second or third Nyquist zone. DDC preserves the signal information if the sampling frequency is at least double the bandwidth of the RF signals [6]. This condition is complied. Furthermore the RF signals are sampling in quadrature in order to extract the in-phase and quadrature components. From these components it is direct get the amplitude and phase of the field resonating in cavities. The components are physical meaningful and can be controlled independently.

ADCs have to guarantee an high resolution and an high sampling rate. The sampling rate is important since the DDC was chosen, while the high resolution is related to the stability of phase and amplitude in cavity. For a mod-

* bortolato@lnl.infn.it

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUPHA117

ern heavy ion linac like ALPI, it is required a phase stability and a amplitude stability of at least 0.5° and 0.5% rms, respectively. In other words the phase and gradient stability can be studied from the phase error and amplitude error. From these values we can extract the ADC specification for signal-to-noise ratio (SNR) [7]. According with the amplitude error the SNR is:

$$SNR_{Mag} = -20 * \log(Err_{\text{MAGNITUDE}}) \quad (1)$$

while according with the phase error the SNR is:

$$SNR_{Ph} = -20 * \log(\sin(45° + Err_{\text{PHASE}}) - \cos(45°)) \quad (2)$$

To calculate the SNR due to the phase error, we need to solve the amplitude difference between the in-phase I and quadrature components Q. The worst case is when the magnitude of I is equal to the magnitude of Q, in example at 45° [7]. The SNR requirement has to be kept in the whole gradient dynamic range $|E_{MIN}| \rightarrow |E_{MAX}|$, that in ALPI typical configurations is $|E_{MIN}| = 3.5$ MV/m in a low beta cavity and $|E_{MAX}| = 5$MV/m in a medium beta cavity. Hence the ADC must have a SNR_{ADC} greater than:

$$SNR_{ADC} \geq \max(SNR_{Mag}, SNR_{Ph}) + 20 * \log\left(\frac{|E_{MAX}|}{|E_{MIN}|}\right) \quad (3)$$

where $20 * \log(|E_{MAX}/|E_{MIN}|) \approx 3dB$.

A gradient stability of 0.5% rms means a $SNR = -20\log(0.005) = 46dB$. Whereas a phase requirement of 0.5° implicates a $SNR = -20 * \log(sin(45 + 0.5) - cos(45)) = 44.2dB$. The SNR of an ideal ADC is given by the following equation:

$$SNR_{ADC} = 6.02 * N + 1.76 \quad (4)$$

This means that the ADCs have to have at least an equivalent number of bit equals to $ENOB = (SNR_{ADC} - 1.76)/6.02 = 7.9 \rightarrow 8$, with $SNR_{ADC} = 46 + 3 = 49$ dB.

SLOW CONTROL

The slow control system refers to the different communication protocols and associated firmware or software, needed to monitor and control the electronic programmable devices present in the RF controller. In this project the FPGA, housed in the RF IOC, communicates with a remote or local host using standard hardware such as USB or Ethernet. The communications are used for monitoring or communication with the accelerator control systems. A communication controller in the FPGA and a driver in the host exchange data with the USB or Ethernet communication link.

In the RF IOC there are two different slow control system communication link.

- The first one is based on a USB communication link. The serial link in the board is formed by the chain usb-connector, CYUSB3014 and some GPIO in the FPGA, that implements inside it a usb core block. The core acts as a USB device that transfer a byte stream in both direction over the bus. CYUSB3014 is a super-speed peripheral controller, providing integrated and flexible features. It has a fully configurable, parallel, general programmable interface, which can connect to an FPGA. Basically it is a programmable state machine that enables a flexible interface that may function either as a master.
- Instead of the other one the communication link is a Gigabit Ethernet. The communication is based on IP-bus protocol [8]. On the board there is a specific bidirectional high-speed serial link in the QSFP connector, linked to a GTX transceiver in the FPGA. Since the communication link is a Ethernet cable, a 1000BASE-T COPPER SFP Optical Transceiver is used with the QSFP connector.

IPbus allows the communication between the RF controller and the accelerator control system, without placing a computer, where an EPICS IOC can run, close to the controller. The software IOC is executed on a virtual machine. In this way you can exploit the advantages given by a virtual machines, constantly backed-up and easy to maintain, and reduce the wiring required. Therefore the communication via IPBUS was preferred on USB one. In spite of the USB communication has been used for the first test, IPBUS protocol is going to be used in the stable version of the control system.

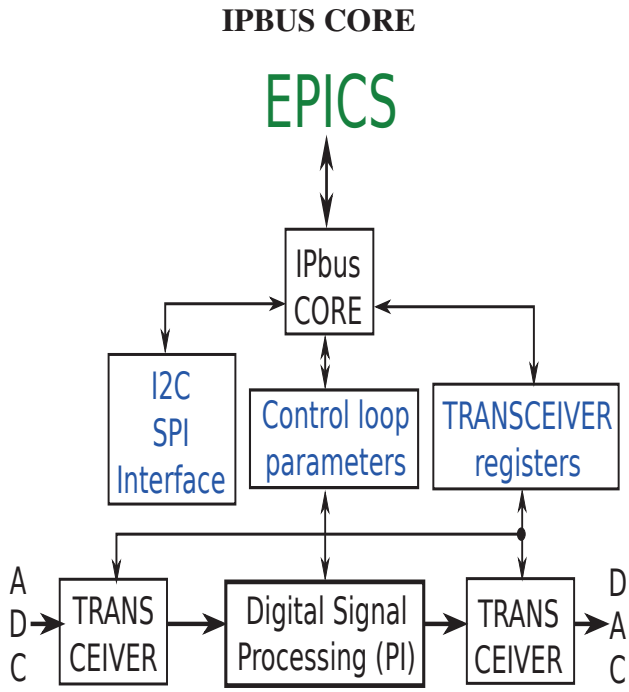

Figure 2: Block diagram of the firmware implemented.

The IPbus protocol allows to control hardware through a virtual bus. This bus has 32 bits address and 32 bits data. It uses standard IP based on gigabit ethernet connection. It

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUPHA117

is the interface between the RF IOC and the IOC EPICS based, that allows to set and get registers implemented in the FPGA firmware. The IPbus protocol belong to the application layer in the OSI model. Each IPbus host device (in this project the RF IOC board) has an IP address and a port number where it accepts IPbus control packets. The IPbus firmware suite was downloaded from the CERN repository `https://svnweb.cern.ch/trac/cactus`.

The registers are the so called "Configuration registers", "control loop registers" and "transceiver registers" as shown in Fig. 2.

Registers

The FPGA firmware [9] implements a set of control and status registers, through which the accelerator control system, via IPbus protocol, can set the amplitude and phase loop parameters and the configuration parameters for the ICs on the RF IOC, RFFE and PM boards. These registers in Fig. 2 are labeled as "Configuration registers" and "control loop registers". The latter is devoted for the configuration parameters and amplitude/phase loop parameters respectively. Actually it is formed by eight blocks of registers: one block for each cavity controlled. These registers, in the IPbus philosophy, are the slave blocks.

The "Configuration registers" are used to configure the ICs on the RF IOC, RFFE and PM board. Furthermore they read the digitized values of RF power from the PM board. These ICs implement an SPI or IIC interface in order to access their registers. From the perspective of the accelerator control system the SPI or IIC interface is totally transparent and the access to the ICs internal registers is done via read or write IPbus commands. Both protocols have a master-slave architecture with a single master. The master device originates the frame for reading and writing. In this case the master device is the FPGA, while the slaves are the ICs listed before. The lowest-level read and write functions to the memory-mapped registers, implemented in the FPGA, are based on the read and write function respectively, provided by the μHAL [8]. This is a C++ library that is a component of the IPbus suite, too.

MEASUREMENT

After having developed the FPGA firmware and the IOC EPICS, it was possible configure the boards. When the EPICS architecture to control the RF controller was completed rf control system validation started. It consisted in the installation of the new RF controller with its control system EPICS based in the ALPI facility. The cavities were SEL locked and a beam was accelerated. The stability of the LLRF controller was assessed. Suitable indicators for validate the stability performance are the rms value of the residual errors, in phase and magnitude, of the RF IOC board. A good visualization of the different perturbation frequency is achieved calculating the integrated rms detuning spectrum [10], [11]:

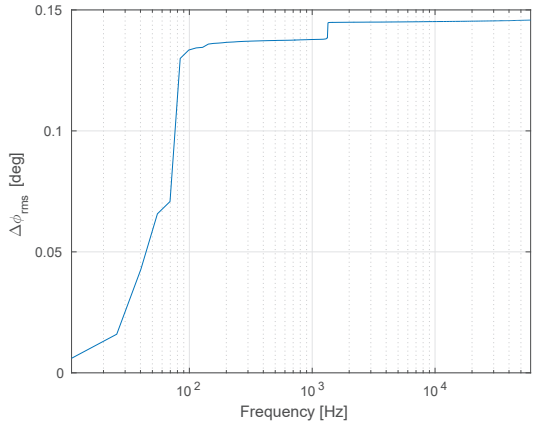

Figure 3: Cumulative spectrum of the phase error for a low beta cavity SEL driven.

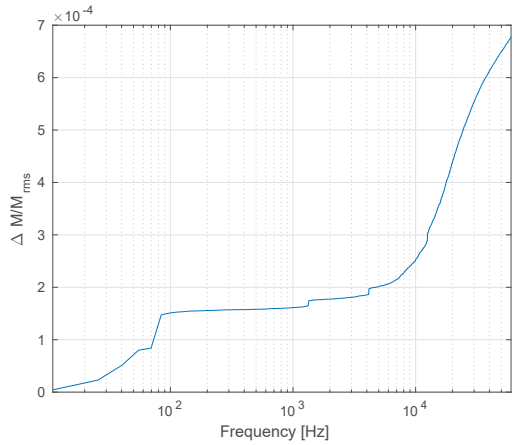

Figure 4: Cumulative spectrum of the amplitude error for a low beta cavity SEL driven.

$$\Delta d(f_n)_{rms} = \frac{\sqrt{\sum_1^n |\mathcal{F}[\Delta d(t)]_i|^2}}{\sqrt{2}} \qquad (5)$$

where $\mathcal{F}[\Delta d(f_n)_{rms}]$ represents the spectrum of the time series collected. It is gotten accumulating up to the perturbation frequency f_n, the absolute value squared of the Fourier components $\mathcal{F}[\Delta d(t)]_i$.

Figure 3 shows the integrated phase error for a low beta cavity. This graph shows the effect of the disturbances at microphonic frequencies.

Instead of in the graph of the integrated field error Fig. 4, there is a source of noticeable amplitude error around the 10 KHz. At the moment it is unknown the source of this disturbance.

From Fig. 3 and 4, it appears that the total value of the phase fluctuation is 0.145° rms, while for the field fluctuation is $6.9 \cdot 10^{-4}$.

Substituting in equation 1 $Err_{\text{MAGNITUDE}} = 6.9 \cdot 10^{-4}$ and in equation 2 $Err_{\text{PHASE}} = 0.145$ and finally applying

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUPHA117

the equation 3 the SNR estimated is:

$$SNR_{ADC} = \max(63.22, 55.0) + 20 * \log(\frac{5}{3.5}) \approx 66dB \quad (6)$$

Making the assumption of chapter the ENOB is calculated as:

$$ENOB = \frac{SNR_{ADC} - 1.76}{6.02} = 10.7 \quad (7)$$

This value is better than the ENOB requirements.

CONCLUSION

The measurements show that the new RF system guarantees a phase and an amplitude stability margins consistent with those required for a heavy ion linear accelerator as ALPI.

The measurements done to qualify RF control system have been come to an end. The hardware developed is now ready for the first production in order to substitute the old analog controllers.

REFERENCES

[1] G. Prete et al., *Status of the SPES Facility for Acceleration of High Intensity Protons and Production of Exotic Beams*, EPJ Web of Conferences 66, 11003 (2014).

[2] A. Dainelli et al., *Commissioning of the ALPI post-accelerator*, Nucl. Instr. and Meth A 382 (1996) 100-106.

[3] G. Bisoffi et al., *ALPI Setup as the SPES Accelerator of Exotic Beams*, EPJ Web of Conferences 66 , 11003 (2014).

[4] D. Bortolato et al., *New LLRF control system at LNL*, Proceedings of Real Time Conference (RT), 2016 IEEE-NPSS.

[5] S. Pavinato et al., *Development of a digital LLRF control system at LNL*, Proceedings of LINAC Conference, 2016.

[6] Walt Kester, Editor with the technical staff of Analog Devices, *Data Conversion Handbook*.

[7] C. Hovater, et al. *Direct Digital Down/Up Conversion for RF Control of Accelerating Cavities*

[8] Tom Williams for the CMS Collaboration, *IPbus A flexible Ethernet-based control system for xTCA hardware*, CMS Conference Report -2014/334.

[9] *Notes on Firmware Implementation of an IPbus SoC Bus*, V1.0 23/5/2012, DMN.

[10] A. Neumann et al., *Analysis and active compensation of microphonics in continuous wave narrow-bandwidth superconducting cavities*, Physical Review Special Topics - Accelerators and Beams 13, 082001 (2010).

[11] M. Konrad, *A Development and commissioning of a digital rf control system for the S-DALINAC and migration of the accelerator control system to an EPICS-based system*, PhD Thesis, 2013.