Simulations and comparisons of basic analog and digital circuit blocks employing Tunnel FETs and conventional FinFETs

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INTRODUCTION — In the past decade the Tunnel Field Effect Transistor (TFET) relying on band-to-band tunneling (BTBT) has emerged as one of the most promising small slope FETs able to achieve a subthreshold swing (SS) below the room temperature 60 mV/dec limit of conventional MOSFET [1]. Many simulation studies attributed to TFETs the potential to outperform conventional MOSFETs in the ultra-low voltage domain (V_{DD} < 0.4 V) in both analog [2-3] and digital [4-7] applications. However, only basic digital and analog circuits have been fabricated up to date, such as current mirrors [8] and inverter gates [9]. As for semiconductor materials, III-V hetero-structure TFETs may be able to achieve a sub-thermal SS in a wide current range and, at the same time, very competitive on currents [1], as demonstrated by a recently fabricated vertical InAs/GaAsSb/GaSb nanowire *n*-type TFETs [10].

The aim of this work is to benchmark a complementary III-V TFET technology platform against the mainstream FinFET reference, by considering basic building blocks of digital and analog applications. To this purpose, we selected a complementary III-V TFET technology platform designed and optimized using full quantum simulations in [11], where *n*- and *p*-type TFET pairs are realized in the same InAs/AlGaSb material system. The use of such devices allowed us to remove the excessively optimistic assumption of perfectly symmetric *n*- and *p*-type TFETs, very frequently embraced in previous simulation studies (e.g. in [2, 7]). We present circuit-level simulations performed on current mirrors and inverter-based logic blocks, which are identified as basic topologies representative of the analog and digital design realms, respectively. Similar benchmarking results for the same technology platforms have been obtained by focusing the comparison on more complicated circuit blocks [3], [5] and [6].

METHODOLOGY — From a methodological standpoint, we have used the *Synopsys Sentaurus TCAD* tools [12] to simulate the III-V TFETs, after an extensive calibration of the TCAD models against the full quantum simulations in [11] (details about the TCAD deck calibration are reported in [6]). Then we generated look-up-tables (LUTs) for the I_D, C_{GS}, and C_{GD} characteristics versus V_{GS} and V_{DS} of the TFETs and imported them in the *Cadence Virtuoso* environment by means of Verilog-A models, thus eventually enabling full circuit-level simulations.

DEVICES — The geometric structures of the *p*/*n*-type TFETs and FinFETs considered in this work are shown in Fig.1. In particular, the AlGaSb/InAs nanowires (NWs) TFETs have a square cross section with a side, L_S, of 7 nm, a gate length, L_G, of 20 nm and equivalent oxide thickness, EOT, of 1 nm. The benchmarking FinFET technology was obtained via the predictive-technology-models (PTM) for 10 nm node FinFETs, designed and optimized in [13] and available at [14], where FinFETs have fin height (h_{fin}) of 21 nm, fin width (t_{fin}) of 9 nm, L_G of 14 nm and EOT of 0.88 nm. Despite the different geometry, the benchmark is fair since the two architectures have almost the same area under the assumption of having vertical TFET nanowires (e.g. see [10]) and conventional lateral FinFETs. The I_D-V_{GS} characteristics of the devices are shown in Fig. 2 (top). The comparison is performed by aligning both *n*- and *p*-type TFETs transfer-characteristics at the same off-current (I_{OFF} ~ 2 pA) as the FinFET counterparts for $|V_{DS}| = 0.3$ V. This ensures very similar static power when the same circuit design is implemented with TFETs or with FinFETs. Note that, while the I_D-V_{GS} characteristics of *p*- and *n*-type FinFET are essentially symmetric, the ones of TFETs are strongly asymmetric: for example the *p*-type TFET has four times smaller on-current compared to the one of the *n*-type, moreover, the *n*-TFET suffers from a larger ambipolarity compared to the *p*-TFET. In Fig.2 (bottom) the I_D-V_{DS} characteristics of the devices are compared showing that both *p*/*n*-type TFETs have better saturation behavior compared to the FinFETs, while the current conduction in TFETs is essentially unidirectional.

CURRENT MIRRORS — One key requirement for FETs for most analog applications is a large output resistance in saturation. As regards the current mirrors, a high output resistance enables an almost constant output

current in a wide range of load conditions. Fig.3 (top) shows the three current mirror circuits considered in this work, consisting in the simple, cascode and high compliance current mirror topologies, which have been compared considering a reference current (I_{REF}) of 100 nA. In [8], the reported experimental comparison of TFET and FinFET current mirrors revealed a similar sensitivity of the output current (I_{OUT}) to channel width variations, but a much smaller I_{OUT} dependence on the channel length for the TFET compared to the FinFET implementation. This is also highlighted by the results depicted in Fig.4, where it is clear that in the simple current mirrors with *n*- and *p*-type FinFETs it is not trivial to keep the output current close to the target, due to the remarkable sensitivity to V_{OUT}. For the same reason, the FinFET cascode solution requires to be operated at a relatively high minimum output drain voltage (V_{OUTmin} around 0.35 V and 0.4 V for the *n*-FinFET and *p*-FinFET respectively) compared to the TFETs counterpart. That is why a more complicated high-compliance topology is required in a FinFET design to compete with the simple TFET implementation, resulting in an increased circuit complexity also due to the need for additional biasing circuitry. On the contrary, simple current mirrors implemented with TFET show a performance comparable to the FinFET high-compliance topology in terms of I_{OUT}/I_{REF} as a function of V_{OUT} (with V_{OUTmin} around 0.1 V and 0.2 V for *n*-type and *p*-type devices, respectively), essentially because of the higher output resistance also shown in Fig.2 (bottom). As regards TFETs, when comparing the cascode current mirror with the simplest implementation, there is a relatively small improvement in terms of how close to 1 the I_{OUT}/I_{REF} ratio can be maintained, but we have to cope with a slight increase in the V_{OUTmin}, which can be ascribed to the poor TFET drain current saturation at low V_{DS} (see again Fig.2), whose implications are exacerbated in topologies with two or more TFETs stacked in series. These results suggest that TFETs have the ability to implement current mirrors that, for a given performance target, use simpler topologies and thus fewer transistors compared to FinFETs.

INVERTERS — As regards the logic circuits, minimum size inverter-based blocks have been considered for both TFETs and FinFETs, namely the fan-out 4 inverters (FO4) sketched in Fig.3d, and the 5-stage ring-oscillator (5RO) in Fig.3e. In the FO4, one single inverter is loaded by four equal stages and driven with nearly ideal square waveforms with negligible rise and fall times. Low-to-high (L→H) and high-to-low (H→L) delays are plotted for different V_{DD} in Fig.5. Unlike FinFETs, which are essentially symmetric, asymmetric electrical characteristics of TFETs result in an asymmetric FO4 rise and fall transitions. Despite such asymmetry, the TFET FO4 is shorter than the FinFET counterpart for V_{DD} below ~370 mV (~410 mV) if we consider the rise time (fall time). As regards the ring-oscillator, we have extracted the oscillation frequency (T_{osc}^{-1}) and the energy per cycle. T_{osc} is generally correlated with the critical path delay of a generic logic circuit, representing a limit for its maximum operating frequency, whereas the energy per cycle is in turn correlated with the energy per operation when the same digital circuit is operated at the maximum frequency. In Fig.6, energy versus T_{osc} points, extracted for various V_{DD} in the range 200~600 mV (step 100 mV), are plotted for both TFET and FinFET ring-oscillators, showing that for time-relaxed applications, the TFETs offer an energy budget saving, which in this case occurs for $T_{osc} > 1.5$ ns and for energy below 100 aJ/cycle.

CONCLUSIONS — In this paper we have compared the potentialities of two virtual complementary platforms in the ultralow voltage regime. Our results suggest that TFETs enable the use of simpler and thus more area effective circuit schemes compared to FinFET for some analog applications and that, despite the asymmetric characteristics of *n*- and *p*-type TFETs, these devices may offer energy saving for low to moderate frequencies digital applications.

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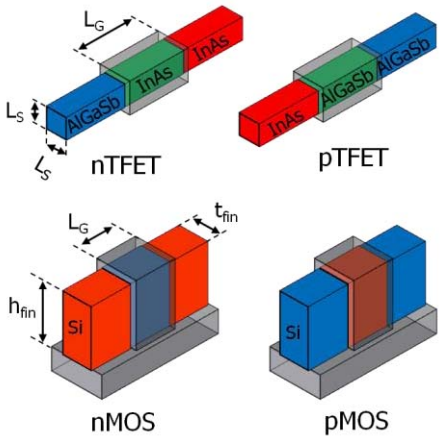

Figure 1. *n*- and *p*-type TFET and FinFET device architectures (as in [6]). Red and blue colors indicate the n- and p-doping types, respectively (green: intrinsic semiconductor, transparent-grey: oxide). TFET dimensions are: L_G = 20 nm, L_S = 7 nm, EOT = 1 nm [11]. FinFET dimensions are: L_G = 14 nm, t_{fin} = 9 nm, h_{fin} = 21 nm, EOT = 0.88 nm. [14]

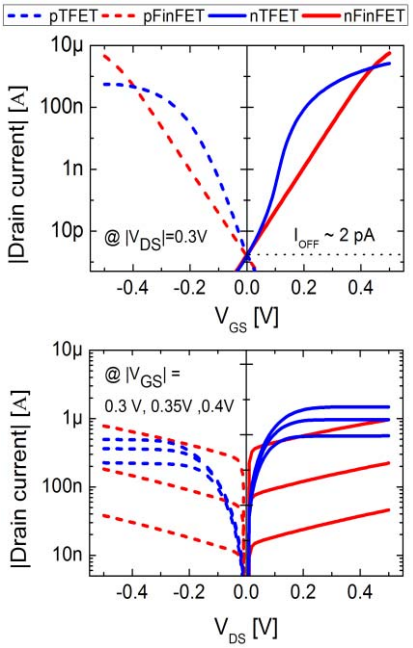

Figure 2. I_D-V_{GS} (**top**) and I_D-V_{DS} (**bottom**) characteristics for p/n-type TFET and FinFET devices, aligned at the same absolute I_{OFF} at |V_{DS}|=0.3 V.

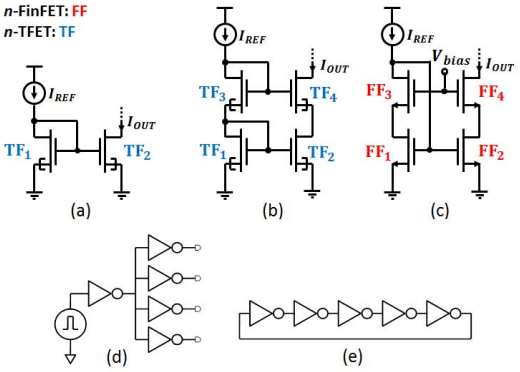

Figure 3. **Top**: Simulated current mirror circuits: (a) simple, (b) cascade and (c) high-compliance topologies. **Bottom**: (d) Simulated fan-out 4 inverters (FO4) and (e) 5-stages ring-oscillator (5RO).

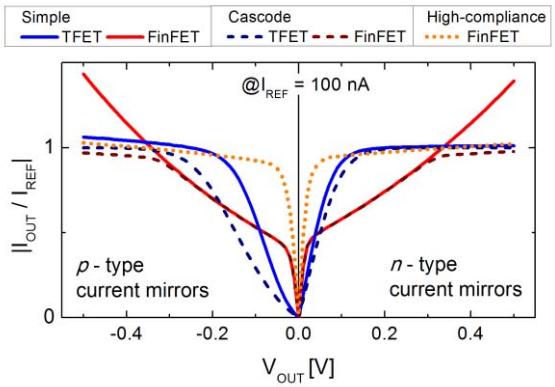

Figure 4. Simulated I_{OUT}/I_{REF} for the *p*- and *n*-type TFET current mirrors compared to different FinFET current mirror topologies. The circuits are compared considering the same reference current of 100 nA.

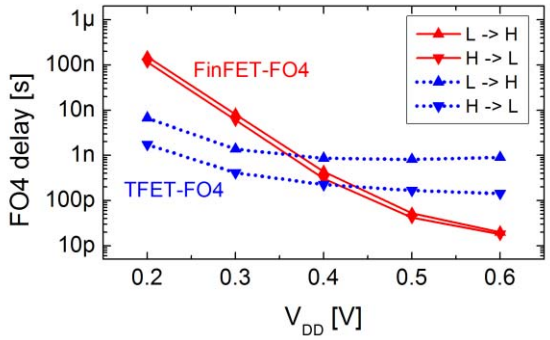

Figure 5. TFET and FinFET Fan-Out 4 (FO4) minimum-size inverters: low-to-high (L⟶H) and high-to-low (H⟶L) delays as a function of V_{DD}.

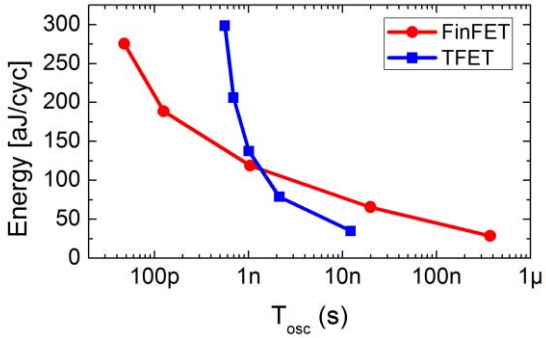

Figure 6. TFET versus FinFET benchmark based on the energy per cycle versus T_{osc} plot for minimum size 5-stages Ring Oscillators. The single points on the curves are obtained for different V_{DD}s (step of 100 mV).