

An Inductor Emulator Approach to Peak Current Mode Control in a 4-Phase Buck Regulator

by

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ABSTRACT

High-efficiency DC-DC converters make up one of the important blocks of state-of-the-art power supplies. The trend toward high level of transistor integration has caused load current demands to grow significantly. Supplying high output current and minimizing output current ripple has been a driving force behind the evolution of Multi-phase topologies. Ability to supply large output current with improved efficiency, reduction in the size of filter components, improved transient response make multi-phase topologies a preferred choice for low voltage-high current applications.

Current sensing capability inside a system is much sought after for applications which include Peak-current mode control, Current limiting, Overload protection. Current sensing is extremely important for current sharing in Multi-phase topologies. Existing approaches such as Series resistor, SenseFET, inductor DCR based current sensing are simple but their drawbacks such low efficiency, low accuracy, limited bandwidth demand a novel current sensing scheme.

This research presents a systematic design procedure of a 5V - 1.8V, 8A 4-Phase Buck regulator with a novel current sensing scheme based on replication of the inductor current. The proposed solution consists of detailed system modelling in PLECS which includes modification of the peak current mode model to accommodate the new current sensing element, derivation of power-stage and Plant transfer functions, Controller design. The proposed model has been verified through PLECS simulations and compared with a transistor-level implementation of the system. The time-domain parameters such as overshoot and settling-time simulated through transistor-level implementation are in close agreement with the results obtained from the PLECS model.

DEDICATION

Dedicated to Shri Lakshmi Narayana – protector of all who seek his refuge, Shri Saraswati Devi – Goddess of knowledge and wisdom and Jagadguru Shri Madhvacharya – chief advocate of Dvaita philosophy and the supreme guru to all souls.

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CHAPTER 1

INTRODUCTION

1.1 Background

DC-DC Converters, which form a major component of a power management system, are widely used for applications demanding high efficiency. Switching converters use a power switch which offers zero resistance when closed and infinite impedance when open. In other words, the power dissipation is zero in both the situations. If we were to account for non-idealities, there would be power dissipation, although very small, from the switching and conduction losses [1].

The switching waveform is then filtered using a lossless LC filter to obtain an averaged output. Figure 1.1 shows one of the widely used and the simplest switching converter topologies – The Buck Converter. A closed-loop system is necessary to ensure stability and improvement in the transient response. Due to dynamic load and line fluctuations, it is extremely important to design a controller for the system to ensure stability and a better transient performance. Voltage Mode Control, one of the Pulse Width Modulation techniques [2][3] revolutionized the power supply industry since its invention in 1976. Peak current mode control [4] was introduced a couple of years later which falls under a different class of PWM Control.

Multi-phase Buck regulators are employed for supplying a high-load current. Individual phases of a Multi-phase Buck regulator operate in interleaved fashion to collectively source current to the load. Peak current mode control is a preferred choice since it lends itself to a simple implementation for Multi-phase converters. However, Inductor current sensing becomes an additional component of this control scheme and thus introduces circuit complexity.

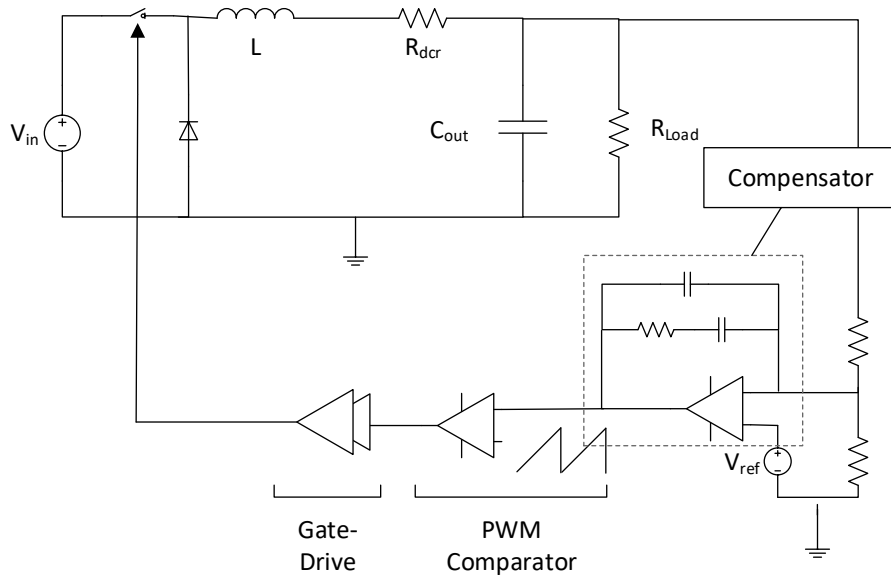


Figure 1.1 Buck Converter with Voltage-mode Control

1.2 Motivation

Due to the ever-increasing trend towards high integration and density, the current demands have increased. Expecting a single-phase/single-module converter to source a large current may result in degraded efficiency and reliability issues. If the current sourcing task is divided among different modules/phases, a significant improvement over an equivalent single-phase implementation can be achieved. Individual phases of a Multi-phase Buck regulator operate in interleaved fashion to collectively source current to the load. This trend also promotes smaller filter components such as inductors and capacitors while maintaining the voltage and current ripple at an acceptable level. Other important performance indicators such as improved transient response and efficiency make Multi-phase converters a preferred choice for low voltage, high-current applications [7][34].

Voltage-mode and Current-mode Control are two widely used control techniques for DC-DC Converters. Faster dynamic response, Cycle by cycle current limiting, Simple current sharing implementation and Modularity make Peak current mode control(PCMC) an attractive choice for control technique in Multi-phase converters [4][5][6]. Current sharing is achieved naturally in PCMC as the control signal generated by the controller serves as a reference to the inner current loop of

the individual phases thus ensuring the equality of individual phase currents [4]. Figure 1.2 shows a Buck converter with peak current mode control.

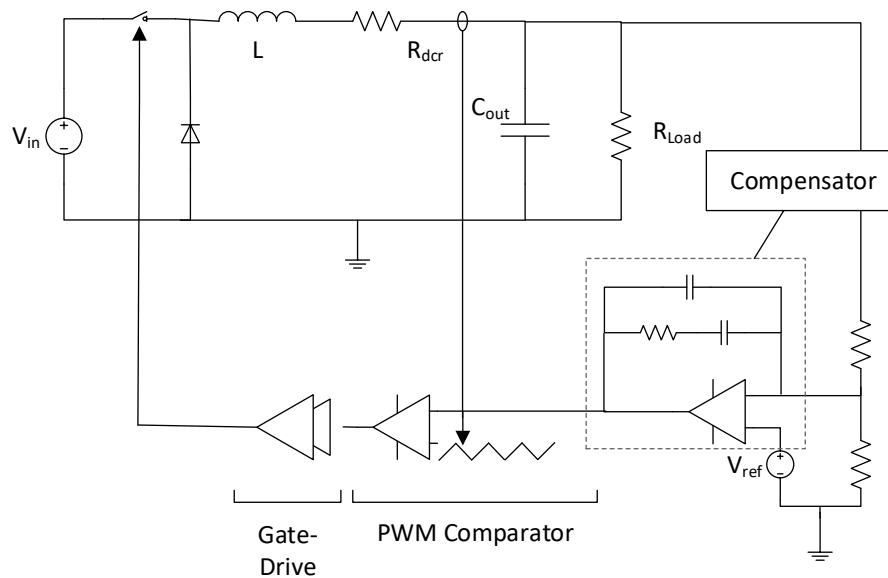


Figure 1.2. Buck Converter with Peak current-mode control

The sensed inductor current is compared with the control signal to generate reset pulses which control the turn-off of Power-FETs. Hence, inductor current sensing becomes an integral component of peak current mode control. In present trends, to cater to the needs of high switching frequency converters, the current sensing circuit must be efficient, accurate, fast and immune to switching node noise.

Reliability, Fault-tolerance, High current sharing accuracy are necessary for a multi-phase system [8][9]. Average currents of individual modules can deviate from the rest due to non-identical phases. Hence, a current-sharing mechanism or a dedicated external current-share loop becomes extremely important to ensure uniform current sharing in the presence of mismatches among individual phases. A Master-Slave current sharing technique is implemented to minimize current sharing error [8].

1.3 Prior work

Prior research in this field has been focused towards SenseFET [11][13] and $R_{ds,on}$ [13] based current sensing schemes for single-phase and Multi-phase Buck Converters.

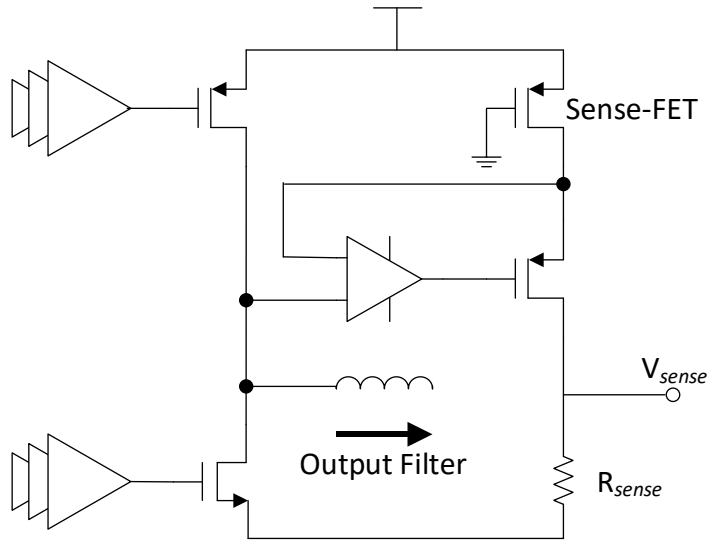


Figure 1.3 Sense-FET based Current Sensing

[12] proposes a Multiphase buck converter with Voltage mode control where current balancing scheme is implemented for better load sharing accuracy. Inductor current is obtained by high-side and low-side senseFET current sensors. This approach makes use of a scaled current mirror to copy the current through the PowerFET during its ON interval. The sensed current accuracy is dependent on the accuracy and precision of MOS transistor on resistance ($R_{ds,on}$) and the current mirror. To improve current mirroring accuracy, a high-gain, high-speed, low offset amplifier is used which equates the V_{DS} of the sense-FET and power-FET[11][14]. An important drawback of the senseFET based circuit is the current mirror mismatch and op-amp non-idealities [14][15][16].

[32] proposes a Multiphase buck converter with an instantaneous and average current sensor. A senseFET based current mirror forms the core of this instantaneous current sensor. The mirrored current sensed across a separate sense resistor is used for peak current mode control. Use of a separate sense resistor limits accuracy of the current sensor as it is dependent on the relative value of R_{sense} and $R_{ds,on}$ of the sense-FET [17].

$R_{ds,on}$ sensing [13] can be employed to detect the inductor current but this technique is prone to switching node ringing and PVT variations. To minimize the impact of switch-node ringing, Blanking [21] needs to be implemented which puts a constraint on the minimum duty cycle.

A Gyrator-based approach is proposed for active inductor synthesis in [18][20]. Although inductors can be synthesized using Gyration, this technique doesn't address replication of the inductor current. [19] proposes an inductor emulator circuit for ripple cancellation in DC-DC converters. This technique replicates only the ripple component of the inductor current. However, both the average and ripple components are required to be able to use it for Peak current mode control.

Prior works on current sharing include [8][9][10] which present a master-Slave current sharing technique. [8] implements a Master-Slave (MSC) scheme with a uniform current distribution among individual phases. Robustness to phase mismatches is a particularly desirable feature of this work. Slave-phases track the single master-phase to achieve a uniform current distribution. A dedicated external current share loop is implemented which corrects for the average inductor current mismatch. [10] investigates different paralleling schemes under MSC technique for multi-phase/multi-module converters. Two variants of a conventional MSC scheme are presented. One of the variants implements individual output capacitor for each module. A second variant is investigated which increases the reliability of the system by implementing an individual voltage feedback circuit and a respective voltage reference. In this scheme, failure of a module doesn't lead to failure of the entire system since each module behaves as a standalone voltage regulator. However, it introduces additional design complexity.

1.4 Proposed solution

A Multiphase Buck converter employing peak current mode with an inductor current sensing scheme and a dedicated current sharing loop is preferred to meet the requirements such as high current, smaller filter components, fast transient response, high efficiency and reliability.

A systematic approach detailing the design procedure of this system is described. Block level and Circuit level modeling simplifies the design task thus reducing the design effort. Also, model makes the design more intuitive and easy to understand. Keeping this in mind, the entire system was modelled in PLECS and power-stage transfer functions were derived. The Controller was designed based on the pole-zero placement approach to achieve a 60° phase margin. The model was verified through PLECS simulations and transistor level implementation was then carried out to verify the PLECS model through Spectre simulations.

1.5 Thesis Organization

Chapter 1 introduces the research topic and the proposed solution. Chapter 2 provides a detailed System overview, modelling approach, transfer-function relations and Controller design. Chapter 3 details the circuit implementation of the model. Chapter 4 discusses the model and circuit simulation results and provides a comparison between the model and its circuit implementation. The conclusions and future improvements are discussed in Chapter 5.

CHAPTER 2

SYSTEM OVERVIEW AND MODELLING

2.1 System Overview

2.1.1 Ripple Current Sensing

The primary objective of the proposed solution is to come up with a transistor-level implementation of inductor current sensing element which can be employed for peak current mode control [37]. In this setup, only the current sense component is different and rest of the system functions as the conventional peak current mode control in a Buck Converter [6].

The inductor current ripple during the on-time and off-time of the Buck converter is given by the relation:

$$\Delta iL_{on} = (V_{in} - V_o) * D * \frac{T_s}{L} \quad (2.1)$$

$$\Delta iL_{off} = -V_o * (1 - D) * \frac{T_s}{L} \quad (2.2)$$

V_{in} = Input Voltage

V_o = Output Voltage

D = Duty Cycle given by V_o/V_{in}

L = Inductance

T_s = Switching period of the converter

Ripple component of inductor current has a triangular shape. We observe from the equations that the inductor current slope during ramp-up is dependent on the switch on-time, Input and Output Voltage and the inductance. Voltage developed across a Capacitor if charged by a constant current of magnitude I_c for $D*T_s$ seconds is given by

$$\Delta vC_{on} = I_c * D * \frac{T_s}{C} \quad (2.3)$$

We observe from the equation above that a capacitor, charged using a constant current source, exhibits a ramp nature of its output voltage. This property of a capacitor can be utilized to construct the inductor current. Noting the similarities of inductor current and capacitor voltages, we can arrive at the first order Inductor emulator principle. Apart from the similarity of shapes of capacitor voltage and inductor current, we must ensure that their magnitudes are equal as well.

Equating (2.1) and (2.3),

$$I_c * (D) * \frac{T_s}{C} = (V_i - V_o) * D * \frac{T_s}{L}$$

Consider $D * T_s = T_{on,cap}$ and $D * T_s = T_{on,ind}$

Rewriting the equation, we can arrive at the emulator equation:

$$\frac{I_c * T_{on,cap}}{C} = (V_i - V_o) * \frac{T_{on,ind}}{L} \quad (2.4)$$

$T_{on,cap} = T_{on,ind}$ implies that the time during which a capacitor charges should equal that of inductor. If,

$$I_c = (V_i - V_o) * \frac{C}{L} \quad (2.5)$$

magnitude of peak capacitor voltage equals that of peak inductor current.

Interpreting the equation, if a capacitor is charged with a constant current source of magnitude derived in equation 2.5, we can replicate the peak inductor current. The main idea is to charge a capacitor with a current of magnitude proportional to $V_i - V_o$, which is the voltage across inductor during its ON time. If the capacitor is discharged at the instant its voltage reaches control signal, a ramp waveform as shown in the Figure 2.1 can be generated. Due to inherent mismatch between the inductor and emulator circuit, it is challenging to generate a precise current source which accurately tracks the input and output voltages. However, it is the emulated signal that is being compared with the control signal. Hence, despite mismatches within a $\pm 20\%$ range, the feedback

loop generates an appropriate value required for output voltage regulation. It is, however, critical to ensure accurate matching between turn-on times of inductor and the inductor emulator.

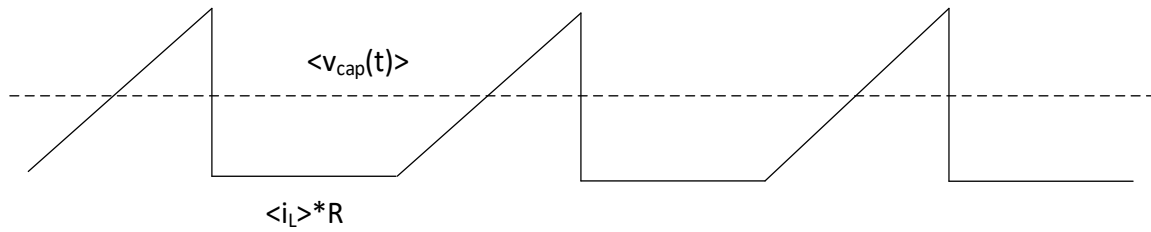


Figure 2.1 Emulated Inductor Current Waveform

Figure 2.2 describes the circuit which realizes the emulator equation.

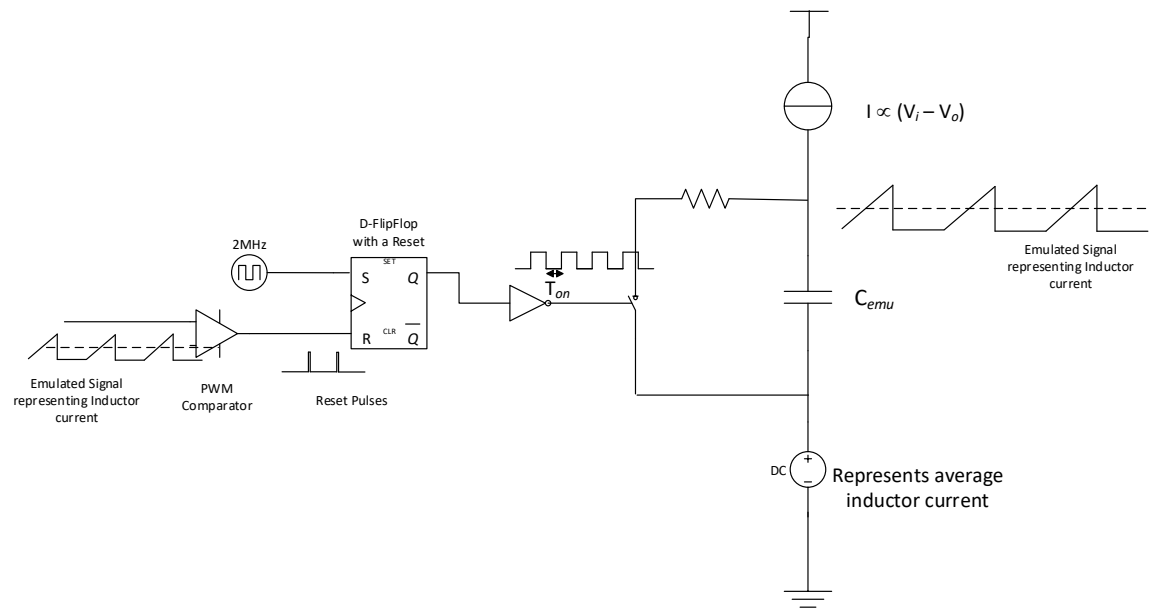


Figure 2.2 Inductor Emulator Circuit

Switch across the capacitor is off for the duration which equals the ramp-up time of the inductor current. In other words, the capacitor is being charged for the interval which equals ramp-up time of inductor current. The capacitor is then discharged at the instant its voltage hits the control signal. In the peak current mode setting, the control signal is generated by an external voltage loop controller. Only the ramp-up time is considered in the circuit implementation as the peak current mode control requires only the positive slope inductor current. The proposed current sensing solution implements a transistor-level schematic of the technique in [37]. Inductor DCR sense

based average current sensing scheme is used instead of track and hold based average current sensing scheme.

2.1.2 Average Current Sensing Block

Average current information is also required along with the peak current. In conventional PCMC, the control voltage generated by controller is compared with the consolidated inductor current which has both ripple and average components. Hence, an average current block is designed to replicate the entire inductor current which can be utilized for PCMC.

Inductor DCR sensing can be employed for average current sensing. This scheme doesn't require matching of LR and RC time constants [32][35]. An RC filter is added in parallel with Inductor. The voltage across this filter capacitor is due to the voltage drop across Inductor DCR. This voltage is sensed to extract the average inductor current information. The filter components must be large enough to obtain an accurate average current information. It is important to point out the tradeoff between the current sensing speed and accuracy. Large R and C introduces considerable delay in the average current sensing process.

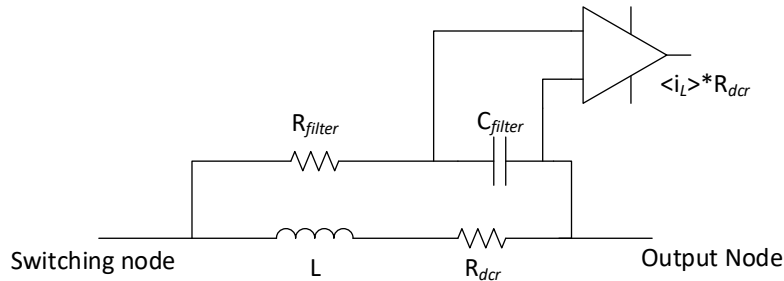


Figure 2.3 Average Inductor Current Sensing

From the figure above, the voltage across capacitor can be derived as

$$V_c(s) = K * (sL + R_{dcr}) * \frac{I_L(s)}{RCs + 1} \quad (2.6)$$

$$V_c(0) = K * I_L(0) * R_{dcr} \quad (2.7)$$

Where

$V_c(s)$ = Capacitor voltage

sL = Inductor impedance

R_{dcr} = Inductor DCR

R,C = Filter components

K = Difference amplifier gain

In other words, the average component of the capacitor voltage is a function of average inductor current. This relation is independent of the LR and RC time constant matching. Rest of the DC-DC converter blocks such as Power-FETs, Power-Stage, Controller, PWM Comparator, Gate-Drive blocks and Multi-Phase Clock generator function as the ones used in a conventional PCMC Buck Converter. Their circuit implementation is explained in Chapter 3.

2.1.3 Master-Slave Current Sharing Block

One of the major challenges in the proposed current sensing scheme is matching between the power-stage Inductor and Emulator components. Any mismatch between them can result in variation of the inductor current slope which ultimately leads to mismatch in the individual phase average currents. Hence, a Master-Slave Current sharing approach with slave phase calibration is implemented to ensure uniform current sharing among different phases[12].

All the slave phases are made to follow the master-phase by forcing each slave phase to source the same current equal to that of master-phase. This is achieved by operating each phase with the same duty-cycle thus enforcing equal currents. The master-phase is controlled by the single compensator whereas the each of the slave phases' control signal is calibrated to ensure the equality of duty cycle of each phase.

2.1.3.1 Slave Phase Calibration

Presence of mismatches between the power-stage and emulator components can result in severe mismatch between individual phase average inductor currents. In this scheme, the error current information is extracted and is used to calibrate each of the slave phases' control signal so that their individual duty cycle matches with that of the master-phase. Matching the duty-cycle ensures the equality of the average currents.

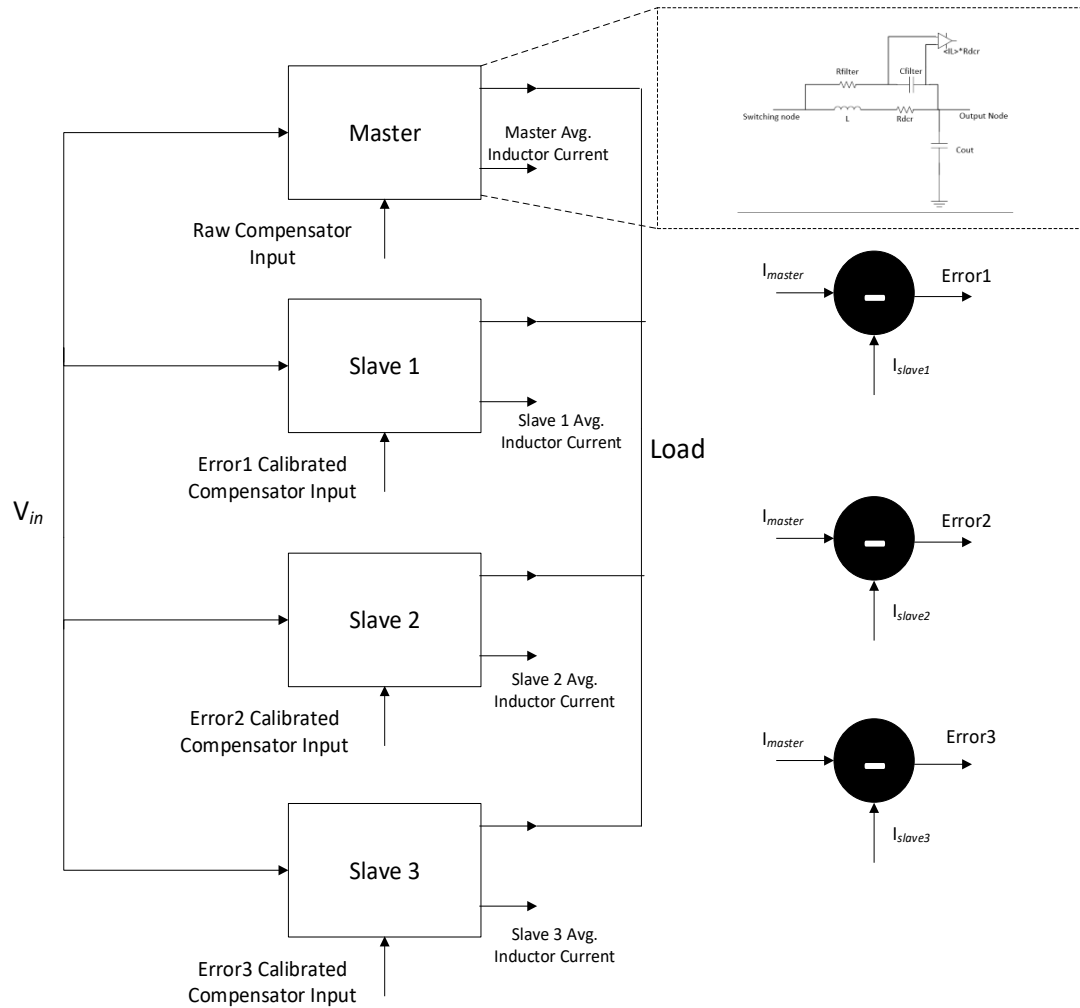


Figure 2.4 System Model excluding Current Sense Block

2.2 Modelling

Any switching converter is a Non-linear, Time-varying system. Hence, a Linear, Time-Invariant model must be developed for a Switching Mode Power Supply(SMPS) to apply the conventional linear control methods [25].

2.2.1 Modelling Procedure

Considering the time-variant nature of an SMPS, to apply linear control methods, first a time-invariant model needs to be developed. Since an SMPS is a switching system, the operating modes of the converter depends on the on/off state of the power-switches. In other words, the system is not time-invariant. Hence, an averaged (time-invariant) model needs to be developed so that small-signal (linear) models of a time-invariant system could be obtained[25]. In that regard, State-space

averaging [22] and Circuit Averaging [23] are two widely used techniques for deriving an average model for the power-stage of an SMPS.

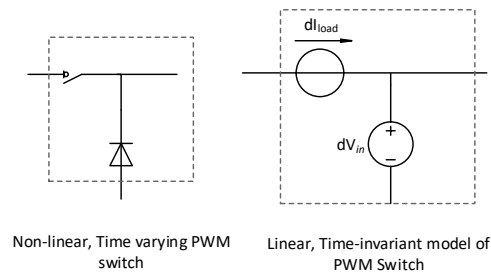


Figure 2.5 PWM Switch Model as described in [25]

Having derived the average model, next step would be to linearize this model around an operating point and derive small - signal models or rather, perturbation models. The control system so developed compensates for perturbations caused due to any dynamic transients in a system. Hence, perturbation (small-signal) models are derived to characterize the controller action during any transients.

2.2.1.1 Power-Stage Transfer functions

Duty ratio to Output voltage (V_{out}) and Duty ratio to inductor current ($I_{inductor}$) are two important transfer functions obtained after deriving averaged, small-signal models. Since duty ratio is the control input and V_{out} , $I_{inductor}$ are output quantities, it is essential to derive the relation between the control and output quantities so that an appropriate controller can be designed which compensates for perturbations in the output quantities. Figures 2.6 and 2.7 represent the perturbation model of the averaged model which were used to derive these transfer functions [24].

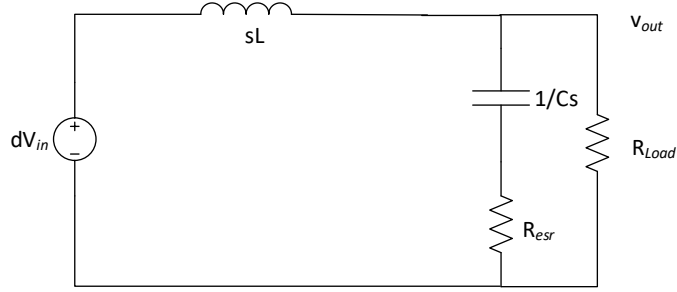


Figure 2.6 Averaged small-signal model for deriving control to output relation

Considering an ideal inductor with $R_{dcr} = 0\Omega$, following transfer function was derived

$$v_{out} = \frac{R_{load} \parallel \left(R_{esr} + \frac{1}{sC} \right)}{sL + \left(R_{load} \parallel \left(R_{esr} + \frac{1}{sC} \right) \right)} * d * V_{in} \quad (2.8)$$

$$\frac{v_{out}}{d} = V_{in} * \frac{1 + sCR_{esr}}{1 + s \left(\frac{L}{R_{load}} + CR_{esr} \right) + s^2 * LC \left(1 + \frac{R_{esr}}{R_{load}} \right)} \quad (2.9)$$

This transfer function represents the control to output transfer function of Voltage-mode control.

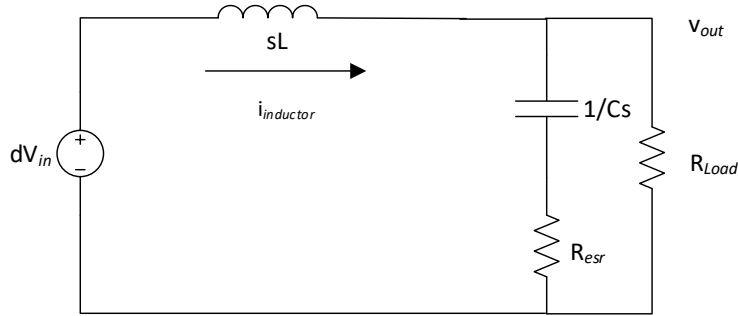


Figure 2.7 Averaged small-signal model for deriving control to inductor current relation

$$i_L = d * \frac{V_{in}}{\left(sL + \left(R_{load} \parallel \left(R_{esr} + \frac{1}{sC} \right) \right) \right)} \quad (2.10)$$

$$\frac{i_L}{d} = \frac{V_{in}}{R_{load}} * \frac{1 + sC(R_{esr} + R_{load})}{1 + s \left(\frac{L}{R_{load}} + CR_{esr} \right) + s^2 LC \left(1 + \frac{R_{esr}}{R_{load}} \right)} \quad (2.11)$$

This transfer function represents the control to average inductor current transfer function of Voltage-mode control.

2.2.1.2 Prior Peak current mode model

According to the peak current mode control theory, the inductor of a Buck or a Buck-derived converter behaves as a voltage controlled current source if the power-switch is opened when the inductor current reaches a threshold. This threshold is variable and is generated by an external voltage loop which ensures output voltage regulation. In other words, the external controller adjusts the control signal so as to enforce a current which results in the desired output voltage [4].

The model shown in Figure 2.8 can be obtained if the inductor is treated as a current source. This approximation neglects the LC double pole thus transforming the plant to a 1st order system. However, this model is accurate only up to 1/50 of the switching frequency [25].

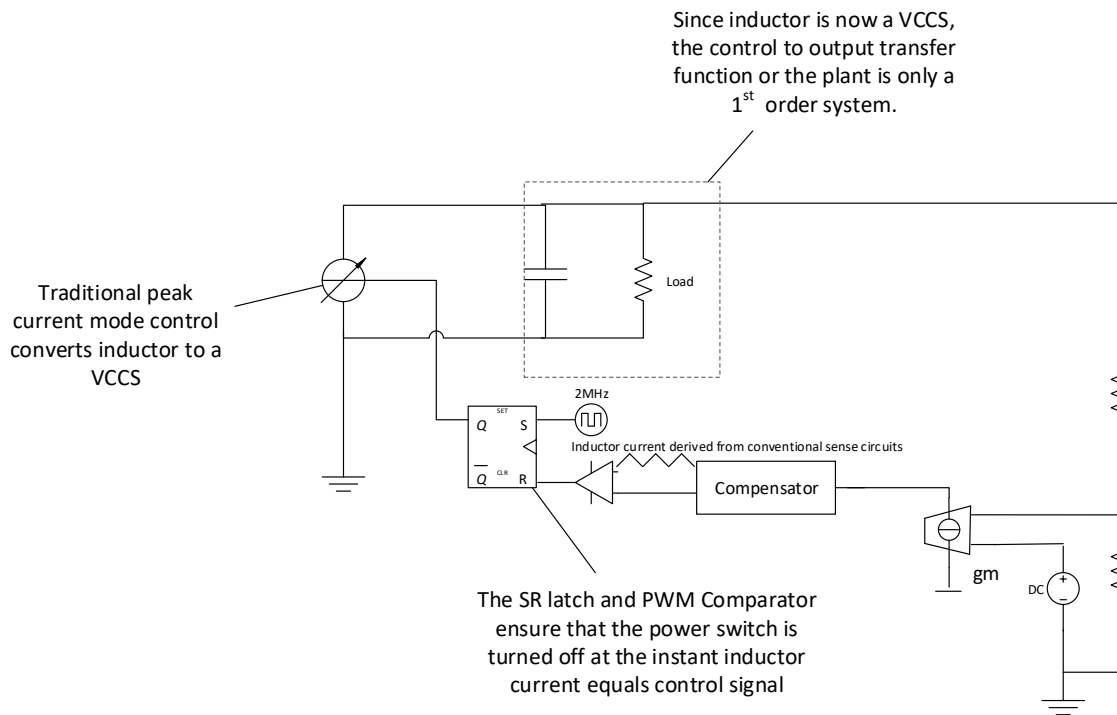


Figure 2.8 Conventional Peak current mode model as described in [25]

2.2.2 Proposed Peak current mode model

A different modelling approach is followed in this work. The plant is not approximated as a 1st order system and a general model is obtained [26].

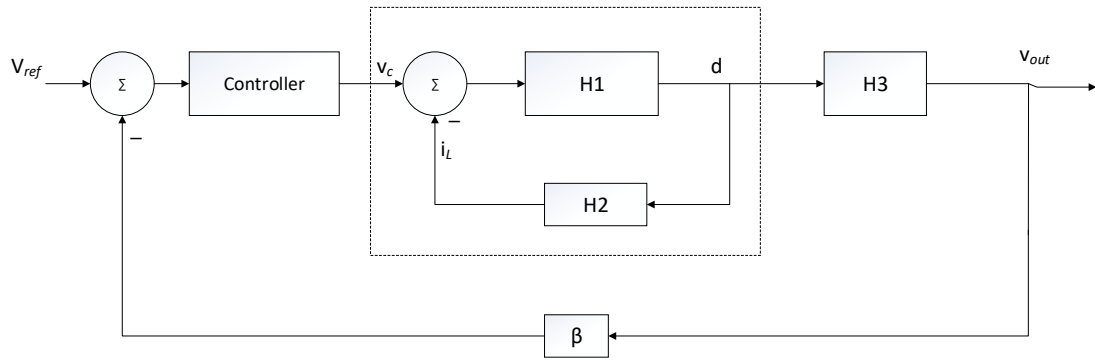


Figure 2.9 Closed-loop system describing Reference to Output Relation

The model depicts the v_{ref} to v_{out} transfer function of the system. In the figure above,

β = Feedback factor or resistor divider term

Summer and Controller together represent the Error Amplifier and compensator network

Second loop represents the inner current loop.

H1 = PWM gain

H2 = d to i_L transfer function as derived in equation (2.11)

H3 = d to v_o transfer function as derived in equation (2.9)

The design procedure of compensator assumes that the Controller looks at a single plant, which can be obtained by reducing the inner loop using Mason's gain rule. Hence, the model shown in Figure 2.10 can be reduced to the one shown in Figure 2.11.

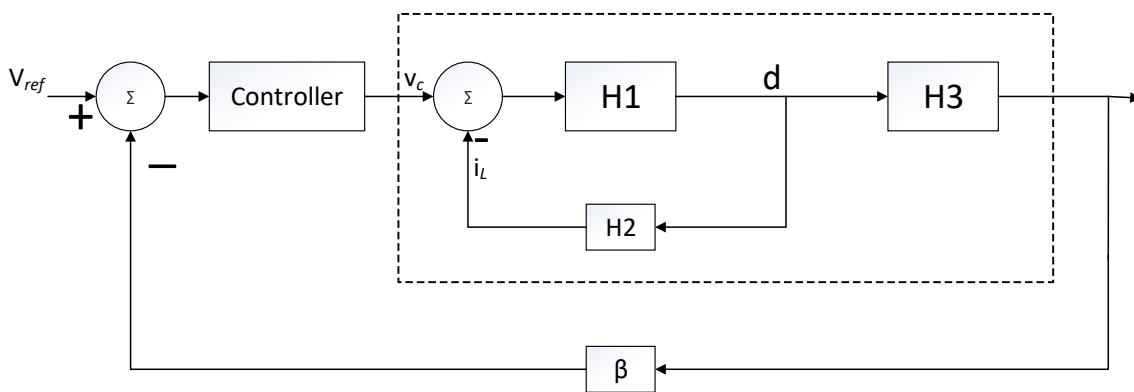


Figure 2.10 A Closed loop system with multiple loops

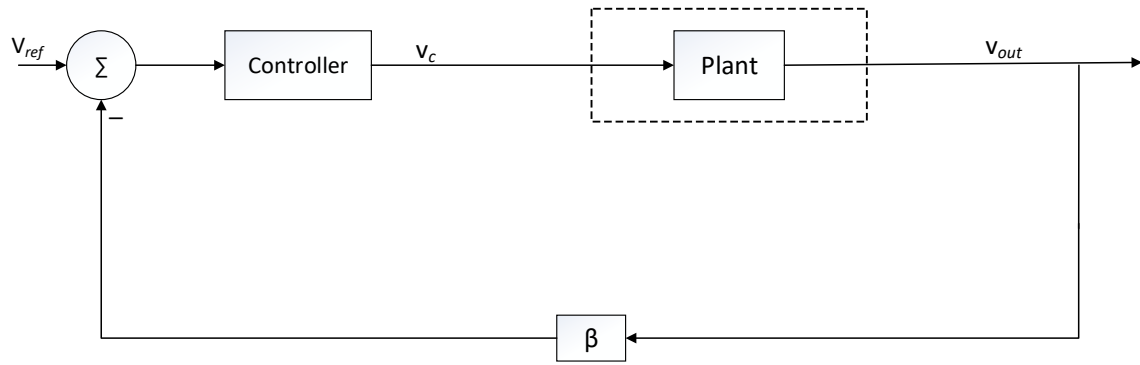


Figure 2.11 A Multi-loop system reduced to a single-loop system

2.2.3 System Model of the Proposed Solution

Model developed in [26] was modified to integrate the proposed current sensing element and the average current sensing blocks. Figure 2.12 depicts an averaged, linearized model of a single-phase Buck converter. The same model can be scaled to include a 4-Phase Buck converter.

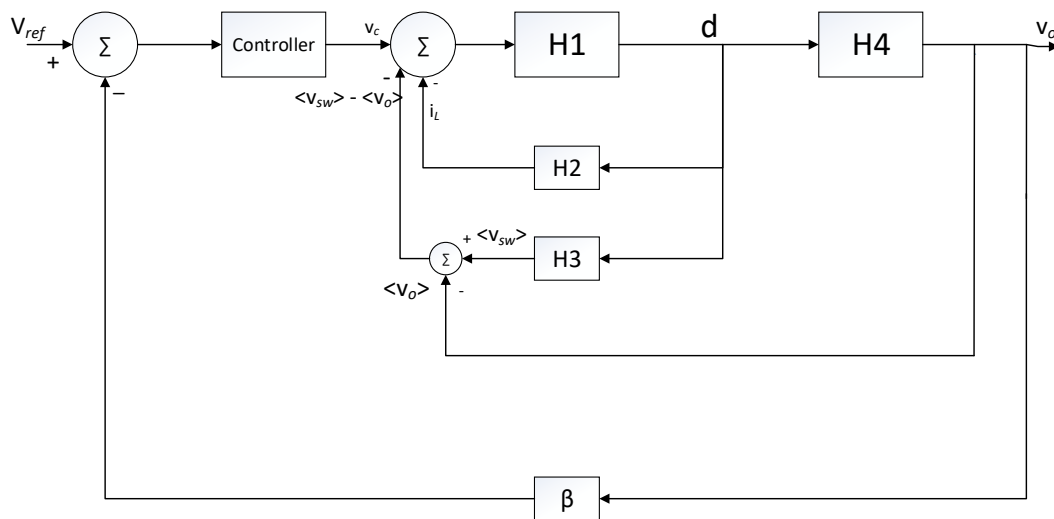


Figure 2.12 A Closed Multi-loop system model of the proposed Buck Converter (Single-phase)

In the figure above,

- V_{ref} represents the reference voltage output generated from an on-chip reference/external block.

- Summer and Controller block together represent the error amplifier and external voltage loop compensator designed for the system.
- Summer inside the external loop represents the PWM comparator block.
- H1 represents the PWM gain which was derived according to the proposed current sensing block.
- H2 represents the transfer function of duty-cycle to emulated peak voltage.
- H3 represents the transfer function of duty-cycle to switching node average.
- H4 represents the transfer function of duty-cycle to output voltage.
- β represents the feedback factor or resistor divider ratio.

In the model above, both average and peak current block are specified as both are necessary to extract the inductor current information for peak current mode control. The peak and average current information are combined to form a replica of the inductor current.

2.2.4 Transfer-Function Derivation

2.2.4.1 PWM Gain

H1 represents PWM gain. [27] proposes a PWM gain function for conventional inductor current sensing. This approach was modified to arrive at the PWM gain function for the proposed current sensing scheme.

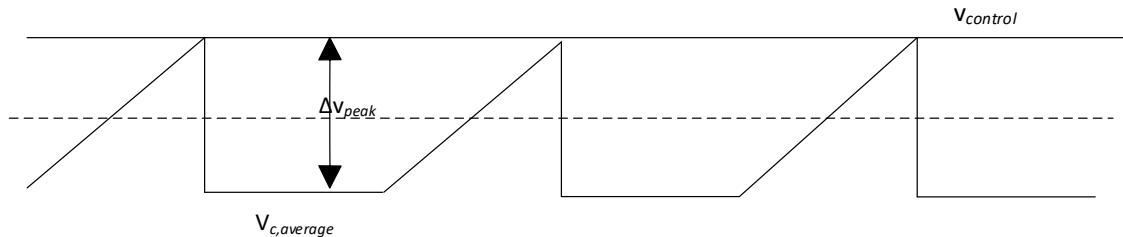


Figure 2.13 Capacitor voltage waveform replicating the ramp-up inductor current ripple

From the figure above,

$$V_{ctrl} - \Delta v_{peak} = V_{c,average}$$

$$\Delta v_{peak} = I_c * d * \frac{T_s}{C}$$

$$I_c = K_{vi} * (V_i - V_o)$$

$$V_{ctrl} - \left\{ K_{vi} * (V_i - V_o) * d * \frac{T_s}{C} \right\} = V_{c_{average}}$$

$$(V + v_{ctrl}) - \left\{ K_{vi} * (V_i - (V_o + v_o)) * (D + \tilde{d}) * \frac{T_s}{C} \right\} = (V_c + v_{c_{average}})$$

Where,

- V_{ctrl} = control output of the controller (DC + perturbation term).
- Δv_{peak} = peak-peak ripple of emulated voltage.
- I_c = Magnitude of the constant current source.
- K_{vi} = Voltage to current gain of the emulator circuit.
- V_i = Steady state input voltage of the Buck.
- v_i = input voltage perturbation.
- V_o = Steady state desired output voltage.
- v_o = output voltage perturbation.
- D = steady state duty cycle.
- \tilde{d} = duty cycle perturbation.
- T_s = Switching period.
- C = Emulator Capacitance.
- $V_{c_{average}}$ = quantity representing the average inductor current.
- $v_{c_{average}}$ = perturbation term.

The equation above contains both steady state and perturbation terms.

Considering only perturbation model and linearizing it around an operating point,

$$v_{ctrl} - \left\{ K_{vi} * (V_i - V_o) * \tilde{d} * \frac{T_s}{C} \right\} = v_{c_{average}}$$

$$\frac{\tilde{d}}{v_{ctrl} - v_{Caverage}} = \frac{C}{K_{vi} * (V_i - V_o) * T_s} = H1 \quad (2.12)$$

2.2.4.2 Inductor Emulator

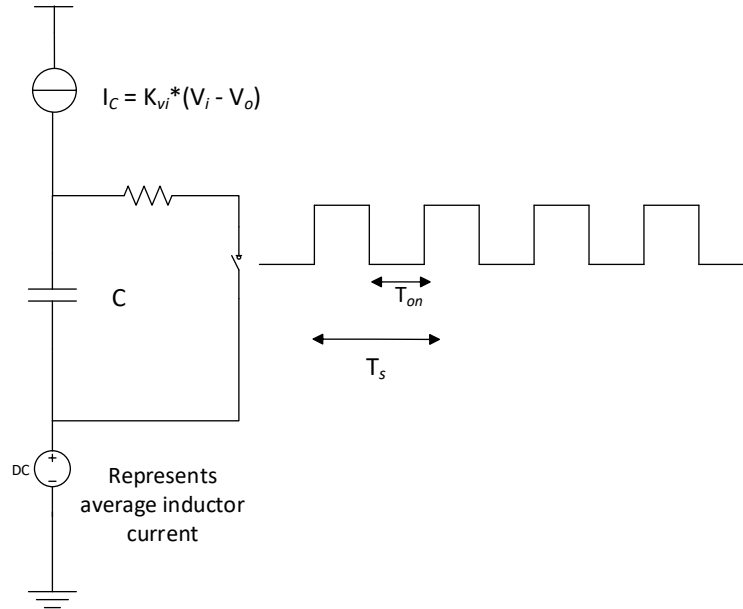


Figure 2.14 Inductor Emulator Model

Figure above represents the model of the inductor emulator. The capacitor charges during switch OFF interval and discharges to 0V during switch ON interval. T_{on} represents the ramp-up time of capacitor voltage. Figure 2.15 represents the emulated voltage indicative of peak and average inductor current.

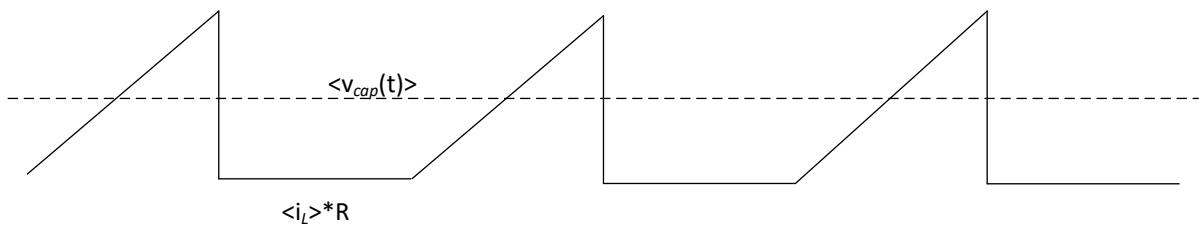


Figure 2.15 Emulated inductor current waveform

$$\langle v_{cap}(t) \rangle = \langle i_L(t) \rangle * R + \frac{1}{T_s} * \left[\int_0^{dT_s} v_{cap}(t) dt + \int_{dT_s}^{(1-d)T_s} v_{cap}(t) dt \right] \quad (2.13)$$

Since the capacitor is being discharged during the switch on interval, equation (2.13) can be modified as

$$\langle v_{cap}(t) \rangle = \langle i_L(t) \rangle * R + \frac{1}{T_s} * \int_0^{dT_s} v_{cap}(t) dt \quad (2.14)$$

Equation above represents the relation for the average value of emulated signal. Only the ramp up time of the inductor current is considered. The term, $\langle i_L(t) \rangle * R$ represents the voltage signal indicative of average component of inductor current. The term, $\frac{1}{T_s} * \int_0^{dT_s} v_{cap}(t) dt$ represents average of the ripple component. If a capacitor is charged using a time-varying current source, voltage across it is given by the following relation:

$$v_{cap}(t) = \frac{1}{C} * \int i_c(t) dt$$

Where $i_c = K_{vi} * (v_i - v_o)$, K_{vi} indicating voltage to current gain. This equation depicts that the emulator capacitor is being charged with current of magnitude proportional to $(v_i - v_o)$.

Evaluating the capacitor voltage during the switching interval,

$$v_{cap}(t) = \frac{1}{C} * \left[\int_0^{dT_s} i_c(t) dt + \int_{dT_s}^{(1-d)T_s} i_c(t) dt \right]$$

Hence, the equation (2.14) can be expressed as

$$\langle v_{cap}(t) \rangle = \langle i_L \rangle * R + \frac{1}{T_s} * \int_0^{dT_s} \int_0^{dT_s} \frac{i_1 - i_2}{C} dt \quad (2.15)$$

- $i_c = i_1 - i_2$ represents the instantaneous current of magnitude proportional to $(V_i - V_o)$ term according to the inductor emulator principle.
- $i_1 - i_2$ are indicative of the v_i and v_o term respectively. They have been included to specify the utility of input and output voltages in the emulator principle.

- It is important to note that the capacitor voltage term during the interval: dT_s to $(1 - d)T_s$, has not been included as the capacitor is being discharged and the hence the ripple component is zero.

Identifying the DC and perturbation terms, the equation can be expressed as

$$\langle v_{cap}(t) \rangle = \langle i_L \rangle * R + \frac{1}{T_s} * \int_0^{dT_s} \int_0^{dT_s} \left\{ \frac{(I_1 - I_2)}{C} + \frac{(\tilde{i}_1 - \tilde{i}_2)}{C} \right\} dt \quad (2.16)$$

The perturbation term due to I_1 component, \tilde{i}_1 has been neglected as the input is assumed to be a steady DC source.

$$\begin{aligned} \langle v_{cap}(t) \rangle &= \langle i_L \rangle * R + \frac{1}{C * T_s} \int_0^{dT_s} \left[(I_1 - I_2) * t \Big|_0^{dT_s} - \int_0^{dT_s} \tilde{i}_2(t) dt \right] \\ \langle v_{cap}(t) \rangle &= \langle i_L \rangle * R + \frac{1}{C * T_s} * \left[\int_0^{dT_s} (I_1 - I_2) * d * T_s - \int_0^{dT_s} \int_0^{dT_s} \tilde{i}_2(t) dt \right] \\ \langle v_{cap}(t) \rangle &= \langle i_L \rangle * R + \frac{T_s}{C} * (I_1 - I_2) * d^2 - \frac{1}{C * T_s} * \int_0^{dT_s} \int_0^{dT_s} \tilde{i}_2(t) dt \end{aligned} \quad (2.17)$$

d is the duty cycle term which contains both DC and perturbation terms, or $d = D + \tilde{d}$

Rewriting equation (2.17) with both DC and perturbation terms yields

$$\begin{aligned} \langle \widetilde{v_{cap}(t)} \rangle &= \tilde{d} * \left[\frac{\tilde{i}_L}{\tilde{d}} \right] * R + (I_1 - I_2) * \frac{T_s}{C} * (D + \tilde{d})^2 - \frac{T_s}{C} * (D + \tilde{d})^2 * \tilde{v}_o \\ \langle \widetilde{v_{cap}(t)} \rangle &= \tilde{d} * \left[\frac{\tilde{i}_L}{\tilde{d}} \right] * R + (I_1 - I_2) * \frac{T_s}{C} * (D^2 + \tilde{d}^2 + 2 * \tilde{d} * D) - \frac{T_s}{C} * (D^2 + \tilde{d}^2 + 2 * \tilde{d} * D) \tilde{v}_o \end{aligned}$$

Linearizing the equation above yields

$$\langle \widetilde{v_{cap}(t)} \rangle = \underbrace{\tilde{d} * \left[\frac{\tilde{i}_L}{\tilde{d}} \right] * R}_{\text{H3}} + \underbrace{(I_1 - I_2) * \frac{T_s}{C} * 2 * D * \tilde{d}}_{\text{H2}} - \underbrace{\frac{T_s}{C} * D^2 * \tilde{v}_o}_{\text{H5}} \quad (2.18)$$

Referring to the Figure 2.16 and identifying each transfer functions we can arrive at the following transfer functions:

- $H3 \triangleq \text{AverageCurrent Block} = \left[\frac{\tilde{i}_L}{\tilde{d}} \right]$ represents the transfer function indicative of average current block.
- $\left[\frac{\tilde{i}_L}{\tilde{d}} \right]$ is obtained in case of conventional average current sensing. In this work, $(H3 - H4)$ represents the average current block. The expressions for H3 and H4 shall be derived in the subsequent sections.

$$H2 = \frac{\langle v_{cap}(t) \rangle}{\tilde{d}} = 2 * D * T_s * \frac{I_1 - I_2}{C} \quad (2.19)$$

represents the inductor emulator transfer function, where $I_1 = K_{vi} * V_i$ and $I_2 = K_{vi} * V_{out}$

- H5 represents the contribution of output voltage term, which is neglected.

Equation (2.18) can be represented through a block diagram as shown below

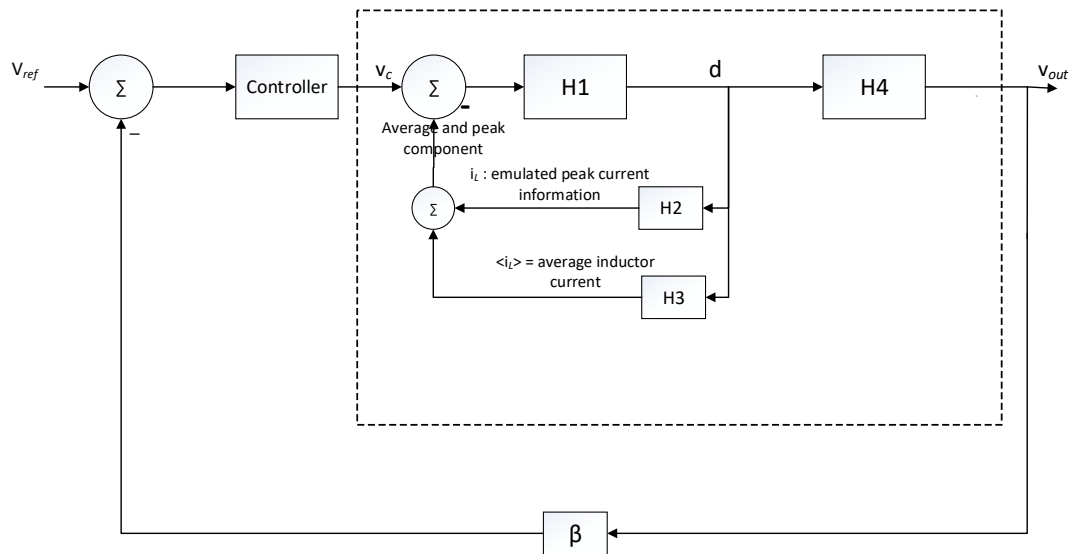


Figure 2.16 Block Representation of (2.18)

Where,

H1 = PWM gain function as derived in 2.2.4.1

H2 = Inductor emulator transfer function.

H3 = average inductor current transfer function.

In this work, the transfer function H3 is replaced by the inductor DCR sense block as shown in the Figure 2.17.

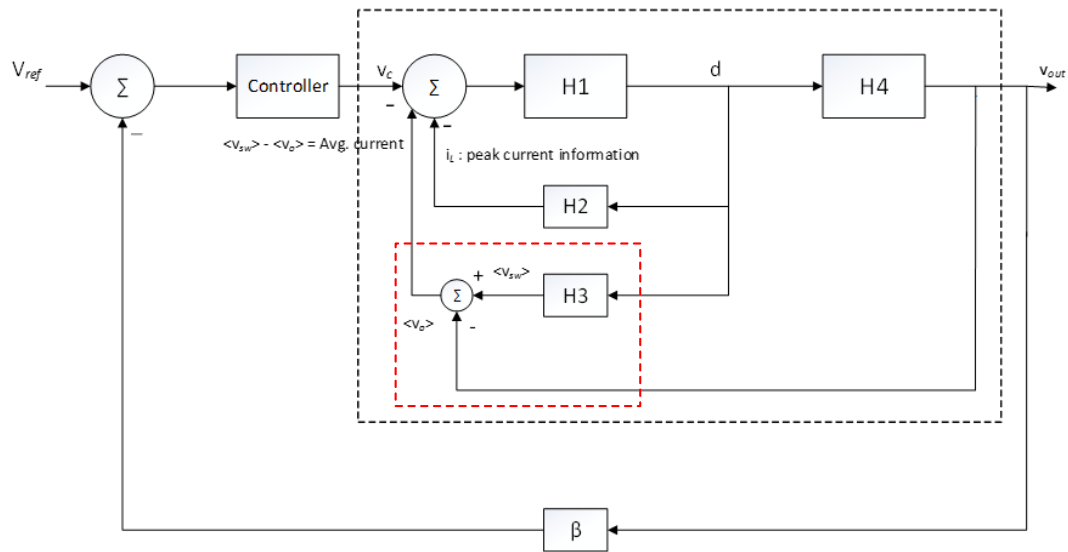


Figure 2.17 Modified Block Representation of 2.16 indicating Inductor DCR Sense

In the figure above, (H3 – H4) represents the inductor DCR average current sense block. If v_{avg} is the average inductor current component,

$$\frac{v_{avg}}{d} = \frac{\langle v_{sw} \rangle - v_{out}}{d} = \frac{\langle v_{sw} \rangle}{d} - \frac{(v_{out})}{d} = H3 - H4$$

2.2.4.3 Average Inductor Current Block (duty-cycle to switching node average)

As explained in section 2.2.4.2, Inductor DCR sensing has been employed for average inductor current sensing.

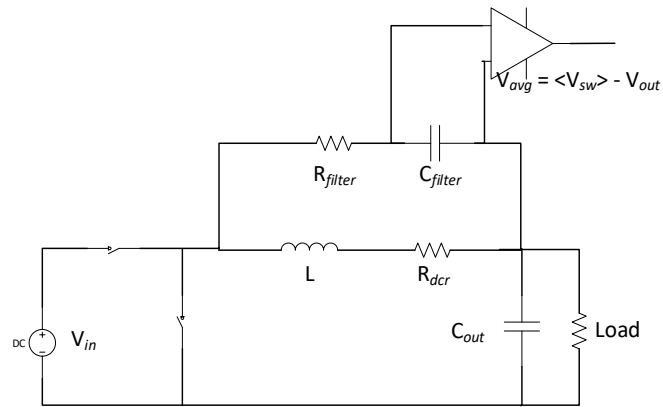


Figure 2.18 Inductor DCR Sense

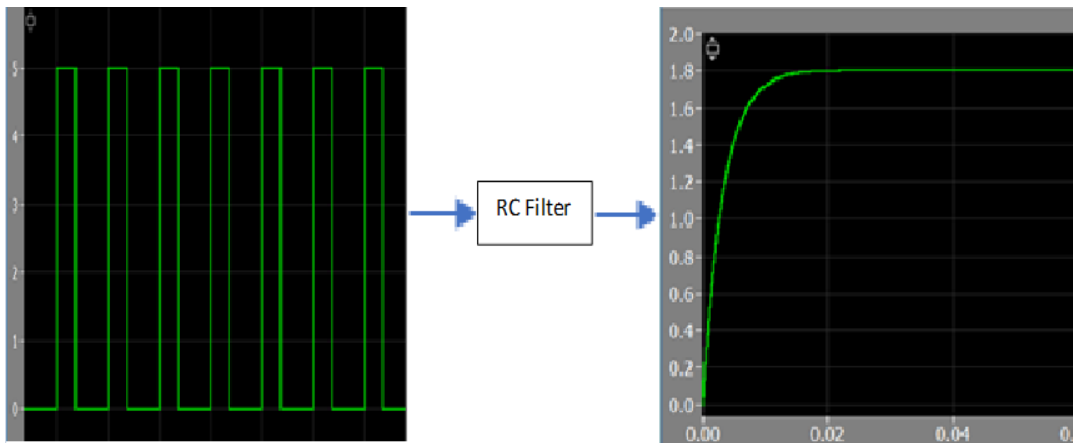


Figure 2.19 Switching Node Average

Figure above represents an ideal switching node waveform and its average value. This information is obtained from RC filtering the switching node as shown in Figure 2.19. However, due to large filter components, there is a large current sensing delay due to the RC time constant. Hence, this delay needs to be considered in deriving the transfer function for average current sense block.

The following relation can be obtained from Figure 2.19

$$\langle v_{sw} \rangle = \tilde{d} * V_{in} * \left(1 - e^{\left(-\frac{t}{RC}\right)}\right) \quad (2.20)$$

Laplacian representation of the equation above yields

$$\frac{\langle v_{sw}(s) \rangle}{\tilde{d}} = \frac{V_{in}}{s * (1 + as)} = H3 \quad (2.21)$$

Where,

$\langle v_{sw} \rangle$ = Average of switching node voltage

\tilde{d} = perturbation in the duty cycle.

V_{in} = Input voltage.

a = RC = time constant of the RC filter.

2.2.4.4 Control to Output Block

The duty-cycle to output voltage transfer function is same as the one derived in section 2.2.1.1

$$\frac{v_o}{\tilde{d}} = V_{in} * \frac{1 + sCR_{esr}}{1 + s\left(\frac{L}{R_{Load}} + CR_{esr}\right) + s^2 * LC\left(1 + \frac{R_{esr}}{R_{Load}}\right)} = H4 \quad (2.22)$$

2.2.5 Master-Slave Current Sharing Model

A model as shown in Figure 2.20 is derived for incorporating Master-slave current sharing algorithm. [12] implements this algorithm where output of the controller is calibrated with the average current error and is then input to each of the slave phases. Slave-phases receive a calibrated value and the master-phase receives a raw control input from the external controller. The duty cycle of each phase is made equal through this algorithm.

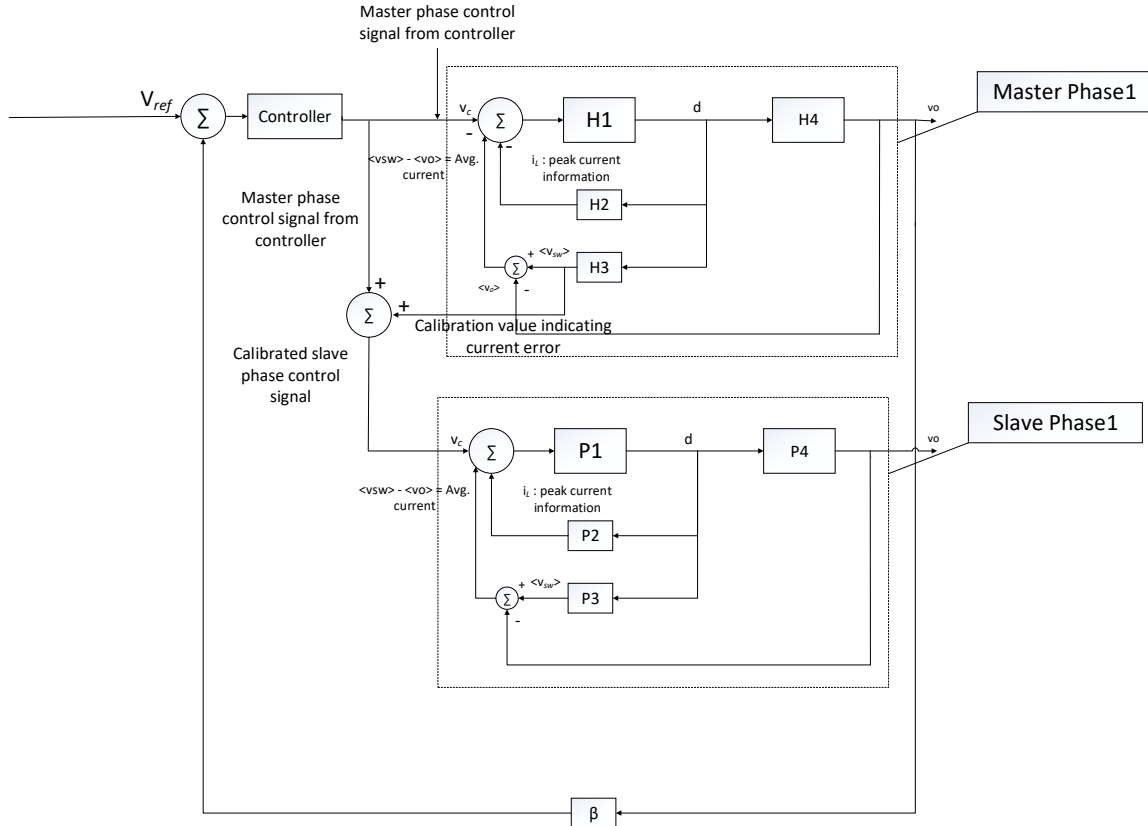


Figure 2.20 Master-Slave Sharing - Slave-Phase Calibration

As derived in Section 2.2.4.2 ($\langle v_{sw} \rangle - v_{out}$) indicates the average inductor current term of each phase. In a 2-phase system,

$$K * (\langle v_{sw1} \rangle - v_{out}) = \langle v_{avg1} \rangle$$

$$K * (\langle v_{sw2} \rangle - v_{out}) = \langle v_{avg2} \rangle$$

$$\langle v_{avg1} \rangle - \langle v_{avg2} \rangle = v_{error}$$

$$v_{comp} + v_{error} = v_{calibrated}$$

Where K represents the average current sensor gain(difference amplifier gain) and $v_{calibrated}$ represents the calibrated control signal which is fed to each of the slave phases.

$$v_{control} + [(\langle v_{sw1} \rangle - v_{out}) - (\langle v_{sw2} \rangle - v_{out})] = v_{calibrated}$$

$$v_{control} + [\langle v_{sw1} \rangle - \langle v_{sw2} \rangle] = v_{calibrated}$$

Note : $\langle v_{sw1} \rangle - \langle v_{sw2} \rangle$ will be non-zero only when there are mismatches between the phases.

$\langle v_{sw1} \rangle = A(s) * v_{control}$ can be obtained from the closed-loop gain from $v_{control}$ to $\langle v_{sw} \rangle$ as shown in the Figure 2.21. The quantity $\langle v_{sw2} \rangle$ is local to the slave-phase loop and can be obtained as mentioned in section 2.2.4.3. Hence, only $\langle v_{sw1} \rangle$ is considered for modeling slave-phase calibration as shown in Figure 2.20.

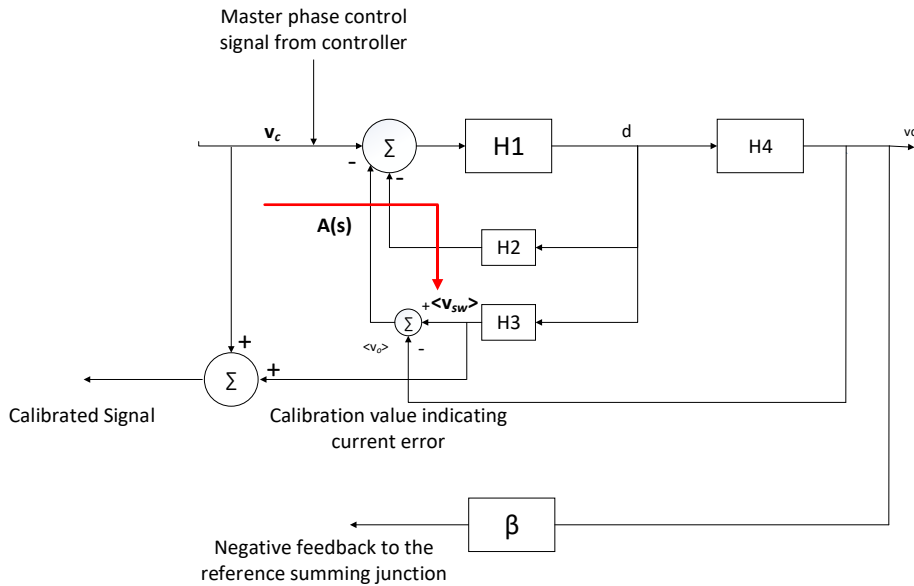


Figure 2.21 Calibration Gain

$$v_{cal} = v_{comp} + v_{comp} * A(s)$$

$$v_{cal} = v_{comp} * (1 + A(s))$$

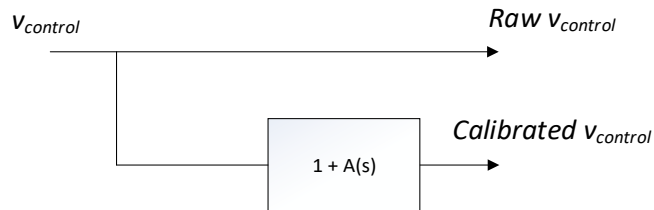


Figure 2.22 Slave-Phase Calibration

For a 2-Phase system, the gain, $A(S)$ can be obtained as

$$A(s) = \frac{H1 * H3}{1 + H1 * H2 + H1 * H3 - H1 * H4}$$

Similarly, the calibrated control signals for rest of the slaves can be obtained. The model depicted in Figure 2.23 can be used to derive the plant transfer function for a 4-phase system.

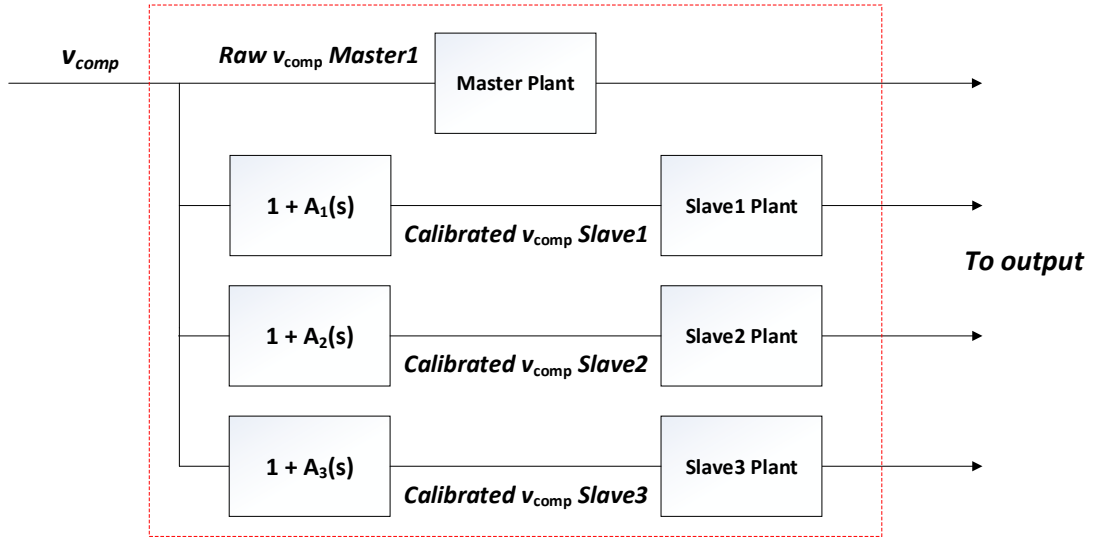


Figure 2.23 4-Phase Slave-Phase Calibration

2.2.5.1 Summary of transfer functions

Transfer Function	Description	Expression
H1	Pulse width Modulator Gain	$\frac{\tilde{d}}{v_{ctrl} - v_{average}} = \frac{C}{K_{vi} * (V_i - V_o) * T_s}$
H2	Inductor Emulator Gain	$\frac{\langle \widehat{v_{cap}}(t) \rangle}{\tilde{d}} = 2 * D * T_s * \frac{I_1 - I_2}{C}$
H3	Avg. switching node Gain	$\frac{\langle v_{sw}(s) \rangle}{d} = \frac{V_{in}}{s * (1 + as)}$
H4	Control to output relation	$\frac{v_o}{d} = V_{in} * \frac{1 + sCR_{esr}}{1 + s\left(\frac{L}{R_{Load}} + CR_{esr}\right) + s^2 * LC\left(1 + \frac{R_{esr}}{R_{Load}}\right)}$

Table 2.1 Summary of Transfer Functions

2.2.6 Controller Design

Now that all the important blocks have been derived, a consolidated transfer function for the plant is obtained using Mason's gain rule [28] for the Figure 2.24.

$$Plant = H(s) = H1 * \frac{H4}{1 - H1H2 - H1H3 + H1H4}$$

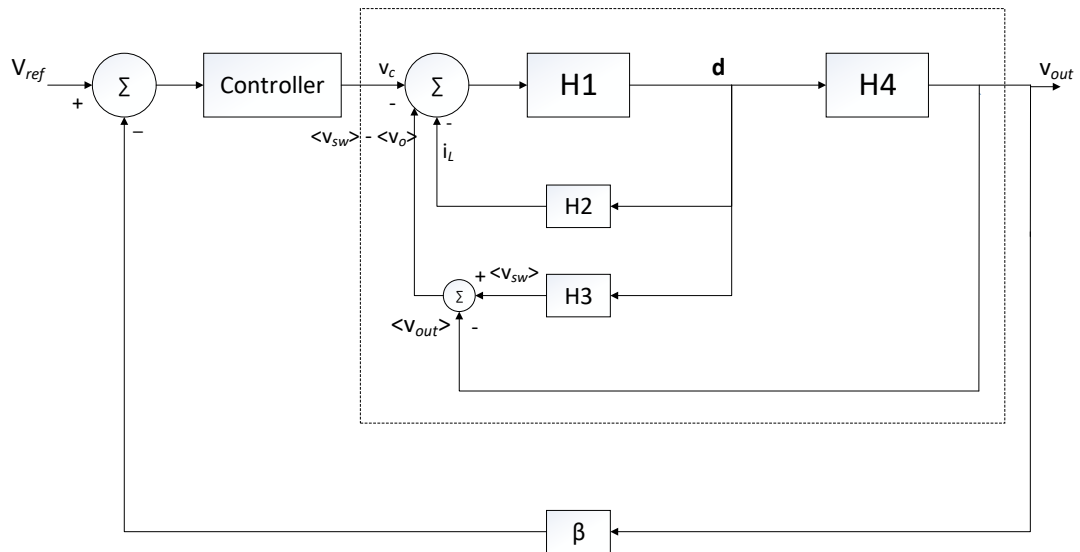


Figure 2.24 Consolidated Block Representation of Single-Phase Buck with Peak Current Mode

Pole-zero placement approach:

Having derived the plant transfer function, next step in the design procedure is to design the controller.

Design steps:

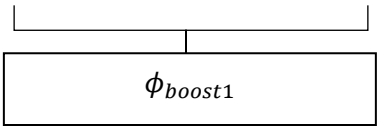
- Unity gain crossover frequency (f_{ug}) of the loop was assumed to be $\frac{f_{sw}}{10}$.
- Typically, $\frac{f_{sw}}{5} < f_{ug} < \frac{f_{sw}}{30}$. Choosing $f_{ug} < \frac{f_{sw}}{5}$ may result in an unstable system and $f_{ug} > \frac{f_{sw}}{30}$ may result in a slow transient response.

- Phase of the plant is calculated at f_{ug} .
- In this work, phase loss of the plant is found to be 172° . Phase of the loop gain at f_{ug} after accounting for the compensator pole at origin will be -262° . In order to achieve a phase margin of 60° , a phase boost of 140° is required.
- An appropriate compensator is decided based on the desired phase margin. Type III Controller is chosen based on the phase boost requirement.
- Type III compensator is a 3pole , 2zero system with the transfer function as mentioned below:

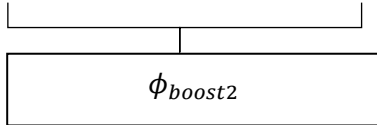
$$Controller = H_c(s) = K_c * \left(1 + \frac{s}{w_{z1}}\right) * \frac{1 + \frac{s}{w_{z2}}}{s * \left(1 + \frac{s}{w_{p1}}\right) * \left(1 + \frac{s}{w_{p2}}\right)} \quad (2.23)$$

- The poles are chosen based on the cross-over frequency and desired phase boost.
- Phase boost of the plant is given by the relation:

$$\phi_{boost} = \left\{ \tan^{-1} \left(\frac{w_{ug}}{w_{z1}} \right) - \tan^{-1} \left(\frac{w_{ug}}{w_{p2}} \right) \right\} + \left\{ \tan^{-1} \left(\frac{w_{ug}}{w_{z2}} \right) - \tan^{-1} \left(\frac{w_{ug}}{w_{p1}} \right) \right\}$$



ϕ_{boost1}



ϕ_{boost2}

- ϕ_{boost1} is the phase boost contribution by the first zero and second pole.
- ϕ_{boost2} is the phase boost contribution by the second zero and first pole.

2.2.6.1 OTA-based compensator

An OTA-based Type III compensator was designed to realize the controller transfer function obtained in equation (2.19) [31].

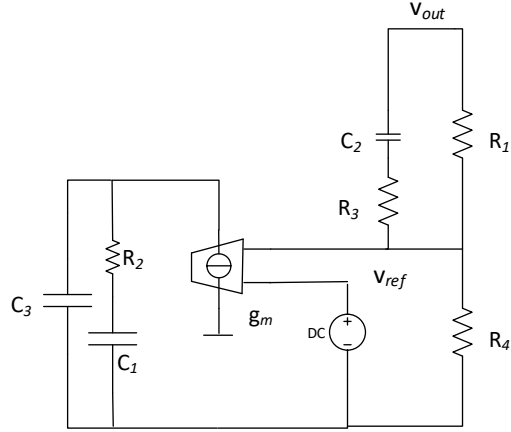


Figure 2.25 Type-III OTA Controller

The constant term and pole-zero relations can be obtained as

$$K_c = g_m * \frac{R_4}{(R_1 + R_4) * (C_1 + C_2)}$$

$$w_{z1} = \frac{1}{R_2 * C_1}$$

$$w_{z2} = \frac{1}{(R_1 + R_3) * C_2}$$

$$w_{p1} = \frac{1}{((R_1 || R_4) + R_3) * C_2}$$

$$w_{p2} = \frac{C_1 + C_3}{R_2 * (C_1 C_3)}$$

It is important to note that selection of w_{z2} and w_{p1} is constrained by the feedback factor. Assume

$$\frac{w_{p1}}{w_{z2}} = k \text{ and feedback factor, } \beta = \frac{R_4}{R_1 + R_4}.$$

Expressing w_{p1} as $\frac{1}{(\beta * R_1 + R_3) * C_2}$, we obtain the following relation

$$\frac{R_1}{R_3} = \frac{k - 1}{1 - \beta k}$$

For acceptable values of R_1 and R_3 , $1 < k < \frac{1}{\beta}$. Since $k_{max} = 1/\beta$, the selection of second zero and first pole is constrained by the feedback factor.

2.2.6.1.1 Bode plot of Plant Transfer Function

Bode plot of the consolidated plant transfer function was plotted to obtain the phase loss information at the cross-over frequency. This information is important to design a controller.

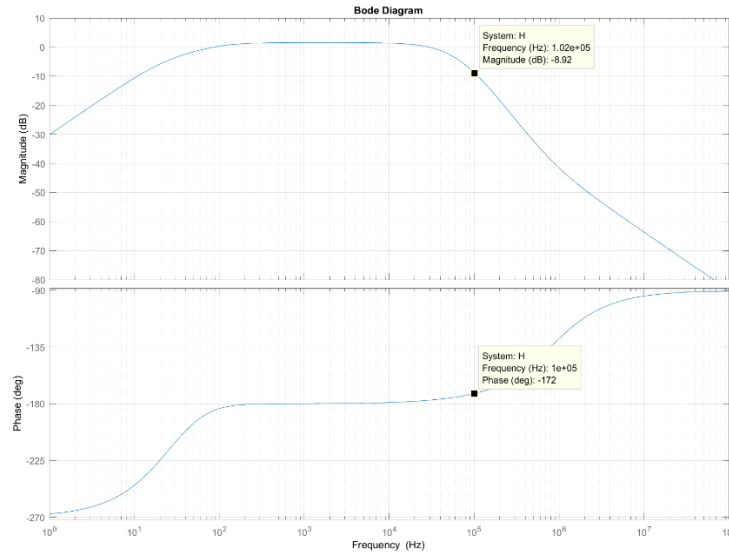


Figure 2.26 Bode Plot of Plant

The phase loss of the plant as observed from the figure above is 172° . Hence, a type III controller must be designed to compensate for the phase loss and to achieve a phase margin of 50° . To achieve a phase boost of 140° , poles and zeros must be chosen accordingly. Mentioned below is the table containing Controller values.

Controller Parameter	Value
Crossover frequency, w_{ug}	100KHz
K_c	2.2338e5
First zero location, f_{z1}	8KHz
Second pole location, f_{p2}	1.2MHz

ϕ_{boost1}	80.65°
Second zero location, f_{z2}	30KHz
First pole location, f_{p1}	400KHz
ϕ_{boost2}	59.26°
ϕ_{boost}	140°

Table 2.2 Controller Parameters

2.2.6.1.2 Bode plot of Controller Transfer Function

A controller was modelled after all its parameters were obtained. Figure 2.27 depicts the bode plot of the controller transfer function. High gain and a phase boost of 140° at the w_{ug} can be observed.

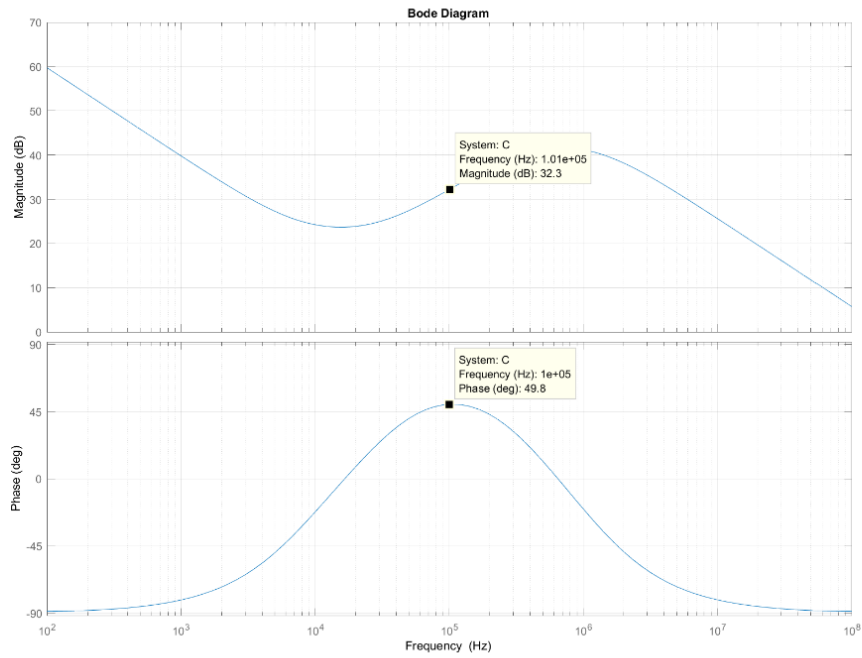


Figure 2.27 Controller Bode Plot

2.2.6.1.3 Bode plot of Loop gain

To verify the compensator block, bode plot of the loop gain of the system was obtained and phase and gain at w_{ug} were noted. Phase loss of 130° indicates a phase margin of 50° and unity gain at the cross-over frequency.

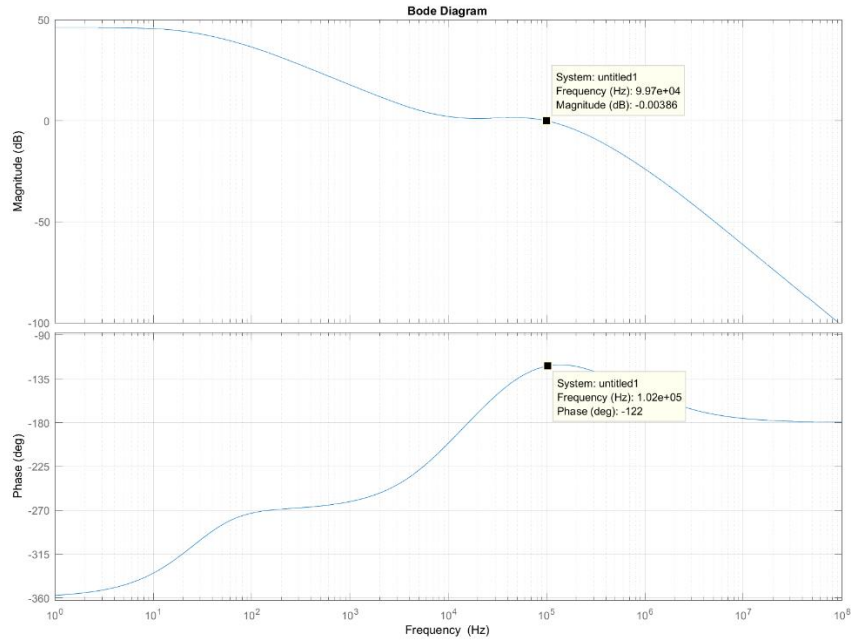


Figure 2.28 Bode Plot of Loop Gain

With the Controller transfer function obtained, an OTA-based type III compensator as explained in 2.2.6.1 is designed. The R and C values are determined based on the Compensator design procedure detailed in [31]. A Single-Phase Buck Converter with the controller is implemented in both PLECS (ideal components) and Cadence(Transistor schematic) and the results are compared as detailed in Chapter 4. Table below lists the controller components used for PLECS and Cadence simulations. It can be observed that there was a minor deviation in the controller values used for Spectre simulations.

Controller Component	PLECS	Spectre
G_m	100uS	100uS
R_1	1.4M Ω	1.4M Ω
R_2	3.3M Ω	3.25M Ω
R_3	12.6K Ω	12.6K Ω
R_4	100K Ω	100K Ω
C_1	6pF	6pF
C_2	3.75pF	3.75pF
C_3	40fF	75fF

Table 2.3 Compensator component values

2.2.7 System Model

The model in Figure 2.29 depicts the entire 4-Phase Buck Converter. Error 1,2,3 are difference of master-phase and individual slave-phase currents respectively. Current Sense model is illustrated in Figure 2.30.

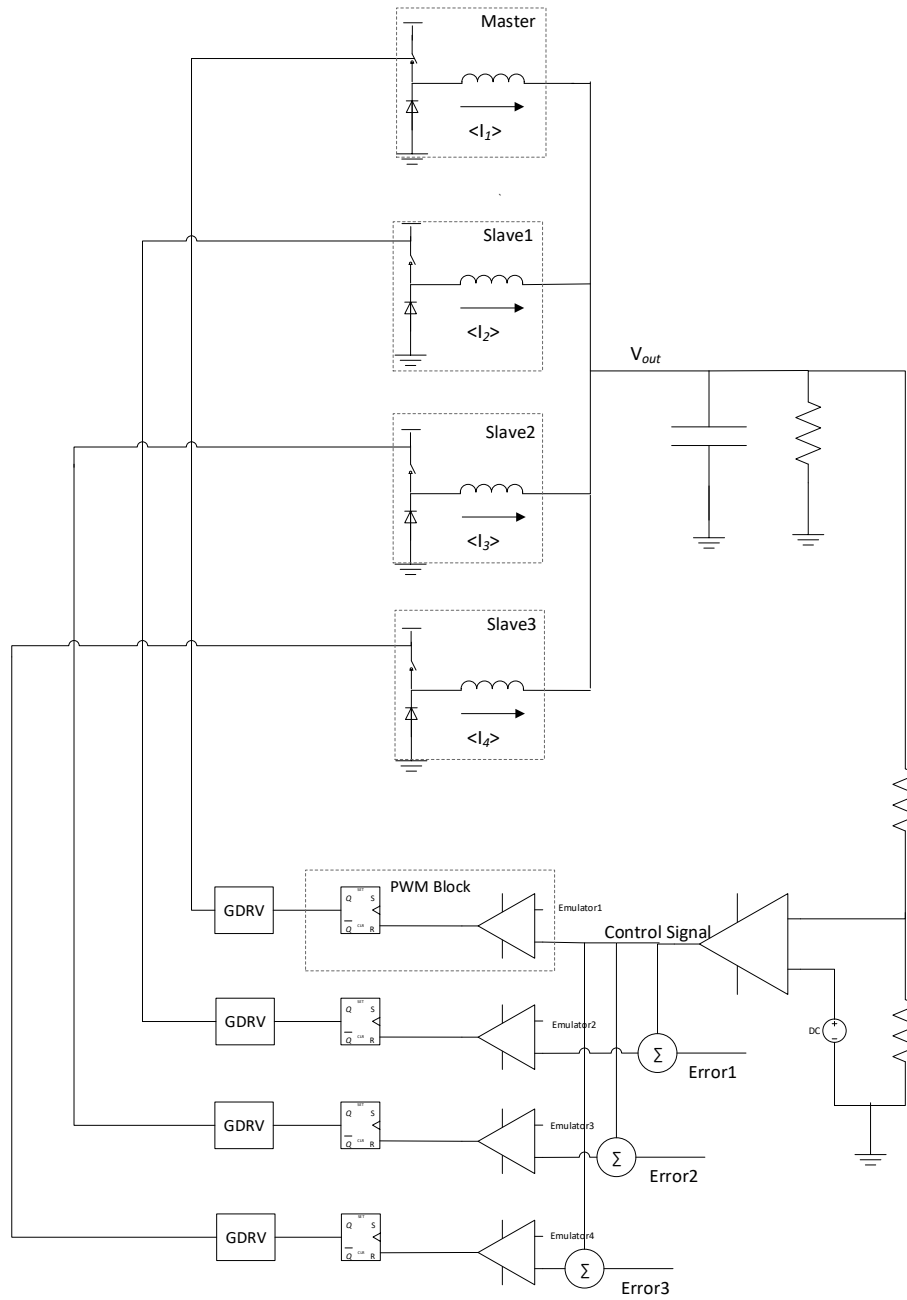


Figure 2.29 4-Phase Buck Converter with Current Sharing scheme

2.2.7.1 Inductor Emulator Block

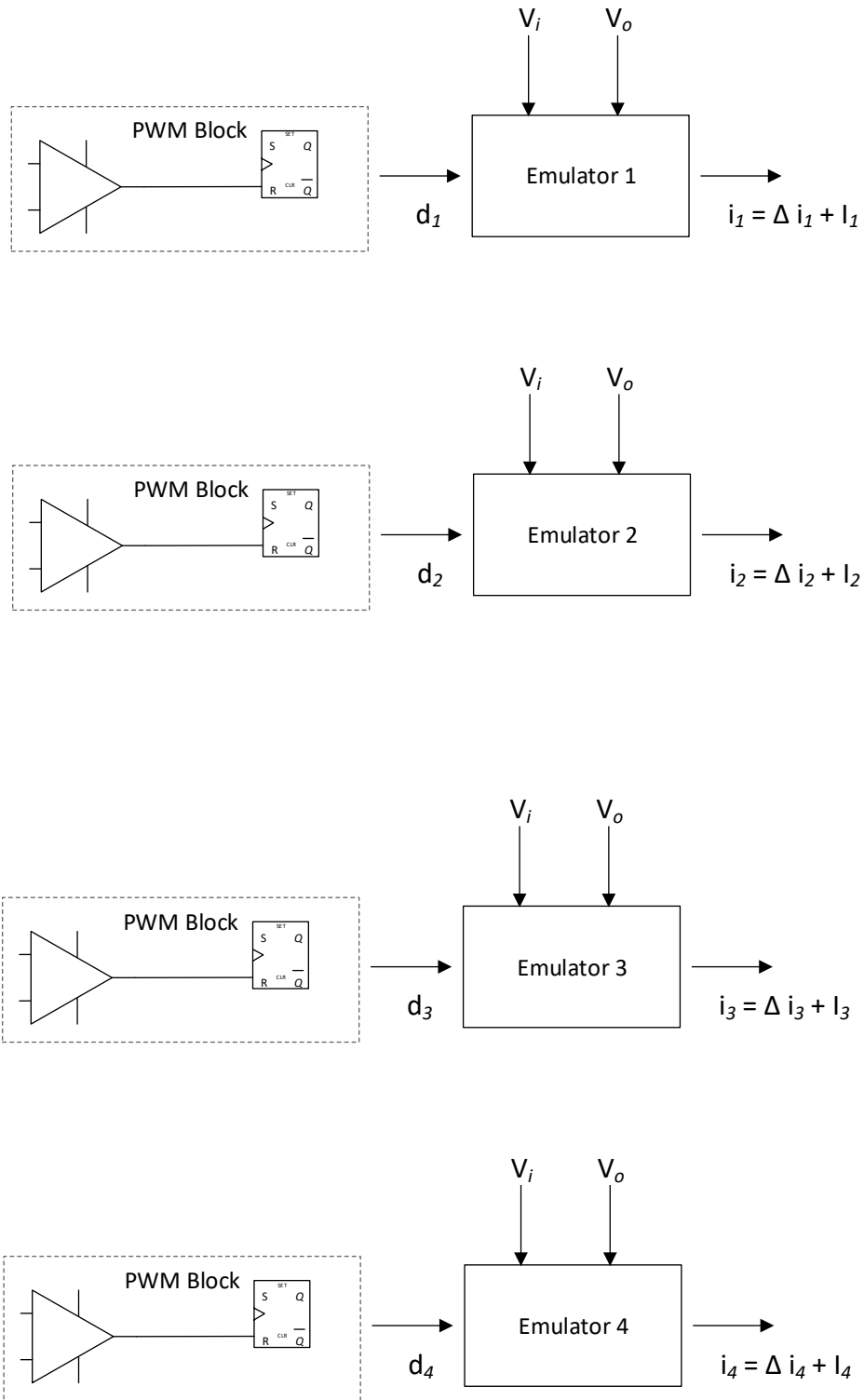


Figure 2.30 Current Sense Block

2.2.8 System and Component Specifications

System Specifications		
V_{in}	Input Supply	5V
V_{out}	Desired Output Voltage	1.8V
I_{out}	Max. Load Current (4-Phase)	8A
F_{sw}	Switching Frequency	2MHz
Component Values		
$R_{on,pmos}$	R_{ds} of PMOS FET	120m Ω
$R_{on,nmos}$	R_{ds} of NMOS FET	90m Ω
L	Filter Inductance	3 μ H
DCR	DC Resistance of Inductor	5m Ω
C	Output Capacitor	10 μ F
ESR	Effective Series Resistor	20m Ω

Table 2.4 System Specifications

CHAPTER 3

CIRCUIT IMPLEMENTATION

The model is implemented in tsmc250nm process using 5V devices. The building blocks of the proposed 4-Phase Buck Regulator are recognized as shown in the Figure 3.1.

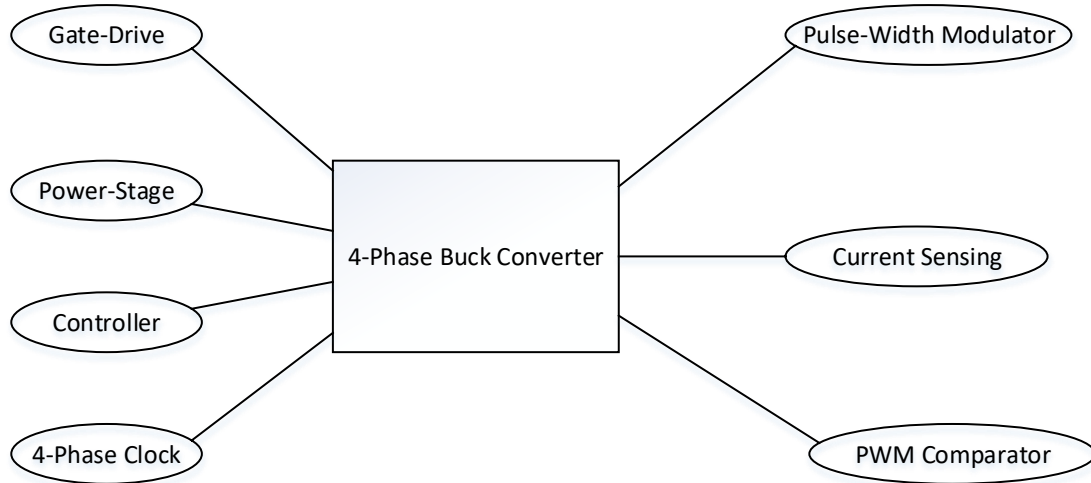


Figure 3.1 System Model of a Multi-Phase Buck Converter

3.1 Power-Stage

The power stage representing PWM switch consists of PMOS and NMOS powerFETs as shown in Figure 3.1. The power switches are sized according their $R_{ds,on}$ requirements. The $R_{ds,on}$ of the PMOS and NMOS FETs of the proposed work is 120m Ω and 90m Ω respectively.

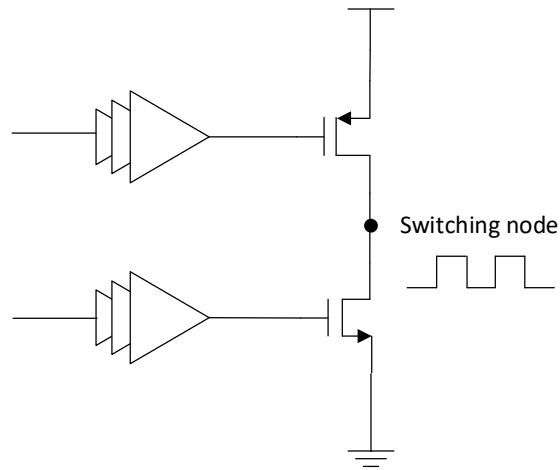


Figure 3.2 Gate-Driver and PowerFETs

3.2 Gate-Drive

A gate drive circuit is designed to drive the power FETs. A large current is required to charge this capacitance in a very short time. Conventional buffer based drivers suffer from a short-circuit power loss since both the power switches are ON for a short interval [36]. [29] proposes a modified gate-driver circuit with deadtime control to prevent short-circuit power losses. A delay is introduced between the turn on instants of PMOS and NMOS power switch. In other words, both the power switches are off for a short interval due to the dead-time circuitry.

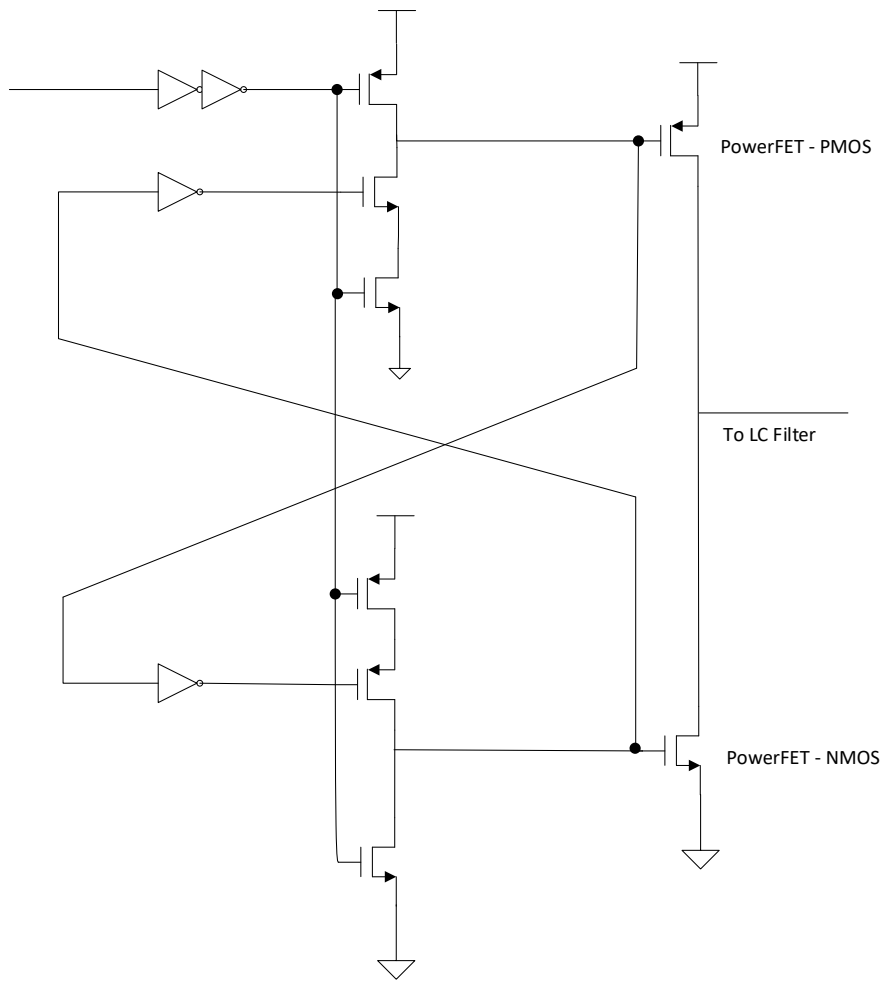


Figure 3.3 Gate-Drivers with deadtime control

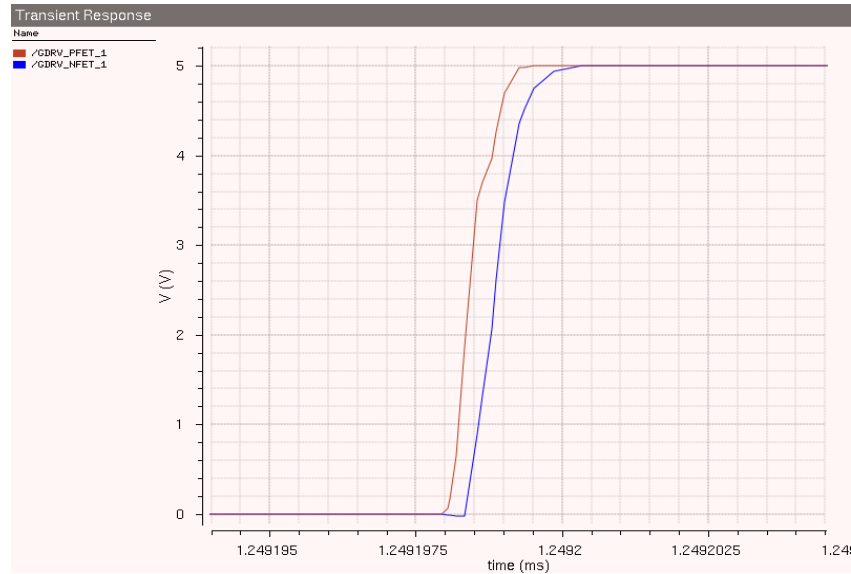


Figure 3.4 GDRV circuit waveform

3.3 Pulse-Width Modulator

A pulse width modulator based on the Phase-Frequency detector(PFD) circuit is realized [30]. A D-Flipflop with a reset functionality forms the core circuit of a PFD. The main idea is to set the flipflop at every rising edge of the clock and reset it when the signal at Reset pin goes high. This feature can be used to realize a PWM circuit for peak current mode control. Reset pulses are generated by the comparator when the inductor current equals control signal. This signal resets the flipflop which results in turning off of top power switch and ramping down of inductor current [6]. The comparator is implemented using a Voltage Controlled Voltage Source(VCVS) with an open-loop gain of 75dB and propagation delay of 15ns.

A D-Flipflop with reset functionality can be realized using 2 SR latches as shown in Figure 3.5. The rising edge at Clock pin sets the flipflop and a reset pulse generated by the comparator resets the flipflop.

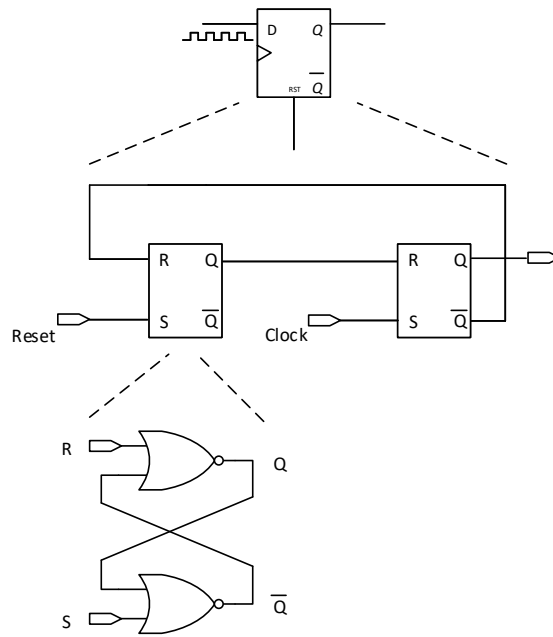


Figure 3.5 Pulse-width Modulator

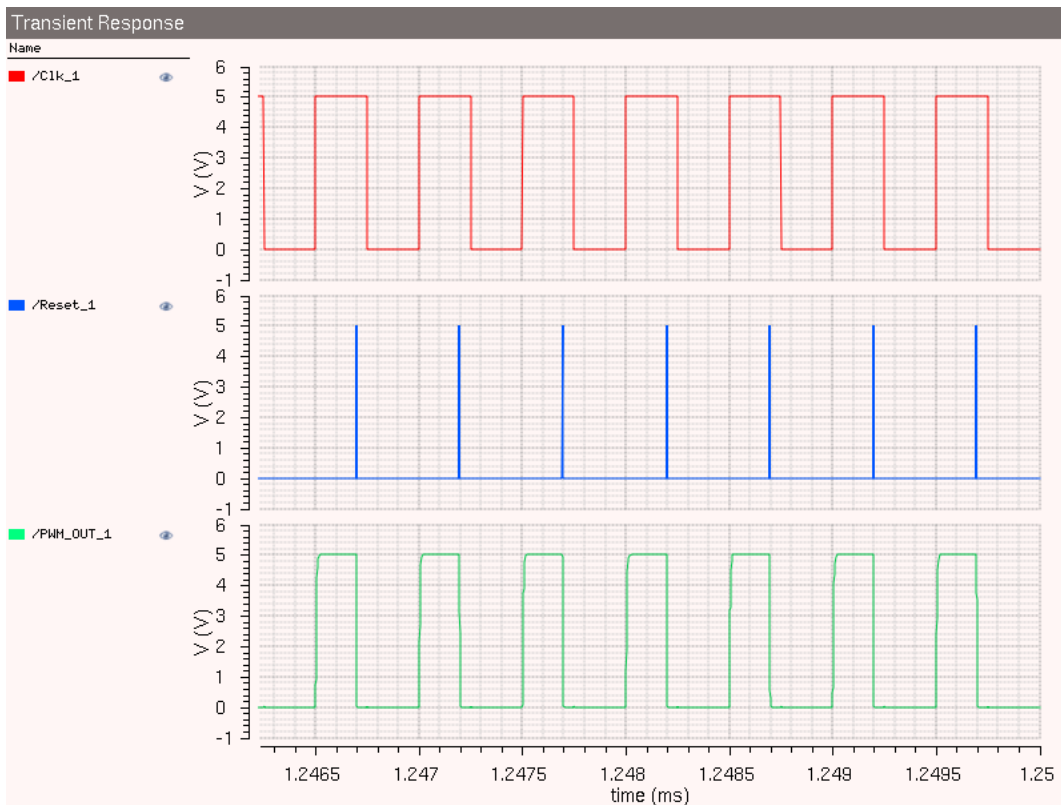


Figure 3.6 PWM Circuit Waveform

3.4 Current Sensing Block

The inductor emulator circuit generates a voltage signal representative of peak and average inductor currents. [19] proposes an emulator circuit for inductor multiplier purpose which replicates the inductor current ripple. For peak current mode control, both the ripple and average component of inductor current are required. Assuming the op-amp has a high enough gain, a current of magnitude $\frac{V_{in}-V_{out}}{R}$ is generated in the current-setting branch. Resistance R is chosen according to the emulator equation (2.5). This current is then mirrored to the emulator capacitor through cascode current mirrors. A switch across this capacitor is turned on at the instant capacitor voltage equals the control signal generated by the external controller. Thus, voltage across this capacitor resembles that of an inductor current. V_{avg} represents the voltage signal representative of average inductor current which is generated by the DCR sensing block as discussed in section 2.1.2.

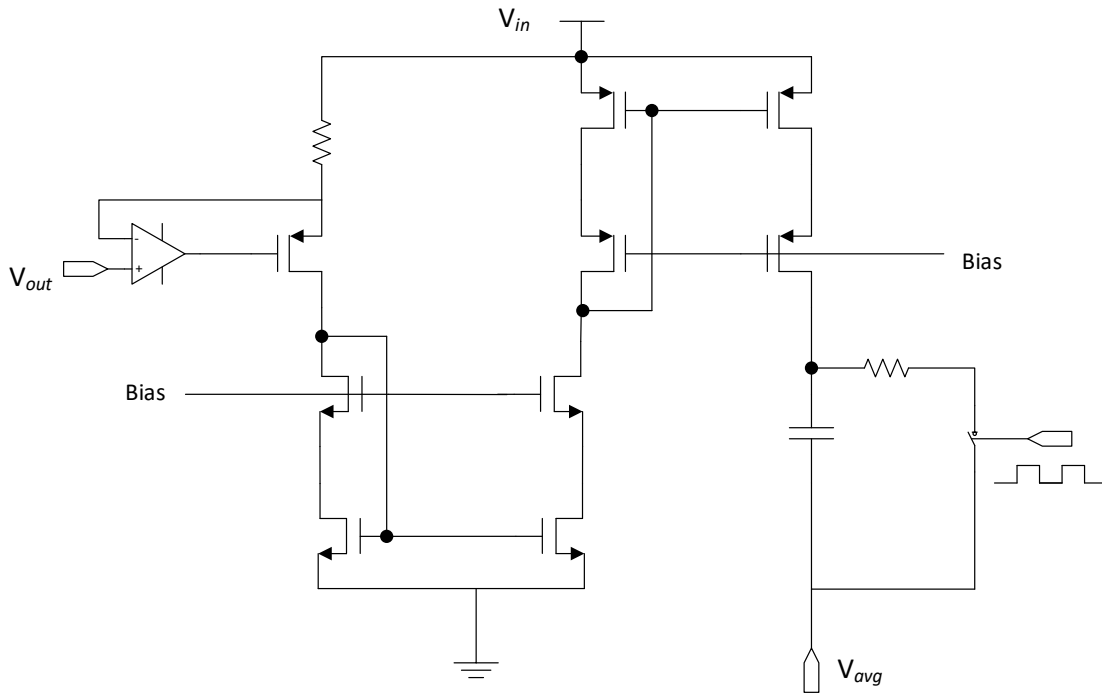


Figure 3.7 Inductor Emulator with both peak and average components

A PMOS input Telescopic cascode topology is implemented for the amplifier. PMOS input is chosen to ensure that the input pair is in saturation when driving a PMOS FET load. The schematic and

AC response are shown in Figures 3.7 and 3.8. DC Gain of 80dB, (Unity-gain Bandwidth) UGBW of 12 MHz and a Phase margin of 62° are obtained.

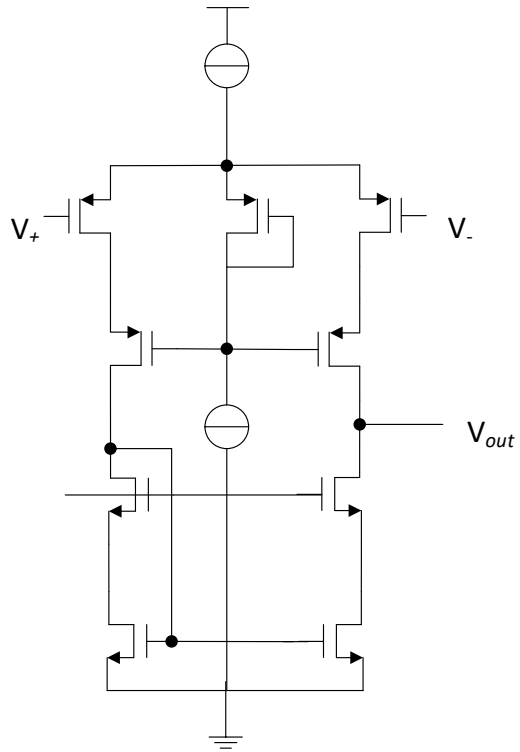


Figure 3.8 PMOS input Telescopic Cascode

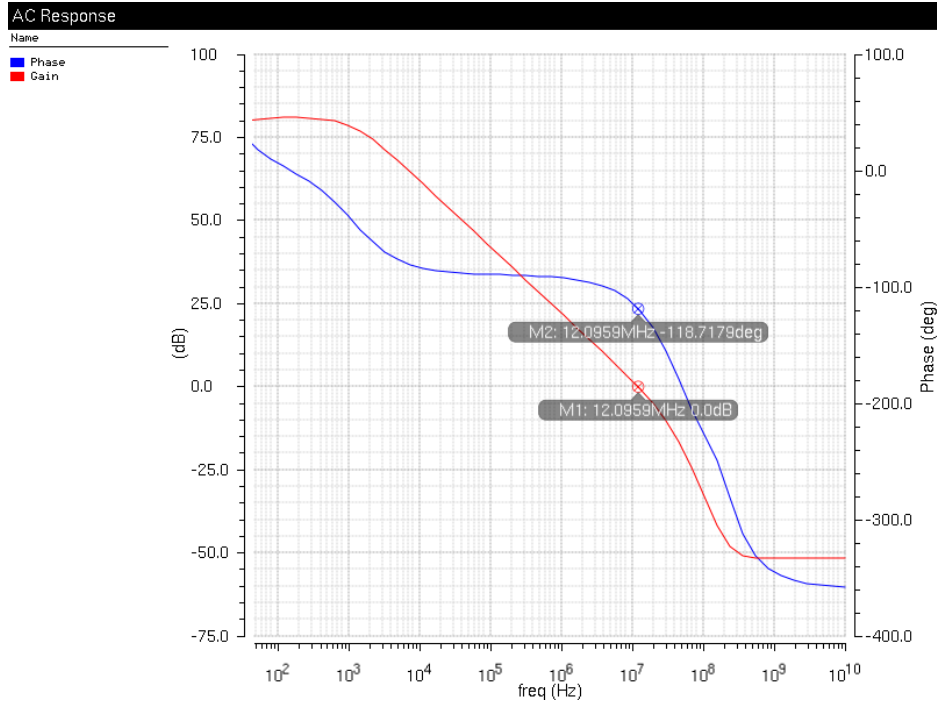


Figure 3.9 AC response of amplifier in the current sense block

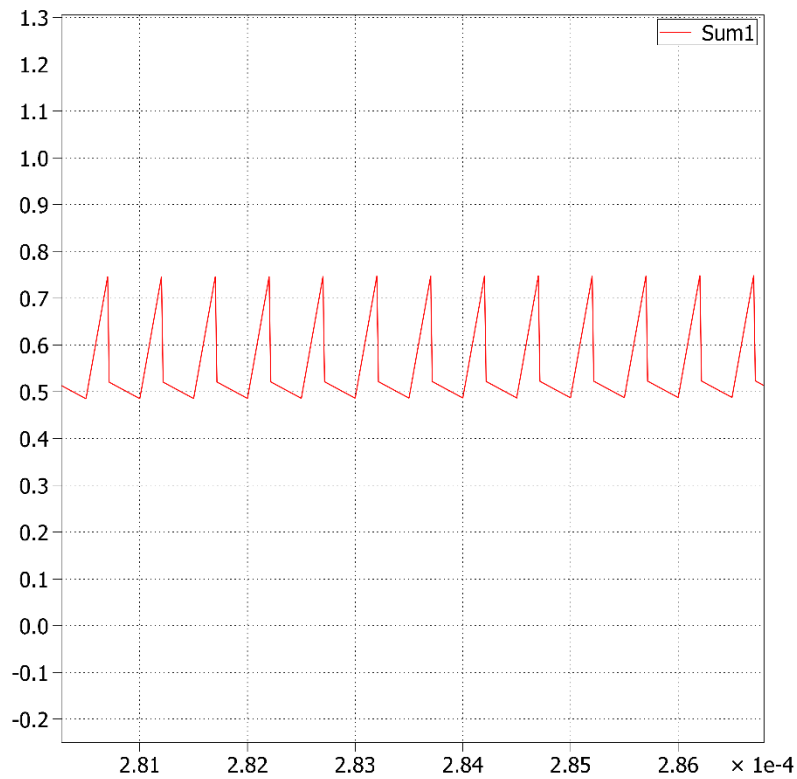


Figure 3.10 PLECS Simulation of Inductor Emulator using Ideal Components

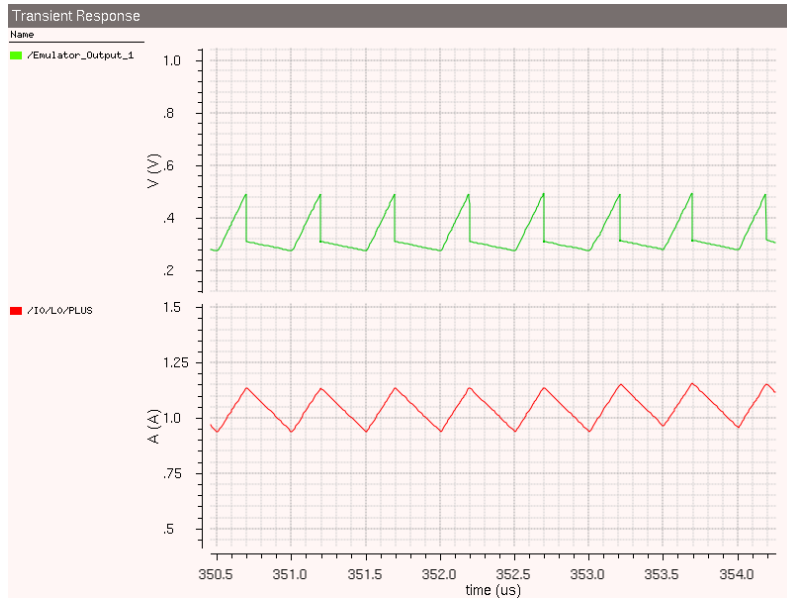


Figure 3.11 Spectre Simulation of Inductor Emulator using Non-ideal components

3.5 4-Phase Clock Generator

A 4-Phase clock circuit required for the proposed 4-Phase Buck regulator is designed as shown in Figure 3.12. An XOR gate is used to generate a 90° phase shifted clock. An Inverter is used to generate a 180° phase shifted clock. A Verilog model was used to realize the frequency divider.

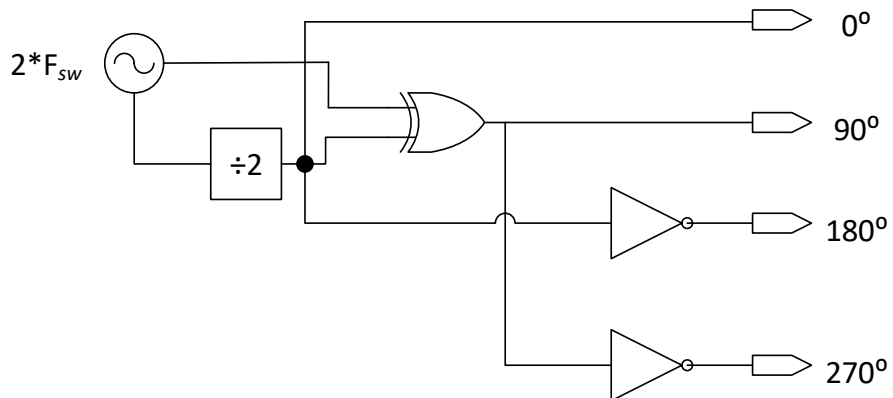


Figure 3.12 4-Phase Clock Generator

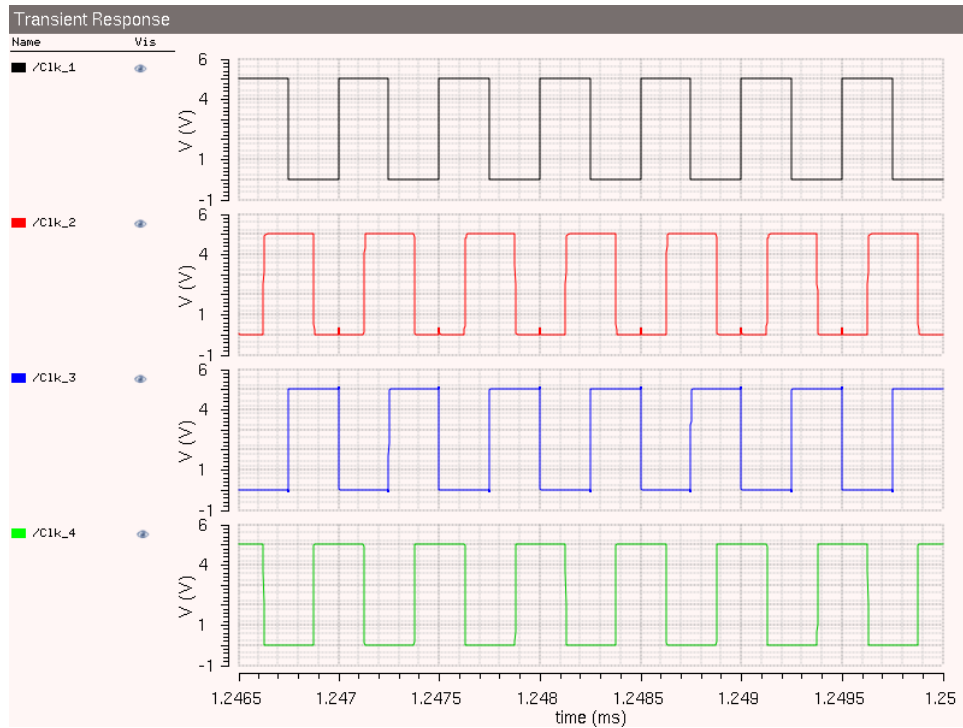


Figure 3.13 4-Phase Clock Generator Output

3.6 Controller

An OTA based compensator is designed to realize the type III compensator transfer function. An ideal Voltage Controlled Current Source (VCCS) is used to model an OTA. Controller components as derived in section 2.2.6 are used.

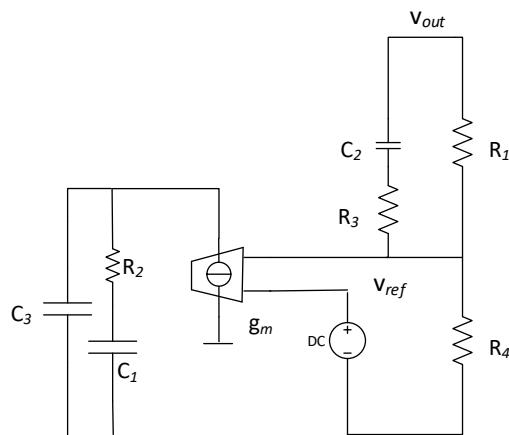


Figure 3.14 Type-III OTA-based Controller

3.7 Slave-Phase Calibration

A Master-Slave current sharing approach is implemented where all the slave-phases follow a single Master-phase. Eventually, in this process the current is shared between the master and individual slave-phases [8][9][10][12]. Presence of mismatches among the individual phases affects current sharing. Slave-phase calibration is implemented to improve the current sharing accuracy. In this scheme, master and each slave-phase average current error is used to calibrate individual slave-phase control signal [12]. The error and control signals originally in the voltage domain are converted to currents and added in the current domain. This current is sensed across a resistor situated at the tail of an OTA to get a calibrated control signal which serves as reference to individual slave-phases. A PMOS input amplifier for V-to-I converter, as explained in section 3.4 is implemented. A VCVS is used for implementing error block.

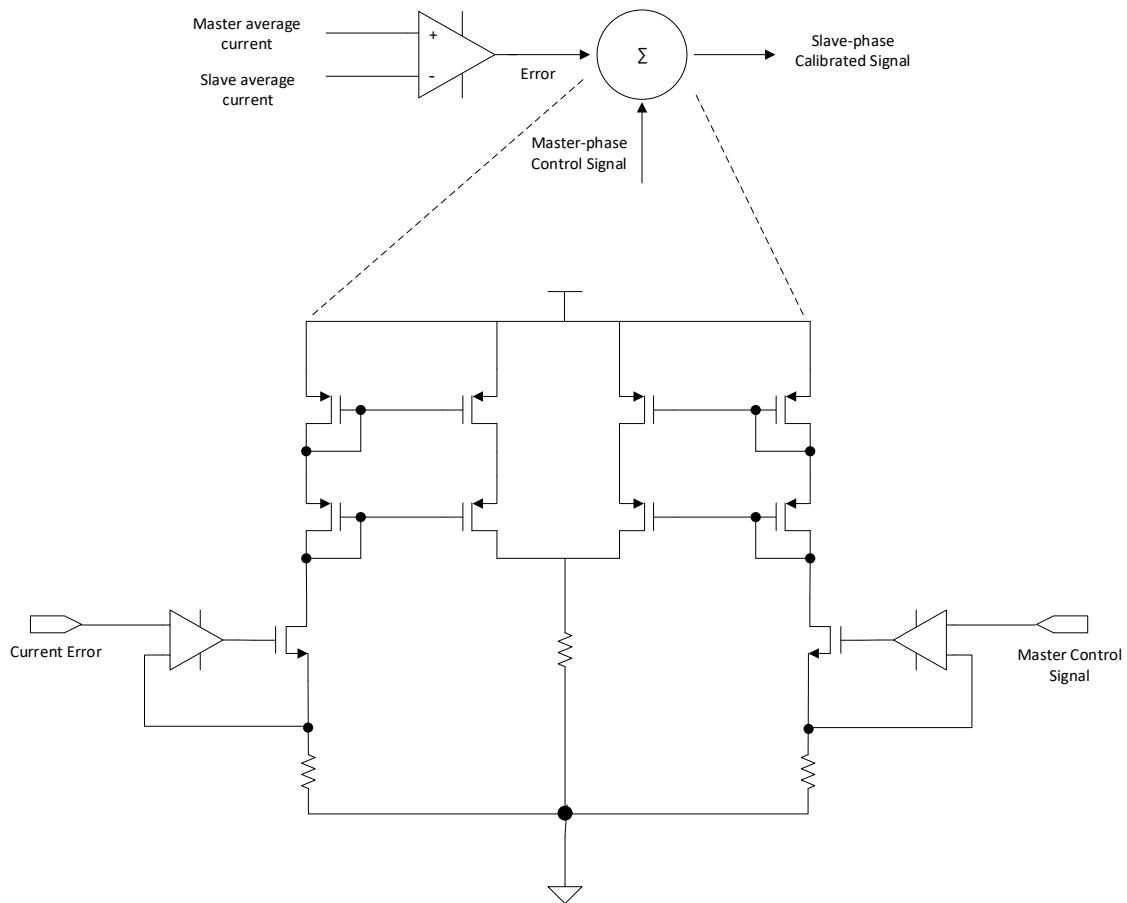


Figure 3.15 Slave-Phase Calibration Implementation

3.8 Peak Current-mode operation

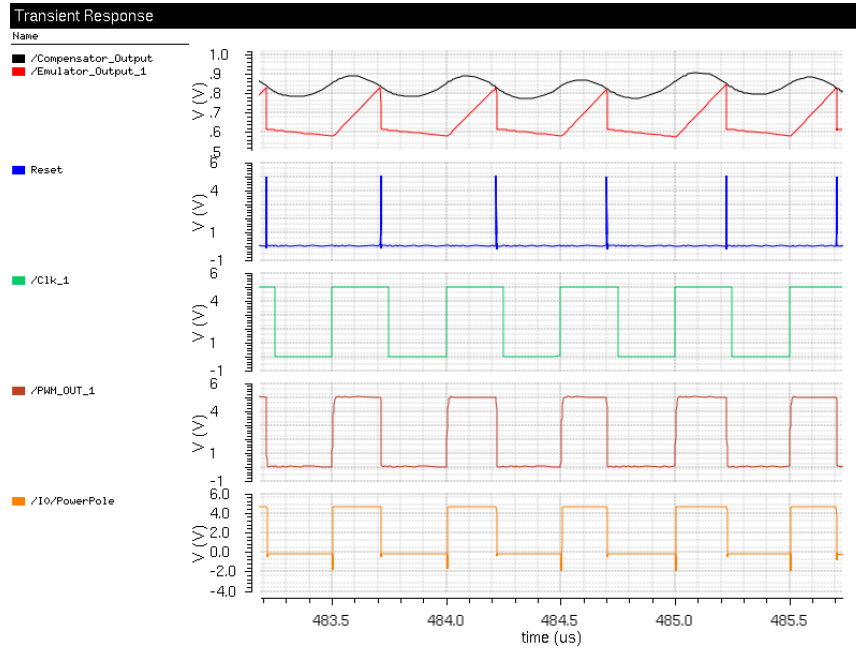


Figure 3.16 Peak Current mode Control waveforms

Figure above depicts consolidated waveforms of peak current mode operation. Reset pulses are generated at the instant replicated inductor current is compared with the control signal. This action resets the flip-flop which turns off the power FET.

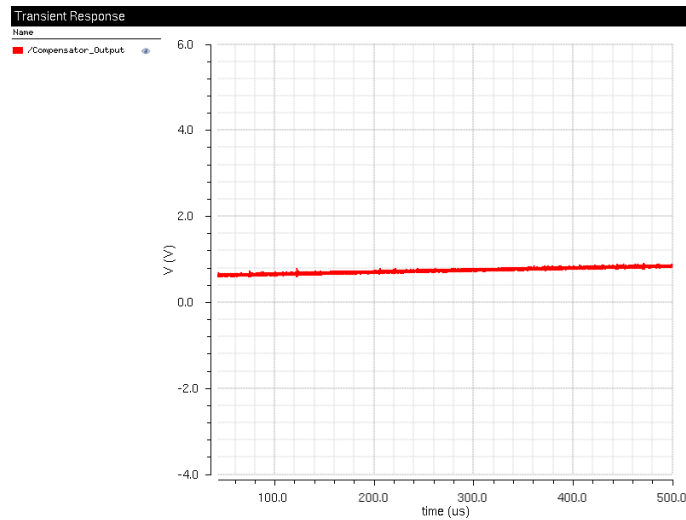


Figure 3.17 Control signal transient simulation

Zoomed out picture of control signal indicating that the high frequency ripple component is attenuated.

CHAPTER 4

SIMULATION RESULTS

4.1 Single-Phase

4.1.1 Load Transient Response - V_{out}

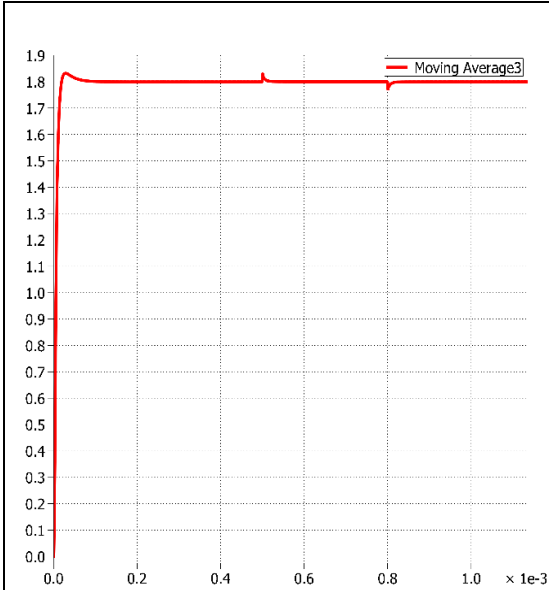


Figure 4.1 Output voltage of Single-phase Buck simulated in PLECS

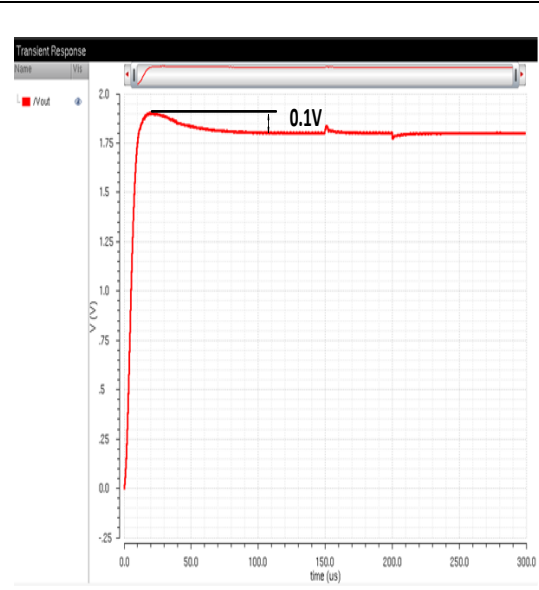


Figure 4.2 Output Voltage of Single-phase Buck simulated in Spectre

PLECS simulation showing start-up transient and load step response

Spectre simulation in agreement with PLECS results

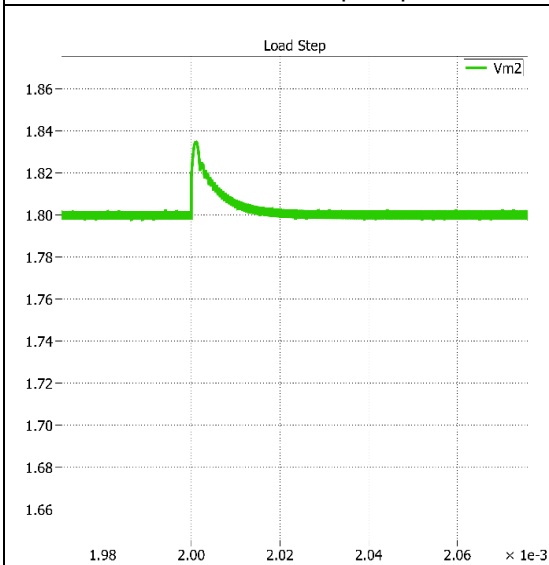


Figure 4.3 Overshoot value as seen through PLECS simulations

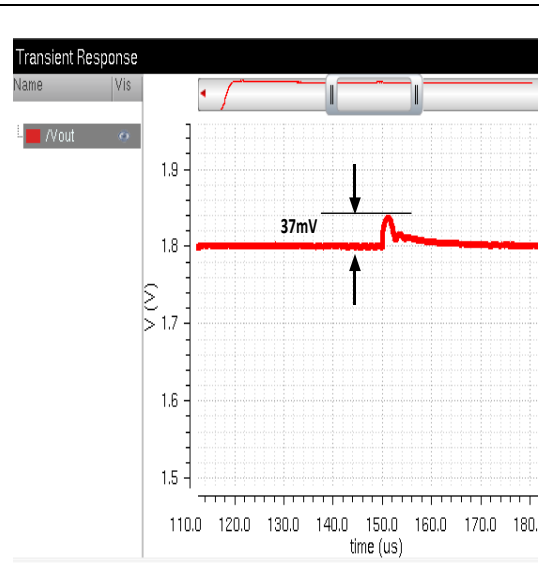


Figure 4.4 Overshoot value as seen through Spectre simulation

Overshoot value of 34mV for a load step of 1.1A – 50mA

Overshoot value of 37mV in close agreement with PLECS result

4.1.2 Load Transient Response – Inductor Current

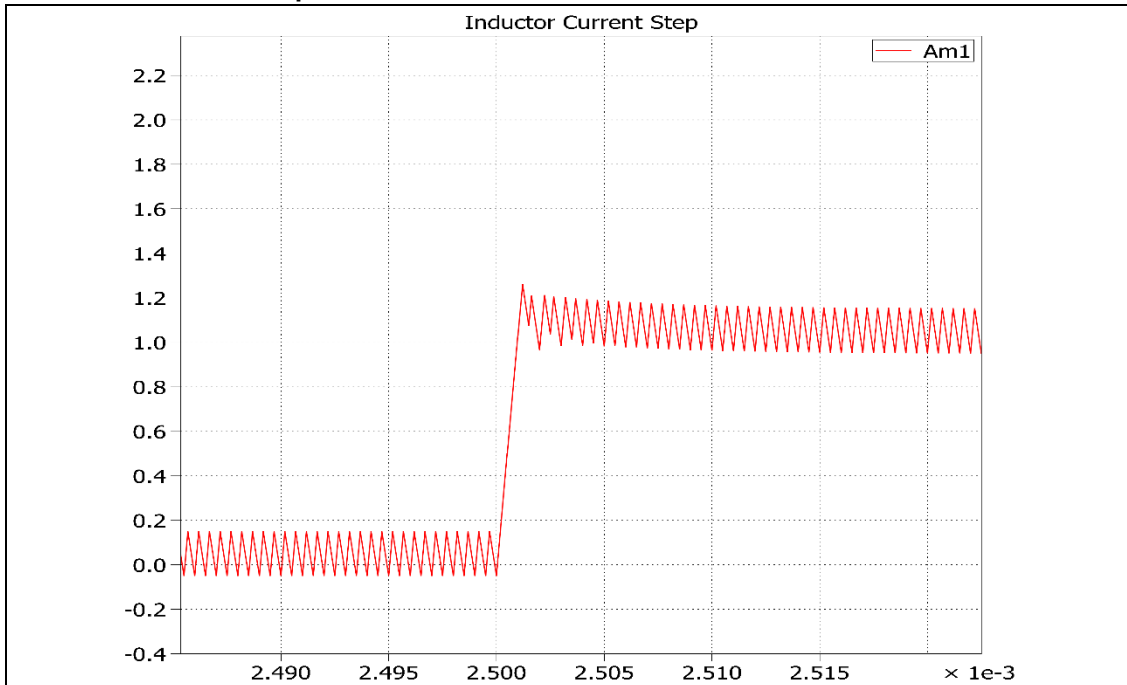


Figure 4.5 Inductor current response to a load step in a Single-Phase Buck as simulated in PLECS

Inductor response to a load step from 1A to 2A

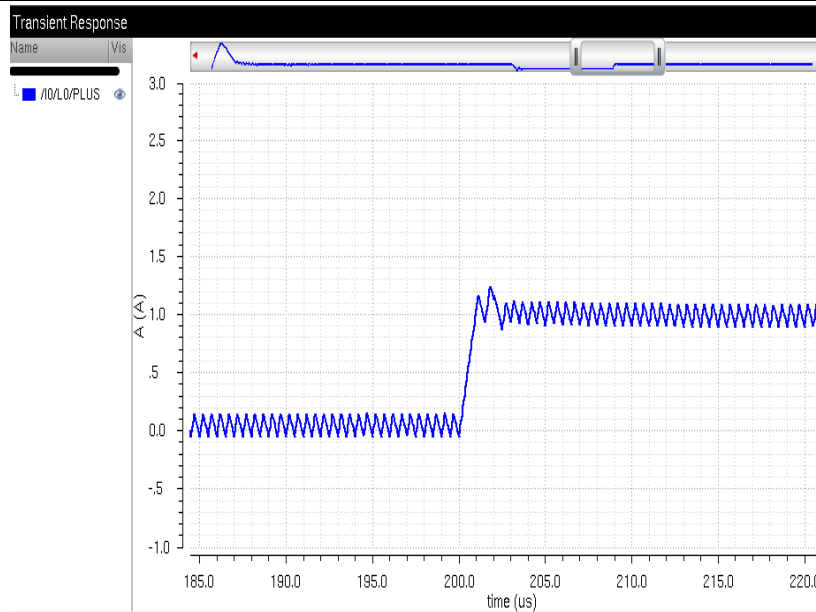


Figure 4.6 Inductor Current response as observed through Spectre Simulations

Inductor current overshoot and settling time obtained through Spectre simulation nearly equal to that of PLECS.

4.1.3 Reference Step Response - V_{out}

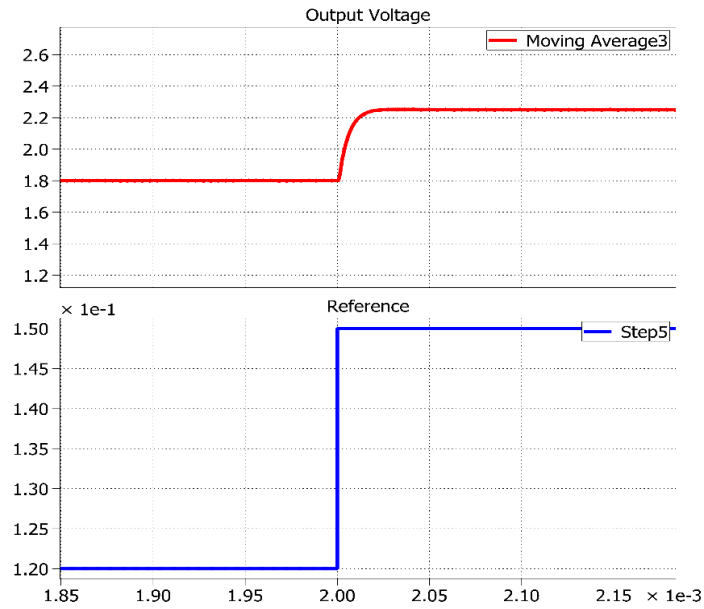


Figure 4.7 PLECS response of the single-phase Buck Converter to a step in the reference voltage

Output voltage response to a step in V_{ref} as obtained through PLECS simulation. This shows a first order settling of the closed-loop system.

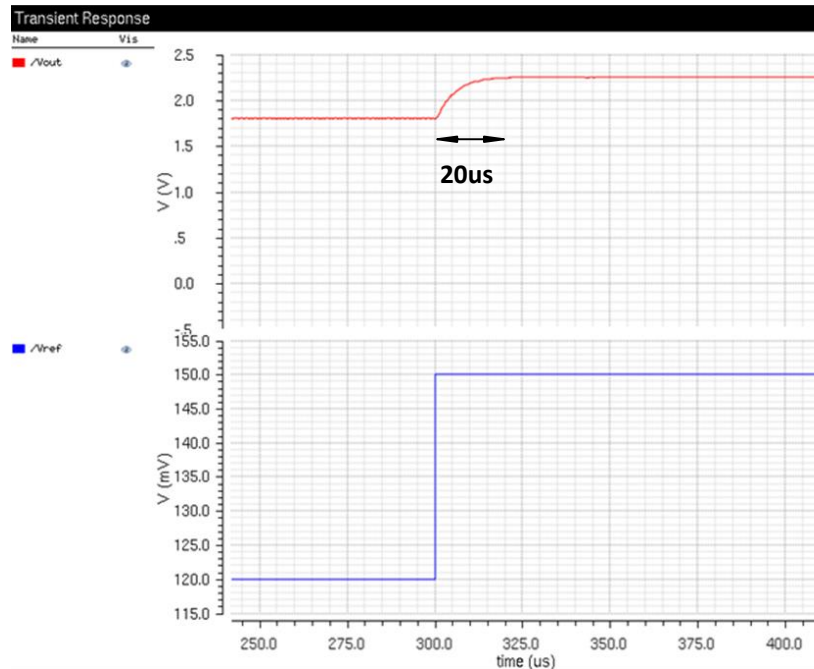


Figure 4.8 Spectre response of the single-phase Buck Converter to a step in the reference

Output voltage response to a step in V_{ref} as obtained from Spectre simulation. The settling time and nature of the response nearly match that of PLECS.

4.1.4 Line Rejection

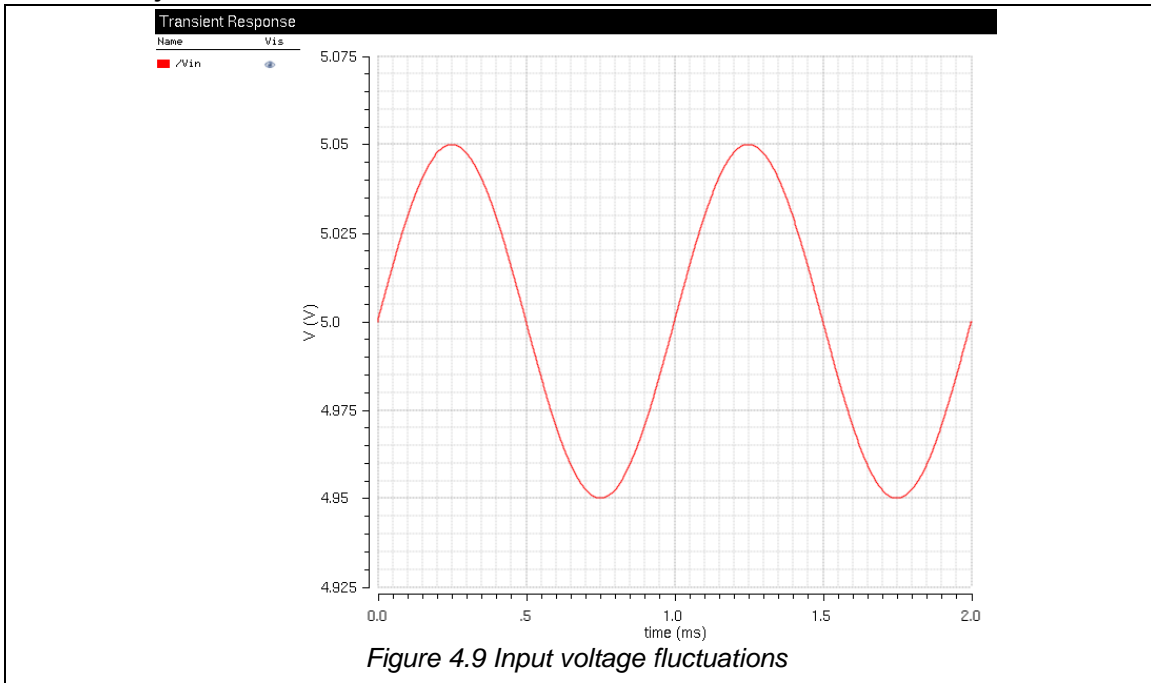


Figure 4.9 Input voltage fluctuations

Figure above depicting line disturbances (Input Voltage)

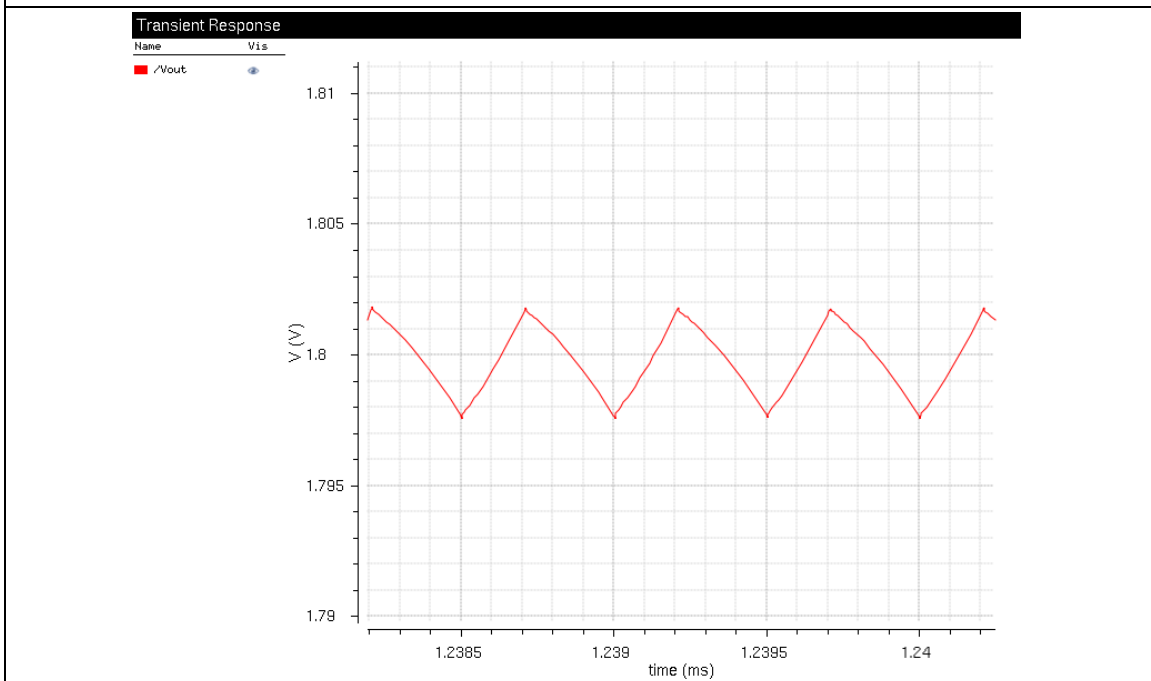


Figure 4.10 Output voltage response to line fluctuations

Figure above depicting attenuation of line disturbances at the output.

4.1.5 Inductor-Emulator mismatch

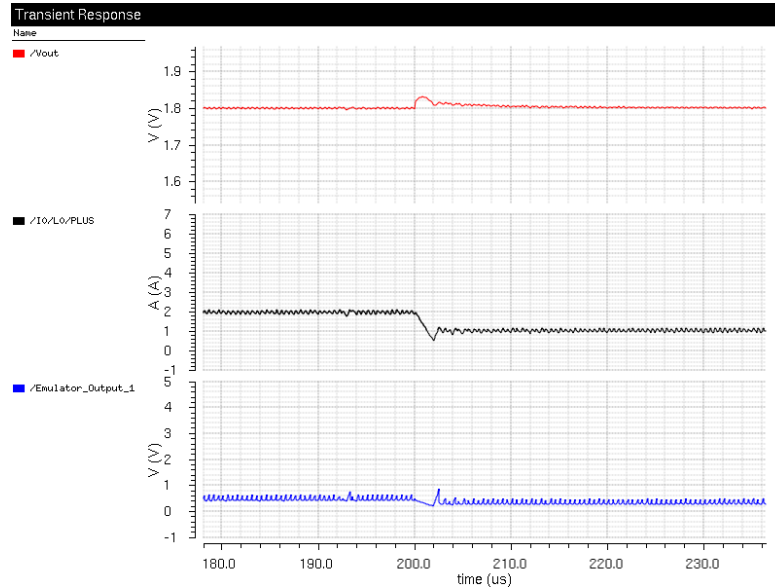


Figure 4.11 Load step response in a Single-Phase Buck with 20% mismatch between power-stage inductor and emulator

Figure above depicts the load step response of the converter with a 20% mismatch between the inductor and emulator blocks. It can be observed that the system responds well to the transients in the presence of mismatches.

4.1.5.1 Component variation analysis

It is a challenging task to accurately replicate the inductor current as the Emulator can't track the Inductance. Hence, there will be mismatches between the slopes of inductor current and the replicated voltage (across emulator capacitor). The converter has been simulated in the presence of R_{dcr} , R_{emu} and C_{emu} variations from the ideal values and the results have been represented in the figures below.

Ideal component values:

$$R_{dcr} = 5m\Omega, R_{emu} = 300K\Omega, C_{emu} = 10pF, L = 3\mu H$$

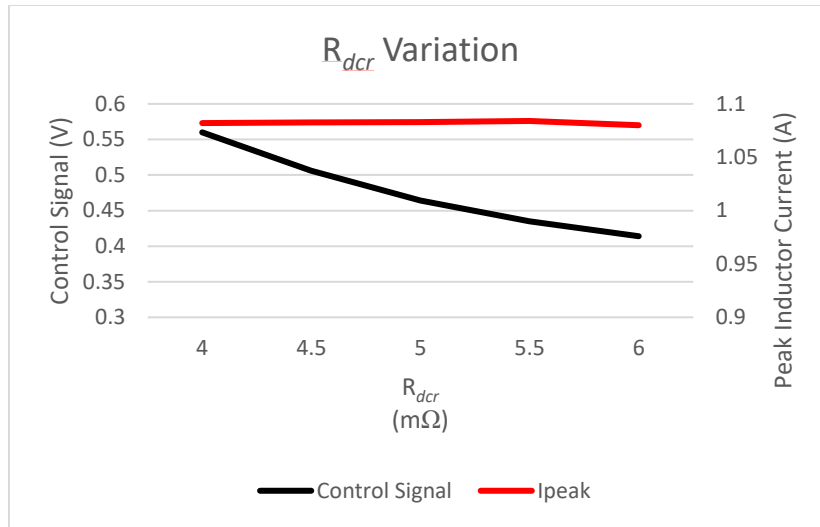


Figure 4.12 Control Signal and I_L peak variation with R_{dcr} variation

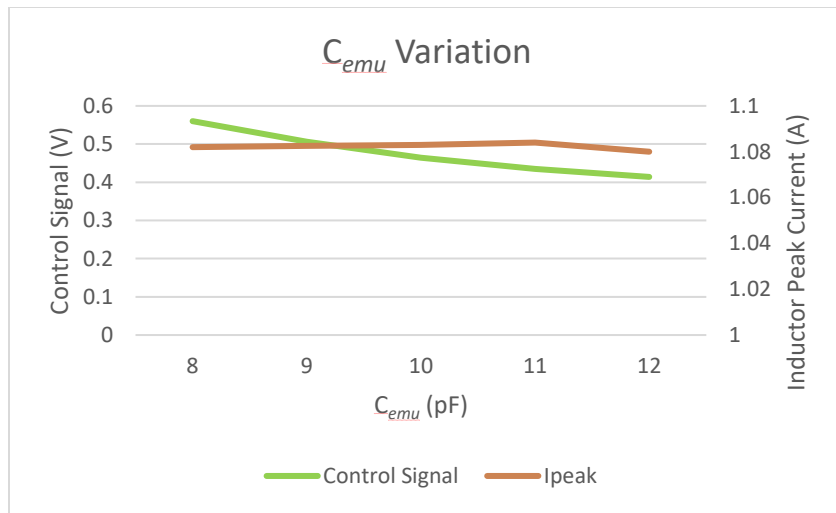


Figure 4.13 Control Signal and I_L peak variations with C_{emu} variations

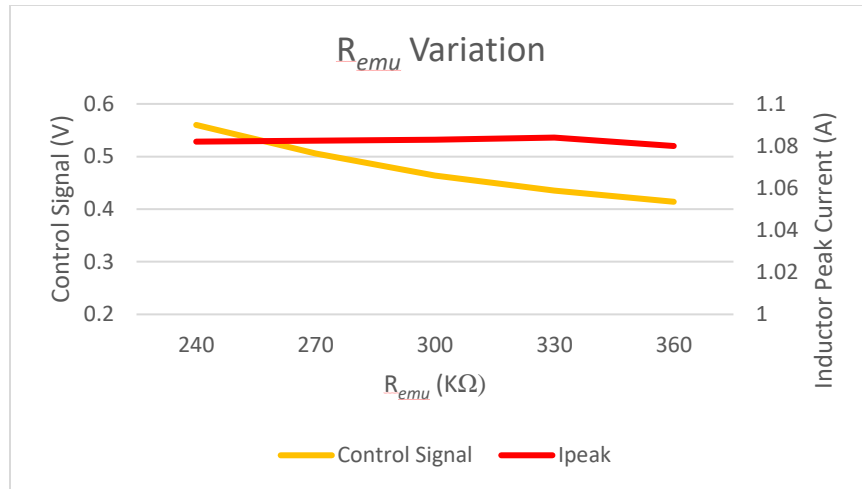


Figure 4.14 Control Signal and I_L peak variations with R_{emu} variations

Considering Fig. 4.12, R_{dcr} was varied from 4m Ω to 6m Ω against the ideal value of 5m Ω . The control signal and inductor peak current were observed. In all the cases, it was noted that the compensator adjusted the control signal so as to obtain a peak inductor current corresponding to the load. A similar trend can be observed in Figures 4.13 and 4.14.

4.1.6 Discussion

A single-phase Buck Converter based on the model designed in PLECS. Ideal components with parasitic resistances are included for PowerFETS, Inductor, Output Capacitor to make the model more informative. This circuit is simulated with the controller components as obtained in 2.2.6.

The PLECS circuit is verified through transistor level design in Virtuoso and simulations in Spectre. Load, Line transients and Reference step responses of Output voltage and Inductor current are observed and the similarities are noted in the following table.

		PLECS		VIRTUOSO/SPECTRE	
		Overshoot	Settling time	Overshoot	Settling time
Load Step	V_{out}	1.78%	15us	1.6%	12us
	$I_{inductor}$	10%	10us	10%	12us
Reference Step	V_{out}	N/A	22us	N/A	20us
Startup Transient	V_{out}	2.22%	60us	1.9%	65us

Table 4-1 Overshoot and Settling comparison

4.2 4-Phase

4.2.1 Load Transient Response – V_{out}

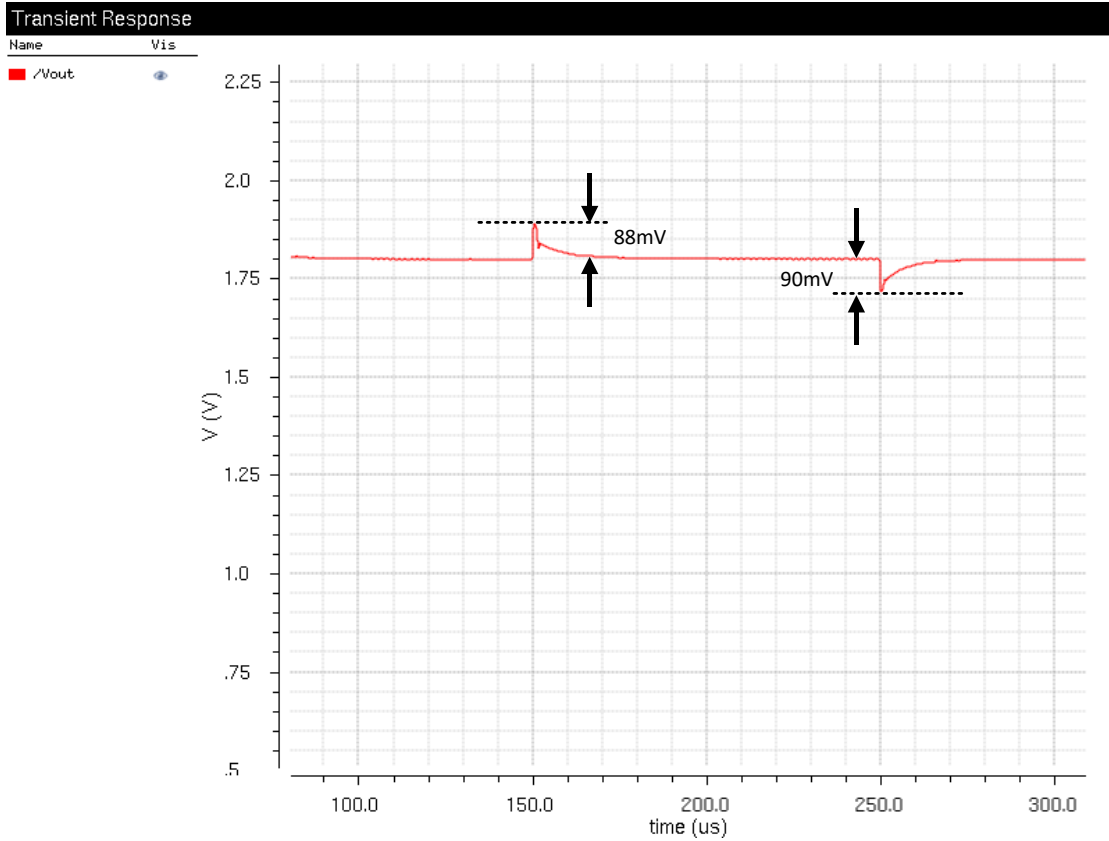


Figure 4.15 V_{out} Load step response in the 4-Phase Buck Converter

Figure showing the output response to a load step from 2A – 1A – 2A.

4.2.2 Load Transient Response – Inductor Current

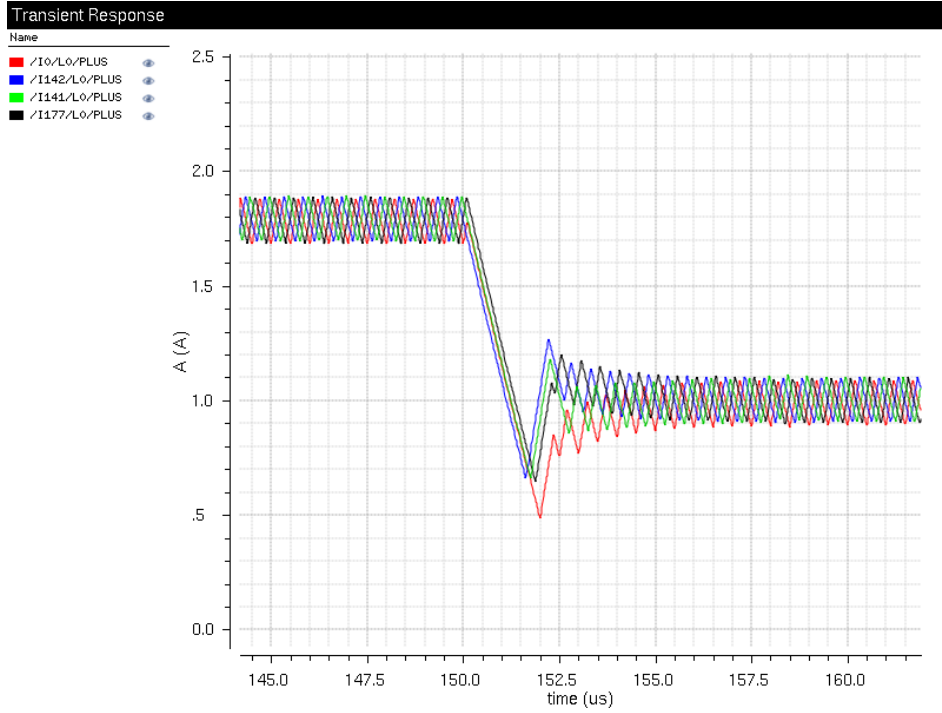


Figure 4.16 Inductor Current response to a load step from 7.5A – 4A.

Response of the individual inductor currents to a load step from 7.5A – 4A. The system settles to a steady-state after 5us or 10 cycles.

4.2.3 4-Phase Individual Currents – Ideal

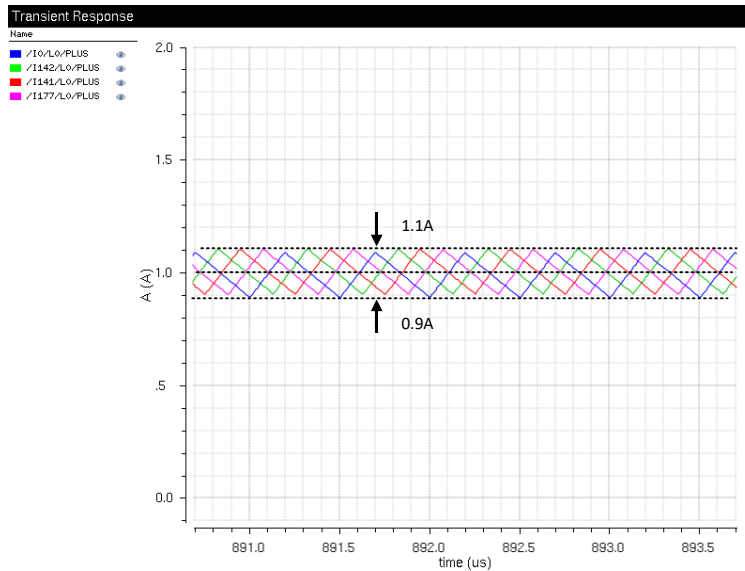


Figure 4.17 Individual phase inductor currents with identical power-stage and current sensing blocks.

4.2.4 4-Phase Individual Phase Currents – Inductor and Emulator Mismatch

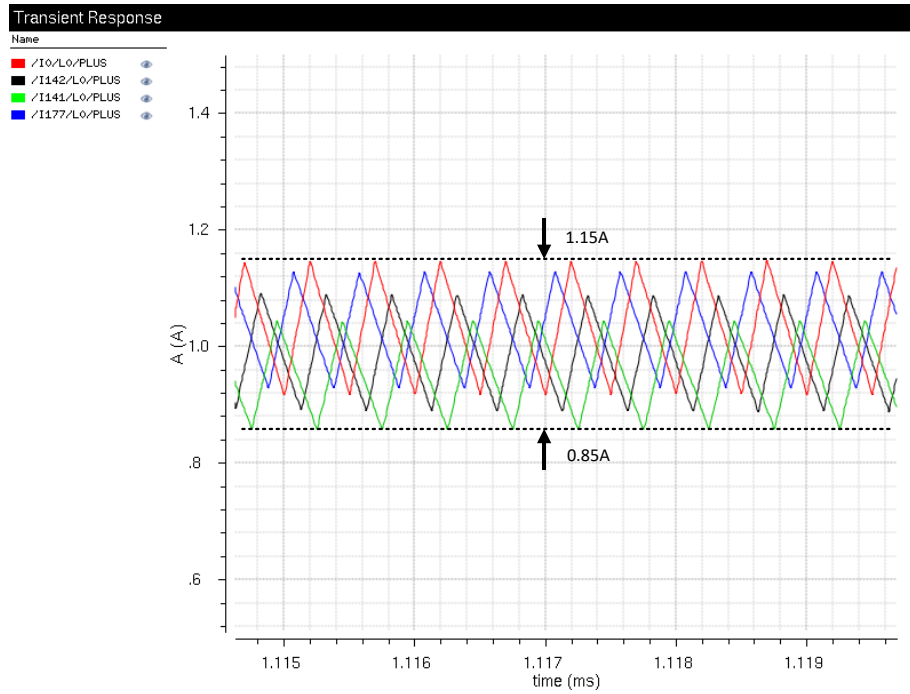


Figure 4.18 Individual Phase Currents in the 4-Phase Buck Converter with 2-% worst case mismatch between inductor and emulator block

Individual phase inductor currents with a worst-case mismatch of 20% between the inductor and emulator. The load is chosen to be 4A, inductor to be $L \pm 10\%$ and emulator Capacitor to be $C \pm 10\%$. A maximum current sharing error of 4% for the given values is obtained.

4.2.5 4-Phase Individual Currents – Individual DCR Mismatch

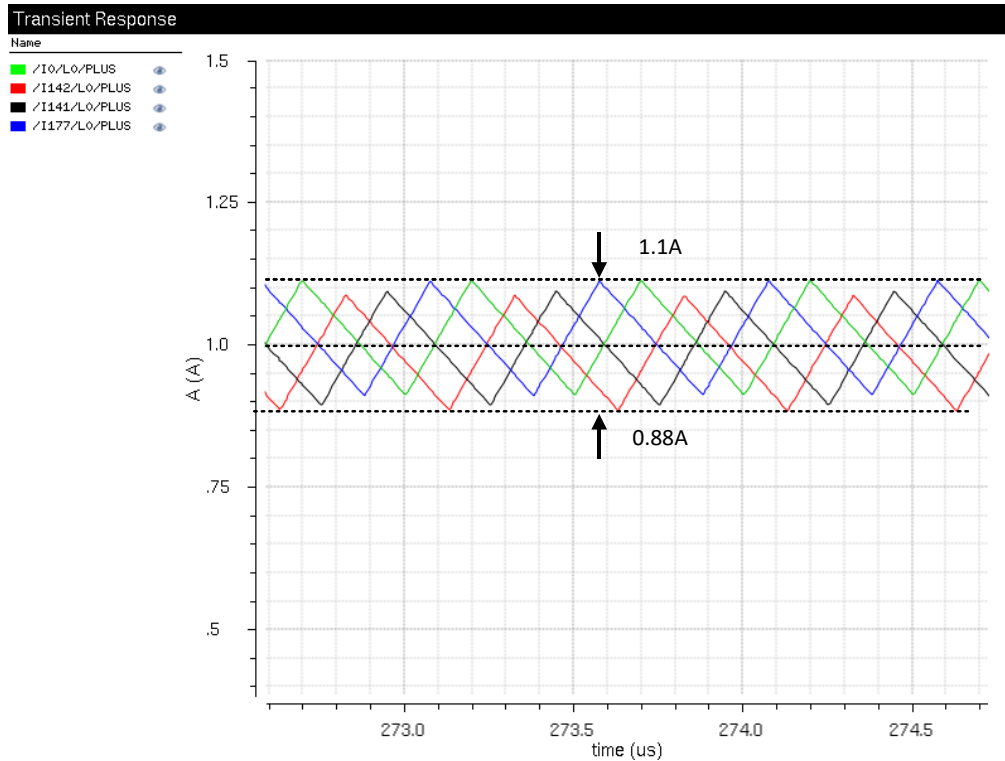


Figure 4.19 Individual phase currents in the 4-Phase Buck Converter with a worst-case DCR mismatch of 10%

Individual phase inductor currents with a worst-case mismatch of 10% between individual phase inductor DCR. For a load of 4A, and ideal DCR of 5mΩ,

$DCR_{Master} = DCR \pm 10\%$, $DCR_{Slave1} = DCR \pm 5\%$, $DCR_{Slave2} = DCR \pm 5\%$. $DCR_{Slave3} = DCR \pm 5\%$,

Current sharing error of 2% is obtained.

4.2.5.1 Accuracy/Speed Trade-off

An RC filter with a time constant of 3.2ms is used to sense the average inductor component.

Eventhough, accuracy of the average current sensor is improved, it affects the speed. Also, accuracy of load sharing improves if the measurements are taken after the average current sense circuit has settled within an acceptable accuracy level of 5%.

4.3 Efficiency Plots

4.3.1 Load v/s Efficiency – Single Phase

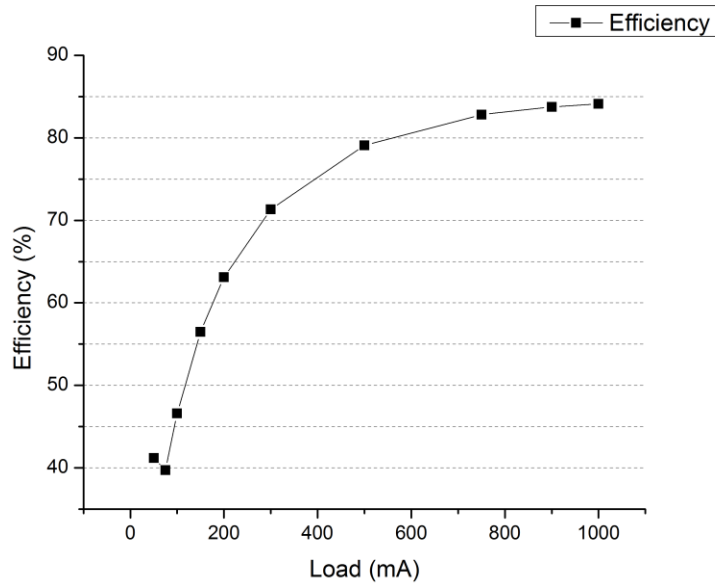


Figure 4.20 Load v/s Efficiency plot for single-phase Buck Converter

4.3.2 Load v/s Efficiency – 4-Phase

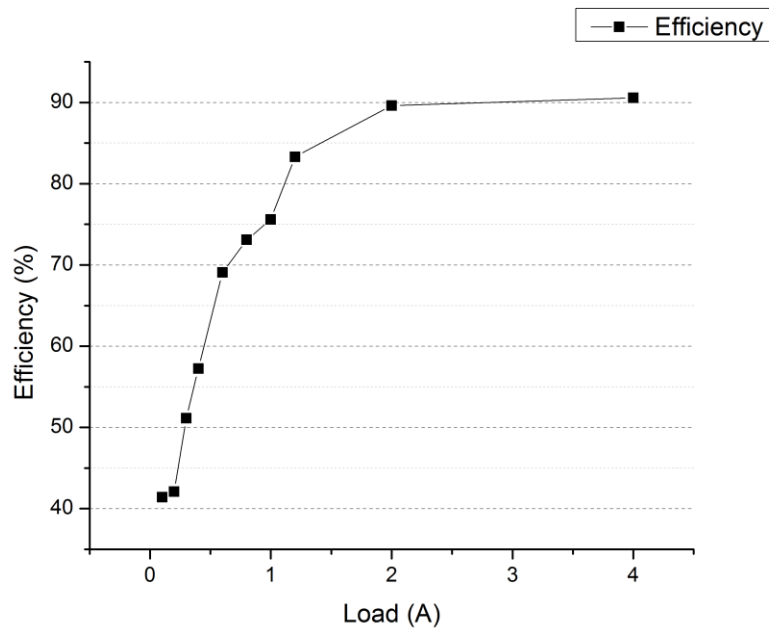


Figure 4.21 Load v/s Efficiency plot for the 4-Phase Buck Converter

4.4 Current-Sharing Error

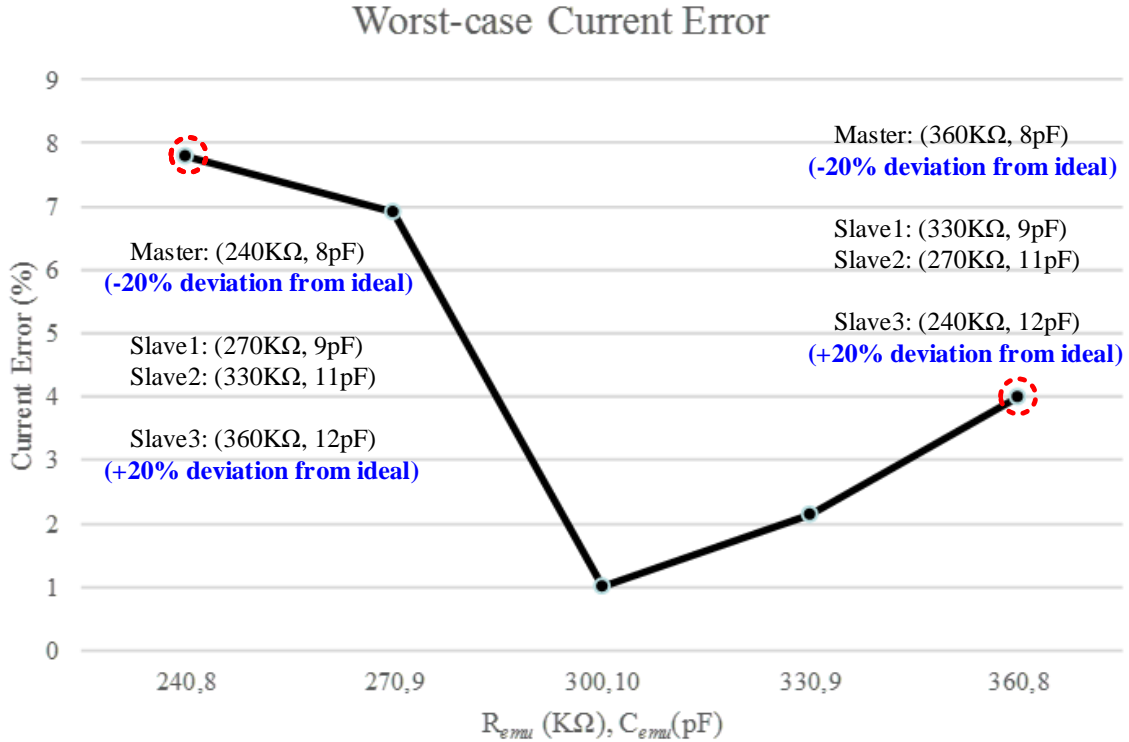


Figure 4.222 Current Sharing error in presence of Emulator Component variations in the 4-Phase Buck Converter

Figure above depicts the worst-case and best-case current sharing performance in the 4-Phase Converter. A current sharing error of 8% was obtained for the emulator component values as mentioned in the figure. R_{emu} and C_{emu} indicate the Resistor and Capacitance values used in the emulator circuit. Current error is defined as the deviation of each phase inductor current from the ideal individual inductor current. Figure below illustrates individual phase inductor currents in the presence of mismatches and variations.

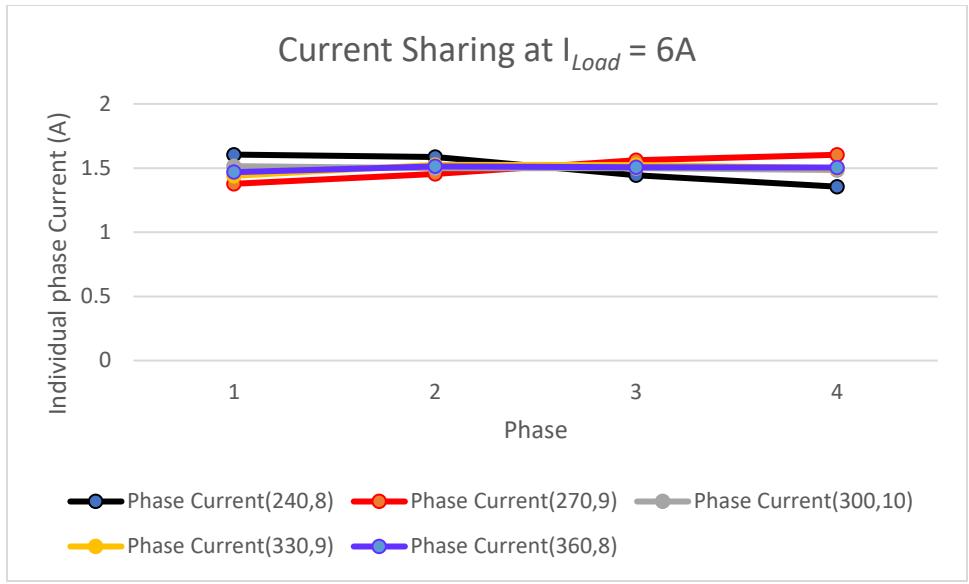


Figure 4.23 Individual phase currents in the presence of Emulator Component variations in the 4-Phase Buck Converter

CHAPTER 5

SUMMARY AND FUTURE IMPROVEMENTS

An Inductor emulator based 4-Phase Buck regulator with Peak current mode control is proposed as part of this research. The current sensing technique is based on replicating the inductor current based on the input, output voltage and the duty cycle information. The proposed current sensing is employed for peak current mode control. Additionally, a Master-Slave current sharing technique is implemented for current sharing among individual phases.

This work comes up with an approach to implement an external inductor current replicating circuit. The proposed work is modelled and verified in PLECS and circuit design of the modelled system is implemented in 250nm TSMC process and verified through simulations. An experimental current sensing technique is implemented and has the capability of having high efficiency and high accuracy. This solution proposes an innovative way to sense the inductor current through replication and employing it for peak current mode control. A peak efficiency of 90.5% is obtained with 5V to 1.8V conversion at 4A load.

5.1 Future Improvements

Future improvements to the proposed solution can be focused towards minimizing the impact of inductor DCR mismatch and inductor – Emulator mismatch. An inductor Built-In Self-Test (BIST) can be implemented to accurately measure the inductor DCR [35]. Also, an adaptive compensator as used in [35] can be implemented to ensure a stable loop response and current sharing over wide range of inductor DCR and Emulator components.

Thus, the inductor emulator approach can become one of the innovative solutions for current sensing if a BIST mechanism and adaptive compensator are implemented to improve the system accuracy and stability.

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