High Gain DC-DC and Active Power Decoupling Techniques for Photovoltaic Inverters

by

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ABSTRACT

The dissertation encompasses the transformer-less single phase PV inverters for both the string and microinverter applications. Two of the major challenge with such inverters include the presence of high-frequency common mode leakage current and double line frequency power decoupling with reliable capacitors without compromising converter power density. Two solutions are presented in this dissertation: half-bridge voltage swing (HBVS) and dynamic dc link (DDCL) inverters both of which completely eliminates the ground current through topological improvement. In addition, through active power decoupling technique, the capacitance requirement is reduced for both, thus achieving an all film-capacitor based solution with higher reliability. Also both the approaches are capable of supporting a wide range of power factor.

Moreover, wide band-gap devices (both SiC and GaN) are used for implementing their hardware prototypes. It enables the switching frequency to be high without compromising on the converter efficiency. Also it allows a reduced magnetic component size, further enabling a high power density solution, with power density far beyond the state-of-the art solutions.

Additionally, for the transformer-less microinverter application, another challenge is to achieve a very high gain DC-DC stage with a simultaneous high conversion efficiency. An extended duty ratio (EDR) boost converter which is a hybrid of switched capacitors and interleaved inductor technique, has been implemented for this purpose. It offers higher converter efficiency as most of the switches encounter lower voltage stress directly impacting switching loss; the input current being shared among all the interleaved converters (inherent sharing only in a limited duty ratio), the inductor conduction loss is reduced by a factor of the number of phases.

Further, the EDR boost converter has been studied for both discontinuous conduc-

tion mode (DCM) operations and operations with wide input/output voltage range in continuous conduction mode (CCM). A current sharing between its interleaved input phases is studied in detail to show that inherent sharing is possible for only in a limited duty ratio span, and modification of the duty ratio scheme is proposed to ensure equal current sharing over all the operating range for 3 phase EDR boost. All the analysis are validated with experimental results.

...to my daughter, Anika

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Chapter 1

INTRODUCTION

Solar energy is among the fastest growing renewable energy resources which accounts for an increasing and significant share of new generation capacity additions each year [1]. In the U.S. new solar installations have exceeded 1 GW DC in each quarter since 2014, reaching a total capacity of 29 GW DC in March 2016. In Q1 of 2016, solar photovoltaic (PV) systems accounted for 64% of new electric generation added in the U.S. market, making it the largest source of capacity addition across all the fuel types [1]. The distributed PV systems are garnering the interest of both the utility providers and residential consumers with the reducing solar panel costs, government incentive programs, and regulatory policies [2, 3]. The power electronic converter is a key component of the grid connected PV systems, extracting maximum power from PV panels and interfacing them to the grid.

1.1 PV Inverter

Currently, there are three widely used grid interactive PV systems: the centralized inverter system, the string inverter system, and the microinverter system [4].

1.1.1 Central Inverter

The central inverters are typically in the $100 - 1000$ kW range with three-phase topology and modular design for large power plants and typical unit sizes of 100, 150, 250, 500 and 1000 kW. The PV modules are arranged in series-parallel combinations, connected to one common central inverter as shown in Figure 1.1. The following are the merits and demerits of central inverter system.

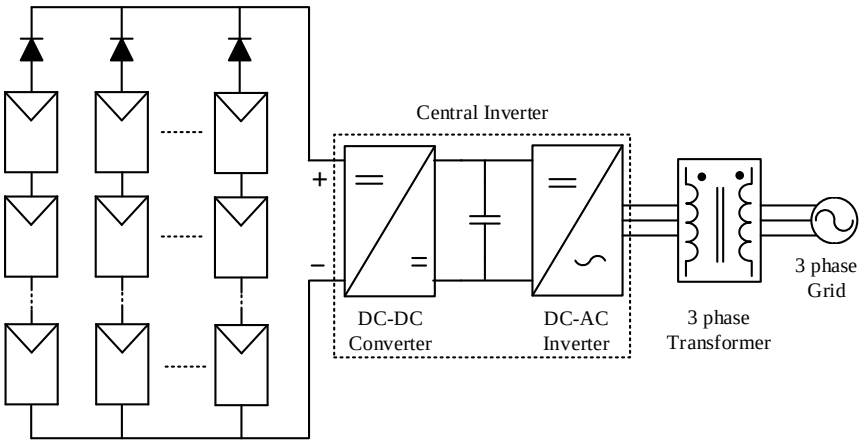


Figure 1.1: Central Inverter System.

- High efficiency (more than 98 %) power conversion
- Cost effective for utility scale applications
- Maximum power point tracking (MPPT) control is disproportionate as it is common for the combined PV array
- Reduction in energy yield in case of partial shading, and may lead to hot spot failure under significantly unequal shading
- Loss of a single inverter leads to the loss of the entire or a large part of the power generation, so the system is not reliable
- Need for high-voltage DC cables between PV panels and inverter.

1.1.2 String Inverter

The string inverters, shown in Figure 1.2, are based on a modular concept, where PV strings, made up of series-connected solar panels, are connected to separate inverters. The string inverters are paralleled and connected to the grid. If the string voltage is high enough then no voltage boosting is necessary, thereby improving the system efficiency. Fewer PV panels can also be used, but then a DC/DC converter

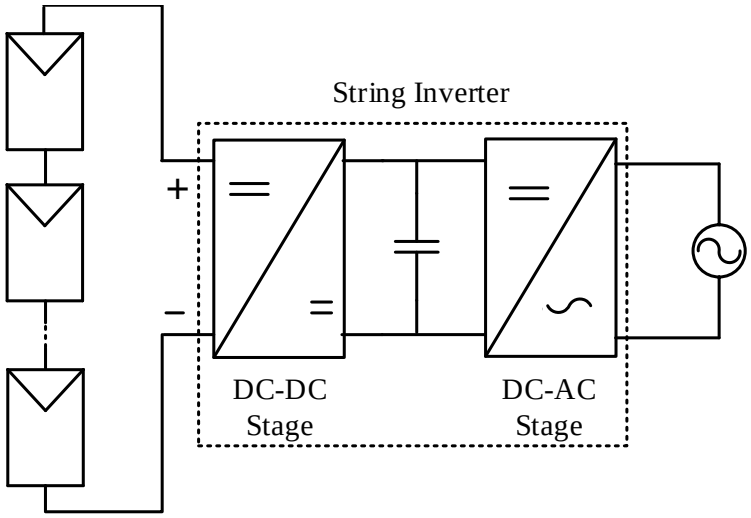


Figure 1.2: String Inverter System.

or a line/high frequency transformer is needed for a boosting stage. The advantages compared to the central inverter are as follows:

- No losses in string diodes (no diodes needed)
- Separate MPPTs for each string so better power yield, but still it is not optimal.

However, due to the series connection of modules, the current from the PV string is limited by the weakest link, i.e., a shaded module, and therefore, the loss of generation is still larger than the corresponding microinverters for partial shading with string inverters.

1.1.3 Microinverter

The microinverter, as shown in Figure 1.3 is popular for the power level ranging from 200-500 W. Each such power processing device is responsible for the independent MPPT of every single PV panel, thus maximizing the power production. It converts the PV output to the AC voltage through one or more stages of power conversion, and is integrated to the grid individually. It outperforms the string inverters under

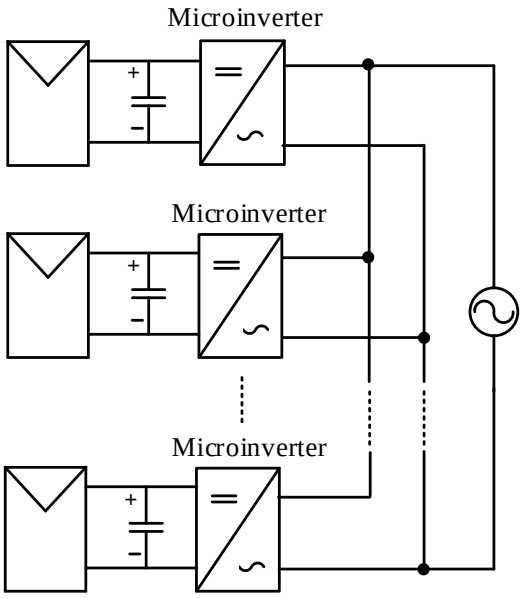


Figure 1.3: Microinverter System.

partial shading conditions created, for example, by-passing clouds. The output from the unshaded modules is not affected under partial shading condition, and hence, the total power is significantly higher. The following are the advantages of microinverter system.

- The microinverter is an integrated part of the PV panel. It remove losses due to the mismatch between panels and support panel level MPPT. For a string inverter or a centralized inverter, a string or multistring of PV panels shares a single MPPT controller, but the mismatch loss is significant in partial shading conditions [5]. Considering the mismatch loss together with the DC/AC conversion loss contributing to the whole PV system loss, string/centralized inverters may have lower system efficiency than microinverters due to higher mismatch loss although they usually have higher DC/AC conversion efficiency than microinverters.

- Panel level hot-spot risk is removed and panel lifetime can be improved. Hot

spot takes place when a shaded cell within a partially shaded panel becomes reverse biased and dissipates power in the form of heat [6]. For series connected PV panels used with a string/centralized inverter, a by-pass diode is added to each panel in practice. For the microinverter solution, the by-pass diode is not necessary because each panel has its own power processing unit, leading to no direct connection between the PV panels.

- Its 'plug and play' feature simplifies system installation and maintenance. The microinverter solution allows for more flexible PV project planning and multi-faceted PV panel installation.

1.2 Transformer-less Single Phase PV Inverter

The focus of the present work encompasses the transformer-less single phase PV inverters, both the string and the microinverter implementation. The transformer-less PV inverters are becoming increasingly more attractive due to their lower cost, reduced footprint, and improved efficiency compared to inverters with transformer isolation. However, a major challenge with the transformer-less inverters is the presence of common mode leakage currents [7] which can increase the system loss, distort the grid current, and induce severe electromagnetic interference.

In addition, similar to most single-phase converters, another main challenge is the presence of double line frequency power ripple [8, 9], which is the difference between the instantaneous grid injected power and the constant dc power corresponding to the maximum power point (MPP) from the PV panels, necessitating the use of large filters in conventional topologies.

Finally, for the transformer-less microinverter application, another challenge is to achieve a very high gain DC-DC stage simultaneously maintaining a high conversion efficiency. The following gives a detailed discussion of the implementation challenges.

1.2.1 Challenge I: Capacitive Ground Current

The frame of a PV module is required by codes to be grounded. There is significant parasitic capacitances between the positive and negative PV terminals to the frame, and hence to the ground. When the positive and/or negative terminals are connected to a switching node of the inverter with respect to ground, it can lead to significant, common mode ground currents through these parasitic capacitances. [7,10–13] present different methods to mitigate this problem in transformer-less PV inverters.

The straight-forward way to address this issue would be directly connecting the PV terminal ground to the grid neutral with topological variations which would generate no common mode voltage [14,15] or at least ensuring a low-frequency (typically fundamental frequency) or constant potential of the PV negative terminal relative to the grid neutral using half-bridge, or neutral point clamped (NPC) inverters [16]. For a conventional full bridge DC-AC inverter with unipolar sinusoidal pulse width modulation (SPWM), the voltage across this stray capacitance swings at switching frequency, increasing the leakage current, whereas realization with bipolar SPWM reduces the common mode ground currents. Other solutions to the ground current issue would involve disconnecting the PV negative from the grid neutral at certain operating inverval over a cycle with additional switches and diodes [17,18].

1.2.2 Challenge II: Power Decoupling

Figure 1.4 shows the power decoupling consideration required for single phase inverters. The input power from the PV array being purely DC as shown by P_{IN} and the output being a sinusoidally varying power superimposed on a DC average as shown by P_O, the instantaneous power from input is clearly not equal to that of the output. Considering the grid voltage and current as given in (1.1), the grid power is

given in (1.2) which is a double line frequency varying ripple power.

$$v_g = V_g \sin(\omega t); \qquad i_g = I_g \sin(\omega t + \theta) \tag{1.1}$$

$$P_g = \frac{V_g I_g}{2} \left(\cos\theta - \cos(2\omega t + \theta)\right) \tag{1.2}$$

Thus a energy storage element, like a large DC-link capacitor is required to store and deliver the balance power over one fundamental cycle. This ensures that the PV input is free from any voltage ripple which would otherwise degrade the MPPT efficiency of the converter. The state-of-the-art approaches predominantly use electrolytic capacitors for these decoupling purposes, which have relatively high equivalent series resistance (ESR) and low RMS current rating per μF. Moreover, these capacitors have limited lifetime [19] which further degrades with electrical and thermal stresses, and thermal cycling [20]. Consequently they pose reliability challenges to the inverters, which require to compete with the 25 years of warranted lifetime of the PV module [21].

Thus an extensive research has been directed to replace these electrolytic capacitors with corresponding film capacitors and increase the reliability of the inverters. But as the capacitor to volume ratio of a film capacitor is low compared to an electrolytic capacitor, so instead of directly replacing them, novel power decoupling tech-

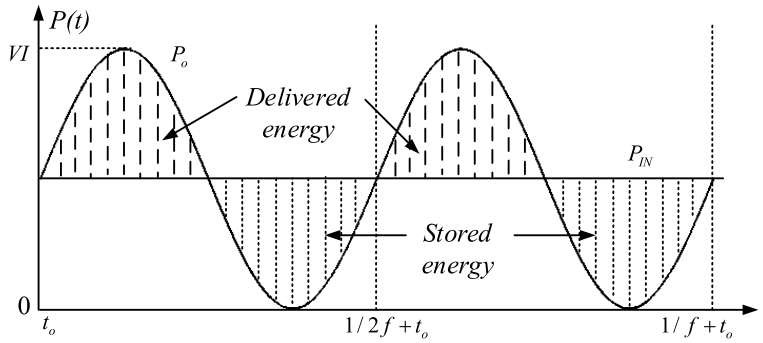


Figure 1.4: Power Decoupling Concept.

niques are proposed in literature [8, 19, 22–27] to reduce the capacitor requirement and address the double line frequency power with smaller capacity energy storage component.

Some converters address the issue by adding an additional conversion stage (an auxiliary circuit) to handle the ripple power [22,24], which can be connected in either series or parallel to the primary converter. The main disadvantages of such approaches are higher cost, complex circuitry, and often higher losses with the addition of more active components. They also have to encounter higher current stress on the auxiliary circuit if connected in series [24] or higher voltage stress if connected in parallel.

For power factor correction (PFC) applications, [25] achieves reduction in the capacitance by allowing higher voltage ripple across the DC-link but at the cost of distorted line input current. Other papers have discussed sophisticated control schemes to reduce the DC-link capacitor without affecting the power quality [26, 27]. But all these approaches do not essentially stretch the limit on reducing the capacitors to the minimum and there is still much room for improvement. As such decoupling capacitor volume reduction remains an active area of research. In a recent study in [28], several decoupling approaches have been compared including DC side decoupling and AC side decoupling, with DC side decoupling shown to outperform AC decoupling approaches. The best solution shown in [28] achieves 15 F/kW at 800 V, but using six switches and without considering the ground current issues or non-unity power factor operation.

1.2.3 Challenge III: High Volatage Gain

As mentioned in Section 1.1, the microinverters are directly connected to each of the PV panel with typical input voltage spanning from 20 to 40 V, whereas, to interface to the grid the AC output voltage needs to be 120 V/ 230 V RMS. This

necessitates a high voltage boost for interfacing a PV panel to the grid. Thus a high voltage gain is required by the DC-DC stage and with a transformer-less implementation, it poses a big challenge. A review of the high gain DC-DC boost is discussed in the following Section 1.3.

1.3 High Gain Transformer-less DC-DC Boost Stage

Though ideally the conventional boost or buck-boost converter can achieve high gain, in practical implementation their voltage gain is limited, typically to 5-8, by the inductor series resistance and losses incurred by the semiconductor components which need to operate under extreme-duty-ratio, high voltage stress, and overall poor converter performance as duty ratio approaches unity. Hence, alternate topologies for high step-up conversion and improved system operation is an active area of research exploring both isolated and non-isolated converters.

A high frequency transformer-isolated DC-DC converter is a popular choice in applications which necessitate galvanic isolation between the input and output ports [29, 30]. It can also be employed in high step-up applications not demanding isolation as it has the advantage of achieving high gain with a flexible selection of the transformer turns ratio at the design stage. But it has the drawback of higher switch voltage stress, current spike, and lower efficiency due to the transformer leakage inductance and parasitic capacitance formed between its primary and secondary winding. Active clamp or snubber circuit can be implemented to avoid voltage spike, but these lead to complex circuitry and loss in the auxiliary circuit [31, 32]. Integrated magnetic based isolated converters can also be implemented to increase the power density and efficiency with added performance features like soft switching of the converter switches [33, 34]. Resonant converter based isolated converters are further proposed where the transformer leakage inductance is used as the resonant inductance [35–37].

On the other hand, non-isolated high gain converter has the benefits of higher efficiency, smaller foot-print, reduced volume, and lower cost with the elimination of the lossy and bulky transformer. A wide variety of non-isolated topologies based on switched capacitor [38–41], voltage multiplier cell (VMC) [42–45], three state switching cell (3SSC) [46–48], coupled and/or interleaved inductor [49–54], or a combination of these [55–61] are available in literature. A number of soft switching approaches to improve the efficiency with the above mentioned voltage boost techniques or even with the conventional converters extreme-duty-ratio-operation have also been reported [62, 63].

Switched capacitor based high step-up converters [38–41] have been presented to attain improved efficiency, higher power density, and better performance as it has no magnetic components making it a low noise with minimal radiated electromagnetic interference (EMI) solution [40]. Due to its modular structure, the voltage scaling is flexible with this technique. But it has the disadvantages of pulsating input current and poor voltage regulation as the voltage gain is predetermined by the circuit structure and the input must be an integer fraction of the output voltage. The VMC based converters [42–45] more commonly referred to as hybrid switched capacitor can be used to circumvent this problem. Primarily the voltage multiplier cell is composed of capacitor-diode-resonance inductor which can be integrated to classical DC-DC converters. The resonance inductor allows the zero current switching (ZCS) turn-on of the main switch, but is not mandatory for basic operation of the multiplier cell [44].

For high gain applications, 3SSC converters based on acitve switches, diodes, and coupled inductor are alternatively proposed to reduce inductor size, lower input and output current ripple, and decrease the voltage stress of the main switch [46, 47]. In fact the voltage stress across the switch is naturally clamped by the output filter capacitor. [48] attains high gain by integrating VMC and 3SSC approaches.

Besides, the coupled inductor based converters can provide high voltage step-up by manipulating the turns ratio but maintaining lower voltage switch stress and conduction loss [49, 50]. However, these have high ripple at the input and the ripple increases with the increase of turns ratio to meet the higher voltage gain requirement. Also their efficiency is degraded due to the losses associated with the leakage inductors and active clamping is proposed to recycle the leakage energy at the cost of circuit complexity [51, 52, 64]. For high input current application, interleaving has been proven to provide lower input ripple, reduced passive component size, and lower loss, but the voltage gain is still the same as the classical boost converter [53, 54].

Converters combining the features of previously discussed approaches are demonstrated to provide high gain with improved system performance but have inherently complex implementations. [55, 56] combine the features of coupled inductor and switched capacitor technique, while [57, 58] integrate coupled inductor and VMC attributes. The coupled inductor and 3SSC techniques are merged in [59, 60], whereas in a recent publication in [61], features of coupled inductor, VMC, and 3SSC are all integrated in one converter. Additionally, the hybrid boost-flyback topology is introduced to achieve high static gain with low voltage stress across the switches, but it requires large input filters as the input current is pulsed [65, 66]. For improved efficiency [62, 63] propose soft switching technique with the interleaved converter.

1.4 Objectives and New Contributions of the Work

The dissertation focuses on developing single phase transformer-less PV intervers for string and microinverter application, ensuring higher efficiency, high power density, wide band-gap device based high switching frequency, and reduced decoupling capacitance requirement through active power decoupling. The new contributions of this work are:

- extended duty ratio (EDR) boost converter has been thoroughly analyzed and implemented for high gain purpose as the DC-DC stage for the non-isolated microinverter application;
- a novel sensor-less current sharing technique with duty ratio and phase shift modification of the carrier signal has been proposed to ensure wide input/output voltage range of operation for the EDR boost converter;
- discontinuous conduction mode (DCM) operation for the EDR converter is studied for different operating zones for high gain dc-dc light load application;
- an active power decoupling scheme with large sinusoidal swing of the half-bridge capacitors and a double line frequency DC-link voltage ripple termed as half-bridge voltage swing (HBVS) inverter has been proposed to reduce the capacitor requirement; the proposed converter is studied, implemented and tested for its performance validation in string inverter application;
- another active power decoupling scheme with dynamic DC-link (DDCL) approach has been analyzed, implemented, and tested for microinverter application which uses only four switches and reduced capacitance for decoupling purposes along with the feature of double grounding.

The papers published during the course of this dissertation are:

- J. Roy and R. Ayyanar, "Sensor-Less Current Sharing Over Wide Operating Range for Extended-Duty-Ratio Boost Converter," in IEEE Transactions on Power Electronics, vol. 32, no. 11, pp. 8763-8777, Nov. 2017.
- Y. Xia; J. Roy; R. Ayyanar, "A capacitance-minimized, doubly grounded transformerless photovoltaic inverter with inherent active-power decoupling," in IEEE Transactions on Power Electronics, vol. 32, no. 7, pp. 5188-5201, July 2017.

- Y. Xia; J. Roy; R. Ayyanar, " A T-Type Single Phase Transformer-less String Inverter with Dynamic and Adaptive DC-Link Voltage Control," under revision in IEEE Transactions on Power Electronics.

- R. Ayyanar, Y. Xia, and J. Roy, Arizona State University, Reduced volume single-phase double-grounded transformer-less photovoltaic inverter with active power decoupling, Patent pending, Application No. 62/263,068, Dec 2015

- J. Roy; R. Ayyanar, "Seamless Transition of the Operating Zones for the Extended-Duty-Ratio Boost Converter," accepted in 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, Ohio, 2017.

- J. Roy; Y. Xia; R. Ayyanar, "GaN-based High Gain Soft Switching Coupled-Inductor Boost Converter," accepted in 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, Ohio, 2017.

- J. Roy; Y. Xia; R. Ayyanar, "Sliding Mode Control of a Single Phase Transformer-less PV Inverter with Active Power Decoupling," accepted in 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, Ohio, 2017.

- Y. Xia; J. Roy; R. Ayyanar, "Optimal Variable Switching Frequency Scheme for Grid Connected Full Bridge Inverters with Bipolar Modulation Scheme," accepted in 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, Ohio, 2017.

- Y. Xia; J. Roy; R. Ayyanar, "A Single Phase Doubly Grounded, PV Inverter using Coupled Inductor with Integrated Magnetics and Active Power Decoupling Technique," accepted in 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, Ohio, 2017.

- J. Roy; R. Ayyanar, "A single phase transformer-less string inverter with integrated magnetics and active power decoupling," accepted in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), March, 2017.

- J. Roy; Y. Xia; R. Ayyanar, "GaN based transformer-less microinverter with extended-duty-ratio boost and doubly grounded voltage swing inverter," accepted in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), March, 2017.

- Y. Xia; J. Roy; R. Ayyanar, "A GaN based doubly grounded, reduced capacitance transformer-less split phase photovoltaic inverter with active power decoupling," accepted in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), March, 2017.

- J. Roy; R. Ayyanar, "GaN based high gain non-isolated DC-DC stage of microinverter with extended-duty-ratio boost," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), presented, Sept 2016.

- J. Roy; Y. Xia; R. Ayyanar, "A single phase transformerless string inverter with large voltage swing of half bridge capacitors for active power decoupling," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), presented, Sept 2016.

- Y. Xia; J. Roy; R. Ayyanar, "A high performance T-type single-phase doubly grounded transformer-less photovoltaic inverter with active power decoupling," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), presented, Sept 2016.

- A. Sastry et al., "Failure modes and effect analysis of module level power electronics," Photovoltaic Specialist Conference (PVSC), 2015 IEEE 42nd, New

Orleans, LA, 2015, pp. 1-3.

1.5 Chapter Overview

Chapter 2 discusses the EDR boost for transformer-less high step-up application. Comprehensive analysis of converter operating principles, key theoretical waveforms, and steady state circuit performance corresponding to all the possible zones of operation have been presented for a 3-phase EDR boost converter. Methods for sensor-less current sharing among the different phases of the 3-phase EDR boost have been introduced. The sharing scheme has been convincingly demonstrated in a 250 W GaN based hardware prototype for different operating regions.

The EDR converter shows interesting performance features and current sharing characteristics in the discontinuous conduction mode (DCM) operation. For an M-phase converter in DCM, all the boost inductors would still share the current equally inherently in each of Zone I to Zone M-1, while only Zone M (the least gain region) would not experience inherent equal current sharing. In fact, in Zone M, the inductor current for phases 2 to M will have negative excursion at certain operating interval. A comprehensive analysis of the operation of 3-phase EDR boost converter in DCM for each of its operating zones is presented in **Chapter 3**. Further, the results are validated from the GaN-based 3-phase 100 W experimental prototype.

In **Chapter 4**, a power decoupling scheme for single phase inverters has been proposed. The converter termed as half-bridge voltage swing (HBVS) inverter is a combination of boost and half-bridge stages along with a power decoupling stage. A large sinusoidal swing of the half-bridge capacitors are allowed along with a double line frequency DC-link voltage ripple to address the power decoupling with a reduced capacitor value of only 54 μF/ kW at a peak of 550 V DC-link voltage. Further, the inductors of the buck-boost and the half-bridge inverter stages are integrated in one

single core to reduce the converter volume and cost. The experimental results with the integrated inductors at 1 kW output are provided for validation of the concept for string inverter application.

In **Chapter 5**, another power decoupling technique is introduced based on a doubly grounded transformer-less PV inverter topology with active power decoupling built into the basic topology termed as dynamic DC-link (DDCL) inverter. It is based on a single stage of power conversion by a unique combination of boost-coupled half bridge circuit using only four switches overall and capable of supporting a wide range of power factor. The simulation and experimental results at 300 W output are provided for validation of the concept for microinverter application with a high-gain DC-DC stage as the front-end converter.

The report is concluded in **Chapter 6** with the summary and future work of this research contribution.

Chapter 2

EXTENDED DUTY RATIO BOOST CONVERTER

2.1 Introduction

The extended-duty-ratio (EDR) boost converter (M-phase version is shown in Figure 2.1), has been studied for the high step-up implementation. It inherits the merits of switched capacitors and interleaved inductor technique and offers lower converter losses as most of the switches encounter lower voltage stress, and thus switches with lower voltage rating and thus lower $R_{DS(ON)}$ can be used. Also the input current is shared among all the interleaved converters (inherent sharing only in a limited duty ratio), so the inductor conduction loss is reduced by a factor of the number of phases. Besides, the current through the switches is a fraction of the input current resulting in minimized conduction and switching losses. Buck implementation of EDR converter is proposed in a number of previous works intended for voltage step-down applications as voltage regulators (VR) or point of load (POL) implementation [67–70], whereas its variations are reported in [71–78]. These papers primarily studied the converter in only one operating zone, where the phase currents (output inductor currents for buck operation) are being shared inherently. In a recent work EDR converter has been employed in a bidirectional application [79].

In this chapter, the operation of the EDR boost converter in different operating zones is studied in detail along with the current sharing between its interleaved input phases.

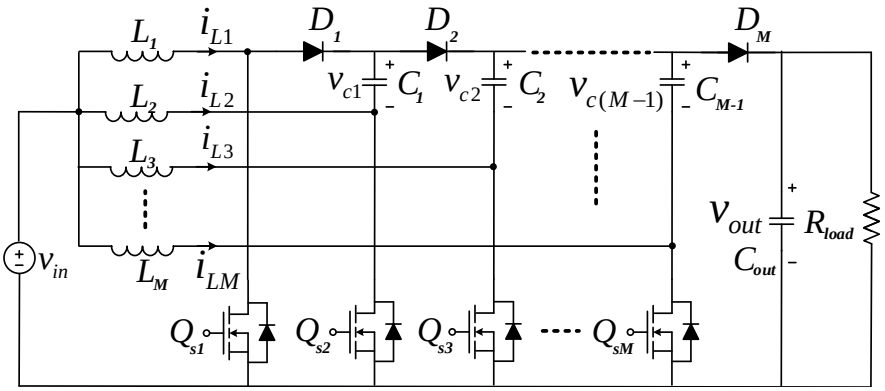


Figure 2.1: Topology for M-Phase Extended Duty Ratio (EDR) Boost.

2.2 M-Phase EDR Boost Converter

Figure 2.1 shows the M-phase EDR boost topology. It is a combination of interleaved inductor with switched capacitor configuration. The circuit consists of M switched capacitors C_M whose voltage levels v_{cM} are a fraction of the output voltage v_{out}, and M interleaved boost inductors which share the input current in equal or unequal proportion depending on the operating duty ratio of the converter. The load is connected across the final capacitor i.e., $v_{cM} = v_{out}$. Each boost phase is interleaved which means that they are phase shifted by $(360/M)^\circ$.

For a comprehensive analysis and design of a general M-phase converter, the operation needs to be studied under M different zones with the duty ratio for the m^{th} zone given by (2.1).

$$\frac{M-m}{M} \leq D \leq \frac{M-m+1}{M} \text{ for all } m \in [1, M] \tag{2.1}$$

The converter gain in different zones cannot be expressed with any general expression, as the operating modes in each zone is not the same. As an example for Zone I (this is the zone with maximum voltage gain), the operating modes only encompass intervals with either all M phases being simultaneously on or intervals where $(M-1)$ phases are on in a certain pattern depending on interleaving sequence. Here, the

lower switch turned on is referred to as the phase being on. The voltage gain of the converter in this zone is given by (2.2).

$$k_I = \frac{M}{1-D} \text{ for } m = 1 \tag{2.2}$$

On the contrary, for Zone M (this is the zone with minimum voltage gain), the operating modes only encompass intervals with either a single phase being on or intervals where neither of the phases are on. And the gain in this zone is given by (2.3).

$$k_M = \frac{1}{(1-D)^M} \text{ for } m = M \tag{2.3}$$

It is also interesting to notice that the current is inherently shared among all the interleaved boost inductors only in Zone I operation. This can be verified with the basic capacitor charge balance principle for all the switched capacitors. Thus it is the preferred operating zone as the maximum voltage gain is also obtained in this region. However, with a wide range of operating input and output voltages, the converter is required to be operated for an expanded range of duty ratio forcing the converter to also operate in some other $M-1$ operating zones where the current is no longer shared equally inherently.

So outside this region some of the phases might be overloaded, if a proper current sharing scheme is not employed. This would lead to higher switching and conduction losses in overloaded phases leading to hot spot; the inductors might also saturate altogether disrupting the converter operation. So it is very important to address the current sharing issue.

Current sensors can be employed to realize the current sharing by advanced control technique [69]. But it would incur higher component count as each phase would require separate sensor and associated conditioning circuitry, increased control com-

plexity, and higher cost. It has been observed that in the rest of the $(M-1)$ zones where the phase currents are not inherently shared, either the magnitude or the phase-shift of the duty ratio of each interleaved phase can be modified to ensure input current being shared equally or more evenly between the phases. This property has been exploited to ensure current sharing in EDR boost converter.

2.3 Operating Principles

The following analysis considers the converter operating in continuous conduction mode (CCM) where the inductor current of all the boost phases would always be continuous.

As has been discussed in Section 2.1, to get an insight of the converter operation in various zones, each operating zone with unique combination of operating modes needs to be analyzed individually. A basic 3-phase topology as given in Figure 2.2 is considered to comprehend the converter operation where $M = 3$. Figure 2.3 shows the different operating modes of the converter resulting from different combination of the switching pattern. For example, Figure 2.3a with $S_1S_2S_3 = 111$ mode signifies that all the switches are on; whereas, Figure 2.3h with $S_1S_2S_3 = 000$ mode signifies that all the switches are off. The rest of the modes can be similarly recognized from

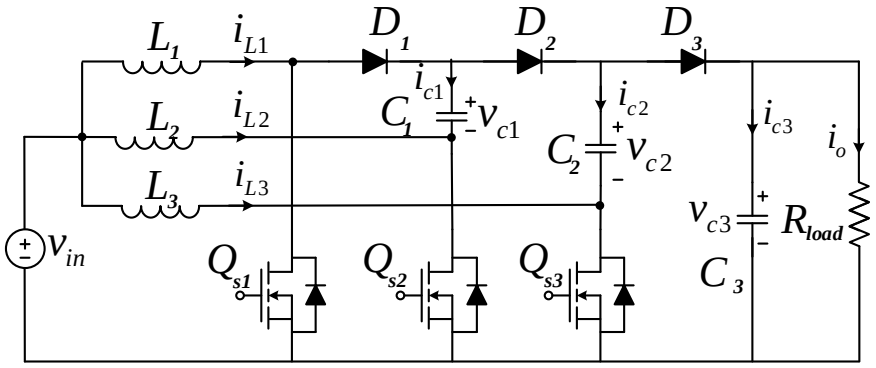


Figure 2.2: Topology for 3-Phase EDR Boost.

Figure 2.3b to Figure 2.3g. Figure 2.4 shows the typical gate signal, corresponding inductor current, and switch voltage stress in each of the operating zones for 3-phase converter.

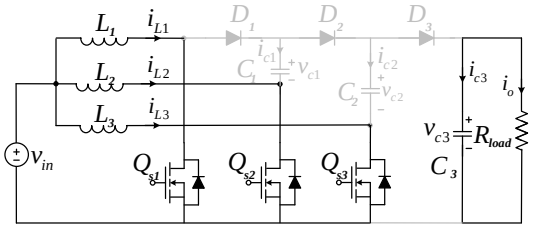
2.3.1 Zone I

Table 2.1 gives the detail of the operation in Zone I where duty ratio of each phase is equal and is beteween $2/3 \leq D \leq 1$. The switch states, time interval, and corresponding inductor current and capacitor voltage slopes have been tabulated along with the figure reference for the operating modes. It also gives the charging/discharging conditions of the passive component in these intervals denoted by $\uparrow$ and $\downarrow$ respectively. Figure 2.4a shows the typical gate signal, corresponding inductor current, and switch voltage stress, both the diode (denoted by V_D) and MOSFETs (denoted by V_{DS}) in this zone of operation, where $x_I = (D-2/3)T_s$ and $y_I = (1-D)T_s$.

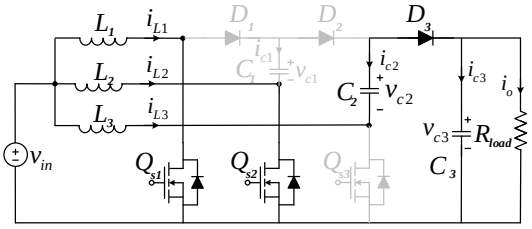
The voltage v_{cM} for each capacitor can be established in terms of the input voltage V_{in} by applying the inductor volt-second balance and is given by (2.4) where v_{c3} is also the output voltage, v_{out}.

$$v_{c1} = \frac{V_{in}}{(1-D)}; \qquad v_{c2} = \frac{2V_{in}}{(1-D)}; \qquad v_{c3} = \frac{3V_{in}}{(1-D)} \tag{2.4}$$

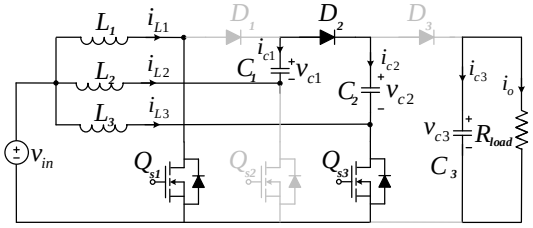
In this zone the input current is inherently shared among all the three boost phases. This can be analyzed from Table 2.1 by applying capacitor charge balance principle. As each of the intermediate capacitors are carrying current only in two operating intervals, it is straightforward to understand the inherent current share. For example, the charge balance of C_1 shows $i_{L1} = i_{L2}$. The current in each boost inductor is given by (2.5).



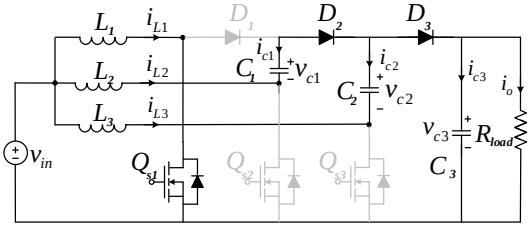
(a) $S_1S_2S_3 = 111$, possible mode in Zone I



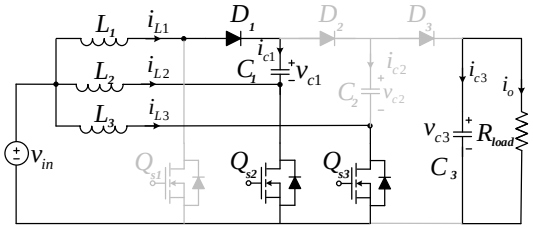
(b) $S_1S_2S_3 = 110$, possible mode in Zone I and Zone II



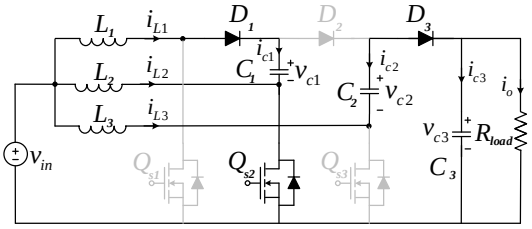
(c) $S_1S_2S_3 = 101$, possible mode in Zone I and Zone II



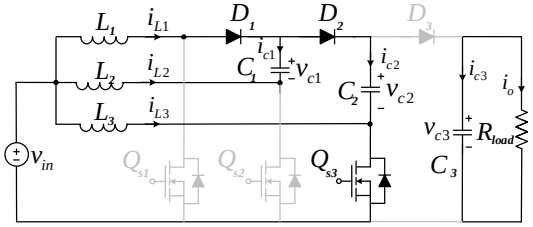
(d) $S_1S_2S_3 = 100$, possible mode in Zone II and Zone III



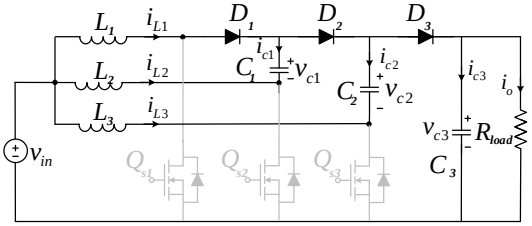
(e) $S_1S_2S_3 = 011$, possible mode in Zone I and Zone II



(f) $S_1S_2S_3 = 010$, possible mode in Zone II and Zone III

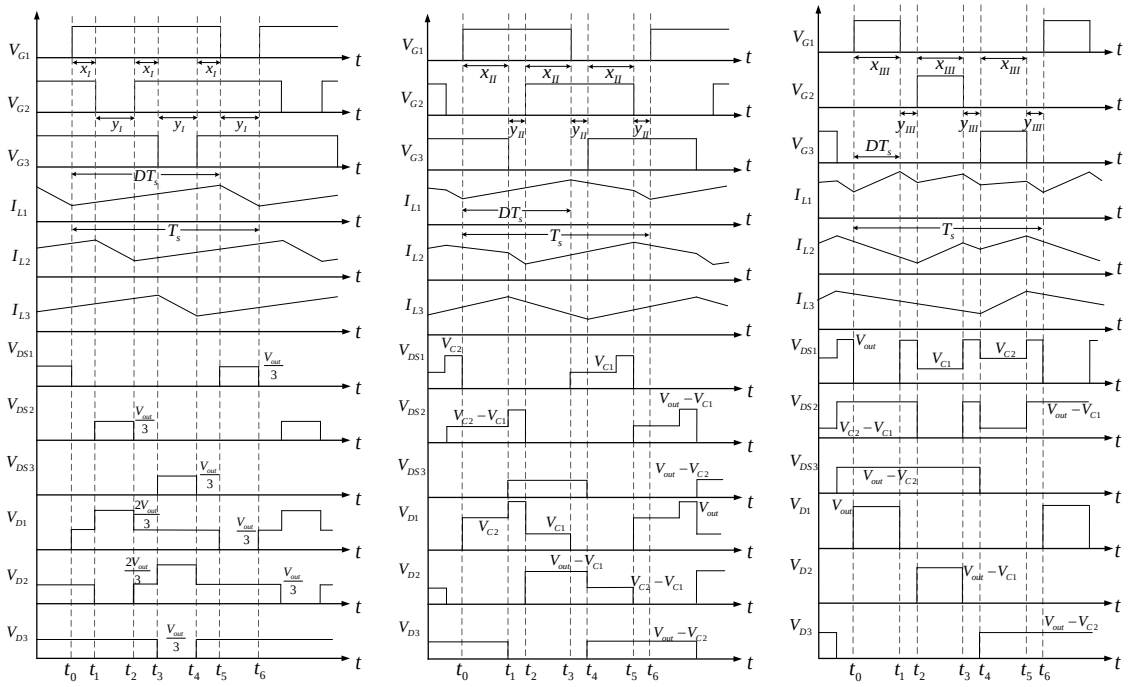


(g) $S_1S_2S_3 = 001$, possible mode in Zone II and Zone III



(h) $S_1S_2S_3 = 000$, possible mode in Zone III

Figure 2.3: Current Path Corresponding to Each of the Operating Intervals/Modes for 3-Phase EDR Boost.



(a) Zone I (b) Zone II (c) Zone III

Figure 2.4: Gate Signal, Inductor Current, and Device Voltage at Three Operating Zones for 3-Phase EDR Boost.

$$i_{L1} = i_{L2} = i_{L3} = \frac{i_o}{(1-D)} \tag{2.5}$$

Finally, the gain of the converter for this zone follows in (2.6). As v_{c1} and v_{c2} are integer fractions of v_{c3}, it is to be noted from Table 2.1 that the voltage applied across each input inductor is equivalent, i.e., they have the same voltage magnitude and duration, and thus equivalent current slope, but phase shifted by $360/3 = 120°$ for interleaving.

$$k_I = \frac{v_{c3}}{V_{in}} = \frac{i_{L1} + i_{L2} + i_{L3}}{i_o} = \frac{3}{(1-D)} \tag{2.6}$$

2.3.2 Zone II

Table 2.2 gives the details of the operation in Zone II where duty ratio of each phase is equal and is beteween $1/3 \leq D < 2/3$. Similar to Table 2.1 the details of the switch states, time interval, and corresponding inductor current and capacitor voltage are tabulated along with the figure reference for the operating modes. By applying inductor volt-second balance, the voltage v_{cM} for each capacitor is obtained and is given by following sets of equation.

$$v_{c1} = \frac{V_{in}(D^2 - 5D/3 + 7/9)}{(1-D)^3} \tag{2.7}$$

$$v_{c2} = \frac{V_{in}(D^2 - 2D + 10/9)}{(1-D)^3} \tag{2.8}$$

$$v_{c3} = \frac{V_{in}(2D^2 - 4D + 19/9)}{(1-D)^3} \tag{2.9}$$

It can be observed that unlike Zone I, the intermediate capacitor voltage is not an integer fraction of the output voltage. Figure 2.4b shows the typical gate signal, corresponding inductor current, and switch voltage stress both the diode (denoted by V_D) and MOSFETs (denoted by V_{DS}) in this zone of operation, where $x_{II} = (D - 1/3)T_s$ and $y_{II} = (2/3 - D)T_s$. The inductor current is derived by applying the capacitor charge balance principle and is given in (2.10)-(2.11).

$$i_{L1} = \frac{i_o}{(1-D)}; \qquad i_{L2} = \frac{i_o}{3(1-D)^2} \tag{2.10}$$

$$i_{L3} = \frac{i_o(D^2 - 5D/3 + 7/9)}{(1-D)^3} \tag{2.11}$$

It can be clearly noticed that current is not the same in each of the phases, it is the highest in phase 1, and the lowest in phase 2. (2.12) gives the converter gain in this operating zone.

$$k_{II} = \frac{v_{c3}}{V_{in}} = \frac{(2D^2 - 4D + 19/9)}{(1-D)^3} \tag{2.12}$$

2.3.3 Zone III

This is the zone for minimum converter gain with the least duty ratios. Table 2.3 gives the detail of the operation in Zone III where duty ratio of each phase is considered equal and is beteween $0 \leq D < 1/3$. Similar to the previous two Tables 2.1 and 2.2, the attributes of the switch states, time interval, and corresponding inductor current and capacitor voltage are tabulated along with the figure reference for the operating modes. The capacitor voltage v_{cM} is obtained by applying inductor volt-second balance, and is given in (2.13)-(2.14).

$$v_{c1} = \frac{V_{in}D}{(1-D)^3}; \qquad v_{c2} = \frac{V_{in}D(2-D)}{(1-D)^3} \tag{2.13}$$

$$v_{c3} = \frac{V_{in}}{(1-D)^3} \tag{2.14}$$

Similar to Zone II, the intermediate capacitor voltage is not an integer fraction of the output voltage. Thus from Table 2.3 and from v_{cM} expressions it can be seen that the inductor voltage of each phase is not equivalent to each other. The inductor current is derived by applying the capacitor charge balance principle and is given in (2.15).

$$i_{L1} = \frac{i_o}{(1-D)}; \quad i_{L2} = \frac{i_o D}{(1-D)^2}; \quad i_{L3} = \frac{i_o D}{(1-D)^3} \tag{2.15}$$

Even in this zone, the current is not the same in each phase; phase 1 has the highest current and phase 2 the least. Figure 2.4c shows the typical gate signal, corresponding inductor current, and switch voltage stress for this zone both the diode (denoted by V_D) and MOSFETs (denoted by V_{DS}), where $x_{III} = DT_s$ and $y_{III} = (1/3 - D)T_s$. (2.16) gives the converter gain in this operating zone.

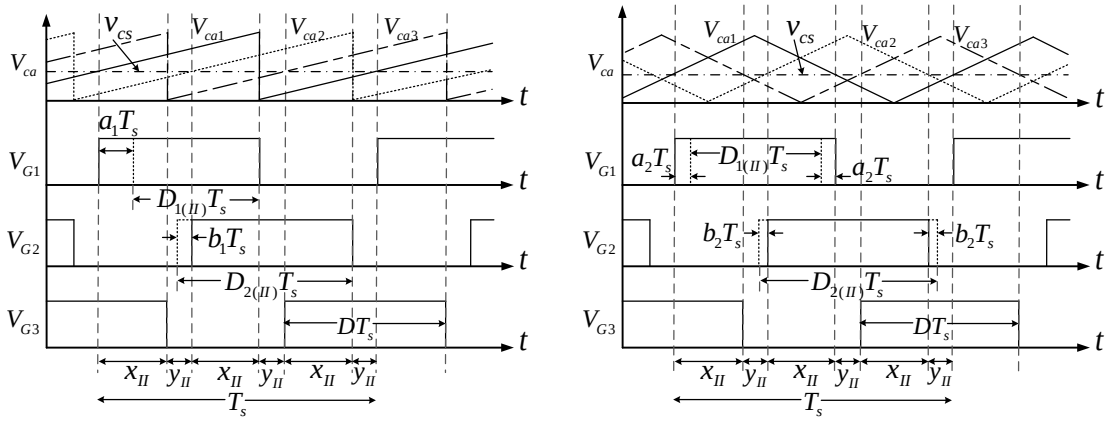
$$k_{III} = \frac{v_{c3}}{V_{in}} = \frac{1}{(1-D)^3} \tag{2.16}$$

2.4 Current Sharing

Equal duty ratio does not ensure equal current sharing except in Zone I, as mentioned in Section 2.3. Therefore, this paper proposes suitable adjustment of duty ratios for each phase to ensure equal current sharing or at least to minimize the current RMS error in the worst scenario. Since in Zone I current is inherently shared with duty ratio of all the phases being in the range of $2/3 \leq D \leq 1$, the discussion here would consider the remaining two operating zones. Depending on the operating zone, the correction of duty ratio of each phase would be different with the objective of either sharing the current equally between phases or minimizing the standard deviation of the current error.

2.4.1 Zone II

As shown in Section 2.3, in Zone II the current in phase 1 is the highest and that in phase 2 is the least, i.e., $i_{L1} > i_{L3} > i_{L2}$. Also from Table 2.2 and Figure 2.4b, it can be seen that i_{L1} is charged from t_0 to t_3 for an interval of DT_s and discharged from t_3 to t_6 for an interval of $(1 - D)T_s$. So to decrease the average of i_{L1}, it could be as simple as decreasing the duty ratio of phase 1 by a certain value, lets assume it a. Similar analysis would indicate increasing the duty ratio of phase 2 by b to



(a) Asymmetric PWM: true for $a_1T_s \leq x_{II}$ (b) Symmetric PWM: true for $a_2T_s \leq x_{II}$

Figure 2.5: Adjusted Duty Ratio for Three Phases to Balance Current in Zone II Operating Region for 3-Phase EDR Boost.

increase the average of i_{L2}, and keeping the duty ratio of phase 3 unchanged. The carrier signals (V_{ca1}, V_{ca2}, V_{ca3}) and modified duty ratios are shown in Figure 2.5 for two different pulse width modulation (PWM) generation schemes, asymmetric (saw-tooth carrier) and symmetric (triangle carrier) PWM. Finally, this modification of duty ratio of each phase would lead to the change in the converter gain, which is now an involved function of a, b, and D.

This section discusses the estimation of a and b for meeting the specified gain of the converter for Zone II operation for both asymmetric and symmetric PWM schemes. The operation with unequal duty ratios affects the two PWM schemes differently and imposes different restrictions on the limit of duty ratio modification. Thus the converter is analyzed separately in each of the two PWM schemes of operation.

Case I (Asymmetric PWM)

For asymmetric PWM, the duty control signal of phase 1 is decreased by a_1, and that of phase 2 is increased by b_1. Thus the modified duty ratio of each phase becomes: $D_{1(II)} = D - a_1$, $D_{2(II)} = D + b_1$, and $D_{3(II)} = D$. The corresponding gate and

carrier signals along with the primary control signal (v_{cs}) are shown in Figure 2.5a. The inductor current and capacitor voltage would be modified accordingly as involved functions of a_1, b_1, and D as given in (2.17)-(2.22) obtained by capacitor charge and inductor volt-second balance principles respectively.

$$i_{L1} = \frac{i_o}{\gamma}(1 - D - b_1) \tag{2.17}$$

$$i_{L2} = \frac{i_o}{\gamma}(1/3 + a_1 + b_1) \tag{2.18}$$

$$i_{L3} = \frac{i_o(D^2 - \frac{5}{3}D + \frac{7}{9} + 2Db_1 + \frac{a_1}{3} - \frac{5}{3}b_1 - a_1b_1)}{(1-D)\gamma} \tag{2.19}$$

$$v_{c1} = \frac{V_{in}D^2}{\zeta} - \frac{V_{in}(\frac{5}{9} - b_1^2 - a_1b_1 + \frac{5}{3}a_1 + \frac{4}{3}b_1)D}{(\frac{1}{3} + a_1 + b_1)\zeta} + \frac{V_{in}(\frac{7}{9}a_1 - \frac{2}{3}a_1b_1 - \frac{2}{3}b_1^2 + \frac{5}{9}b_1 + \frac{7}{27})}{(\frac{1}{3} + a_1 + b_1)\zeta} \tag{2.20}$$

$$v_{c2} = \frac{V_{in}}{\zeta}(D^2 - D(2 - b_1) + \frac{1}{3}a_1 - \frac{2}{3}b_1 + \frac{10}{9}) \tag{2.21}$$

$$v_{c3} = \frac{V_{in}}{\zeta}(2D^2 - D(4 + a_1 - 2b_1) + \frac{4}{3}a_1 - \frac{5}{3}b_1 - a_1b_1 + \frac{19}{9}) \tag{2.22}$$

where, $\zeta = (1-D)(D^2 - D(2 + a_1 - b_1) + (1 + a_1)(1 - b_1))$ and $\gamma = (1-D)^2 - D(a_1 - b_1) + a_1 - b_1 - a_1b_1$. To impose equal current sharing among all the phases, (2.23) needs to be satisfied (where k is the corresponding converter gain).

$$i_{L1} = i_{L2} = i_{L3} = \frac{ki_o}{3} \tag{2.23}$$

With further simplification of (2.17)-(2.19) by using (2.23), the condition for equal current among all the phases can be derived as (2.24).

$$a_1 = 2/3 - D; \quad b_1 = 0 \tag{2.24}$$

The relationship between duty ratio and gain in this operating region is given in (2.25) which is interestingly independent of a_1 and b_1.

$$k_{II(1)} = 1/(\frac{5}{9} - \frac{2}{3}D); \qquad D = \frac{1}{6}(5 - \frac{9}{k_{II(1)}}) \tag{2.25}$$

It is worth noting that this condition is only true for $a_1 T_s \leq x_{II}$, i.e., $a_1 \leq (D - 1/3)$, implying $D \geq 0.5$ beyond which the operating modes would no longer be the same as given in Table 2.2 for Zone II, and condition (2.24) would not anymore ensure equal current sharing. Finally by clubbing the condition in (2.25) it is seen that the minimum gain with asymmetric PWM in Zone II is 4.5, with the current being shared equally among the phases.

Case II (Symmetric PWM)

With the similar reasoning as the asymmetric PWM, the duty control signal of phase 1 in symmetric PWM is decreased by a_2, and that of phase 2 is increased by b_2 as shown in Figure 2.5b along with the carrier signals and the primary control signal (v_{cs}). Thus the modified duty ratio of each phase becomes: $D_{1(II)} = D - 2a_2$, $D_{2(II)} = D + 2b_2$, and $D_{3(II)} = D$. Similar to the asymmetric case, the corresponding inductor current and capacitor voltage would be altered as involved functions of a_2, b_2, and D which are not provided here to avoid lengthy repetition. The condition for equal current among all the phases can be derived as (2.26) by using (2.23).

$$a_2 = \frac{4}{5}(2/3 - D); \quad b_2 = \frac{2}{5}(2/3 - D) \tag{2.26}$$

Finally the relationship between duty ratio and gain in this operating region is given in (2.27) which is again independent of a_2 and b_2.

$$k_{II(2)} = 1/(\frac{23}{45} - \frac{3}{5}D); \qquad D = \frac{23}{27} - \frac{5}{3k_{II(2)}} \tag{2.27}$$

It is to be noted that this condition is only true for $a_2T_s \leq x_{II}$, i.e., $a_2 \leq (D-1/3)$, and $b_2T_s \leq y_{II}$, i.e., $b_2 \leq (2/3-D)$ Beyond these values, the operating modes would no longer be the same as given in Table 2.2 for Zone II, and (2.26) would not anymore ensure equal current sharing. The limit on a_2 is stringent than on b_2, in fact, the condition on b_2 is always true for (2.26). The limit on a_2 implies $D \geq 3/7$. Thus the range of duty ratio for which (2.23) is satisfied is expanded from asymmetric PWM scheme of $[2/3, 1/2]$ to symmetric PWM scheme of $[2/3, 3/7]$. Finally by clubbing the condition in (2.27) the minimum gain of 3.94 is obtained for this case with current being shared equally among the phases.

For the rest of the region in this zone i.e., for $1/3 \leq D < 3/7$, the converter duty ratio modification would be discussed in the next sub-section as the analysis would be similar to that of Zone III.

2.4.2 Zone III

In this zone the current in phase 1 is the highest and that in phase 2 is the least, i.e., $i_{L1} > i_{L3} > i_{L2}$ (shown in Section 2.3). Also from Table 2.3 and Figure 2.4c, it can be seen that i_{L3} is charged from t_4 to t_5 for an interval of D_3T_s and discharged from t_0 to t_4 and t_5 to t_6 for an interval of $(1 - D_3)T_s$, i_{L2} is charged for an interval of $(D_2 + D_3)T_s$ and discharged for an interval of $(1 - D_2 - D_3)T_s$, and i_{L1} is charged for an interval of $(D_1 + D_2 + D_3)T_s$ and discharged for an interval of $(1 - D_1 - D_2 - D_3)T_s$. From this discussion it is clear that the average of i_{L3} could be increased by increasing the duty ratio of phase 3. But it would also increase the average of the i_{L1} and i_{L2}.

With similar reasoning the average of i_{L2} cannot be increased with a simultaneous decrease of i_{L1} and thus current balance is not possible in this case with interleaved phases.

Case I ($1 \leq k_{III} \leq 3$)

The average of i_{L1} would be the minimum if the duty of phase 1 is set to 0, i.e., $D_{1(III)} = 0$ and the duty of other phases are varied according to the converter gain requirement. Figure 2.6 shows the duty ratio for this scenario, along with the modulating signals. V_M are now interleaved by $360/2 = 180°$, thus the converter would retain the operating modes of Zone III as discussed in Section 2.3 for $0 \leq D_{n(III)} \leq 1/2$ rather than for only $0 \leq D_{n(III)} \leq 1/3$, where $D_{n(III)}$ is the modified duty ratio of phase n in this zone; and the analysis would be less complex. The operation in this case for both the asymmetric and symmetric PWM would be similar.

The inductor current and capacitor voltage would be modified accordingly as a function of $D_{2(III)}$ and $D_{3(III)}$. The corresponding expressions are given in (2.28)-(2.33) obtained by capacitor charge and inductor volt-second balance principles respectively.

$$i_{L1} = i_o \tag{2.28}$$

$$i_{L2} = \frac{i_o D_{2(III)}}{(1 - D_{2(III)})} \tag{2.29}$$

$$i_{L3} = \frac{i_o D_{3(III)}}{(1 - D_{2(III)})(1 - D_{3(III)})} \tag{2.30}$$

$$v_{c1} = 0 \tag{2.31}$$

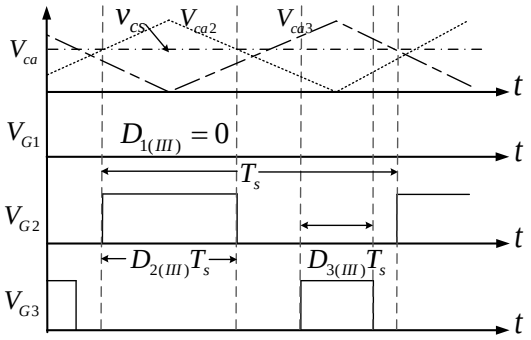


Figure 2.6: Adjusted Duty Ratio of Three Phases to Reduce the RMS Current Error in Zone III (Case 1) Operating Region for 3-Phase EDR Boost with $1 \leq k_{III} \leq 3$.

$$v_{c2} = \frac{V_{in} D_{2(III)}}{(1 - D_{2(III)})(1 - D_{3(III)})} \tag{2.32}$$

$$v_{c3} = \frac{V_{in}}{(1 - D_{2(III)})(1 - D_{3(III)})} \tag{2.33}$$

As i_{L1} in (2.28) is independent of the duty ratio, equal current sharing is not a function of $D_{2(III)}$ and $D_{3(III)}$ anymore, and under only one condition with $D_{2(III)} = 1/2$ and $D_{3(III)} = 1/3$, (2.23) holds true where each phase current is equal to i_o i.e., $i_{L1} = i_{L2} = i_{L3} = i_o = i_{in}/3$. And the converter gain at this condition is 3 as obtained from the converter gain relationship given in (2.34).

$$k_{III(1)} = \frac{1}{(1 - D_{2(III)})(1 - D_{3(III)})} \tag{2.34}$$

Further from (2.28)-(2.30) it is clear that for a given converter gain, the current in phase 1 is constant while that of phase 2 and 3 are variable depending on the values of $D_{2(III)}$ and $D_{3(III)}$. Thus a minimization problem to find the best combination of $D_{2(III)}$ and $D_{3(III)}$ can be formulated so as to decrease the per unit RMS error of the phase current i_e (2.35), with the equality constraint on converter gain (2.34) and inequality constraint on the duty ratios (2.36) ensuring no overlap of the phases with 180° interleaving.

$$i_e = \frac{1}{\sqrt{3} i_{in}} [(\frac{i_{in}}{3} - i_{L1})^2 + (\frac{i_{in}}{3} - i_{L2})^2 + (\frac{i_{in}}{3} - i_{L3})^2]^{0.5} \tag{2.35}$$

where, $i_{in} = i_{L1} + i_{L2} + i_{L3} = k_{III} i_o$

$$D_{2(III)} \leq 0.5 \qquad D_{3(III)} \leq 0.5 \tag{2.36}$$

This is a non-linear minimization and need not be solved on-line to save on the controller computation time. Optimization solver in MATLAB is used to solve the minimization problem and compute a look-up table in advance with the values of $D_{2(III)}$ and $D_{3(III)}$ vs $k_{III(1)}$ to be used during converter operation.

Alternatively, this can also be solved by Lagrange multiplier method with the problem formulation as defined in (2.37). Here, $\mathscr{L}$ is the Lagrangian with $f(D_{2(III)}, D_{3(III)})$ as the function to be minimized subject to the constraint $g(D_{2(III)}, D_{3(III)})$.

$$\begin{gathered} \mathscr{L} = f - \lambda g \qquad \text{where,} \quad f = i_e \\ \text{and} \quad g = k_{III} - \frac{1}{(1 - D_{2(III)})(1 - D_{3(III)})} = 0 \end{gathered} \tag{2.37}$$

(2.38) gives the duty ratio values in terms of the converter gain as obtained from solving the Lagrangian $\mathscr{L}$. The solution is similar to that obtained from the previous minimization technique from MATLAB.

$$D_{2(III)} = \frac{k_{III} - 1}{k_{III} + 1}; \qquad D_{3(III)} = \frac{D_{2(III)}}{1 + D_{2(III)}} \tag{2.38}$$

Case II $(3 \leq k_{III} \leq 3.94)$

Until now the converter operation with modified duty ratio is discussed with gain in the range of $[9, 3.94]$ and $[3, 1]$. For the rest of the operating region, the function would be mostly similar to case 1 in Zone III but with modified $D_{1(III)}$. In case

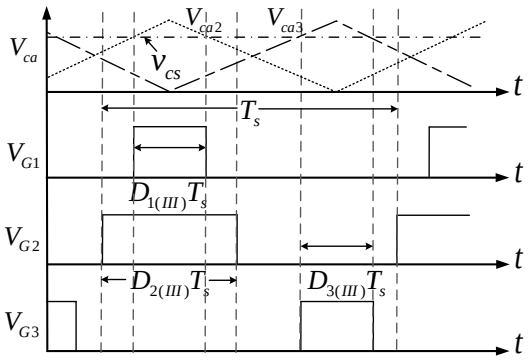


Figure 2.7: Modified Duty Ratio of Three Phases Ensuring Equal Current Sharing in Zone III (Case 2) for 3-Phase EDR Boost with $3 \leq k_{III} \leq 3.94$.

1, i_{L1} is always higher than corresponding i_{L2} and i_{L3}, whereas, with $k > 3$, i_{L1} becomes less than the rest two. Thus $D_{1(III)}$ is modified to be non-zero and overlap $D_{2(III)}$ in phase, which increases the average value of i_{L1} and modifies i_{L2} but has no effect on the converter gain or other capacitor voltages. The corresponding gate and modulating signals are shown in Figure 2.7.

The modified current expressions are given in (2.39) and (2.40), the rest of the variables remain the same as in case 1. Here the constraint (2.36) is modified to $D_{2(III)} + D_{3(III)} \leq 1$, and only with symmetrical PWM phase 2 and 3 overlapping is restricted, which are still 180° interleaved.

$$i_{L1} = \frac{i_o}{(1 - D_{1(III)})} \tag{2.39}$$

$$i_{L2} = \frac{i_o(D_{2(III)} - D_{1(III)})}{(1 - D_{1(III)})(1 - D_{2(III)})} \tag{2.40}$$

Again by applying (2.23), (2.41) is obtained, i.e., under this condition equal current sharing is ensured in this region.

$$D_{1(III)} = 1 - \frac{3}{k_{III(2)}}; \quad D_{2(III)} = \frac{1}{2} + \frac{D_{1(III)}}{2}$$

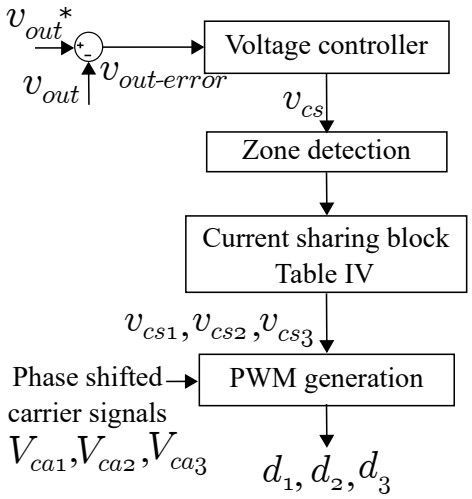


Figure 2.8: Implementation Flow Diagram of Current Sharing with Modified Duty Ratio for 3-Phase EDR Boost.

$$D_{3(III)} = 1/3 \tag{2.41}$$

2.4.3 Implementation

Table 2.4 provides the summary of operating duty ratio, the status of current sharing, and converter gain at different operating regions for a quick reference. Figure 2.8 shows the implementation flow diagram of current sharing with modified duty ratio for 3-phase EDR boost. The output voltage error (difference of a reference voltage and the sensed output voltage) is fed to a voltage controller to generate a common control signal v_{cs}. The operating zone is determined based on its value which then determines the individual control signal for each phase in the current sharing block. Finally, the corresponding PWM signals are generated by comparing the control signals with the phase shifted carrier signals.

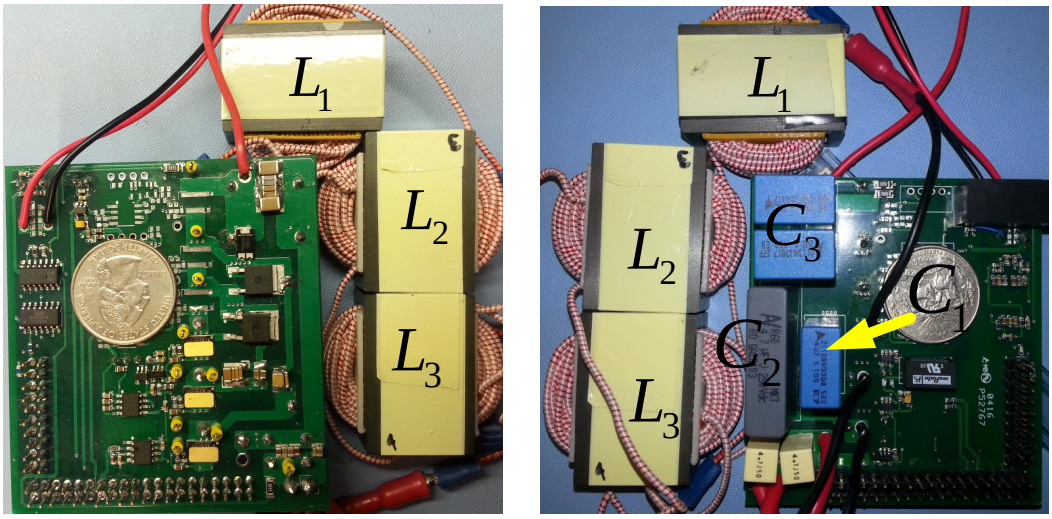
2.5 Discontinuous Conduction Mode

The EDR boost converter might also potentially operate in discontinuous conduction mode (DCM) when the load current is quite low. For an M phase converter, all the boost inductors would still share the current equally inherently in each of Zone I to Zone $M-1$, while only Zone M would not experience inherent equal current sharing. In fact, in Zone M, the inductor current for phases 2 to M will have negative excursion (phase 1 is defined as the one which is closest to the input as seen from Figure 2.1) which would lead to circulating current resulting in higher RMS current of all the inductors, diodes, and MOSFETs, and consequently lower efficiency. Whereas, in buck version of EDR converter, the DCM operation would lead to negative current excursion and uneven current sharing in all the possible operating zones. Shenoy and Amaro [80] has proposed an improved interleaving technique to address the negative phase current problem in 2-phase converter by uneven phase interleaving approach. In this chapter, the analysis of improved modulation technique for equal phase current sharing is primarily focused on the CCM operation of EDR boost.

2.6 Experimental Results

2.6.1 Hardware Prototype

A 250 W GaN based hardware prototype for 3-phase EDR boost as shown in Figure 2.9, has been built to validate the current sharing concept. Table 2.5 and Table 2.6 give the converter specifications and the passive and active component details for the hardware set-up respectively. The inductors are designed based on a specified ripple current percentage on each of the phase in Zone I operation, this is the zone which sees inherent current sharing among the boost inductors and each inductor is subjected to same voltage waveform (as seen from Figure 2.4a). So the



(a) Top view (b) Bottom view

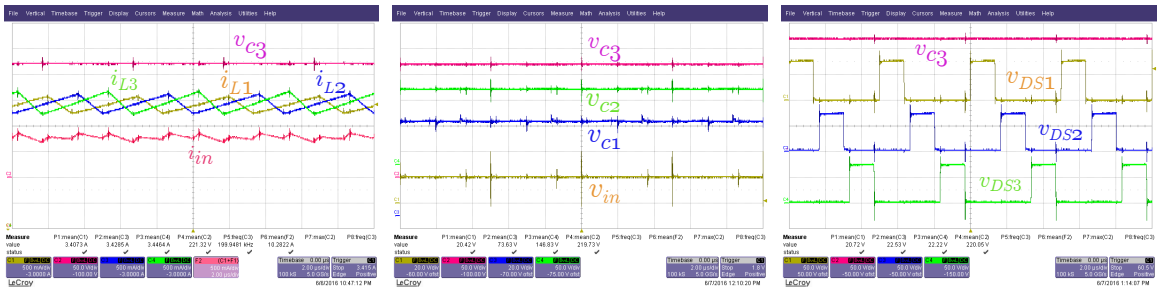
Figure 2.9: Experimental Prototype for 3-Phase EDR Boost.

inductor values are equal for each phase.

UCC27511 from TI has been used as gate driver with the provision for independent turn-on and turn-off gate resistors which is critical for operation with GaN devices at relatively high switching frequency. Digital isolator Si8610BB from Silicon Labs is used for isolating the PWM signals from the control and power sections. The auxiliary power supply for the control section is derived externally. EZDSP TMSF28335 has been used to generate the 200 kHz interleaved PWM signals. LeCroy 6200A oscilloscope is used to capture the relevant waveforms and power analyzer YOKOGAWA WT3000 is used to measure the efficiency.

2.6.2 Converter Operation Without Duty Ratio Adjustment

The input current, individual inductor current, input and output voltage, intermediate capacitor voltage, and the device drain-source voltage v_{DS} have been shown in Figs. 2.10, 2.11, and 2.12 respectively for each of the operating zones. For Zone I, the conversion is from 20 V to 220 V at 200 W with duty ratio of 0.73 for each



(a) Inductor currents (b) Capacitor voltages (c) Device drain-source voltages

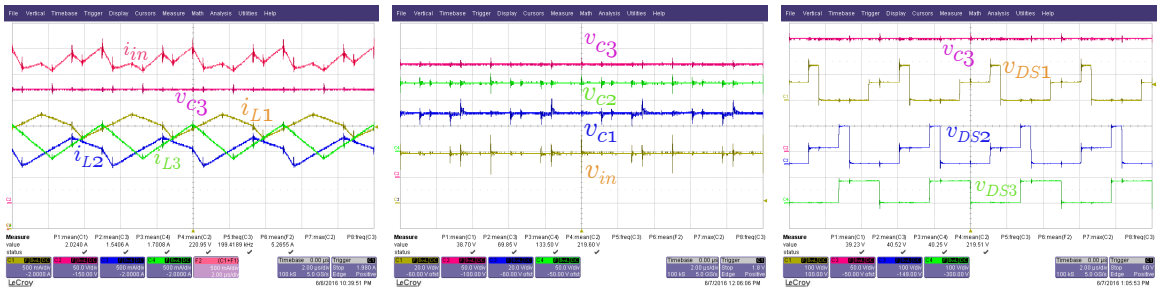
Figure 2.10: Waveforms for Zone I 3-phase EDR boost with $D_1 = D_2 = D_3 = 0.73$ operating from 20 V to 220 V at 200 W (current: 0.5 A/div, v_{in}, v_{c1} : 20 V/div, v_{c2}, v_{c3} : 50 V/div, $v_{DS1}, v_{DS2}, v_{DS3}$: 50 V/div, time : 2 μs/div).

phase. The input current is shared equally and v_{DS} is same for all phases, the input current has reduced ripple, the switch stress is $1/3^{rd}$ of the output voltage, and the intermediate capacitor voltages are $1/3^{rd}$ and $2/3^{rd}$ of the output voltage respectively. A peak efficiency of 96.06% is obtained in this operating condition.

For Zone II, the conversion is from 40 V to 220 V at 200 W with duty ratio of 0.55 for each phase. v_{DS} is not the same for all the phases, the switch stress for Q_{s1} is V_{c2}, whereas, for Q_{s2} and Q_{s3} it is $V_{out} - V_{c1}$ and $V_{out} - V_{c2}$ respectively. A peak efficiency of 96.01% is obtained in this operating condition.

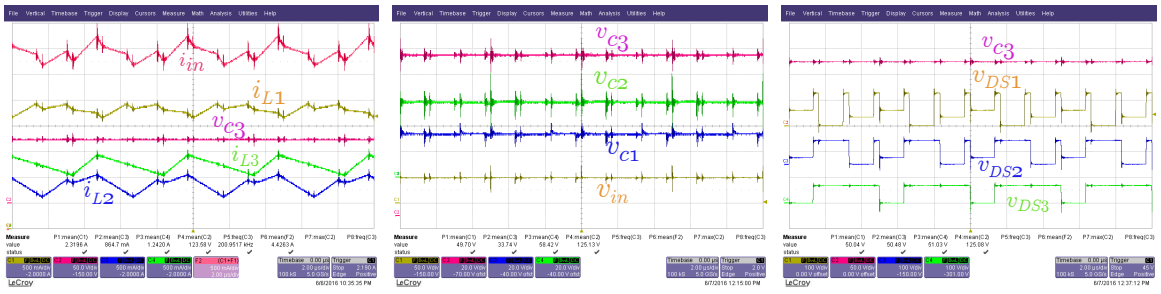
For Zone III, the converter is operated from 50 V to 125 V at 220 W with duty ratio of 0.27 for each phase. Even in this zone, v_{DS} is not the same for all phases, in fact Q_{s1} encounter full output voltage, whereas, Q_{s2} and Q_{s3} experience the same voltage stress as in Zone II. Due to the limitation of the component voltage ratings, the operation of Zone III is shown for a maximum of 50 V input to 125 V output. A peak efficiency of 94.28% is obtained in this operating condition.

As expected, the inductor current is not equally shared between the phases for Zones II and III and the input current has higher ripple. For better visualization, each inductor current are captured with the same current offset in the scope. As expressions for voltage and current in different operating zones have been derived for



(a) Inductor currents (b) Capacitor voltages (c) Device drain-source voltages

Figure 2.11: Waveforms for Zone II 3-phase EDR boost with $D_1 = D_2 = D_3 = 0.55$ operating from 40 V to 220 V at 200 W (current: 0.5 A/div, v_{in}, v_{c1} : 20 V/div, v_{c2}, v_{c3} : 50 V/div, $v_{DS1}, v_{DS2}, v_{DS3}$: 100 V/div, time : 2 μs/div).



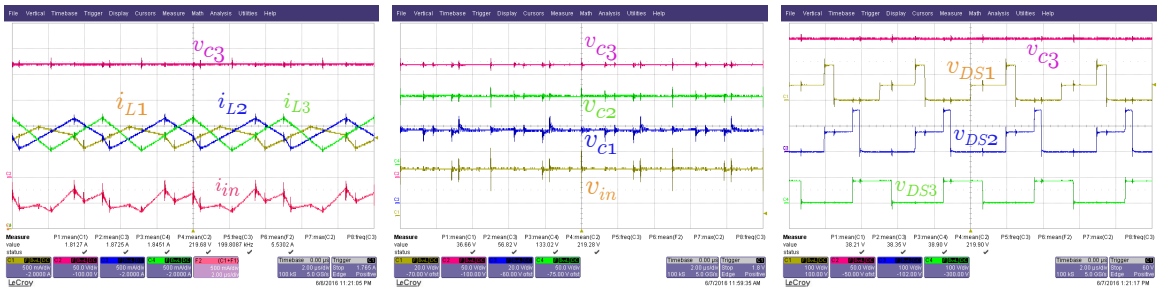
(a) Inductor currents (v_{c3} : 50 V/div) (b) Capacitor voltages (v_{c3} : 20 V/div) (c) Device drain-source voltages (v_{c3} : 50 V/div)

Figure 2.12: Waveforms for Zone III 3-phase EDR boost with $D_1 = D_2 = D_3 = 0.27$ operating from 50 V to 125 V at 220 W (current: 0.5 A/div, v_{in} : 50 V/div, v_{c1}, v_{c2} : 20 V/div, $v_{DS1}, v_{DS2}, v_{DS3}$: 100 V/div, time : 2 μs/div).

ideal case in Section 2.3, the experimental values can be verified to be very close to that computed from these equations.

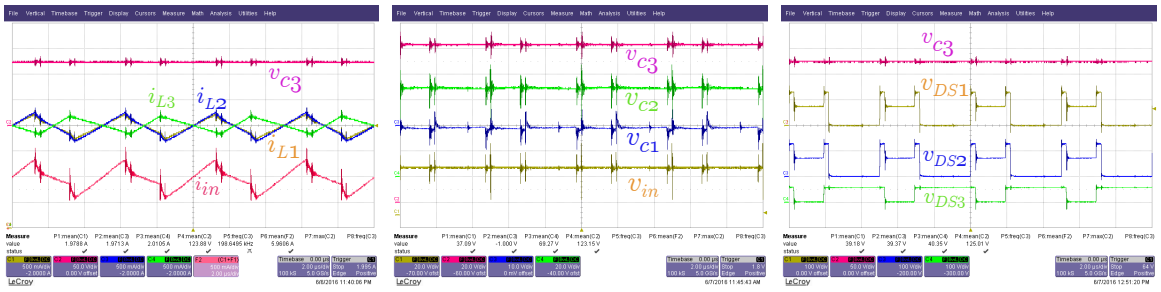
2.6.3 Converter Operation With Duty Ratio Adjustment

The input current, individual inductor current, input and output voltage, intermediate capacitor voltage, and the device drain-source voltage have been shown in Figure 2.13 for Zone II operation with symmetric PWM. The converter is operated from 36 V to 220 V at 200 W with duty ratio of 0.57 for phase 3, and for other phases it is calculated from expression given in Table 2.4. v_{DS} is same as that of non-adjusted



(a) Inductor currents (b) Capacitor voltages (c) Device drain-source voltages

Figure 2.13: Waveforms with modified duty ratio scheme for Zone II 3-phase EDR boost with symmetric PWM, $D_3 = 0.57$ and D_1 and D_2 calculated from expression given in Table 2.4, operating from 36 V to 220 V at 200 W (current: 0.5 A/div, v_{in}, v_{c1} : 20 V/div, v_{c2}, v_{c3} : 50 V/div, $v_{DS1}, v_{DS2}, v_{DS3}$: 100 V/div, time : 2 μs/div).

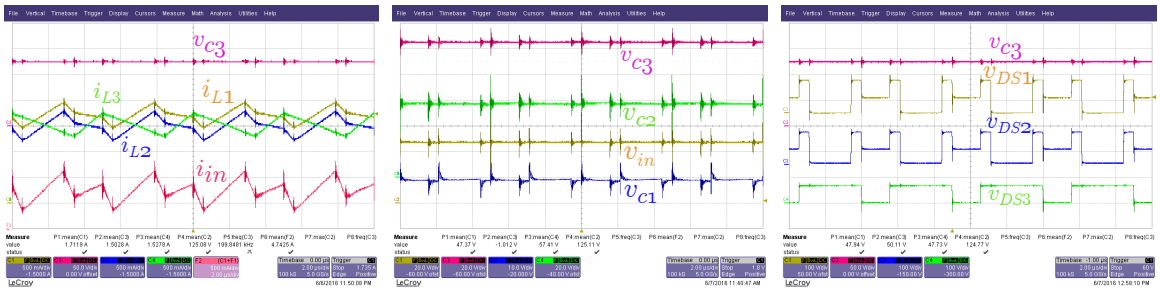


(a) Inductor currents (v_{c3} : 50 V/div) (b) Capacitor voltages (v_{c3} : 20 V/div) (c) Device drain-source voltages (v_{c3} : 50 V/div)

Figure 2.14: Waveforms with modified duty ratio scheme for Zone III (Modified D-higher gain) 3-phase EDR boost with symmetric 180° interleaved PWM, D_1 and D_2 in phase, $D_1 = 0.18$, $D_3 = 0.33$ and D_2 calculated from expression given in Table 2.4, operating from 37 V to 125 V at 220 W (current: 0.5 A/div, v_{in}, v_{c2} : 20 V/div, v_{c1} : 10 V/div v_{DS1}, v_{DS2}, v_{DS3} : 100 V/div, time : 2 μs/div).

duty ratio Zone II operation as discussed in Section 2.6.2. A peak efficiency of 96.27% is obtained in this operating condition.

Figs. 2.14 and 2.15 respectively give the input current, individual inductor current, input and output voltage, intermediate capacitor voltage, and the device drain-source voltage waveforms for both modified D-higher gain and modified D-lower gain regions in Zone III operation. For former with symmetric 180° interleaved PWM, the converter is operated from 37 V to 125 V at 220 W with duty ratio of 0.18 for phase 1,



(a) Inductor currents (v_{c3} : 50 V/div)

(b) Capacitor voltages (v_{c3} : 20 V/div)

(c) Device drain-source voltages (v_{c3} : 50 V/div)

Figure 2.15: Waveforms with modified duty ratio scheme for Zone III (Modified D-lower gain) 3-phase EDR boost with symmetric 180° interleaved PWM, $D_1 = 0$, $D_2 = 0.46$ and D_3 calculated from expression given in Table 2.4, operating from 47 V to 125 V at 220 W (current: 0.5 A/div, v_{in}, v_{c2} : 20 V/div, v_{c1} : 10 V/div v_{DS1}, v_{DS2}, v_{DS3} : 100 V/div, time : 2 μs/div).

0.33 for phase 3, and for phase 2 it is calculated from expression given in Table 2.4, also D_1 and D_2 are in phase. For modified D-lower gain region with symmetric 180° interleaved PWM, it is operated from 47 V to 125 V at 220 W with duty ratio of 0 for phase 1, 0.46 for phase 2, and for phase 3 it is calculated from expression given in Table 2.4. A peak efficiency of 94.67% is obtained in this operating condition. The voltage stress on the switches in each of these two cases is the same as that of non-adjusted duty ratio operation in Zone III discussed in Section 2.6.2.

With the proposed duty ratio scheme, it is shown that equal current sharing among the three phases has been achieved for Zone II and Zone III modified D-higher gain region (Figs. 2.13a and 2.14a respectively), and for Zone III in modified D-lower gain region (Figure 2.15a) the RMS current error has been significantly reduced. The voltage and current values can be verified to be very close to that obtained from the equations in Section 2.4 which were derived assuming ideal converter operation.

2.7 Conclusion

EDR boost has been studied for high step-up application. Comprehensive analysis of converter operating principles, key theoretical waveforms, and steady state circuit performance corresponding to all the possible zones of operation have been presented. Methods for sensor-less current sharing among the different phases of the 3-phase EDR boost have been introduced. It is shown that inherent current sharing in three boost phases is only possible in Zone I operation. For Zones II and III equal current sharing can only be ensured with adapted duty ratio scheme until certain range of converter gain. Beyond this, though the current cannot be shared equally among phases, the per unit RMS current error can be minimized with modified duty ratio value and phase. The sharing scheme has been convincingly demonstrated in a 250 W GaN based hardware prototype for different operating regions.

Table 2.1: Zone I $(2/3 \leq D \leq 1)$ Operating Modes

Mode	**Ref Fig.**	**Switch** $S_1S_2S_3$	**Time**	**Inductor current slope**			**Capacitor voltage slope**		
				L_1	L_2	L_3	C_1	C_2	C_3
1	2.3a	111	x_I	$\uparrow \frac{V_{in}}{L_1}$	$\uparrow \frac{V_{in}}{L_2}$	$\uparrow \frac{V_{in}}{L_3}$	0	0	$\downarrow \frac{-i_o}{C_3}$
2	2.3c	101	y_I	$\uparrow \frac{V_{in}}{L_1}$	$\downarrow \frac{V_{in}+v_{c1}-v_{c2}}{L_2}$	$\uparrow \frac{V_{in}}{L_3}$	$\downarrow \frac{-i_{L2}}{C_1}$	$\uparrow \frac{i_{L2}}{C_2}$	$\downarrow \frac{-i_o}{C_3}$
3	2.3a	111	x_I	$\uparrow \frac{V_{in}}{L_1}$	$\uparrow \frac{V_{in}}{L_2}$	$\uparrow \frac{V_{in}}{L_3}$	0	0	$\downarrow \frac{-i_o}{C_3}$
4	2.3b	110	y_I	$\uparrow \frac{V_{in}}{L_1}$	$\uparrow \frac{V_{in}}{L_2}$	$\downarrow \frac{V_{in}+v_{c2}-v_{c3}}{L_3}$	0	$\downarrow \frac{-i_{L3}}{C_2}$	$\uparrow \frac{i_{L3}-i_o}{C_3}$
5	2.3a	111	x_I	$\uparrow \frac{V_{in}}{L_1}$	$\uparrow \frac{V_{in}}{L_2}$	$\uparrow \frac{V_{in}}{L_3}$	0	0	$\downarrow \frac{-i_o}{C_3}$
6	2.3e	011	y_I	$\downarrow \frac{V_{in}-v_{c1}}{L_1}$	$\uparrow \frac{V_{in}}{L_2}$	$\uparrow \frac{V_{in}}{L_3}$	$\uparrow \frac{i_{L1}}{C_1}$	0	$\downarrow \frac{-i_o}{C_3}$

$\uparrow$ denotes charging, $\downarrow$ denotes discharging of inductor and capacitor

$x_I = (D - 2/3)T_s$ and $y_I = (1 - D)T_s$

Table 2.2: Zone II $(1/3 \leq D < 2/3)$ Operating Modes

Mode	Ref Fig.	Switch $S_1S_2S_3$	Time	Inductor current slope			Capacitor voltage slope		
				L_1	L_2	L_3	C_1	C_2	C_3
1	2.3c	101	x_{II}	$\uparrow \frac{V_{in}}{L_1}$	$\downarrow \frac{V_{in}+v_{c1}-v_{c2}}{L_2}$	$\uparrow \frac{V_{in}}{L_3}$	$\downarrow \frac{-i_{L2}}{C_1}$	$\uparrow \frac{i_{L2}}{C_2}$	$\downarrow \frac{-i_o}{C_3}$
2	2.3d	100	y_{II}	$\uparrow \frac{V_{in}}{L_1}$	$\downarrow \frac{V_{in}+v_{c1}-v_{c3}}{L_2}$	$\downarrow \frac{V_{in}+v_{c2}-v_{c3}}{L_3}$	$\downarrow \frac{-i_{L2}}{C_1}$	$\downarrow \frac{-i_{L3}}{C_2}$	$\uparrow \frac{i_{L2}+i_{L3}-i_o}{C_3}$
3	2.3b	110	x_{II}	$\uparrow \frac{V_{in}}{L_1}$	$\uparrow \frac{V_{in}}{L_2}$	$\downarrow \frac{V_{in}+v_{c2}-v_{c3}}{L_3}$	0	$\downarrow \frac{-i_{L3}}{C_2}$	$\uparrow \frac{i_{L3}-i_o}{C_3}$
4	2.3f	010	y_{II}	$\downarrow \frac{V_{in}-v_{c1}}{L_1}$	$\uparrow \frac{V_{in}}{L_2}$	$\downarrow \frac{V_{in}+v_{c2}-v_{c3}}{L_3}$	$\uparrow \frac{i_{L1}}{C_1}$	$\downarrow \frac{-i_{L3}}{C_2}$	$\uparrow \frac{i_{L3}-i_o}{C_3}$
5	2.3e	011	x_{II}	$\downarrow \frac{V_{in}-v_{c1}}{L_1}$	$\uparrow \frac{V_{in}}{L_2}$	$\uparrow \frac{V_{in}}{L_3}$	$\uparrow \frac{i_{L1}}{C_1}$	0	$\downarrow \frac{-i_o}{C_3}$
6	2.3g	001	y_{II}	$\downarrow \frac{V_{in}-v_{c2}}{L_1}$	$\downarrow \frac{V_{in}+v_{c1}-v_{c2}}{L_2}$	$\uparrow \frac{V_{in}}{L_3}$	$\downarrow \frac{-i_{L2}}{C_1}$	$\uparrow \frac{i_{L1}+i_{L2}}{C_2}$	$\downarrow \frac{-i_o}{C_3}$

$\uparrow$ denotes charging, $\downarrow$ denotes discharging of inductor and capacitor

$x_{II} = (D - 1/3)T_s$ and $y_{II} = (2/3 - D)T_s$

Table 2.3: Zone III $(0 \leq D < 1/3)$ Operating Modes

Mode	Ref Fig.	Switch $S_1S_2S_3$	Time	Inductor current slope			Capacitor voltage slope		
				L_1	L_2	L_3	C_1	C_2	C_3
1	2.3d	100	x_{III}	$\uparrow \frac{V_{in}}{L_1}$	$\underset{\downarrow}{\frac{V_{in}+v_{c1}-v_{c3}}{L_2}}$	$\underset{\downarrow}{\frac{V_{in}+v_{c2}-v_{c3}}{L_3}}$	$\downarrow \frac{-i_{L2}}{C_1}$	$\downarrow \frac{-i_{L3}}{C_2}$	$\uparrow \frac{i_{L2}+i_{L3}-i_o}{C_3}$
2	2.3h	000	y_{III}	$\underset{\downarrow}{\frac{V_{in}-v_{c3}}{L_1}}$	$\underset{\downarrow}{\frac{V_{in}+v_{c1}-v_{c3}}{L_2}}$	$\underset{\downarrow}{\frac{V_{in}+v_{c2}-v_{c3}}{L_3}}$	$\downarrow \frac{-i_{L2}}{C_1}$	$\downarrow \frac{-i_{L3}}{C_2}$	$\underset{\uparrow}{\frac{i_{L1}+i_{L2}+i_{L3}-i_o}{C_3}}$
3	2.3f	010	x_{III}	$\underset{\uparrow}{\frac{V_{in}-v_{c1}}{L_1}}$	$\uparrow \frac{V_{in}}{L_2}$	$\underset{\downarrow}{\frac{V_{in}+v_{c2}-v_{c3}}{L_3}}$	$\uparrow \frac{i_{L1}}{C_1}$	$\downarrow \frac{-i_{L3}}{C_2}$	$\uparrow \frac{i_{L3}-i_o}{C_3}$
4	2.3h	000	y_{III}	$\underset{\downarrow}{\frac{V_{in}-v_{c3}}{L_1}}$	$\underset{\downarrow}{\frac{V_{in}+v_{c1}-v_{c3}}{L_2}}$	$\underset{\downarrow}{\frac{V_{in}+v_{c2}-v_{c3}}{L_3}}$	$\downarrow \frac{-i_{L2}}{C_1}$	$\downarrow \frac{-i_{L3}}{C_2}$	$\underset{\uparrow}{\frac{i_{L1}+i_{L2}+i_{L3}-i_o}{C_3}}$
5	2.3g	001	x_{III}	$\underset{\uparrow}{\frac{V_{in}-v_{c2}}{L_1}}$	$\underset{\uparrow}{\frac{V_{in}+v_{c1}-v_{c2}}{L_2}}$	$\uparrow \frac{V_{in}}{L_3}$	$\downarrow \frac{-i_{L2}}{C_1}$	$\uparrow \frac{i_{L1}+i_{L2}}{C_2}$	$\downarrow \frac{-i_o}{C_3}$
6	2.3h	000	y_{III}	$\underset{\downarrow}{\frac{V_{in}-v_{c3}}{L_1}}$	$\underset{\downarrow}{\frac{V_{in}+v_{c1}-v_{c3}}{L_2}}$	$\underset{\downarrow}{\frac{V_{in}+v_{c2}-v_{c3}}{L_3}}$	$\downarrow \frac{-i_{L2}}{C_1}$	$\downarrow \frac{-i_{L3}}{C_2}$	$\underset{\uparrow}{\frac{i_{L1}+i_{L2}+i_{L3}-i_o}{C_3}}$

$\uparrow$ denotes charging, $\downarrow$ denotes discharging of inductor and capacitor
$x_{III} = DT_s$ and $y_{III} = (1/3 - D)T_s$

Table 2.4: Gain Summary

Condition	**Current sharing**	**Duty ratio**	**Ideal gain**	
Zone I	Inherent sharing with equal D	$\frac{2}{3} \leq D_1 = D_2 = D_3 \leq 1$	$\frac{3}{(1-D)}$	$\infty - 9$
Zone II	Typically not shared with equal D	$\frac{1}{3} \leq D_1 = D_2 = D_3 \leq \frac{2}{3}$	$\frac{(2D^2 - 4D + 19/9)}{(1-D)^3}$	$9 - 3.375$
	Modified D (Asym PWM) - shared equally	$D_1 = 2D - \frac{2}{3}$; $D_2 = D_3 = D$; $\frac{1}{2} \leq D \leq \frac{2}{3}$	$\left(\frac{5}{9} - \frac{2}{3}D\right)^{-1}$	$9 - 4.5$
	Modified D (Sym PWM) - shared equally	$D_1 = \frac{13}{5}D - \frac{16}{15}$; $D_2 = \frac{1}{5}D + \frac{8}{15}$; $D_3 = D$; $\frac{3}{7} \leq D \leq \frac{2}{3}$	$\left(\frac{23}{45} - \frac{3}{5}D\right)^{-1}$	$9 - 3.94$
Zone III	Typically not shared with equal D	$0 \leq D_1 = D_2 = D_3 \leq \frac{1}{3}$	$\frac{1}{(1-D)^3}$	$3.375 - 1$
	Modified D-higher gain (case 2) - shared equally	$D_1 = D$; $D_2 = \frac{1}{2} + \frac{1}{2}D$; $D_3 = \frac{1}{3}$, 180° interleaving with D_1 in phase with D_2	$\frac{1}{(1-D_2)(1-D_3)}$	$3.94 - 3$
	Modified D-lower gain (case 1) - RMS error minimized	$D_1 = 0$; $D_2 = D$; $D_3 = \frac{D_2}{1+D_2}$, 180° interleaving	$\frac{1}{(1-D_2)(1-D_3)}$	$3 - 1$

Table 2.5: Converter Specification

Parameter	**Rating**
Input	20-50 V
Output	220 V, 250 W
Switching frequency	200 kHz

Table 2.6: Component Details

Component	**Parameters**
C_1 , C_2 , C_3	4.7 μF/ 100 V, 4.7 μF/ 200 V, 4.7 μF/ 300 V
L_1 , L_2 , L_3	180 μH
Q_{s1} , Q_{s2} , Q_{s3}	GS66508P
D_1 , D_2 , D_3	C3D04060E (2), SBR10U200

Chapter 3

DISCONTINUOUS CONDUCTION MODE OPERATION OF EDR BOOST CONVERTER

3.1 Introduction

The extended duty ratio (EDR) converter shows interesting performance features and current sharing characteristics in the discontinuous conduction mode (DCM) operation. For an M-phase converter in DCM, all the boost inductors would still share the current equally inherently in each of Zone I to Zone M-1, while only Zone M (the least gain region) would not experience inherent equal current sharing. In fact, in Zone M, the inductor current for phases 2 to M will have negative excursion at certain operating interval. A comprehensive analysis of the operation of 3-phase EDR boost converter in each of its operating zones is presented in this chapter. Further, the results are validated from the GaN-based 3-phase 100 W experimental prototype.

3.2 Operating Principles

Figure 3.1 shows the 3-phase EDR boost converter, the circuit configuration is already discussed in the previous chapter. Like continuous conduction mode (CCM), for DCM operation too it has three different operating zones. With equal duty ratio for each phase and a phase shift of 120° between them, the input current is shared between the interleaved phases for operating Zones I and II, while for Zone III it is still not shared. Moreover, Zone III operation has multiple cases depending on the duty ratio and the average input current of the converter with different combination of operating modes as discussed shortly.

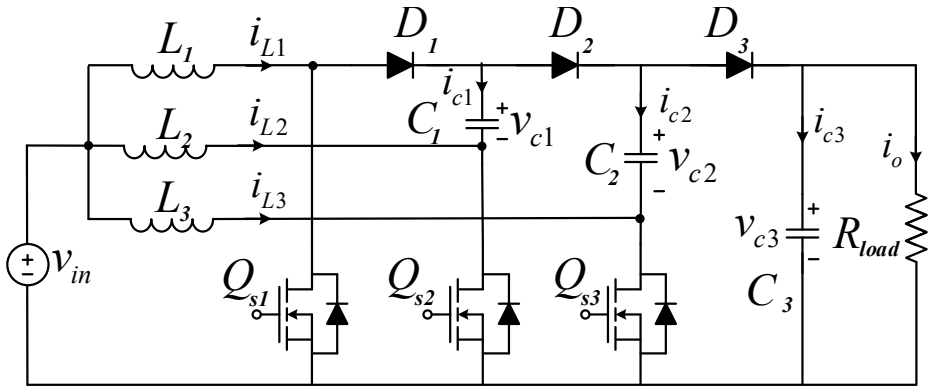


Figure 3.1: Topology for 3-Phase Extended Duty Ratio (EDR) Boost Converter.

The boundary between CCM and DCM operation can be derived in a similar way to the conventional boost converter. For DCM operation, the average inductor current for each phase i_{Li_avg} should be less than its corresponding peak-peak ripple Δi_{Li} which leads to the following condition for DCM.

$$\frac{2L}{RT_s} < \frac{DD'^2}{3} \tag{3.1}$$

The dimensionless parameter k is defined by $k = \frac{2L}{RT_s}$ and its critical value k_{crit} for DCM can be identified form (3.1). Smaller value of $k < k_{crit}$ leads to the discontinuous operation of the EDR converter.

3.2.1 Zone I Operation

Zone I corresponds to the duty ratio range $2/3 \leq D < 1$. For DCM operation, Figure 3.2 shows the typical gate signal, corresponding inductor current, and switch voltage stress of both the diode (denoted by V_D) and MOSFETs (denoted by V_{DS}) in this zone of operation, where $x_I = (D - 2/3)T_s$ and $y_I = (1 - D)T_s$. The maximum voltage stress for each device has been marked. It can be seen that all the switches experience a voltage stress of $v_o/3$, while it is $2v_o/3$ for the diodes of first two phases and $v_o/3$ for the third one. Also, the inductor currents are equivalent in all three

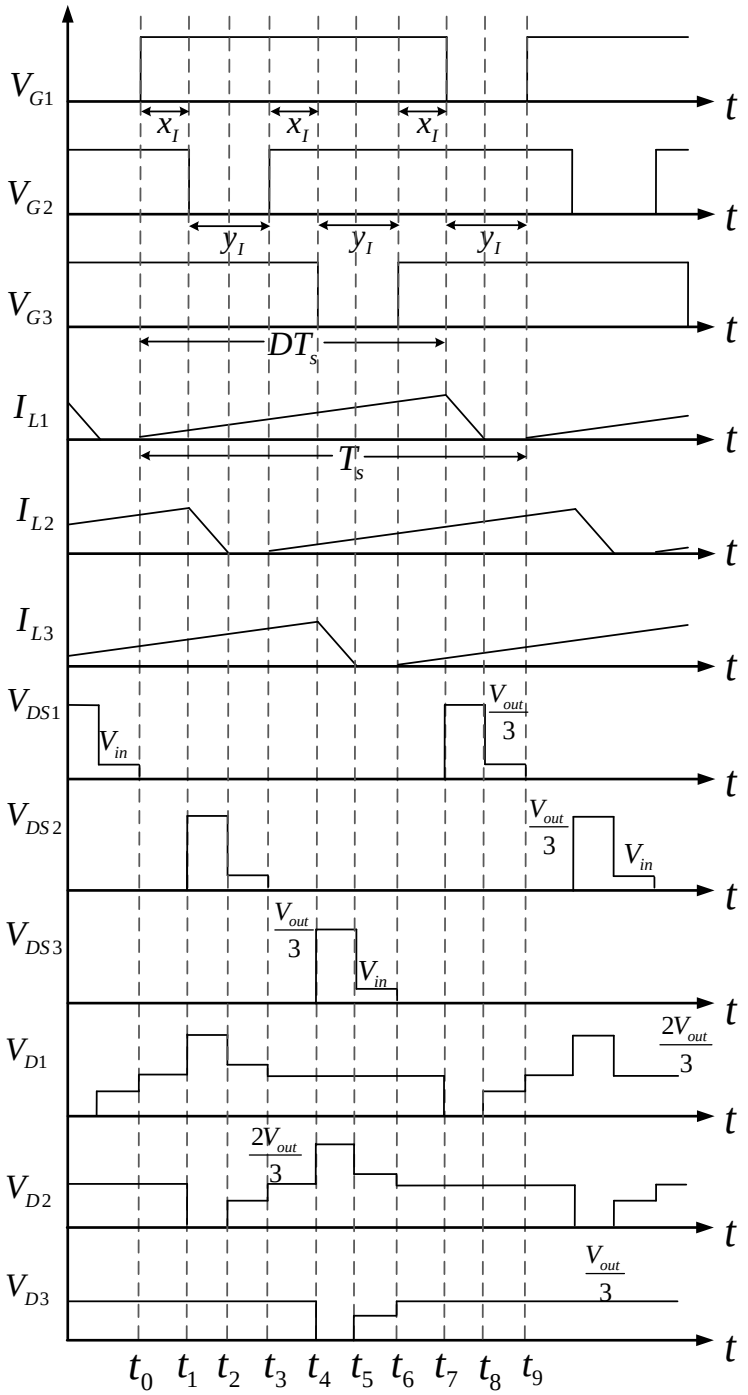


Figure 3.2: Gate Signal, Inductor current, and Device Voltages for DCM Operation in Zone I for 3-Phase EDR Boost.

phases with similar slope, peak, and average values.

3.2.2 Zone II Operation

For Zone II, the duty ratio range is given as $1/3 \leq D < 2/3$. It is interesting to note that for Zone II operation in DCM, the waveforms are similar to that of Zone I with $x_{II} = (D - 1/3)T_s$ and $y_{II} = (2/3 - D)T_s$, and thus are not repeated. This is different than the CCM operation, where Zone II has different combination of operating modes, higher device voltage stress, and unequal phase inductor current than that of Zone I.

Zone III operation is more involved and is discussed in the next section.

3.3 Zone III Operation

Zone III corresponds to the duty ratio range $0 \leq D < 1/3$. In this zone, individual inductor current has negative current excursion even for non-synchronous circuit implementation. This is because of the coupling between the interleaved phases with the switched capacitors. The negative current path can be appreciated by noting the conducting devices during each of the operating interval as discussed below. The presence of the negative phase current leads to circulating current in the converter accounting to additional conduction loss. It is to be noted that depending on the converter duty ratio and k, Zone III can further have different operating cases as analyzed below.

3.3.1 Case I

For DCM operation, Figure 3.3 shows the typical gate signal, corresponding inductor current, and switch voltage stress of both the diode (denoted by V_D) and MOSFETs (denoted by V_{DS}) for Case I operation in Zone III, where $x_{III} = DT_s$

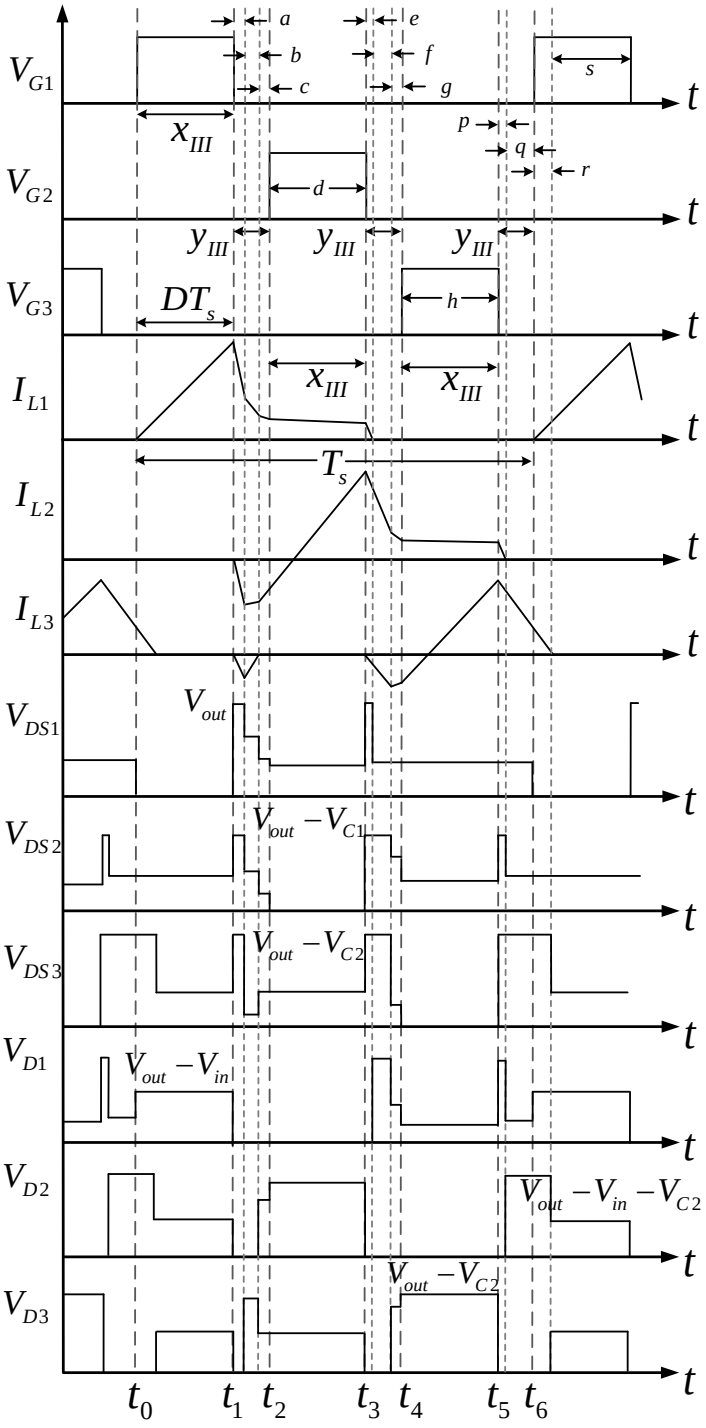


Figure 3.3: Gate Signal, Inductor Current, and Device Voltages for DCM Operation in Zone III, Case I for 3-Phase EDR Boost.

and $y_{III} = (1/3 - D)T_s$. The maximum voltage stress for all the devices is shown. Different operating intervals are marked in Figure 3.3, based on which Table 3.5 gives the conducting devices, inductor voltages, and capacitor currents. For each of the interval, the inductor voltages are obtained by applying KVL. However, additionally the conditions $v_{L1} + v_{L2} + v_{L3}$ and $v_{L1} + v_{L2}$ are respectively applied for interval b and c to derive the corresponding voltages. Capacitor currents are obtained by applying KCL. The final column in Table 3.5 describes the condition of transition from one interval to its subsequent one. For Case I, none of the diode of the main MOSFETs conduct.

Denoting i_{L1a} as the inductor current of boost phase I at the end of the interval a, and by noting its slope from Table 3.5 at that interval, i_{L1a} can be obtained as

$$i_{L1a} = \frac{v_{in}}{L} DT_s + \frac{v_{in} - v_o}{L} aT_s \tag{3.2}$$

Similarly, each of the phase currents can be obtained at the end of each operating interval (representation similar to i_{L1a} is followed for all others). Subsequently the mathematical expression of these intervals can be obtained by applying the condition which marks the end of the interval (given in the final column of Table 3.5). For example, interval a ends when condition $i_{L1a} + i_{L2a} + i_{L3a} = 0$ is satisfied, which is used to derive the expression for a as

$$a = \frac{v_{in} D}{3v_o - 3v_{in} - v_{c1} - v_{c2}} \tag{3.3}$$

The expression for all other intervals can be similarly obtained and are given in Table 3.1.

Table 3.1: Computing Operating Interval for Case I Operation in Zone III

Condition applied	**Expression of interval**
$i_{L1a} + i_{L2a} + i_{L3a} = 0$	$a = \dfrac{v_{in}D}{3v_o - 3v_{in} - v_{c1} - v_{c2}}$
$i_{L3b} = 0$	$b = \dfrac{(v_o - v_{in} - v_{c2})3a}{2v_{c2} - v_{c1}}$
$a + b + c = \dfrac{1}{3}(1 - 3D)$	$c = \dfrac{1}{3} - D - a - b$
$d = D$	$d = D$
$i_{L1e} = 0$	$e = \dfrac{i_{L1d}}{v_o - v_{in}}\dfrac{L}{T_s}$
$i_{L2f} + i_{L3f} = 0$	$f = \dfrac{i_{L2e} + i_{L3e}}{2v_o - 2v_{in} - v_{c1} - v_{c2}}\dfrac{L}{T_s}$
$g + e + f = \frac{1}{3}(1 - 3D)$	$g = \frac{1}{3} - D - e - f$
$h = D$	$h = D$
$i_{L2p} = 0$	$p = \dfrac{i_{L2h}}{v_o - v_{in} - v_{c1}}\dfrac{L}{T_s}$
$p + q = \frac{1}{3}(1 - 3D)$	$q = \frac{1}{3} - D - p$
$i_{L3r} = 0$	$p = \dfrac{i_{L3q}}{v_o - v_{in} - v_{c2}}\dfrac{L}{T_s}$
$r + s = D$	$s = D - r$

3.3.2 Case II

In this case, the diode of Q_3 conducts, i.e., negative current flows through it for certain intervals $(b + c)$ as shown in Figure 3.3 which shows the typical gate

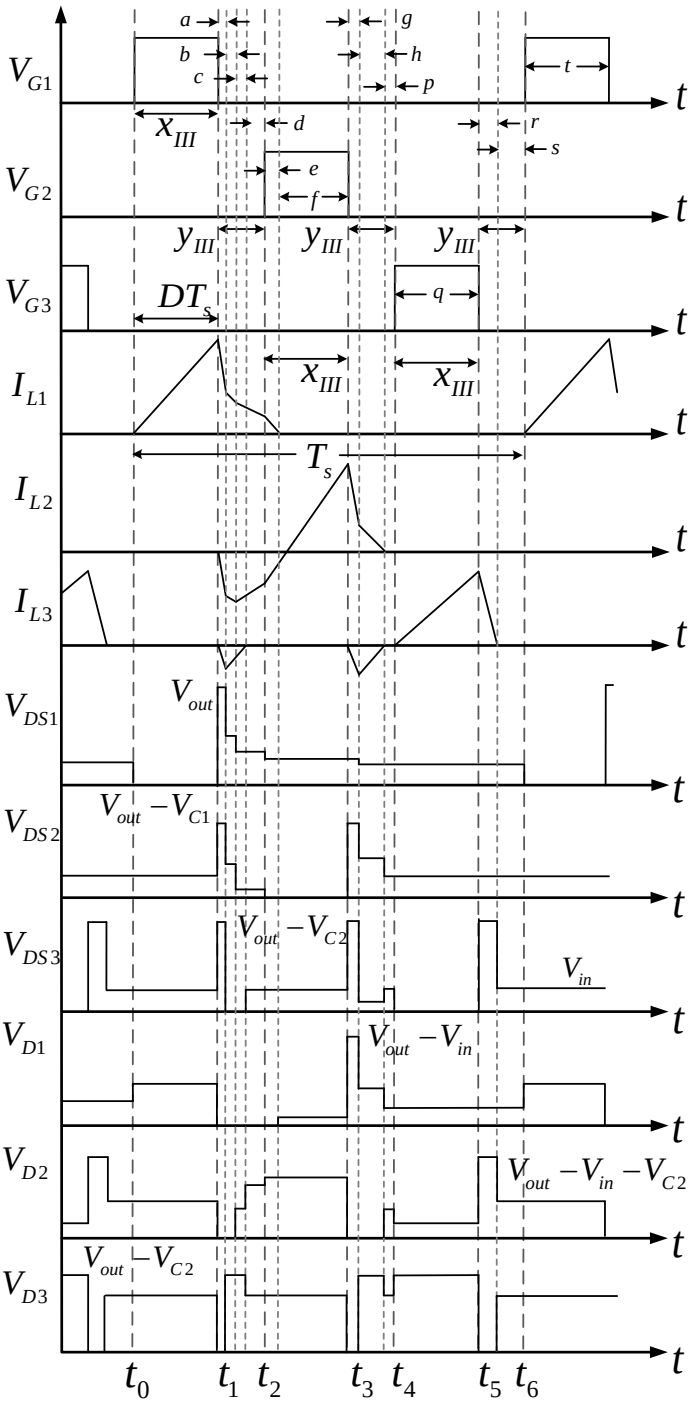


Figure 3.4: Gate Signal, Inductor Current, and Device Voltages for DCM Operation in Zone III, Case II for 3-Phase EDR Boost.

signal, corresponding inductor current, and switch voltage stress of both the diode (denoted by V_D) and MOSFETs (denoted by V_{DS}) for Case II operation in Zone III. The negative conduction happens if the condition $3v_{in} < 2v_{c2} - v_{c1}$ is satisfied. The intervals x_{III} and y_{III} is similar to that of the previous case. The maximum switch voltage stress is also marked in the Figure, the voltage stress for all the intervals can be found by referring to Table 3.7. Different operating intervals are marked in Figure 3.3, based on which Table 3.7 gives the conducting devices, inductor voltages, and capacitor currents. Similar to Case I, the final column in the table describes the condition of transition from one interval to its next.

Following the same procedure as above, the expression for each of the operating interval is derived as given in Table 3.2.

3.3.3 Case III

Case III is characterized by the negative conduction of both Q_2 and Q_3. The operating intervals can be similarly derived as Cases I and II and are not shown here to avoid lengthy repetition.

Also it is to be noted that apart from the presented waveforms in Figures 3.3 and 3.4, there can exists variation in the combination of operating intervals. However, these additional cases have very similar operating characteristics as the basic ones discussed here with limited differences in the operating intervals. In fact, the new ones would constitute a sub-set of these three operating cases. For example, a variant of Case II has no p interval, though it retains the basic operating principles of Case II.

Table 3.2: Computing Operating Interval for Case II Operation in Zone III

Condition applied	**Expression of interval**
$i_{L1a} + i_{L2a} + i_{L3a} = 0$	$a = \dfrac{v_{in}D}{3v_o - 3v_{in} - v_{c1} - v_{c2}}$
$i_{L1b} + i_{L2b} = 0$	$b = \dfrac{i_{L1a} + i_{L2a}}{2v_{c2} - 2v_{in} + v_{c1}} \dfrac{L}{T_s}$
$i_{L3c} = 0$	$c = \dfrac{i_{L3c}}{v_{in}} \dfrac{L}{T_s}$
$a + b + c + d = \dfrac{1}{3}(1 - 3D)$	$d = \dfrac{1}{3} - D - a - b - c$
$i_{L1e} = 0$	$e = \dfrac{i_{L1d}}{v_{c1} - v_{in}} \dfrac{L}{T_s}$
$e + f = D$	$f = D - e$
$i_{L2g} + i_{L3g} = 0$	$g = \dfrac{i_{L2f}}{2v_o - 2v_{in} - v_{c1} - v_{c2}} \dfrac{L}{T_s}$
$i_{L2h} = 0$	$h = \dfrac{2i_{L2g}}{v_{c1} - v_{c2}} \dfrac{L}{T_s}$
$g + h + p = \frac{1}{3}(1 - 3D)$	$p = \frac{1}{3} - D - g - h$
$q = D$	$q = D$
$i_{L3r} = 0$	$r = \dfrac{i_{L3q}}{v_o - v_{in} - v_{c2}} \dfrac{L}{T_s}$
$r + s = \dfrac{1}{3}(1 - 3D)$	$s = \dfrac{1}{3} - D - r$
$t = D$	$t = D$

Table 3.3: Converter Specification

Parameter	Rating
Input	20-50 V
Output	220 V, 100 W
Switching frequency	150/200 kHz

Table 3.4: Component Details

Component	Parameters
C_1 , C_2 , C_3	4.7 μF/ 100 V, 4.7 μF/ 200 V, 4.7 μF/ 300 V
L_1 , L_2 , L_3	6.5 μH
Q_{s1} , Q_{s2} , Q_{s3}	GS66508P
D_1 , D_2 , D_3	C3D04060E (2), SBR10U200

3.4 Simulation and Experimental Results

3.4.1 Hardware Prototype

A 100 W GaN based hardware prototype for 3-phase EDR boost as shown in Fig. 3.5 has been built to study the DCM operation. Table 3.3 and Table 3.4 give the

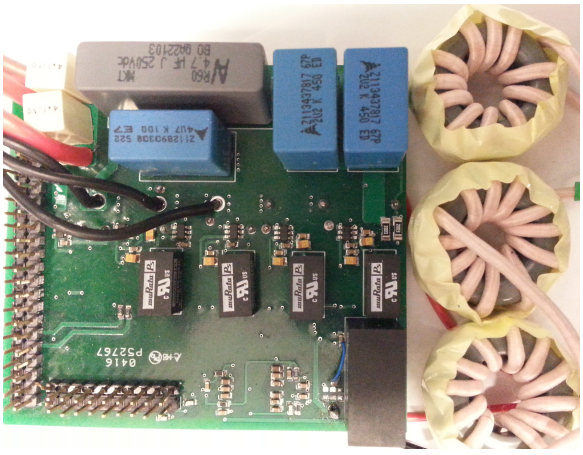
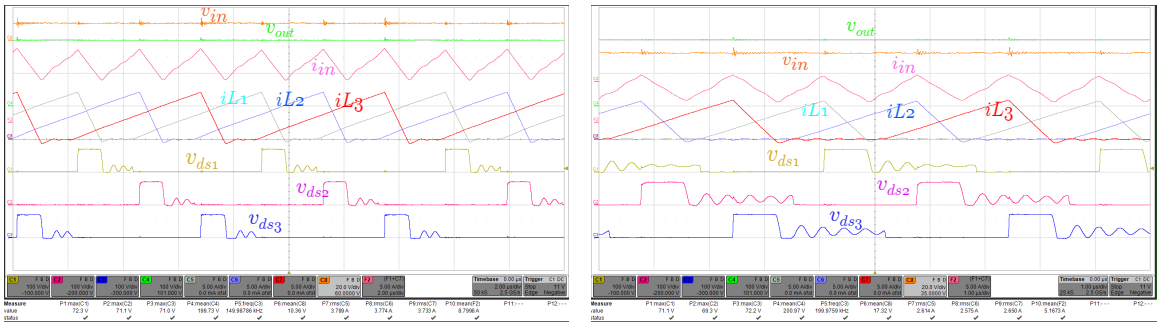


Figure 3.5: Experimental Prototype for 3-Phase EDR Boost.



(a) (b)

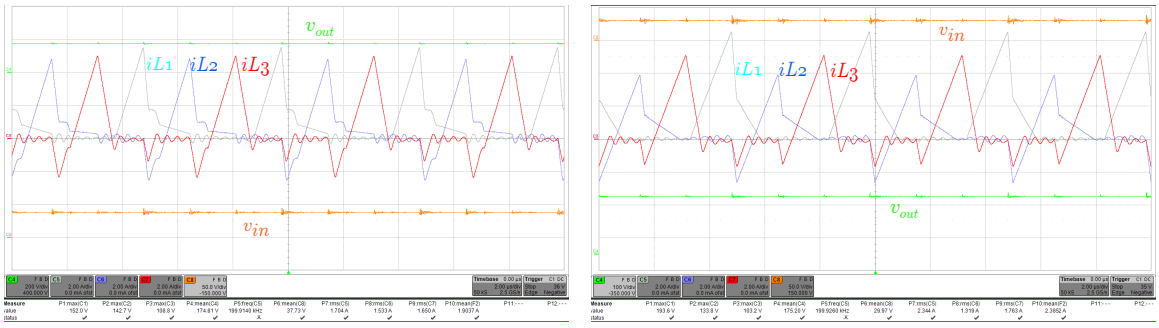
Figure 3.6: Waveforms for DCM operation (current: 5 A/div, v_{in} : 20 V/div, othe voltages : 100 V/div, time : 2 μs/div) of 3-phase EDR boost for (a) Zone I with $D_1 = D_2 = D_3 = 0.7$ operating from 10 V to 200 V at 150 kHz switching frequency (time : 2 μs/div), (b) Zone II with $D_1 = D_2 = D_3 = 0.45$ operating from 17 V to 200 V at 200 kHz switching frequency (time : 1 μs/div).

converter specifications and the passive and active component details for the hardware set-up respectively. A 500 Ω load resistor is used for the experiment. The inductors are designed with toroid MPP core CO-55351-A2 from Magnetics. Litz wire is used to limit the high frequency conduction loss. The value of the dimensionless parameter k for this case is 3.9×10^{-3} and 5.2×10^{-3} for 150 kHz and 200 kHz respectively.

EZDSP TMSF28335 has been used to generate the 200 kHz interleaved PWM gate signals. LeCroy 6200A oscilloscope is used to capture the relevant waveforms and power analyzer YOKOGAWA WT3000 is used to measure the efficiency.

3.4.2 Experimental Results

Figs. 3.6a and 3.6b respectively show the experimental waveforms for Zones I and II operation under DCM. The interleaved phase currents, device voltages, input current and voltage, and output voltages are shown for each zone. It can be seen that for both the zones, the inductor currents are equivalent in all three phases with similar slope as discussed earlier. Further, the voltage stress for all the three devices can be observed to be $v_o/3$. An experimental efficiency of 90.92% and 93.98% are



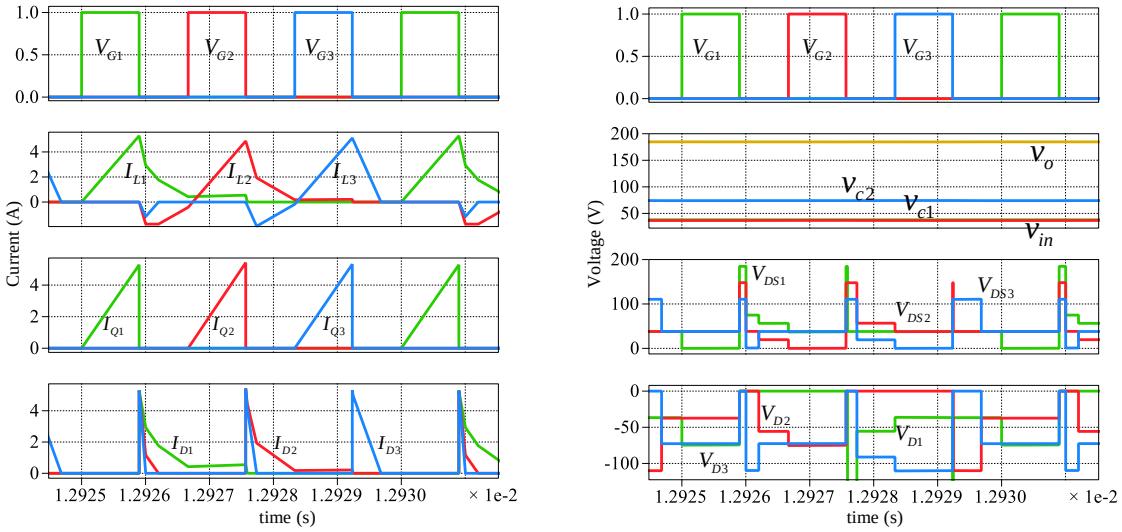
(a) (b)

Figure 3.7: Waveforms for Zone III DCM operation at 200 kHz switching frequency (current: 2 A/div, v_{in} : 50 V/div, time : 2 μs/div) in 3-phase EDR boost for (a) Case I with $D_1 = D_2 = D_3 = 0.18$ operating from 37 V to 175 V (v_o : 200 V/div) , (b) Case II with $D_1 = D_2 = D_3 = 0.3$ operating from 29 V to 175 V (v_o : 100 V/div).

observed in operating Zones I and II respectively.

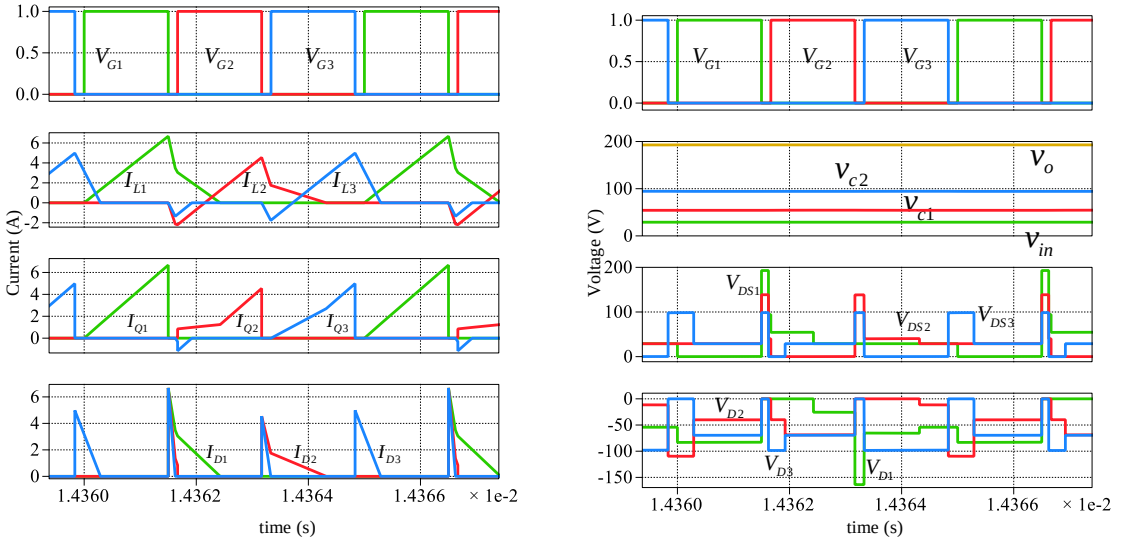
Figs. 3.7a and 3.7b respectively show the waveforms from hardware prototype for Cases I and II operation in Zone III under DCM for 175 V output. The interleaved phase currents, and input and output voltages are shown for each case. An efficiency of 91.07% and 89.97% are observed in experiment for Cases I and II operation respectively.

High-frequency ringing is present in the experimental waveforms due to circuit non-idealities. Thus simulation results are provided for further validation of the converter operation. Figs. 3.8 and 3.9 present the corresponding simulation results for Cases I and II operation respectively showing all the relevant waveforms of the converter. It can be verified that $3v_{in} < 2v_{c2} - v_{c1}$ is satisfied for Case II operation where Q_{D3} conducts. Also it can be seen that the presented simulation and experimental results are in good agreement with the analysis presented in the previous sections.



(a) (b)

Figure 3.8: PLECS simulation waveforms for Case I of Zone III 3-phase EDR boost corresponding to $D_1 = D_2 = D_3 = 0.18$ operating from 37 V showing all the relevant waveforms.



(a) (b)

Figure 3.9: PLECS simulation waveforms for Case II Zone III 3-phase EDR boost corresponding to $D_1 = D_2 = D_3 = 0.3$ operating from 29 V showing all the relevant waveforms.

3.5 Conclusion

In this chapter, EDR boost has been studied for high step-up light load application in DCM operation. Comprehensive analysis of converter DCM operating principles, key theoretical waveforms, and steady state circuit performance corresponding to all the possible zones of operation have been presented. It is shown that inherent current sharing in three boost phases is possible in Zones I and II operation unlike for only Zone I in CCM operation. For Zone III, multiple operating cases exist with different combination of operating modes. Finally, the DCM operation analysis is validated in a 100 W GaN based hardware prototype for different operating regions.

Table 3.5: Zone III $(2/3 \leq D \leq 1)$ Case I

Interval	Conducting device(s)	v_{L1}	v_{L2}	v_{L3}	i_{c1}	i_{c2}	i_{c3}	Comment
a	D_1, D_2, D_3	$v_{in} - v_o$	$v_{in} - v_o + v_{c1}$	$v_{in} - v_o + v_{c2}$	$-i_{L2}$	$-i_{L3}$	$i_{L1} + i_{L2} + i_{L3} - i_o$	ends when $i_{L1} = -i_{L2} - i_{L3}$
b	D_1, D_2	$\frac{-v_{c1} - v_{c2}}{3}$	$\frac{2v_{c1} - v_{c2}}{3}$	$\frac{2v_{c2} - v_{c1}}{3}$	$-i_{L2}$	$-i_{L3}$	$-i_o$	ends when $i_{L1} = -i_{L2}$ and $i_{L3} = 0$
c	D_1	$-v_{c1}/2$	$v_{c1}/2$	0	i_{L1}	0	$-i_o$	ends when Q_2 starts conducting
d	D_1, Q_2	$v_{in} - vc1$	v_{in}	0	i_{L1}	0	$-i_o$	ends when Q_2 stops conducting
e	D_1, D_2, D_3	$v_{in} - v_o$	$v_{in} - v_o + v_{c1}$	$v_{in} - v_o + v_{c2}$	$-i_{L2}$	$-i_{L3}$	$i_{L1} + i_{L2} + i_{L3} - i_o$	ends when $i_{L1} = 0$

Continued to next page

Table 3.6: Zone III $(2/3 \leq D \leq 1)$ Case I (Contd..)

Interval	Conducting device(s)	v_{L1}	v_{L2}	v_{L3}	i_{c1}	i_{c2}	i_{c3}	Comment
f	D_2, D_3	0	$v_{in} - v_o + v_{c1}$	$v_{in} - v_o + v_{c2}$	$-i_{L2}$	$-i_{L3}$	$i_{L2} + i_{L3} - i_o$	ends when $i_{L2} = i_{L3}$
g	D_2	0	$\frac{v_{c1} - v_{c2}}{2}$	$\frac{-v_{c1} + v_{c2}}{2}$	$-i_{L2}$	$-i_{L3}$	$-i_o$	ends when Q_3 starts conducting
h	D_2, Q_3	0	$v_{in} + v_{c1} - v_{c2}$	v_{in}	$-i_{L2}$	i_{L2}	$-i_o$	ends when Q_3 stops conducting
p	D_2, D_3	0	$v_{in} - v_o + v_{c1}$	$v_{in} - v_o + v_{c2}$	$-i_{L2}$	$-i_{L3}$	$i_{L2} + i_{L3} - i_o$	ends when $i_{L2} = 0$
q	D_3	0	0	$v_{in} - v_o + v_{c2}$	0	$-i_{L3}$	$i_{L3} - i_o$	ends when Q_1 starts conducting
r	Q_1, D_3	v_{in}	0	$v_{in} - v_o + v_{c2}$	0	$-i_{L3}$	$i_{L3} - i_o$	ends when $i_{L3} = 0$
s	Q_1	v_{in}	0	0	0	0	$-i_o$	ends when Q_1 stops conducting

Table 3.7: Zone III $(2/3 \leq D \leq 1)$ Case II

Interval	Conducting device(s)	v_{L1}	v_{L2}	v_{L3}	i_{c1}	i_{c2}	i_{c3}	Comment
a	D_1, D_2, D_3	$v_{in} - v_o$	$v_{in} - v_o + v_{c1}$	$v_{in} - v_o + v_{c2}$	$-i_{L2}$	$-i_{L3}$	$i_{L1}+i_{L2}+$ $i_{L3} - i_o$	ends when $i_{L1} = -i_{L2} - i_{L3}$
b	D_1, D_2, Q_{D3}	$v_{in} - v_{c2}$	$v_{in} + v_{c1} - v_{c2}$	v_{in}	$-i_{L2}$	$-i_{L3} + i_{QD3}$	$-i_o$	ends when $i_{L1} = -i_{L2}$
c	D_1, Q_{D3}	$-v_{c1}/2$	$v_{c1}/2$	v_{in}	$-i_{L2}$	0	$-i_o$	ends when $i_{L3} = 0$
d	D_1	$-v_{c1}/2$	$v_{c1}/2$	0	$-i_{L2}$	0	$-i_o$	ends when Q_2 starts conducting
e	D_1, Q_2	$v_{in} - vc1$	v_{in}	0	i_{L1}	0	$-i_o$	ends when D_1 stops conducting and $i_{L1} = 0$
f	Q_2	0	v_{in}	0	0	0	$-i_o$	ends when Q_2 stops conducting

Continued to next page

Table 3.8: Zone III $(2/3 \leq D \leq 1)$ Case II (Contd..)

Interval	Conducting device(s)	v_{L1}	v_{L2}	v_{L3}	i_{c1}	i_{c2}	i_{c3}	Comment
g	D_2, D_3	0	$v_{in} - v_o + v_{c1}$	$v_{in} - v_o + v_{c2}$	$-i_{L2}$	$-i_{L3}$	$i_{L2} + i_{L3} - i_o$	ends when $i_{L2} = -i_{L3}$
h	D_2	0	$\frac{v_{c1} - v_{c2}}{2}$	$\frac{-v_{c1} + v_{c2}}{2}$	$-i_{L2}$	$-i_{L3}$	$-i_o$	ends when $i_{L2} = i_{L3} = 0$
p	–	0	0	0	0	0	$-i_o$	ends when Q_3 starts conducting
q	Q_3	0	0	v_{in}	0	0	$-i_o$	ends when Q_3 stops conducting
r	D_3	0	0	$v_{in} - v_o + v_{c2}$	0	$-i_{L3}$	$i_{L3} - i_o$	ends when D_3 stops conducting i.e., $i_{L3} = 0$
s	–	0	0	0	0	0	$-i_o$	ends when Q_1 starts conducting
t	Q_1	v_{in}	0	0	0	0	$-i_o$	ends when Q_1 stops conducting

Chapter 4

HALF BRIDGE VOLTAGE SWING INVERTER

4.1 Introduction

As discussed in Section 1.2.2, the input power from the PV array being purely DC and the output being a sinusoidally varying power superimposed on a DC average, the instantaneous power from input is clearly not equal to that of the output. Also the problem of capacitive ground current has been introduced in Section 1.2.1. Here, a power decoupling scheme for single phase inverters has been proposed which addresses both the challenges of transformer-less application as discussed above [81]. The proposed converter termed as half-bridge voltage swing (HBVS) inverter topology is a combination of the boost and half-bridge stages along with a power decoupling stage. A large sinusoidal swing of the half-bridge capacitors are allowed along with a double line frequency DC-link voltage ripple to address the power decoupling with a reduced capacitor value of only 54 μF/ kW at 550 V peak, and only uses film capacitors for this purpose. Unlike many other active decoupling solutions, the proposed approach does not significantly increase the DC-link voltage and therefore the switch voltage stress. Also being a half-bridge implementation, the voltage ripple seen by the stray ground capacitor is only at grid frequency of 60 Hz, yielding very low capacitive leakage current and EMI. The string inverter is implemented with SiC devices, with a 100 kHz switching frequency.

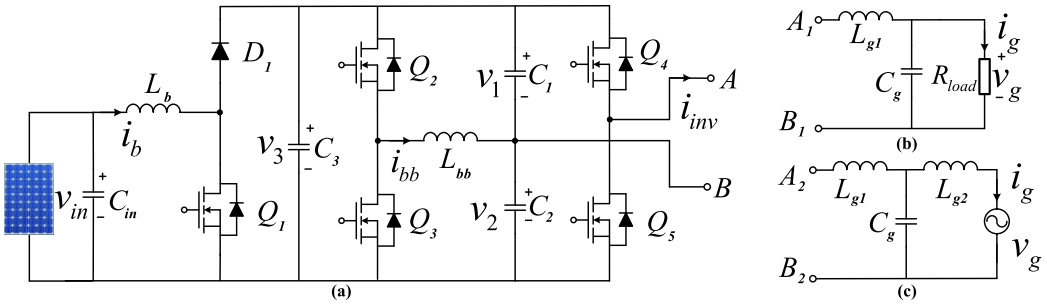


Figure 4.1: Proposed Half Bridge Voltage Swing (HBVS) Inverter for Transformer-less PV Application.

4.2 Circuit Configuration

Figure 4.1 shows the topology of the half bridge voltage swing (HBVS) inverter for transformer-less PV application. The converter has an input boost stage followed by a buck-boost power decoupling and half-bridge inverter stages. The buck-boost stage comprises of two switches Q_2 and Q_3 and an inductor L_{bb} and controls the voltage of the half-bridge capacitors, C_1 and C_2 such as to provide a part of 120 Hz power decoupling. Whereas, the unidirectional boost stage consisting of a diode D_1, a switch Q_1, and input inductor L_b boosts the PV input voltage v_{in} to a higher dc-link voltage v_3 with a 120 Hz ripple which supports the rest of the grid ripple power. Additionally this stage adds to the flexibility of accepting a wide input voltage range, as required by the PV inverters to address the partial shading conditions.

The half-bridge inverter comprises of two switches Q_4 and Q_5. In stand-alone (Figure 4.1b) and grid connected (Figure 4.1c) modes, node $A\{B\}$ is shorted with $A_1\{B_1\}$ and $A_2\{B_2\}$, respectively. For grid connected implementation LCL (L_{g1}, C_g, L_{g2}) and for stand-alone operation LC (L_{g1}, C_g) filters are considered. The grid neutral is connected to the middle point of half-bridge capacitor, which ensures that the PV panel stray capacitance encounter only fundamental frequency current, and thus address the ground current issue. Though this is true for any half-bridge based inverter, but for the double line frequency decoupling power they necessitate very large

capacitors in the range of mF. In the proposed converter through active power decoupling scheme, the capacitance requirement is greatly minimized, a detailed discussion is given in the next section.

4.2.1 Power Decoupling

The power decoupling is predominantly taken care of by the buck-boost stage through the control of the half-bridge capacitors. The grid neutral is connected to the middle point of half-bridge capacitor, which ensures that the PV panel stray capacitance encounter only line frequency current, and thus address the ground current issue. This is true for any half-bridge based inverter, but for power decoupling they necessitate large capacitor in the range of mF. In the proposed converter through active power decoupling scheme, the capacitance requirement is greatly minimized.

Considering no capacitor is present on the DC-link i.e., $C_3 = 0$ and the DC-link voltage v_3 is held constant, i.e., with zero 120 Hz voltage ripple on the DC-link, the voltage across the two capacitors v_1 and v_2 are given by (4.1) and (4.2) respectively.

$$v_1 = \frac{v_3}{2} + A\sin(\omega t + \phi) \tag{4.1}$$

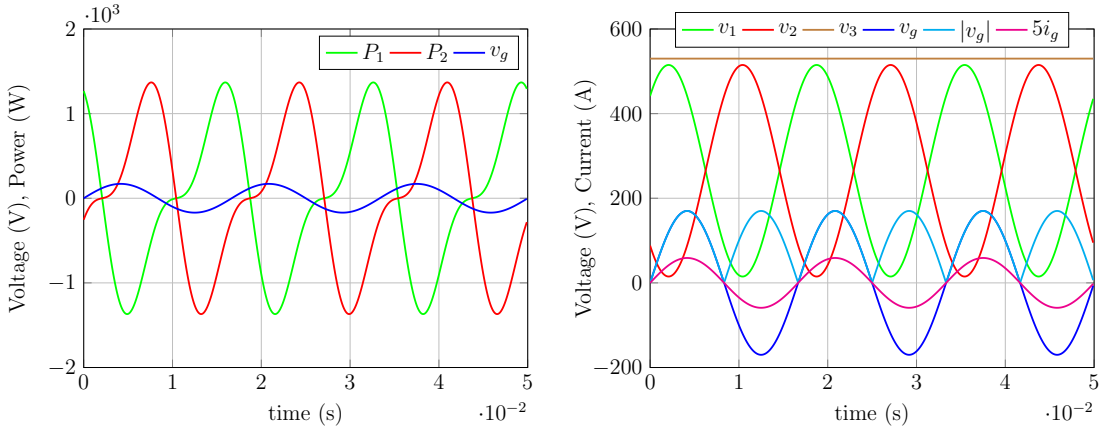
Table 4.1: Converter Specification

Parameter	**Rating**
DC Input	100-450 V
Output	120 V, 60 Hz, stand-alone
Operating power factor (pf)	0.7 lagging - 0.7 leading
Switching frequency, f_{sw}	100 kHz

$$v_2 = \frac{v_3}{2} - A\sin(\omega t + \phi) \tag{4.2}$$

Ideally, v_1 and v_2 can swing from 0 to v_3, i.e., $A = v_3/2$. In such scenario, the capacitance can be reduced to a minimum vale and the power decoupling principle in this converter can be analyzed as follows. In a quarter cycle when C_1 gets charged from 0 to $v_3/2$ and C_2 is discharged from v_3 to $v_3/2$ keeping the sum of them to be constant to v_3, the increment of power for C_1 is less than that discharged by C_2 and thus the balanced power is fed to the grid. In the next quarter, C_1 gets charged from $v_3/2$ to v_3 and C_2 is discharged from $v_3/2$ to 0 again maintaining the sum of the capacitor voltages to be constant to v_3, the increment of power for C_1 is more than that discharged by C_2 and the thus C_1 sinks the balanced power between the input and the grid. Exactly opposite happens in the other two quarter cycles.

Figure 4.2a shows the variation of the pulsating power P_1 and P_2 supported by these capacitors, and the total ripple power addressed by the two capacitors corresponding to the specification given in Table 4.1 and at unity power factor (UPF).



(a) Capacitor ripple power and grid voltage

(b) Different voltage variables and scaled grid current

Figure 4.2: Analytic Plots for Operating Condition Corresponding to V_g = 120 V, P = 1 kW, v_3 = 530, A 250, C = 43 μF.

The pulsating power for each capacitor is given in (4.3).

$$P_1 = \frac{1}{2}\frac{d}{dt}\left(C_1 v_1^2\right); \qquad P_2 = \frac{1}{2}\frac{d}{dt}\left(C_2 v_2^2\right) \tag{4.3}$$

Further (4.4) is obtained by substituting for v_1 and v_2 from (4.1) and (4.2) respectively and by considering $C_1 = C_2 = C$ for symmetry.

$$P_1 + P_2 = \omega C A^2 \sin(2\omega t + 2\phi) \tag{4.4}$$

Figure 4.2b gives the analytic waveforms of three capacitor voltages, grid voltage, and scaled grid current at $A = 0.94(v_3/2)$ corresponding to the specification given in Table 5.1 and UPF. Though ideally, v_1 and v_2 can swing from 0 to v_3 and $A = v_3/2$, but it cannot be realized because of the additional constraint imposed on the instantaneous values of v_1 and v_2 at any operating power factor. The constraint expression is given in (4.5). This ensures that the inverter stage does not operate at modulation index more than 1, which would otherwise distort the output waveforms and impact their total harmonic distortion (THD) performance.

$$\begin{cases} v_1 > v_g & \text{if } v_g \geq 0 \\ v_2 > |v_g| & \text{if } v_g < 0 \end{cases} \tag{4.5}$$

This is quite different from any HB inverter with $v_1 = v_2$ and conventional decoupling scheme which uses a very large dc-link capacitor, generally electrolytic, with a small double line frequency voltage ripple, V_r on the dc-link. Thus no additional constraint is imposed on the instantaneous HB voltages w.r.t. the grid voltage, where it is enough to satisfy $2v_1 > V_g$ globally.

Finally by comparing the magnitude and phase of $2\omega t$ terms in P_g and $P_1 + P_2$ from (1.2) and (4.4), the condition for double line frequency power decoupling as

given in (4.6) are obtained, where S_g is the inverter VA. Thus the capacitor values and its voltage phase are determined independently.

$$C = \frac{V_g I_g}{2\omega A^2} = \frac{S_g}{\omega A^2}; \qquad \phi = \frac{\pi}{4} + \frac{\theta}{2} \tag{4.6}$$

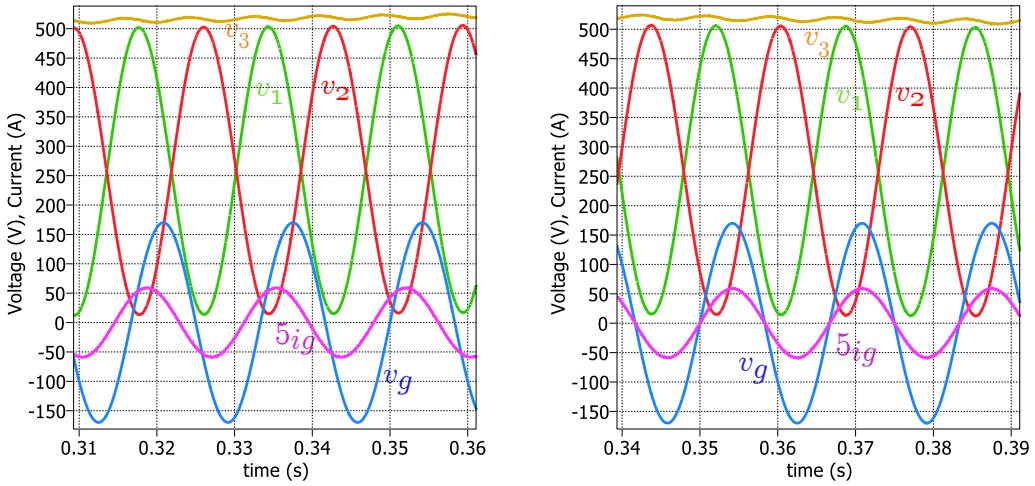
(4.6) shows that the capacitor value is dependent only on the voltage swing across the capacitor and unlike the full bridge inverter or most of other power decoupling approaches, it is independent of the DC-link voltage.

4.3 Capacitance Optimization and Operation

Until now the DC-link capacitor is considered to be zero with no voltage ripple at the DC link i.e., $C_3 = 0$ and $v_3 = 0$. But it has been observed that the total capacitor values required for power decoupling can be further reduced by allowing a limited double line frequency voltage ripple at the DC-link with a non-zero DC link capacitor. This section studies an optimization problem to arrive at the best capacitance value with a constraint on the switch voltage stress and instantaneous values of v_1 and v_2 with respect to v_g.

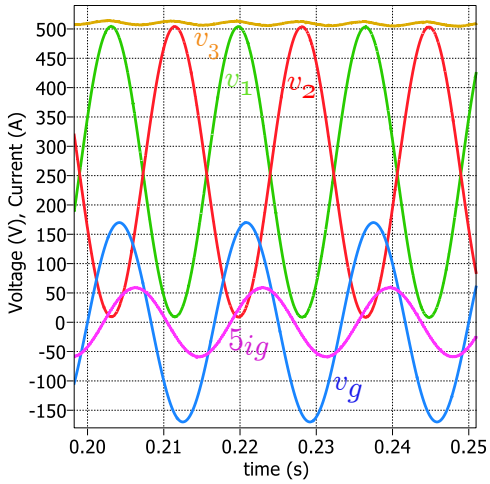
4.3.1 Case Studies

Figure 4.3 gives the simulation waveforms of capacitor voltages, DC-link voltage, grid voltage, and scaled grid current for 1 kW converter corresponding to the specification given in Table 5.1 and at three different power factor with 530 V as the allowable switch voltage stress corresponding to a 600 V (with the safety margin for converter transient). Figures 4.3a, 4.3b, and 4.3c respectively present waveforms at 0.7 leading pf, UPF, and 0.7 lagging pf with a total of 86 μF capacitor (C_1 + C_2). It can be seen that the condition given in (4.5) has been satisfied in all three cases. Further, the worst operating condition occurs at leading power factor when the v_g



(a) pf = 0.7 leading

(b) pf = 1



(c) pf = 0.7 lagging

Figure 4.3: Waveforms from PLECS for Operating Condition Corresponding to V_g = 120 V, P = 1 kW, v_3 = 530, A 250, C = 43 μF.

waveform barely touches v_1 and v_2 waveforms at the critical point, with the difference in voltage being very minimal. Thus to design the values of the passive components, especially the decoupling capacitor, the range of power factor the inverter needs to operate should be carefully noted as the voltage difference at the critical point varies along the power factor. And even if condition (4.6) is satisfied with the chosen capacitor, (4.5) can impose more stringent requirement at leading power factor requiring a

higher capacitor value than given by the former.

However, the total capacitance requirement can be reduced if instead of having a constant DC-link voltage, a limited double line frequency ripple is allowed in the DC-link. The DC-link voltage would now be pulsating as given in (4.7). This introduces two new variables in the converter parameter, one is the DC-link ripple V_r and the other is the DC-link capacitor C_3.

$$v_3 = V + V_r \sin(2\omega t + \theta) \tag{4.7}$$

The ripple power addressed by C_3 is given in (4.8) which can be further written as (4.9) by combing the expression of v_3 from (4.7).

$$P_3 = \frac{1}{2}\frac{d}{dt}\left(C_3 v_3^2\right) \tag{4.8}$$

$$P_3 = \omega C_3 V V_r \cos(2\omega t + \theta) + \omega C_3 V_r^2 \sin(4\omega t + 2\theta) \tag{4.9}$$

With the ripple on DC-link, the expression for P_1 and P_2 and thus $P_1 + P_2$ are also modified as shown in (4.10).

$$\begin{aligned} P_1 + P_2 = {} & \omega C(A^2 + V V_r)\cos(2\omega t + \theta) \\ & + \frac{1}{2}\omega C V_r^2 \sin(4\omega t + 2\theta) \end{aligned} \tag{4.10}$$

And the total ripple power supported by all three capacitors is given in (4.11).

$$P_t = P_1 + P_2 + P_3 \tag{4.11}$$

Finally by comparing the magnitude and phase of $2\omega t$ terms in P_g and P_t from (1.2) and (4.11), the condition for double line frequency power decoupling as given in (4.12) is obtained.

$$VV_r(2C_3 + C) + CA^2 = \frac{V_g I_g}{2\omega} = \frac{S_g}{\omega} \tag{4.12}$$

4.3.2 Optimization Problem

Unlike previous case, where the half-bridge capacitance C can be uniquely determined from (4.6), it is interesting to note that now there could be multiple combinations of $V,\ V_r,\ C,\ C_3$, and A values satisfying the condition (4.12) and no particular solution exist for this. But each of this solution is not necessarily a good choice as all of these combinations not necessarily ensure satisfaction of (4.5) and minimized voltage stress on the switches. So the analysis has been modified to a multi-objective optimization problem instead of a straightforward equation based problem with the objective of minimizing the total capacitance value while limiting the voltage stress on the switches i.e., the DC-link voltage peak and satisfying condition (4.5). The objectives and constraints of the optimization problem are formulated as discussed below.

Objectives

- Maximize dc voltage utilization factor of the decoupling capacitors.
- Minimize the average voltage on the dc-link which directly translates to the average switching loss over a grid cycle.
- Minimize the decoupling capacitor requirement so as to improve on converter power density and reduce cost.
- Maximize the voltage swing of capacitors C_1 and C_2, i.e., to maximize A so as to provide maximum power decoupling with the designed capacitance value.

Constraints

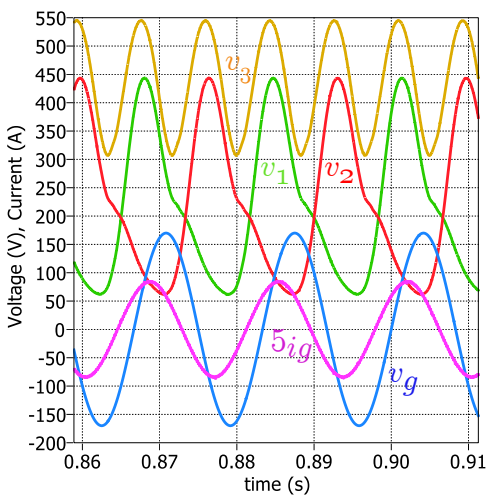
- Satisfy the active power decoupling equality constrain in (4.5).
- Limit the voltage stress V_{switch} on switches depending on the switch voltage rating. The voltage stress is the peak of the dc-link voltage.
- Satisfy the no-over-modulation criteria in (4.5).

The optimization problem formulates as follows in (4.13) where w_i is the weighing function for each objective. It is solved using MATLAB optimization solver for the converter specifications given in Table 4.1. The total capacitance required has been optimized to only 54 μF/ kW with 500 V maximum switch stress to support 1 kW at 0.7 lagging - 0.7 leading pf range. Table 4.2 gives the detail of the decoupling capacitor values.

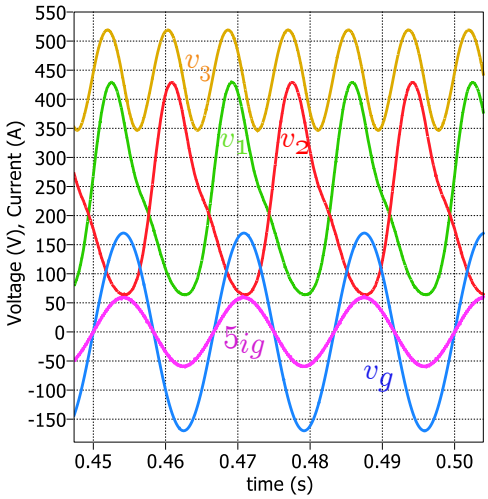
$$\text{Minimize } f = -\sum_{i=1}^{3} w_i \eta_{vi} + w_4(V) + w_5(C + C_3) - w_6 A$$

$$\text{Subject to} \begin{cases} VV_r(2C_3 + C) + CA^2 = \frac{V_g I_g}{2\omega} = \frac{S_g}{\omega} \\ v_1 > v_g \quad \text{if } v_g \geq 0 \\ v_2 > |v_g| \quad \text{if } v_g < 0 \\ V + V_r \leq V_{switch} \end{cases} \tag{4.13}$$

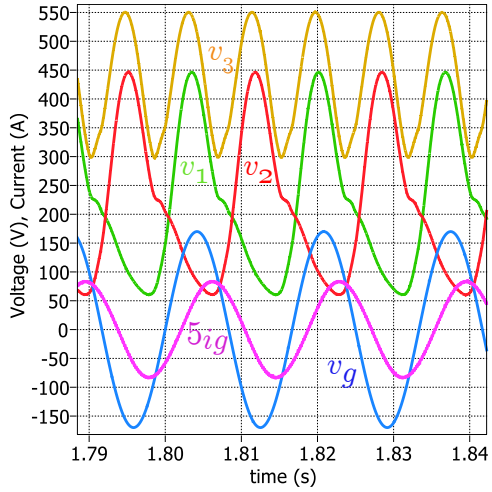
The corresponding simulation waveforms of capacitor voltages, DC-link voltage, grid voltage, and scaled grid current are shown in Figures 4.4a, 4.4b, and 4.4c respectively at 0.7 leading pf, UPF, and 0.7 lagging pf showing DC-link ripple. As previously discussed it is seen that the condition given in (4.5) has been satisfied in all three cases with the worst operating condition occurring at leading power factor when the v_g waveform barely touches v_1 and v_2 waveforms at the critical point.



(a) pf = 0.7 (lead)



(b) pf = 1



(c) pf = 0.7 (lag)

Figure 4.4: Waveforms from PLECS for Operating Condition Corresponding to V_g = 120 V, P = 1 kW, $v_3 = 530$, $A = 200$, $C_3 = 30$ μF, and $C = 12$ μF.

4.3.3 Pulsating Power Elimination

Additionally, from (4.11) it is seen that, P_t has a fourth-order component resulting from the interaction between the second-order terms in the capacitor voltages and currents. In conventional FB inverters with large decoupling capacitors and minimized voltage ripple on the dc-link, this term can be neglected. But with the

proposed decoupling approach, this residual ripple power in the dc-link of the PV inverter suggests that the elimination of fluctuating power is not complete.

To improve the performance of power decoupling, [82] PV with Leakage current and power decoupling) a voltage compensation term v_{comp} is introduced into the capacitor voltages as follows

$$v_{1c} = v_1 + v_{comp}; \qquad v_{2c} = v_2 + v_{comp} \tag{4.14}$$

such that the following differential equation is satisfied.

$$C\frac{d}{dt}\left(v_{1c}^2 + v_{2c}^2\right) + C_3\frac{d}{dt}v_3^2 = -V_g I_g \cos(2\omega t + \theta) \tag{4.15}$$

Numerically, it is complex to solve (4.15). Also it does not take into account the circuit non-idealities like the ESR of capacitors, on-resistance of the switches, series resistance of inductors, distortions caused by the deadtime, and effect of inductors on the pulsating power. However, this can be mitigated by the closed-loop implementation.

4.3.4 Operating Principles

The operation of the HBVS inverter is straightforward. Q_1 controls the boost stage gain so as to have double line frequency component on the dc-link and input is free of any ripple component. Its duty ratio d_b is given in (4.16) which is a dc superimposed on line frequency harmonic terms.

$$d_b = \frac{V + V_r \sin(2\omega t + \theta) - v_{in}}{V + V_r \sin(2\omega t + \theta)} \tag{4.16}$$

The duty ratio d_{bb} of Q_2 is given in (4.17) to control the HB capacitor voltages to provide the power decoupling as discussed in the previous section. The HB stage

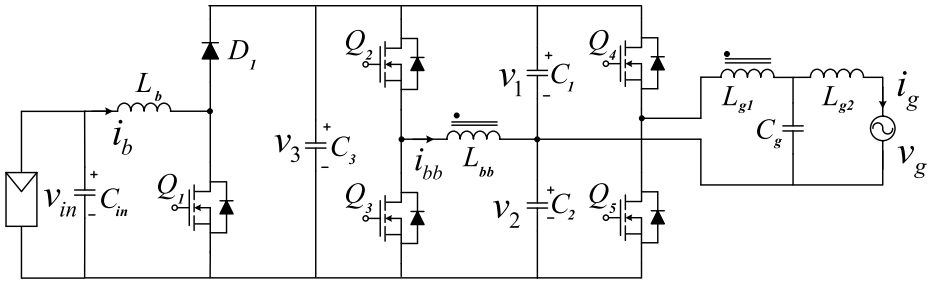


Figure 4.5: Proposed Integrated Magnetic Based Transformer-less String Inverter.

modulates the output ac waveform, the duty ratio d_{inv} of Q_5 is given in (4.18). Unlike in conventional HB inverters apart from the fundamental frequency component, d_{inv} also contains higher order harmonics. Q_3 and Q_5 operates complementary to Q_2 and Q_4 respectively with appropriate deadtime. In the presence of internal damping during the actual inverter operation, the exact duty ratio is to be determined using a closed-loop control scheme.

$$d_{bb} = \frac{V + 2v_{comp} + V_r \sin(2\omega t + \theta) - 2A \sin(\omega t + \zeta)}{2V + 2V_r \sin(2\omega t + \theta)} \tag{4.17}$$

$$d_{inv} = \frac{V + 2v_{comp} + V_r \sin(2\omega t + \theta) - 2A \sin(\omega t + \zeta) + 2v_g}{2V + 2V_r \sin(2\omega t + \theta)} \tag{4.18}$$

4.4 Integrated Magnetics

Figure 4.5 shows the topology of the transformer-less string inverter with integrated magnetics (IM) scheme. The advantages of transformer-less implementation offering reduced volume, lower cost, and higher efficiency can be further enhanced

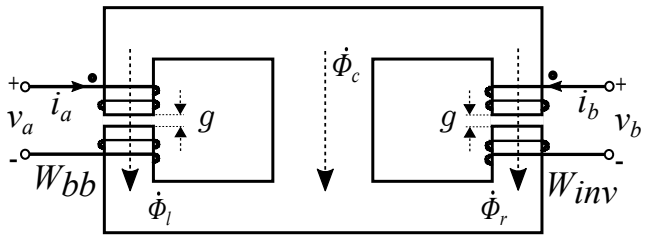


Figure 4.6: Integrated Inductor for Buck-Boost and Inverter Stage.

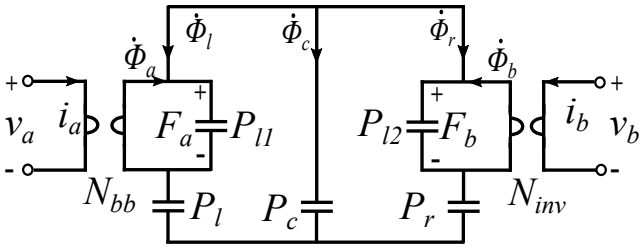


Figure 4.7: Gyrator Capacitor Model for the Integrated Inductor in Buck-Boost and Inverter Stage.

by IM scheme. For DC-DC application IM implementation has been shown to reduce converter volume with some improved performance features [83–87]. In [88] IM has been applied to parallel inverters leading to reduced volume and suppressed circulating current.

The inductors of half-bridge and power decoupling stages are integrated in one single core as shown in Figure 4.6. v_a and i_a are the voltage across and current through the winding W_{bb} (buck-boost stage inductor), and v_b and i_b are the corresponding variables for winding W_{inv} (inverter stage inductor). g is the air gap in each of the outer two limbs, the further details are discussed in the Section 4.4.

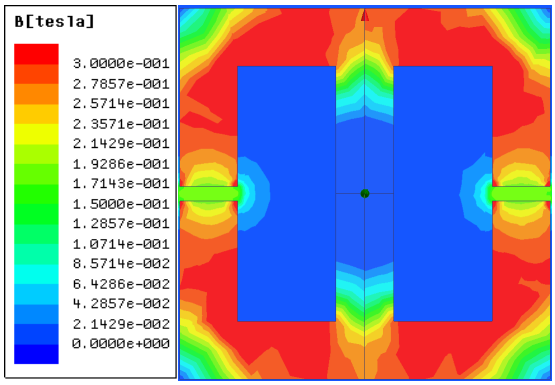


Figure 4.8: Flux density distribution in the magnetic core at one instant for the integrated inductor of the buck-boost and inverter stages with air-gap only at the outer limbs for minimized coupling.

4.4.1 Magnetic Circuit Analysis

The IM implementation is studied by using gyrator-capacitor model, where each winding W_{bb} and W_{inv} is modeled as a gyrator [89, 90] linking the electrical and magnetic domain as shown in Figure 4.7. N_{bb} and N_{inv} are the number of turns of each corresponding winding W_{bb} and W_{inv}, with $N_{bb} : N_{inv} = 1$. $\dot{\Phi}_l$, $\dot{\Phi}_c$, $\dot{\Phi}_r$ and P_l, P_c, P_r are the flux-rate and permeance of the left, center, and right limbs respectively. P_{l1} and P_{l2} are the leakage permeance of winding W_{bb} and W_{inv} respectively.

For the buck-boost stage inductor winding, the interface between the magnetic and electrical circuits are decided by the relationship given in (4.19).

$$v_a = N_{bb}\dot{\Phi}_a; \qquad i_a = \frac{F_a}{N_{bb}}; \qquad \dot{\Phi}_a = P\frac{dF_a}{dt} \tag{4.19}$$

where, v_a is the voltage, i_a is the current, F_a is the magnetomotive force (mmf), and $\dot{\Phi}_a$ is the flux-rate corresponding to the left limb with buck-boost inductor winding.

Similar expression can also be written for the inverter stage inductor winding on the right limb as given in (4.20).

$$v_b = N_{inv}\dot{\Phi}_b; \qquad i_b = \frac{F_a}{N_{inv}}; \qquad \dot{\Phi}_b = P\frac{dF_b}{dt} \tag{4.20}$$

4.4.2 Finite Element Analysis

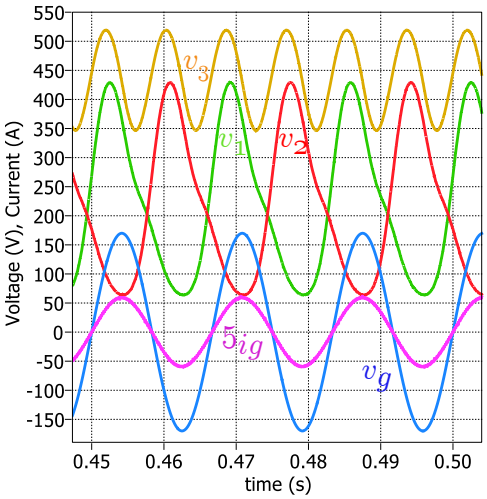
Ferrite core dimensions corresponding to E65/32/27 has been used for FEA with an air gap (g in Figure 4.6) of 2.5 mm in each of the outer limbs. The center limb does not have any air gap ensuring minimized coupling between the two windings. Thus $P_l, P_r \ll P_c$. Ansys Maxwell has been used for this analysis.

Figure 4.8 shows the flux density distribution at one particular instant, flux is shown to cancel in the center limb. With 32 turns of each winding, the inductance

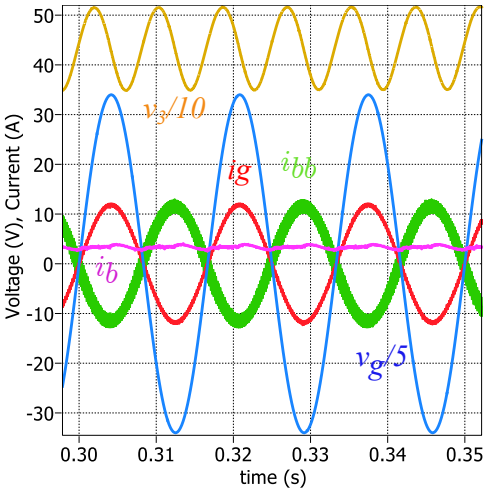
value of L_{bb} and L_{inv} is 214.24μH and mutual inductance is 6.32μH, obtained from FEA.

4.4.3 Simulation Results

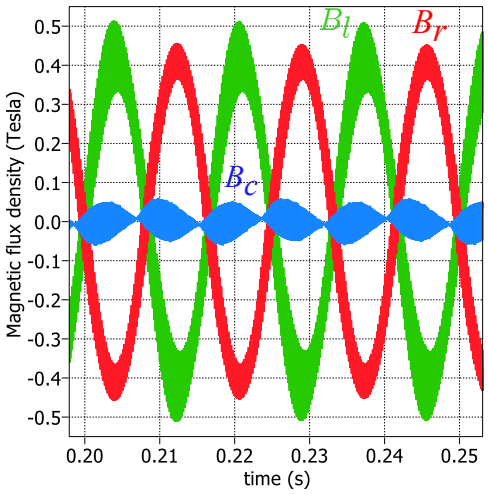
PLECS has been used for the circuit simulation, where the magnetic circuit is modeled with gyrator-capacitor structure as discussed. Figures 4.9a and 4.9b give the



(a) Voltage waveforms



(b) Current waveforms



(c) Magnetic flux density

Figure 4.9: PLECS waveforms for UPF Operation at $V_g = 120$ V, P = 1 kW, $v_3 = 530$, $A = 200$, $C_3 = 30$ μF, and $C = 5$ μF

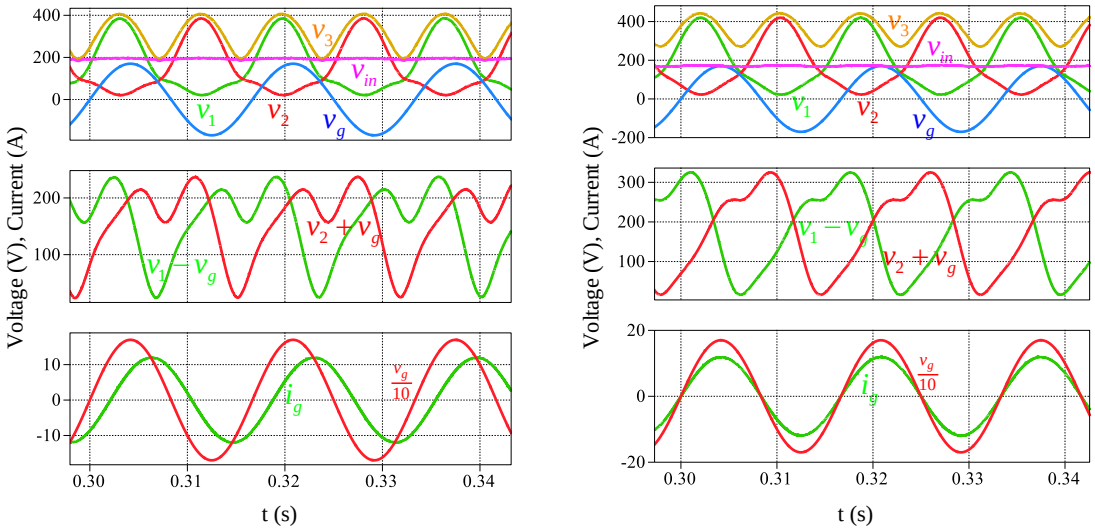
simulation waveforms of different voltage and current variables at the rated power and unity pf (UPF) operation. The flux density of left, center, and right limbs are shown in Figure 4.9c (B_l, B_c, and B_r respectively). It is to be noted that the buck-boost current is out of phase with respect to the grid current, thus the flux density of left and right limbs are out-of phase, with fundamental frequency flux being canceled in the center limb. As the flux is canceled, the cross sectional area of the center limb can be made smaller compared to that of the individual inductor case, thus further saving on the converter cost and volume. It is observed that the maximum flux cancellation is obtained when the switching frequency carrier signals of the buck-boost and inverter stages are in phase.

4.5 Efficiency Optimization

As the average switching loss in a converter over a grid cycle is proportional to the dc-link average V, the associated loss can be minimized by operating it at the minimum dc-link average value as required to instantaneously satisfy the no-over-modulation condition of (4.5) for different operating conditions. Also with lower V,

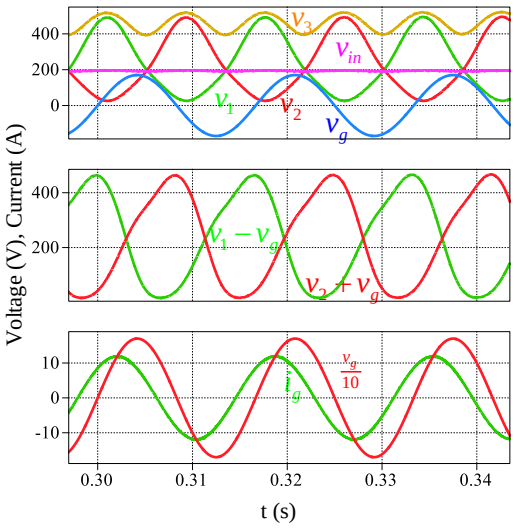
Table 4.2: Component Details

Component	**Parameters**
C_1 , C_2, C_3	12 μF/ 700 V (2), 30 μF/ 700 V
C_{in}, C_g	5 μF/ 500 V, 2.5 μF/ 300 V AC
L_b , L_{bb} , L_{g1}, L_{g2}	180 μH, 190 μH (2), 22 μH
Q_1 - Q_5	CREE C3M0120090D (5)
D_1	CREE C2D05120A



(a)

(b)



(c)

Figure 4.10: Steady state waveforms at 1 kVA showing converter voltages, grid current, and the voltage margin at (a) 0.7 lagging pf, (b) unity pf, (c) 0.7 leading pf operations highlighting the voltage margin of 20 V, fixed for each operating point by implementation of ADCL voltage control scheme.

the inductor current ripple can be decreased accounting for lower high frequency copper and core loss, directly translating into improved inverter efficiency.

The inverter is to be designed based on the worst operating condition which corresponds to the rated VA at leading pf case [10]. Once the decoupling capacitors are fixed, an adaptive dc-link (ADCL) average voltage can be implemented to operate it at the minimum dc-link average voltage thus improving the efficiency over wide power and pf range, as analyzed below.

4.5.1 Minimum DC-Link Average Voltage Requirement

Instead of a 0 voltage margin V_{mi}, over a grid cycle (4.5) can be modified as follows to accommodate requirements on the switch dead-time, limit on modulation margin (modulation index is limited to 0.95), and a non-zero ripple on v_{in}.

$$V_{m1} = v_1 - |v_g| > 0; \qquad V_{m2} = v_2 + |v_g| > 0 \tag{4.21}$$

From Section 4.3 it is clear that v_1 and v_2 and thus V_{m1} and V_{m2} are functions of the dc-link average voltage V, operating VA (S_g) and pf of the inverter. Thus a change on any one of S_g or pf parameters would allow a change in V, provided (4.21) is satisfied.

The dependence of V and V_{mi} on S_g is intuitive from decoupling power balance expression (4.12), whereas their dependence on pf can be observed from the steady state simulation results given in Figure 4.10. It gives the converter voltages (plot 1), grid current (plot 3), and the voltage margin (plot 2) waveforms corresponding to different operating pf - unity, 0.7 lagging, and 0.7 leading. Figure 4.10c shows that the leading pf gives the worst voltage margin [10] and thus needs a higher dc-link mean, whereas, lagging pf [see Figure 4.10a] gives the best margin requiring minimum dc-link mean. It has been accomplished by the ADCL scheme with the minimum voltage

margin V_{mi} over a grid cycle always being barely around 20 V at the critical point (Figure 4.10). It can be further seen that the constraints given in (4.5) have been satisfied in all three cases.

Additionally, though V_{mi} is not dependent on v_{in}, V is restricted by v_{in}. Because of the input boost stage, the minimum of the dc-link needs to be at least higher than v_{in} which limits its average. Thus while computing V through ADCL scheme, all the three parameters v_{in}, S_g, and operating pf need to be considered.

4.5.2 Adaptive DC-Link Scheme

For different values of S_g and pf different minimum V_{avg} is required to satisfy (4.21). However, it is very complex to derive the solutions of the optimal V for different S_g and pf values analytically. Therefore, numerical method is used to find the minimum V in MATLAB by sweeping the dc-link voltage average value over the specified operating range. 3-D plots showing the dependence of minimum V required are given in Figure 4.11 for various combination of S_g (swept from 100 to 1000 VA corresponding to 10 to 100 % of VA) and pf angle (swept from $-45°$ to $45°$ corresponding to 0.7 lagging and 0.7 leading pf respectively).

From the 3-D plot, the difference between the highest (for 0.7 leading pf at 100 % VA) and the lowest (for 0.7 lagging pf at 10 % VA) V is 56.76% for the specified range of operating conditions. It is 27.47% for UPF operation (fixed pf but varying S_g). But without the ADCL voltage scheme, V will always be set to the largest value even at conditions that does not require such high dc link voltage, and loss reduction could not be achieved. With adaptive dc link scheme the voltage at the best case condition can be reduced by 56.76% which corresponds to around 56.76% switching loss reduction (switching loss is linear with the voltage stress across the semiconductor) and even higher percentage of savings in the high-frequency inductor

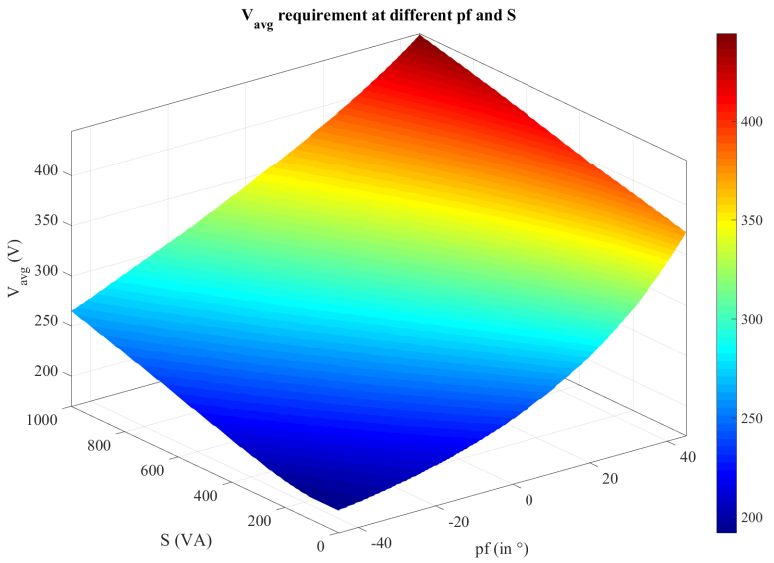


Figure 4.11: Relationship between the Minimum V Required to Satisfy (4.5) for Various Combinations of S_g and pf in the Given Operating Range.

core and copper loss.

Though the ADCL scheme does not interfere with the basic inverter control design, it is impossible or very difficult to be implemented with analog controller. In digital control platform, instead of providing a constant dc-link average as conventionally done, V will be decided based on the converter's operating point and provided as an reference to the dc-link controller. Alternatively, the values of V can be saved in a look-up-table (LUT) off-line corresponding to different S_g, v_{in}, and pf to save the computation burden on the digital controller.

4.6 Controller Implementation

4.6.1 Controllers

Figure 4.12 shows the overall controller block diagram in grid connected mode, the primary objective is to control the input voltage according to the MPPT reference and control the grid injected current as per the pf command. Without the input PV

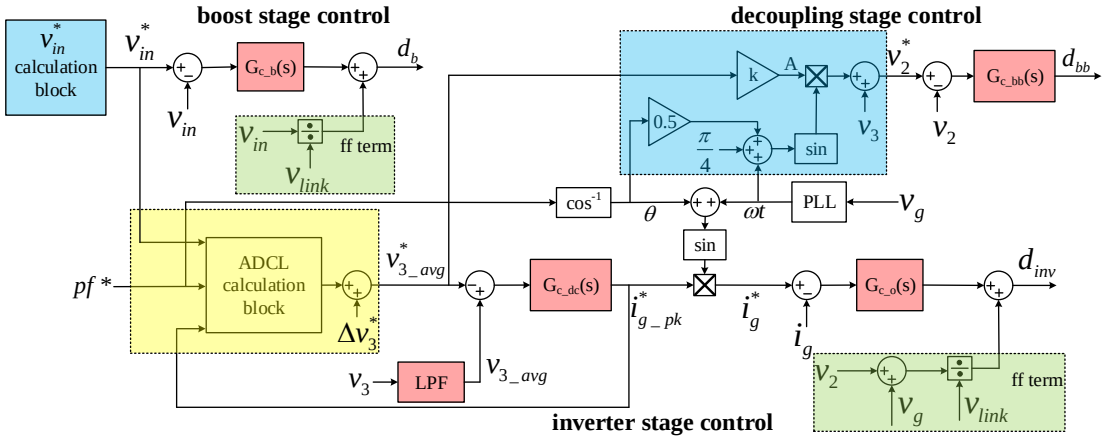


Figure 4.12: Controller Block Diagram of HBVS Inverter in Grid Connected Mode.

panel in the hardware setup, the input of the converter comes from a dc source in series with a resistor to closely mimic the PV characteristic.

Boost stage control

The objective of the input boost stage controller G_{c_b} is to regulate the input voltage such that v_{in} is free of any double line frequency ripple. Its reference is generated by MPPT controller, in this case it is provided manually. G_{c_b} has a high bandwidth to generate the boost stage duty d_b or else 120 Hz ripple would leak to v_{in} disrupting the MPPT efficiency when connected across the PV source.

Inverter stage control

PI controllers with appropriate feed forward terms are used for both the dc-link and inverter control loops as shown. The dc-link controller G_{c_dc} regulates the average of the dc-link voltage to a reference value generated by the ADCL voltage control scheme as detailed in the next section. A first-order low-pass-filter (LPF) with cutoff frequency of 12 Hz is used to filter out the 120 Hz component in the dc-link voltage before comparing it with the reference so as to remove the line frequency harmonics

in the controller response.

The output current controller G_{c_o} is designed to control the grid current with the current peak reference derived from the dc-link voltage control loop and the phase and frequency of the sinusoidal waveform determined by a phase-locked loop (PLL) and an external pf command. The output of the controller decides the inverter stage duty d_{inv}.

Decoupling stage control

By regulation of the duty ratio d_{bb} of Q_3, the decoupling stage controller G_{c_bb} controls the voltage v_2. As v_3 is already controlled to its reference by the inverter stage control, it implies v_1 is automatically controlled to (4.2). The reference generation for the lower capacitor voltage v_2 is highlighted with blue in Figure 4.12 .

Alternatively, as v_2 is an internal variable, its dynamic response is not critical. Without compromising the power decoupling support, it can also be operated open loop with the duty ratio given as

$$d_{bb} = 0.5 + \frac{A}{V}\sin(\omega t + \zeta) \tag{4.22}$$

where, ωt will be generated by the PLL block, similar to the closed loop scenario.

4.6.2 ADCL Calculation Block

The ADCL controller is highlighted in Figure 4.12. The calculation block is implemented with an LUT, which takes in the three operating parameters v_{in} S_g, and pf, and outputs the dc-link average reference. As LUT has one switching cycle response and requires minimal mathematical formulation, it is fast and stable but is affected by the parameters uncertainty. Thus a minor correction term Δv_3^* is added to the LUT output based on the flow-chart shown in Figure 4.13. This loop operates at line

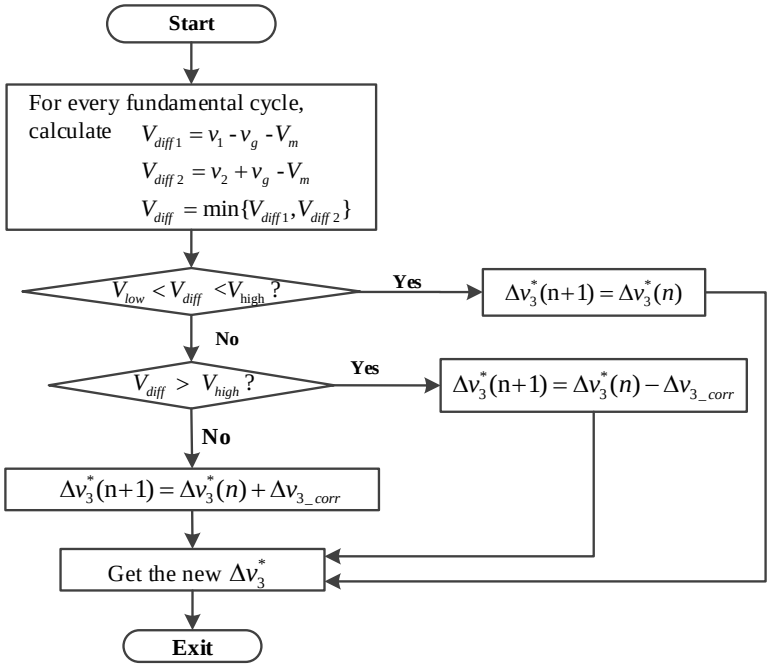


Figure 4.13: Flow-chart for Calculating Δv_3^* for the ADCL Voltage Controller Block.

frequency which calculates V_{diff} based on the following

$$\begin{cases} V_{diff1} = v_1 - v_g - V_m \\ V_{diff2} = v_2 + v_g - V_m \\ V_{diff} = \min\{V_{diff1}, V_{diff2}\} \end{cases} \tag{4.23}$$

where the value of V_m is user-defined. A hysteresis control algorithm calculates Δv_3^* in every iteration. If V_{diff} is within the predefined limit between V_{low} and V_{high}), Δv_3^* is preserved as previously stored value. But if V_{diff} is lower than V_{low}, the new Δv_3^* is obtained by adding a variable step Δv_{3_corr} given by (4.24). Otherwise, the new Δv_3^* is calculated by subtracting the same step. This calculation loop operates at a much slower rate (line frequency update in contrast to switching frequency response of LUT), but it provides an accurate regulation of the dc-link reference $v_{3\_avg}^*$.

$$\Delta v_{3\_corr} = KV_{diff} \tag{4.24}$$

4.7 Hardware Prototype and Experimental Results

4.7.1 Hardware Prototype

The hardware prototype of 1 kW inverter is shown in Figure 4.14. The component details are given in Table 4.2. The input is given in series with a 5 Ω resistor to mimic PV panel input. The controller is implemented in a customized DSP board built with TMS320F28335 (indigo board in Figure 4.14). The auxiliary power as required by the gate driver and controller section is derived externally.

Planar ferrite core E64/10/50-3C94 with appropriate air gap on all the three limbs are used for the inductors to have low profile design. Litz wire of 400 strands AWG 40 is used for the inductor winding to reduce high-frequency copper loss. The capacitors are chosen based on the rated voltage. SiC devices of rating 900 V, 23A, 120 mΩ are used as switches with external anti-parallel SiC schottky diodes to minimize the loss during dead-time. Avago ACPL 337J is used as the driver IC with negative voltage for reliable device turn-off.

4.7.2 Steady State Experimental Results

The experimental results represented in this section correspond to 1 kVA, UPF operation at steady state with specifications given in Table 4.1. Figure 4.15a shows the input voltage v_{in}, grid voltage v_g and current i_g, dc-link voltage v_3, and HB capacitor voltages v_1 and v_2. Figure 4.15b shows the magnified input voltage and different converter currents - input, decoupling stage inductor, and inverter stage inductor (i_{in}, i_{bb}, and i_{inv} respectively).

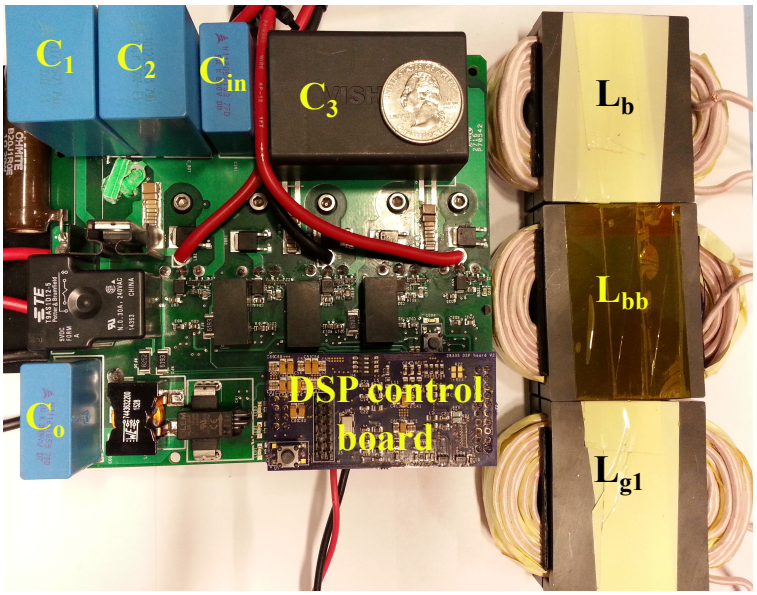
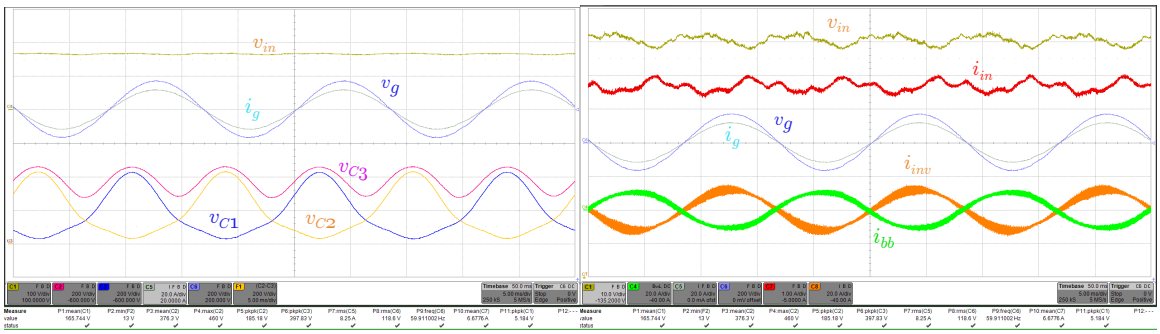


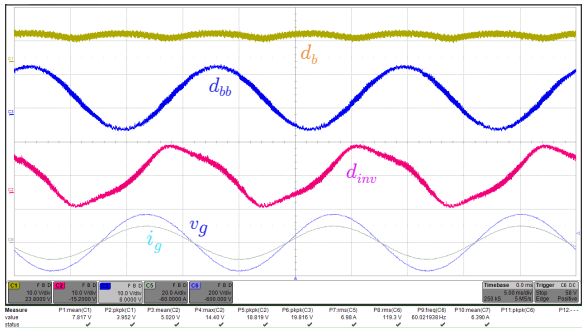
Figure 4.14: 1 kVA Experimental Prototype for the SiC Based Proposed HBVS Inverter.

The grid current has a THD of 2.6% calculated by using fast Fourier transform (FFT) in MATLAB on the measured i_g data. It can be noticed that the decoupling and inverter stages current are exactly out-of phase but with different ripple profile, as expected. The steady state waveforms demonstrate that the power has been decoupled through C_1, C_2, and C_3, whereas, the input voltage has very little peak-peak ripple constituting both the 120 Hz and switching frequency components. The 120 Hz ripple (obtained using MATLAB FFT) is only 3.5 V, which is 2.12% of the average input voltage of 165 V, demonstrating that the performance of input voltage controller is good in restricting the 120 Hz ripple only to the dc-link making the input free of double line frequency ripple resulting in higher MPPT efficiency.

Figure 4.15c shows the duty ratios of all the three stages. The duty ratio is obtained by cycle-by-cycle averaging of measured gate voltage V_{gs}. As V_{gs} is 20 V when turned ON and -6 V when turned OFF, the 0 and 1 of the duty ratio can be established from Figure 4.15c accordingly. It can be seen that, d_{bb} is sinusoidal whereas, d_{inv} which modulates v_1 and v_2, has double-line-frequency component to



(a) (b)



(c)

Figure 4.15: Steady state waveforms at 1 kVA, UPF operation with 165 V input, 375 V dc-link average, and 120 V/60 Hz output (time : 5 ms/div). (a) Input and outut voltage and current with the internal capacitor voltages (v_{in}: 100 V/div, v_1, v_2, v_3, v_g: 200 V/div, i_g: 20 A/div), (b) Magnified input current and voltage and converter currents (v_{in}: 10 V/div, i_{in}: 1 A/div, i_{bb}, i_{inv}, i_g: 20 A/div), (c) Cycle-by-cycle averaged duty ratios for all the three stages (i_g: 20 A/div, v_g: 200 V/div).

mitigate the influence of large 120 Hz dc-link ripple on the grid output. Also in order to regulate the input voltage to be a pure dc with ripple on dc-link, the boost duty ratio ($d_{Q_1} = d_b$) should contain 120 Hz component as shown.

Figure 4.16 shows the instantaneous drain-to-source voltage of the MOSFETs Q_1 ($V_{ds\_Q_1}$), Q_2 ($V_{ds\_Q_2}$), and Q_4 ($V_{ds\_Q_4}$) and the three inductor currents at around $-45°$ of the output voltage (between negative peak and zero crossing) at 100 kHz to highlight some of the switching waveforms using SiC MOSFETs.

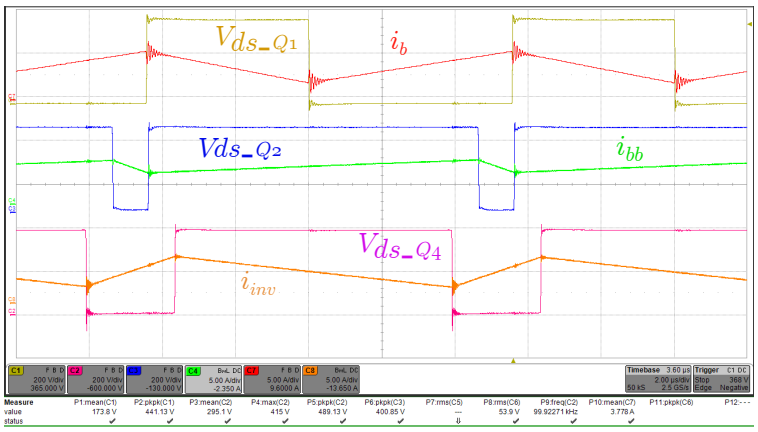
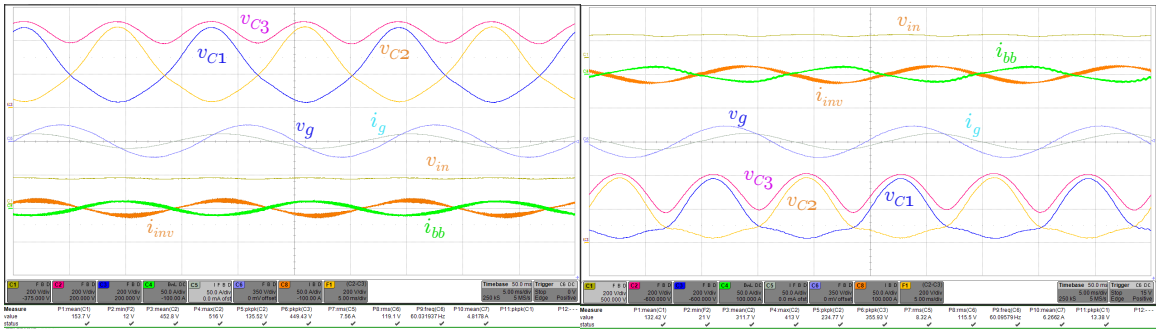


Figure 4.16: Instantaneous 100 kHz switching level waveforms at 1 kVA, UPF operation (voltage: 200 V/div, current: 5 A/div, time : 2 μs/div).



(a) (b)

Figure 4.17: Steady state waveforms at 1 kVA (v_{in}, v_1, v_2, v_3: 200 V/div, v_g: 350 V/div, currents: 50 A/div, time : 5 ms/div). (a) leading pf with 453 V dc-link average, (b) lagging pf with 311 V dc-link average.

4.7.3 ADCL Waveforms

The waveforms corresponding to 1 kVA non-upf operation with the ADCL voltage control scheme implemented is shown in Figure 4.17. The average dc-link voltage is computed within controller which is 453 V and 311 V for leading and lagging pf respectively. Figure 4.18 shows the transient waveforms of the inverter for an active-power step change from 1 kW to 500 W with $v_{in} = 165$ V, at UPF operation, i.e., $pf = 0°$. As can be seen, average value of v_{link} changes from 375 V to 329 V dynamically, as calculated from the ADCL control block. It also shows the voltage

margin $v_{c1} - v_g$ and $v_{c2} + v_g$ demonstrating that the margin finally settles to the minimum value after the step change. Also good tracking of step changes in active-power command with transient times well below one fundamental period can be observed from the waveforms in Figure 4.18.

4.7.4 Efficiency

Figure 4.19 shows the efficiency measured at UPF for different power levels based on California Energy Commission (CEC) requirement for PV inverters. The weighted CEC efficiency at switching frequency of 75 and 100 kHz is obtained to be 96.48% and 95.72% while a peak of 96.25% and 96.81% are measured respectively. These measurements do not consider the controller and auxiliary power consumption including the power for gate drivers, DSP controller, and other ICs which is around 2.7 W. It is to be noted that the peak as well as the CEC efficiency has been improved significantly by implementing the ADCL voltage control method, specially in the light load conditions.

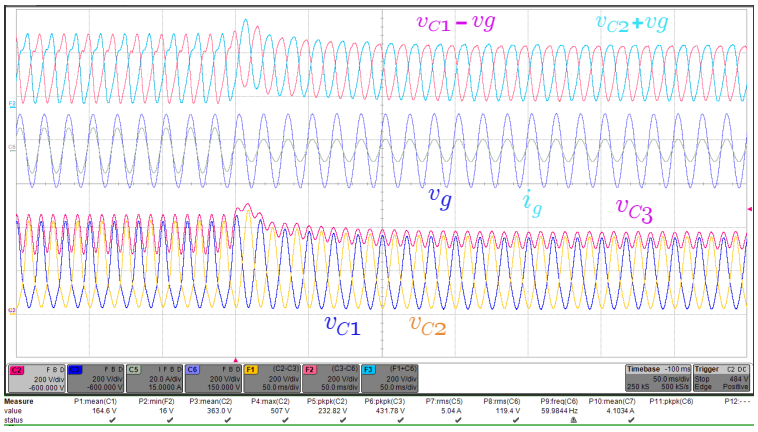


Figure 4.18: Step change response with the ADCL control implementation for 500 W to 1 kW step-up load showing the voltage margin (voltage: 200 V/div, current: 20 A/div, time : 50 ms/div).

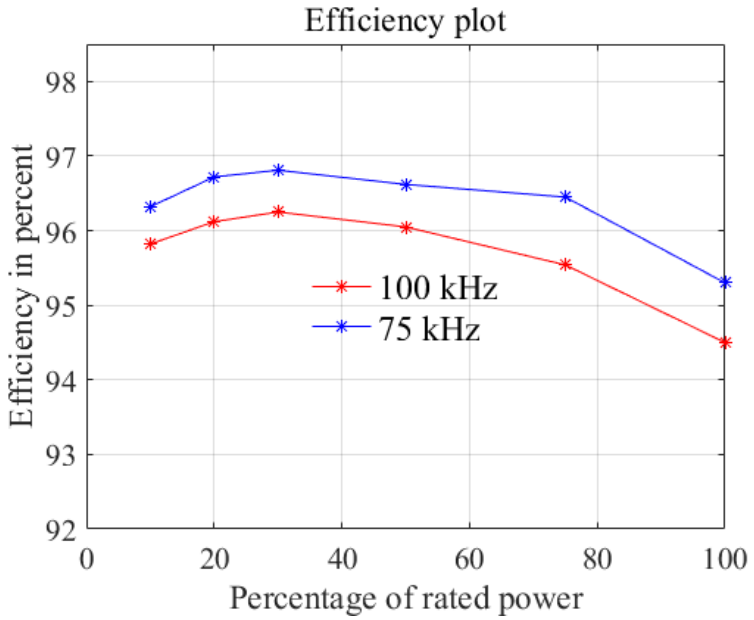


Figure 4.19: Efficiency of HBVS Inverter with ADCL Voltage Control Scheme Implemented.

4.8 Conclusion

An IM scheme for transformer-less string inverter which addresses both the challenges of transformer-less application has been thoroughly discussed. The proposed converter topology is a combination of boost and half-bridge stages along with a power decoupling stage. The capacitance required for power decoupling is minimized through active power decoupling scheme with a large voltage swing of half-bridge capacitors requiring only a total of 54 μF/kW at a peak of 550 V DC-link voltage for decoupling. The inductors of buck-boost and half-bridge inverter stages are integrated in one single E-core to furhte reduce the converter volume and cost. The experimental results with with integrated inductors at 1 kW, 120 V, 60 Hz output are provided from a 100 kHz SiC-based hardware prototype for validation of the concept.

Chapter 5

DOUBLY GROUNDED DYNAMIC DC-LINK (DDCL) INVERTER

5.1 Introduction

In this Chapter, another power decoupling technique is introduced based on a doubly grounded transformer-less PV inverter topology with active power decoupling built into the basic topology. It is based on a single stage of power conversion by a unique combination of boost-coupled half bridge circuit using only four switches overall and capable of supporting a wide range of power factor. This topology, termed as dynamic DC-link (DDCL) inverter, effectively addresses both the issues of single phase, transformer-less PV inverters, with the connection of AC neutral to PV negative terminal eliminating common mode module ground currents, and the active decoupling at high DC-link voltage resulting in DC-link capacitance that is well below the values used in state-of-the-art commercial products.

5.2 Operating Principles

Figure 5.1 shows the DC-DC boost stage followed by doubly grounded voltage swing inverter considered for the transformer-less microinverter application. The DC-DC stage is already discussed, which is the high gain boost converter.

The output of the DC-DC boost stage is the first DC-link v_{dc1} which is connected to the doubly grounded voltage swing inverter, i.e., the DC-AC stage. The later comprises of a synchronous boost stage which further boosts its input to a higher voltage v_{dc2} (a second DC-link), as it is advantageous to perform the decoupling at higher DC voltage from the perspective of capacitance volume. (5.1) and (5.2) give

the expressions for the corresponding DC-link voltage.

$$v_{dc1} = V_{dc1} + V_{r1}\sin(2\omega t + \theta) \tag{5.1}$$

$$v_{dc2} = V_{dc2} + V_{r2}\sin(2\omega t + \theta) \tag{5.2}$$

where, V_{dc1} and V_{dc2} are the nominal DC voltage and V_{r1} and V_{r2} are the amplitude of the ripple component for capacitors C_{dc1} and C_{dc2} respectively, and the grid power factor is given by $\cos\theta$.

The boost stage is followed by a half bridge inverter. The grid neutral is directly connected to the PV negative, thus the capacitive ground current is completely eliminated, a very critical requirement for transformer-less PV inverters. In order to regulate the grid current and voltage without distortion, the condition given in (5.3) needs to be satisfied instantaneously ensuring that the converter is not over-modulated at any operating interval.

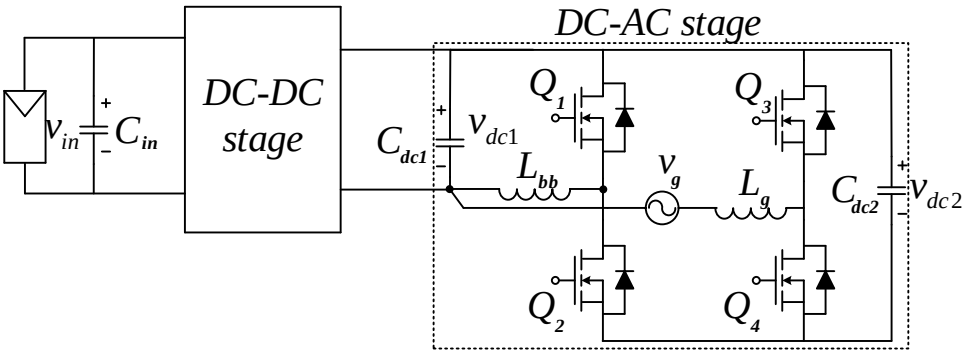


Figure 5.1: Transformer-less Microinverter Topology with a DC-DC Stage and Doubly Grounded DC-AC Stage.

$$\begin{cases} v_{dc1} > v_g & \text{if } v_g \geq 0 \\ v_{dc2} - v_{dc1} > |v_g| & \text{if } v_g < 0 \end{cases} \tag{5.3}$$

The grid voltage and current at an arbitrary power factor $\cos\theta$ is given in (5.4) and the corresponding instantaneous grid power is shown in (5.5).

$$v_g = V_g \sin(\omega t); \qquad i_g = I_g \sin(\omega t + \theta) \tag{5.4}$$

$$P_g = \frac{V_g I_g}{2} \left(\cos\theta - \cos(2\omega t + \theta)\right) \tag{5.5}$$

The 120 Hz ripple power supported by both the DC-link capacitors C_{dc1} and C_{dc2} are P_1 and P_2 respectively, as given in (5.6).

$$P_1 = \frac{1}{2}\frac{d}{dt}\left(C_{dc1} v_{dc1}^2\right); \qquad P_2 = \frac{1}{2}\frac{d}{dt}\left(C_{dc2} v_{dc2}^2\right) \tag{5.6}$$

Thus the total ripple power supported by both the capacitors $P_t = P_1 + P_2$ can be expressed as (5.7) by substituting for v_{dc1} and v_{dc2} from (5.1), (5.2) in (5.6).

$$\begin{aligned} P_t = {} & \omega C_{dc1}(2V_{dc1}V_{r1}\cos(2\omega t + \theta) + V_{r1}^2 \sin(4\omega t + 2\theta)) \\ & + \omega C_{dc2}(2V_{dc2}V_{r2}\cos(2\omega t + \theta) + V_{r2}^2 \sin(4\omega t + 2\theta)) \end{aligned} \tag{5.7}$$

By comparing the similar frequency terms ($2\omega t$) of P_g and P_t from (5.5) and (5.7), the relationship between C_{dc1} and C_{dc2} with the corresponding DC voltage levels and ripple component are obtained as given in (5.8).

$$C_{dc1}V_{dc1}V_{r1} + C_{dc2}V_{dc2}V_{r2} = \frac{V_g I_g}{4\omega} \tag{5.8}$$

This however, is not a closed form equation, and the values of the DC-link mean and ripple are optimized for the minimum total capacitance values with the constraint set by the switch voltage stress.

5.3 Capacitance Optimization

Figure 5.2 shows the flowchart to determine the optimum capacitance value. At first, various combinations of V_{r1}, V_{dc1}, V_{r2}, and V_{dc2} are obtained for different combinations of C_{dc1} and C_{dc2} values from (5.8). From all these values, the ones which satisfy (5.3) are stored as valid combinations, from which the minimum capacitor value is identified. The optimization is stopped once the number of iterations reached the maximum iteration length specified.

5.4 Controller Design and Simulation Results

Based on the microinverter specifications given in Table 5.1, the controllers (Figure 5.3) are designed and the corresponding simulation results are given in this section.

5.4.1 Controller Design

For the microinverter operation in grid connected mode, the objective of the controller is to control the input voltage according to the MPPT voltage reference which

Table 5.1: Converter Specification

Parameter	**Rating**
Input	20 V
Output	120 V, 60 Hz, 300 W
Switching frequency, f_{sw}	100 kHz

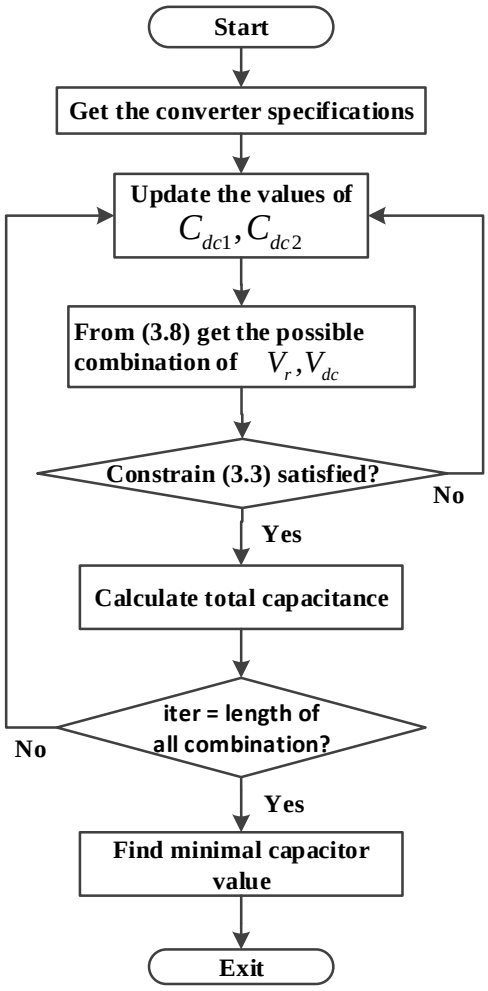


Figure 5.2: Capacitance Optimization Flow Chart for the Proposed Transformerless Microinverter Topology.

fixes the input power, control the grid current depending on the input power (with the fixed grid voltage), and control both the DC-link voltages to a mean value ensuring the voltage stress on the switches is kept within limits. However in the stand-alone operation, the input is a DC source in series with a resistor to coarsely mimic the PV panel characteristic. The output AC voltage is controlled to a reference value and the output power is determined by the AC load. Based on this the input voltage reference

is fixed. Figure 5.3 shows the basic controller block diagram employed to design the four basic controllers required for each of the stages of the proposed microinverter in stand-alone mode.

The controller block diagram shows that the EDR boost (DC-DC stage) controller has two control loops, the inner loop controls the input voltage and regulate the boost stage duty d_b. The input voltage reference is derived from an outer loop controller which controls the first DC-link voltage (v_{dc1}) based on the set reference. The DC-AC stage controller comprises of two independent stages to generate the duty of the second boost stage (d_{bb}) and the half-bridge inverter stage (d_{inv}). The first controller controls the mean of the second DC-link voltage (v_{dc1}) which sets the duty d_{bb}. Based on the sinusoidal reference value, the second controller regulates the output voltage through d_{inv}.

5.4.2 Simulation Results

Figure 5.4 shows the input (v_{in}), DC-link (v_{dc1}, v_{dc2}), and all the intermediate capacitor voltages (v_{c1}, v_{c2}) at 300 W, unity power factor (UPF) operation. It can

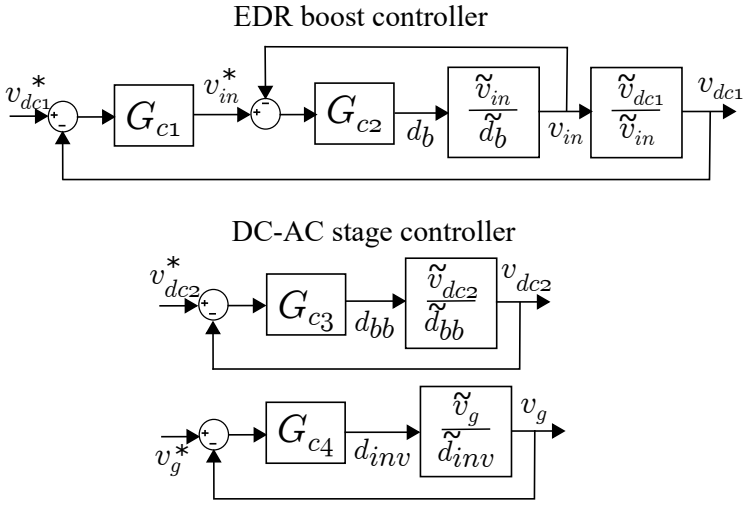


Figure 5.3: Controller Block Diagram in Stand-alone Operation for the Proposed Transformer-less Microinverter Topology.

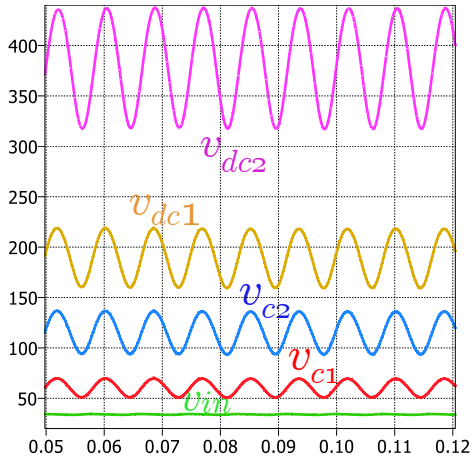


Figure 5.4: PLECS Simulation Waveforms for Input, DC-link, and all the Intermediate Capacitor Voltages at 300 W Operation.

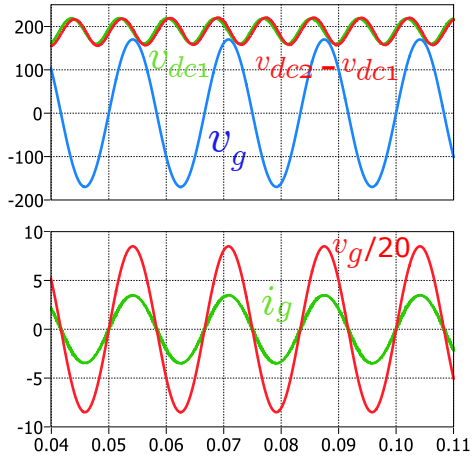


Figure 5.5: PLECS simulation waveforms at 300 W operation showing the first DC-link voltage v_{dc1} and the difference of the first and second DC-link voltage $v_{dc2} - v_{dc1}$ with the grid voltage showing the voltage margin between v_g and v_{dc1} and $v_{dc2} - v_{dc1}$, scaled output voltage and current.

be noticed that all the voltages have 120 Hz component, except for the input voltage which has been regulated to be free of any 120 Hz component, which would otherwise deteriorate the MPPT efficiency when connected across the PV panel.

Figure 5.5 gives the corresponding waveforms for v_{dc1}, $v_{dc2}-v_{dc1}$, v_g, and i_g showing the voltage margin between v_g and v_{dc1} and $v_{dc2} - v_{dc1}$. It is seen that throughout the operating range, the condition for no over-modulation as given in (5.3) is satisfied.

5.5 Hardware Implementation and Experimental Results

5.5.1 Component Selection and Hardware Prototype

Figure 5.6 shows the 3-level EDR boost followed by doubly grounded voltage swing inverter considered for the transformer-less microinverter application.

The component details for a 300 W DC-AC stage of microinverter are given in Table 5.2. The inductors are designed based on the allowed current ripple. Planar E38/8/25-3F3 has been used as the inductor core to obtain a low profile design. Litz wire (270 strands of AWG 42) has been used as the inductor winding. The component details for the DC-DC stage is same as discussed in Chapter 2.

A 300 W GaN based converter prototype has been developed, as shown in Figs. 5.7a and 5.7b. UCC27511 from Texas Instruments has been used as gate driver which has the provision for separate on and off gate resistors, critical for operation at high switching frequency. This allows the use of higher turn-on and lower turn-off gate resistance ensuring the reduction of ringing during turn-on for improved electromagnetic interference (EMI), as well as decreasing the chance of Miller turn-on of the complementary switch during the switch turn-off. In the present prototype, 20 Ω turn-on and 2.2 Ω turn-off gate resistors are used. EZDSP TMSF28335 has been used as the controller platform. LeCroy 6200A oscilloscope is used to capture the waveforms

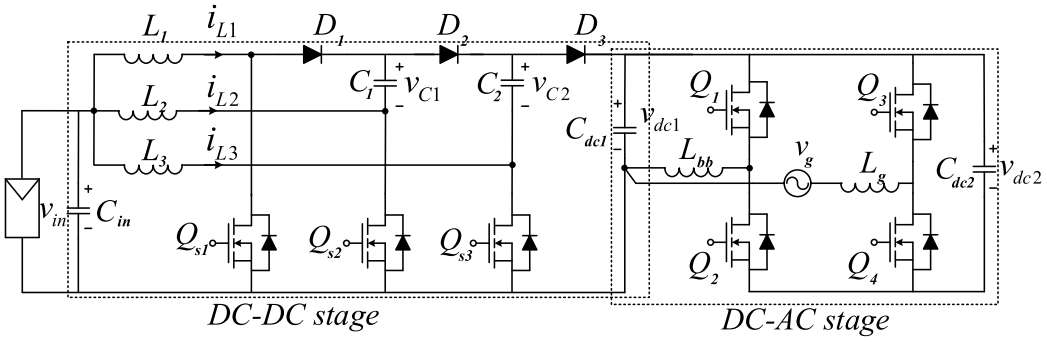
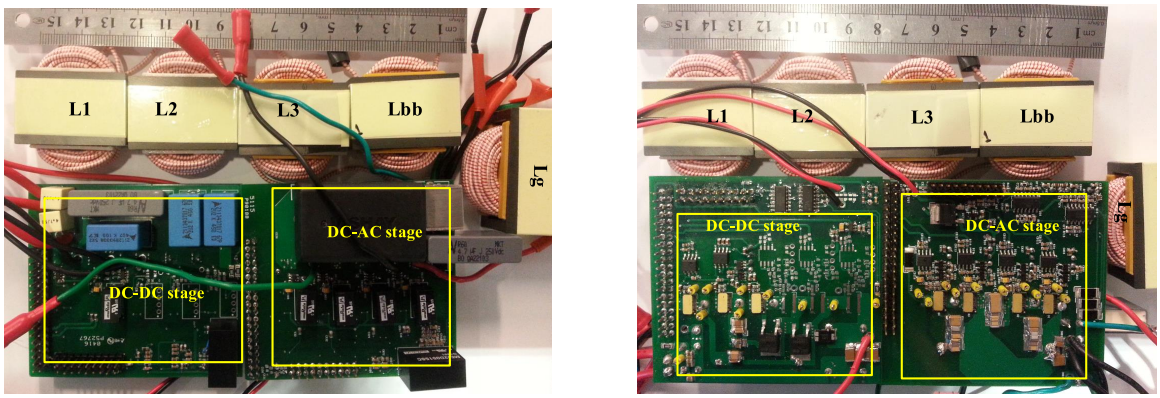


Figure 5.6: Transformer-less Microinverter Topology with a DC-DC Stage and Doubly Grounded DC-AC Stage.



(a) Hardware prototype top view

(b) Hardware prototype bottom view

Figure 5.7: GaN Based Hardware Prototype of Transformer-less Microinverter with EDR Boost and Doubly Grounded DDCL inverter.

Table 5.2: Component Details

Component	**Parameters**
C_{in} ,C_{dc1}, C_{dc2}	4.7 μF/ 50 V, 4.7 μF/ 300 V, 15 μF/ 575 V
L_b , L_g	190 μH, 630 μH
$Q_1 - Q_4$	GS66508P (4)

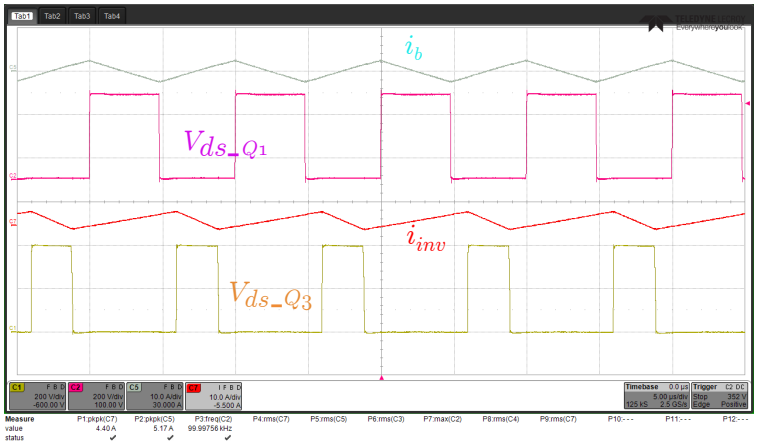


Figure 5.8: 100 kHz instantaneous switching level waveforms from hardware for the dc-ac stage at 300 W, UPF operation (voltage: 200 V/div, current: 10 A/div, time : 5 μs/div).

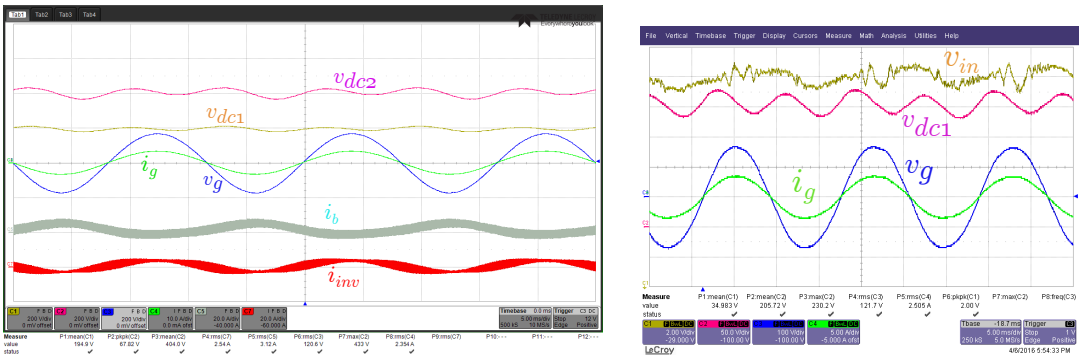
and power analyzer YOKOGAWA WT3000 is used to measure the efficiency.

5.5.2 *Switching Level Experimental Results*

Fig. 5.8 shows the instantaneous experimental waveforms for dc-ac stage. It gives the drain-to-source voltage of the MOSFETs Q_1 ($V_{ds\_Q_1}$) and Q_3 ($V_{ds\_Q_3}$) and the two inductor currents at around 25° of the output voltage (between positive peak and zero crossing) at 100 kHz switching frequency. At this instant, the peak-peak ripple of i_b is around 5.2 A and that of i_{inv} is around 4.4 A. It is to be noted that the boost inductor current ripple remains nearly constant while the inverter stage ripple varies with the point on the sine wave similar to any conventional inverter.

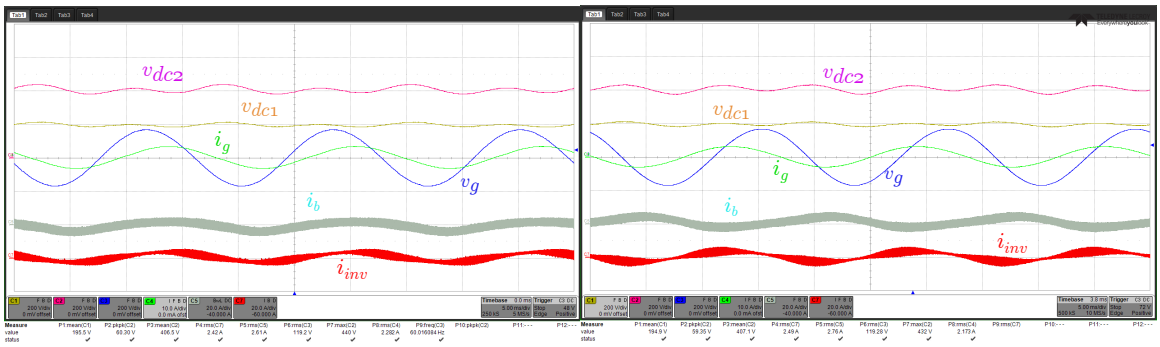
5.5.3 *Steady State and Dynamic Experimental Results*

In stand-alone mode, the experiments are performed with 45 V dc voltage source in series with a 1.1 Ω resistor to emulate the PV input characteristic, with an effective 35 V input to the microinverter. Figure 5.9 gives the closed loop operating waveforms for the microinverter operation from 35 V input to 120 V, 60 Hz output at 300 W, UPF. Figure 5.9a illustrates the waveforms of two dc-link voltages (v_{dc1}, v_{dc2}),



(a) (b)

Figure 5.9: Steady state experimental waveforms for GaN based transformer-less microinverter operating from 35 V dc input to 120 V, 60 Hz ac output at 300 W (time : 5 ms/div) showing (a) Output and two dc-link voltages, and output, buck-boost stage inductor, and inverter stage inductor currents (v_{dc1}, v_{dc2}, v_g: 200 V/div, i_g: 10 A/div, i_b, i_{inv}: 20 A/div), (b) Input, output, and first dc-link voltages, and output current (v_{in} : 2 V/div, v_{dc1}: 50 V/div, v_g: 100 V/div, i_g: 5 A/div).



(a) (b)

Figure 5.10: Steady state experimental waveforms for GaN based transformer-less microinverter operating at nominal operating condition illustrating the output and two dc-link voltages, and output, buck-boost stage inductor, and inverter stage inductor currents (v_{dc1}, v_{dc2}, v_g: 200 V/div, i_g: 10 A/div, i_b, i_{inv}: 20 A/div, time : 5 ms/div) at (a) 0.7 lagging pf, (b) 0.7 leading pf.

output voltage and current, and dc-ac stage inductor current (i_b, i_{inv}) corresponding to 100 kHz switching frequency. Both the dc-links have been shown to share the 120 Hz ripple, whereas, the input voltage is shown to have negligibly small double line frequency ripple [see Figure 5.9b] demonstrating that the MPPT efficiency would not be compromised. In Figure 5.9b the scale of v_{in} is magnified (2 V/div) to show the very small 120 Hz ripple in the input voltage (only 0.9 V 120 Hz component as obtained using MATLAB FFT which is 2.6% of the average input voltage of 35 V), thus verifying the closed loop controller performance is effective in restricting the double line frequency ripple from input.

Figs. 5.10a and 5.10b respectively show all the relevant waveforms for the 0.7 lagging and 0.7 leading pf operation with stand-alone load, which matches very well with the corresponding simulation results presented in earlier section. As expected, it can be observed that the voltage margin is maximum with the lagging pf and minimum with the leading pf [10], when the average of both the dc-link voltages are same for all the pf operations (i.e., over the entire range of the converter operation).

Figure 5.11 shows the transient waveforms of the inverter with a 50% step-up

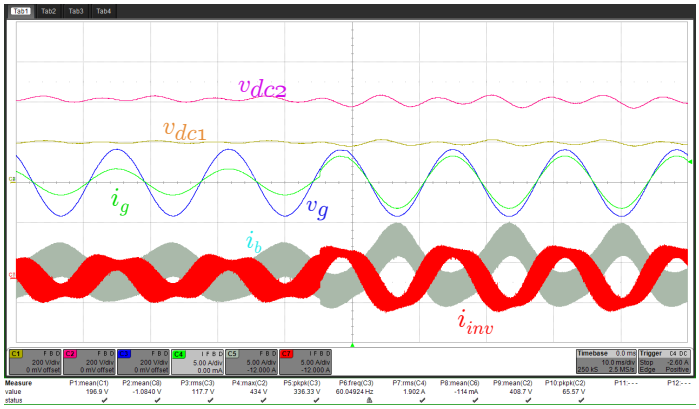


Figure 5.11: Experimental waveform for a step-up load change from 150 W to 300 W at UPF showing the output and two dc-link voltages, and output, buck-boost stage inductor, and inverter stage inductor currents (voltages: 200 V/div, currents: 10 A/div, time : 10 ms/div).

change (a step change of power from 150 W to 300 W) in the active-power at UPF operation. Good tracking of step changes in active-power command with transient times well below one fundamental period can be observed from the waveforms.

5.5.4 Efficiency

The power analyzer YOKOGAWA WT3000 is used to measure the efficiency of the converter. The peak measured efficiency for dc-dc EDR boost stage is 96.78% and 96.11% for 100 kHz and 200 kHz respectively. Whereas, the peak measured efficiency for the inverter stage is 97.91% and 97.45% for 50 kHz and 100 kHz respectively. Figure 5.12 shows the efficiency of the proposed 300 W non-isolated microinverter at different operating loads. The boost stage is always operated at 100 kHz and the inverter stage is operated at 50 kHz and 100 kHz to obtain the efficiency plots. At 50 kHz, the CEC and peak efficiencies are 94.09% and 94.43% respectively. And at 100 kHz, the CEC and peak efficiencies are 93.54% and 93.89% respectively. The reported efficiency does not include the controller and auxiliary power consumption of around 2 W required for gate drivers, DSP controller, and other control ICs.

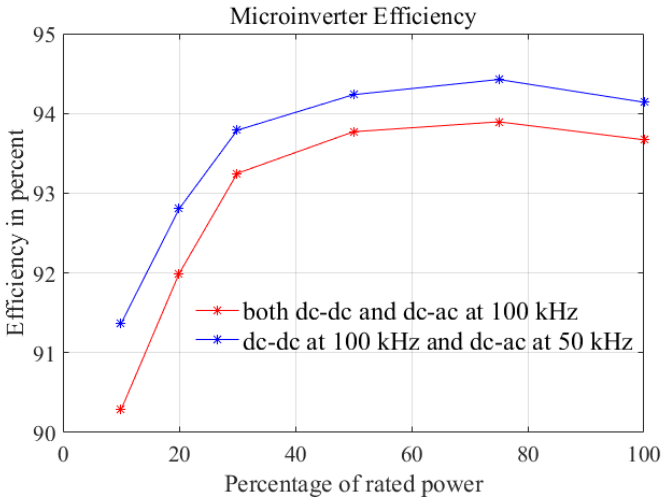


Figure 5.12: Efficiency plot for the proposed 300 W non-isolated microinverter with dc-dc boost stage operating at 100 kHz, and dc-ac voltage swing inverter stage operating at 50 kHz and 100 kHz.

Comparison of the proposed topology with a number of recently proposed microinverter topologies of comparable ratings in terms of the number of active components, voltage gain, presence of transformer, power decoupling capacitor used, and reported efficiency are presented in Table 5.3. It shows that the proposed converter has one of the higher reported efficiencies, while switching at relatively higher frequency and achieving significant reduction in decoupling capacitor requirement. However, there is still scope for efficiency improvement through better inductor and gate driver design using a lower gate resistor, which is a part of the future work.

5.6 Conclusion

An active power decoupling technique with doubly grounded voltage swing inverter has been discussed. The converter operation is elaborated along with the details of design and component selection. A 300 W GaN based experimental prototype for transformer-less microinverter has been developed and the experimental results validate the converter's operation with input of 40 V and 120 V, 60 Hz output and

Table 5.3: Performance Comparisons with Various Other Topologies

Topology	**No. of switches** (S, D)	V_{in}, V_o, P_{rated} (V), (V), (W)	**Isolation**	**Primary decoupling capacitor** (μF)	**Switching frequency** (kHz)	**Efficiency** (%) CEC	peak
Proposed	7, 3	35, 120, 300	non-isolated	film, 32	100	94.09	94.43
[91]	5, 0	45, 220, 250	isolated	electrolytic, 5000	50	NR *	94
[92]	5, 0	35, 230, 220	isolated	electrolytic, 18800	20	NR *	93
[93]	4, 3	48, 110, 200	non-isolated	film, 47	50	NR *	89.3
[94]	5, 0	50, 110, 300	non-isolated	electrolytic, 2200	50	94.43	94.55
[95] #	8, 17	45, 110, 120	isolated	electrolytic, 2000	70	92.4	93.1

* not reported

efficiency reported for 8 phases

operating at switching frequency of 100 kHz. The doubly grounded voltage swing inverter has the advantages of connecting the PV negative terminal directly to the grid neutral, thereby eliminating the capacitive-coupled common-mode ground currents.

Also through dynamically variable DC-link with large voltage swing approach, the decoupling capacitor is reduced.

Chapter 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

This dissertation is an effort to develop single phase transformer-less PV intervers for string and microinverter application, ensuring higher efficiency, high power density, wide band-gap device based high switching frequency, and reduced decoupling capacitance requirement through active power decoupling. A high gain DC-DC stage with advanced features have been proposed along with two power decoupling techniques for single phase inverter active power decoupling purposes. The following list presents a summary of the dissertation work:

- **Chapter 2** discusses the EDR boost converter for transformer-less high step-up application. Comprehensive analysis of converter operating principles, key theoretical waveforms, and steady state circuit performance corresponding to all the possible zones of operation have been presented for a 3-phase EDR boost converter. It is shown that inherent current sharing in three boost phases is only possible in Zone I operation. For Zones II and III equal current sharing can only be ensured with adapted duty ratio scheme until certain range of converter gain. Beyond this, though the current cannot be shared equally among phases, the per unit RMS current error can be minimized with modified duty ratio value and phase. The sharing scheme has been convincingly demonstrated in a 250 W GaN based hardware prototype for different operating regions at 200 kHz switching frequency.

- In **Chapter 3**, EDR boost has been studied for high step-up application in DCM operation. Comprehensive analysis of converter DCM operating principles, key theoretical waveforms, and steady state circuit performance corresponding to all the possible zones of operation have been presented. It is shown that inherent current sharing in three boost phases is possible in Zones I and II operation unlike for only Zone I in CCM operation. For Zone III, multiple operating cases exist with different combination of operating modes. It is straightforward to express the converter gain in 1st two zones, while for Zone III, the gain expression is obtained by curve fitting technique over the duty ratio range. Finally, the DCM operation analysis is validated in a 100 W GaN based hardware prototype for different operating regions.

- In **Chapter 4**, a power decoupling scheme for single phase inverters has been proposed. The converter topology is a combination of boost and half-bridge stages along with a power decoupling stage. A large sinusoidal swing of the half-bridge capacitors are allowed along with a double line frequency DC-link voltage ripple to address the power decoupling with a reduced capacitor value of only 40 μF/ kW at a peak of 550 V DC-link voltage. Further, the inductors of the buck-boost and the half-bridge inverter stages are integrated in one single core to reduce the converter volume and cost. The experimental results with the integrated inductors with SiC based hardware prototype are provided at 100 kHz for validation of the concept for string inverter application.

- In **Chapter 5** an active power decoupling technique with doubly grounded voltage swing inverter has been discussed. The converter operation is elaborated along with the details of design and component selection. A 300 W GaN based experimental prototype for transformer-less microinverter has been developed

and the experimental results validate the converter's operation with input of 40 V and 120 V, 60 Hz output and operating at switching frequency of 100 kHz. The doubly grounded voltage swing inverter has the advantages of connecting the PV negative terminal directly to the grid neutral, thereby eliminating the capacitive-coupled common-mode ground currents. Also through dynamically variable DC-link with large voltage swing approach, the decoupling capacitor is reduced to only 10 μF for 300 W microinverter.

6.2 Future Work

The potential future work for this research endeavor are listed as follows:

- Efficiency improvement of the string and micro inverters with improvements in magnetics design including coupled and integrated magnetics, through optimization of the gate drive circuitry and switching frequency.
- Design of more advanced controller like sliding mode control to enhance the PV inverters dynamic performance.
- Investigation of soft-switching technique to further push the efficiency of the high gain dc-dc converters. Additionally, topologies based on coupled inductor can be explored for high gain application.
- An interesting study would include coupling of the interleaved inductors in the EDR boost converter. Coupling will affect the converter current sharing. Also it will introduce inherent leakage inductances in the current path which can in turn be used for implementing soft switching.

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