Full Duplex CMOS Transceiver with On-Chip Self-Interference Cancelation

by

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ABSTRACT

The demand for the higher data rate in the wireless telecommunication is increasing rapidly. Providing higher data rate in cellular telecommunication systems is limited because of the limited physical resources such as telecommunication frequency channels. Besides, interference with the other users and self-interference signal in the receiver are the other challenges in increasing the bandwidth of the wireless telecommunication system.

Full duplex wireless communication transmits and receives at the same time and the same frequency which was assumed impossible in the conventional wireless communication systems. Full duplex wireless communication, compared to the conventional wireless communication, doubles the channel efficiency and bandwidth. In addition, full duplex wireless communication system simplifies the reusing of the radio resources in small cells to eliminate the backhaul problem and simplifies the management of the spectrum. Finally, the full duplex telecommunication system reduces the costs of future wireless communication systems.

The main challenge in the full duplex wireless is the self-interference signal at the receiver which is very large compared to the receiver noise floor and it degrades the receiver performance significantly. In this dissertation, different techniques for the antenna interface and self-interference cancellation are proposed for the wireless full duplex transceiver. These techniques are designed and implemented on CMOS technology. The measurement results show that the full duplex wireless is possible for the short range and cellular wireless communication systems.

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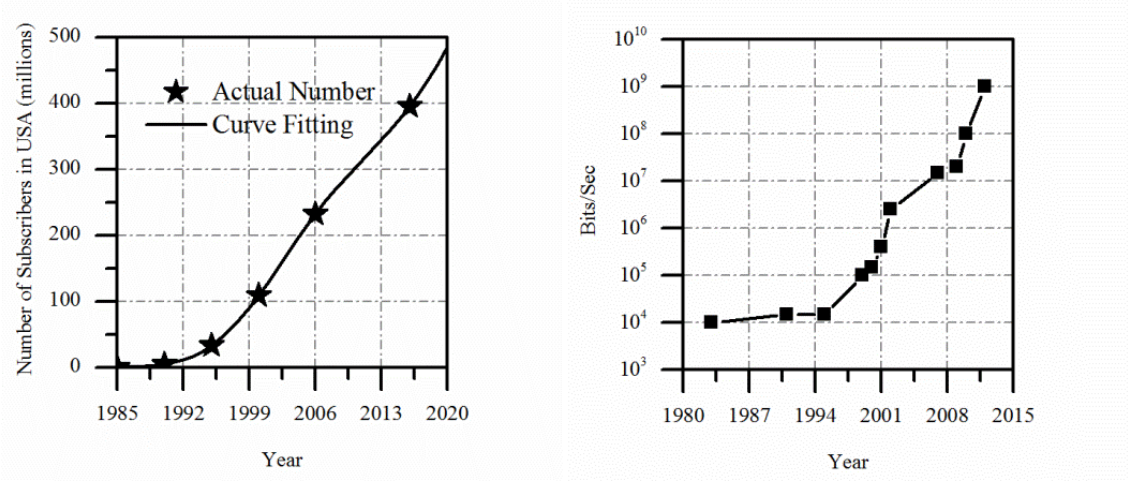
CHAPTER 1

INTRODUCTION

Nowadays, wireless telecommunication is one of the important parts of the human life. Phone calls, text messages, emails, access to the internet, and data transfer are the key applications of the wireless telecommunication. Wireless telecommunication telephony has been introduced in 1980s and completed in early 1990s which was the first generation of the wireless telecommunication systems, it was completely analog, and it did not have the digital data transfer. Demand on the higher data rate and larger bandwidth has led the wireless telecommunication system to the fifth generation (5G) which can provides up to 1 Gbps data rate [1].



(a) (b)

Figure 1-1 (a) Number of the Cellphone Subscribers in USA [2] and (b) Data Rates of the Wireless Telecommunication [3].

Not only the demanded data rate is increasing, but also the number of the subscriber of the telecommunication system is increasing. Figure 1-1 (a) shows the number of

cellphone subscription in United States since 1985 [2], and Figure 1-1 (b) shows the data rate of the cellphones [3]. As it is shown, both number of the cellphone subscriber and the data rate is increasing significantly. But, the electromagnetic spectrum is a limited physical parameter. Consequently, improving the efficiency of using of the electromagnetic spectrum is very important in designing and implementing the telecommunication systems.

Next generation of the wireless telecommunication, 5G, which is going to be started working in 2020, will be 20 times faster than the fourth generation (4G). Besides, it increases the number of the devices 900,000 per square kilometers, and the latency in the system will be reduced to one tenth. Using millimeter wavelength and small cells will increase the bandwidth of the 5G [4].

Improving the spectral efficiency in this telecommunication system relies on full duplex wireless, Massive Multi Input Multi Output (Massive MIMO), and Device to Device (D2D) communication [4]. Full duplex wireless is a novel wireless system which enables transmitting and receiving the data at the same time and the same frequency. In this dissertation, antenna interface, Receiver (RX), and self-interference cancellation for full duplex wireless has been proposed which enables transmitting and receiving the data at the same time and the same frequency.

1.1 Full Duplex Transceiver

Conventional wireless telecommunication systems work in Half-Duplex mode. Half-Duplex wireless is divided to two subcategories: Frequency Division Duplexing (FDD) and Time Domain Duplexing (TDD). In TDD, Transmitter (TX) and RX use the

same frequency channel at the different times, and in FDD, TX and RX use different frequency channels simultaneously. In the both cases, there is no Self-interference (SI) signal in the frequency channel of the RX. The challenge in the TDD is the switches of the front end which has to share the same antenna between the TX and the RX, and the challenge in the FDD is the duplexer and filters which separate the TX and RX.

Full duplex wireless enables transmitting and receiving the data at the same time and the same frequency which is neither TDD nor FDD. Simultaneous transmitting and receiving the data eliminates the front end switches from the Transceiver (TRX), and using the same channel frequency for both TX and RX eliminates the filters from the front end. Figure 1-2 shows the TDD, FDD, and full duplex wireless versus time and frequency. As it is shown in this figure, the SI in the RX should be cancelled to not degrade the RX performance.

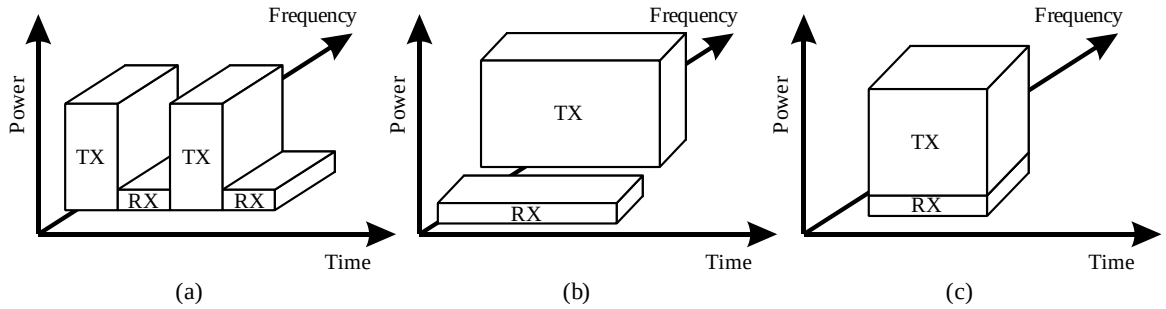


Figure 1-2 TX and RX Signals in (a) TDD, (b) FDD, and (c) Full Duplex Wireless Systems.

Not only full duplex wireless can improve the channel efficiency, but also it simplifies the management of the electromagnetic spectrum, reuses radio resources in small cells in the 5G to eliminate the backhaul problem, and reduces the costs of the telecommunication systems [5, 6]. In hardware point of view, it removes the large and

expensive filters in the TRX front ends which simplifies the circuit of the TRX and reduces the size of the TRX.

Similar to all the engineering problems, full duplex wireless has its own problems and challenges. The main challenge in a full duplex TRX is the huge power of the SI signal in the RX. As an example, for a transceiver with 20 MHz Bandwidth (BW), 10 dB Noise Figure (NF), and 23 dBm TX average power, the SI signal power is 114 dB above the RX noise floor. To solve this problem, SI cancellation is necessary in the full duplex wireless TRX.

If the required SI cancellation is not provided in the full duplex wireless TRX, the SI signal will degrade the RX performance and reduces the channel efficiency of the telecommunication system. Another problem in full duplex wireless is the telecommunication channel between TX and RX which changes versus time; therefore, an adaptive method for SI cancellation is required. The adaptive method can also reduce the channel efficiency of the telecommunication system. It has to be considered that the channel efficiency of the Half Duplex wireless is 50 %; consequently, losing the channel efficiency more than 50 % in the full duplex wireless makes it useless.

In [7], a full duplex wireless TRX has been demonstrated by using off the shelf components as shown in Figure 1-3. A ferromagnetic circulator shares the same antenna between TX and RX and provides about 15 dB SI cancellation. A SI cancellation circuit at the Radio Frequency (RF) has been proposed which provides more than 50 dB SI cancellation before the Low Noise Amplifier (LNA). The RF SI cancellation circuit consists of multiple microstrip delay lines with controllable attenuation. This circuit sample the TX signal after the Power Amplifier (PA), and inject the modified version of

the TX signal in to the RX input to provide SI cancellation. The remnant of the SI signal is cancelled in digital domain. In this demonstration, the bandwidth of the full duplex wireless TRX is 80 MHz, its TX power is 20 dBm, and the total SI cancellation is 110 dB.

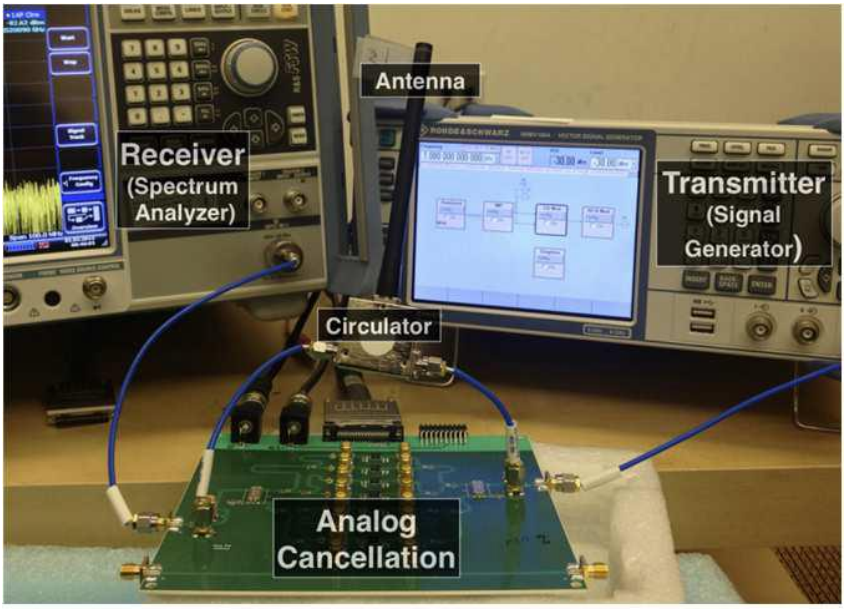


Figure 1-3 A Demonstrated Full Duplex TRX with off the Shelf Components for Full Duplex TRX [7] (Figure 6 in [7]).

1.2 Objectives

In this research, full duplex wireless TRX front end and analog leakage cancellation is designed, fabricated, and measured. The proposed structures enable the full duplex wireless for different applications. To achieve this goal, the following requirements have to be satisfied.

- TRX front end should provide enough power for the TX.
- The Noise Figure (NF) of the RX must meet the requirement.
- The SI signal should not degrade the RX performance (NF and gain).

- The power of the SI signal must be within the Analog to Digital Converter (ADC) dynamic range.
- The total SI cancellation should be enough to push the SI signal below RX noise floor.
- An adaptive algorithm is required to track the telecommunication channel variations in time domain.

1.3 Summary of the Following Chapters

This dissertation is organized as follows,

- CHAPTER 2: *Review of Full Duplex TRX and Leakage Cancellation*. In this chapter different techniques and structures for the antenna interface which connects the TX and RX to the antenna is discussed. Besides, state of the arts SI cancellation in analog and digital domain is evaluated.

- Chapter 3: *Integrated Quasi-Circulator*. An integrated reconfigurable CMOS quasi-circulator operating at 2.4 GHz is presented. A passive structure delivers transmit Power Amplifier (PA) output signal to the differential Low Noise Amplifier (LNA) input as a common-mode signal and simultaneously delivers received signal as a differential-mode signal at the LNA input. The leakage of the PA output signal at the LNA input is reduced in two steps. First, the use of a reconfigurable impedance matching circuit, instead of a fixed 50 Ω resistance reduces the leakage by compensating the antenna impedance mismatch, and improves transmitter-

receiver isolation. Second, a reconfigurable summing stage adds amplitude and phase adjusted PA output signal to LNA output to cancel the residual PA output leakage. Measurement results show that the receiver achieves a reduction of 90 dB for a single tone and more than 50 dB for a QPSK modulated 40 MHz bandwidth transmit signal. The receiver gain is more than 10 dB and the noise figure in the receiver path is 4.5 dB. The reconfigurable quasi-circulator along with the receiver LNA is designed and fabricated on a 130 nm CMOS technology. The cancellation circuitry occupies 0.27 mm^2 and consumes 30 mW quiescent power, while the total active area of the chip is 1 mm^2, and it consumes 65 mW power.

- Chapter 4: *Reconfigurable RX with On-Chip Hybrid and Baseband Leakage Cancellation*. A reconfigurable CMOS RX with a highly linear hybrid and baseband SI canceller operating at 1.7-2.7 GHz is presented. A passive hybrid delivers transmit PA output signal to the antenna and simultaneously delivers received signal as a differential-mode signal to the mixer first RX input. The power of leakage of the PA output signal at the RX input is reduced in two steps. First, the use of a reconfigurable impedance matching circuit compensates the antenna impedance errors, and second, a reconfigurable baseband SI canceller adds the amplitude and phase adjusted PA output signal to RX baseband to cancel the residual PA output leakage. Measurement results show that the receiver achieves a reduction of 70 dB for 20 MHz bandwidth transmit signal. The receiver gain is more than 50 dB and the noise figure in the receiver path in the full

duplex mode is 11.5 dB. The reconfigurable proposed structure is designed and fabricated on a 65 nm CMOS technology. The cancellation circuitry occupies 4 mm^2 and consumes 110 mW quiescent power.

- CHAPTER 5: *Conclusion and Recommendations*. This chapter concludes the dissertation and provides recommendations for the future works.

CHAPTER 2

REVIEW OF FULL-DUPLEX TRANSCEIVER AND LEAKAGE CANCELLATION

2.1 Introduction

Conventional TRXs which are working in TDD or FDD wireless networks are well known in state of the art literature. In TDD, the TX and RX share one antenna by using a switch or use two different antennas to transmit and receive the data; in addition, there is no SI signal while the TRX is receiving the data. In FDD, the TX and RX share one antenna by using duplexer or use two different antennas; but, this is not enough for the FDD TRX since there is a large SI signal while the RX is receiving the data. Consequently, additional filtering or SI cancellation is necessary in FDD TRX to suppress the SI signal power.

In full duplex TRX, using a switch between the antenna, TX, and RX is not possible because TX and RX work simultaneously. In addition, using filters are also not possible because TX and RX work at the same frequency. Consequently, using two different antennas for the TX and RX or using one antenna if a circulator or a hybrid is used, are the only options which have been used in the state of the art literature in the TRX front end.

As mentioned before, the SI signal power after the antenna interface is still large for the RX in a full duplex TRX. Therefore, using a SI canceller is necessary which can be implemented at the RF, baseband, and digital. In this chapter, first, basic of the full duplex TRX is presented, and then different methods for the antenna interface and SI cancellation is discussed.

2.2 Basic of Full-Duplex Wireless TRXs

A general full duplex TRX is shown in Figure 2-1 which consists of TX, RX, antenna interface, analog self-interference canceller, and digital SI canceller. The TX signal in digital domain $s(f-f_{LO})$ is converted to analog by a Digital to Analog Converter (DAC) and up-converted by the mixer. Then, the up-converted TX signal is amplified by the PA. The transmitted signal after the PA goes to the antenna by passing through the antenna interface. The received signal goes to the RX from the antenna by passing through the antenna interface. In addition to the received signal current, a portion of the transmitted signal also goes to the RX which is the SI signal. The SI signal power is very large for the RX; therefore, RX needs a large dynamic range. An additional SI cancellation is necessary in analog domain to relax the RX from the high power SI signal. As shown in Figure 2-1, the TX signal can be sampled at the baseband, RF, or after the

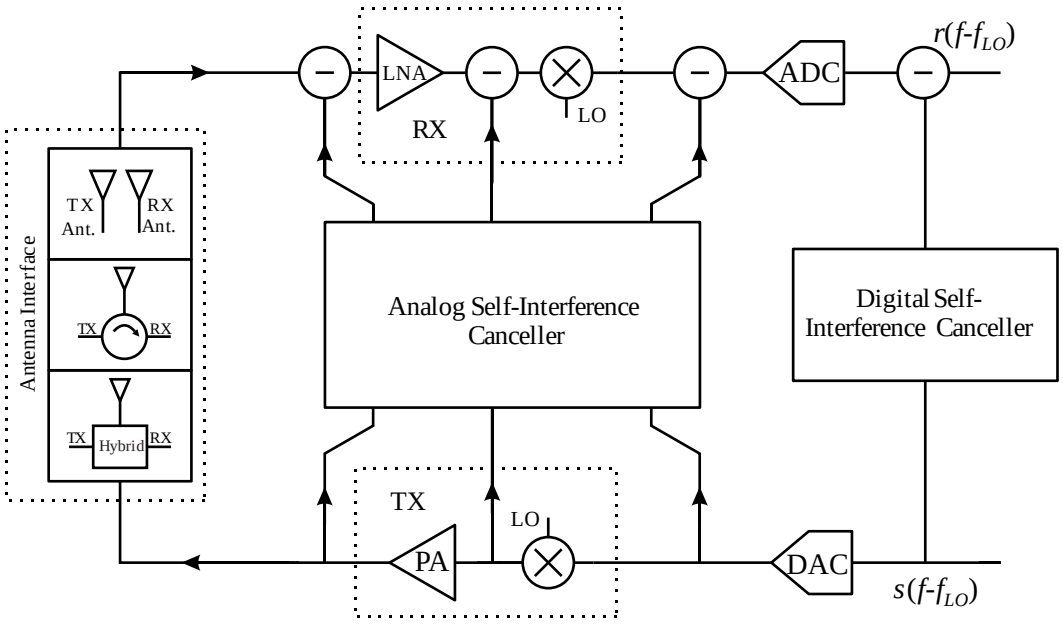


Figure 2-1 Full Duplex TRX with Antenna Interface, Analog SI Canceller, and Digital SI Canceller.

PA and then gets modified to generate the proper cancellation signal. The cancellation signal can also be injected into the different points of the RX such as before the LNA, after the LNA, or the baseband to provide analog SI cancellation in the RX. Finally, the remnant of the SI signal is cancelled in digital domain after the Analog to Digital Converter (ADC). The signal after the digital SI cancellation $r(f\text{-}f_{LO})$ should only be related to the desired received signal at the antenna, and the SI signal has to be below the RX noise floor.

2.3 Antenna Interfaces

Antenna interface is the most important part of the full duplex TRX which connects the TX and RX to the antenna system as shown in Figure 2-1. Antenna interface sees the maximum power of the TX and simultaneously, sees the minimum noise power in the RX path. Consequently, the antenna interface has to provide a very large dynamic range and work with the maximum power of the PA and RX noise power without degrading them. This puts a stringent requirement for the antenna interface maximum power handling, linearity, and noise floor. Antenna interface can be implemented by different antennas for TX and RX, or by one antenna for TX and RX if a circulator or hybrid is used. In all these cases, a tuning circuit is necessary to improve the SI cancellation in the antenna interface. In this section, all of these methods are discussed.

2.3.1 Antenna Separation for TX and RX Antennas

Using different antennas as antenna interface in the full duplex TRX provides SI cancellation between TX output and RX input. The SI cancellation in this system is a

function of the antennas' positions such as the distance and angle between the antennas. In addition, antenna polarizations and the environment around the antennas affect the SI cancellation between two antennas [8].

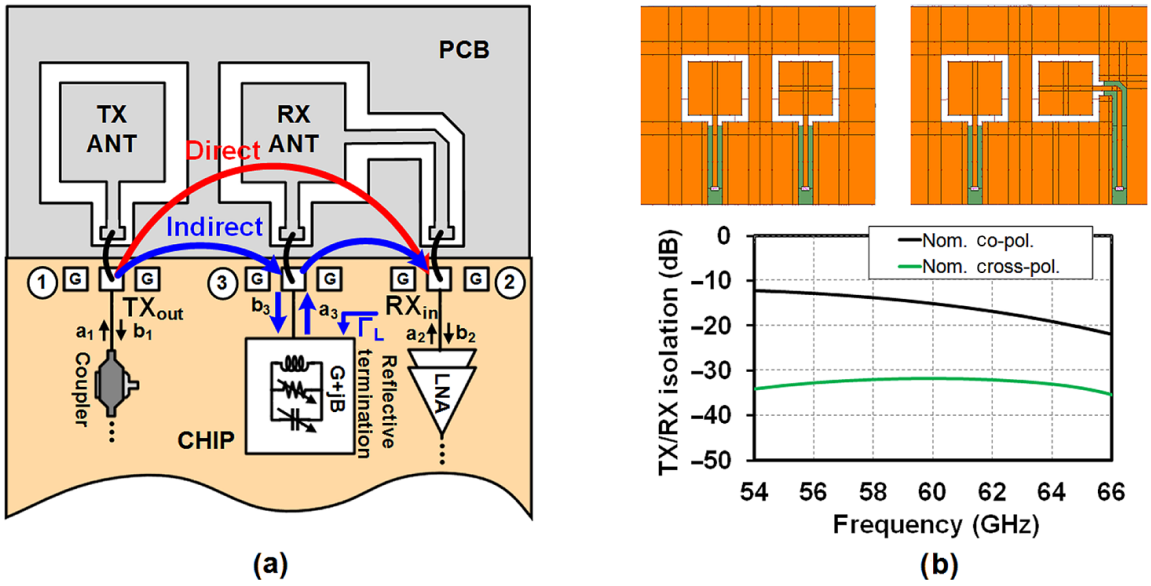


Figure 2-2 Antenna Interface Proposed in [9] (Fig. 6 in [9]) with Antenna Tuning Circuit.

Since the SI cancellation is a function of the environment around the antennas and the environment is not fixed, additional circuit is necessary to keep the maximum SI cancellation in the antenna interface at all times. An antenna interface at 60 GHz with an on-chip tuning is proposed in [9] which provides more than 30 dB SI cancellation. In this design, the antennas distance and polarizations are optimized to provide a good SI cancellation in the antenna interface. Then, an additional port is added in the RX antenna for the tuning circuit. The tuning circuit doesn't degrade the RX performance. In this structure, two leakage paths are considered between TX and RX antennas. First path is the direct path and the second path is the indirect path as shown in Figure 2-2. The

indirect path sees the tuning circuit which is the reconfigurable impedance and the transfer function of the indirect path is tuned by the reconfigurable impedance.

The advantages of using different antennas for the TX and RX are no insertion loss between the TX and the antenna, no insertion loss between the antenna and the RX, and no non-linear response in the path between the TX and RX. But the disadvantage of using different antennas as antenna interface is the size of the structure for the application below 3 GHz. For frequencies below 3 GHz, the antenna size and the required distance between the antennas can be more than 20 cm.

2.3.2 Circulator and Quasi-Circulator

A circulator is a three port component which conducts the signal between the ports in one direction and rejects the signal in the opposite direction. A circulator is shown in Figure 2-3 (a). A circulator with an antenna can be used as an antenna interface in the full duplex TRX. Indeed, a circulator shares the same antenna between TX and RX and conducts the TX signal from the TX to the antenna, conducts the received signal from the antenna to the RX, and isolates the TX and RX. In a circulator as shown in Figure 2-3 (a), the signal from the RX can also be conducted to the TX which is unnecessary. Instead of the circulator, a quasi-circulator can be used which doesn't conduct any signal from the TX to the RX or vice versa as shown in Figure 2-3 (b).

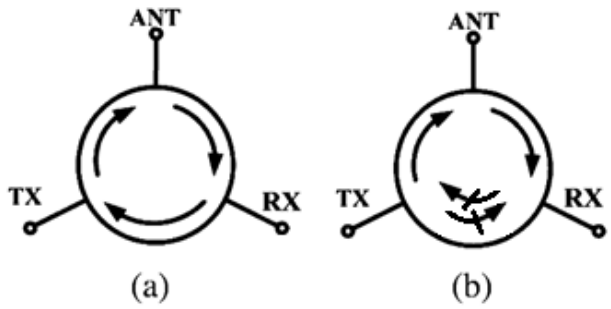


Figure 2-3 Antenna Interface with (a) Circulator and (b) Quasi-Circulator

Conventional circulators are implemented by using ferromagnetic materials which are bulky and costly. These circulators are working based on different phase shift for signals in different directions [10]. By integrating this method on the chip, very weak isolation was achieved [11] since the SI cancellation is a function of the dimension of the ferromagnetic material in the circulator.

In addition, the SI cancellation of the circulator is a function of the antenna impedance and environment around the antenna. Assuming an ideal circulator with infinite isolation, the SI cancellation in the antenna interface is equal to the antenna return loss. As mentioned before, not only the antenna impedance degrades the SI cancellation, but also the echoes from the environment descend the SI cancellation in the circulator. Therefore, an additional tuning circuit is necessary to compensate the errors in the antenna and environment. The goals in designing the integrated circulators or quasi-circulators for the full duplex TRX are small insertion loss in the path between TX and antenna, small noise figure in the antenna and RX path, high SI cancellation in the TX to RX path, high power tolerance in the TX to antenna path, and linearity in all the paths of the circulator.

Integrated circulator and quasi-circulator can be categorized in two subcategories: circulators based on time invariant circuit and circulators based on time variant circuits. In the following sections both categories will be discussed.

Circulator Based on Time Invariant Circuits

Time invariant integrated circulators are using the unilateral property of the transistors in the gate to drain path. A simple configuration is proposed in [12, 13] which provides more than 12 dB SI cancellation. This structure is using three transistors which provide a signal path in one direction and cancellation in the opposite direction. The disadvantage of this structure is the NF for the antenna to RX path. In addition, it doesn't have any tuning circuit to improve the SI cancellation in the circulator and compensates the antenna errors.

The divider/combiner quasi-circulator which is proposed in [14] divides TX signal in two paths. One part of the TX signal goes to the antenna and the other part goes to a dummy load. In this structure, LNA is a differential amplifier and the TX signal is a common-mode signal at its input. LNA should provide a good common-mode cancellation to cancel the TX signal at its inputs. The RX signal from the antenna goes to the LNA input as a differential-signal and is amplified by the LNA. The advantage of this structure is compensating the antenna errors by replacing the dummy load with a reconfigurable load. The disadvantage of this structure is the insertion loss between the TX and antenna which its minimum is 3 dB.

By employing a current reuse technique, a quasi-circulator is proposed in [15]. This technique provides SI cancellation better than 12 dB and insertion loss better than

7.9 dB. The advantage of this technique is the small power consumption, and its disadvantages are small SI cancellation and high insertion loss. In addition, this technique cannot compensate the antenna errors and it needs an additional antenna impedance tuner.

Circulator Based on Time Variant Circuits

The main goal of using time variant circuit is to design a non-reciprocal path. Indeed, the time variant circuit should respond differently to the signals in the opposite directions. This idea was proposed for the first time in [16, 17] which is based on non-reciprocal time varying resonators. The proposed circuit is shown in Figure 2-4. Figure 2-4 (a) shows one resonator with a constant inductor and two variable capacitors. Each capacitor is varying versus time by using a modulating signal. The modulating signals of the capacitors in one resonator have the same frequency and amplitude but 120° phase shift. This phase shift in the modulating signals causes the wave travelling from left to right to see a different transfer function than the wave travelling from right to left. By using this non-reciprocal response of the time varying resonator, a non-magnetic circulator is designed in [16, 17] which is shown in Figure 2-4 (b) and (c).

The advantage of this structure is no insertion loss and no NF in the signal path of the circulator for the ideal circuit. But the disadvantages of this structure are the small power handling which is about 0 dBm and the additional inter-modulated signals generated from the multiplication of the modulating signal and the input signal. In addition, this structure similar to all the circulators needs an additional antenna impedance tuner to compensate the antenna errors.

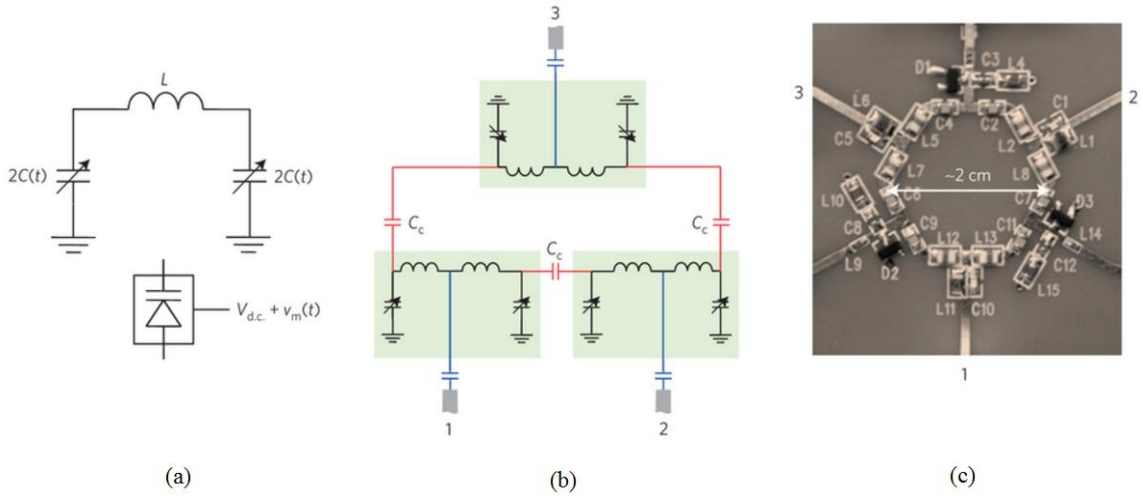
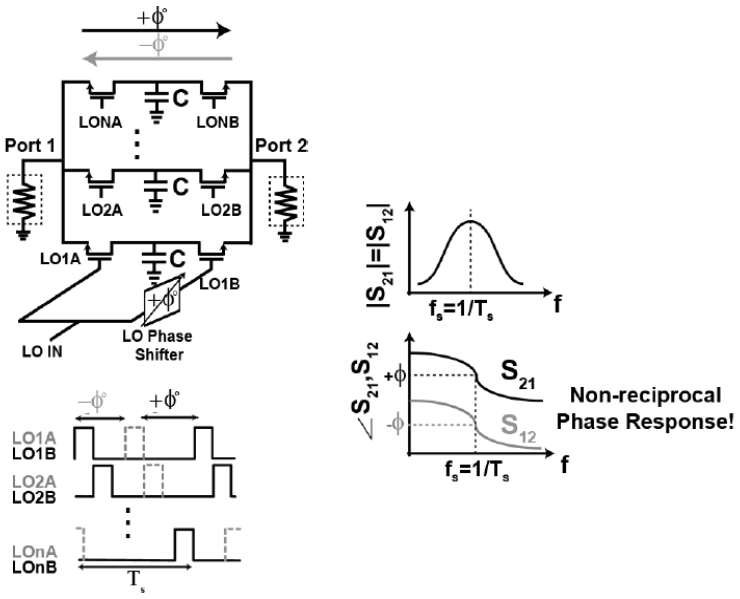
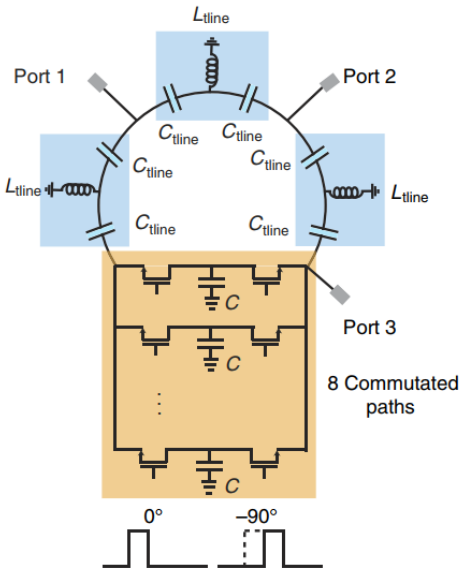


Figure 2-4 (a) Time Variant Non-Reciprocal Resonator [16], (b) Schematic of the Coupled Time Variant Non-Reciprocal Resonator to Implement the Circulator [16], and (c) the Manufactured Circulator on the Board.

An integrated time varying path based on N-path filter is proposed in [18] which its frequency response is non-reciprocal for the different signal directions. This non-reciprocal path provides the same amplitude response but 180° phase difference for the opposite directions in the signal paths. Figure 2-5 (a) shows this non-reciprocal path based on time varying circuit. The wave travelling from left to right is sampled at the baseband capacitors by the switches on the left side of the path and the signal travelling from right to left is sampled at the baseband capacitors by the switches on the right side of the path. As shown in this figure, different phase shifts can be achieved for different directions of the signals by controlling the time delay between the LO signals of the switches in this path.



(a)



(b)

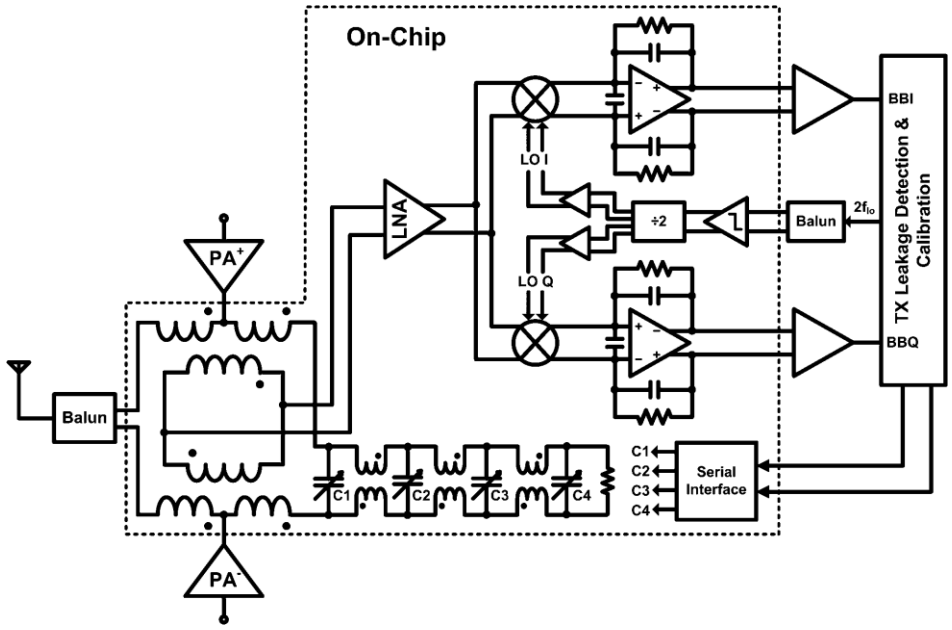
Figure 2-5 (a) Schematic of the Time Varying Non-Reciprocal Path and (b) the Proposed Circulator in [18].

This non-reciprocal path with 180° phase difference for different directions is used in an on-chip circuit to achieve an on-chip circulator which is shown in Figure 2-5 (b). The advantage of this structure is low insertion loss in its signal paths. The insertion

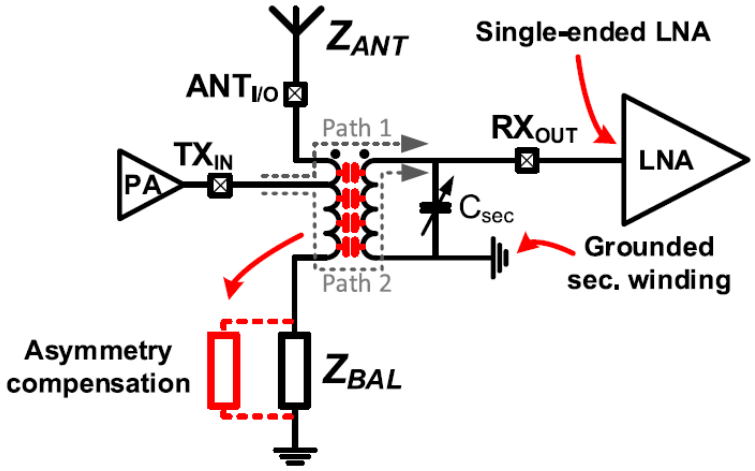
loss in this structure is a function of the order of the N-path filter and the on resistor of the switches of the N-path filter. Increasing the number of the paths and size of the switches reduces the insertion loss in this structure, but it makes the switching more difficult. The frequency of the switching should be N/2 times larger than the operation frequency. It means for an 8-path structure, the switching frequency should be 4 times larger than the operation frequency which limits the application of this structure to the sub-GHz applications. In addition, another disadvantage of this structure is the small power handling of this circulator. In [19], an RX with an integrated circulator is proposed with 8 dBm peak power handling and a tuner circuit to compensate the antenna errors. But, the antenna impedance tuner range is very small and it needs an additioanl fixed tuner off the chip.

2.3.3 Hybrid

A duplexer based on hybrid structure is proposed in [20] which provide more than 60 dB SI cancellation in a FDD wireless system. In this structure, two transformers and one reconfigurable impedance are used to implement a reconfigurable duplexer which can compensate the antenna impedance errors. Similar structure is proposed in [21] which works for 36 dBm peak power and is shown in Figure 2-6 (a). This structure cannot be used for full duplex TRX since there are two PAs in the structure which have uncorrelated noise signals. The uncorrelated noise signals cannot be cancelled by this hybrid structure. Figure 2-6 (b) shows the hybrid with 70 dBm IIP3 [22] which can be used for full duplex TRX. This hybrid also uses a reconfigurable impedance to compensate the antenna impedance errors.



(a)



(b)

Figure 2-6 (a) Proposed Hybrid Structure for FDD TRX [21], and (b) Proposed Hybrid Structure for FDD and Full Duplex TRX [22].

The main advantages of the hybrid structure in the full duplex TRX are the high-power TX signal and antenna errors compensation. The typical value for the leakage

cancellation in the hybrid is 50 dB without using additional off the chip antenna impedance tuner. The disadvantage in the hybrid structures is the tradeoff between the minimum NF in the antenna to RX path and the minimum insertion loss in the TX to antenna path [23]. Ideally, the NF and insertion loss are 3 dB.

2.4 Leakage Cancellation

The SI cancellation in the antenna interface is not enough for a full duplex TRX and additional analog SI cancellation is necessary to relax the RX. As mentioned before, the analog SI cancellation can be implemented at the RF before or after the LNA or at the baseband. In this section, different techniques for analog SI cancellation which have been proposed in the state of the art literature are discussed.

2.4.1 RF Leakage Cancellation

To cancel the SI signal at RF, the transmitted signal should be sampled from one point at the TX and get modified to generate the proper cancellation signal. The cancellation signal can be injected before or after the LNA. The tradeoff between injecting the cancellation signal before or after the LNA is between the RX NF and the LNA linearity. Injecting the cancellation signal before the LNA requires very small noise power in the cancellation circuit to not degrade the RX NF. And, injecting the cancellation signal after the LNA requires very good linearity from the LNA to not generate large distortion signals due to the high power SI signal at the LNA input.

In [24], an RF cancellation technique has been proposed which samples the transmitted signal after the PA and modifies the amplitude and phase of the sampled

signal, and finally, injects it before the LNA. The variable phase shifter and attenuator and the injection point at the RX are implemented by using a passive structure which is shown in Figure 2-7. In this structure, the cancellation circuit doesn't have any active elements; consequently, the proposed cancellation technique doesn't degrade the RX NF and has a very good linearity. The disadvantage of this structure is the high insertion loss of the RF SI cancellation path which limits the maximum power of the leakage signal for proper SI cancellation. It means that the SI cancellation in the antenna interface should be large enough; otherwise, this structure cannot cancel the SI signal. In addition, just using a phase shifter and attenuator provides a proper cancellation signal for one frequency in the operation bandwidth which results in a narrow bandwidth SI cancellation.

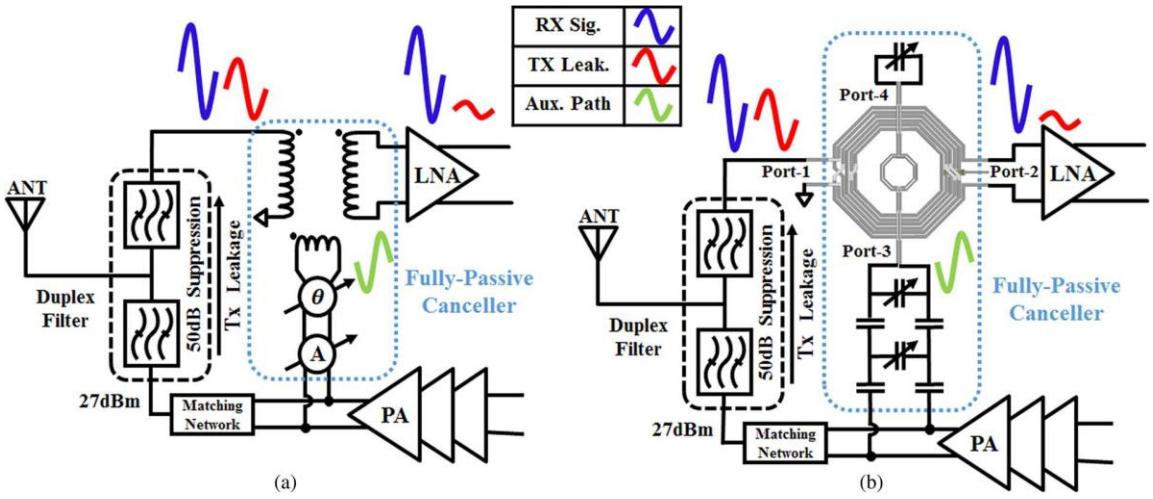


Figure 2-7 (a) Block Diagram and the Signals in the Proposed RF Cancellation in [24] and (b) Schematic of the Proposed Passive RF Canceller in [24].

To increase the bandwidth of the SI cancellation in the full duplex TRX, the RF cancellation circuit should mimic the frequency response of the channel between the TX and the RX. It means that the SI cancellation circuit should provide proper variation in

amplitude and phase of the cancellation signal versus frequency to provide SI cancellation in the operation bandwidth.

To achieve wideband SI cancellation in [25], the operation bandwidth is divided into the smaller sub-channels and for each sub-channel a variable gain and phase shifter is used to change the amplitude and phase of each sub-channel separately. This structure is shown in Figure 2-8. The challenge of this approach is the required narrow band high-Q filters at RF. The insertion loss and the mechanical size of the high-Q filters at RF are very large and they are not integrable on a chip. To solve this problem, N-path filters are used which their operation frequency and bandwidth can be controlled by the LO frequency and the baseband circuit. The phase shifter and attenuator of each path are absorbed in the circuit of N-path filter.

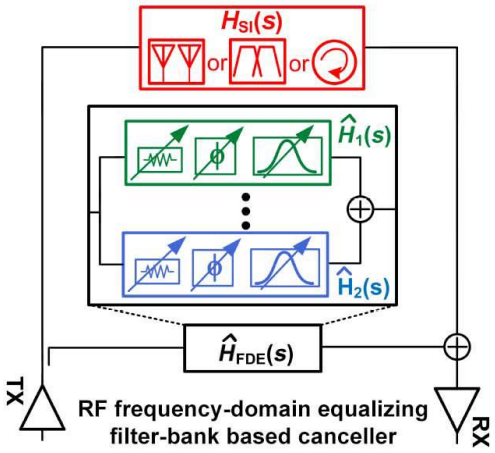


Figure 2-8 Proposed Wideband RF Cancellation in [25] Based on Sub-Channelizing the RF Cancellation Path.

The advantage of this structure is the bandwidth of the SI cancellation which is the function of the number of the sub-channels in the cancellation path; therefore, the

bandwidth of the SI cancellation can be increased by increasing the number of the sub-channels in the cancellation path. The disadvantages of this structure are the large insertion loss of the cancellation path which put a limitation on the minimum SI cancellation in the antenna interface and nonlinear response of the cancellation path which can generate the intermodulation signals.

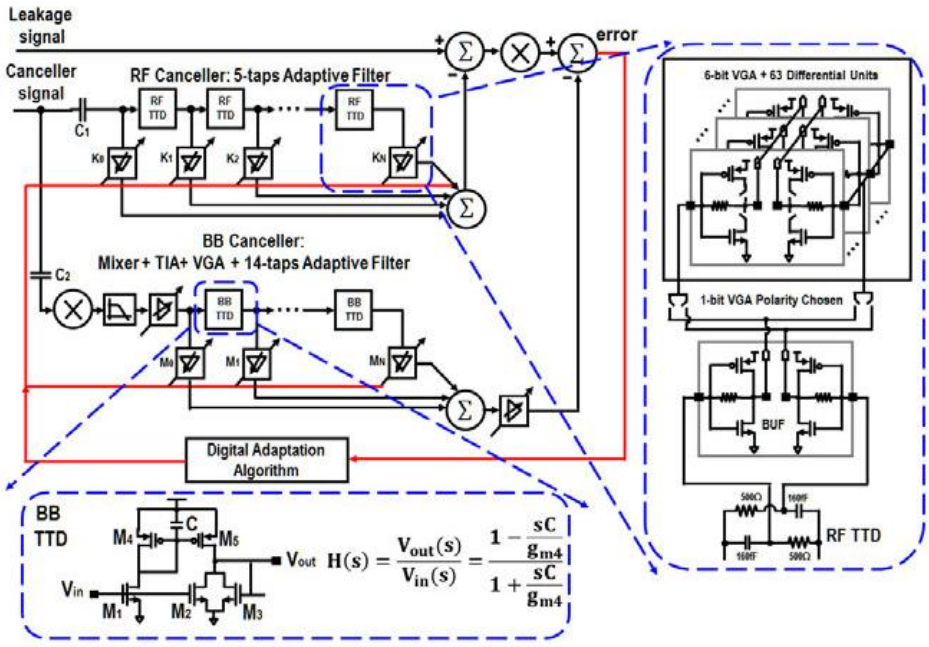


Figure 2-9 Adaptive Wideband RF and Baseband Cancellation Based on Filter Equivalent to FIR Filter by Using True Time Delay Lines [26].

Another method to provide RF SI cancellation in the full duplex TRX is using an analog filter equivalent to Finite Impulse Response (FIR) filter at the RF [26]. The true time delay by using a resistor and capacitor are implemented and the delayed signals are added with the different weights in current mode. The variable weights are implemented by using Gm-stage units which are switched in or out of the circuit. The advantage of this structure is that the bandwidth of the SI cancellation can be increased by increasing the order of the FIR filter and also using all the well-known adaptive techniques to find the

optimum weights of the FIR filter. The disadvantage of this structure is that increasing the order of the FIR filter degrades the NF of the RX. Figure 2-9 shows the proposed RF SI cancellation in [26].

2.4.2 Baseband Leakage Cancellation

The last step of the analog SI cancellation in the full duplex TRX is the baseband. Similar to the RF SI cancellation, a sample of the transmitted signal is needed to create the cancellation signal. If the cancellation signal is sampled after the PA, additional down-converter is needed for the baseband SI cancellation; otherwise, the transmitted signal can be sampled at the TX baseband and there is no need to the down-converter. The baseband cancellation signal can be designed based on time domain model of the channel between TX and RX by using true time delay lines or it can be designed based on the frequency domain model of the channel between the TX and RX by using phase shifter and equalizer filters.

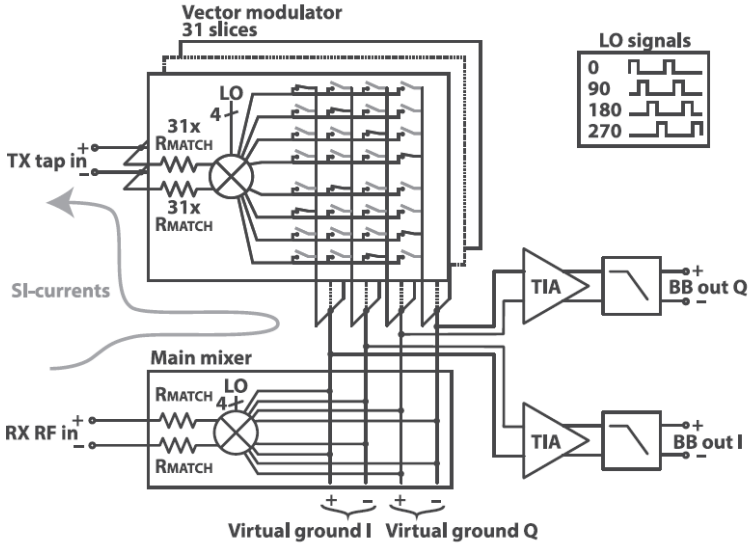


Figure 2-10 Baseband SI Cancellation Based on Vector Modulation Which Is Proposed in [27].

In [27], TX signal is sampled after the PA, its phase and amplitude is modified by vector modulator down-converter, and finally it is injected into the RX baseband to cancel the SI signal. This vector modulator is based on a N-path down-converter mixer which can control the amplitude and phase of the baseband signal by turning on and off the baseband switches. This structure is shown in Figure 2-10. Since this method cannot mimic the response of the channel between the TX and RX, the bandwidth of the SI cancellation is small.

To increase the bandwidth of the SI cancellation, analog filter equivalent to FIR filter based on true time delay is proposed in [26]. The proposed circuit is also shown in Figure 2-11. The true time delay is built by the resistor and capacitor. This technique mimics the channel response between the TX and RX in time domain to provide wideband SI cancellation in time domain. As mentioned before, the similar technique at RF degrades the NF of the RX path, but the NF in the RX path is not degraded since the baseband SI cancellation injects the signal after the LNA. Consequently, by increasing the order of the FIR filter the cancellation bandwidth can be increased easily.

2.4.3 Digital SI Cancellation

The last step of the SI cancellation in the full duplex TRX is in digital domain. Not only the digital canceller should cancel the SI signal, but also it should cancel the distortion of the SI signal due to the nonlinear response of the RX and the analog SI canceller. Increasing the bandwidth, the SI signal power, and the distortion signal power make the digital cancellation more complicated. On the other hand, if the digital canceller provides more cancellation for the higher power of the SI signal or the distortion signal,

the analog hardware would be simpler. Consequently, there is a tradeoff between analog and digital circuit complexity.

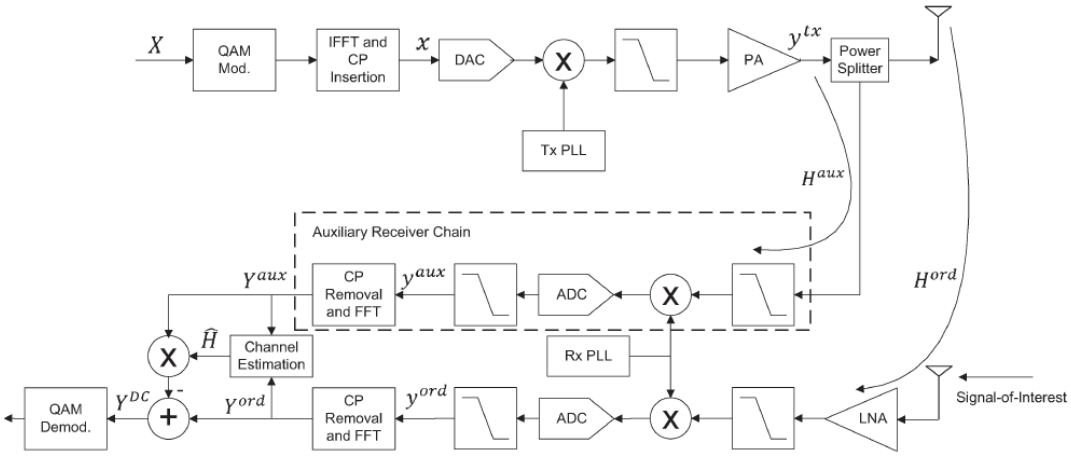


Figure 2-11 Proposed Digital SI Cancellation in [28] Which Is in Frequency Domain.

In [28], a digital SI cancellation for full duplex TRX in frequency domain is proposed. The transmitted signal is sampled after the PA and down-converted and digitized with an auxiliary path. Both the TX sampled signal and the RX signal are transformed from the time domain to the frequency domain. The channel frequency response and the non-linear response of the RX are estimated by comparing the sampled TX signal and the RX signal. Finally, the cancellation signal is generated by using the estimated channel response and the nonlinear model of the RX. This structure is shown in Figure 2-11. In this method, three scenarios for the passive cancellation (25 dB, 45 dB, and 60 dB) have been assumed and the RX noise floor is −90 dBm. Assuming that the RX noise floor degradation is only 3 dB due to the SI signal, the maximum TX power for each scenario is −5 dBm, 10 dBm, and 20 dBm, respectively. Consequently, the digital SI cancellation is 50 dB and the analog passive SI cancellation is 60 dB for the scenario with 20 dBm transmitted signal.

The digital cancellation which is proposed in [29] is based on Volterra series. This digital SI cancellation is shown in Figure 2-12. In this method, the transmitted signal is sampled before the DAC in the TX and is delayed by using N delay units. After each delay unit, the signal is tapped and passes through a polynomial with the order of p. The weights in this polynomial are the unknown parameters for the digital SI cancellation. Finally, the output signal of all the polynomials are added together to generate the digital SI cancellation signal. The output signal versus the input signal is shown in the following equation.

$$y[n] = \sum_{k=0}^{N} h_1[k]x[n-k] + \sum_{k=0}^{N} h_2[k]x^2[n-k] + ... + \sum_{k=0}^{N} h_p[k]x^p[n-k] \qquad (1)$$

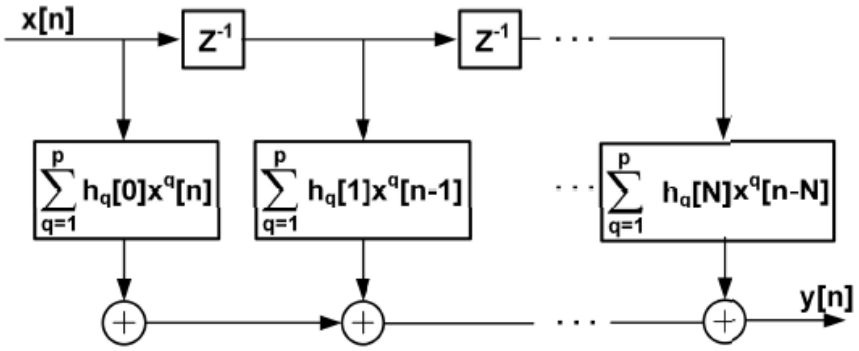


Figure 2-12 Digital SI Cancellation in Time Domain Which Is Proposed in [29].

The number of the parameters which should be set for this method is $N \times p$. In [29], to achieve more than 40 dB SI cancellation and distortion cancellation in digital domain, the nonlinear order terms is considered as 4 (p=4) and the length of the delayed signal is considered 41 (N=41). It means that the total number of the unknown parameters

in the proposed digital SI cancellation in [29] is 164 which have to be found adaptively when the full duplex TRX is working.

CHAPTER 3

INTEGRATED QUASI-CIRCULATOR

3.1 Introduction

Conventional three port circulators are based on the Faraday Effect and use strongly biased magnetic materials that respond differently to waves propagating in opposite directions. Use of specialized materials and bulky discrete components prohibit the application of these circulators for system-on-chip applications. Integrated CMOS circulators offer smaller size, minimal external components, and allow integration with the RF and baseband modules. Integrated monolithic circulators can improve the performance of a wide range of applications such as integrated RADAR [30, 31, 32], automobile collision avoidance systems [33, 34], full duplex Simultaneous Transmit and Receive (STAR) TRXs [7, 35], and optical TRXs [36, 37]. RF circulators can also be used to eliminate front end RF filters such as Bulk Acoustic Wave (BAW) filters and block the TX signal leakage [38, 39].

First active BJT circulator was presented in 1965 [12], followed by a GaAs FET implementation [40]. A CMOS circulator at 2.4 GHz was presented in [41], but only had 10 dB of isolation. The active quasi-circulators are proposed in recent years [14, 42, 43, 44, 45, 46, 47, 15], however, the performance in each port is highly variable. In [16, 17], a time varying resonator is proposed. An N-path filter using non-reciprocal path, achieving insertion loss less than 1.8 dB is presented in [48, 18, 29, 19]. Methods presented in [16, 17, 48, 18, 29, 19] are based on time varying circuits, and have minimal Insertion Loss (IL) and NF. Time invariant circuits using the non-reciprocity property of the transistors [49] or loss mechanism of a passive circuit [50, 21], are presented to

provide isolation between the TX and RX. However as mentioned in [29, 19], to compensate for the antenna return loss and circuit mismatch, an antenna impedance tuner is needed between the circulator and the antenna. In [19], a balance network and fixed antenna impedance tuner is proposed to compensate the antenna impedance errors. In [21], a reconfigurable duplexer based on loss mechanism is proposed which compensates the antenna Return Loss (RL) and circuit mismatch to improve the isolation between TX and RX without using an additional antenna tuner.

Limitations of the integrated CMOS circulators and quasi-circulators are insertion loss, return loss, noise figure, leakage between TX and RX, maximum transmit power, and limited isolation bandwidth. In the TRX, the circulator noise and the TX PA noise floor can impact the RX noise figure and dynamic range. Limited linearity and non-linear products of the transmitted signal further degrade the RX performance. In addition, antenna impedance mismatch limits the isolation between TX and RX, and an antenna impedance tuner is necessary to improve the leakage cancellation in the circulator. To improve the leakage cancellation after the circulator, an additional leakage cancellation block [51, 25, 27] can be added to the circulator [52].

In this section, an on-chip reconfigurable quasi-circulator operating at 2.4 GHz and implemented in 130 nm CMOS technology is presented. At differential LNA input of the proposed architecture, transmit PA output signal is a common-mode signal and the received signal is a differential-mode signal. The PA output signal leakage (echo) in the RX is cancelled in two steps. First, a reconfigurable impedance matching circuit is used to compensate the antenna impedance mismatch, and reduce the leakage of PA output signal at LNA input. Second, a reconfigurable block adds PA output signal at the LNA

output after tuning amplitude and phase of the PA output signal to further cancel the residual leakage. The rest of the paper is organized as follows. Section 3.2 describes the proposed reconfigurable quasi-circulator architecture, full-duplex link budget, and the analysis of PA output power leakage in RX. Section 3.3 discusses the transistor level implementation. Section 3.4 presents the measurement results for the test chip implemented.

3.2 System Architecture

3.2.1 Architecture

Figure 3-1 shows the block diagram of the proposed on-chip quasi-circulator. The proposed topology consists of a power divider, an LNA, reconfigurable impedance Z_V, an output SI cancellation, and an output buffer.

The transmit signal $s(f)$ is fed to divider Z_1 and Z_2, to the antenna as $s_1(f)$, to the

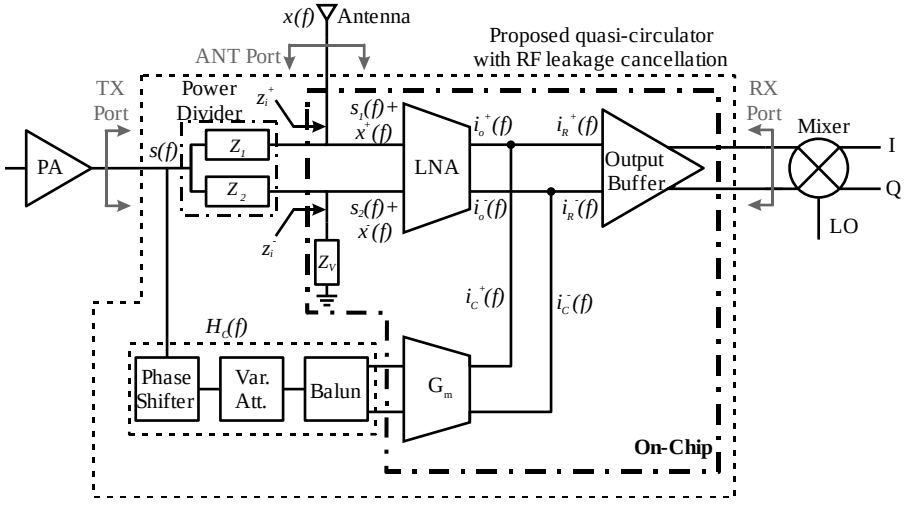


Figure 3-1 Proposed On-Chip Reconfigurable Quasi-Circulator.

reconfigurable load as $s_2(f)$, and to the LNA as a common mode signal $s_{cm}(f)=\frac{s_1(f)+s_2(f)}{2}$. Any mismatch from the transmit signal path to the LNA will generate a differential-mode error signal $s_e(f)=s_1(f)-s_2(f)$. The reconfigurable impedance block Z_V is a common-source active circuit with inductive source degeneration to compensate for any mismatches in the signal path to the LNA inputs.

The LNA is a common-source differential gain stage with LC resonant load tuning. The received signal, $x(f)$, goes directly from the antenna to the LNA as $x^+(f)$, and after 180° phase-shift via the divider blocks as $x^-(f)$ where the LNA differential input signals is defined as $x_d(f)=x^+(f)-x^-(f)$. The LNA differential output signal $i_o(f)$ consists of the amplified desired received signal $g_{md}\ x_d(f)$ and the residual leakage of the transmit signal $i_{res}(f)$ which is minimized by the cancellation circuit. The cancelation circuit $H_C(f)$ and a transconductance gain stage (G_m) generate the correction signal $i_C(f)$ by sampling and changing the phase and amplitude of the transmitted signal. The correction signal $i_C(f)$ is injected to the LNA output to cancel any residual leakage at the LNA output, $i_{res}(f)$, where ideally $i_{res}(f) \approx i_C(f)$. The final output after the correction is $i_{RX}(f) = i_o(f)-i_C(f)$. This is followed by the output buffer conducting the $i_R(f)$ to the output load and it is matched to 100 Ω.

3.2.2 Full Duplex Link-Budget

The circulator performance can be measured by the isolation between the TX input and RX output. The metric used is the *Self-interference Cancelation Ratio (SIC)* which is the ratio of the transmit signal power P_{TX} to the leakage power at the circulator RX port P_{leak} expressed in decibels as $SIC= P_{TX} - P_{leak}$.

If the RX maximum allowable signal power is P_{max}, with noise floor P_{noise} (without distortion), and dynamic range margin M, the RX dynamic range would be $DR_{Rx}= P_{max} - P_{noise} + M$ where $P_{noise}=-174$ dBm/Hz$+10\log_{10}(BW)+NF$. The leakage power at the circulator output has to be smaller than the RX maximum allowable signal power P_{max}. By assuming that the leakage signal at the circulator output has the highest signal power in the RX, the RX dynamic range would be $DR_{Rx}= P_{leak} - P_{noise}+M$.

The required *SIC* in the quasi-circulator can be calculated as follows:

$$TLCR = P_{TX} - DR_{RX} - P_{noise} + M \tag{3-1}$$

where DR_{RX} is the RX dynamic range and P_{TX} is the transmit signal power. In addition, the distortion signals at the circulator output have to be within the RX dynamic range DR_{RX}. Given this, the third order intercept-point between the circulator TX port and receive port, defined by $IIP3_{TX\text{-}RX}$ is calculated as follows,

$$IIP3_{TX-RX} = \frac{3}{2}P_{TX} - \frac{1}{2}\left(P_{noise} + DR_{RX} + TLCR - M\right) \tag{3-2}$$

For example, for a short-range wireless communication system, if the RX bandwidth BW is 40 MHz with RX noise figure NF=5 dB, TX power P_{TX}=0 dBm, dynamic range margin M=5 dB and required DR_{Rx}=50 dB with noise floor at $P_{noise} = -93$ dBm, the required *SIC* achieves approximately 50 dB of rejection by the circulator and $IIP3_{TX\text{-}RX}$ would be −1 dBm. A cancelation of 50 dB can also be accomplished by the

impedance matching at the LNA input port by 25 dB and the leakage cancellation after LNA by 25 dB. Besides, the LNA input port and reconfigurable impedance block Z_v are the main sources of the distortion in the quasi-circulator [31]. This puts a stringent requirement at the LNA input and reconfigurable impedance Z_v to achieve $IIP3_{TX\text{-}RX}$ of more than −1 dBm. Table 3-1 summarizes the design targets for the quasi-circulator for a short-range full-duplex wireless system.

Figure 3-2 shows the quasi-circulator with the divider block, antenna port impedance, reconfigurable port Z_v, and the LNA. The LNA output $i_o(f)$ contains the desired signal $g_{md}\, x_d(f)$ and the residue of the transmit signal $i_{res}(f)$:

Table 3-1 Summary of the Design Targets for the Quasi-Circulator.

		Goals
Receiver Specification	Operation Frequency	2.4 GHz
	Signal Bandwidth	40 MHz
	NF	5 dB
	Noise Floor	−93 dBm
	Dynamic Range	50 dB
TX Specification	Operation Frequency	2.4 GHz
	Signal Bandwidth	40 MHz
	Transmit Power	0 dBm
Transmit Leakage Cancellation	Leakage Power	−50 dBm
	Total SIC	50 dB
	$IIP3_{TX\text{-}RX}$	−1 dBm

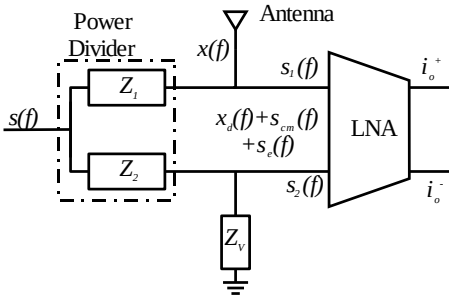


Figure 3-2 Transmit and Receive Signals at the LNA.

$$i_o(f) = g_{md}\, x_d(f) + i_{res}(f) \tag{3-3a}$$

$$i_{res}(f) = g_{md}\, s_e(f) + g_{mc}\, s_{cm}(f) \tag{3-3b}$$

where g_{md} and g_{mc} are the differential-mode and common-mode transconductance of the LNA. The overall transfer function of the residual current $i_{res}(f)$ at the output of the LNA to the transmit signal at the output of the PA $s(f)$ is:

$$\frac{i_{res}(f)}{s(f)} = g_{md} T(f) + \frac{z_i^+}{Z_{01}}\, g_{mc} \angle(-90°) = A_0(f) \angle \varphi_0(f) \tag{3-4}$$

where, $T(f)=s_e(f)/s(f)$ is the transfer function of the mismatch in the transmit signal path, z_i^+ is the impedance at the antenna port and Z_{01} is the characteristic impedance of the transmission line in Z_1 block, and $A_0(f)$ and $\varphi_0(f)$ are the magnitude and phase of $i_{res}(f)/s(f)$. The main objective of this architecture is to minimize the residual current $i_{res}(f)$ at the LNA output which depends on the mismatch error in the divider, LNA input, antenna impedance, and the reconfigurable impedance Z_v. To reduce the residual current $i_{res}(f)$, the common-mode transconductance g_{mc} and the error signal $s_e(f)$ have to be

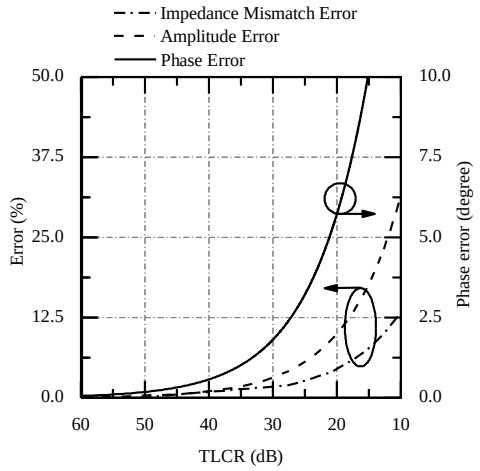


Figure 3-3 SIC in dB vs. Normalized Impedance Mismatch Error $|(z_i^+ - z_i^-)/z_i^+|$ at LNA Input, and Amplitude and Phase Error at Leakage Cancellation.

minimized. The transfer function ratio of $T(f)=s_e(f)/s(f)$ is calculated by using *ABCD* matrix of the transmission line [10] as,

$$\frac{s_e(f)}{s(f)} = T(f) = \frac{z_i^+}{z_i^+ \cos\theta_1(f) + jZ_{01}\sin\theta_1(f)} - \frac{z_i^-}{z_i^- \cos\theta_2(f) + jZ_{02}\sin\theta_2(f)} \tag{3-5}$$

where, $\theta_i(f)$ and Z_{0i} ($i=1,2$) are electrical length and characteristic impedance of divider and z_i^+ and z_i^- are the impedances at the antenna port and impedance block Z_v. Figure 3-3 shows the *SIC* vs. the normalized impedance error $|(z_i^+ - z_i^-)/z_i^+|$ at the LNA input. For the example above, the goal is to achieve a SIC more than 25 dB at the LNA input. In this case, normalized impedance error should be less than 3%.

The correction signal $i_C(f)$ is injected at the LNA output to minimize the transmit signal leakage $i_{leak}(f)=i_{res}(f)-i_C(f)$. By assuming that gain error and phase error in radian between residual of transmit signal $i_{res}(f)$ and the correction signal $i_C(f)$ are ΔA and $\Delta\varphi$, respectively, the transmit signal leakage is $i_{leak}(f)=A_0(f)\angle\varphi_0(f)-(A_0(f)+\Delta A)\angle(\varphi_0(f)+\Delta\varphi)$.

By using Taylor series and assuming small amplitude and phase errors, the amplitude of the leakage current $i_{leak}(f)$ vs. the residual current $i_{res}(f)$ can be modeled as,

$$\left|\frac{i_{leak}(f)}{i_{res}(f)}\right| \cong \left(\Delta\varphi^2 + \left(\frac{\Delta A}{A_0}\right)^2\right)^{1/2} \tag{3-6}$$

Figure 3-3 also shows the leakage cancellation block amplitude ΔA and phase errors $\Delta\varphi$ vs. the *SIC* after the leakage cancellation. To achieve more than 25 dB of rejection, the phase and amplitude errors at the leakage cancellation block should be: ΔA <4 % and $\Delta\varphi$ <2°. The SIC in the proposed quasi-circulator can be expressed as:

$$TLCR = 20\log_{10}\left(\frac{Z_{01}}{z_i^+ g_{md}}\left(\Delta A^2 + |A_0(f)|^2 \Delta\varphi^2\right)^{1/2}\right) \tag{3-7}$$

In addition to SIC, insertion loss between PA and antenna is important in the quasi-circulator. Assuming an ideal power divider, the transmitted signal power is divided between the antenna and the reconfigurable impedance. Therefore, the minimum insertion loss between TX and antenna in the proposed architecture is 3 dB. The transmit signal at the antenna is $s(f)\frac{z_i^+}{z_{01}}\angle(-90^\circ)$.

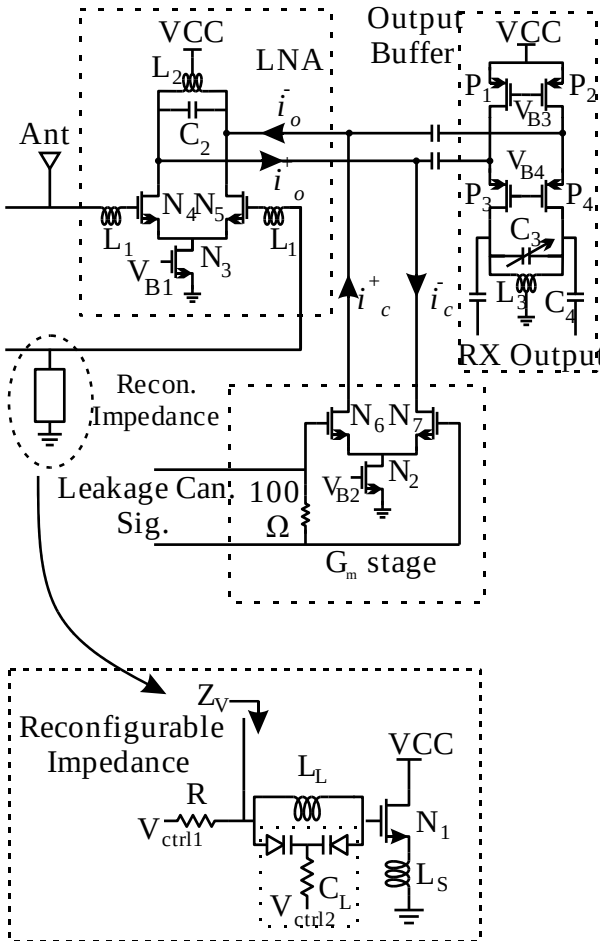


Figure 3-4 Schematic of LNA, Leakage Cancellation G_m-Stage, Output Buffer, and Active Reconfigurable Impedance Block.

3.3 Circuit Implementation

The active CMOS quasi-circulator is fabricated in IBM 130 nm CMOS technology.

3.3.1 Low-Noise Amplifier (LNA)

The LNA is a common-source differential amplifier with LC resonant load tuned at 2.4 GHz, as shown in Figure 3-4. The goal in designing the LNA is reducing the noise

figure *NF* below 5 dB, reducing the common-mode transconductance g_{mc} by 25 dB less than the differential-mode transconductance g_{md}, and large common-mode voltage range at LNA input to tolerate the high power transmit signal without generating distortions.

Gate inductor L_1 is used for improving the equivalent transconductance of the LNA and impedance matching. The output has a resonance LC tank to provide resonance at 2.4 GHz, DC biasing and high impedance at the operating frequency. The proper biasing of the differential amplifier maximizes the common-mode voltage range at the LNA input which is necessary to improve the linearity of the LNA in presence of TX signal. In this design, the common-mode voltage range at LNA input is 2.5 Volts which is enough for 18 dBm TX signal power. To reduce the common-mode transconductance g_{mc}, all the well-known layout techniques have been used.

3.3.2 Reconfigurable Impedance Block Z_V

The reconfigurable impedance block is a common-source NMOS transistor with inductive source degeneration as shown in Figure 3-4. This block provides a variable impedance matching to compensate for the antenna impedance errors and improve the SIC. The proposed active impedance matching block generates less noise compared to the passive impedance [14, 53]. The input impedance (Z_V) of the reconfigurable impedance block is:

$$Z_V = \frac{g_{mL}}{C_{gsL}} L_s + j\left(\frac{L_L \omega}{1 - L_L C_L \omega^2} - \frac{1}{C_{gsL}\omega} + \omega L_s \right) \qquad (3\text{-}8)$$

where, g_{mL} is the transconductance of transistor N_1, C_{gsL} is the gate-to-source capacitance of N_1, L_L is the inductance at the gate of N_1, L_S is the source degeneration inductance of N_1, and C_L is the variable capacitance of a varactor diode placed at the gate of N_1. The input impedance of this circuit is controlled by a DC bias voltage V_{ctrl} which controls g_{mL}, and by the variable capacitor C_L. The reconfigurable impedance is tuned for 50 Ω at 2.4 GHz with return loss lower than 13 dB and transmit signal distortion below −50 dBm for 0 dBm transmit signal power.

3.3.3 LNA Output-Leakage Cancellation Path

The LNA output leakage cancellation path consists of a gain and a phase adjustment block $H_C(f)$ followed by a transconductance amplifier (G_m). The goals of this reconfigurable block is to cancel any residual transmit signal at the output of the LNA. This is accomplished by generating the cancelation current $i_C(f)$ by the phase and amplitude adjustment of the transmit signal. As discussed in the previous section, the required amplitude resolution is 0.25 dB with the phase resolution of 2°.

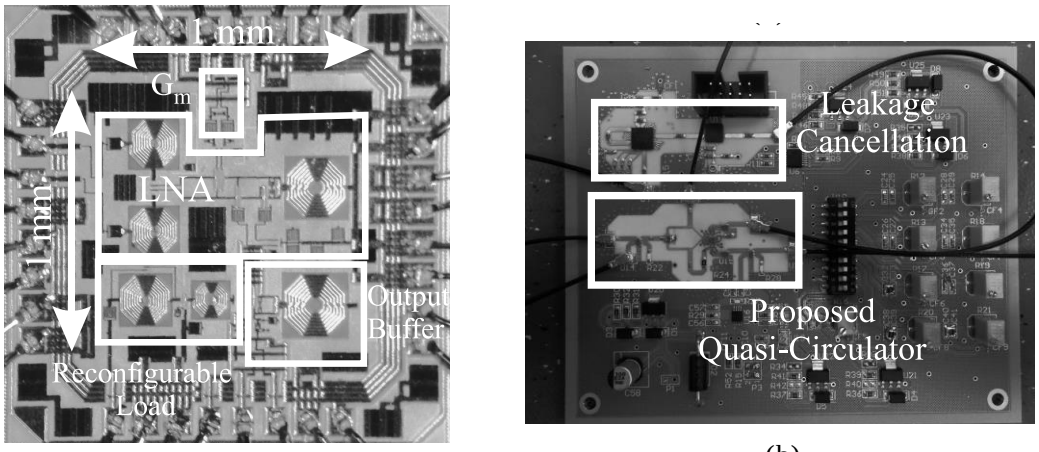
3.3.4 Output Buffer

The goal in the output buffer provides low impedance at its input and impedance matching at its output. The Output buffer is a differential common-gate amplifier with LC resonant load tuned at 2.4 GHz, as shown in Figure 3-4. The buffer provides low input impedance, and its output is matched to 100 Ω. P_3 and P_4 are common-gate input transistors, and transistors P_1 and P_2 form current sources. The LC tank consisting of a

symmetric inductor L_3 in parallel with a variable capacitor C_3, and series capacitors C_4 form output matching network.

3.3.5 Power Divider

An on-board power divider using transmission lines has been designed. The characteristic impedance and electrical length of the transmission lines are 70.7 Ω and 90°, respectively. Compared to an on-chip power divider, the on-board power divider has lower loss at 2.4 GHz due to low loss on-board transmission lines.



(a) (b)

Figure 3-5 (a) Die Micrograph and (b) Board Photograph.

3.4 Measurement and Simulation Results

The three port active CMOS circulator was fabricated using the IBM 130 nm process. The overall chip area is 1x1 mm^2 as shown in Figure 3-5. The key parameters of the three port quasi-circulator include forward path gain, SIC, impedance matching, linearity, and noise.

3.4.1 ANT-RX Path

The desired ANT-RX parameters are: gain>10 dB, RL>10 dB, and NF<5 dB in the frequency range of 2.3-2.5 GHz with BW=200MHZ which are shown in Figure 3-6. The measured gain is greater than 10 dB, and the RL is better than 10 dB. The ANT-RX gain as a function of the received signal power is shown in Figure 3-6 (b). The measured P1dB in the antenna to RX path is −9 dBm. The RX gain reduces by 0.35 dB in the presence of the 0 dBm transmitted signal.

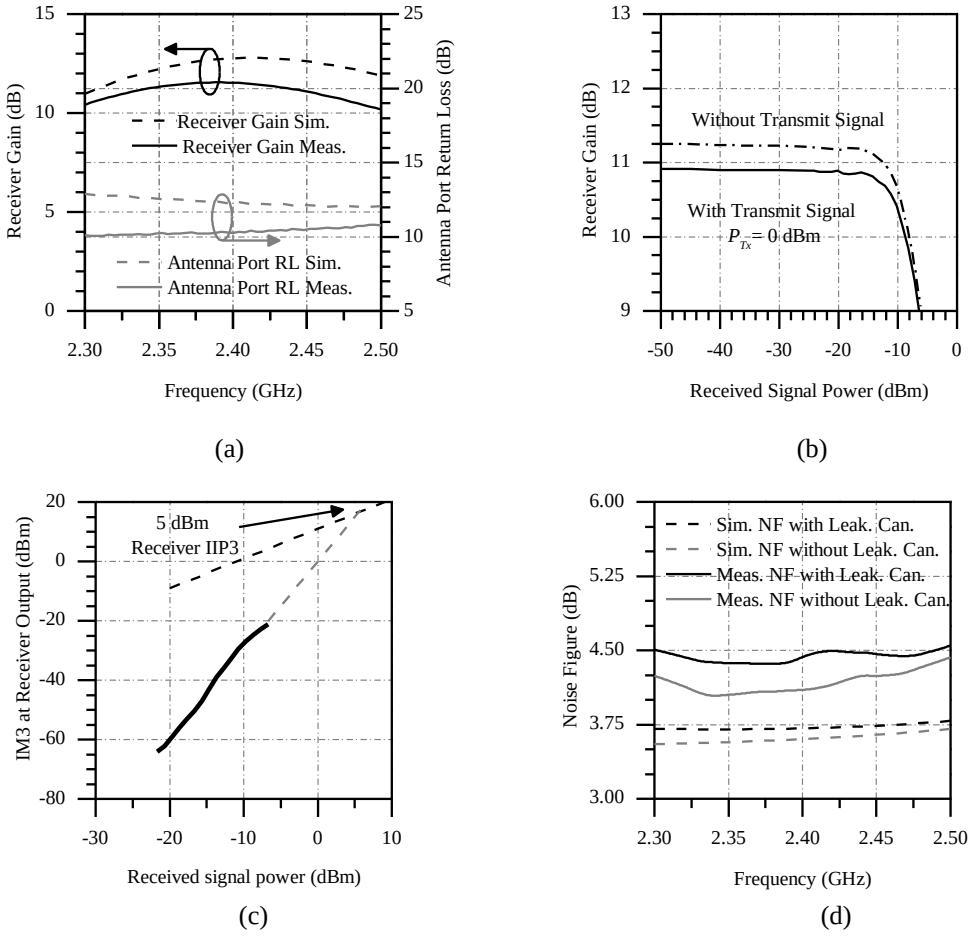
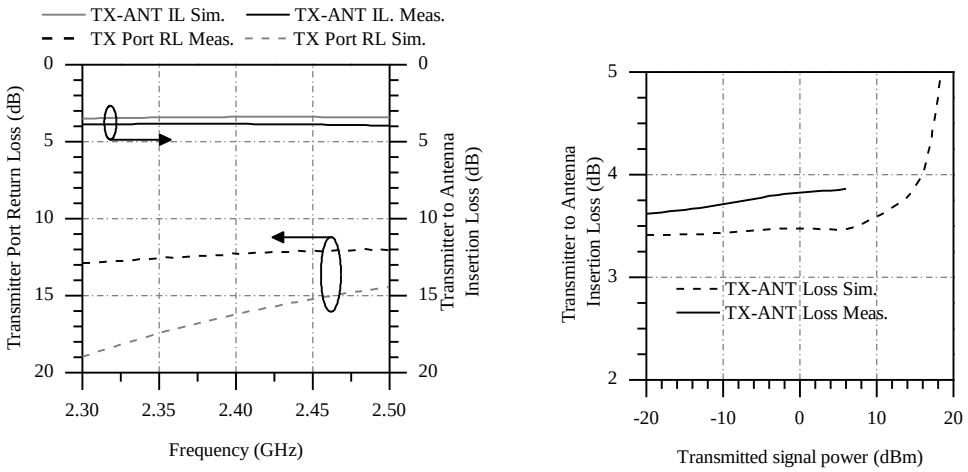


Figure 3-6 ANT-RX Path Measured and Simulated Results (a) Gain and Return Loss (RL), (b) Gain vs. Received Signal Power With and Without Transmitted Signal, (c) IM3 and IIP3, and (d) NF With and Without Leakage Cancellation.

The measured third-order inter-modulation distortion (IM3) for different powers of received signal is shown in Figure 3-6 (c) and the IIP3 is equal to 5 dBm. As shown in Figure 3-6 (d), the measured value of ANT-RX NF is below 4.5 dB. The output leakage cancelation adds about 0.25 dB of NF to the ANT-RX port.

3.4.2 TX-ANT path

The desired TX-ANT path parameters are impedance matching at the TX port with the RL better than 10 dB, and the insertion loss IL less than 4 dB (ideally 3 dB). The measured TX-ANT port parameters are RL >12 dB and IL< 3.8 dB as shown in Figure 3-7 (a). Figure 3-7 (b) shows the variation of measured IL of TX-ANT path as a function of the TX power P_{TX}. The figure shows 0.2 dB variation of IL when P_{TX} is increased up to 6 dBm. The P1dB between TX and antenna ports cannot be measured because the large TX power can cause damage at quasi-circulator but the simulation results show the P1dB in the TX-Ant path is 18 dBm.



(a) (b)

Figure 3-7 TX-ANT Path Measured and Simulated (a) IL and RL at TX Port, and (b) Insertion Loss vs. TX Power P_{TX}.

3.4.3 TX-RX Path

The goal is to provide at least 50 dB of isolation for the transmit signal echoing back in the RX path with IIP3=0 dBm. Figure 3-8 shows the SIC as a function of the antenna impedance matching for Z_A=30, 50, and 80Ω. Without the reconfigurable impedance matching for Z_A=30 and 80 Ω, the SIC is 0 dB. The SIC is above 30dB with the tuned reconfigurable impedance Z_V. The reconfigurable impedance Z_V compensates the antenna impedance errors and improved the SIC to over 30dB with RL>13 dB.

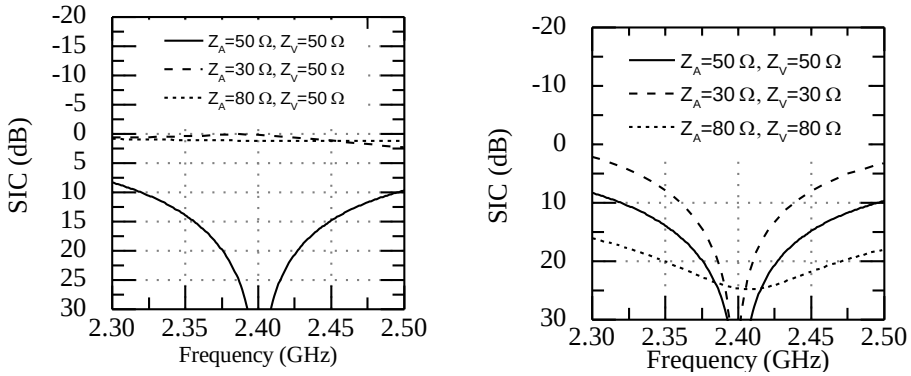


Figure 3-8 SIC for: (a) Different Z_A and 50 Ω Z_V (b) Different Z_A, With Tuned Z_V for the Best SIC.

The overall measured SIC in the RX path including the output leakage cancelation block is shown in Figure 3-9 (a). The solid line shows the SIC with the tuned reconfigurable impedance block and leakage cancellation block. For a single tone transmitted signal at 2.4 GHz with 0 dBm power, the SIC is 90 dB.

The measured third-order inter-modulation distortion (IM3) for different TX signal power is shown in Figure 3-9 (b) with all the signals referred to the antenna port. The measured TX-RX IIP3 is 0 dBm. The measured SIC of the quasi-circulator vs.

transmitted signal power P_{TX} is shown in Figure 3-9 (c). This figure shows that the quasi-circulator can provide large SIC for a wide range of transmit signal power.

The measured Power Spectral Density (PSD) for a wideband QPSK signal with BW=40MHZ is shown in Figure 3-9 (d). With the reconfigurable impedance block and leakage cancellation block, there is over 50 dB of cancelation. The measurement results are summarized and compared to the state-of-the-art literature in Table 3-2.

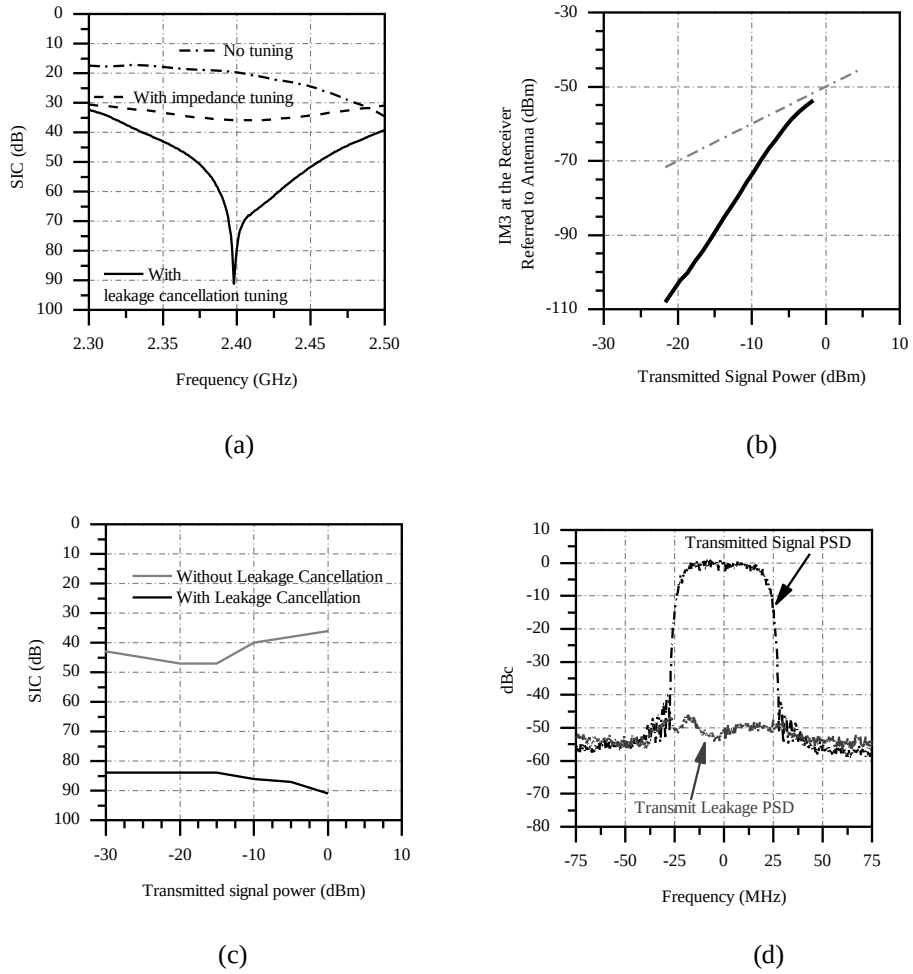


Figure 3-9 TX-RX Path Measured and Simulated Results (a) SIC With and Without Leakage Cancellation, (b) IM3 vs. TX power, (c) SIC vs. Transmit Signal Power With and Without Leakage Cancellation, and (d) PSD of the 40 MHz QPSK Modulated Transmit Signal and the Leakage Signal.

Table 3-2 Comparison Table and Performance Summary

	TMTT 2010 [17]	TMTT 2015 [21]	JSSC 2015 [38]	JSSC 2016 [27]	ISSCC 2017 [28]	This work
Process	180 nm CMOS	180 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	130 nm CMOS
Frequency	24 GHz	24 GHz	0.1-1.5 GHz	0.6-0.8 GHz	0.6-0.97 GHz	2.3-2.5 GHz
Receiver NF	17 dB	4-11 dB	5-8 dB	5 dB	6.3 dB	4.5 dB
NF Degradation in Full-Duplex	N/A	N/A	N/A	5.9 dB	1.7 dB	0.5 dB
SIC	70 dB at 1.5 GHz	20 dB at 380 MHz	33 dB at 300 KHz	42 dB at 12 MHz	40 dB at 20 MHz	more than 55 dB at 40 MHz
IL_{TX-Ant}	N/A	5.7 dB	N/A	1.7 dB	1.8 dB	3.8 dB
TX Port Power Handling	0 dBm	8 dBm[8]	-17.3 dBm	N/A	8 dBm	6 dBm
$IIP3_{TX-RX}$	N/A	N/A	-5 dBm	1 dBm [2]	9 dBm [4]	0 dBm [6]
$IIP3_{Ant-RX}$	0.6 dBm	N/A	-25 dBm	-33 dBm [3]	-18.4 dBm [5]	5 dBm [7]

1- From Figure 31 (a) in [38]. 2- The measured IIP3 for the circulator and baseband cancellation with 42 dB gain. 3- IIP3 in antenna and receiver path. Receiver gain is 42 dB. 4- Receiver gain is 26 dB. 5- Receiver gain is 28 dB. 6- Receiver gain is 11 dB. 7- Receiver gain is 11 dB. 8- From Figure 27 in [21].

CHAPTER 4

RECONFIGURABLE RX WITH ON-CHIP HYBRID AND BASEBAND LEAKAGE CANCELLATION

4.1 Introduction

Full duplex wireless has recently gained significant attention since it improves the spectral efficiency up to two times. Also, it simplifies the management of the spectrum, reuses radio resources in small cells to eliminate the backhaul problem, and reduces the costs of future telecommunication systems [5, 6].

Full duplex wireless enables simultaneous transmit and receive of the data at the same time and same frequency in the TRX. The feasibility of the SI cancellation for the wireless full duplex with discrete-components has been shown in [7, 35]. SI cancellation at the RX input has been implemented by a circulator [7], or increasing the isolation at the TX and RX antennas [54, 55, 56, 57]. Also, a replica of the TX output has been modified and injected to the RX to perform a SI cancellation [7, 54, 57, 58]. Finally, the rest of the SI has been cancelled in digital domain [57, 59, 60, 61, 62].

Although the feasibility of FD wireless has been shown in [29], designing a fully-integrated full duplex TRX with high TX power and large BW is still a big challenge. TX signal power, RX NF, SI cancellation BW, and high-power SI at the RX are the concerns in designing the full duplex TRX. On-chip tuning of the antenna system is reported in [9] to reduce the SI in mm-wave TRX. Using two antennas for the applications which are not mm-wave is bulky; consequently, it is better to use a circulator or hybrid and share one antenna between TX and RX. The main challenge of using a circulator is compensating the antenna impedance errors which need an additional reconfigurable antenna

impedance tuner. Additional reconfigurable antenna impedance tuner increases the loss between TX and antenna and NF in the RX path.

On-chip circulators based on time varying circuits have been reported in [18, 20, 21, 29, 48]. The main challenges of using circulators based on time varying circuits in FD wireless are the large transmitted signal power and non-idealities of the antenna impedance. In [21], a balance network is proposed in an on-chip circulator to compensate the antenna impedance errors, but it still needs an off chip fixed matching circuit. On-chip hybrids and quasi-circulators based on passive cancellation [22, 24, 63] provides higher TX power, higher SIC, and wider range of the antenna impedances without using the off chip antenna impedance tuner, but they have more insertion loss compared to the on-chip circulators based on time varying circuits. Antenna separation, on-chip circulator, and on-chip hybrid cannot provide enough SIC in a fully-integrated FD TRX. The rest of SI can be cancelled at the RF [24, 25, 26] or at the baseband [26, 27, 29, 48]in a fully integrated TRX with SIC.

In this paper, we present a FD integrated RX with an on-chip hybrid and BASEBAND SI canceller. In the proposed structure, the transmitted signal power is 23 dBm average and 30 dBm peak, the signal bandwidth is 20 MHz, and the carrier frequency can be set between 1.7~2.7 GHz. This paper is outlined as follows. Section II discusses the FD system design. Section III describes the RX with BASEBAND SI canceller. Section IV shows the circuit implementation on CMOS technology. Section V reports the measurement results of the FD TRX, and finally, section VI concludes the paper.

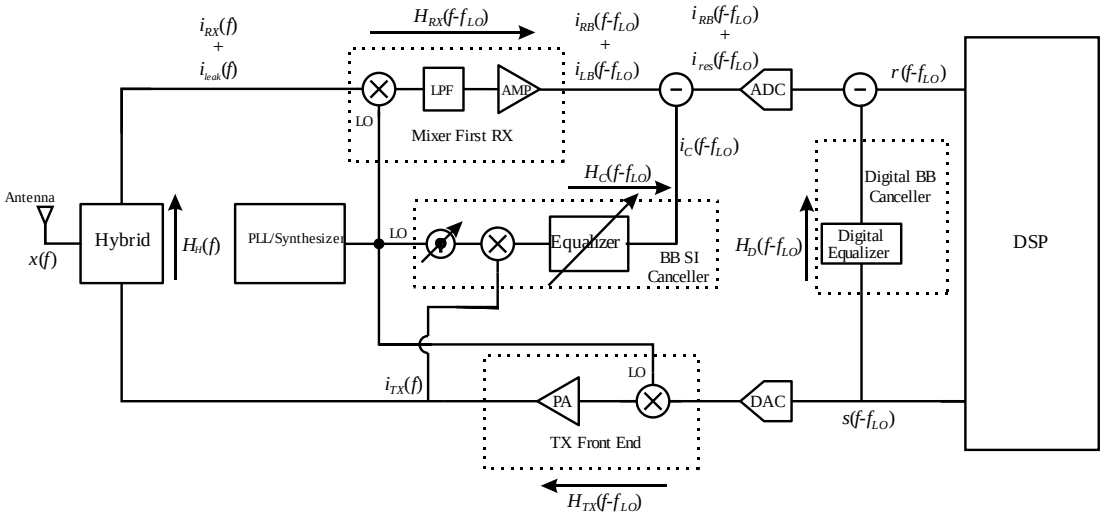


Figure 4-1 Top Level Block Diagram for the FD Wireless TRX With a Hybrid and Baseband SI Canceller.

4.2 Full-Duplex System Design

4.2.1 Architecture

The proposed architecture is shown in Figure 4-1. This block diagram consists of TX, RX, hybrid, BASEBAND SI canceller, and digital SI canceller. The baseband TX signal $s(f–f_{LO})$ is up-converted by the TX, and the TX signal current after the Power Amplifier (PA) is $i_{TX}(f)$. The TX signal current after the PA, $i_{TX}(f)$, goes to the antenna through the hybrid. Hybrid shares one antenna between TX and RX. Ideally, hybrid conducts the TX signal to the antenna, conducts the desired RX signal $x(f)$ from the antenna to the RX, $i_{RX}(f)$, and doesn't conduct any part of the $i_{TX}(f)$ to the RX. Because of mismatches in antenna impedance, hybrid, and echo from the environment, a portion of the TX signal current $i_{TX}(f)$ leaks to the RX which is the SI signal current $i_{leak}(f)$.

Both desired RX signal current $i_{RX}(f)$ and SI signal current $i_{leak}(f)$ is down-converted by the mixer-first RX to the baseband. Mixer first RX provides high Q bandpass response at its input due to the Low Pass Filter (LPF) in baseband, which

improves the out of band blocker signal cancellation [64, 65]. The baseband Low Noise Amplifier (LNA) amplifies both desired RX signal and SI signal current and its output current is $i_{RB}(f-f_{LO})+i_{LB}(f-f_{LO})$. The $i_{RB}(f-f_{LO})$ is the desired RX signal current and $i_{LB}(f-f_{LO})$ is the SI current at the baseband.

The SI current at the baseband $i_{LB}(f-f_{LO})$ is cancelled further by injecting the cancellation current $i_C(f-f_{LO})$ in to RX. To cancel the SI current at the baseband $i_{LB}(f-f_{LO})$, the cancellation current $i_C(f-f_{LO})$ has to be equal to the SI current at the baseband, $i_C(f-f_{LO})\sim i_{LB}(f-f_{LO})$. To generate the cancellation current $i_C(f-f_{LO})$, the baseband SI canceller samples the TX signal current after the PA $i_{TX}(f)$, and down-converts it to the baseband. Phase of the down-converted signal is controlled by a phase shifter at the LO path of the down-converter mixer. A reconfigurable equalizer provides a variable phase and amplitude versus frequency to mimic the frequency response of the path between TX and RX. By providing variable phase and amplitude versus frequency in the baseband SI canceller circuit, the bandwidth (BW) of the baseband SIC will be increased. Finally, Variable Gain Amplifier (VGA) controls the amplitude of the cancellation current $i_C(f-f_{LO})$ and injects it to the RX.

Because of amplitude and phase mismatches between $i_{LB}(f-f_{LO})$ and $i_C(f-f_{LO})$, a portion of the SI current leaks to the RX output which is $i_{res}(f-f_{LO})=i_{LB}(f-f_{LO})-i_C(f-f_{LO})$. After SIC at the baseband, the signal at the RX output is converted to digital by the Analog-to-Digital Converter (ADC). Finally, the residual TX signal is cancelled in digital domain, by the digital filter. The digital filter samples the TX signal in digital domain and modifies the sampled TX signal. Then, digital filter cancels the residual TX signal and TX distortions to push the leaked signal below the RX noise floor. The digital RX signal

after digital SIC is $r(f-f_{LO})$ which ideally just consists of the information of the desired RX signal at the antenna $x(f)$.

4.2.2 Full Duplex Link Budget

Fig 4-2 shows the SI signals and SIC in the proposed FD TRX. The TX signal current after the PA $i_{TX}(f)$ is shown in this figure which consists of main TX signal in red and the TX noise in gray. Besides, the desired RX signal $x(f)$ at the antenna is shown with the blue color, and the generated distortion signals in the hybrid, RX, and baseband SI canceller due to the non-linear response of the signal path is shown in green. In this paper, all the SICs are in dB and all the signal powers are in dBm.

In the proposed structure, SIC at the hybrid is $SIC_H = -20\log_{10}|H_H(f)|$where H_H(f) is the transfer function between TX port and RX port in the hybrid. Besides, the SIC in the baseband is $SIC_{BB}=-20\log_{10}|i_{res}(f-f_{LO})/i_{LB}(f-f_{LO})|$. Hybrid and baseband SI canceller

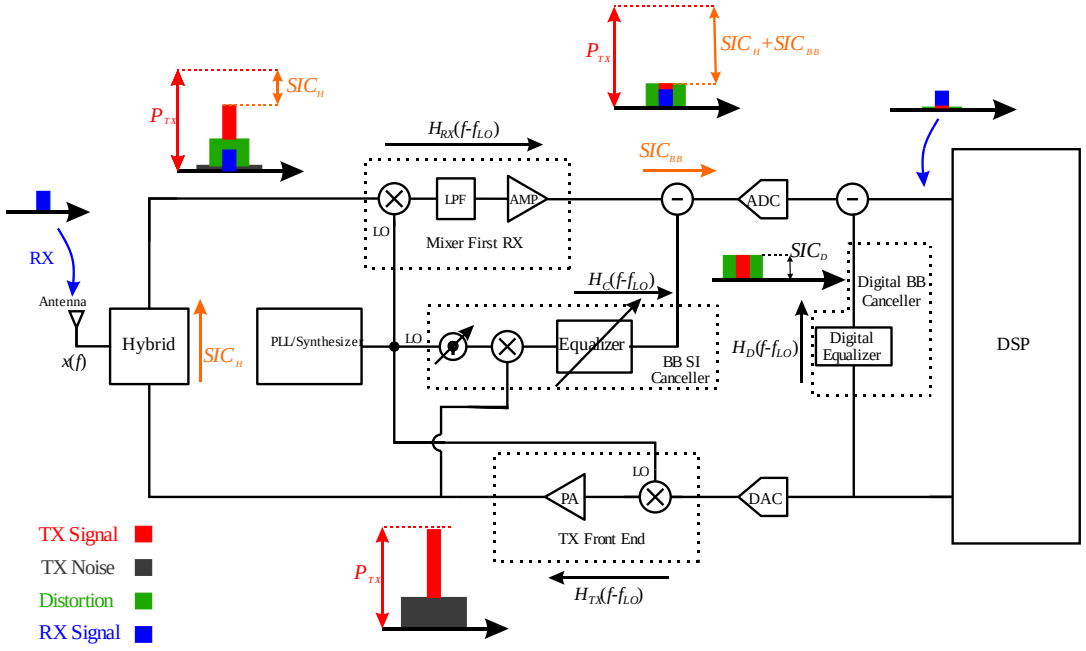


Figure 4-2 FD TRX Block Diagram With SIC and SI Signals in the Proposed Structure.

have to keep the residual signal inside the ADC dynamic range ADC_{DR}. The ADC dynamic range ADC_{DR} in the proposed structure is $ADC_{DR}=P_{TX}-P_n-SIC_H-SIC_{BB}$ +10 where 10 dB margin is assumed for ADC dynamic range, P_n is noise power at the RX ($P_n=-174\text{dBm/Hz}+10\log_{10}(BW)+NF$), and PTX is the transmit signal power.

SIC in digital domain is necessary to push the SI signal below the RX noise floor. Not only the digital cancellation has to cancel the residual TX signal in the digital domain, but also it has to cancel the distortions of the SI signal in the RX. Larger distortion and SI in the RX path requires more complexity in the digital algorithm for SI and distortion cancellation, and also, it increases the required ADC dynamic range ADCDR. In this paper, it is assumed that the power of the distortion of the SI signal after baseband SIC is equal to the power of the residual of SI signal after the baseband SIC. By having this assumption, the third-order input referred intercept point (IIP3) of the hybrid, RX, and baseband SI canceller are calculated. The IIP3 between TX port and RX port of the hybrid, IIP3H, is calculated as follows:

$$IIP3_H = P_{TX} + \frac{1}{2}TLCR_{BB} + 2 \tag{4-1}$$

where 2 dB margin is added for the IIP3 between TX and RX ports of the hybrid. The remnant of the SI after the hybrid is down-converted to the baseband and cancelled by the baseband SI canceller. The required IIP3 of the RX $IIP3_{RX}$ is calculated as follows,

$$IIP3_{RX} = P_{TX} - TLCR_H + \frac{1}{2}TLCR_{BB} + 2 \tag{4-2}$$

As it is shown in (2), increasing the SIC in the hybrid relaxes the required IIP3 of the RX. In addition to hybrid and RX, the baseband SI canceller also has to provide enough IIP3 to not degrade the linearity performance of the FD TRX. The TX signal after the PA is sampled by a coupler and fed to the baseband SI canceller. Assuming the coupling factor of the coupler is C in dB, the IIP3 of the baseband SI canceller $IIP3_C$ is calculated as,

$$IIP3_C = P_{TX} - C + \frac{1}{2}TLCR_{BB} + 2 \tag{4-3}$$

Assuming a Long-Term Evolution (LTE) wireless system with 20 MHz bandwidth, 23 dBm average TX power, 10 dB RX noise figure, 50 dB SIC in hybrid, 20 dB SIC at the baseband, and 20 dB coupling factor in the coupler of the baseband SI canceller, the ADC dynamic range is ADC_{DR} =54 dB, hybrid IIP3 is $IIP3_H$ =35 dBm, RX

Table 4-1 Summary of the LTE System Link-Budget

		Goals
RX	Frequency	1.7-2.7 GHz
	BW	20 MHz
	NF	11 dB
	ADC Dynamic Range	54 dB
TX	Frequency	1.7-2.7 GHz
	BW	20 MHz
	Average Power	23 dBm
	Peak Power	30 dBm
SIC	Total SIC	113 dB
	Analog SIC	70 dB
	Digital SIC	43 dB

IIP3 is $IIP3_{RX}$ = −15 dBm, and baseband SI canceller IIP3 is $IIP3_C$= 15 dBm. Table I summarizes the LTE FD link budget.

4.3 Baseband Self-interference Canceller

Figure 4-3 shows the block diagram of the proposed N-path mixer first RX with baseband SI canceller. The RX down-converts the received current $i_{RX}(f)$ and the SI current $i_{leak}(f)$ and its output signals are RX current at the baseband $i_{RB}(f-f_{LO})$ and baseband SI current $i_{LB}(f-f_{LO})$. The goal of the baseband SI canceller is to provide more than 20 dB SIC in the operation bandwidth.

To cancel the baseband SI current in a wide bandwidth, the baseband SI canceller should mimic the transfer function of the path between the PA and the RX output in the

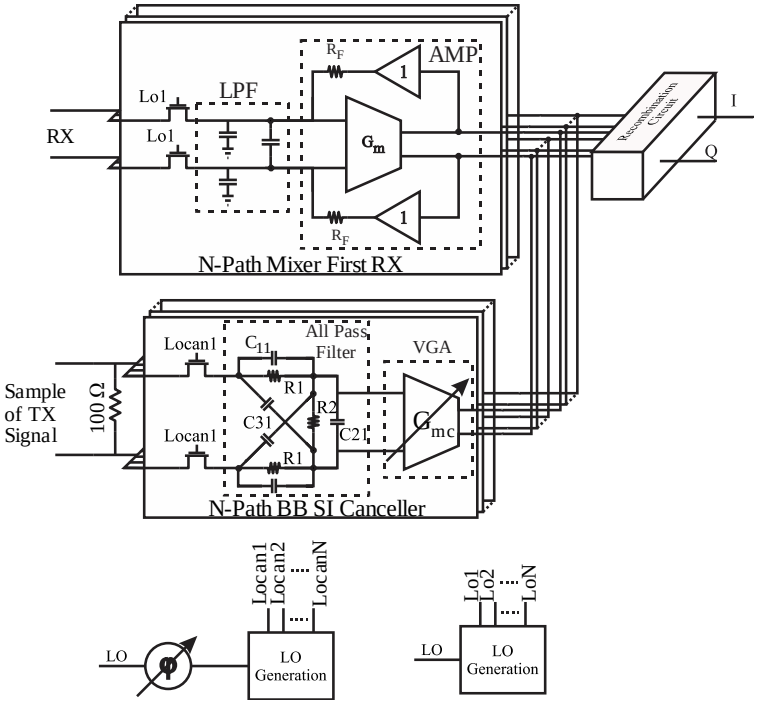


Figure 4-3 Proposed N-Path Mixer First RX With N-Path Wideband Baseband SI Canceller.

operation bandwidth. The amplitude and phase of the transfer function between PA and RX output varies versus frequency. In addition, the echo from the environment and the antenna impedance are not known and are changing versus time. Consequently, the transfer function of the path between PA and RX output is an unknown and varying versus both time and frequency.

To achieve 20 dB SIC at RX output in the operation bandwidth, the phase and amplitude error between the leakage path and cancellation path in the operation bandwidth should be less than 0.6 dB and 4°, respectively. Consequently, phase shifter tuning step should be less than 4°, the VGA tuning step should be less than 0.6 dB, and equalizer should have enough flexibility to provide required variation in phase and amplitude versus frequency for the cancellation signal.

The proposed equalizer structure is a continuous time analog filter which consists of a variable pole on the left side of the s-plane, and a variable zero on the left or right side of the s-plane. In Figure 4-3, in path i^{th}, C_{1i} and R_1 create a zero on the left side of s-plane, C_{3i} and R_1 create a zero on the right side of the s-plane, and R_1, R_2, C_{1i}, C_{2i}, and C_{3i} create a pole on the left side of the s-plane. By varying capacitors C_{1i}, C_{2i}, and C_{3i}, frequency of the pole and zero can be set in the equalizer.

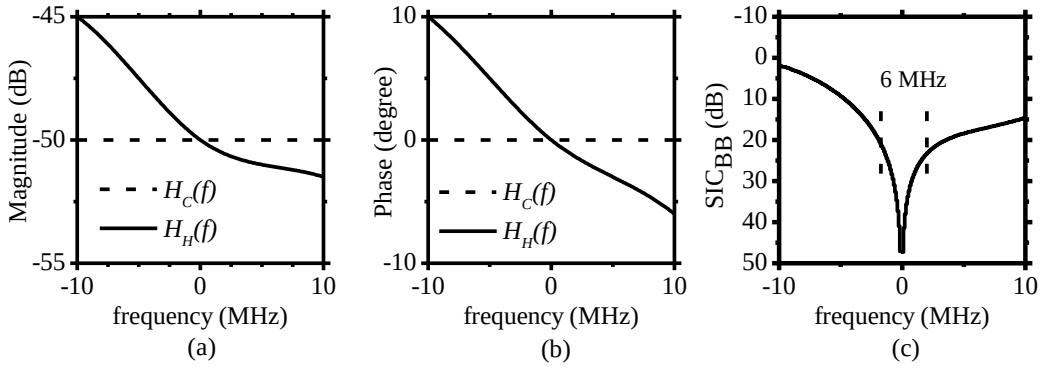


Figure 4-4 (a) Magnitude and (b) Phase of the Transfer Functions of the Hybrid With Antenna Impedance Model and Baseband SI Canceller Without the Equalizer, and (c) SIC at the RX Output SIC_{BB}.

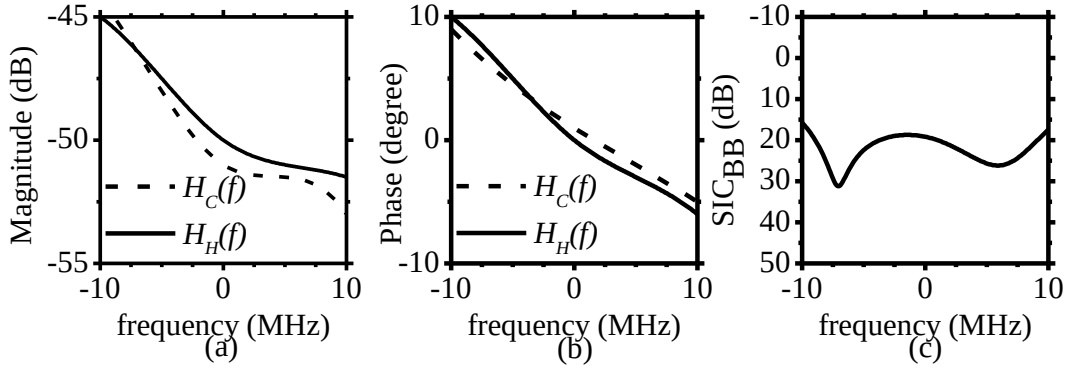


Figure 4-5 Magnitude and (b) Phase of the Transfer Functions of the Hybrid With Antenna Impedance Model and Baseband SI Canceller With the Equalizer, and (c) SIC at the RX Output SIC_{BB}.

Each path of the N-path baseband SI canceller has its own equalizer with controllable zero and pole frequencies. The minimum/maximum frequency of the poles and zeros of the equalizer are the key parameters of the equalizer design. For this design, antenna impedance is modeled with the frequency-independent lumped element for wideband frequencies [66, 67]. By simulating the proposed structure, the baseband SI canceller parameters are found. The required minimum/maximum frequency of the

Table 4-2 Summary of the Baseband SIC Performance

		Goals
baseband SI canceller	Pole frequency	5-100 MHz
	Left or right zero frequency	5-160 MHz
	Phase step	4°
	VGA step	0.6 dB
	IIP3 with *C*=22 dB	15 dBm

equalizer pole and zero should be within 5-100 MHz and 5-160 MHz, respectively, to achieve more than 20 dB SIC in the operation bandwidth at the baseband.

Figure 4-4 shows the baseband SIC without using the equalizer. The phase shifter and VGA provide flat phase/magnitude response versus frequency for the baseband SI canceller which cannot mimic the phase/magnitude of the frequency response of the path between TX and RX output. In this example, a physical model is used for the antenna impedance. As it is shown in Figure 4-4 (c), the 20 dB SIC bandwidth is 6 MHz. Figure 4-5 shows the same example for the baseband SIC with equalizer. In this figure, more than 20 dB SIC has been achieved in 20 MHz bandwidth. Table II summarizes the specification of the baseband SI canceller.

4.4 Implementation and Circuit Design

The proposed structure is designed and fabricated on a CMOS 65 nm technology. Figure 4-6 shows the implemented on-chip circuit for the hybrid, mixer first RX, and baseband SI canceller to enable the FD wireless. Hybrid is implemented by two transformers and a reconfigurable load. Two back to back diodes are added between hybrid and RX as a power limiter which does not affect the performance of the RX in the

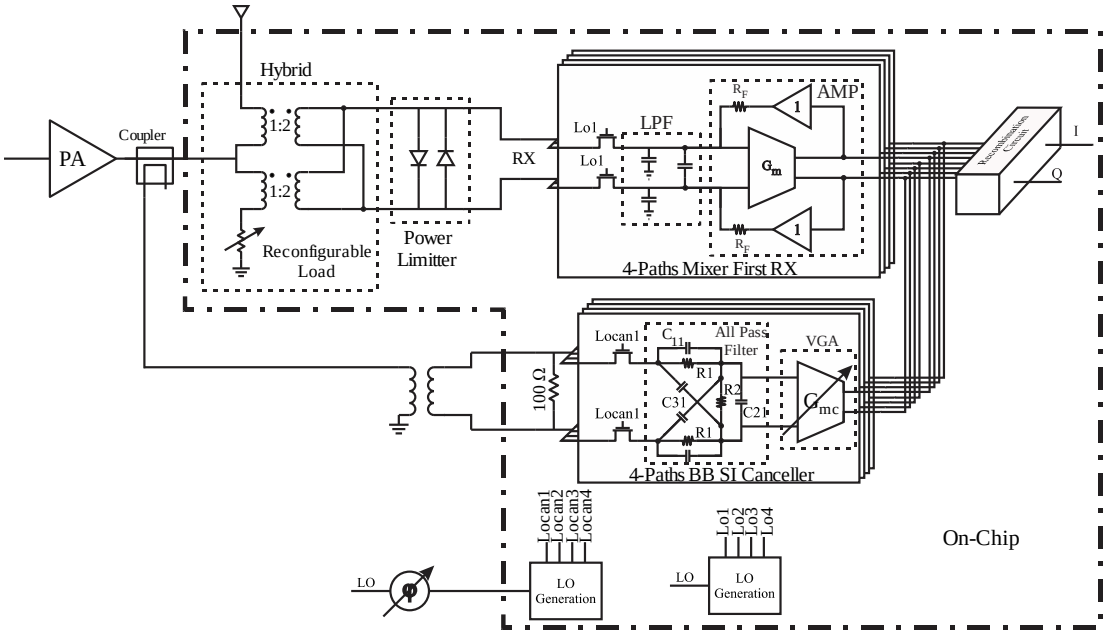


Figure 4-6 The Implemented On-Chip RX for LTE Standard With a Hybrid and a Baseband SI Canceller for the FD Wireless TRX.

normal situation. If high power signal goes to the RX, the diodes will turn on and protect the RX. The RX is a four paths mixer first architecture and the LO phase generator block generates the LO clock phases with 25% duty cycle for the RX down-converter.

The TX signal is sampled after the PA with an off the chip coupler which has 22 dB coupling factor, and the sampled TX signal is transformed to a differential signal by using an off the chip Balun, and then it goes to the on-chip baseband SI canceller circuit. The baseband SI canceller is a four paths down-converter. Phase of the down-converted signal is controlled by an off the chip phase shifter in the LO path of the down-converter. In this section, circuit design is discussed in details.

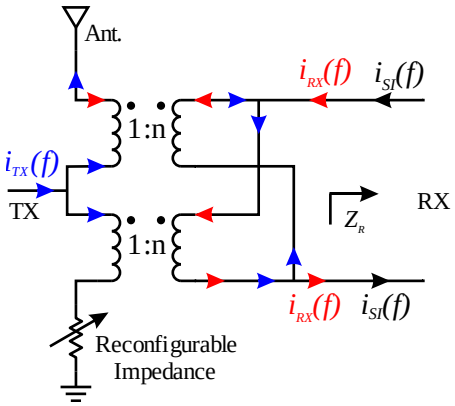


Figure 4-7 Proposed Hybrid Topology Which Cancels the TX Signal Current $i_{TX}(f)$ at the RX Port and Conducts the RX Signal From the Antenna to the RX Port.

4.4.1 Hybrid

Figure 4-7 shows the hybrid topology which contains of two transformers with the ratio n and a reconfigurable load. The blue arrows show the TX current $i_{TX}(f)$ in the hybrid, and the red arrows show the RX current $i_{RX}(f)$ in the hybrid. The RX signal current at the antenna $i_x(f)$ by passing through the transformers goes to the RX as differential-mode signal $i_{RX}(f)$; the TX signal current $i_{TX}(f)$, by passing through the transformers, is divided by two. One part of the transmitted signal goes to the antenna and the other part goes to the reconfigurable load. In balance situation, TX signal is cancelled at the RX port; otherwise, a portion of the TX signal leaks to the RX $i_{leak}(f)$.

There are three paths in the on-chip hybrid: ANT-RX, TX-ANT, and TX-RX. The goals in ANT-RX and TX-ANT paths are impedance matching at the antenna and TX ports, and low insertion loss in ANT-RX and TX-ANT paths. The goal in TX-RX path is cancelling the leakage signal.

Assuming transformer ratio n=2, impedance of the reconfigurable load Z_L=50 Ω, impedance of the RX Z_R=100 Ω, the antenna impedance will be Z_{ANT}=50 Ω and the input impedance of the TX port will be Z_{TX}=25 Ω. In addition, the ratio between the RX current

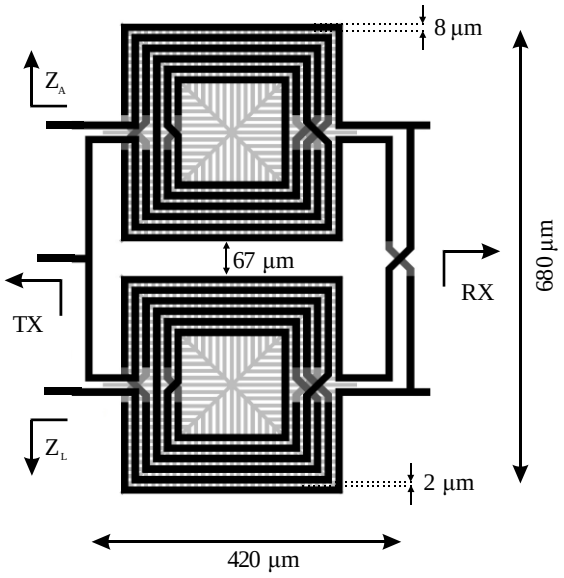


Figure 4-8 Implemented Layout for the Hybrid Structure on CMOS Technology.

after the hybrid $i_{RX}(f)$ and the RX current at the antenna $i_x(f)$ is 0.5 which means 3 dB insertion loss (it has to be considered that the RX impedance is twice the antenna impedance), and the ratio between the TX current at the antenna $i_{TA}(f)$ and the TX current at the TX port $i_{TX}(f)$ is 0.5 which means 3 dB insertion loss (it has to be considered that the antenna impedance is twice the TX impedance).

Figure 4-8 shows the layout of the proposed hybrid topology which contains two transformers with the ratio 2. In the layout of the hybrid, the metal width is 8 µm and the gap between the metals is 2 µm. The metal width has chosen based on the maximum current of the peak power of the TX signal. The distance between the transformers doesn't have any effect on the SIC, but it can degrade the impedance matching at the antenna port. This structure has been simulated by the full-wave simulators, and the minimum distance between the transformers, 67 µm, has been found to not degrade the impedance matching of the antenna port. The total area of this structure is 420 µm × 680 µm.

The goals of the reconfigurable load are tolerating the TX power (23 dBm average and 30 dBm peak power plus 3 dB margin), generating small distortions (IM3 at the reconfigurable load has to be less than −47 dBm with 3 dB margin for the TX power), and tracking the antenna impedance to provide SIC more than 53 dB in the hybrid. Assuming small difference between impedance of the antenna and impedance of the reconfigurable load, the SIC in the hybrid is $SIC_H \approx -20\log_{10}|\Delta z/400|$, where $\Delta z = Z_L - Z_A$. Consequently, to achieve 53 dB SIC (50 dB plus 3 dB margin) in the hybrid, the difference between impedance of the antenna and impedance of the reconfigurable load should be less than 0.9 Ω.

The circuit of the variable impedance is shown in Figure 4-9 (a) which contains of

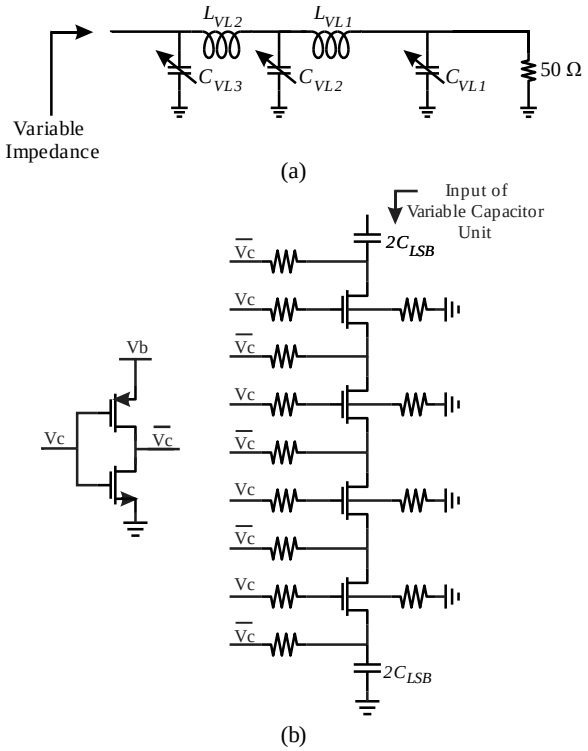


Figure 4-9 Variable Impedance Which Contains Two Constant Inductors and Three High-Voltage Tolerant Variable Capacitors, (b) Unit Cell of the High Voltage Tolerant Variable Capacitor.

two constant inductors which are 2 nH and three high-voltage tolerant variable capacitors. Each capacitor is a digitally controlled capacitor which varies between 500 fF - 3.7 pF with 100 fF step. High-voltage tolerant switch with good linearity has been designed [21, 22] to connect and disconnect these capacitors to the variable impedance circuit. Switches have been designed by using 4 thick gate oxide MOSFETs in stack as it is shown in Figure 4-9 (b). When the switches are off, the drain and source of the switches are biased at Vb to keep the transistors in the off region in presence of the high-power RF signal which is described in details in [21, 22].

4.4.2 Baseband Amplifiers

Figure 4-10 (a) shows the baseband LNA circuit along with the VGA of baseband SI canceller which is repeated in all the paths. The differential input current which is down-converted from the hybrid, goes to the input of a Gm-stage. The Gm-stage consists

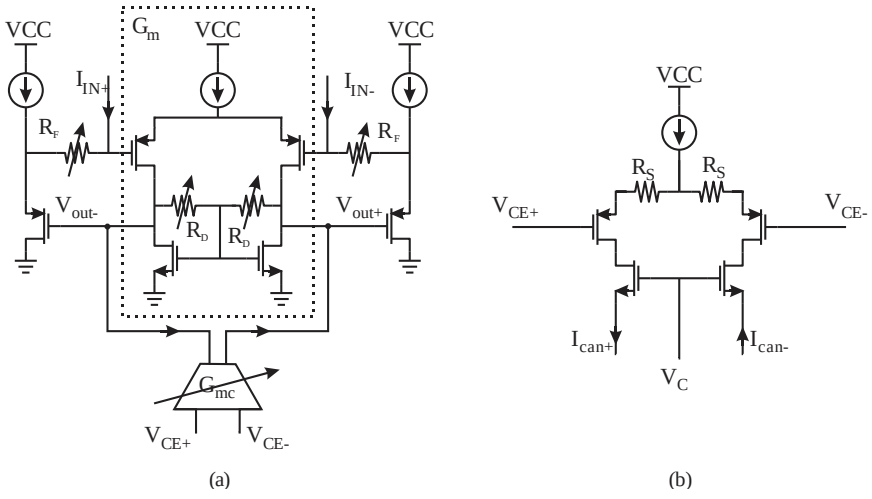


Figure 4-10 (a) Baseband Amplifier Circuit With the Gm-Stage, Buffers, Feedback Resistors, and Variable Gmc-Stage (b) Unit Cell of the Variable Digitally Controlled Gmc-Stage Which Injects the Cancellation Current in to the Gm-Stage Output.

of differential amplifier and variables resistors, R_D, which enables the Gm-stage to provide variable gain between 15 dB to 30 dB. Two unity gain source-follower P-channel MOSFETs connect the Gm-stage output to the feedback resistors, R_F. The variable feedback resistor R_F provides variable impedance at the RX input port [64, 65]which improves RX input impedance matching.

Figure 4-10 (b) shows a unit cell of the VGA which is a differential resistive source degenerative Gm which its outputs can be turned on and off by two N-channel MOSFETs. The degenerative resistors are added to improve the linearity of the VGA. The VGA is a digitally controlled variable Gm-stage which is controlled by 6 digital bits V_C.

4.4.3 Baseband Equalizer

Figure 4-11 (a) shows the baseband equalizer circuit which provides a zero on the left or right side of the s-plane and a pole on the left side of the s-plane. To achieve the goals described in Table II, each variable capacitor should vary between 200 fF to 8 pF with 250 fF step, and R_1 and R_2 should be 5 kΩ and 3.5 kΩ, respectively. Each capacitor in the equalizer is a binary weighted variable capacitor with 5 control bits. Figure 4-11 (b) shows the unit cell of each variable capacitor. When the switch is on, voltage of drain and source of the switch is zero, and when the switch is off, the voltage of drain and source of the switch is Vbc.

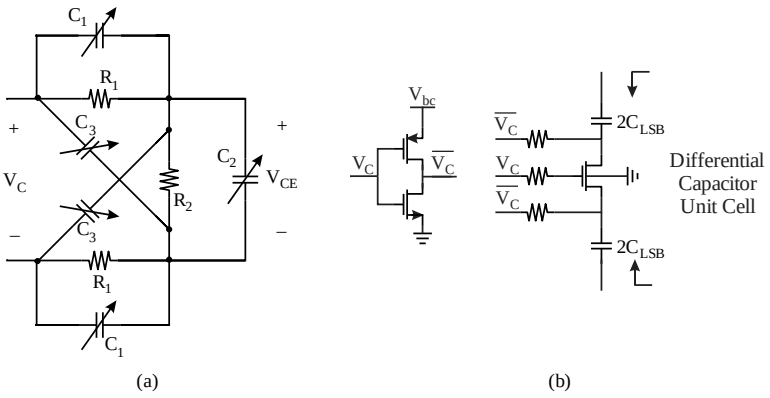


Figure 4-11 (a) Baseband Equalizer Circuit With a Variable Zero on Left or Right Side of s-Plane and a Variable Pole on the Left Side of the s-Plane (b) Unit Cell of the Digitally Controlled Variable Capacitor.

4.5 Measurement

The RX with a hybrid and baseband SI canceller are implemented in CMOS 65 nm technology for FD wireless and its microphotograph is shown in Figure 4-12. The total area of this chip is 2mm × 2mm which consists of the hybrid, RX, baseband SI canceller, Electrostatic Discharge (ESD) protections, and Serial Peripheral Interface (SPI) controls. The core area of the proposed structure is 1.6 mm × 1.6 mm. The implemented chip is packaged in QFN 56. The key parameters of the FD TRX are the return loss of the antenna and TX port, NF, TX to antenna insertion loss, SIC in the path between TX and RX, and the linearity of the RX, hybrid, and the baseband SI canceller. The measurement results are presented in three subcategories: ANT-RX path, TX-ANT path, and TX-RX path.

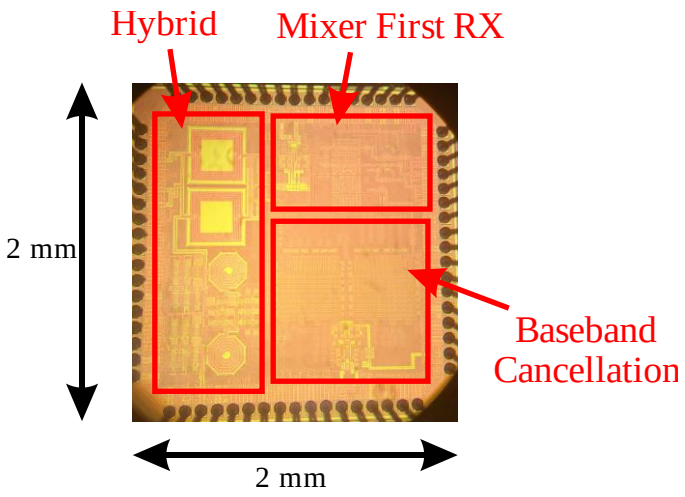


Figure 4-12 The Microphotograph of the Implemented Chip in CMOS 65 nm.

4.5.1 ANT-RX path

The ANT-RX path in the implemented chip is the path between the antenna port and the RX output. The goals in this path are having a return loss of the antenna port better than 10 dB, NF better than 11 dB, more than 20 MHz complex baseband bandwidth for the RX, and the RX tuning frequency between 1.7 – 2.7 GHz. The return loss of the antenna port is shown in Figure 4-13 for different LO frequencies. As it is shown, the return loss of the antenna port is better than 15 dB and the gets worse for the frequencies far from the LO frequency. This bandpass filtering response is caused by the baseband capacitor and the transparency of the passive mixer.

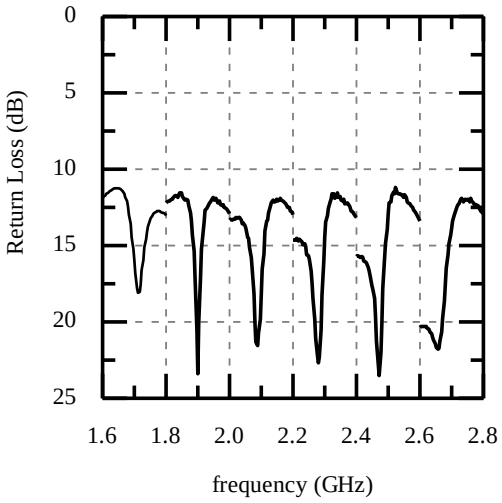


Figure 4-13 The Return Loss of the Antenna Port Versus Frequency for Different LO Frequencies.

The NF of the ANT-RX path is shown in Figure 4-14 which is better than 10 dB in the operation bandwidth, The RX NF was measured for each LO frequency in a half-duplex mode and all the parameters of the chip were tuned for the maximum SIC. The NF degradation due to the transmitted signal with 23 dBm average power is less than 0.5 dB which shows that the effect of TX on RX is negligible.

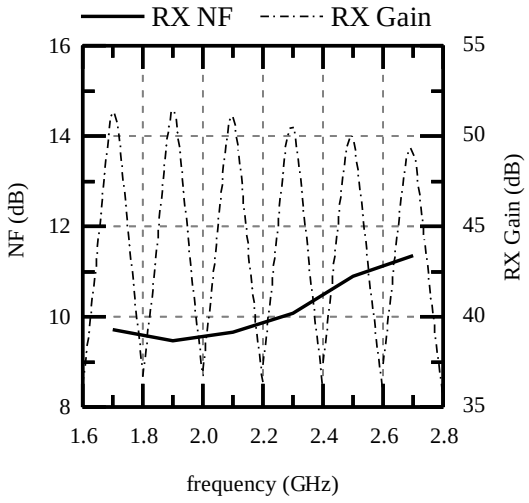


Figure 4-14 NF and the Gain of the RX Versus the Frequency.

In addition, the gain of the RX is shown in Figure 4-14. As it is shown, the RX gain is about 50 dB between the antenna input at the RF and the RX output at the baseband. Due to the LPF at the RX baseband, the RX gain performance is equivalent to a high Q band pass filter which cancels the out of band blocker signals.

In addition, the measured third order intermodulation signals (IM3) and the fundamental signals are shown for the ANT-RX path in Figure 4-15. In this figure, the IM3 signals and the fundamental signals are referred to the antenna port for better comparison. The input third order intercept point for this path ($IIP3_{ANT-RX}$) is -37 dBm for 50 dB RX gain.

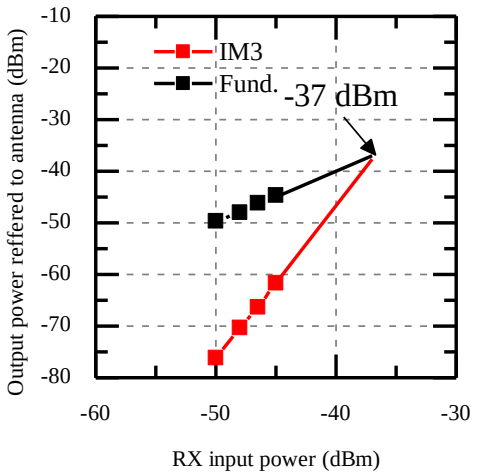


Figure 4-15 IM3 and Fundamental Signals in the ANT-RX Path Which Are Referred to the Antenna Port.

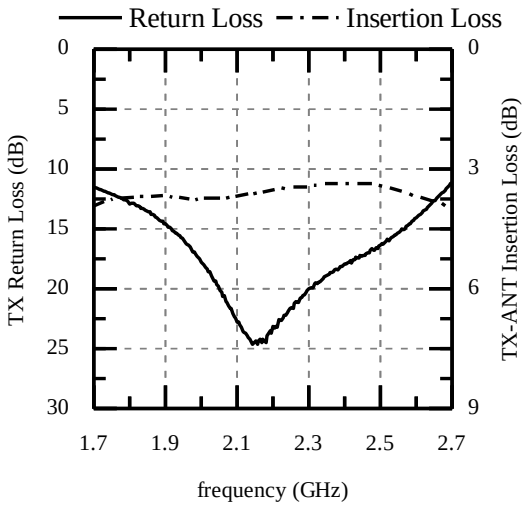


Figure 4-16 Return Loss of the TX Port and the Insertion Loss of the TX-ANT Path.

4.5.2 TX-ANT path

The TX-ANT path is between the TX port and antenna port in the implemented chip. The goals in this path are the return loss of the TX port better than 10 dB, insertion loss below 4 dB (the minimum insertion loss in the hybrid is 3 dB), and small distortion in transmitted signal at the antenna port. The return loss of the TX port is shown in Figure 4-16 versus frequency and it is better than 10 dB in 1-7-2.7 GHz. In addition, the insertion loss between the TX port and the antenna port is shown in Figure 4-16 which the results show the insertion loss below 3.8 dB in the entire operation bandwidth.

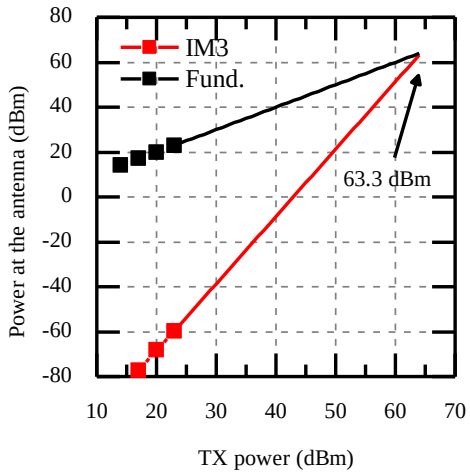


Figure 4-17 The IM3 and Fundamental Signals in the TX-ANT Path Which Are Referred to the Antenna Port.

The IM3 distortion due to the TX signal at the antenna port is measured and its results are shown in Figure 4-17. The power of the IM3 signals at the antenna port is about −59.7 dBm for the TX signal with 23 dBm average power. In this Figure, all the signals are referred to the antenna for the better comparison and the hybrid is tuned for the best SIC. The IIP3 in the TX-ANT path based on the measured IM3 is 63.3 dBm.

4.5.3 TX-RX path

The goal in the TX-RX path are achieving more than 70 dB SIC in analog domain and minimizing the effects of the TX signal on the RX performance. The average TX power should be 23 dBm and the peak power should be 30 dBm. The distortion signals due to the non-linear response of the hybrid, RX, and the baseband SI canceller should be below −47 dBm.

Figure 4-18 shows the SIC at the hybrid which the reconfigurable impedance was tuned for the best SIC at the different frequencies. In this measurement, the TX power

signal was a single tone signal with 0 dBm power. More than 50 dB SIC has been achieved for the frequencies where the reconfigurable impedance was tuned for.

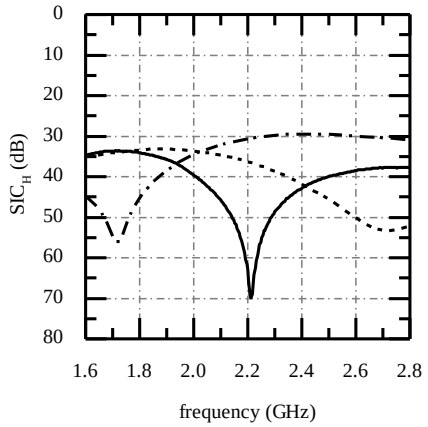


Figure 4-18 SIC at the Hybrid (SIC_H) For a Single Tone Signal With 0 dBm Power.

Figure 4-19 shows the worst-case measurement results for SIC with the baseband SI cancellation which happened at 2.4 GHz carrier frequency. The total SIC, hybrid and baseband, is more than 78 dB in 20 MHz bandwidth for a 0 dBm single tone signal. This measurement was done by using a single tone signal with 23 dBm power.

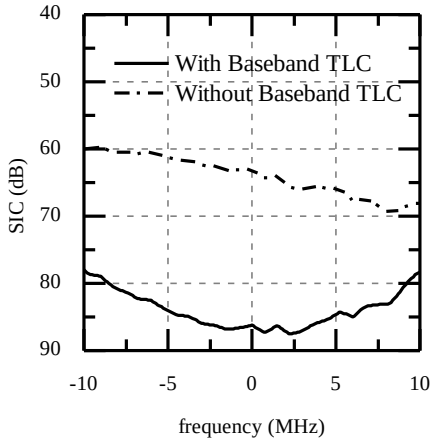


Figure 4-19 The Worst Case Measured Results For the Total SIC Which Happened at 2.4 GHz Carrier Frequency.

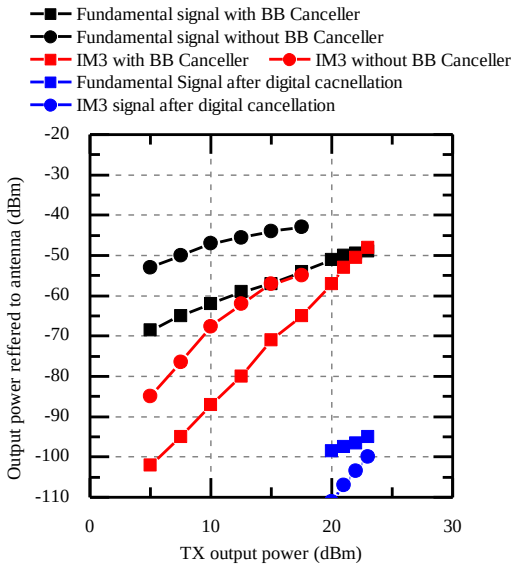


Figure 4-20 The Fundamental and IM3 Signal in the TX-RX Path Versus the Transmitted Signal Power at the Antenna.

The IM3 signals were measured versus the transmitted signal power at the antenna port. The signals at the RX output are referred to the antenna port for better comparison. The IM3 signal power is −50 dBm for 23 dBm input signal power. As it is shown in Figure 4-20, the baseband SI cancellation relaxes the RX; consequently, the transmitted power can be increased. The digital SIC has been implemented in Matlab by using a truncated Voltera series in a tapped delay line which is similar to the method was used in [29]. Equation 4-4 shows the function of the digital canceller in time domain

$$y[n] = \sum_{q=1}^{p} \sum_{k=1}^{N} h[k,q] x^{p}[k-n] \qquad (4\text{-}4)$$

where, *y[n]* is the cancellation signal in digital domain, *x[n-k]* is the delayed version (*k* is the index of the delay) of the transmitted signal which is sampled in digital domain, *p* is

the order of the truncated Voltera series, and *h[k, q]* is the unknown coefficients in the Voltera series.

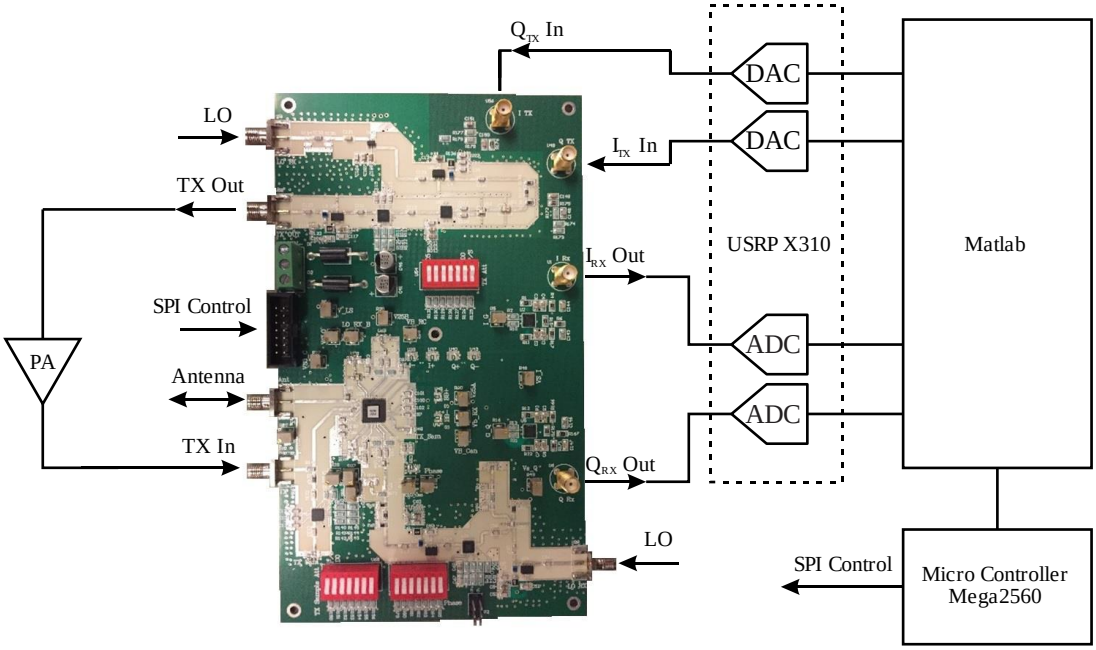


Figure 4-21 Hardware Setup For Pseudo Real-Time Signal Processing.

The received signal is captured by USRP X310 and the captured data is processed by Matlab to generate the cancellation signal in digital domain in 10 MHz bandwidth (the bandwidth is limited by the data capturing hardware in a pseudo real-time signal processing system). To reduce the power of the SI signal below the RX noise floor in the operation bandwidth, the length of the tapped delay line is 35 (N=35) and the order of the truncated Voltera series is 4 (p=4). The fundamental and IM3 distortion signals after the digital SIC are also shown in Figure 4-20 which are less than receiver noise floor, -90 dBm, which means more than 113 dB SIC in the full duplex transceiver. The hardware setup for the pseudo real-time signal processing is shown in Figure 4-21. The measurement results are summarized and compared to the state-of-the-art literature in Table 4-3.

Table 4-3 Summary and Comparison Table

	ISSCC 2017 [26]	JSSC 2017 [29]	ISSCC 2017 [19]	This Work
Process	CMOS 40 nm	CMOS 65 nm	CMOS 65 nm	CMOS 65 nm
Architecture	Adaptive RF and baseband cancellation based on equivalent analog FIR filter	On-chip magnetic free circulator, RX, and baseband self-interference cancellation	Magnetic free circulator and RX based on N-path filter and on-chip balance network	Mixer First RX with an on-chi hybrid and baseband self-interference cancellation
Frequency	1.7-2.2 GHz	0.6-0.8 GHz	0.61-0.975 GHz	1.7-2.7 GHz
RX Gain	20-36 dB	42 dB	28 dB	50 dB
NF in full duplex mode	5.5[1] dB	10.9 dB[4]	8 dB	11.5 dB
Integrated antenna interface	NO	Yes	Yes	Yes
Analog SIC	50 dB[2] at 42 MHz	42 dB at 12 MHz[5]	40 dB at 20 MHz	>70 dB at 20 MHz
Total SIC incl. digital SIC	N/A	85 dB	80 dB	113 dB
TX port power handling	25 dBm at 35 dB antenna interface isolation	N/A	8 dBm	30 dBm
IIP3 ANT-RX	N/A	-33 dBm at 42 dB RX gain	-18.4 dBm at 28 dB RX gain	-37 dBm at 50 dB RX gain
IIP3 TX-RX	N/A	1 dBm at 42 dB RX gain	9 dBm at 26 dB RX gain	59.5 dBm at the maximum SIC and 50 dB RX gain
Power consumption	33.5 mW[3]	159 mW[6]	108 mW[7]	110 mW

[1]RX NF is 4 dB, and RF canceller adds 1.05 dB and baseband canceller adds 0.5 dB to the NF. [2]35 dB leakage cancellation is achieved at RF and 15 dB leakage cancellation is achieved at the baseband. [3]RX power consumption is 22 mW, RF canceller power consumption is 3.5 mW, and baseband canceller power consumption is 8 mW. [4]5 dB NF in time division duplex and 5.9 dB NF degradation due to the full duplex mode. [5]22 dB leakage cancellation in the on-chip circulator and 20 dB leakage cancellation in the baseband cancellation. [6]Power consumption of the RX, baseband leakage canceller, and circulator are 70 mW, 30 mW, and 59 mW, respectively. [7]Power consumption of the RX and circulator are 72 mW and 36 mW, respectively.

4.6 Adaptive Algorithm

To provide large SIC in a full duplex TRX, the unknown parameters of the baseband SI canceller, hybrid and digital canceller have to be found. During finding the unknown parameters, RX cannot receive the desired signal due to the large SI signal which is not cancelled properly. Consequently, this procedure can reduce the channel efficiency of the full duplex TRX. To provide a tuning procedure compatible with LTE standard and not losing the channel efficiency significantly, we can use the Sounding Reference Signal (SRS) [68, 69] which is used for uplink channel estimation. The duration of SRS is 1 mS or more and it is added to the end of the uplink frame. In this algorithm, a multi tone signal with 2 MHz frequency difference has been used as SRS in the operation bandwidth. Consequently, while TX is transmitting SRS for channel estimation, baseband SI canceller, hybrid, and digital canceller can be tuned for the maximum SIC. Repetition of the SRS in LTE channel is sufficient to provide enough analog SIC in full duplex TRX in time varying indoor and outdoor channels. To find the unknown coefficients, first a search algorithm is used to optimize the SIC in the hybrid. Then, the SIC in the baseband SI canceller is optimized, and finally, the unknown coefficients of digital cancellation have been found by a search algorithm.

Because the channel is varying during time, the analog and digital SIC have to be recalibrated if it is necessary. But the search algorithm can be very slow. To solve this problem, the gradient descent algorithm is used to reduce the time of the calibration procedure and results from the previous operating point have been used as initial value for the gradient descent algorithm.

CHAPTER 5

CONCLUSION AND RECOMMENDATIONS

This dissertation introduces an integrated quasi-circulator and integrated hybrid, RX, and baseband SI canceller to enable the full-duplex wireless communication. Both structures were designed and manufactured on CMOS technology, and their performances were measured. In this chapter, conclusion and recommendation for future works will be discussed.

5.1 Conclusions

An on-chip CMOS reconfigurable quasi-circulator, designed and fabricated in a 130 nm CMOS technology is presented in section 3. SI signal is cancelled at the LNA input as a common-mode signal and the received signal is amplified as a differential-mode signal. Reconfigurable impedance is used to compensate the antenna impedance errors to improve the SIC in the quasi-circulator. Furthermore, a leakage cancellation block is added to cancel the residual SI signal at the LNA output. The quasi-circulator has more than 90 dB SIC for a single tone transmit signal and more than 50 dB SIC for a 40 MHz modulated transmitted signal. The proposed quasi-circulator is shown to have better SIC, wider signal bandwidth, and better noise figure in comparison to state-of-the-art integrated circulators, enabling full-duplex STAR telecommunication by cancelling the high power transmitted signal and relaxing the receiver from compression point caused by the SI.

Using this structure enables full duplex for short range wireless telecommunication. To increase the transmit signal power, the second structure with an integrated high-power hybrid, mixer first RX, and baseband SI canceller is proposed.

An on-chip mixer first RX with reconfigurable hybrid and baseband SI canceller designed and fabricated on a 65 nm CMOS technology is presented in section 4 which enables the wireless full-duplex communication. SI signal is cancelled at the hybrid RX port and the received signal is conducted from the antenna to the RX as differential mode signal. Reconfigurable impedance is used to compensate the antenna impedance errors to improve the SIC in the hybrid. The hybrid shares the same antenna between the TX and the RX and can tolerate transmit the signal with 23 dBm average power and 30 dBm peak power. Furthermore, a baseband leakage cancellation block is added to cancel the residual SI signal at the RX baseband. The total analog SIC in this structure is more than 70 dB at 20 MHz bandwidth. The residue of the SI signal is cancelled in digital domain which has made the total SIC more than 113 dB. The structure shown in section 4 enables full-duplex STAR telecommunication by cancelling the high power transmitted signal and relaxing the receiver from compression point caused by the SI for the wireless telecommunication systems such as LTE.

5.2 Recommendations

This research proposed a quasi-circulator as an antenna interface for short range full duplex wireless communication and a RX with analog baseband SI canceller and hybrid for cellular full duplex wireless communication systems. To improve this system the following steps are recommended.

1. Design a new antenna interface based on time varying circuit to perform as a circulator and tolerate high power transmit signal with more than 30 dBm peak power and provide insertion loss and noise figure below 1 dB.
2. Designing and implementing an algorithm which finds the unknown parameters adaptively in a real-time signal processing system.
3. Implementing a full duplex telecommunication system with real-time signal processing.

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