Analog signal path circuit for a four transistor pixel in standard 0.13µm CMOS technology

ABSTRACT

This project is aimed to develop the layout for the analog signal path of a 4 transistor pixel CMOS image sensor using EDA tools in standard 0.13εm Silterra fabrication technology. The sub-circuit blocks that define the analog input-output path consists of the 320×240 pixel array, 320 column parallel correlated double sampling circuits, an output buffer amplifier and all associated bias circuitry. Each pixel size has a dimension of 10εm × 10εm. The pixel's frame rate is targeted to be 120 frames per second (fps) working in a QVGA picture format (320× 240 pixels). From simulation, the illumination range of 0.01 lux to 0.25 lux has been tested and shows only a 2.8% error from the ideal output linearity.

Keyword: CMOS image sensor; Slow motion video; 4T pixel; Active pixel sensors