VLSI implementation of huffman design using FPGA with a comprehensive analysis of power restrictions

ABSTRACT

Lossless compression is important in Information hypothesis as well as today's IT field. Lossless design of Huffman is most to a large degree used in the compression arena. However, Huffman coding has some limitations where it depends on the stream of symbols appearing in a file. In fact, Huffman coding creates a code with very few bits for a symbol that has a very high probability of occurrence and an utmost number of bits for a symbol with a low probability of occurrence. In this work Hardware implementation of static Huffman coding for data compression using has been designed, this hardware contains both encoder and decoder-based hardware. The proposed systems Altera DE-2 Board have been used in order to implement the text data compression. The experiments with a simulated environment and the real-time implementation for FPGA with Synopsys power analysis show that constraint has been fulfilled and the target design of the buffer length is appropriate. Power consumption that achieved by the proposed algorithm was 0.0161 mW with frequency 20MHz.and 0.1426 mW with frequency 180MHz within the design limitations. The proposed design is implemented by using ASIC and FPGA design methodologies. In order to implement the encoder and decoder architectures, 130 nm standard cell libraries was used for ASIC implementation. The simulations are carried out by using Modelsim tool. The architecture of compression and decompression algorithm design has been created using Verilog HDL language. Quartus II 11.1 Web Edition (32-Bit). In addition, simulated using ModelSim-Altera 10.0c (Quartus II 11.1) Starter Edition. And it is implemented using Altera FPGA (DE2) for real time implementation.

Keyword: Data compression; FGPA; ASIC; Binary tree; Clock; Synchronous circuit; VLSI