Crosstalk-aware multiple error detection scheme based on two-dimensional parities for energy efficient network on chip

ABSTRACT

Achieving reliable operation under the influence of deep-submicrometer noise sources including crosstalk noise at low voltage operation is a major challenge for network on chip links. In this paper, we propose a coding scheme that simultaneously addresses crosstalk effects on signal delay and detects up to seven random errors through wire duplication and simple parity checks calculated over the rows and columns of the two-dimensional data. This high error detection capability enables the reduction of operating voltage on the wire leading to energy saving. The results show that the proposed scheme reduces the energy consumption up to 53% as compared to other schemes at iso-reliability performance despite the increase in the overhead number of wires. In addition, it has small penalty on the network performance, represented by the average latency and comparable codec area overhead to other schemes.

Keyword: Coupling capacitance; Error control; Fault tolerance; Network on chip; Reliability