A framework for system dependability validation under the influence of intrinsic parameters fluctuation

ABSTRACT

This paper presents a framework to analyze and evaluate effects of cell failures induced by impact of intrinsic parameters fluctuation (IPF) on system dependability. The method of evaluation is based on generating the actual cell failures model and the realistic conditions of hardware-software interactions, where the actual error pattern can be captured. The case study of this paper is the impact of cell failures in L1 data cache of a general-purpose microprocessor. The failure modules are generated corresponding to the individual and combined impact of IPF sources in nanometer scale Ultra Thin Body – Silicon on Isolator (UTB-SOI) transistor on 6T-SRAM cell stability. A novel fault injection mechanism has been introduced to propagate errors, through modifying data of cache transactions according to error(s) incurred, dynamically at system-level. By applying a representative system workload using a well-selected suit of real benchmark programs, this study demonstrates that the framework: 1) provides an accurate user visible description for the implications of cell failures at the higher levels of abstraction induced by IPF sources at the lower levels of abstraction, 2) links individual and combined impact of IPF sources with the corresponding implications at system-level which offers a tool to systems designer to involve IPF impacts within the design plan, 3) allows for a detailed simulation process of a system-level environment in the presence of cell failures induced by IPF within an accepted period of time using the look-up file technique and thus offers a foundation to system dependability studies that require vast statistical models, 4) offers high credible evaluation results because the framework is based on the actual error pattern incurred in the system, and 5) improves system reliability where it offers valuable perceptions for an optimal fault tolerance technique in L1 cache with a high failures rate.

Keyword: Dependability evaluation; Fault tolerance; Cache memory