SILICON CARBIDE BASED DC-DC CONVERTERS FOR DEPLOYMENT IN HOSTILE ENVIRONMENTS

A THESIS SUBMITTED TO THE FACULTY OF SCIENCE,
AGRICULTURE AND ENGINEERING FOR THE DEGREE
OF DOCTOR OF PHILOSOPHY

by

Omid Mostaghimi

School of Electrical and Electronic Engineering
Newcastle University
United Kingdom

March 2015

Abstract

The development of power modules for deployment in hostile environments, where the elevated ambient temperatures demand high temperature capability of the entire converter system, requires innovative power electronic circuits to meet stringent requirements in terms of efficiency, power-density and reliability. To simultaneously meet these conflicting requirements in extreme environment applications is quite challenging. To realise these power modules, the relevant control circuitry also needs to operate at elevated temperatures. The recent advances in silicon carbide devices has allowed the realisation of not just high frequency, high efficiency power converters, but also the power electronic converters that can operate at elevated temperatures, beyond those possible using conventional silicon-based technology.

High power-density power converters are key components for power supply systems in applications where space and weight are critical parameters. The demand for higher power density requires the use of high-frequency DC-DC converters to overcome the increase in size and power losses due to the use of transformers. The increase in converter switching frequency reduces the size of passive components whilst increasing the electromagnetic interference (EMI) emissions.

A performance comparison of SiC MOSFETs and JFETs in a high-power DC-DC converter to form part of a single phase PV inverter system is presented. The drive design requirements for optimum performance in the energy conversion system are also detailed. The converter was tested under continuous conduction mode at frequencies up to 250 kHz. The converter power efficiency, switch power loss and temperature measurements are then compared with the ultra-high speed CoolMOS switches and SiC diodes. The high voltage, high frequency and high temperature operation capability of the SiC DUTs are also demonstrated. The all SiC converters showed more stable efficiencies of 95.5% and 96% for the switching frequency range for the SiC MOSFET and JFET, respectively. A comparison of radiated noise showed the highest noise signature for the SiC JFET and lowest for the SiC MOSFET. The negative gate voltage requirement of the SiC MOSFET introduces up to 6 dBμV increase in radiated noise, due to the induced current in the high frequency resonant stray loop in the gate drive negative power plane.

A gate driver is an essential part of any power electronic circuitry to control the switching of the power semiconductor devices. The desire to place the gate driver physically close to the power switches in the converter, leads to the necessity of a temperature resilient PWM generator to control the power electronics module. At elevated temperatures, the ability to control electrical systems will be a key enabler for future technology enhancements.

Here an SiC/SOI-based PWM gate driver is proposed and designed using a current source technique to accomplish variable duty-cycle PWM generation. The ring oscillator and constant current source stages use low power normally-on, epitaxial SiC-JFETs fabricated at Newcastle University. The amplification and control stages use enhancement-mode signal SOI MOSFETs. Both SOI MOSFETs will be replaced by future high current SiC-JFETs with only minor modification to the clamp-stage circuit design. In the proposed design, the duty cycle can be varied from 10% to 90%. The PWM generator is then evaluated in a 200 kHz step-up converter which results in a 91% efficiency at 81% duty cycle.

High temperature environments are incompatible with standard battery technologies, and so, energy harvesting is a suitable technology when remote monitoring of these extreme environments is performed through the use of wireless sensor nodes. Energy harvesting devices often produce voltages which are unusable directly by electronic loads and so require power management circuits to convert the electrical output to a level which is usable by monitoring electronics and sensors. Therefore a DC-DC step-up converter that can handle low input voltages is required.

The first demonstration of a novel self-starting DC-DC converter is reported, to supply power to a wireless sensor node for deployment in high temperature environments. Utilising SiC devices a novel boost converter topology has been realised which is suitable for boosting a low voltage to a level sufficient to power a sensor node at temperatures up to 300 °C. The converter operates in the boundary between continuous and discontinuous mode of operation and has a VCR of 3 at 300 °C. This topology is able to self start and so requires no external control circuitry, making it ideal for energy harvesting applications, where the energy supply may be intermittent.

To My Parents,

My Brother Amin and My Lovely Wife Behnaz

ACKNOWLEDGMENTS

I would like to express my special appreciation and thanks to my supervisors Dr Alton Horsfall and Prof. Nick Wright for their continued support throughout my studies, for encouraging my research and for allowing me to grow as a research scientist. Their advice on my research and career has been priceless.

Words cannot express how grateful I am to my parents, for all the sacrifices that they have made for me. Without their support I would never have been able to finish my thesis and their advice has been a great help to me on countless occasions during my studies. I would also like to thank Dr. Amit Tiwari and Dr. Benjamin Furnival, who as good friends and colleagues were always willing to help and give their best suggestions.

I would like to acknowledge the financial support of the EPSRC and BAE SYSTEMS through the Dorothy Hodgkin Postgraduate Award that provided the financial support for this PhD project.

I also take this opportunity to record my sincere thanks to all the academic staff of the school of electrical and electronic engineering for their help and encouragement. A number of the test fixtures used in the lab experiments were fabricated by the technicians at the school mechanical workshop, for which I would like to thank Jack, Allan, Luke, Stuart, Matt and Chris.

I would like to express my gratitude to the electronic lab technicians and supervisors: Mr. Jeffrey Warren, Mr. Darren Mackie, Mr. Paul Killan, Mr. Graham Ewart, Mr. Stephen Mitchell, Mr. James Richardson and Mr. Stephen Robson. I would also like to thank my office mates and colleagues, for their support, advice and friendship throughout my research at Newcastle University. These include but are by no means limited to: Dr Karthik Nagareddy, Dr Rupert Stevens, Dr Hua Chan, Dr Hassan Habib, Mr. Daniel Brennan and Dr Simon Barker. To those of you who I have missed I wish to apologise, however, I am sure you are aware of how grateful I am for the support you have given me. In addition, I would like to thank Dr Dave Atkinson, Prof. Volker Pickert, Dr Jonathan Goss, Dr Martin Johnston, Dr John Bennett and Dr Chris Bateman for their support, guidance and encouragement.

I would like to acknowledge the financial, academic and technical support of Newcastle University and its staff that provided the necessary support throughout my 4 years of study at Newcastle University, during my Master's and PhD programs.

I would like to gratefully thank Mr. Keith Ramsay, my favourite team leader and manager, and Mr. Gary White my colleague and friend at Mercedes AMG High Performance Powertrains for their continuous support and understanding towards the completion of my PhD. Their advice has been a great help to me on many occasions during the writing of my thesis. Last but not least, I would like to thank my other work colleagues and friends: Mr. Denis Wittich, Mr. John Robertson, Mr. Peter Conboy, Mr. George Belding, Mr. Carl Bailey, Mr. Stefano Patassa, Mr. Grant Rushton and Dr Zeng Zhaohui. They were always supporting me and encouraging me with their best wishes.

PUBLICATIONS

[1] O. Mostaghimi, N.G. Wright, A.B. Horsfall, "Design and Performance Evaluation of SiC based DC-DC Converters for PV Applications," Energy Conversion Congress and Exposition (ECCE), 2012 *IEEE*, pp. 3956-3963, 15-20, Sep. 2012.

[2] O. Mostaghimi, N.G. Wright, A.B. Horsfall, "Silicon Carbide Multilevel Converters for Grid-connected PV Applications," *Materials Science Forum*, vol. 740-742, pp. 1073-1076, Jan. 2013.

[3] O. Mostaghimi, N.G. Wright, A.B. Horsfall, "Swiching Losses in a SiC-based DC-DC Multilevel Boost Converter," *Materials Science Forum*, vol. 717-720, pp. 1241-1244, May 2012.

[4] O. Mostaghimi, R.C. Stevens, N.G. Wright, A.B. Horsfall, "Electromagnetic Interference in Silicon Carbide DC-DC Converters," *Materials Science Forum*, vol. 740-742, pp. 1044-1047, Jan. 2013.

[5] O. Mostaghimi, D.R. Brennan, R.C. Stevens, N.G. Wright, A.B. Horsfall, "A New SiC/SOI-based PWM Generator for SiC-based Power Converters in High Temperature Environments," Power and Energy Conference at Illinois (PECI), 2012 *IEEE*, pp. 1-5,24-25, Feb. 2012.

[6] D.R. Brennan, O. Mostaghimi, K.V. Vassilevski, N.G. Wright, A.B. Horsfall, "Novel SiC Self Starting DC-DC Converter for High Temperature Wireless Sensor Nodes," Sensors, 2012 *IEEE*, pp. 1-4, 28-31, Oct. 2012.

Contents

List of Figures

List of Tables

Abbreviations and Nomenclature

Abbreviation	Description	Units
τ	Time constant	s
EMC	Electromagnetic Compatibility	
T	Time period, Temperature	s, °C
GaN	Gallium Nitride	
T_{on}	On time in a period	s
T_{off}	Off time in a period	s
$T_{turn\text{-}on}$	Turn-on time	s
$T_{turn\text{-}off}$	Turn-off time	s
ESR	Equivalent Series Resistance	Ω
ESL	Equivalent Series Inductance	H
EMI	Electromagnetic Interference (Voltage)	V, dBV, dBμV
VCR	Voltage Conversion Ratio	
D	Duty cycle	
DCR	DC Resistance	Ω
V_{in}	Input voltage	V
V_{out}	Output voltage	V
f_{sw}	Switching frequency	Hz
MOSFET	Metal-oxide-semiconductor Field-effect-transistor	
JFET	Junction Field Effect Transistor	
SBD	Schottky Barrier Diode	
JBS	Junction Barrier Schottky	
CCM	Continuous Conduction Mode	
DCM	Discontinuous Conduction Mode	

PV	Photovoltaic	
MBC	Multilevel Boost Converter	
SMPS	Switched Mode Power Supply	
P	Power	W
η	Efficiency	
Q_{rr}	Reverse recovery charge	C
EM	Enhancement Mode	
DM	Depletion Mode	
PFC	Power Factor Correction	
R_{on}	On-resistance	Ω
DUT	Device Under Test	
PWM	Pulse Width Modulation	
SOI	Silicon-On-Insulator	
HT	High Temperature	
Si	Silicon	
VCO	Voltage Controlled Oscillator	
RO	Ring Oscillator	
RF	Radio Frequency	
Rs	Series resistance	Ω
t_d	Delay time	s
DIL	Dual In Line	
TIRO	Tri Inverter Ring Oscillator	
V_s	Supply voltage	V
PCB	Printed Circuit Board	
C_{in}	Input capacitance	F
C_{out}	Output capacitance	F
I_L	Inductor current	A

WSN	Wireless Sensor Node	
TEG	Thermoelectric Generator	
WBG	Wide Bandgap	
MPPT	Maximum Power Point Tracking	
IGBT	Insulated Gate Bipolar Transistor	
T_j	Junction temperature	°C
T_c	Case temperature	°C
IC	Integrated Circuit	
V_{gs}	Gate-source voltage	V
V_{ds}	Drain-source voltage	V
C_j	Junction capacitance	F
FET	Field Effect Transistor	
SOIC	Small Outline Integrated Circuit	
I_{ds}	Drain-source current	A
PTC	Positive Temperature Coefficient	
CCS	Constant Current Source	
SOB	Self-oscillating Boost	
SoC	System-on-chip	
AlN	Aluminium Nitride	
SiC	Silicon Carbide	
GaAs	Gallium Arsenide	
SIA	Semiconductor Industry Association	
ITRS	International Technology Roadmap for Semiconductors	
PHEV	Plug-in Hybrid Electric Vehicle	
HEV	Hybrid Electric Vehicle	
BJT	Bipolar Junction Transistor	

Chapter 1. Introduction

1.1 Background and Motivation

Power supply designers have been always trying to reduce the power losses in the power conversion system and hence improve system efficiency and reliability. There has also been a demand to reduce the size and weight of the power electronic converters and/or increase the output power, hence improve the system power density [1-3]. To achieve one or more of these goals, a trade-off needs to be made between size, cost, performance and power density. Depending on market demands, the most suitable solution for a specific application needs to be determined. For instance to increase the power density of a switched mode power supply, one approach is to increase the switching frequency and hence reduce the size of transformers, inductors and capacitors. This approach is; however, limited by the high switching capability of the power devices in the power conversion system. At higher switching frequencies, the switching power losses in the active devices, inductor core, winding, and dielectric increase, which leads to a reduction in power efficiency and increased device junction temperature that may affect system reliability [4].

There has been much research on the development of converter systems using new switching schemes, such as soft-switching and resonant converter structures in order to allow higher frequency high power-density converters without excessive switching losses [5-7]. These techniques; however, impose additional complications in the system design and have associated limitations with large line-voltage, load-current variations in terms of control and stabilisation. The additional control circuitry, snubber circuits, bulky resonant components and filters all need to be taken into account for accurate power-density evaluations.

On the other hand, there has been continuous development on Silicon based power semiconductor devices in order to achieve higher efficiency. Silicon as the most dominant semiconductor in the power conversion industry has now reached its theoretical limits [8]. Wide bandgap (WBG) power devices have emerged that have great potential to become the superior candidate for future power conversion systems. The devices based on WBG materials offer fast switching speeds, high break-down

voltages, high thermal conductivity and high temperature capability [9, 10]. Most of these devices are still under development, therefore thorough evaluation in currently available products are required. The cost of WBG power devices is currently higher than Silicon devices for identical voltage and current ratings. The factors affecting the higher cost of WBG power semiconductor devices are higher starting material cost, higher manufacturing cost, poor wafer yield and packaging cost. However, this can be offset by the increased energy efficiency, robustness benefits and system-level cost [11].

Among the devices based on WBG materials, SiC is the closest to commercial maturity and it has achieved highest level of commercialisation. SiC technology is capable of surviving extreme temperature environments, due to its high thermal conductivity and low intrinsic carrier concentration that is due to the wide bandgap of the material. In addition, due to the high saturation electron drift velocity, SiC devices can operate at very high frequencies. As a result of high dielectric breakdown field strength, SiC devices can be made to have a thinner drift layer and/or higher doping concentration when compared to Silicon based devices. This results in higher breakdown voltages and low on-resistance for SiC devices [12-15].

When power electronic systems operate at higher temperatures, either because of the increased power density or because of the environment, all the components and materials in the system need to withstand those elevated temperatures. If the components and packaging can tolerate these temperatures, less aggressive thermal design would be sufficient hence reduce the size and volume of the system. In addition, a higher level of power electronic integration into the associated sources or loads can be achieved due to the availability of smaller converters that operate at elevated temperatures [4].

1.2 Commercial Availability of SiC Devices

There is an increasing variety of SiC devices and it is expected to grow as the market matures. The common availability of 100mm SiC substrates has enabled the design of SiC vertical power devices in the medium and high voltage ranges. The introduction of 150mm wafers by CREE in 2012, will further reduce the device cost [16, 17]. SiC diodes have already achieved universal acceptance in many applications including the hybrid applications where SiC diodes are used as rectifiers or anti-parallel

diodes along with Si transistors. The SiC Schottky diodes are commercially available with a current rating up to 50A per device and voltage ratings in the range of 600V to 1.7kV. SiC MOSFETs have more recently joined the market and are available with a current rating up to 50A per device and voltage rating of 1.2kV and the emerging 1.7kV. SiC BJTs and JFETs are also available with a current rating up to 50A per device and voltage ratings in the range of 1.2kV-1.7kV. Normally-off JFETs were commercialised by SemiSouth; however, due to their closure in 2012, all available SiC JFETs are normally-on devices. SiC BJT and JFETs lack a gate oxide, therefore unlike MOSFETs are more suitable for very high temperature operation [18].

1.3 Research Challenges in High Efficiency, High Power Density and/or High Temperature Applications

Power conversion systems are an integrated part of the renewable energy industry. The increasing demand for high power density and high efficiency converters have been set by the accelerated growth of energy development from renewable energy sources such as photovoltaic (PV) energy systems. One of the challenges in PV systems is to link the DC renewable energy source with a multilevel inverter. The low voltage generated by the renewable energy source needs to be sufficiently boosted to feed a grid connected inverter [19, 20]. In addition, it is desired that such links are self-balanced to avoid complex control strategies [21]. It is therefore required to design a DC-DC converter to overcome such issues by connecting the input PV array to the multilevel inverter with a self-balancing output voltage and high voltage conversion ratio. This requires the use of an extremely high duty cycle which leaves no scope for voltage regulation to compensate for load and line changes. An extremely high duty cycle in a boost converter also means that the diode sustains a high amplitude current with a short pulse width, resulting in severe reverse recovery transients, which cause high electromagnetic interference (EMI) issues [22, 23].

Furthermore, recent developments in applications such as oil well exploration and aerospace have also identified the need for high density, high temperature power electronic modules. High temperature SiC DC-DC converters have great potential for deployment in such environments. To realise these power modules, the relevant control circuitry also needs to operate at elevated temperatures. For this goal to be achieved,

these parts need to operate at temperatures exceeding 175 ºC with limited cooling strategies [24-26]. The desire to place the gate driver physically close to the SiC power switches in the converter, leads to the necessity of a temperature resilient PWM generator to control the power electronics module [27-30]. As far as the gate driver is concerned, traditional complementary CMOS integrated circuits based on Silicon, can only operate reliably at temperatures below 125 ºC. The development and realisation of integrated converter modules capable of high temperature operation is therefore quite challenging.

SiC based switches such as SiC JFETs are capable of tolerating these elevated temperatures, however, various other components such as passives, magnetics or amplifiers will make this task rather challenging. From a system point of view, the gate drive requirements of normally-on SiC JFETs are a significant challenge. The issue with the start-up process in addition to the differences in the gate voltage requirements make them less desirable for power designers [31, 32]. The gate driver needs to address these design constraints, and also enables fast switching speeds of the device at high temperature. To operate DC-DC converters in high temperature environments, the gate driver needs to rectify the short circuit issue with the SiC JFET start-up and also drive the switch during normal running conditions at elevated temperatures. The simplicity of the design is key when considering the availability of high temperature components.

1.4 Thesis Objectives

One of the objectives of this thesis is to investigate the applications of SiC devices in high power density applications considering high frequency operation, thermal performance, efficiency and noise evaluation. Therefore the performance evaluation of SiC devices in a high power density power converter is required with a detailed comparison to the Si based design. This investigation also needs to consider high power-density systems requiring high voltage conversion ratios.

In addition, to enable a full high-temperature power conversion system, a high temperature PWM generator is desired. The objective is to realise a demonstrator circuit using all-high temperature switching devices offering a wide duty cycle range. Finally, to fully utilise the high-temperature capability of SiC devices in hostile environment where the converter needs to supply a wireless sensor node from a thermoelectric

generator, a SiC DC-DC converter with large voltage conversion ratio is desired. The converter can only use high temperature SiC devices without a need for control electronics, to achieve small size and high reliability.

1.5 Thesis Outline

The thesis will begin with a review of the roadmap of semiconductor devices followed by a review on wide bandgap materials. The resilient properties of SiC, as the most mature wide bandgap semiconductor material, will be detailed. Semiconductor devices based on SiC will be discussed with regards to their requirements and limitations. A roadmap of DC-DC power conversion technology as a key part of the power engineering will be briefed. Currently available literature with regards to high temperature and high efficiency applications of SiC converters in power converter systems will be detailed. Furthermore, high power density converter systems, high voltage conversion ratio requirements and multilevel DC-DC converters will be discussed. The review will be situated in chapter 2, preceding the technical data, which is presented in the following manner:

Chapter 3

This chapter will begin with the design of a pre-regulator DC-DC converter as part of a high power-density inverter system. The design criteria of the converter and the gate drive circuits for different Si and SiC transistors will be detailed. The converters efficiency, thermal performance and radiated noise at various conditions will be evaluated and compared for SiC MOSFET, SiC JFET and Si MOSFET based designs. A transformer-less SiC based multilevel boost converter will also be presented that offers high efficiency, high voltage conversion ratio and low noise, that can directly feed a 3-level clamped inverter circuit.

Chapter 4

This chapter will begin with a review of the requirements of a gate drive circuit suitable for operation in high temperature environments beyond those possible using conventional silicon-based. This will be followed with a PWM generator design that uses normally-on SiC JFETs fabricated at Newcastle University. The SiC/SOI-based

PWM generator based on six functional blocks will be discussed. A ring oscillator in the design enables a wide range of frequency tuning suitable for the operation of SiC-based DC-DC converters.

Chapter 5

This chapter will begin with a review of power sources used for wireless sensor nodes. The investigation then moves towards the use of energy harvesting in high temperature applications. As in practical applications, the low voltage of the thermoelectric generator is insufficient to support the drive for remote sensor applications, a novel SiC step-up DC-DC converter will be proposed. The converter operation will be detailed and the simulation and experimental results will be discussed. The proposed boost converter design offers high voltage conversion ratios at extremely high ambient temperatures.

Finally, conclusions will be drawn from the technical data and possibilities for future work will be discussed in Chapter 6.

1.6 References

[1] J. W. Kolar, et al., "PWM Converter Power Density Barriers," in Power Conversion Conference - Nagoya, 2007. PCC '07, 2007, pp. P-9-P-29.

[2] M. Pavlovsky, et al., "Pursuing high power-density and high efficiency in DC-DC converters for automotive application," in Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, 2008, pp. 4142-4148.

[3] W. G. Homeyer, et al., "Advanced power converters for More Electric Aircraft applications," in Energy Conversion Engineering Conference, 1997. IECEC-97, Proceedings of the 32nd Intersociety, 1997, pp. 591-596 vol.1.

[4] J. Kassakian and T. Jahns, “Evolving and emerging applications of power electronics in systems,” IEEE J. Emerging Sel. Topics Power Electron., vol. 1, no. 2, pp. 47–58, Jun. 2013.

[5] D. Fu, F. C. Lee, Y. Qiu, and F. Wang, “A novel high-power-density three-level LCC resonant converter with constant power-factor-control for charging applications,” IEEE Trans. Power Electron, vol. 23, no. 5, pp. 2411–2420, Sep. 2008.

[6] J. Zhang, J. S. Lai, R. Y. Kim, and W. Yu, “High-power density design of a soft-switching high-power bidirectional dc-dc converter,” IEEE Trans. Power Electron., vol. 22, no. 4, pp. 1145–1153, Jul. 2007.

[7] B.-C. Kim, K.-B. Park, C.-E. Kim, B.-H. Lee, and G.-W. Moon, “LLC resonant converter with adaptive link-voltage variation for a high-power density adapter,” IEEE Trans. Power Electron., vol. 25, no. 9, pp. 2248–2252, Sep. 2010.

[8] R. Singh and M. Pecht, “Commercial impact of silicon carbide,” IEEE Ind. Electron. Mag., vol. 2, no. 3, pp. 19–31, Feb. 2008.

[9] J. Millan, et al., "A Survey of Wide Bandgap Power Semiconductor Devices," Power Electronics, IEEE Transactions on, vol. 29, pp. 2155-2163, 2014.

[10] K. Shenai, et al., "Rugged Electrical Power Switching in Semiconductors: A Systems Approach," Proceedings of the IEEE, vol. 102, pp. 35-52, 2014.

[11] K. Shenai, "Future Prospects of Widebandgap (WBG) Semiconductor Power Switching Devices," Electron Devices, IEEE Transactions on, vol. 62, pp. 248-257, 2015.

[12] J. Biela, et al., "SiC versus Si-Evaluation of Potentials for Performance Improvement of Inverter and DC-DC Converter Systems by SiC Power Semiconductors," Industrial Electronics, IEEE Transactions on, vol. 58, pp. 2872-2882, 2011.

[13] P. G. Neudeck, et al., "High-temperature electronics - a role for wide bandgap semiconductors?," Proceedings of the IEEE, vol. 90, pp. 1065-1076, 2002.

[14] D. Han, J. Noppakunkajorn, and B. Sarlioglu, "Comprehensive efficiency, weight, and volume comparison of SiC and Si-based bidirectional DC-DC converters for hybrid electric vehicles," IEEE Trans. Veh. Technol., no. 99, pp. 1-1, 2014.

[15] J. A. Cooper, Jr., M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, “Status and prospects for SiC power MOSFETs,” IEEE Trans. Electron. Devices, vol. 49, no. 4, pp. 658–64, Apr. 2002.

[16] J. W. Milligan, S. T. Sheppard, W. Pribble, Y.-F. Wu, S. Muller, and J. W. Palmour, “SiC and GaN wide bandgap device technology overview,” in Proc. IEEE Radar Conf., Apr. 2007, pp. 960–964.

[17] Cree Introduces 150-mm 4HN Silicon Carbide Epitaxial Wafers [Online]. Available: http://www.cree.com/News-and-Events/Cree-News/Press-Releases/2012/August/150mm-wafers.

[18] H. A. Mantooth, M. D. Glover and P. Shepherd, “Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems,” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 374–385, Mar. 2014.

[19] S. V. Araujo, et al., "Highly Efficient High Step-Up Converter for Fuel-Cell Power Processing Based on Three-State Commutation Cell," Industrial Electronics, IEEE Transactions on, vol. 57, pp. 1987-1997, 2010.

[20] C. Shih-Kuen, et al., "Novel High Step-Up DC-DC Converter for Fuel Cell Energy Conversion System," Industrial Electronics, IEEE Transactions on, vol. 57, pp. 2007-2017, 2010.

[21] R. Davoodnezhad, et al., "A Novel Three-Level Hysteresis Current Regulation Strategy for Three-Phase Three-Level Inverters," Power Electronics, IEEE Transactions on, vol. 29, pp. 6100-6109, 2014.

[22] E. H. Ismail, et al., "High Conversion Ratio DC-DC Converters With Reduced Switch Stress," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 55, pp. 2139-2151, 2008.

[23] L. Huber and M. M. Jovanovic, "A design approach for server power supplies for networking applications," in Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE, 2000, pp. 1163-1169 vol.2.

[24] X. Zhuxian, et al., "Investigation of Si IGBT Operation at 200 ºC for Traction Applications," Power Electronics, IEEE Transactions on, vol. 28, pp. 2604-2615, 2013.

[25] W. Zhiqiang, et al., "A High Temperature Silicon Carbide mosfet Power Module With Integrated Silicon-On-Insulator-Based Gate Drive," Power Electronics, IEEE Transactions on, vol. 30, pp. 1432-1445, 2015.

[26] M. A. Huque, et al., "Silicon-on-insulator-based high-voltage, high-temperature integrated circuit gate driver for silicon carbide-based power field effect transistors," Power Electronics, IET, vol. 3, pp. 1001-1009, 2010.

[27] J. Valle-Mayorga, et al., "High-Temperature Silicon-on-Insulator Gate Driver for SiC-FET Power Modules," Power Electronics, IEEE Transactions on, vol. 27, pp. 4417-4424, 2012.

[28] H. Kosai, et al., "Design and Performance Evaluation of a 200 ºC Interleaved Boost Converter," Power Electronics, IEEE Transactions on, vol. 28, pp. 1691-1699, 2013.

[29] S. Waffler, et al., "High temperature (200°C) isolated gate drive topologies for Silicon Carbide (SiC) JFET," in Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE, 2008, pp. 2867-2872.

[30] V. Bondarenko, et al., "SiC devices for converter and motor drive applications at extreme temperatures," in Aerospace Conference, 2006 IEEE, Big Sky, 2006.

[31] K. Mino, et al., "A gate drive circuit for silicon carbide JFET," in Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE, 2003, pp. 1162-1166 Vol.2.

[32] S. Round, et al., "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter," in Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005, 2005, pp. 410-416 Vol. 1.

Chapter 2. Literature Review

2.1 Roadmap of Semiconductor Devices

In 1965, Gordon E. Moore presented a paper stating that the number of integrated components per Integrated Circuit would increase exponentially over time [1]. This vision, known as Moore's Law has been used in semiconductor industry for more than 5 decades to set targets for research, development and long-term planning. Through transistor scaling, a better performance to cost ratio is obtained which results in an exponential growth of the market for semiconductor devices. In return, this allows further investments in novel technologies, which will allow further scaling. This idea then became a roadmap in semiconductor industry [2, 3].

All these scaling trends have been enabled by significant R&D investments and to guide these research and development programs, the semiconductor industry association (SIA), started the international technology roadmap for semiconductors (ITRS) in 1999; to improve the quality of research investment decisions and to particularly focus on the areas where research breakthroughs are needed [4].

Si semiconductor technology, of course, is based on the most mature semiconductor material; however, due to recent development advances, it has approached its theoretical limits. Performance requirements of power electronic circuits, however, have increased dramatically up to a point that Si based semiconductor power devices cannot function. These requirements include higher efficiency, switching frequency, blocking voltage and reliability. Wide bandgap semiconductors have superior characteristics that can potentially offer performance improvements over their Silicon counterparts [5-7].

2.2 Wide Bandgap Semiconductors

WBG semiconductor materials such as silicon carbide (SiC), gallium nitride (GaN), Gallium Arsenide (GaAs) and diamond, have significantly better electrical properties in comparison to Silicon. The higher bandgap means that they can operate at

higher temperatures. Higher electric breakdown field in WBG materials results in semiconductor devices with higher breakdown voltages. Due to their higher thermal conductivity, WBG materials can conduct heat to their surroundings more quickly, hence the device temperature increases more slowly [8-12]. The higher electron mobility and electron saturation velocity of WBG devices allows higher frequency operation. The key material characteristics are summarised in table 2.1 [13].

	Semiconductor Materials						
	Si	GaAs	3C-SiC	6H-SiC	4H-SiC	2H-GaN	Diamond
Bandgap (eV)	1.12	1.43	2.4	3.0	3.2	3.4	5.6
Electron Mobility ($cm^2V^{-1}s$)	1350	8500	1000	500	950	400	2200
Thermal Conductivity ($Wcm^{-1}K^{-1}$)	1.5	0.6	5.0	5.0	5.0	1.3	20.0
Critical Electric Field ($MVcm^{-1}$)	0.25	0.3	2.0	2.5	2.2	3.0	5.0

Table 2.1: Key electrical parameters of bulk Si and a range of popular wide bandgap materials

Diamond has the widest bandgap of the commercially available semiconductors and consequently has the highest electric breakdown field compared with the commonly available polytypes of SiC or GaN. The data in the table shows that SiC and GaN have very similar bandgap and electric breakdown field values, which are significantly greater than GaAs and Si. The higher electric breakdown field means that more doping can be applied to the semiconductor material and so the breakdown voltage limits of WBG materials, will increase further, in comparison to silicon. Diamond has approximately five times higher thermal conductivity than the commercially available polytypes of SiC, whilst GaN has the poorest thermal conductivity, even lower than Si [14, 15].

Diamond is the hardest material and requires highest temperatures for processing. Even though diamond shows the best theoretical performance, process technology is still immature. Whilst it has been demonstrated at a research level for

field emission devices and sensors, power devices are not currently available. GaN has a thermal conductivity approximately one fourth of that observed in SiC. Growing GaN on SiC wafers improves the overall thermal conductivity, but the performance cannot compete with that observed in bulk SiC wafers. GaN JFETs are now commercially available, however the devices are normally on and so are being manufactured with a cascode structure that has an internal Si MOSFET to allow enhancement mode gate control [16]. Transphorm Inc. holds fundamental patents in the area of GaN power conversion, but at the present time, the voltage rating of their available devices is limited to 600V. Higher thermal conductivity combined with wide bandgap and high electric breakdown field make SiC semiconductor devices the most suitable candidates for applications in harsh environments where the high temperature and high power density are key requirements.

2.3 SiC Technology and Material Properties

In terms of process technology, SiC is the most mature wide bandgap semiconductor. As outlined above, the properties of SiC make it an excellent choice for high frequency, high temperature and high power applications. SiC has a large number of polytype structures, a detailed summary of which can be found in [17]. However, not all the two hundred possible polytypes are easy to grow and the most popular ones are the cubic 3C, hexagonal 4H and hexagonal 6H structures. The number indicates the stacking sequence and the letter shows the geometrical form of the crystal structure.

The higher bandgap of SiC common polytypes (3.2, 3 and 2.4 eV for 4H-SiC, 6H-SiC and 3C-SiC, respectively) compared with the 1.1 eV bandgap of Silicon enables SiC based devices to operate at temperatures beyond 500 °C [18-20]. The approximately 10 times higher electric breakdown field of SiC material compared with Si, enables the conduction region to be reduced, hence a very low specific on resistance can be achieved. The greater saturation velocity of all three common SiC polytypes, than that of Si (1.10^7 cm/s), results in higher frequency operation.

Modified seeded sublimation growth was the first breakthrough by Tairov and Tzvetkov in 1978, to realise reproducible 6H Silicon Carbide crystal growth [21]. They produced high purity substrates; hence the SiC wafer was born. In 1989, the first 1-inch

6H polytype wafers became commercially available. Because of the higher carrier mobility and lower anisotropy, the 4H SiC polytype is the preferred choice for the realisation of power semiconductor devices [22]. In 1993, CREE provided the 1-inch 4H-SiC wafers to the market. Along with higher quality wafers and significant improvements in epitaxy, continuous enhancement of SiC wafer continues. Today, for the n-type substrates, the 4-inch wafers are the main product on the market, however the supply of the 6-inch n-type wafers is catching up rapidly. The price ratio between 6 and 4-inch n-type substrates are still significant, although decreasing rapidly therefore the 6-inch wafers are not yet appealing for device manufacturers [23]. SiC device sales and their predictions for the coming years according to Yole Développment are shown in figure 2.1 and the data shows the application of SiC technology to a wide range of industrial sectors.

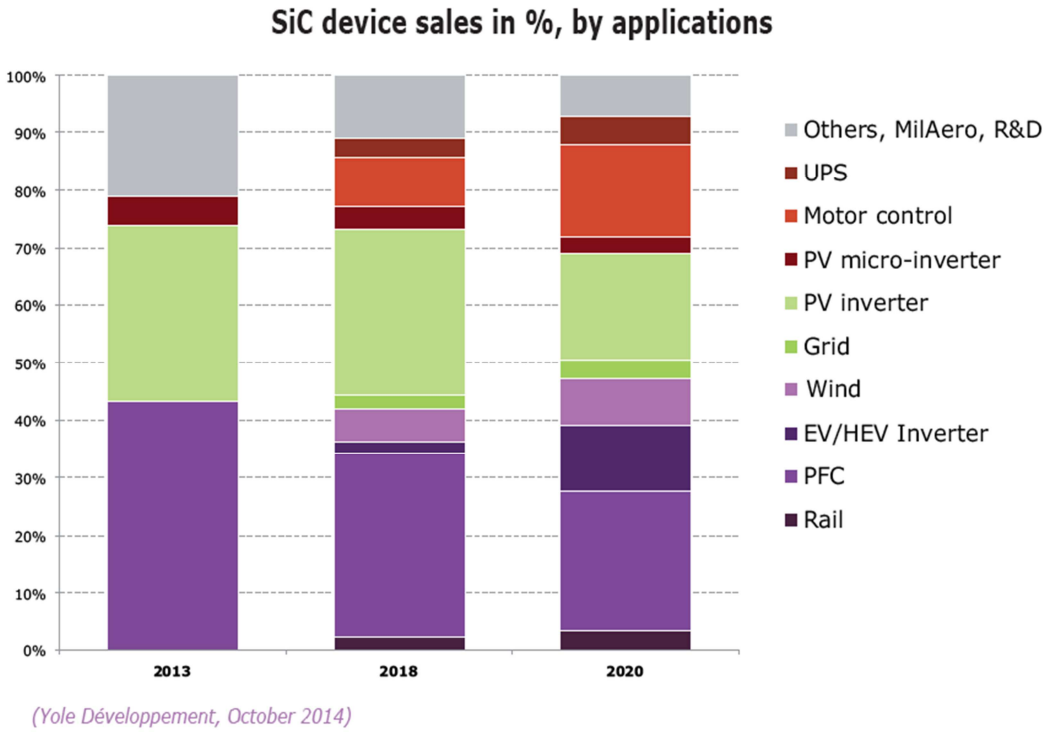


Figure 2.1: Percentage of SiC device sales based on applications [23]

2.4 Power Switching Devices Based on SiC

Silicon carbide technology has advanced significantly since the foundation of CREE in 1987. Even though there was a number of material problems in the early wafers, including screw dislocations and micropipes that limited the die size, the first Silicon carbide power semiconductor devices, SiC Schottky diodes, were

commercialised offering 600V blocking voltage, twice that of the Si Schottky diodes (300V)[24]. In addition to SiC Schottky diodes, many other power devices have been researched and commercialised including PiN diodes, JFETs, MOSFETS, thyristors, GTOs, BJTs and IGBTs. The use of these SiC power devices instead of Si counterparts leads to system level advantages such as reduced power losses, reduced size and volume and increased efficiency [25]. It has been shown that replacing Si devices with SiC devices in a traction drive application resulted in increased efficiency and reduced cooling requirements to one-third, in a hybrid electric vehicle [26]. However, when in addition to the reduced power losses, size and volume of the heatsink, the effect of switching frequency is considered, a DC power supply will have proportionally smaller filters and transformers as the switching frequency increases. Figure 2.2 shows progress in the commercial availability of SiC based bipolar and unipolar devices [27].

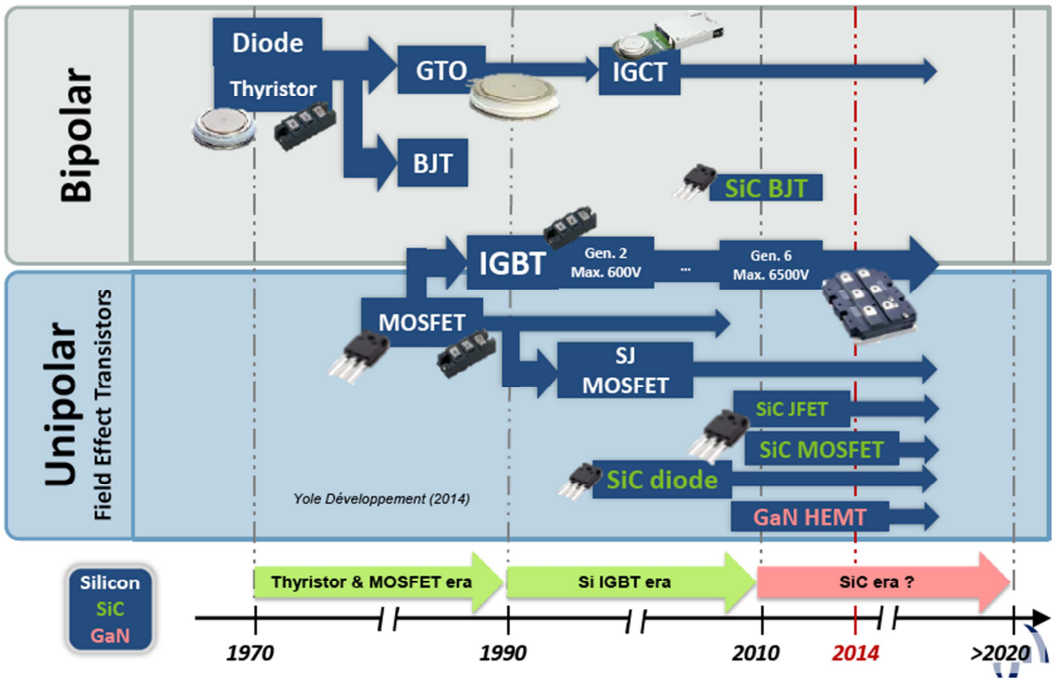


Figure 2.2: Availability of bipolar and unipolar semiconductor devices [27]

2.4.1 SiC Diodes

SiC Schottky diodes were the first commercialised SiC power semiconductor devices, introduced by Infineon in 2001 [28]. The main advantage of SiC Schottky diodes is the elimination of reverse recovery charge (Q_{rr}) that is the dominant cause of the switching losses in bipolar Silicon PiN power diodes. Unlike PiN diodes, Schottky

diodes are majority carrier devices hence they do not require a reverse recovery current to discharge the minority carriers in the depletion region [28].

Minimised switching and conduction power losses are required in high performance power converter applications. To reduce the conduction loss of the power Schottky diode without compromising the device blocking voltage, the Schottky barrier height can be reduced. This, however, causes higher leakage currents during the reverse bias of the power diode.

Junction barrier Schottky (JBS) diodes can have lower leakage than conventional Schottky diodes for the same blocking voltage [29]. JBS structures are not commonly used in Si Schottky diodes. This is because the threshold of the PiN junction is only 0.7V, which can potentially make the device operate in bipolar mode when the P-N junction turns on together with the Schottky barrier junction for a higher bias voltage. Due to wider bandgap of Silicon carbide, the threshold of the SiC P-N junction is around 3V. Consequently, the P-N junction does not turn on during forward conduction [29]. Currently, commercial SiC Schottky diodes are available from a number of manufacturers including Cree, Infineon, Microsemi, IXYS, Rohm and STMicroelectronics.

2.4.2 SiC MESFET

A number of research groups have demonstrated MESFET technology, including DERA and NASA. Based on SiC-based metal-semiconductor field-effect transistors (MESFETs), NASA have demonstrated logic gates operating at 600º C [30]. AC amplifiers based on SiC MESFETs and ceramic packaging operating at 500º C were fabricated using CREE SiC wafers [31]. Although there are increasing demands for using SiC MESFETs in microwave applications, there are surface trapping issues with SiC MESFETs in these applications, therefore various types of passivation materials have been used to improve the surface properties [32]. The majority of research into SiC MESFETs is to develop transistors for GHz frequency range of radio frequency (RF) applications and hence are not suitable for power applications where the devices tend to operate in hundreds of kHz range.

2.4.3 SiC SIT

Static-induction-transistors (SITs) are normally-on devices; therefore require a negative gate voltage to turn off. These devices are unique in the way that they can operate in both unipolar and bipolar modes. Therefore the circuit designer can choose to use either the high frequency or high current capability [33]. Recently there has been some research on SiC SITs used as circuit breakers. These devices demonstrate both a very low on resistance and the large energy-absorption capability required during the interruption process [34]. SiC SITs can also reduce the level of overvoltage during the current interruption phase and this can be achieved by controlling their gate-voltage without the need for additional suppressors such as varistors [35].

2.4.4 SiC BJT

Due to its low current gain and small safe operating area (SOA), caused by the second breakdown issue, the Si bipolar junction transistor (BJT) was replaced in power electronic circuits by Si power MOSFETs and IGBTs many years ago. Since then there has been no significant research work on Si BJTs. However, the use of SiC material with its excellent properties has led to the introduction of SiC BJTs for high voltage and high power applications [36]. These devices are normally off and have positive temperature coefficient (PTC) for the on-resistance of the device. They are free from gate oxide, offering the potential for high reliability and provide very fast switching speeds. TranSiC has developed 1200V SiC BJTs that perform better than 1200V Si IGBTs and do not exhibit the Si IGBT second breakdown phenomenon [36].

There have also been reports on improved common emitter current gain in SiC BJTs. For the same collector current, this means that the device requires a lower base current, therefore reducing the drive power losses. The design criteria and drive requirements for SiC BJTs are totally different form Si based BJTs. There are no issues with storage times at turn-off in SiC based devices [37]. When the device is in on-state, the device base current needs to be continuously provided by the drive circuitry and for example, a 30A SiC based device with a gain of 60 requires a continuous 0.5A current flowing in to the base.

2.4.5 SiC IGBT

Due to the distribution voltage levels in smart-grid applications, Si based IGBTs, which are commercially available at voltage ratings up to 6.5kV, are either utilised in series or are used in multilevel power converter structures. These limitations add to the complexity of the converter topology and the control schemes [38]. Therefore there has been a significant amount of research to develop SiC devices with voltage ratings in excess of 10kV. 4H-SiC MOSFETs rated at 10kV have been developed offering high switching frequencies (beyond 20 kHz) and low on-state resistance. However, SiC MOSFETs similar to Si based MOSFETs exhibit increased drift resistance at higher voltages, which worsens significantly with increasing temperature [38]. Due to the technological challenges in preparing low-resistivity p-SiC substrates, p-IGBT was demonstrated before the n-IGBT. However, with the progress in SiC fabrication capability and wafer growth technology, the n-type SiC device has been demonstrated offering better switching performance and on-state losses compared to the SiC p-type IGBTs [39, 40].

2.4.6 SiC JFET

The manufacturing of junction devices is comparably easier than MOSFET devices. The fabrication of a high performance reliable silicon carbide / silicon dioxide interface is still a significant challenge. Currently, There are normally-on and normally-off SiC JFETs under development or commercially available. The normally-on SiC JFET requires a negative gate voltage to be fully turned off against the rated blocking voltage of the device. There are reliability concerns associated with using these devices, for example in many boost or bridge power converters, the design relies on the switching device being off during start-up. If the gate drive circuitry fails, the use of normally-on devices leads to a short circuit condition and a number of techniques have been proposed to protect against these reliability and failure mode issues [41, 42]. There has also been a great deal of research on normally-on SiC JFET devices used in a so called cascade structure operating along with a low voltage Si MOSFET therefore the device can be switched as a normally-off device [43]. A normally-on JFET with high voltage rating can also be used along with a low voltage normally-off JFET as a compound switch that operates as a normally-off switch [44].

Although the cascode structure solves the challenge of the normally-on characteristics of the device, it adds to the complexity of the design. In addition, the low voltage FET needs to handle the full load current of the high voltage normally-off JFET, which adds to the overall conduction losses. Using the low voltage Si device in the cascade design also results in thermal limitation of the compound package. Several circuit designs have been proposed to directly drive the normally-on devices; these avoid the thermal limitations associated with the Si device as well as its added conduction losses [45].

Despite the above-mentioned design issues, the normally-on SiC JFETs offer high temperature capabilities, extremely low on-resistance and very fast switching speeds. These devices are particularly suitable for solid-state bi-directional circuit breaker applications where the on-state of the device equates to the no-fault operating mode of the system. In these fault protection systems, the device operates in on-state condition for the majority of time; this hence increases the system reliability as the normally-on SiC JFETs do not need an active gate bias for operation in their nominal current conduction [46-48].

The normally-off SiC JFETs first introduced by SemiSouth, are more preferred devices compared to the normally-on SiC JFETs. To fabricate a normally-off JFET, either a very lightly doped or a thin channel is required; this is difficult to achieve reliably [49]. In order to improve R_{ds}(on), the gate voltage has to be large enough that leads to gate diode activation. As a result, a DC current is supplied by the gate drive circuitry during on-state, causing additional power losses within the drive circuit. An approach to minimise the power dissipation is to use an AC coupled gate driver with a non-centred dual power supply; depending on the choice of the driver, there are duty cycle and/or switching frequency limitations [50]. Similar to normally-on devices, the normally-off SiC JFETs also show very low on-resistance, low intrinsic capacitances and fast switching speeds.

2.4.7 SiC MOSFET

SiC MOSFETs offer lower conduction power losses when compared to similarly rated Si MOSFETs. If the SiC MOSFET is designed with low specific on-resistance, it can also be fabricated with lower switching losses than its Silicon counterparts. The main elements that control the power device switching speed are the device

capacitances. The capacitance per unit area in the SiC MOSFET structure is approximately 10 times higher than an equivalent planar Si based MOSFET [51]. To counteract this greater capacitance density, the SiC devices needs to operate at greater current densities than their comparable Si based devices. This hence requires these devices to be fabricated with low specific on-resistance. Therefore, both the specific on-resistance and the device capacitances need to be minimised to fully realise the device performance.

The first SiC MOSFET was reported in the late 1980s and the first power MOSFET based on Silicon carbide was then reported in 1994 [52]. In 2011, CREE released the first commercially available SiC MOSFET. This device was rated at 33A and 1200V, offering the possibility of high power density converters operating with switching speed. Despite the high temperature capability of SiC, this device is conservatively rated at 125º C, due to concerns over the threshold voltage stability, long term reliability issues and constraints from the packaging. The reliability of the gate oxide is the most common concern for SiC MOSFETs. Under voltage and temperature stresses, both threshold voltage shift and time dependant dielectric breakdown problems have been reported in the literature [53-55].

2.5 Roadmap of DC-DC Converters

DC-DC power conversion technology has been a key part of the power engineering and has been under development for more than sixty years. In the 1920s, the technique of the DC-DC power conversion was established [56]. The DC-DC converter in its simplest form was a voltage divider with an output voltage lower than its input voltage and with a low efficiency. The second step in DC-DC conversion was the multiple-quadrant chopper. Choppers directly convert a fixed DC input voltage to a variable output voltage.

Before the Second World War, basic DC-DC converters were used in industrial applications. Although research on this topic was discontinued during the war, the applications for DC-DC power converter were recognised. After the war, due to the need for low voltage DC power sources, DC-DC conversion techniques developed rapidly [56]. There are hundreds of DC-DC converter topologies that have been demonstrated, all designed to meet the specifications and requirements of certain

applications. These converters are usually named based on their function. For instance, the boost converter outputs a higher voltage than the input voltage, whilst the output voltage of a buck converter is lower than its input voltage. The DC-DC converter classification was formalised in 2001 and it has been used ever since [56]. Based on this principle, a DC-DC converter can therefore be allocated into its respective category based on its function and technical features.

2.5.1 Classification of Main DC-DC Converter Topologies

DC-DC converters can be categorised into 6 generations as shown in figure 2.3. The first generation converters are the classical DC-DC converters including the fundamental converters, transformer-type converters, developed converters and voltage-lift and super-lift converters [56, 57].

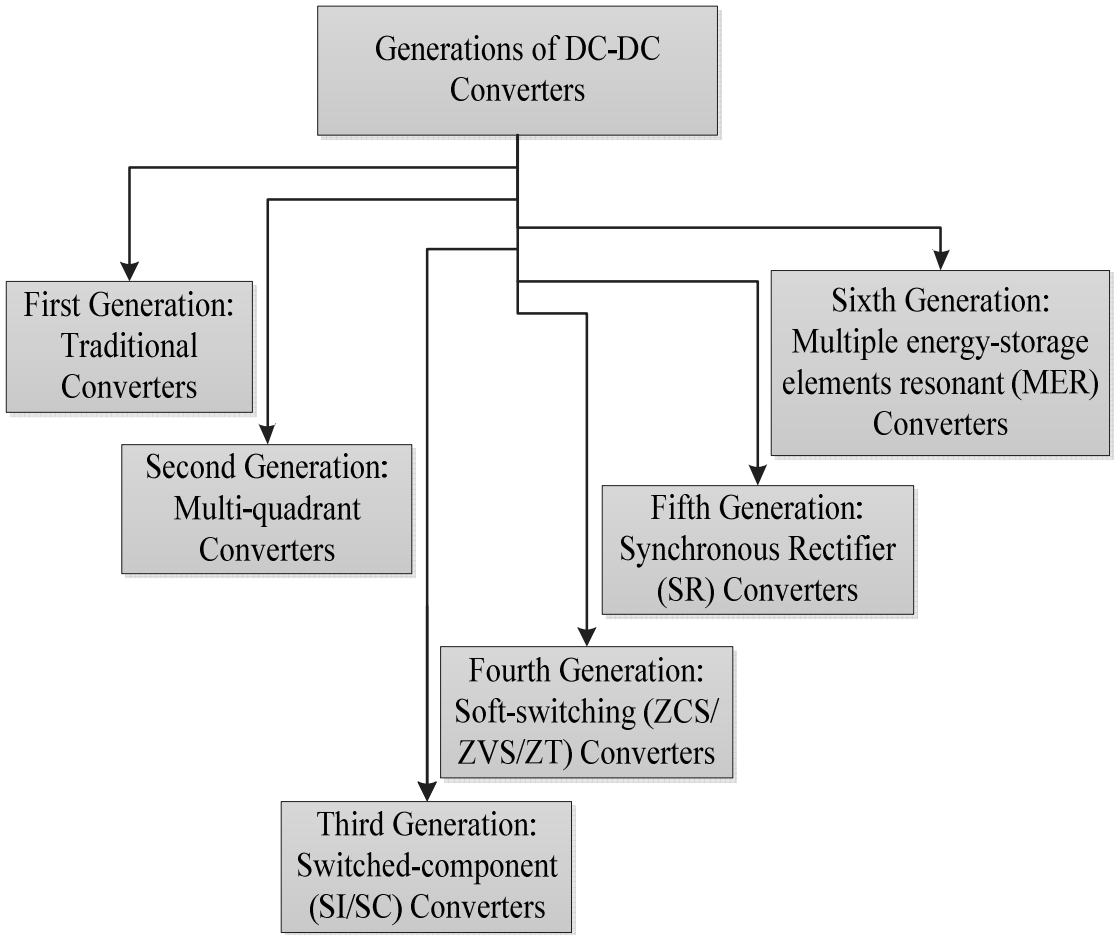


Figure 2.3: Generations of DC-DC converter topologies

2.5.2 The Traditional Converters

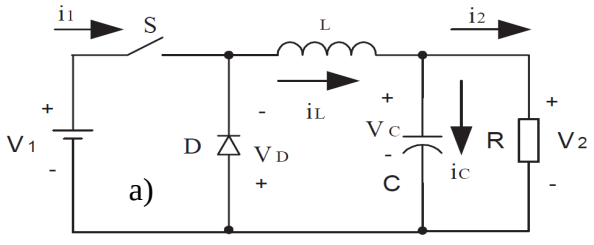
2.5.2.1 The Fundamental Converters

The fundamental converter topologies are buck, boost and buck-boost DC-DC converters. The circuit diagram of the buck, boost and buck-boost converters are shown in figures 2.4 (a), 2.4 (b) and 2.4 (c), respectively. The buck (step-down) converter is a DC-DC converter that regulates the output voltage to a lower level than its input voltage. The current through the inductor increases when the switch is in the on-state. When the switch is off, the diode conducts and the inductor current decreases as the stored energy in the output inductor drops. As the output inductor reduces the output current ripple, the output capacitor directly limits the ripple in the output voltage. The output voltage of the buck converter is calculated using equation 2.1, where $T = 1/f$ is the switching period, t_{on} is the switch on-state time, and $D = t_{on}/T$ is the duty cycle.

$$V_o = \frac{t_{on}}{T} V_{in} = DV_{in} \tag{2.1}$$

The boost (step-up) converter is a DC-DC converter that regulates the output voltage at a level greater than its input voltage. The energy stored in the input inductor increases when the switch is in the on-state. When the switch is off, the diode conducts and the current flows from the input-source through the inductor to the load. The input voltage source in series with the input inductor behaves like a current source. As both the discharge-current in the inductor and the input voltage source are supplying the load during the switch off-state, the voltage across the load is larger than the input voltage. As there is no inductor in the output, the output capacitor needs to be sufficient to reduce the output voltage ripple and maintain a constant output voltage [58, 59]. The output voltage of the boost converter is calculated using equation 2.2.

$$V_o = \frac{T}{T - t_{on}} V_{in} = \frac{1}{1 - D} V_{in} \tag{2.2}$$



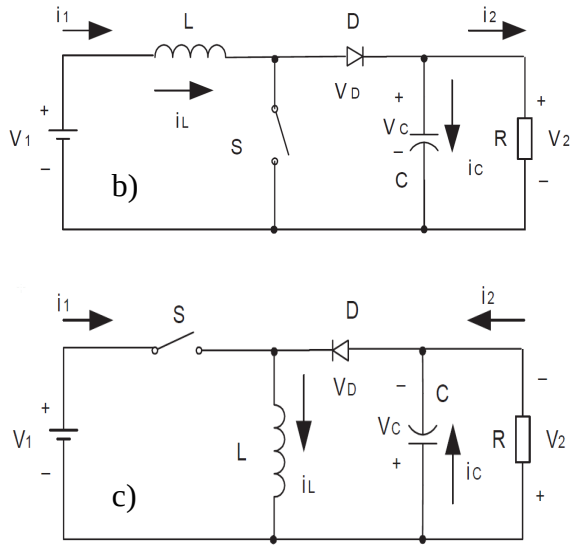


Figure 2.4: Buck converter circuit diagram (a), boost converter circuit diagram (b) and buck-boost converter circuit diagram (c) [56]

The buck-boost converter is a DC-DC converter that can regulate the output voltage at a level lower or greater than its input voltage. Here, depending on the duty cycle, the converter can act as a boost or buck converter. When the switch is off, the diode conducts and the inductor limits the output current ripple. The output capacitor can directly limit the output voltage ripple similar to the buck converter. The output voltage polarity in the buck-boost converter is the opposite of that of the input voltage. The output voltage of the buck-boost converter is calculated using equation 2.3.

$$V_o = -\frac{t_{on}}{T-t_{on}} V_{in} = -\frac{D}{1-D} V_{in} \quad (2.3)$$

2.5.2.2 The Transformer-type Converters

The transformer-type converters were developed in the 1960s-1980s. These converters maintain a link between the primary and secondary of the converter, providing galvanic isolation between both sides. The converters such as half-bridge, full-bridge, fly-back, forward, push-pull and Zeta converters are among the transformer-type DC-DC converters. The voltage conversion ratio, the ratio of the output voltage to input voltage, of these converters are high and depends on the transformer turns ratio and duty cycle of the DC-DC converter.

The Zeta converter is an isolated converter with a low-pass filter, resulting in a small voltage ripple in the output [56]. The forward and push-pull converters are buck-derived converters whereas the fly-back converter is a buck-boost derived topology. The forward converter has a switch and uses a tertiary winding to help the demagnetisation of the transformer core. The push-pull converter has two switches with a centre-tapped transformer resulting in twice the output voltage and avoiding the transformer core saturation when compared with the forward converter. Half-bridge converters are constructed to deploy only the primary winding. The circuit diagram of the bridge DC-DC converter is shown in figure 2.5. The circuit has two more switches compared to the half-bridge and has a gain twice that of the half-bridge. The output voltage of the bridge converter is calculated using equation 2.4, where N is the transformer turn ratio.

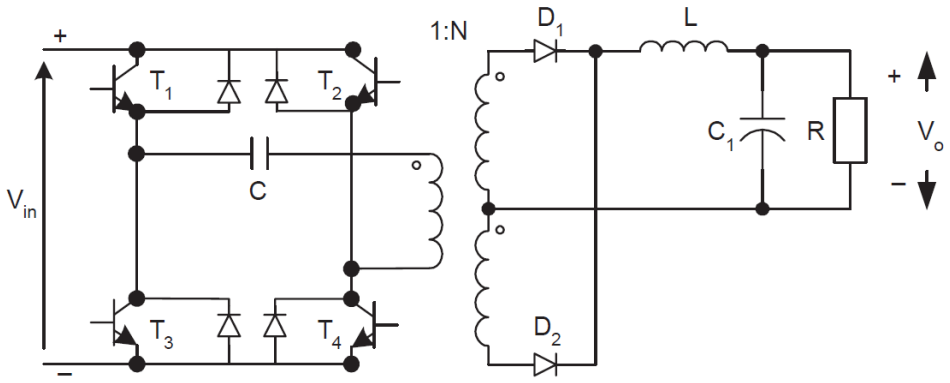


Figure 2.5: Bridge converter circuit diagram [56]

$$V_o = 2DNV_{in} \tag{2.4}$$

If there is a need for multiple outputs, multiple secondary windings with associated conversion circuit may be constructed to satisfy such requirements. A forward DC-DC converter with primary tertiary winding and three outputs is shown in figure 2.6. Each output voltage is calculated using equation 2.5, where N_i is the transformer turn ratio between primary winding and each of the secondary windings.

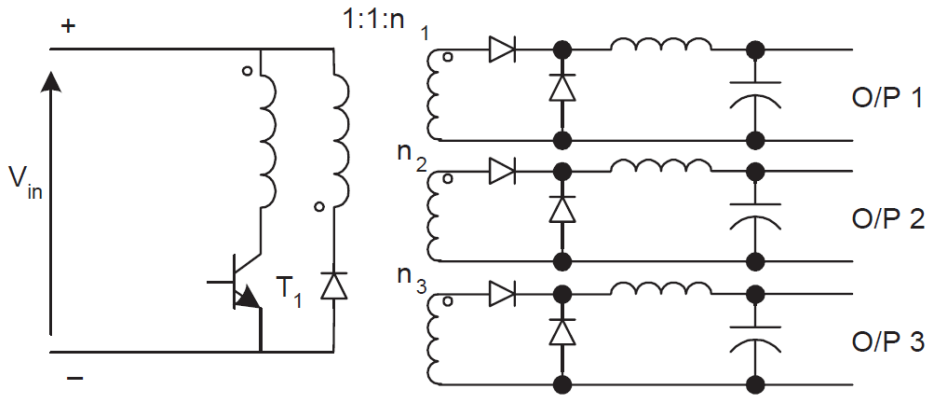


Figure 2.6: Forward converter with three outputs [56]

$$V_o = DN_i V_{in} \tag{2.5}$$

2.5.2.3 The Developed Converters

The first demonstration of this converter topology was published in 1977. This type of converter gives an improvement on the performance of the fundamental DC-DC converters, with the addition of a low-pass filter. Some of these converters are the Watkins-Johnson converter, SEPIC (single-ended primary inductance) converter, Cuk converter and positive output Luo-converters [56, 57]. These converters have small output ripple and the output voltage of these converters is calculated using equation 2.6.

$$V_o = \frac{D}{1-D} V_{in} \tag{2.6}$$

2.5.2.4 The Voltage Lift and Super Lift Converters

Voltage lift converters are series of DC-DC converters that were developed to realise high voltage gain topologies, including self-lift and high-stage lift converters [56]. The super lift converters with a novel approach enhance the voltage gain of the converters even further. Positive output super lift Luo converters are among the super lift converter topologies. One of the sub-series of the positive output super Luo converters is the main series. In an n stage circuit, there is a switch, n inductors, 2n capacitors and (3n-1) diodes [57]. A triple-lift circuit from the main series is shown in figure 2.7. The output voltage of the triple-lift converter is calculated using equation 2.7. The equivalent triple-lift converter from the voltage lift converters requires two switches and it also results in a lower voltage gain of 3/(1-D).

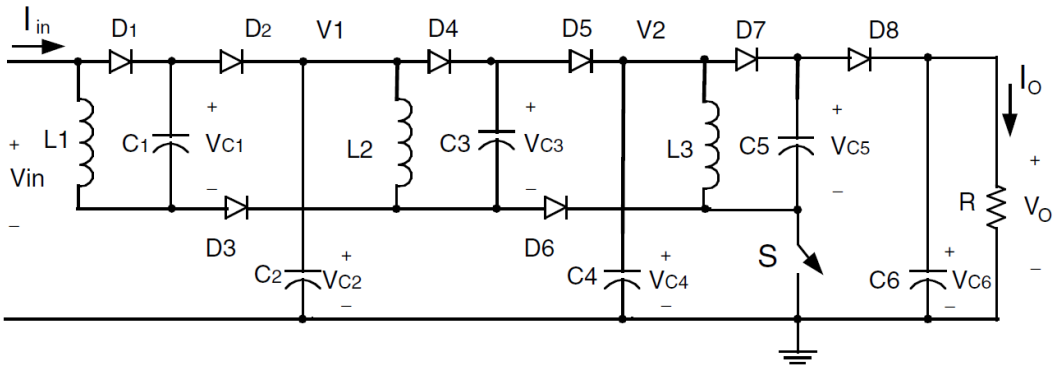


Figure 2.7: Triple-lift converter from the super lift converter topologies [56]

$$V_o = \left(\frac{2-D}{1-D}\right)^3 V_{in} \quad (2.7)$$

2.5.3 The Multi-quadrant Converters

The traditional converter topologies, including the buck converter operate in a single quadrant. For instance a DC motor is required to function in 4 quadrants as shown in figure 2.8. The supply of power to a DC motor is realised by means of an H-bridge (full-bridge) converter topology. The circuit shown in figure 2.9 is a 4-quadrant Luo-converter [60]; a less-known alternative 4-quadrant topology. During mode 1 energy is transferred from source (V_1) to load (V_2) and during mode 2 energy is transferred from load (V_2) to source (V_1). During mode 3 energy is transferred from source (V_1) to load ($-V_2$) and during mode 4 energy is transferred from load ($-V_2$) to source (V_1).

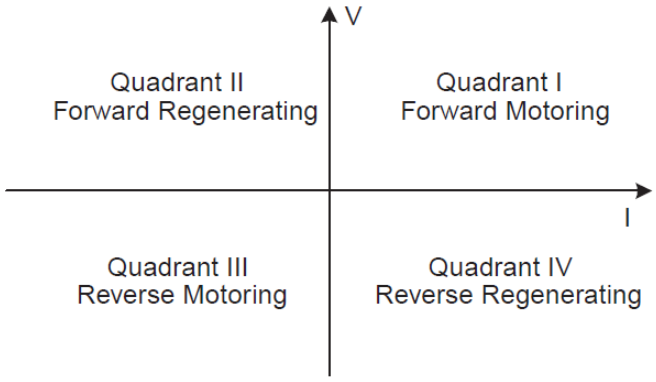


Figure 2.8: 4-quadrant operation

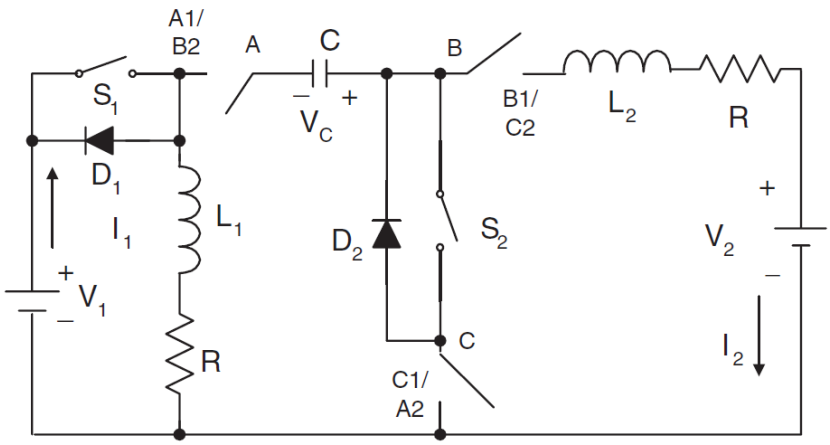


Figure 2.9: 4-quadrant Luo DC-DC converter [60]

2.5.4 The Switched Components Converters

These converters use either inductors or capacitors and are therefore called switched-inductor converters or switched-capacitor converters. Switched capacitor converters are small and have low electromagnetic interference and are therefore suitable for integration into integrated circuits. Although switched capacitor converters have many advantages, to achieve a high voltage gain, a large number of capacitors are required and the control circuits are complex [56].

2.5.5 The Soft Switching Converters

This generation of converters are called soft-switching converters. The three main classifications are the zero voltage switching (ZVS), zero current switching (ZCS) and zero transition (ZT) converters. Zero transition technique implements both the zero voltage switching and zero current switching (ZV-ZCS) techniques. These techniques focus on how to minimise power losses during the turn-on, turn-off or both transitions [56].

2.5.6 The Synchronous Rectifier Converters

The development in microelectronics requires power supplies with high currents and low output voltages. Recalling the buck converter in section 2.5.2, at low output voltages, the switch duty cycle is lower and so the diode has a longer conduction time. A synchronous rectifier is a semiconductor switch that replaces a diode and improves the efficiency of the converter system by reducing the conduction loss in a switched

mode converter. The soft switching techniques can be applied to synchronous converters [56].

2.5.7 The Multiple Energy-storage Resonant Converters

Resonant converters with more than one energy-storage element were developed to increase the power conversion efficiency at high power levels. The energy-storage elements are inductors and capacitors and can be connected in a variety of configurations. The higher the number of elements, the greater the number of possible converter topologies. Different arrangements have been examined to produce soft switching operation with nearly sinusoidal waveforms [56] to achieve high efficiency and power density.

2.6 Modes of Operation

Depending on the inductor current, the operation of DC-DC converters can be described in terms of two distinct modes, continuous conduction mode (CCM) and discontinuous conduction mode (DCM). CCM occurs when the inductor current is always a non-zero value. CCM is used for highly efficient applications with high quality semiconductor switches while requiring a larger inductor when in comparison with DCM operation. DCM occurs when the inductor current is zero for a portion of the switching cycle. The boundary between the continuous and discontinuous modes of operation is called critical or boundary conduction mode (BCM). Generally speaking, discontinuous and critical conduction modes are used in lower powered applications where the converter module can tolerate the large peak currents. DCM is utilised in applications that require special control strategies, such as battery chargers. The order of the system becomes less than that for CCM, due to the fact that the energy in the inductor becomes zero at the beginning and end of a cycle and there is a time interval where the inductor is neither charging nor discharging [58].

DCM and CCM are not generally utilised together in a system because they have different control strategies. The high frequency, high amplitude current ripple observed in the DCM converter leads to an increase in both conducted and radiated Electromagnetic Interference (EMI), requiring a larger filter on the output. The advantage of using the DCM is the simplified circuit design, as well as reducing the

reverse recovery problems in DC-DC converters due to the fact that the diode reverse recovery occurs under zero-current time interval [61]. Consequently, the critical mode of operation can result in acceptable EMI levels, whilst reducing the filter requirements and reducing the switching device stresses and high frequency current ripple [62]. A converter based on BCM is considered as a variable frequency system. If the peak currents are large and the inductor current slope during the switch off-time is rather flat, the switching period is extended. The converter controller observes the current in the inductor and when zero current is detected, the switch is turned on immediately [63].

In power factor correction (PFC) circuits based on boost converters, BCM is used to switch the MOSFET on with a zero current in the Si diode, enabling a zero current switching (ZCS). This strategy, however results in higher peak currents and variable operating frequency. Interleaved BCM converters were proposed to reduce the peak currents offering phase-shifted BCM converters. Significant efforts have been made to reduce the effects of the reverse recovery characteristics of the diode in the boost converter of the front end PFC systems and many soft-switching boost converters have been proposed to control the turn-off current of the boost diode [62-64]. The introduction of SiC Schottky diodes and their use in high power PFC boost converters has enabled the realisation of high efficiency CCM converters without the need for the associated snubber circuits used in traditional soft-switched PFC circuits [64].

2.7 Power Losses in Active Devices

To achieve high efficiency converters, it is vital to identify the location of any power losses and how they are generated. Power losses in the active devices include contributions from both the static and dynamic power losses. Static losses include the on-state losses, and dynamic losses are the switching transient losses that consist of the turn-on and turn-off power losses.

2.7.1 Diode Static and Dynamic Power Losses

The diode conduction loss is proportional to the series resistance and forward voltage-drop. This loss can be expressed by equation 2.8 when the power loss during reverse bias operation can be considered as insignificant. Here, I_F is the diode average current and I_{RMS} is the diode RMS current. Both the forward voltage and series

resistance are temperature dependant parameters and need to be taken into consideration during the loss calculation at different temperatures.

$$P_{conduction} = R_D I_{RMS}^2 + V_F I_F \tag{2.8}$$

There are different temperature dependencies for Silicon and Silicon carbide diodes. Due to different temperature coefficients, the series resistance of the Si diode decrease with temperature whereas the series resistance of the SiC Schottky diode increases with temperature [65]. The larger bandgap and higher doping density of SiC results in a higher forward voltage-drop for the SiC device than a similarly rated Si p-i-n based device. In addition, the forward voltage-drop of the SiC diode increases with temperature, due to its positive temperature coefficient. Although this temperature dependence increases the conduction losses in the SiC diodes at high temperatures, SiC diodes are easier to parallel in higher current applications [65]. The temperature dependence of the on-state characteristics for a Si and SiC diode is shown in figures 2.10 (a) and 2.10 (b).

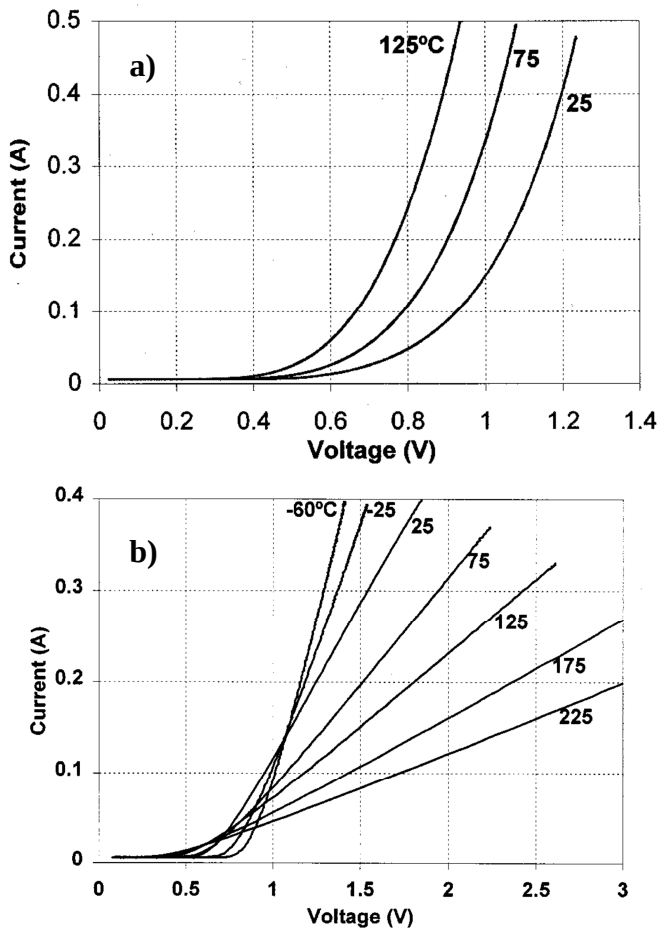


Figure 2.10: On-state characteristics of an ultrafast Si PiN diode (a) and a SiC diode (b) at different temperatures [65]

The majority of the switching losses in a diode are due to the reverse recovery loss. At high frequencies the turn-off process becomes even more critical. The diode can be switched off only when the stored charge in the depletion region is removed. The SiC diode does not have the reverse recovery current, because the majority carrier operation does not require carrier recombination. Therefore the turn-off current is dominated by the displacement current that charges the parasitic capacitance between the anode and cathode of the SiC Schottky diode [66]. As this reverse displacement current does not change with temperature, the switching losses of the SiC diode are not greatly affected by changes in temperature [67]. The Si and SiC diode turn-off current waveforms at different temperatures are shown by the data in figures 2.11 (a) and 2.11 (b). In addition, the negligible switching losses of SiC diodes make them suitable for use in high frequency power converters.

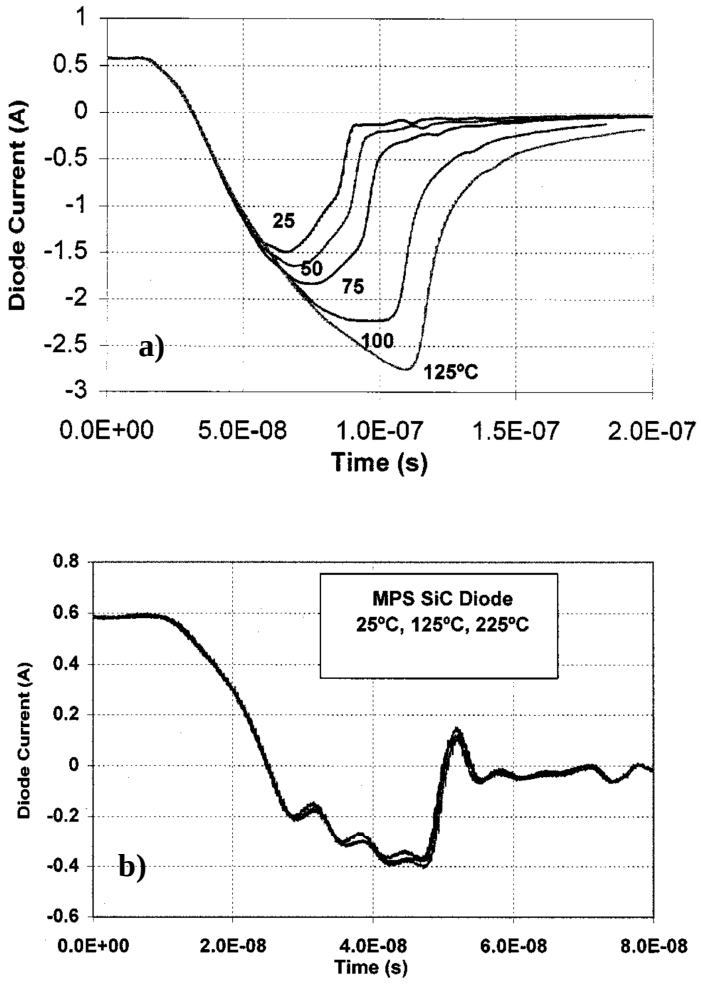


Figure 2.11: Reverse recovery current of an ultrafast Si PiN diode (a) and a SiC diode (b) at different temperatures [65]

The characterisation of Si and SiC diodes in a hard-switching and soft-switching DC-DC converter was shown in [68]. The experimental results showed that the soft-switching converter utilising Si diode had improved efficiency over the hard-switched Si based converter, due to the reduced switching losses. Therefore, the use of soft-switching in the Si converter allowed operation at higher switching frequencies.

The soft-switching converter based on a SiC diode, however, showed only a marginal reduction in power losses when compared to the hard switched SiC converter. This is because the power losses of the SiC diode are dominated by conduction losses hence the soft-switching techniques have minimal effect. This indicates that SiC diodes can be used at very high switching frequencies even in hard switching converters and this also eliminates the need for soft switching and the resulting additional complexity [69].

2.7.2 FET Static and Dynamic Power Losses

Similar to diode, the power losses in the FET consist of contributions from both conduction and switching losses. The FET conduction loss is a product of the series resistance and forward current. This loss can be expressed as shown in equation 2.9, where I_{RMS} is the diode RMS current and R_{ds} (on) is the FET drain to source resistance. The drain-source resistance of a FET is a temperature dependant parameter and needs to be taken into account during the loss calculation at different temperatures.

$$P_{conduction} = R_{ds(on)} I_{RMS}^2 \tag{2.9}$$

The on-resistance per unit area is higher for Si MOSFETs with higher breakdown voltages, because of the increased distance between the source and drain contacts. This is why Insulated Gate Bipolar Transistors (IGBTs) have become the transistor of choice for higher voltage applications. Si IGBTs offer lower on-resistance than Si MOSFETs, due to the high level of minority carriers injected into the drift region. This also results in a tail current at turn-off that increases the turn-off switching losses of the Si IGBTs.

Due to the reduction in drift-layer resistance for devices with an identical voltage rating, SiC MOSFET devices offer lower on-resistance than Si devices and do

not show the tail current. Therefore they have significantly lower switching losses than the Si IGBTs [70, 71]. In addition, the on-resistance of the state-of-the-art Si MOSFETs has a relatively high positive temperature coefficient, which has a direct impact on the conduction loss and thermal design at elevated temperatures.

The data in [72] shows that the on-resistance, R_{ds} (on), of the SiC MOSFET increases by only 20% when the junction temperature increases from 25 ºC to 150 ºC. In contrast, the R_{ds} (on) of the Si SJMOSFET increases by 250% when the junction temperature increases to 150 ºC. In addition the SiC MOSFET shows a significantly lower off-state leakage than an equivalent Si device. For example, at 150 ºC, the SiC MOSFET has 20 times lower leakage current than the Si MOSFET. At 200 ºC the leakage current of the Si MOSFET increases significantly to a level where the power dissipation becomes excessive and the Si device fails [72]. The SiC MOSFET also showed significant reduction of both turn-on and turn-off losses when compared to Si IGBT.

As described previously the use of SiC Schottky diodes reduces the diode switching losses by significantly reducing the turn-off transition loss. The diode turn-off loss has also a direct impact on the transistor turn-on power loss. The data in [73] shows that replacing a Si ultrafast diode with a SiC Schottky diode in a hard-switched Si IGBT application reduces the diode switching power loss by 80% and the IGBT switching loss by 50%. As shown in figure 2.12 (a), a clamped inductive circuit was used for the device performance evaluation. As can be seen in figure 2.12 (b) during turn-off, the Si diode has a 23A peak reverse recovery current and a 100ns recovery time.

In addition there is a 200V overshoot as a result of fast di/dt during this transition. The SiC diode has a 4A peak reverse recovery current and a 33ns recovery time, as can be seen from the data in figure 2.12 (c). The SiC diode only needs to dissipate a small capacitive charge and does not experience any voltage overshoots during the turn-off transition. When the IGBT turns on, the inductor current is transferred from the diode to the IGBT. The diode turn-off transition current and reverse recovery time have a significant impact on the IGBT turn-on transition.

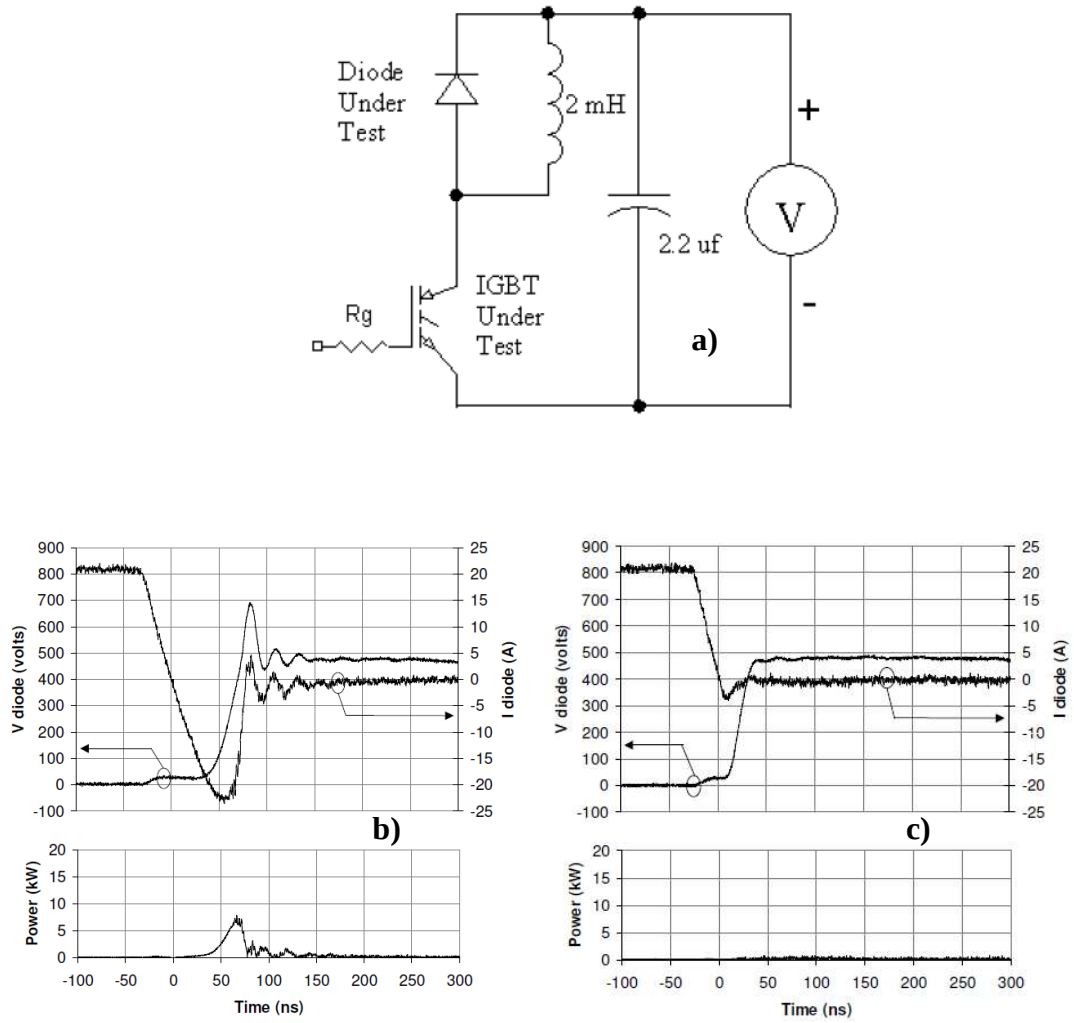


Figure 2.12: Clamped inductive circuit for device evaluation (a) 600V Si ultrafast diode turn-off current, voltage and instantaneous power waveforms at 150 ºC (b) 600V SiC diode turn-off current, voltage and instantaneous power waveforms at 150 ºC (c) [73]

Figures 2.13 (a) and 2.13 (b) show the turn-on voltage, current and instantaneous power waveforms for the IGBT with a Si and SiC diode respectively, operating at 150 ºC. During turn-on the reverse recovery current of the diode is added to the IGBT turn-on current waveform and results in an IGBT peak current of 44A and 22A for the Si and SiC diodes, respectively. The peak instantaneous power dissipated in the IGBT during turn-on transition is reduced from 15kW to 7.5kW. There are also high frequency oscillations in the IGBT turn-off current waveforms for the case with Si ultrafast diode, which cause the generation of significant levels of electromagnetic interference [73].

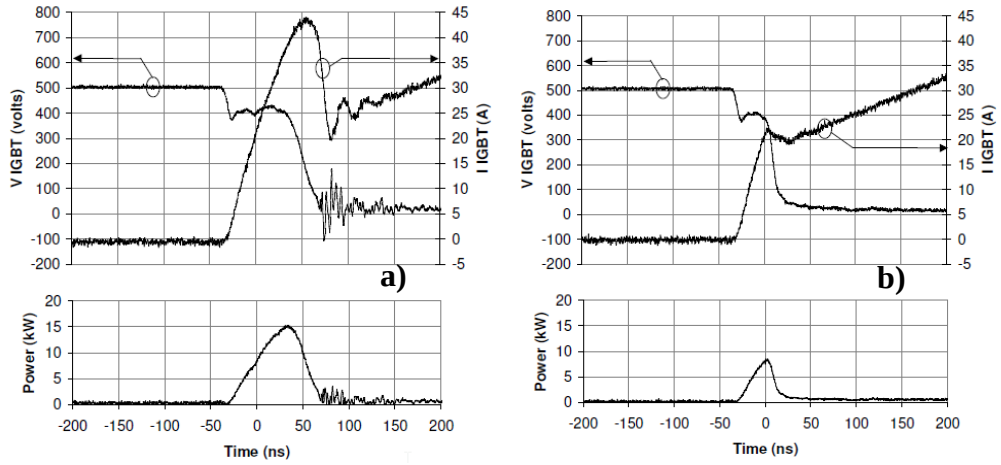


Figure 2.13: IGBT turn-on current, voltage and instantaneous power waveforms at 150 ºC for Si ultrafast diode (a) IGBT turn-on current, voltage and instantaneous power waveforms at 150 ºC for SiC diode (b) [73]

2.8 SiC Converters for High Efficiency and High Temperature Applications

As discussed earlier in the chapter, the continuous development of SiC based semiconductor devices has been a key enabling factor for the realisation of high efficiency power electronic converters. A significant level of research has been performed to evaluate the performance of the converter system using these semiconductor devices. This includes applications of SiC based semiconductors in AC/DC, DC/AC, AC/AC and DC/DC power converters.

In [74], a 600 kHz 92% efficient CCM boost PFC circuit is presented that utilises a Si MOSFET and a SiC diode, resulting in reduced EMI filter and inductor size when compared with the Si based PFC circuit. A two-stage 1 MHz PFC is also proposed that achieved 93% efficiency with 60% size reduction in the EMI filter and 90% reduction in the size of the boost inductor compared with a 100 kHz Si based PFC circuit. In [75], the use of Si IGBTs instead of SiC JFETs in a SWISS rectifier (shown in figure 2.14) resulted in the switching losses increasing by a factor of 1.5. The total chip area for the SWISS rectifier with Si IGBTs and SiC diodes also increased significantly compared to the SiC JFET based implementation.

In [76], the Si IGBT of a single-phase PFC demo circuit was replaced with a normally-off SiC JFET, with the only other component change being the gate driver

circuit. This change resulted in a efficiency gain of 1.25% due to faster switching times and lower losses of the SiC JFET. In [77], the Si MOSFET and Si diode of a single phase PFC circuit were replaced by a SiC DIMOSFET and a SiC SBD resulting in the MOSFET total power loss decreasing from 53W to 18W, due to the reduced conduction and switching losses. In [78], the performance of a 1 MHz 250W PFC boost converter was evaluated using SiC BJT, SiC MOSFET and Si CoolMOSFET devices. Both the SiC MOSFET and SiC BJT based converters showed higher efficiencies than the Si based converter. The SiC MOSFET based converter had the highest efficiency of 91.5%, 2.2% more than that of the Si MOSFET based converter.

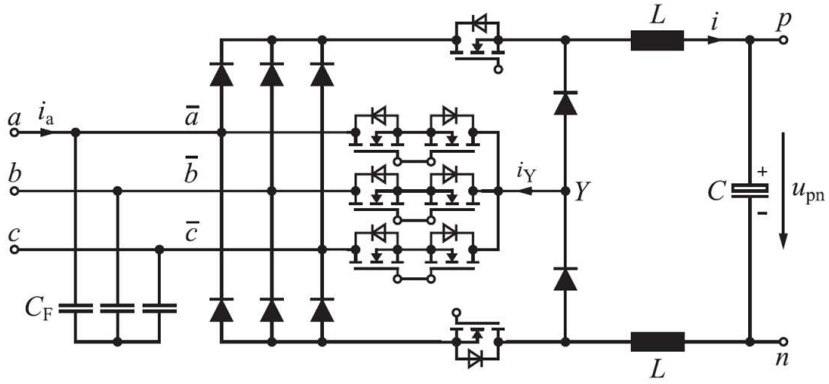


Figure 2.14: SWISS rectifier with unidirectional power flow [75]

A 47kW hybrid inverter based on Si IGBT and SiC Schottky didoes was presented in [79] and compared with an all-Si inverter. The inverter based on SiC diodes showed lower inverter power losses and less stress on the main switches, enabling the use of higher switching frequency operation. A 60kW motor drive system based on SiC MOSFETs was realised and compared with a Si IGBT drive system in [80]. The overall power loss of the SiC based inverter is one third of that of the Si IGBT inverter. Using the same heatsink, the output power of the SiC inverter is 187% of the Si based inverter. In [81], a 1200V 800A all-SiC dual power module was presented that utilises 80A SiC MOSFETs and 50A SiC Schottky diodes as shown in figure 2.15. The module was tested in a full-bridge configuration and operated at junction temperature of 153 ºC. A SPICE model extracted from experimental data was created to simulate an inverter system based on SiC power devices. The results showed a 40% loss reduction in the SiC inverter when compared to the Si based inverter system. In addition the SiC power module was shown to have the ability to run at switching frequencies four times higher than those of that based on equivalent Si power devices.

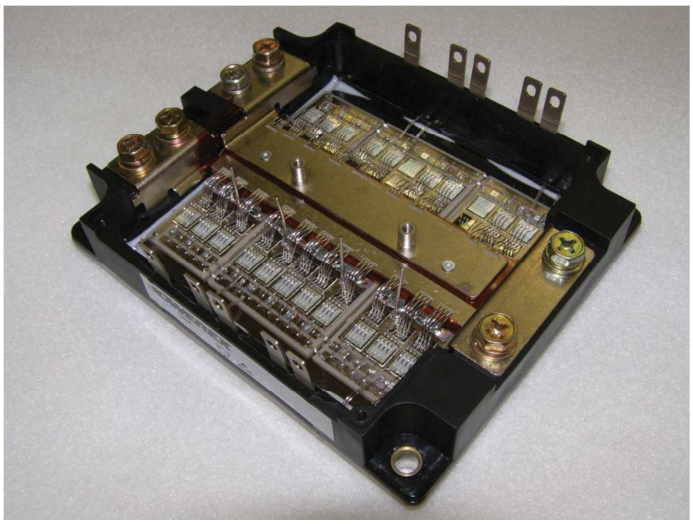


Figure 2.15: 800A power module based on SiC MOSFETs and SiC Schottky diodes [81]

In [82], a SiC based 1200V 100A six-pack inverter power module designed for 200 ºC operation in a hybrid electric vehicle (HEV) application was presented. The module used normally-on SiC JFETs and SiC anti-parallel Schottky diodes. The liquid-cooled SiC inverter module showed an efficiency of 98.5% at 10 kHz switching frequency, 5kW output power and at coolant temperatures up to 95 ºC.

Four three-phase PWM ac-ac power converter topologies based on SiC diodes and SiC JFETs were presented in [83] and the impact of switching frequency on the power density was studies for all the four front-end converters. Thanks to the high-frequency capability of SiC devices, the topologies with lightest total weight for the given specification were identified. The work in [84] presented an evaluation of Si and SiC devices in a matrix converter topology. The converter based on SiC JFETs showed the highest efficiency while the converter based on Si IGBTs had the lowest efficiency. The SiC JFET showed the lowest turn-on loss and the SiC BJT showed the lowest turn-off loss among the switching devices studied. The Si IGBTs showed the highest turn-on and turn-off switching losses. In [85] normally-off SiC JFETs were used in an indirect matrix converter topology to achieve a power density of 72 kVA/litre. The matrix converter showed an efficiency of 96.7% at 80% of its nominal output power.

In [86] SiC Schottky diodes were compared with Si diodes in a 2.5kW DC-DC interleaved boost converter operating with a switching frequency of 16 kHz. The use of SiC diodes resulted in an improved efficiency and a reduction in cooling system requirements of the interleaved boost topology. In [87] the performance of a SiC JFET

operated in a cascode configuration in a DCM boost converter topology is presented. The converter was reported to have an efficiency of 97.5% at 600W output power and a switching frequency 1 MHz. SiC MOSFETs were evaluated in a hard-switched 6kW 200 kHz pump-back converter, where a buck converter feeds a boost converter and the boost converter feeds the common bus [88]. The use of SiC MOSFET reduces the overall power losses by a factor of at least 2 when compared to Si super junction MOSFETs. Similarly in [89] the use of SiC MOSFETs in a 300W soft switching full bridge resulted in 1%-4% efficiency improvements. In [90] SiC BJTs and SiC JFETs were compared in a modular multilevel converter. The SiC JFET based converter showed a better performance than the SiC BJT based converter; primarily because the SiC BJT requires a higher driver current, hence increasing the overall power losses in the system.

There are also applications where converters are expected to function in elevated ambient temperatures, such as those commonly found in automotive and aerospace applications. A 120 ºC ambient temperature automotive inverter using SiC Schottky diodes and normally-off SiC JFETs was presented in [26], where the junction temperature of SiC devices reached 250 ºC. In [91] an 800 kHz 1kW boost converter based on a SiC Schottky diode and a SiC MOSFET was presented where the SiC MOSFET junction temperature reached 320 ºC. In [92], a 74 kHz 2kW interleaved boost converter based on SiC Schottky diodes and SiC JFETs was presented that functioned in ambient temperatures between 20 and 200 ºC. Here the converter gate driver was placed outside the temperature controlled chamber. In [93] a Silicon-on-insulator (SOI) gate driver was proposed capable of operation between -50 ºC and 200 ºC, making it suitable for a range of automotive and aerospace applications. In [67] the high temperature capability of a SiC Schottky diode and a SiC JFET in a 25W buck converter was assessed. The SiC devices were placed in an oven were tested from 25 ºC up to 450 ºC, significantly beyond the maximum operating temperature of Si based devices. The results show that the current rating of the SiC JFET decreases to 20% of the room temperature value at 450 ºC, due to the reduction in electron mobility. Additionally, the series resistance and forward voltage-drop of the SiC diode increase with temperature. As the gate drive circuit was a Si based design, the gate driver was placed outside the temperature controlled oven during the tests and so did not influence the observed changes in converter operation with temperature.

2.9 High Power Density Converters

Power electronic converters are not designed to only address the electrical design specifications, size and weight requirements also need to be taken into account during the design phase. High power density has become a key metric in the development of high performance power converters [94]. The reduced converter volume demand is based on the physical constraints of a specific application. For instance, the space under the bonnet in a hybrid electric vehicle demands a low volume converter design [95], or in aerospace applications where the weight is a major factor that directly affects the mission profile and aircraft operational capabilities [96].

The power density of the converters has improved significantly since the 1990s, due to the development of high power IGBTs and MOSFETs with fast switching capabilities, and the development of fast recovery power diodes that reduce the turn-on power losses of the IGBTs and MOSFETs [97]. As outlined previously, due to their superior electrical properties, SiC devices can achieve very fast switching speeds and low power losses, and can function at elevated temperatures. The high switching frequency operation of the SiC devices in standard voltage-source inverter does not affect the power density of the inverter. Instead, the converter cooling system can be reduced, due to lower overall power losses [98]. However, in DC-DC converters, the increased switching frequency with low switching losses enables a reduction in size for the passive components, including the inductors and transformers [99]. In [100], a SiC high power density, high efficiency on-board battery charger for electric vehicle (EV) and plug-in hybrid electric vehicle (PHEV) applications was presented as shown in figure 2.16. The system is a two-stage power conversion architecture including a bridgeless boost converter and a phase-shifted full-bridge converter switching at 200 kHz. The use of SiC power devices resulted in an efficiency of 95% with a volumetric power density of 5kW/L. The SiC based full-bridge multichip power module (MCPM) based on CREE SiC MOSFETs and Schottky diodes was designed by APEI, Inc as shown in figure 2.17. A metal-matrix composite was used for the base material which offers high thermal conductivity and low coefficient of thermal expansion (CTE); enabling reliable operation at temperature above 200 ºC [100].

Figure 2.16: Full charger system hardware [100]

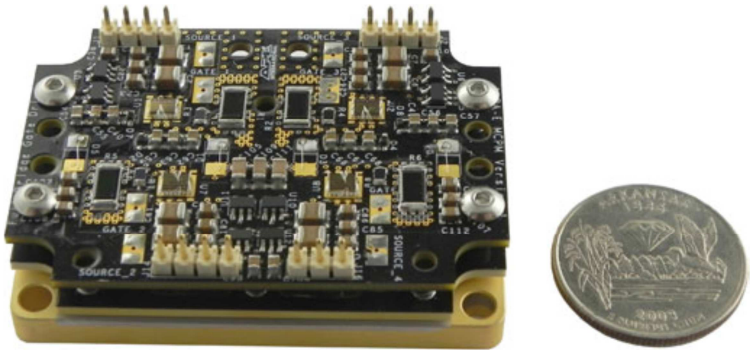


Figure 2.17: APEI, Inc. full-bridge MCPM with accompanying gate driver [100]

In [101] the properties of SiC allowed a reduction in the thermal management system of the converter, resulting in an increase in efficiency and power density. Here it was shown that in addition to the converter-level benefits, the use of SiC devices improved the performance of other components in the powertrain system including a simplified thermal management system and reduced size of the battery bank.

2.10 Electromagnetic Interference

Power electronic systems generate and emit undesirable electrical signals in the form of electromagnetic noise. These unwanted signals can cause electromagnetic interference (EMI) and performance degradation. The discipline of Electromagnetic compatibility (EMC) has been defined to ensure that the systems generating and receiving the electromagnetic energy can function without interruption from other circuits. In the early 1930s, it was understood that electromagnetic noise resulted in disturbance to radio reception and this resulted in the introduction of the international special committee on radio interference (CISPR) to ensure interference free reception [102]. In Europe, the limits of high frequency emissions are specified by either generic standards such as EN50081-2 for industrial environments, or by standards for specific

product families such as EN55011 for radio frequency equipment. Power supplies offer many advantages such as high efficiency, small size and weight, when compared with linear regulators. However, due to their high frequency operation, they cause electromagnetic interference, which includes not only the conducted noise but also radiated noise [103].

In Europe the conducted high frequency emissions are typically specified in the range of 150 kHz to 30 MHz, and the radiated emissions are specified in the range of 30 MHz and 1000 MHz [102]. The high frequency noise can be dealt with, either by suppressing it at the source or by using filters and shielding to prevent it from entering the environment. One of the methods to suppress the high frequency noise at the source is the use of fast rectifiers with soft recovery. Operating a converter in either discontinuous or boundary conduction mode can also be used to reduce the noise emissions during the turn-off phase of the diodes [102]. Based on the SiC diode main characteristics such as negligible reverse recovery current and stability of its high temperature performance, it is possible to offer EMI reduction in both high power density and high temperature applications through the use of SiC devices. The use of a SiC diode in a 70 kHz 300W boost converter was shown in [104], resulting in a marginal efficiency improvement and EMI reduction as a result of reduced peak reverse recovery current. The converter based on a SDP04S60 SiC diode form Infineon, showed conducted noise reduction at frequencies above 24 MHz when compared to two Si ultrafast soft-recovery diodes as shown by the data in figure 2.18, although the noise reduction was not significant. It was also stated that this advantage would be considerably more at higher switching frequencies and in applications where high power density converters are desired.

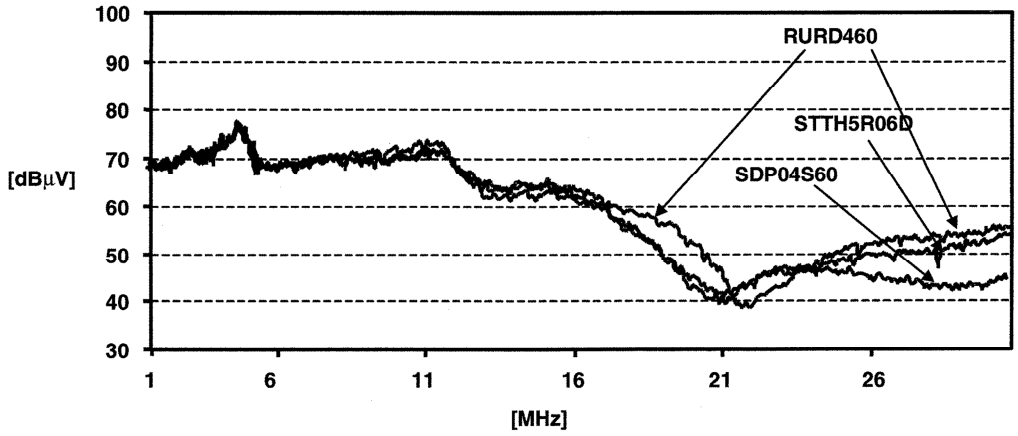


Figure 2.18: Conducted EMI measurement 1MHz-30MHz [104]

The turn-off behaviour of Si and SiC Schottky diodes and their associated converter noise frequency-spectrum were presented for a CCM boost converter in [105]. These results show a similar noise reduction for the SiC-diode based converter for a range of input voltages. The higher the input voltage, the higher the reported noise and the maximum noise reduction was achieved with a switching frequency of approximately 20 MHz. The effect of diode reverse recovery profile has been recently presented in a half bridge circuit in [106]. The data show that the improvement on the noise spectrum of the SiC diode converter over Si based converter depends on the snappiness and peak amplitude of the Si diode recovery profile. It was shown that if the Si diode has a fall time less than 5 ns with a snappy reverse recovery current, the SiC diode converter will have a more significant EMI reduction when compared to the Si based circuit.

In addition to the diode reverse recovery, the transistor switching behaviour and its associated switching current and voltage waveforms (di/dt and dv/dt) are also key sources of the electromagnetic interference. In [107], all-Si, hybrid Si-SiC and all-SiC converters are compared in terms of their switching losses and EMI generation. The Si IGBT-SiC diode combination results in a 50% reduction in total power losses when compared with the Si IGBT-Si diode based power converter. The converter based on SiC MOSFET and SiC diode showed a 90% reduction in total power losses when compared with all-Si converter.

The EMI data in [107] show that the all-SiC converter has the highest noise spectra for the majority of the frequency range studied. It was shown that with a large gate resistor value the noise spectra of the all-SiC converter is comparable with the all-Si converter but it still offers a 50%-70% reduction in overall switching losses. Considering this, the all-SiC converter can perform sufficiently with reduced switching speeds and still achieve an acceptable level of EMI generation. It was also reported that the noise spectra of the all-SiC converter is strongly influenced by the gate resistor. The choice of the gate resistor affected both the turn-on and turn-off di/dt and dv/dt of the SiC MOSFET, whereas only the turn-on dynamics of the trench field-stop IGBT were affected by the gate resistor [107].

2.11 DC-DC Converters with High Voltage Gains and Multilevel Converters

The voltage conversion ratio (VCR), the ratio of the output voltage to the input voltage of a converter, is limited to six in conventional boost converter topologies [108]. To achieve such a high value requires the use of an extremely high duty cycle (D) which leaves no scope for voltage regulation to compensate the load and line changes. An extremely high duty cycle in a boost converter also means that the diode sustains a high amplitude current with a short pulse width, resulting in severe reverse recovery transients, and unacceptably high electromagnetic interference (EMI) [108, 109]. These EMI issues affect system efficiency, cost and size. Thus, the use of multilevel converters can find applications where a high boost ratio in a DC-DC converter is required.

There are many applications requiring a DC-DC conversion with a high VCR [110-114]. One of the most important applications of high VCR converters is the renewable energy power conversion, where the low voltage generated by the renewable energy source needs to be sufficiently boosted to feed a grid connected inverter [115, 116]. Many topologies have been proposed to achieve DC-DC converters with a high VCR without the need for extremely high duty cycles [115, 116]. Coupled inductor DC-DC converters can achieve a high VCR coupled with low voltage stress on the transistor, without the need for very high duty cycles [117, 118]. The transformers or coupled inductors in these converters are bulky, difficult to wind and produce significant power losses particularly at high frequencies. A three state commutation converter derived from a boost converter is shown in figure 2.19.

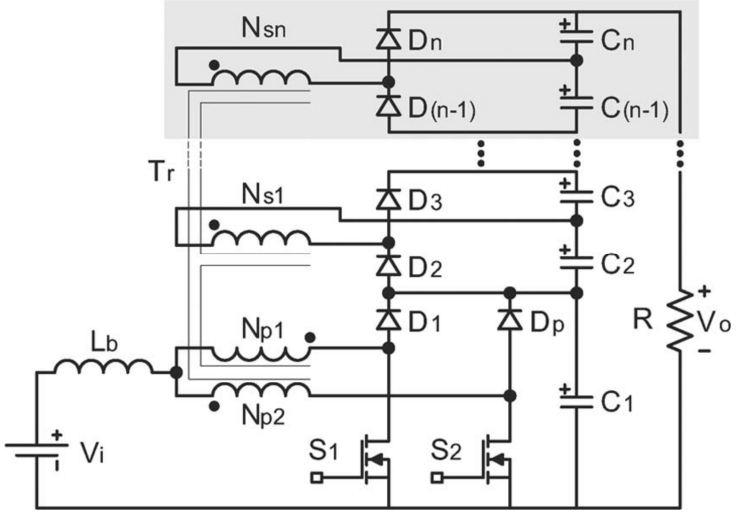


Figure 2.19: Three-state commutation boost converter [115]

Non-coupled inductor converters have been described in the literature, such as cascading converters, converters based on voltage-lift technique and converters based on voltage multipliers [119]. These high VCR topologies require several inductors, which are bulky and lossy especially when operated under high current or high frequency conditions. They also require a higher number of transistors than the conventional topologies, which increases the gate-drive complexity. An example of this topology is shown in figure 2.20 for the converter proposed in [120].

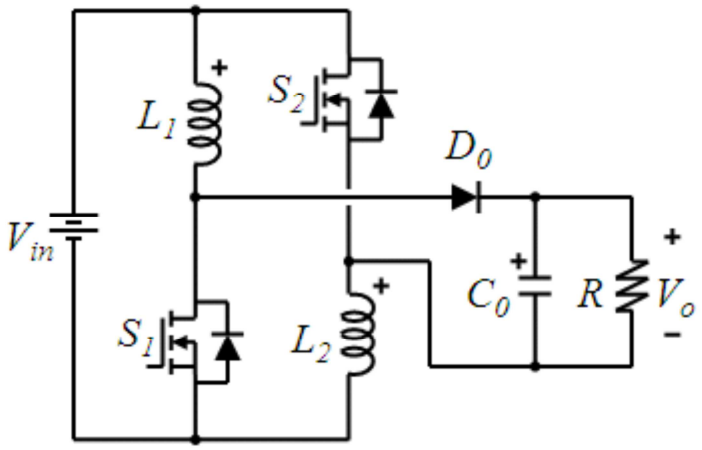


Figure 2.20: Transformer-less DC-DC converter with high step-up gain [120]

Switch-capacitor converters are also popular topologies that offer high efficiency without the need for inductors, as shown in figure 2.21. These converters; however, need multiple switches and so require complex gate-drive designs for their realisation [119].

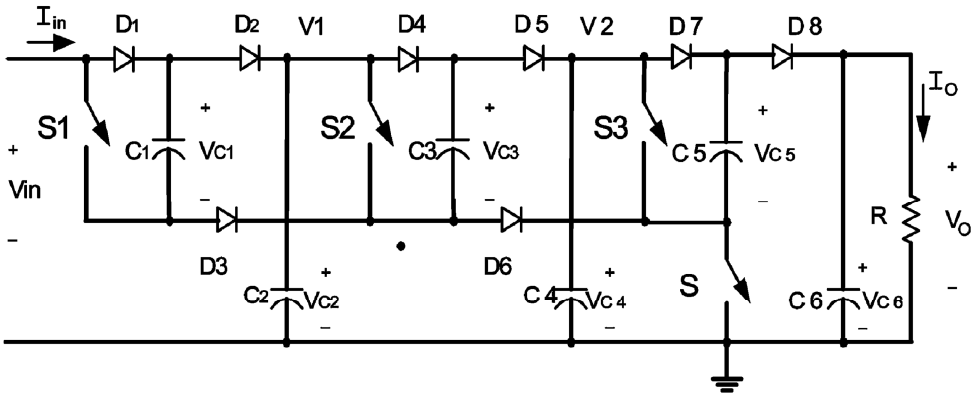


Figure 2.21: 8-Lift positive output Luo-converter [121]

One of the challenges in PV systems is to link the renewable energy source with a multilevel inverter. It is desired that such links are self-balanced to avoid complex control strategies [122]. To achieve a transformer-less DC-DC converter, a high voltage conversion ratio (VCR) is also required. For renewable applications based on multilevel inverters, it is therefore desired to design a DC-DC converter to overcome such issues by connecting the input PV array to the multilevel inverter with a self-balancing output voltage and high VCR. The DC-DC converter family based on the Cockcroft-Walton voltage multipliers was originally proposed in [119] and is shown in figure 2.22. This converter provides a high VCR and several balanced output voltages without the need for extremely high duty cycles. Similar to the AC-DC capacitor multiplier shown in figure 2.22 (a), the multiplier can be extended in either positive or negative side in DC-DC converter structure as shown in figure 2.22 (b). This transformer-less converter has only one inductor and one transistor and offers a high VCR depending on the number of stages and circuit parasitics. The converter can also be used to directly feed a multilevel inverter [123]. In this work, N+1 level means N voltage outputs when counting converter levels. This converter can directly feed a 3-level diode-clamped (or neutral-point-clamped, NPC) inverter, first introduced in [124], the most widely used inverter in industrial applications today [125].

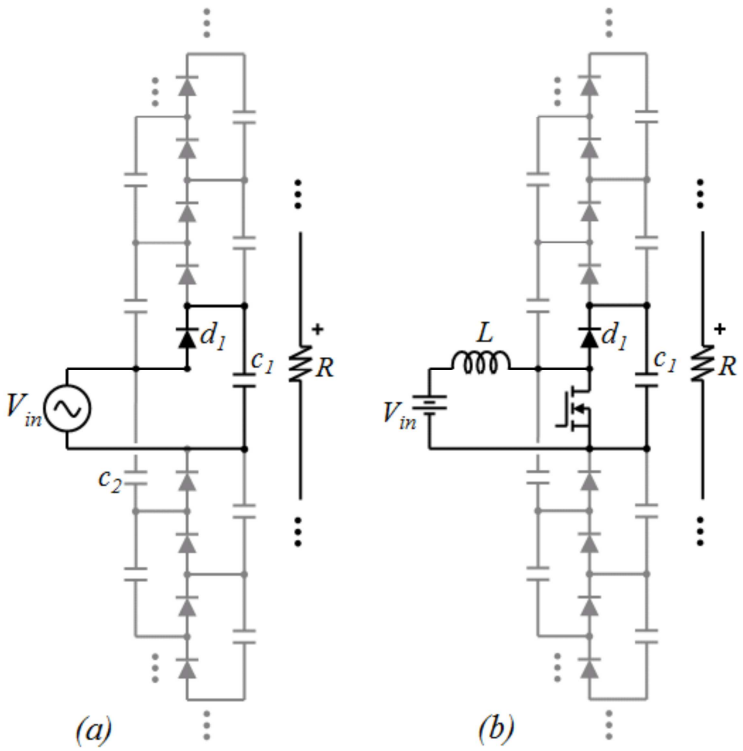


Figure 2.22: Cockcroft-Walton voltage multiplier (a) N+1 level boost converter (b) [119]

2.12 Gate Drivers for SiC MOSFET and SiC JFET Circuits

The Gate drive circuit is an integral part of all power electronic converters and it is an important interface between the power stage of the converter and the control electronics. The capability of high frequency operation is a key metric in the realisation of high efficiency high power density converters. As discussed previously, a number of SiC based transistors have been presented in the literature to date. The only SiC transistor that can be driven from a standard MOSFET/IGBT gate driver is the SiC MOSFET and a fast isolated gate driver for SiC MOSFETs was proposed by CREE in [126]. Recently, a high-speed resonant gate driver was proposed that enables the removal of the gate-resistor by minimising the effect of any parasitic inductance in the gate path and hence achieving voltage fall-times as low as 7.5 ns [127].

SiC JFETs can be fabricated as enhancement mode or depletion mode transistors [128-130]. The normally-on nature of the depletion mode JFET requires additional safety and reliability considerations associated with its start-up process or gate-driver power failures [131]. As shown in figure 2.23, one solution is to use a cascode structure with a low voltage Si MOSFET [132, 133]. The cascode connection enables the switch to be operated as a normally-off device; however, there are drawbacks with this technique. The Si MOSFET will have added conduction loss and limits the high temperature capability. In addition, both the SiC JFET and Si MOSFET need to be matched to efficiently function in the cascode structure [131].

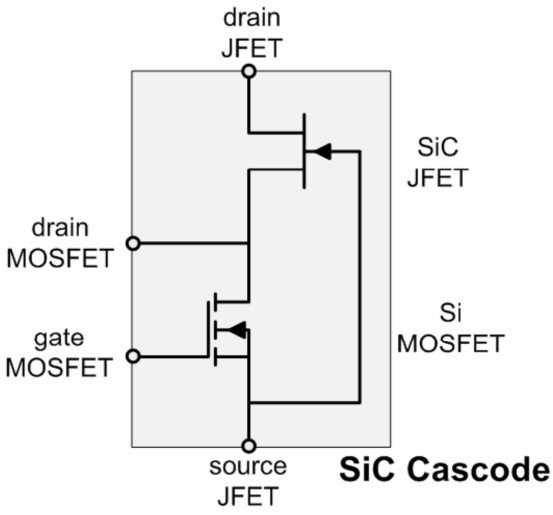


Figure 2.23: SiC JFET/Si MOSFET cascode configuration [134]

A protection scheme against shoot-through for normally-on JFETs in voltage source converters (VSCs) was presented in [135] that uses a Si IGBT in series with a relay and both in parallel with a charging resistor. This protection clears the short circuits very quickly. In [136] a protection circuit was proposed that utilises the start-up inrush current to turn off the JFET in a grid-connected switch-mode power supply. In [131] a forward converter is added to each of the normally-on JFETs to have a redundant gate supply in a self-powered design as shown in figure 2.24; however, this method requires an additional JFET for each JFET in the power stage.

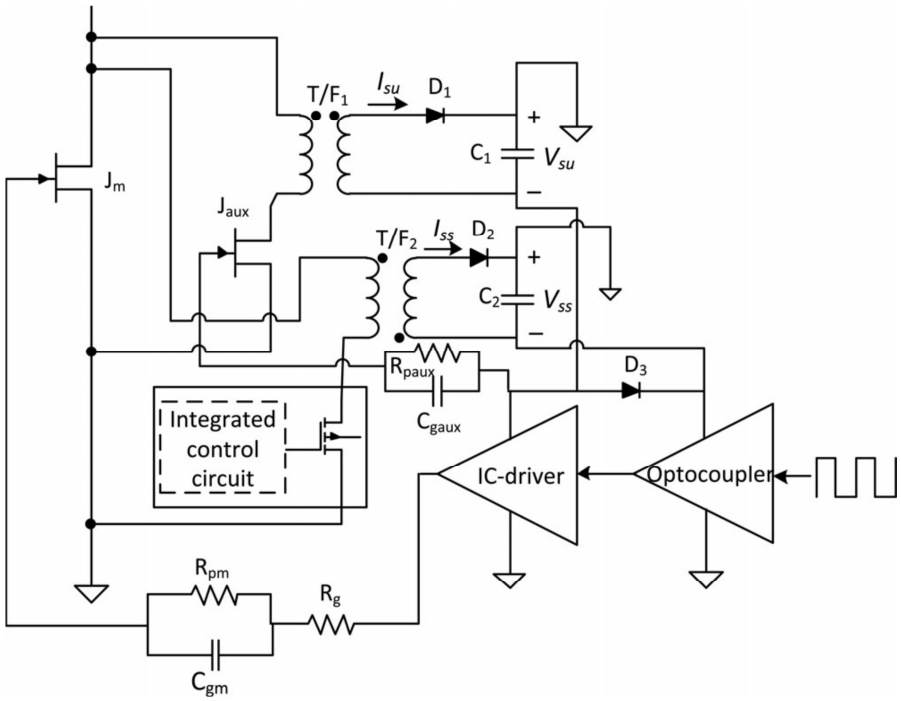


Figure 2.24: Self powered gate driver for normally-on SiC JFETs [131]

One of the most promising devices to replace Si MOSFETs or Si IGBTs is the enhancement mode (normally-off) SiC JFET, first introduced by SemiSouth Laboratories, Inc. in 2009 [137]. Designers prefer enhancement mode SiC devices to exploit the benefits of SiC without the need for redesign of the converter or gate drive. Conventional gate drivers; however, need to be modified to fully exploit the potential of enhancement mode SiC JFETs. The work in [76] presented an AC-coupled gate driver to drive a normally-off SiC JFET in a PFC circuit. With the replacement of the anti-parallel diode across the gate-resistor with a capacitor, an increase in the gate-resistor and replacement of the Si IGBT with the enhancement mode JFET, a

maximum efficiency improvement of 1.25% was achieved. The supply voltage is fed through the capacitor to the gate during turn-on and turn-off and through the resistor during on-state. One of the limitations of this RC gate driver is that the driver capacitor needs to be fully discharged before the start of next switching cycle. The maximum switching frequency of the converter is therefore limited by the time constant of the RC circuit.

An optimised two-stage DC-coupled gate driver was presented in [137] as shown in figure 2.25. The gate driver includes a fast driver with high peak-current capability to enable fast switching. There is also a second driver that reduces the gate-source voltage for on-state operation. A 200ns on-pulse-duration is applied to the first driver stage to quickly charge the input capacitance at turn-on. The p-n-p transistor of the second stage is then enabled for the on-state duration to provide the gate on-state current set by gate resistor R_G. The 15V to 6V DC-DC converter is used to reduce the conduction loss of R_G during on-state. The power loss in the gate resistor can still be excessive at high duty cycles [50]. The gate driver used in a clamped inductive circuit resulted in very low switching losses. The gate voltage must not exceed 3V during the on-state and a current of around 150mA needs to be fed into the gate, depending on the desired drain-source resistance. This gate driver still suffers from switching frequency and duty cycle limitations. The gate driver shown in figure 2.26 was presented in [50] to address these limitations. A V_{cc} of around 3V is applied to the gate during the on-state though R_{GD} and R_{DC}. With low voltage drop across the gate resistor the power dissipation is minimised. At turn-on the driver delivers the required charge using a pre-charge capacitor and at turn-off the gate capacitance is discharged through a low impedance path. This driver circuit also allows operation at frequencies up to 1 MHz.

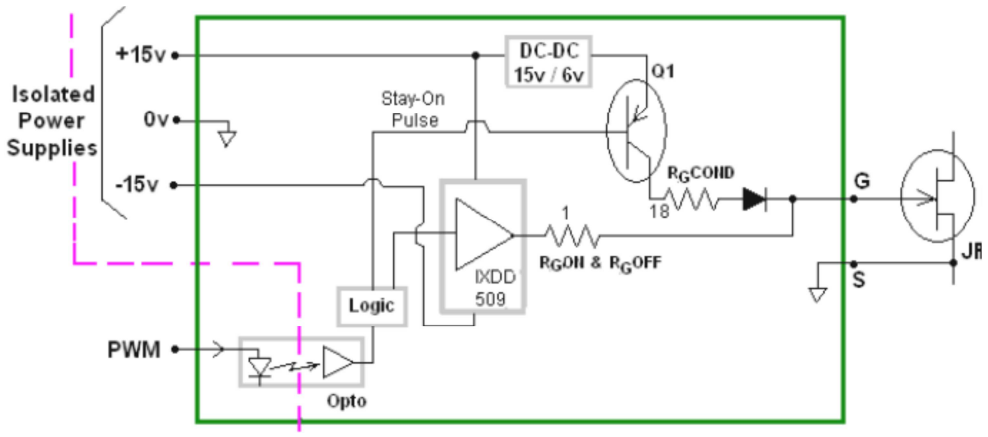


Figure 2.25: Isolated two-stage gate driver for enhancement mode JFETs [137]

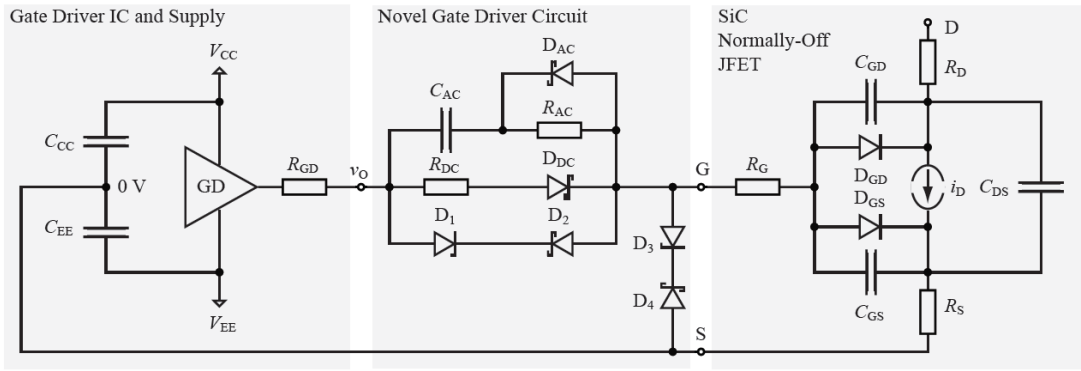


Figure 2.26: AC-coupled gate driver for fast switching of normally-off SiC JFETs [50]

2.13 High Temperature Oscillators and Logic Circuits

Reliable oscillators are required for clock and timing signal generation in many high-temperature applications such as aerospace, military and automotive industries. Crystal oscillators are stable against temperature variations however, cannot be integrated in a system-on-chip (SoC) structure [138]. At high temperatures, analogue designs based on bulk Si CMOS technology suffer from increased junction to substrate leakage, reduced carrier mobility and reduced threshold voltage of the transistor [138]. Silicon-on-insulator (SOI) is an alternative technology for high temperature applications, due to improved temperature-resistance and leakage current in comparison to bulk CMOS [139].

Due to the superior material properties of SiC, the devices based on this technology can replace or complement Si and SOI based devices for applications in high temperature environments. 6H-SiC based CMOS technology has been investigated since the 1990s [140] and 4H-SiC CMOS has been reported more recently [141]. Digital circuit designs capable of operation at 300 ºC were presented in both cases. Until recently, SiC MOSFETs have been limited in their high temperature capability due to their gate-oxide leakage; however with recent advancements in the gate-oxide fabrication [142], SiC MOSFETs are now contenders in high temperature applications, alongside JFETs and BJTs; however at the current time the maximum operating temperature is limited to 400 ºC [143] rather than the 500 ºC capability of the JFET and BJT structures [20, 144-145].

2.14 Concluding Remarks

The development of power converters for deployment in hostile environments, where the elevated ambient temperatures demand high temperature capability of the entire converter system, requires innovative power electronic circuits to meet stringent requirements in terms of efficiency, power-density and reliability. To simultaneously meet these conflicting requirements in extreme environment applications is a significant challenge. The recent advances in silicon carbide devices has allowed the realisation of not just high frequency, high efficiency power converters, but also the power electronic converters that can operate at elevated temperatures, beyond those possible using conventional silicon-based technology.

The use of SiC switching devices improves the volumetric efficiency of power electronic systems. The SiC devices can be switched much faster than Si based devices; this reduces the size of filter inductor sand capacitors in the system. Higher thermal conductivity results in more effective heat removal from SiC devices; this is particularly important to avoid self-heating at high frequency operation. Due to SiC's higher bandgap, higher temperature capability is achieved; this way smaller and lighter power converters with less aggressive thermal management can be realised.

High power-density power converter modules are key components for power supply systems in applications where size and weight are critical parameters. The increase in converter switching frequency minimises the size of passive components whilst increasing the electromagnetic interference (EMI) emissions. The choice of the switching devices, switching frequency and gate drive circuitry are all among the key factors to consider on the performance of the power converter.

The high temperature capability of the power conversion system is needed either because of the high temperature environment or because of increase power density. Either way, other components in the system also need to be able to withstand these elevated temperatures. To realise power modules for such environments, the relevant control circuitry also needs to operate at elevated temperatures. The desire to place the gate driver physically close to the power switches in the converter, leads to the necessity of a temperature resilient PWM generator to control the power electronics module.

2.15 References

[1] G. E. Moore, "Cramming more components onto integrated circuits, Electronics, volume 38, number 8, April 19, 1965.

[2] S. Krishnan, et al., "Towards a Thermal Moore's Law," Advanced Packaging, IEEE Transactions on, vol. 30, pp. 462-474, 2007.

[3] G. E. Moore, "Cramming More Components Onto Integrated Circuits," Proceedings of the IEEE, vol. 86, pp. 82-85, 1998.

[4] ITRS 2013, the 2013 Edition of the International Technology Roadmap for Semiconductors, Available: http://www.itrs.net/.

[5] K. Shenai, "Future Prospects of Widebandgap (WBG) Semiconductor Power Switching Devices," Electron Devices, IEEE Transactions on, vol. 62, pp. 248-257, 2015.

[6] K. Shenai, et al., "Rugged Electrical Power Switching in Semiconductors: A Systems Approach," Proceedings of the IEEE, vol. 102, pp. 35-52, 2014.

[7] J. Millan, "A review of WBG power semiconductor devices," in Semiconductor Conference (CAS), 2012 International, 2012, pp. 57-66.

[8] R. J. Trew, "SiC and GaN transistors - is there one winner for microwave power applications?," Proceedings of the IEEE, vol. 90, pp. 1032-1047, 2002.

[9] M. N. Yoder, "Wide bandgap semiconductor materials and devices," Electron Devices, IEEE Transactions on, vol. 43, pp. 1633-1636, 1996.

[10] P. G. Neudeck, et al., "High-temperature electronics - a role for wide bandgap semiconductors?," Proceedings of the IEEE, vol. 90, pp. 1065-1076, 2002.

[11] K. Shenai, "Grand challenges in power semiconductors," in Electron Devices and Solid-State Circuits, 2008. EDSSC 2008. IEEE International Conference on, 2008, pp. 1-4.

[12] J. Millan, et al., "A Survey of Wide Bandgap Power Semiconductor Devices," Power Electronics, IEEE Transactions on, vol. 29, pp. 2155-2163, 2014.

[13] C.-M. Zetterling, Process Technology for Silicon Carbide Devices: The Institution of Electrical Engineers, 2002.

[14] K. Shenai, et al., "Optimum semiconductors for high-power electronics," Electron Devices, IEEE Transactions on, vol. 36, pp. 1811-1823, 1989.

[15] J. Heena, et al., "Comparision of wide band gap semiconductors for power electronics applications," in Recent Advances in Microwave Theory and Applications, 2008. MICROWAVE 2008. International Conference on, 2008, pp. 878-881.

[16] E. Persson and D. Raffo, "Appliance Motor Drive Performance Improvements Using 600V GaN Cascode FETs," in PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of, 2014, pp. 1-8.

[17] R. Cheung, Silicon Carbide Microelectromechanical Systems for Harsh Environments: Imperial College Press, 2006.

[18] P.G. Neudeck, et al., " Characterization of 6H-SiC JFET Integrated Circuits Over A Broad Temperature Range from -150 °C to +500 °C," Materials Science Forum, pp. 645- 648, 2010.

[19] R. Ghandi, et al., "Silicon Carbide Integrated Circuits With Stable Operation Over a Wide Temperature Range," Electron Device Letters, IEEE, vol. 35, pp. 1206-1208, 2014.

[20] S. L. Garverick, et al., "SiC JFET integrated circuits for sensing and control at temperatures up to 600 ºC," in Energytech, 2012 IEEE, 2012, pp. 1-6.

[21] Y. M. Tairov, et al., "Investigation of Growth Processes of Ingots of Silicon Carbide Single Crystals," Journal of Crystal Growth, vol. 43, pp. 209, 1978.

[22] M. E. Levinshteĭn, S. L. Rumyantsev, and M. Shur, Properties of Advanced Semiconductor Materials: GaN, AlN, InN, BN, SiC, SiGe: Wiley, 2001.

[23] P. Roussel and H. Lin, "SiC Market: SiC Modules, Devices and Substrates for Power Electronics Market," Yole Developpment, 2014.

[24] B. Ozpineci, L. M. Tolbert, S. K. Islam, M. Chinthavali, “Comparison of Wide Bandgap Semiconductors for Power Applications,” 10th European Conference on Power Electronics and Applications, Sept. 2003, Toulouse, France.

[25] K. Shenai, et al., "Design and technology of compact high-power converters," Aerospace and Electronic Systems Magazine, IEEE, vol. 16, pp. 27-31, 2001.

[26] B. Wrzecionko, et al., "A 120 ºC Ambient Temperature Forced Air-Cooled Normally-off SiC JFET Automotive Inverter System," Power Electronics, IEEE Transactions on, vol. 29, pp. 2345-2358, 2014.

[27] K. Madjour, "Silicon Carbide market update: From discrete devices to modules," Yole Developpment, 20th-22nd May, 2014.

[28] P. Fredrichs, “SiC power devices—Lessons learned and prospects after 10 years of commercial availability,” in Proc. CS MANTECH conf., Palm Springs, CA, USA, May 16–19, 2011.

[29] R. Fu, “Modeling of Sic Power Semiconductor Devices For Switching Converter Applications,” Doctoral dissertation, 2013.

[30] P. G. Neudeck, "600 C Logic Gates Using Silicon Carbide JFET's," presented at the 2000 Government Microcircuit Applications Conference, Anaheim, CA, 2000.

[31] L. Chen, D. Spry, P. Neudeck, “Demonstration of 500 ºC AC Amplifier Based on SiC MESFET and Ceramic Packaging “, 2005 Electronics Packaging Technology Conference, 2006.

[32] S. Kun, et al., "Characteristics and optimization of 4H-SiC MESFET with a novel p-type spacer layer incorporated with a field-plate structure based on improved trap models," Journal of Semiconductors, IEEE, Chinese Institute of Electronics, vol. 32, pp. 1-6, 2011.

[33] J. Hornberger, et al., "Silicon-carbide (SiC) semiconductor power electronics for extreme high-temperature environments," in Aerospace Conference, 2004. Proceedings. 2004 IEEE, 2004, pp. 2538-2555 Vol.4.

[34] Y. Tanaka, et al., "700-V 1.0- mΩ. Cm2 Buried Gate SiC-SIT (SiC-BGSIT)," Electron Device Letters, IEEE, vol. 27, pp. 908-910, 2006.

[35] Y. Sato, "SiC-SIT intelligent switches for next-generation distribution systems," in Electric Power Equipment - Switching Technology (ICEPE-ST), 2013 2nd International Conference on, 2013, pp. 1-4.

[36] B. Buono, R. Ghandi, M. Domeij, B. G. Malm, C. M. Zetterling, and M. Ostling, "Modeling and characterization of current gain versus temperature in 4 H-SiC power BJTs," IEEE Trans. Electron Devices, vol. 57, no. 3, pp. 704–711, Mar. 2010.

[37] J. Rabkowski, D. Peftitsis, H.-P. Nee, andM. Zdanowski, "A simple high-performance low-loss current-source driver for SiC bipolar transistors," in Proc. 7th Int. Power Electron.Motion Control Conf., 2012, pp. 222–228.

[38] A. Kadavelugu, et al., "Characterization of 15 kV SiC n-IGBT and its application considerations for high power converters," in Energy Conversion Congress and Exposition (ECCE), 2013 IEEE, 2013, pp. 2528-2535.

[39] B. J. Baliga, "Advanced high voltage power device concepts," New York: Springer-Verlag, 2012.

[40] S. Ryu, et al., "High performance, ultra high voltage 4H-SiC IGBTs," IEEE Energy Conversion Congress and Exposition (ECCE), 2012, pp. 3603-3608.

[41] T. Friedli, et al., "Design and Performance of a 200-kHz All-SiC JFET Current DC-Link Back-to-Back Converter," Industry Applications, IEEE Transactions on, vol. 45, pp. 1868-1878, 2009.

[42] A. Rodriguez Alonso, et al., "Switching Performance Comparison of the SiC JFET and SiC JFET/Si MOSFET Cascode Configuration," Power Electronics, IEEE Transactions on, vol. 29, pp. 2428-2440, 2014.

[43] S. Kumar Singh, et al., "Comparative switching behaviour of silicon transistors and practical silicon carbide transistors," in Power Electronics and Drive Systems, 2009. PEDS 2009. International Conference on, 2009, pp. 585-590.

[44] T. McNutt, et al., "Silicon carbide JFET cascode switch for power conditioning applications," in Vehicle Power and Propulsion, 2005 IEEE Conference, 2005, pp. 499-506.

[45] A. Orellana and B. Piepenbreier, "Fast gate drive for SiC-JFET using a conventional driver for MOSFETs and additional protections," presented at the Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of IEEE, 2004, pp. 938-943 Vol. 1.

[46] Z. J. Shen, et al., "Wide-Bandgap Solid-State Circuit Breakers for DC Power Systems: Device and Circuit Considerations," Electron Devices, IEEE Transactions on, vol. 62, pp. 294-300, 2015.

[47] K. Lawson, et al., "Hard-Switch Stressing of Vertical-Channel Implanted-Gate SiC JFETs," Electron Device Letters, IEEE, vol. 33, pp. 86-88, 2012.

[48] V. Veliadis, et al., "Reliable Operation of SiC JFET Subjected to Over 2.4 Million 1200-V/115-A Hard Switching Events at 150 ºC," Electron Device Letters, IEEE, vol. 34, pp. 384-386, 2013.

[49] G. Kampitsis, et al., "Assessment of the reverse operational characteristics of SiC JFETs in a diode-less inverter," in Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE, 2013, pp. 477-482.

[50] B. Wrzecionko, et al., "Novel AC coupled gate driver for ultra fast switching of normally-off SiC JFETs," in IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society, 2010, pp. 605-612.

[51] J. A. Cooper, Jr. and A. Agarwal, "SiC power-switching devices-the second electronics revolution?," Proceedings of the IEEE, vol. 90, pp. 956-968, 2002.

[52] J. W. Palmour, J. A. Edmond, H. S. Kong, and C. H. Carter, Jr.,“Vertical power devices in silicon carbide,” Silicon Carbide and Related Materials, Inst. of Phys. Conf. Series, no. 137, p. 499, 1994.

[53] N. Thanh-That, et al., "Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation," Power Electronics, IEEE Transactions on, vol. 30, pp. 2445-2455, 2015.

[54] T. Santini, et al., "Gate oxide reliability assessment of a SiC MOSFET for high temperature aeronautic applications," in ECCE Asia Downunder (ECCE Asia), 2013 IEEE, 2013, pp. 385-391.

[55] R. Ouaida, et al., "Gate Oxide Degradation of SiC MOSFET in Switching Conditions," Electron Device Letters, IEEE, vol. 35, pp. 1284-1286, 2014.

[56] F. L. Luo and H. Ye, ADVANCED DC/DC CONVERTERS: CRC Press LLC, 2004.

[57] F. L. Luo and Y. Hong, Power Electronics: Advanced Conversion Technologies. Boca Raton, FL, USA: CRC Press, 2010.

[58] M. H. Rashid, Power Electronics, 2nd ed. Englewood Cliffs, NJ: Prentice Hall, 1993.

[59] N. Mohan, W. P. Robbin, and T. Undeland, Power Electronics: Converters, Applications, and Design, 2nd ed. New York: Wiley, 1995.

[60] F. Luo, et al., "Multiple-quadrant Luo-converters," Electric Power Applications, IEE Proceedings -, vol. 149, pp. 9-18, 2002.

[61] G. Koen De, et al., "Input-Current Distortion of CCM Boost PFC Converters Operated in DCM," Industrial Electronics, IEEE Transactions on, vol. 54, pp. 858-865, 2007.

[62] L. Jih-Sheng and D. Chen, "Design consideration for power factor correction boost converter operating at the boundary of continuous conduction mode and discontinuous conduction mode," in Applied Power Electronics Conference and Exposition, 1993. APEC '93. Conference Proceedings 1993., Eighth Annual, 1993, pp. 267-273.

[63] L. Huber, et al., "Effect of Valley Switching and Switching-Frequency Limitation on Line-Current Distortions of DCM/CCM Boundary Boost PFC Converters," Power Electronics, IEEE Transactions on, vol. 24, pp. 339-347, 2009.

[64] M. M. Jovanovic and J. Yungtaek, "State-of-the-art, single-phase, active power-factor-correction techniques for high-power applications - an overview," Industrial Electronics, IEEE Transactions on, vol. 52, pp. 701-708, 2005.

[65] A. R. Hefner, Jr., et al., "SiC power diodes provide breakthrough performance for a wide range of applications," Power Electronics, IEEE Transactions on, vol. 16, pp. 273-280, 2001.

[66] J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan, “An assessment of wide bandgap semiconductors for power devices,” IEEE Trans. Power Elect., vol. 18, no. 3, pp. 907–914, 2003.

[67] T. Funaki, et al., "Power Conversion With SiC Devices at Extremely High Ambient Temperatures," Power Electronics, IEEE Transactions on, vol. 22, pp. 1321-1329, 2007.

[68] K. Shenai, et al., "Characterization of hard- and soft-switching performance of high-voltage Si and 4H-SiC PiN diodes," Electron Devices, IEEE Transactions on, vol. 49, pp. 1648-1656, 2002.

[69] A. Elasser, et al., "A comparative evaluation of new silicon carbide diodes and state-of-the-art silicon diodes for power electronic applications," Industry Applications, IEEE Transactions on, vol. 39, pp. 915-921, 2003.

[70] G. Yan, et al., "Comparison of Static and Switching Characteristics of 1200 V 4H-SiC BJT and 1200 V Si-IGBT," Industry Applications, IEEE Transactions on, vol. 44, pp. 887-893, 2008.

[71] J. Jordan, et al., "A Comparative Performance Study of a 1200 V Si and SiC MOSFET Intrinsic Diode on an Induction Heating Inverter," Power Electronics, IEEE Transactions on, vol. 29, pp. 2550-2562, 2014.

[72] B. Callanan, "Application Considerations for Silicon Carbide MOSFETs, "CREE Application Note: CPWR-AN08, Jan, 2011, Available: http://www.cree.com/.

[73] J. Richmond, "Hard-Switched Silicon IGBTs?," CREE Application Note: CPWR-AN03, Rev. B, 2013, Available: http://www.cree.com/.

[74] W. Chuanyun, et al., "New Architecture for MHz Switching Frequency PFC," in Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE, 2007, pp. 179-185.

[75] T. Friedli, et al., "The Essence of Three-Phase PFC Rectifier Systems-Part II," Power Electronics, IEEE Transactions on, vol. 29, pp. 543-560, 2014.

[76] R. L. Kelley, et al., "Power factor correction using an enhancement-mode SiC JFET," in Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, 2008, pp. 4766-4769.

[77] M. Kitabatake, et al., "4H-SiC-DIMOSFET power device for home appliances," in Power Electronics Conference (IPEC), 2010 International, 2010, pp. 3249-3253.

[78] X. Xu, et al., "Performance Evaluation of SiC MOSFET/BJT/Schottky Diode in A 1MHz Single Phase PFC," in Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE, 2007, pp. 1268-1272.

[79] B. Ozpineci, et al., "A 55-kW Three-Phase Inverter With Si IGBTs and SiC Schottky Diodes," Industry Applications, IEEE Transactions on, vol. 45, pp. 278-285, 2009.

[80] Z. Tiefu, et al., "Comparisons of SiC MOSFET and Si IGBT Based Motor Drive Systems," in Industry Applications Conference, 2007. 42nd IAS Annual Meeting. Conference Record of the 2007 IEEE, 2007, pp. 331-335.

[81] R. A. Wood and T. E. Salem, "Evaluation of a 1200-V, 800-A All-SiC Dual Module," Power Electronics, IEEE Transactions on, vol. 26, pp. 2504-2511, 2011.

[82] X. Fan, et al., "Development of a SiC JFET-Based Six-Pack Power Module for a Fully Integrated Inverter," Power Electronics, IEEE Transactions on, vol. 28, pp. 1464-1478, 2013.

[83] L. Rixin, et al., "A Systematic Topology Evaluation Methodology for High-Density Three-Phase PWM AC-AC Converters," Power Electronics, IEEE Transactions on, vol. 23, pp. 2665-2680, 2008.

[84] S. Safari, et al., "Experimental and Analytical Performance Evaluation of SiC Power Devices in the Matrix Converter," Power Electronics, IEEE Transactions on, vol. 29, pp. 2584-2596, 2014.

[85] A. Escobar-Mejia, et al., "Realization of a Modular Indirect Matrix Converter System Using Normally Off SiC JFETs," Power Electronics, IEEE Transactions on, vol. 29, pp. 2574-2583, 2014.

[86] C. N. M. Ho, et al., "A Comparative Performance Study of an Interleaved Boost Converter Using Commercial Si and SiC Diodes for PV Applications," Power Electronics, IEEE Transactions on, vol. 28, pp. 289-299, 2013.

[87] A. Rodriguez, et al., "Optimizing the efficiency of a dc-dc boost converter over 98% by using commercial SiC transistors with switching frequencies from 100 kHz to 1MHz," in Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE, 2013, pp. 641-648.

[88] J. S. Glaser, et al., "Direct comparison of silicon and silicon carbide power transistors in high-frequency hard-switched applications," in Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE, 2011, pp. 1049-1056.

[89] J. A. Carr, et al., "Assessing the Impact of SiC MOSFETs on Converter Interfaces for Distributed Energy Resources," Power Electronics, IEEE Transactions on, vol. 24, pp. 260-270, 2009.

[90] D. Peftitsis, et al., "High-power modular multilevel converters with SiC JFETs," in Energy Conversion Congress and Exposition (ECCE), 2010 IEEE, 2010, pp. 2148-2155.

[91] Z. Xueqian, et al., "An All-SiC High-Frequency Boost DC-DC Converter Operating at 320 ºC Junction Temperature," Power Electronics, IEEE Transactions on, vol. 29, pp. 5091-5096, 2014.

[92] H. Kosai, et al., "Design and Performance Evaluation of a 200 ºC Interleaved Boost Converter," Power Electronics, IEEE Transactions on, vol. 28, pp. 1691-1699, 2013.

[93] M. A. Huque, et al., "A 200 ºC Universal Gate Driver Integrated Circuit for Extreme Environment Applications," Power Electronics, IEEE Transactions on, vol. 27, pp. 4153-4162, 2012.

[94] J. W. Kolar, et al., "PWM Converter Power Density Barriers," in Power Conversion Conference - Nagoya, 2007. PCC '07, 2007, pp. P-9-P-29.

[95] M. Pavlovsky, et al., "Pursuing high power-density and high efficiency in DC-DC converters for automotive application," in Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, 2008, pp. 4142-4148.

[96] W. G. Homeyer, et al., "Advanced power converters for More Electric Aircraft applications," in Energy Conversion Engineering Conference, 1997. IECEC-97., Proceedings of the 32nd Intersociety, 1997, pp. 591-596 vol.1.

[97] L. Rixin, et al., "A High-Power-Density Converter," Industrial Electronics Magazine, IEEE, vol. 4, pp. 4-12, 2010.

[98] J. Biela, et al., "SiC versus Si-Evaluation of Potentials for Performance Improvement of Inverter and DC-DC Converter Systems by SiC Power Semiconductors," Industrial Electronics, IEEE Transactions on, vol. 58, pp. 2872-2882, 2011.

[99] A. M. Abou-Alfotouh, et al., "A 1-MHz hard-switched silicon carbide DC-DC converter," Power Electronics, IEEE Transactions on, vol. 21, pp. 880-889, 2006.

[100] B. Whitaker, et al., "A High-Density, High-Efficiency, Isolated On-Board Vehicle Battery Charger Utilizing Silicon Carbide Power Devices," Power Electronics, IEEE Transactions on, vol. 29, pp. 2606-2617, 2014.

[101] Z. Hui, et al., "Impact of SiC Devices on Hybrid Electric and Plug-In Hybrid Electric Vehicles," Industry Applications, IEEE Transactions on, vol. 47, pp. 912-921, 2011.

[102] R. Redl, "Electromagnetic environmental impact of power electronics equipment," Proceedings of the IEEE, vol. 89, pp. 926-938, 2001.

[103] M. H. Nagrial and A. Hellany, "Radiated and conducted EMI emissions in switch mode power supplies (SMPS): sources, causes and predictions," in Multi

Topic Conference, 2001. IEEE INMIC 2001. Technology for the 21st Century. Proceedings. IEEE International, 2001, pp. 54-61.

[104] G. Spiazzi, et al., "Performance evaluation of a Schottky SiC power diode in a boost PFC application," Power Electronics, IEEE Transactions on, vol. 18, pp. 1249-1253, 2003.

[105] T. Ibuchi and T. Funaki, "Effect of diode characteristics on conducted noise spectrum in CCM boost converter," in Electromagnetic Compatibility (EMC Europe), 2014 International Symposium on, 2014, pp. 59-64.

[106] Y. Xibo, et al., "EMI Generation Characteristics of SiC and Si Diodes: Influence of Reverse-Recovery Characteristics," Power Electronics, IEEE Transactions on, vol. 30, pp. 1131-1136, 2015.

[107] N. Oswald, et al., "An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation With Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations," Power Electronics, IEEE Transactions on, vol. 29, pp. 2393-2407, 2014.

[108] E. H. Ismail, et al., "High Conversion Ratio DC-DC Converters With Reduced Switch Stress," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 55, pp. 2139-2151, 2008.

[109] L. Huber and M. M. Jovanovic, "A design approach for server power supplies for networking applications," in Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE, 2000, pp. 1163-1169 vol.2.

[110] L. Wuhua and H. Xiangning, "Review of Nonisolated High-Step-Up DC/DC Converters in Photovoltaic Grid-Connected Applications," Industrial Electronics, IEEE Transactions on, vol. 58, pp. 1239-1250, 2011.

[111] L. Weichen, et al., "A non-isolated high step-up converter with built-in transformer derived from its isolated counterpart," in IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society, 2010, pp. 3173-3178.

[112] L. W. Zhou, et al., "Interleaved non-isolated high step-up DC/DC converter based on the diode-capacitor multiplier," Power Electronics, IET, vol. 7, pp. 390-397, 2014.

[113] W. Li, et al., "Performance analysis of ZVT interleaved high step-up converter with built-in transformer," in Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on, 2010, pp. 1-6.

[114] A. Anthon, et al., "A high power boost converter for PV Systems operating up to 300 kHz using SiC devices," in Electronics and Application Conference and Exposition (PEAC), 2014 International, 2014, pp. 302-307.

[115] S. V. Araujo, et al., "Highly Efficient High Step-Up Converter for Fuel-Cell Power Processing Based on Three-State Commutation Cell," Industrial Electronics, IEEE Transactions on, vol. 57, pp. 1987-1997, 2010.

[116] C. Shih-Kuen, et al., "Novel High Step-Up DC-DC Converter for Fuel Cell Energy Conversion System," Industrial Electronics, IEEE Transactions on, vol. 57, pp. 2007-2017, 2010.

[117] C. S. Leu and L. Ming-Hui, "A Novel Current-Fed Boost Converter With Ripple Reduction for High-Voltage Conversion Applications," Industrial Electronics, IEEE Transactions on, vol. 57, pp. 2018-2023, 2010.

[118] K. I. Hwu and Y. T. Yau, "Voltage-Boosting Converter Based on Charge Pump and Coupling Inductor With Passive Voltage Clamping," Industrial Electronics, IEEE Transactions on, vol. 57, pp. 1719-1727, 2010.

[119] J. C. Rosas-Caro and J. C. Mayo-Maldonado. A Family of DC_DC Multiplier Converters [Online], 2011.

[120] Y. Lung-Sheng, et al., "Transformerless DC-DC Converters With High Step-Up Voltage Gain," Industrial Electronics, IEEE Transactions on, vol. 56, pp. 3144-3152, 2009.

[121] L. Fang Lin and Y. Hong, "Positive output multiple-lift push-pull switched-capacitor Luo-converters," Industrial Electronics, IEEE Transactions on, vol. 51, pp. 594-602, 2004.

[122] R. Davoodnezhad, et al., "A Novel Three-Level Hysteresis Current Regulation Strategy for Three-Phase Three-Level Inverters," Power Electronics, IEEE Transactions on, vol. 29, pp. 6100-6109, 2014.

[123] O. Mostaghimi, et al., "Switching Losses in a SiC-based DC-DC Multilevel Boost Converter," Materials Science Forum, vol. 717-720, pp. 1241-1244, 2012.

[124] A. Nabae, et al., "A New Neutral-Point-Clamped PWM Inverter," Industry Applications, IEEE Transactions on, vol. IA-17, pp. 518-523, 1981.

[125] J. Rodriguez, et al., "A Survey on Neutral-Point-Clamped Inverters," Industrial Electronics, IEEE Transactions on, vol. 57, pp. 2219-2230, 2010.

[126] SiC MOSFET Isolated Gate Driver, CREE Application Note: CPWR-AN10, REV-C, 2014, Available: http://www.cree.com/.

[127] P. Anthony, et al., "High-Speed Resonant Gate Driver With Controlled Peak Gate Voltage for Silicon Carbide MOSFETs," Industry Applications, IEEE Transactions on, vol. 50, pp. 573-583, 2014.

[128] E. Platania, et al., "A Physics-Based Model for a SiC JFET Accounting for Electric-Field-Dependent Mobility," Industry Applications, IEEE Transactions on, vol. 47, pp. 199-211, 2011.

[129] A. E. Grekov, et al., "Parameter Extraction Procedure for Vertical SiC Power JFET," Industry Applications, IEEE Transactions on, vol. 47, pp. 1862-1871, 2011.

[130] C. Zhiyang, et al., "Model for Power SiC Vertical JFET With Unified Description of Linear and Saturation Operating Regimes," Industry Applications, IEEE Transactions on, vol. 47, pp. 1853-1861, 2011.

[131] D. Peftitsis, et al., "Self-Powered Gate Driver for Normally ON Silicon Carbide Junction Field-Effect Transistors Without External Power Supply," Power Electronics, IEEE Transactions on, vol. 28, pp. 1488-1501, 2013.

[132] R. Siemieniec and U. Kirchner, “The 1200V direct-driven SiC JFET power switch,” in Proc. 2011-14th Eur. Conf. Power Electron. Appl., pp. 1–10.

[133] K. Norling, C. Lindholm, and D. Draxelmayr, “An optimized driver for SiC JFET-based switches delivering more than 99% efficiency,” in Proc. IEEE Int. Solid-State Circuits Conf. Digest Tech. Papers, Feb. 19–23, 2012, pp. 284–286.

[134] S. Round, et al., "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter," in Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005, 2005, pp. 410-416 Vol. 1.

[135] L. Rixin, W. Fei, R. Burgos, D. Boroyevich, D. Zhang, and P. Ning, “A shoot-through protection scheme for converters built with SiC JFETs,” IEEE Trans. Ind. Appl., vol. 46, no. 6, pp. 2495–2500, Nov./Dec. 2010.

[136] J. H. Kim, B.-D. Min, J.-W. Baek, and D.-W. Yoo, “Protection circuit of normally-on SiC JFET using an inrush current,” in Proc. 31st Int. Telecommun. Energy Conf., Oct. 18–22, 2009, pp. 1–4.

[137] R. Kelley, et al., "Improved two-stage DC-coupled gate driver for enhancement-mode SiC JFET," in Applied Power Electronics Conference and Exposition ,APEC, 2010 Twenty-Fifth Annual IEEE, 2010, pp. 1838-1841.

[138] N. Sadeghi, et al., "A 0.007-mm2 108-p±/ºC 1-MHz Relaxation Oscillator for High-Temperature Applications up to 180 ºC in 0.13-µm CMOS," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 60, pp. 1692-1701, 2013.

[139] D. Vanhoenacker-Janvier, M. El Kaamouchi, and M. Si Moussa, “Silicon-on-insulator for high-temperature applications,” IET Circuits Devices Syst., vol. 2, no. 1, pp. 151–157, Feb. 2008.

[140] S. H. Ryu, K. T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch, “Digital CMOS ICs in 6H-SiC operating on a 5-V power supply,” IEEE Trans. Electron Devices, vol. 45, no. 1, pp. 45–53, Jan. 1998.

[141] D. Clark, E. P. Ramsay, A. E. Murphy, D. A. Smith, R. F. Thompson, R. A. R. Young, J. D. Cormack, J. McGonigal, C. Zhu, S. Finney, and J. Fletcher, “High temperature silicon carbide CMOS integrated circuits, ”Mater. Sci. Forum, vol. 679/680, pp. 726–729, 2011.

[142] L. C. Yu, et al., "Reliability Issues of SiC MOSFETs: A Technology for High-Temperature Environments," Device and Materials Reliability, IEEE Transactions on, vol. 10, pp. 418-426, 2010.

[143] R. A. R. Young, D. T. Clark, J. D. Cormack, et al., “High temperature digital and analogue integrated circuits in silicon carbide,” Mater. Sci. Forum, vols. 740–742, pp. 1065–1068, Jan. 2013.

[144] L. Lanni, B. G. Malm, M. Östling, et al., “500 °C bipolar intergrated OR/NOR gate in 4H-SiC,” IEEE Electron Device Lett., vol. 34, no. 9, pp. 1091–1093, Sep. 2013.

[145] P. G. Neudeck, et al., "Stable Electrical Operation of 6H-SiC JFETs and ICs for Thousands of Hours at 500 ºC," Electron Device Letters, IEEE, vol. 29, pp. 456-459, 2008.

Chapter 3. High Frequency Operation of DC-DC Converters

3.1 Introduction

High power-density power converters are key components for power supply systems in applications where space and weight are critical parameters. The demand for higher power density requires the use of high-frequency DC-DC converters to overcome the increase in size and power losses due to the use of transformers, inductors and capacitors [1-11]. The increase in converter switching frequency reduces the size of passive components whilst increasing the electromagnetic interference (EMI) emissions. Reduction of EMI requires bulky filters to comply with electromagnetic compatibility (EMC) standards [12-15]. Higher switching frequencies also increase the switching losses, which result in an increased heatsink volume and reduced converter power density.

Devices fabricated using Silicon Carbide, are attractive candidates for achieving light and efficient power electronic converters. The high carrier drift-velocity of SiC offer fast switching capability [15-19]. The lack of stored minority carriers in SiC Schottky Diodes results in minimal reverse recovery charge (Q_{rr}) during turn-off. There is, however, a small displacement current required to charge the junction capacitance. This charging current is not dependent on di/dt, junction temperature and current level but is dependent on dv/dt. In contrast, the reverse recovery charge in Si PiN diodes, increases significantly with temperature, significantly increasing the switching losses in both the diode and associated IGBT [20-22].

Previous work has concentrated on the reduction of switching losses with the use of SiC diodes and hence the reduction of turn-on loss incurred in silicon IGBTs in high voltage converter circuits with inductive loads, resulting in higher system efficiency and power densities [22-25]. Due to the bipolar nature of IGBTs, current tail phenomenon results in higher switching losses than similarly rated Si power MOSFETs [23]. Because of the higher conduction loss of Si MOSFETs, the charge compensation technique was introduced in the 1990's to reduce the conduction loss, therefore enhancing the voltage ratings of power MOSFETs up to 900V. Based on this concept in CoolMOS technology, R_{ds}(on) and output capacitance have been reduced, maximising

the benefits of combining SiC Schottky diode and CoolMOS in power factor correction (PFC) applications [26, 27]. However, the limitations of silicon power devices at elevated temperatures result in the decreased transconductance and slower switching times for silicon MOSFETs [28]. SiC MOSFETs have shown lower switching losses when compared to their silicon counterparts [29]. SiC devices have different electrical characteristics when compared to high power silicon MOSFETs and as a result are not suitable as direct drop-in replacements in power converter applications.

Silicon carbide depletion mode (DM) JFETs are commercially available, offering low on-state resistance and switching losses. However, there are still implementation challenges due to their normally-on characteristics. Driver malfunction results in severe shoot-through failure in the converter DC bus and several shoot-through protection schemes have been proposed, based on desaturation protection circuits [30, 31]. The first report of a commercial fully enhancement mode (EM) SiC JFET in a power factor correction (PFC) circuit has superseded the idea of a SiC JFET as a normally-on device. The EM JFET offers the benefits of DM SiC JFETs and efficiency improvements over silicon-based switches have been reported in the literature [32, 33].

3.2 Conventional Si and SiC DC-DC Converters

The design considerations and performance evaluation of SiC MOSFETs, SiC JFETs and junction barrier Schottky (JBS) diodes in a 1-kW photovoltaic pre-regulator application are presented, considering optimum driving requirements for fair performance comparison. Figure 3.1 shows a typical single-phase transformer-less photovoltaic inverter system [34-38]. The DC-DC pre-regulator boost converter acts as the maximum power point tracker (MPPT) and DC link stabiliser, whilst the inverter delivers AC power to the grid. The specifications of the boost converter are shown in table 3.1. The 400V output enables the generation of 240V AC for grid-connect applications in the UK.

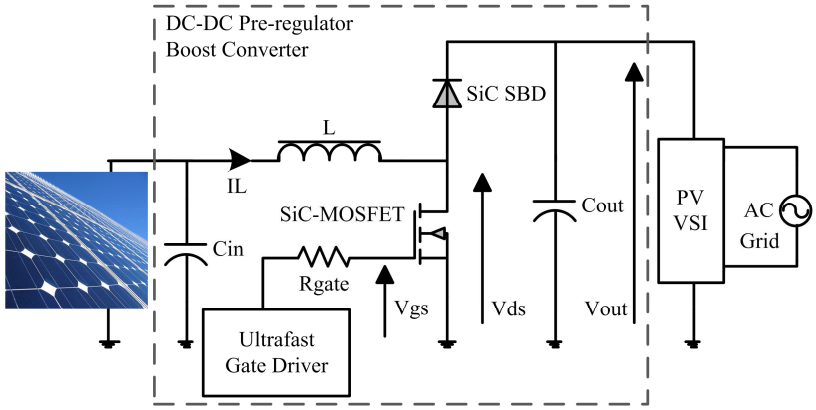


Figure 3.1: PV inverter system including the pre-regulator DC-DC converter

Converter Parameter	**Value**	**Converter Parameter**	**Value**
Input Voltage	210 V_{DC}	Switching Frequency	100 kHz
Output Voltage	400 V_{DC}	Input Inductor Value	250 µH
Output Power	1 kW	Output Filter Capacitors	2×5µF
Inductor Current Ripple	20% of $I_{L,\,avg}$	Max. Ambient/Junction Temperature	25/200 °C
Output Voltage Ripple	2% of $V_{out,\,avg}$	External Cooling Requirements	None

Table 3.1: Summary of design requirements and passive power component values

The design criteria of the converter are based on the requirement for steady-state operation of the semiconductor devices at the desired switching frequency. The converter is operated at an input DC voltage of 210V and an output voltage of 400V DC. The output capacitor is selected as two 5µF capacitors in parallel so that the output voltage ripple is limited to 2% under full load conditions. A 250µH inductor is used to ensure continuous conduction mode operation (CCM) and to limit the inductor current ripple to 20%. Table 3.2 shows the key parameters of the Si and SiC devices under test (DUTs) obtained from the manufacturer datasheets. The test setup for the converter performance evaluation based on different semiconductor technologies is shown in figures 3.2 (a) and 3.2 (b).

Parameter	Devices						Unit
	SiC MOSFET	SiC JFET	CoolMOS	SiC Diode	Si Diode	Si Diode	
Breakdown Voltage	1200	1200	900	600	600	600	V
Rated Current	17@100 °C	20@150 °C	23@100 °C	8@105 °C	8@105 °C	8@105 °C	A
Max. Junction T.	125	150	150	175	175	150	°C
Manufacturer	CREE	SemiSouth	Infineon	ST Micro.	Vishay	Fairchild	
Part No.	CMF20120D	SJEP120R063	IPW90R120C3	STPSC806D	ETX0806	FFP08H60S	

Table 3.2: Parameters of the evaluated Silicon and Silicon Carbide devices

Figure 3.2: Test setup for converter evaluation based on different semiconductor technologies (a) and (b)

To ensure accuracy of the power measurements, the voltage and current waveforms were time aligned. Due to the characteristic propagation delays of the high voltage differential probe (Tektronix P5210, 50 MHz bandwidth) and the Hall Effect

current probe (Tektronix TCP202, 50 MHz bandwidth), the probes were de-skewed by 5.5 ns to avoid inaccurate timing measurements and distorted power waveforms. The current probe was also degaussed after each measurement to remove residual magnetism from the probe core that would otherwise cause measurement errors. A SGI series 600V, 30kW Sorensen high voltage power supply and an MSO4034 Tektronix oscilloscope with an analog bandwidth of 350 MHz were used for the experimental measurements. The oscilloscope was set to Hi Res Mode that improves the accuracy of switching loss measurements which are based on mathematically calculated values. The offset of both the current and voltage probes were also eliminated before proceeding with measurements.

3.2.1 Drive Circuity

The low transconductance and noise margin of the CREE SiC MOSFET requires careful consideration during the gate drive design [39, 40]. To optimise the performance, the device requires a higher gate-source voltage than the typical 10V-15V required by silicon power MOSFETs and -2V to -5V to minimise both the off-state leakage and threshold voltage instability [41]. Despite the higher gate voltage, the lower gate charge of the SiC MOSFET results in the importance of the gate energy metric, which is defined as the product of gate charge and gate voltage. Therefore the higher voltage swing might not adversely affect the gate drive power requirements. The Miller plateau in the Vgs versus gate charge characteristics is not as flat as that observed in Si IGBTs and MOSFETs; due to the low transconductance of the device [40]. As shown in figures 3.3 (a) and 3.3 (b), an ultrafast isolated gate driver has been implemented to test and evaluate SiC MOSFETs in this application. The circuit consists of a totem-pole output opto-coupler and the IXDN614 ultrafast gate driver with a 35V output swing.

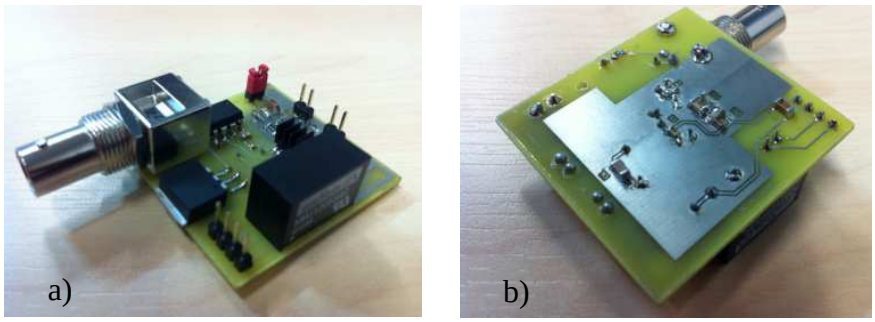


Figure 3.3: Ultrafast isolated gate driver designed for the SiC MOSFET, top view on the left (a) and bottom view on the right (b)

The gate driver IC has a 14A peak drive current and 0.4 Ω typical output resistance to obtain very low voltage rise and fall times. The positive bias voltage is directly connected to the gate driver and also to a 15V voltage regulator to supply the opto-coupler. Power for the negative bias is provided by an isolated DC-DC buck converter with a 3kV DC galvanic isolation to reduce switching noise. Both the source and negative power planes are shown in figure 3.4. A very tight coupling between the source output terminal and the negative power plane was provided to minimise stray inductance.

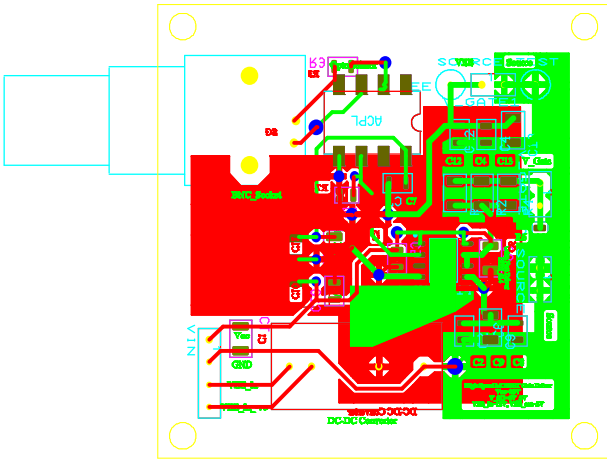


Figure 3.4: Ultrafast isolated gate driver designed for the SiC MOSFET evaluation (source power plane in green, negative power plane in red)

The AC coupled driver in [32] drove an enhancement mode SiC JFET in a commercial PFC board to improve the converter efficiency. However, the frequency limitations due to the RC time constant of the driver resulted in the optimised two-stage DC-coupled gate driver proposed in [42] that offers very fast switching speeds. Here, the DC-coupled gate driver circuit from SemiSouth is used for the device evaluation, as shown in figure 3.5. A ±13V supply voltage was used to power the DC-coupled gate driver for the SiC JFET.

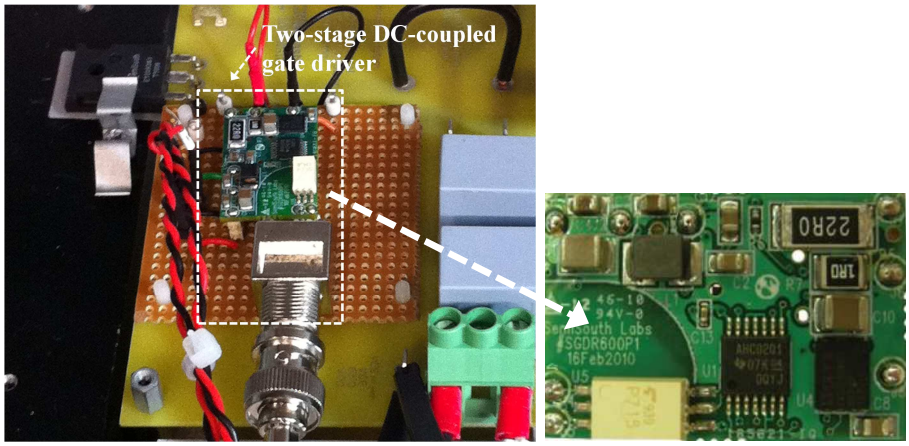


Figure 3.5: Two-stage DC-coupled gate driver from SemiSouth used for the evaluation of the enhancement-mode SiC JFET

The experimental setup of the 1kW converter is shown in figure 3.6. Pliable thermal interface pads with low thermal resistance were used between an aluminium heatsink with a thermal resistance of 0.34 ºC/W and power devices that allowed complete surface contact with excellent heat dissipation. No external cooling was used to cool the Si and SiC devices under test.

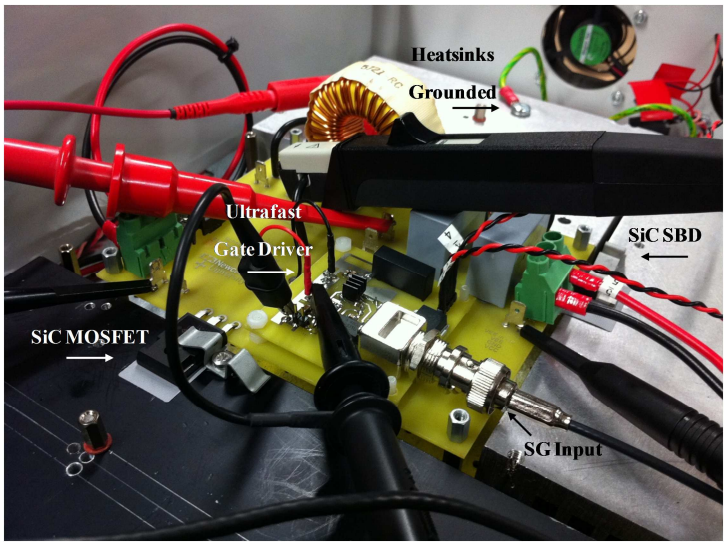


Figure 3.6: Experimental setup of the 1kW DC-DC converter used for device evaluation

3.2.2 Converter Performance Evaluation

3.2.2.1 Si CoolMOS-Si/SiC Diode Evaluation

A summary of the device combinations evaluated in the converter are shown in table 3.3. CoolMOS implements a compensation structure in the vertical drift region of a MOSFET to reduce the on-resistance and also reduces the junction capacitance compared to conventional MOSFET technologies [43, 44]. Figure 3.7 shows the diode turn-off waveforms at 100 kHz with the CoolMOS as the associated switch. A gate-source voltage of $10V_{pp}$ and an external gate resistance of 7.5 Ω were used for the CoolMOS to achieve very fast switching while adequately damping the gate oscillations.

	Device Combination				
	I	II	III	IV	V
Diode	Vishay Diode	Fairchild Diode	SiC Diode	SiC Diode	SiC Diode
Type	Ultrafast	Ultrafast	Schottky	Schottky	Schottky
FET	Si MOSFET	Si MOSFET	Si MOSFET	SiC MOSFET	SiC JFET
Type	CoolMOS	CoolMOS	CoolMOS	Z-FET	EM Trench

Table 3.3: Device combinations used in converter evaluation

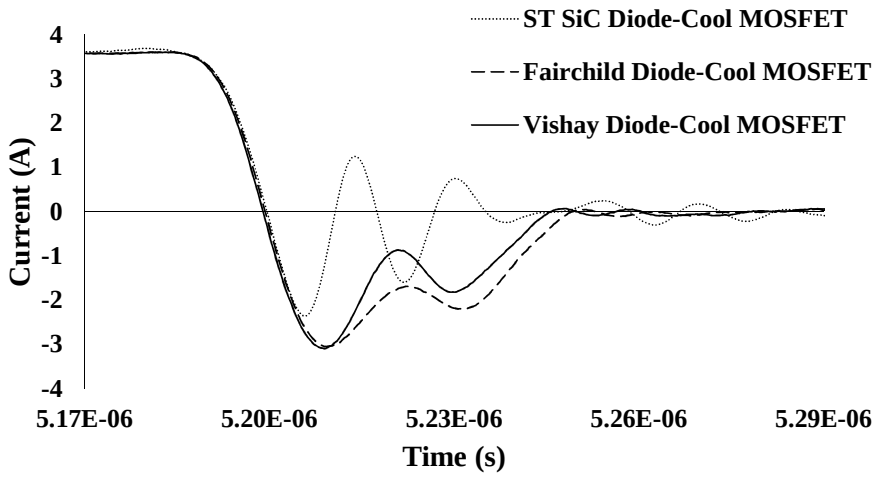


Figure 3.7: Diode turn-off current waveforms for the Si CoolMOS-Si/SiC diode combinations at 100 kHz switching frequency

The converter has an output voltage of $400V_{dc}$. The reverse recovery charge of the Vishay and Fairchild ultrafast diodes are 70.65nC and 90.87nC, respectively, experimentally measured from the diode current waveforms. The reverse recovery charge in the SiC JBS diode is measured as 11.33nC which causes a small displacement current and hence a slight overshoot in the FET turn-on current waveform, as shown in figure 3.8.

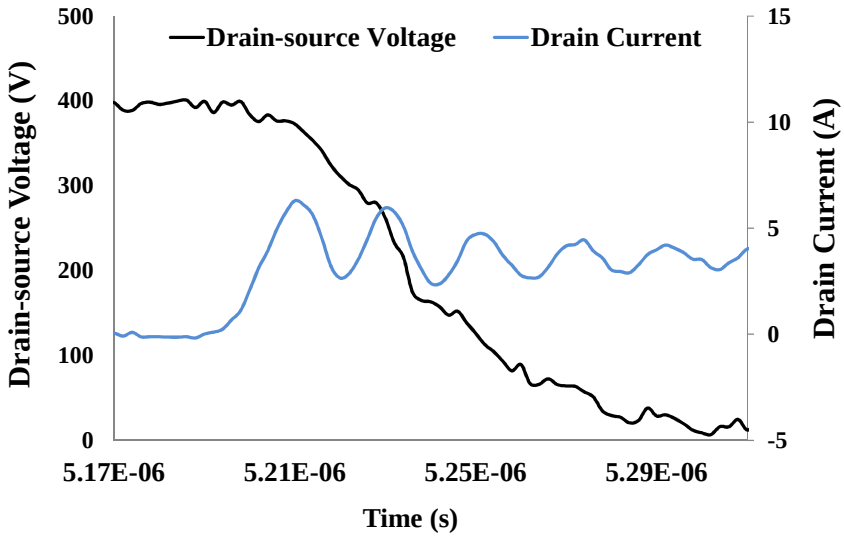


Figure 3.8: Drain current and drain-source voltage of the CoolMOS in the CoolMOS-SiC diode combination at 100 kHz switching frequency

The data in figure 3.9 shows the power efficiency as a function of converter switching frequency for CoolMOS-Ultrafast diode and CoolMOS-SiC Schottky diode combinations. The output voltage of the converter was regulated at $400V_{dc}$. In the case of the Fairchild ultrafast diode, due to the dramatically increasing diode turn-off switching losses with switching frequency, the diode case temperature increases from 55 °C to 101 °C as the frequency is increased from 100 kHz to 200 kHz. The CoolMOS turn-on losses increase from 13.6W to 34.9W resulting in the case temperature rising from 70 °C to 180 °C, which is well above the maximum junction temperature for a Silicon device; considering that the junction temperature is generally higher than the case temperature. Therefore the converter efficiency decreases from 93.9% to 90.9% when increasing the switching frequency from 100 kHz to 200 kHz for this device combination.

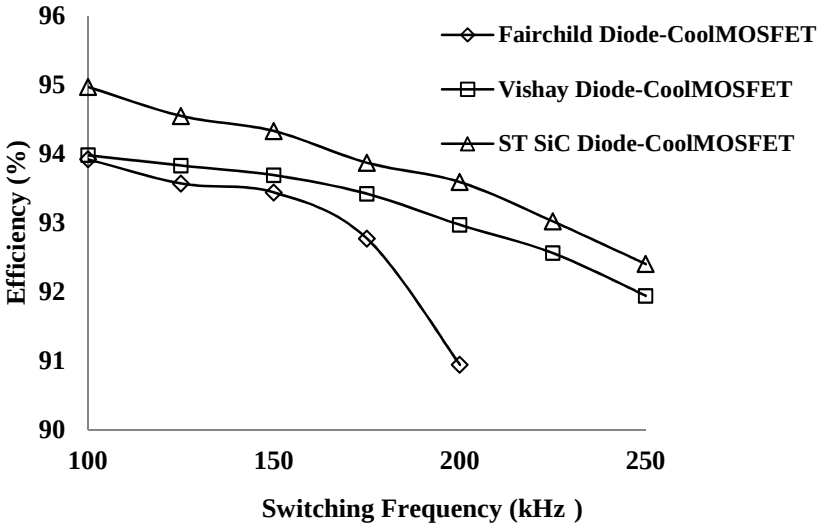


Figure 3.9: Power efficiency against switching frequency for CoolMOS-ultrafast diode and CoolMOS-SiC JBS diode combinations

The converter based on Vishay ultrafast diode and CoolMOS shows improved high frequency performance due to the lower reverse recovery charge of 70.65nC compared to 90.87nC for the Fairchild device. The CoolMOS turn-on losses increase from 12.9W at 100 kHz to 32.1W and 42.1W at 200 kHz and 250 kHz, respectively. The MOSFET case temperature increases from 59 °C at 100 kHz to 114 °C at 200 kHz and 165 °C at 250 kHz, resulting in the converter efficiency decreasing from 94.0% to 92.9% and 91.9% with increasing switching frequency.

Increasing the switching frequency from 100 kHz to 250 kHz in the converter based on SiC JBS diode and CoolMOS resulted in increasing the CoolMOS turn-on losses from 9.1W to 31.64W hence increasing the MOSFET case temperature from 55 °C at 100 kHz to 98 °C at 200 kHz and 142 °C at 250 kHz. This is an improvement in efficiency over the converter based on the Vishay Si ultrafast diode, resulting a 92.5% efficiency at 250 kHz. The SiC JBS diode is therefore used for the SiC FET evaluation to enable fast switching times while keeping the switch junction temperature below the limit.

The data in figure 3.10 shows the efficiency, CoolMOS total power loss and case temperature measurements of the converter as a function of frequency at 210V input voltage and 160 Ω load. For the CoolMOS-SiC diode combination, the increase in switching frequency results in an efficiency reduction from 95% to 92.5%. Increasing

the switching frequency from 100 kHz to 250 kHz in the converter resulted in increasing the CoolMOS total power losses from 13.4W to 42.6W. This increased switching loss increases the junction temperature which increases the conduction loss due to the increased on-resistance, and the efficiency decreases further.

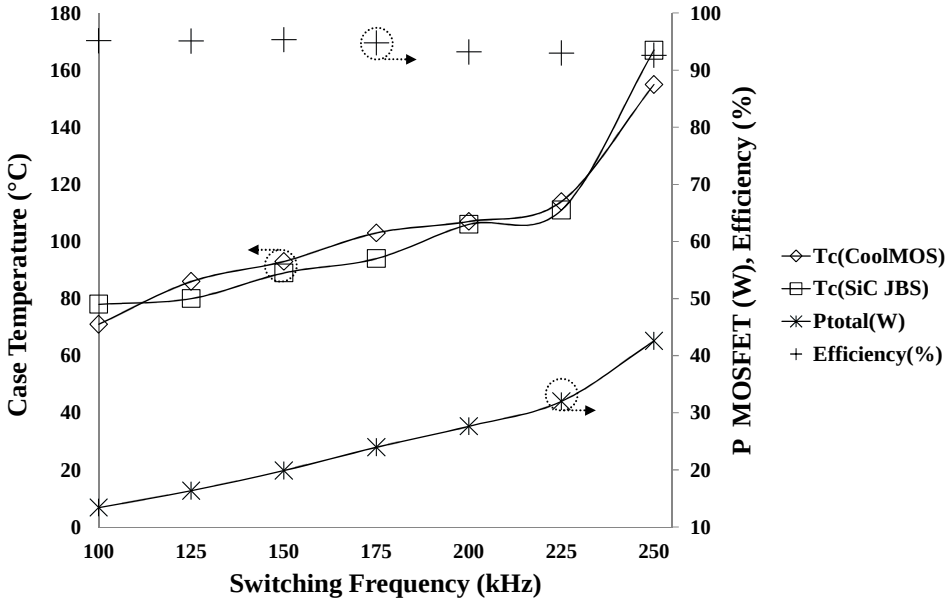


Figure 3.10: System performance metrics as a function of switching frequency for CoolMOS-SiC JBS diode combination

3.2.2.2 All SiC DC-DC Converters

The data in figures 3.11 (a) and 3.11 (b) show the turn-on and turn-off switching transients of the SiC JBS diode-SiC MOSFET based converter at 400V output voltage and 100 kHz switching frequency, respectively. The ultrafast driver with gate pulse voltage of -2V to 20V was used for the SiC MOSFET to achieve very fast switching despite the modest transconductance of the SiC MOSFET in comparison to the Silicon CoolMOS device. Figure 3.12 shows the thermal image of the SiC MOSFET converter using the ultrafast isolated gate driver operating at 100 kHz switching frequency.

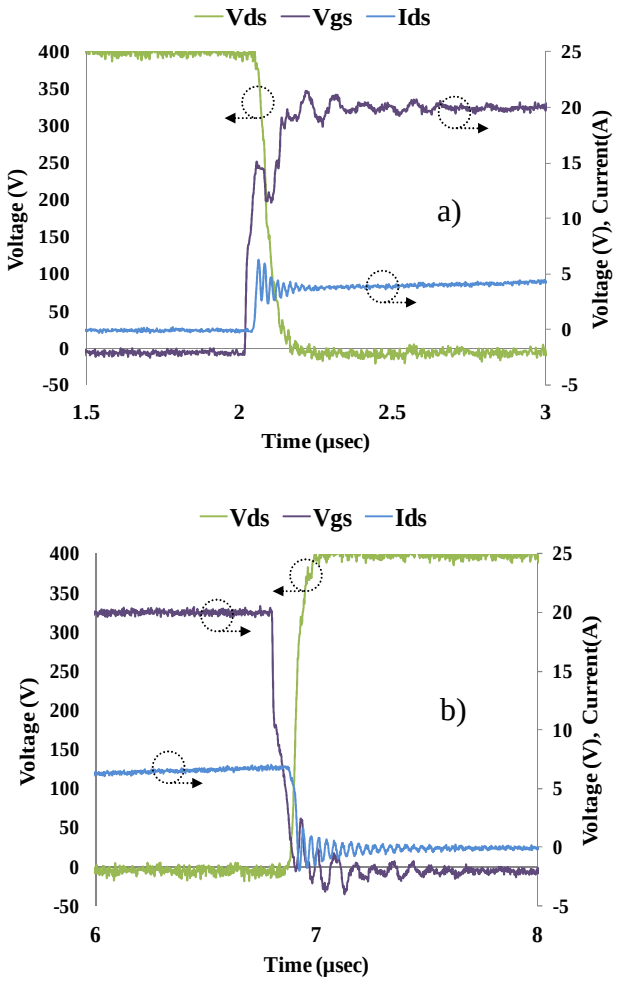


Figure 3.11: Turn-on (a), turn-off (b) switching transients for SiC MOSFET based converter at 400V V_{out} and 100 kHz switching frequency

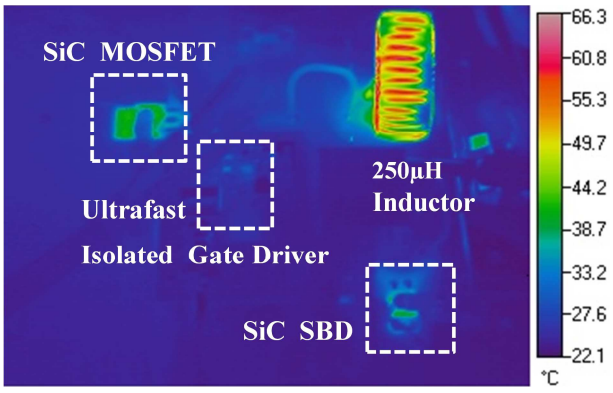


Figure 3.12: Thermal image for the SiC MOSFET based converter operating at 100 kHz switching frequency

To examine the effect of a negative gate voltage during off-state, power efficiency, SiC MOSFET total power loss and temperature measurements for zero

and -2V gate voltage at 210V input voltage and 160 Ω load are shown in figure 3.13. The output voltage of the converter was regulated at $400V_{dc}$. Increasing the switching frequency from 100 kHz to 250 kHz leads to an increase in the FET total power loss resulting in an increase in junction temperature. The use of a negative gate-voltage at turn-off minimises both the turn-on and turn-off power losses of the SiC MOSFET. The turn-on losses are reduced from 8.1W to 7.8W and from 23.3W to 22.4W at 100 kHz and 250 kHz, respectively. The turn-off losses show a greater reduction and are reduced from 3.3W to 2.3W and from 8.2W to 5.3W at 100 kHz and 250 kHz, respectively. The overall power losses are reduced and the SiC MOSFET case temperature drops from 49 ºC to 43 ºC and from 108 ºC to 98 ºC at 100 kHz and 250 kHz, respectively.

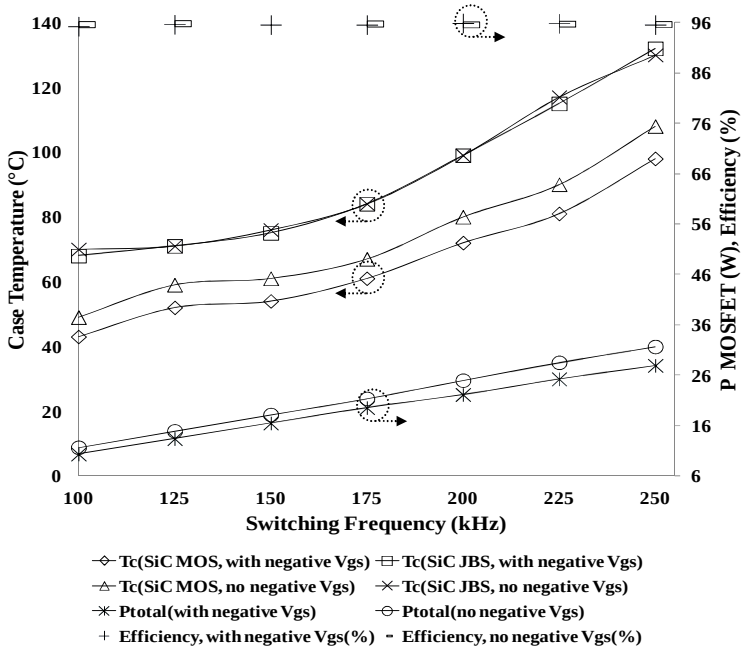


Figure 3.13: Relationship between the power efficiency and switching frequency for the SiC MOSFET-SiC JBS diode combination

As the elevated temperature does not greatly increase the total power losses in the SiC MOSFET, the observed converter power efficiency does not decrease significantly and remains at approximately 95.5%. This may be explained by the reduced conduction power losses in the passive components, due to the reduced current ripple at higher frequencies. Figure 3.14 shows this effect with the thermal images for the power inductor in the circuit at 100 kHz and 200 kHz switching frequencies. At 200 kHz switching frequency, the current ripple is halved and the RMS content of the

current is therefore reduced, resulting in reduced copper losses. As the copper loss dominates the core loss in this ferrite inductor the overall temperature rise is then reduced.

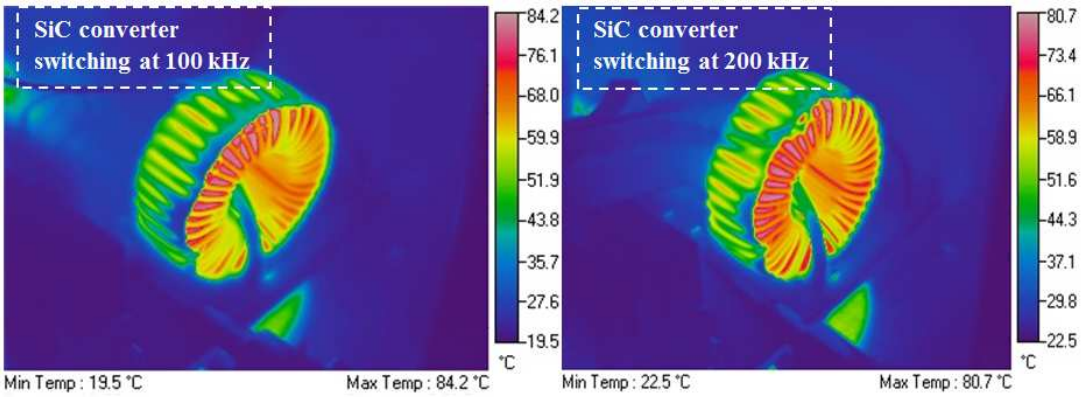


Figure 3.14: Thermal images of power inductor in the SiC MOSFET based converter at 100 kHz and 200 kHz switching frequencies

Even though a negative gate voltage was utilised to allow gate immunity at higher temperatures (due to the reduced MOSFET threshold voltage and instability when operating at elevated temperatures), the results in figure 3.13 show a 10 ºC temperature drop in the MOSFET when using a -2V gate-source voltage during off-time and no significant change in the diode junction temperature. With zero gate voltage during off-time, both the MOSFET turn-on and turn-off power losses increase, which increases the on-resistance and conduction losses, due to the increased junction temperature. Increasing the switching frequency from 100 kHz to 250 kHz leads to an increase in the FET total power loss from 11.7W to 31.7W and from 10.3W to 27.9W for zero and -2V gate voltage, respectively.

As the drain current is not controlled, when the MOSFET's on-resistance increases with temperature, thermal runaway can occur. This was tested for the SiC MOSFET at frequencies between 100 kHz and 250 kHz. The dependence of the SiC MOSFET case temperature during turn-on and turn-off is plotted in figure 3.15 (a). The converter was first switched on until the MOSFET case temperature stabilised and then the converter was turned off until the MOSFET case temperature returned to the starting value. All the temperature measurements have been taken at 2 second intervals. Exponential functions have been fitted to the data during the rise and fall times to obtain the thermal time constants at different switching frequencies. The similarity of the time

constants during the rise and fall times show no thermal runaway condition in the SiC power converter for the switching frequencies studied here. If the time constants during rise times were significantly faster than those of the fall times, the MOSFET would most likely go to a thermal runaway. Figures 3.15 (b) and 3.15 (c) show thermal images of the SiC MOSFETs in the steady state at switching frequencies of 100 kHz and 200 kHz, respectively.

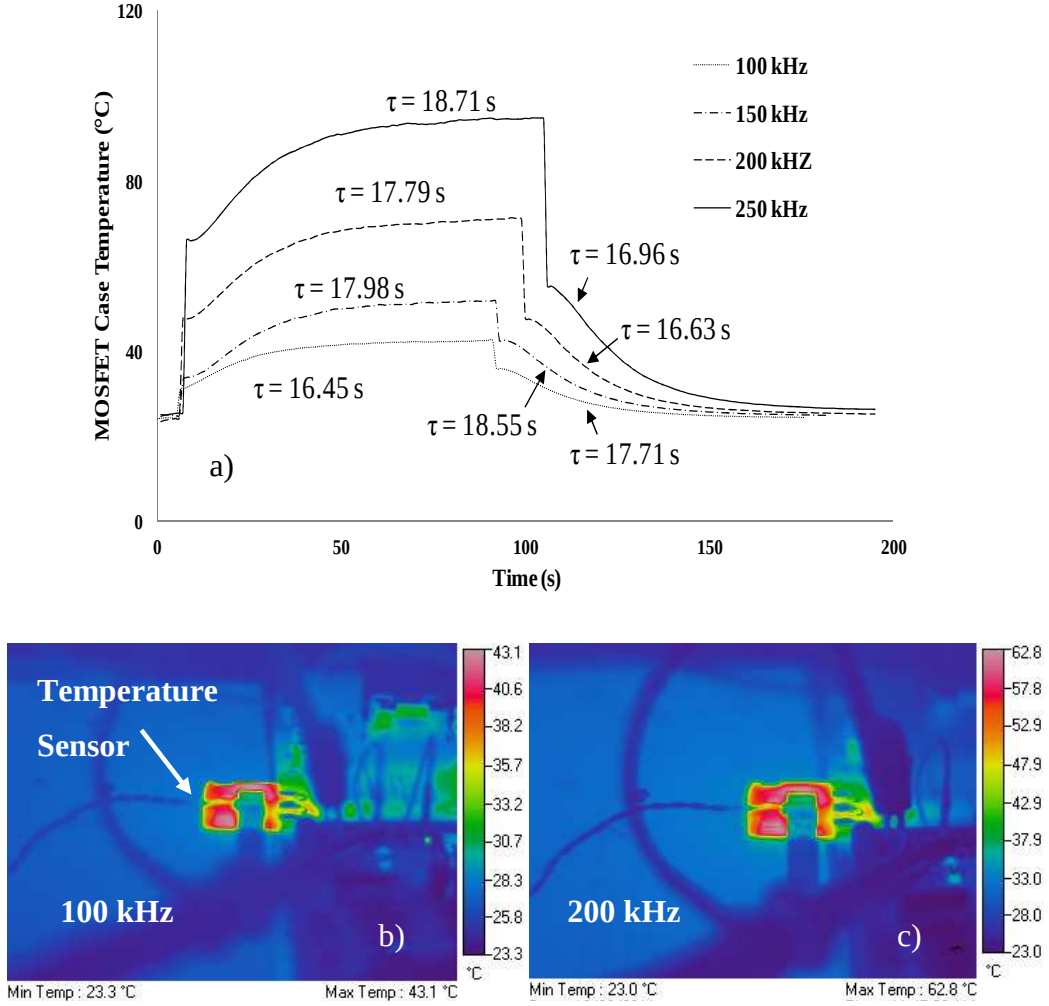


Figure 3.15: SiC MOSFET case temperatures during turn-on and turn-off at 100, 150, 200 and 250 kHz switching frequencies (a), thermal images of the SiC MOSFET in the steady state switching at 100 kHz (b) and 200 kHz (c)

The SiC MOSFET power losses, efficiency and case temperature as a function of input voltage at 100 kHz and 160 Ω load are plotted in figure 3.16; the data is for the case with a -2V gate-source voltage during off-time. The measurements were taken at a fixed duty cycle of 44%; this is to regulate the output to $400V_{dc}$ at a 210V input voltage.

The significant increase in MOSFET turn-on power loss is due to the increased reverse recovery loss in the SiC diode, which results from the increased voltage and current, and hence the switch junction temperature increases. The data in figure 3.17 shows the effect of converter loading by adjusting the load resistor from 160 Ω (2.5A) to 320 Ω (1.25A) at 210V input voltage and 100 kHz switching frequency. The output voltage of the converter was regulated at $400V_{dc}$. The converter efficiency decreases from 95.5% to 90.5% as the load changes from full load (2.5A/160Ω) to half load (1.25A/320Ω). Under high load conditions, the SiC MOSFET power losses, which are dominated by the turn-on power losses, increase rapidly and the power efficiency shows a significant decrease.

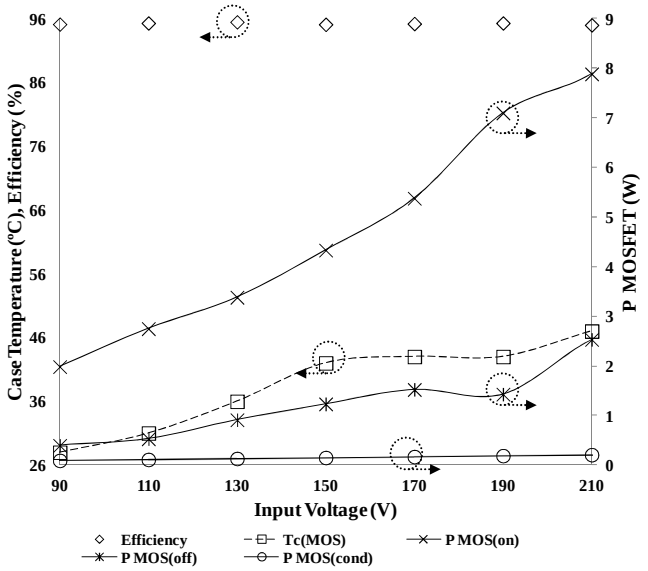


Figure 3.16: Relationship between the power efficiency and input voltage for the SiC MOSFET-SiC JBS diode combination

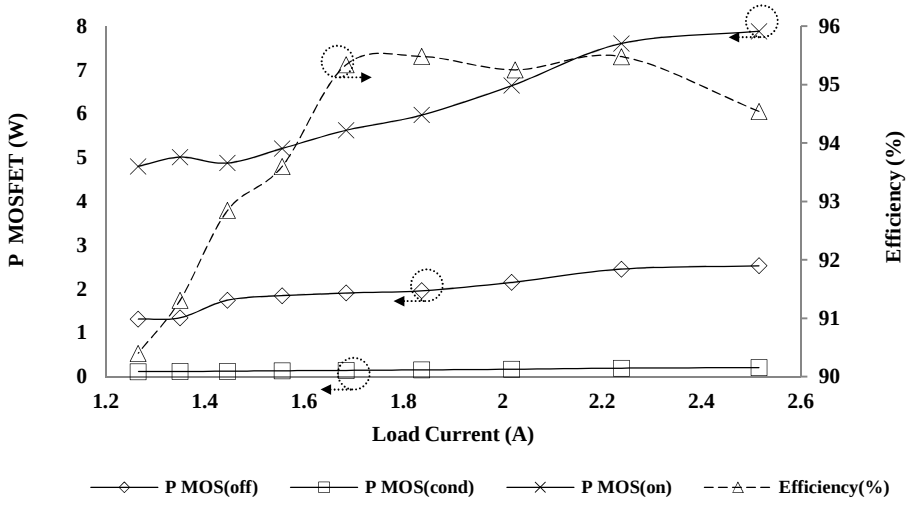


Figure 3.17: Relationship between the power efficiency and load current for the SiC MOSFET-SiC JBS diode combination

A ±13V external supply was used to power the two-stage DC-coupled gate drive circuit for the SiC JFET. The gate voltage and current waveforms of the SiC JFET during turn-on and turn-off transitions at 100 kHz switching frequency are shown in figures 3.18 (a) and 3.18 (b), respectively. During the turn-on transition, a 10V gate pulse is applied for 100ns to speed up the turn-on transition [42] with a 4A gate current-spike. This is to achieve very high switching speeds by rapidly charging the gate-source capacitance to the desired voltage level. This stage delivers the gate current for the on-state via the gate resistor. At a gate-source voltage of approximately 3V, a 7V voltage drop will be across the gate resistor causing high power losses.

Figure 3.19 shows the thermal image of the SiC JFET converter using the two-stage DC-coupled gate driver operating at 100 kHz switching frequency. There is a high temperature stress on the external gate resistor of the SiC JFET driver circuit, due to the higher gate current requirement of the SiC JFET and the high voltage drop cross the external gate resistor. To minimise this power loss during the on-state, a DC-DC converter is deployed to step down the gate voltage to approximately 6V hence the voltage drop is reduced. At high duty cycles and high frequencies, this power loss can still become significant [45].

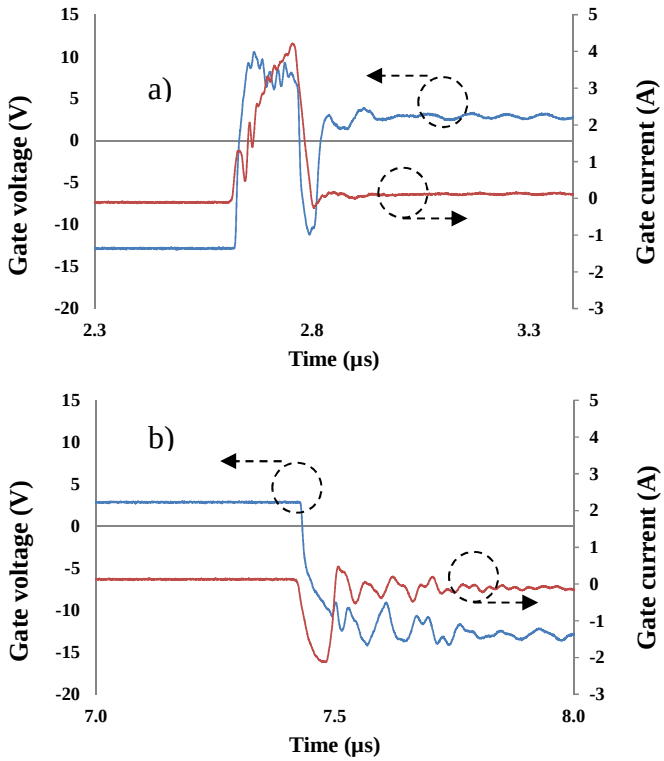


Figure 3.18: SiC JFET gate voltage and current waveforms during turn-on (a) and turn-off (b) transitions at 100 kHz switching frequency

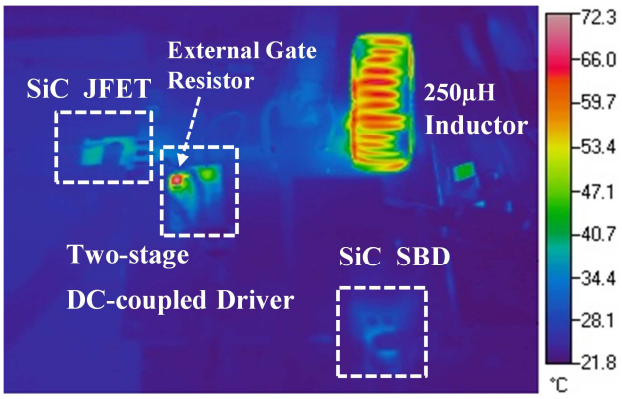


Figure 3.19: Thermal image for the SiC JFET based converter operating at 100 kHz switching frequency

The power losses, efficiency and case temperature of the SiC JFET as a function of switching frequency are plotted in figure 3.20. The output voltage of the converter was regulated at $400V_{dc}$. Increasing the switching frequency has resulted in an increased switching loss in the SiC JFET similar to that observed in the SiC MOS data shown in figure 3.13 and hence the junction temperature increases. This further increases the total switch power loss due to the increase in the JFET on-resistance with temperature. The converter efficiency peaks at 96% demonstrating a 0.5% efficiency improvement over the SiC MOSFET.

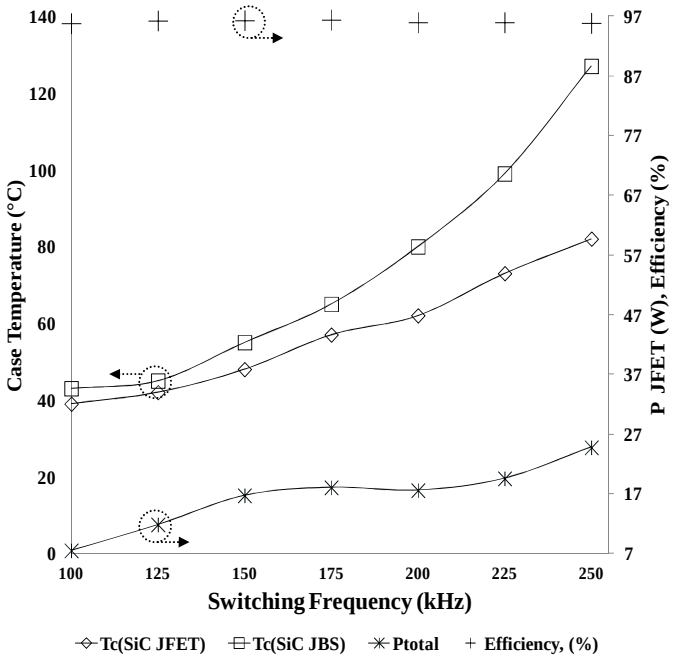


Figure 3.20: Relationship between the power efficiency and switching frequency for the SiC JFET-SiC JBS diode combination

The data in figure 3.21 shows the relationship between the FET switching losses and switching frequency for the Si CoolMOS, SiC MOSFET and SiC JFET based converters. The SiC JFET has lowest turn-off power loss of 1.3W and 2.8W at 100 kHz and 250 kHz, respectively. Although the SiC MOSFET shows higher turn-off power loss of 2.3W and 5.2W respectively, it still shows a weak frequency dependence similar to that of the SiC JFET. However, the Si CoolMOS has the highest turn-off power loss with a larger frequency dependence at frequencies above 200 kHz. In addition, the CoolMOS shows the highest frequency dependent turn-on loss resulting in 31.3W turn-on power loss at 250 kHz in comparison to 22W and 20W turn-on loss for the SiC MOSFET and SiC JFET, respectively. Consequently, the CoolMOS with an overall power loss of 42.6W at 250 kHz has the highest case temperature of 191 ºC. The SiC MOSFET and SiC JFET have a total power loss of 27.9W and 24.8W, and a case temperature of 98 ºC and 82 ºC at 250 kHz switching frequency, respectively.

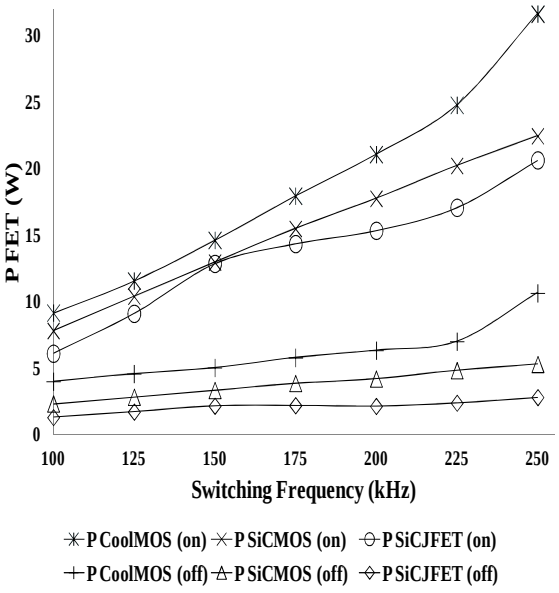


Figure 3.21: Relationship between the switching losses and switching frequency for the Si CoolMOS, SiC MOSFET and SiC JFET converters

The SiC JFET has lowest conduction loss of 0.15 W at 250 kHz when compared to 0.19W and 0.29W for SiC MOSFET and CoolMOS, respectively. The FET total power loss and case temperature as a function of frequency is plotted in figure 3.22. The lowest switching and conduction losses of the SiC JFET result in the lowest total power loss and junction temperatures. The rapid increase in the junction temperature of the

CoolMOS with increased switching losses results in an increased on-resistance, which increases the conduction power loss and takes the converter into thermal runaway condition at frequencies above 225 kHz.

Therefore, the converters based on SiC devices have shown the highest overall efficiencies. These efficiencies show only a weak frequency dependence, in contrast to the CoolMOS/SiC JBS diode combination, which demonstrated a 2.5% drop in efficiency when increasing the frequency from 100 kHz to 250 kHz.

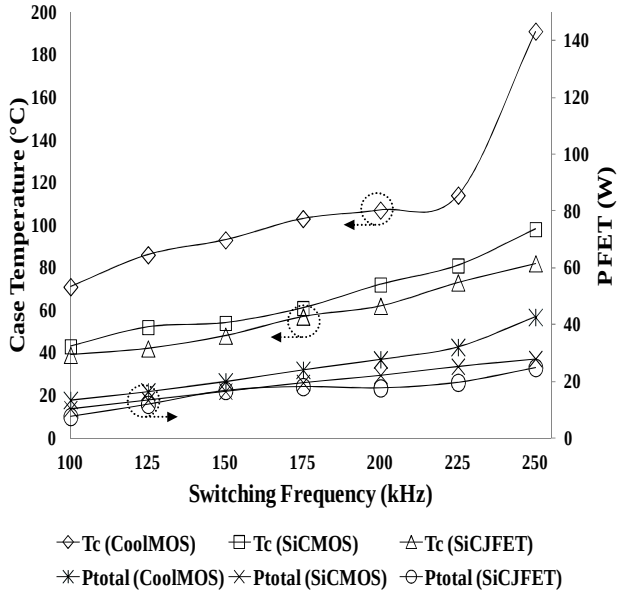


Figure 3.22: Relationship between the FET case temperature, total power loss and the switching frequency for the Si and SiC devices

3.3 Multilevel DC-DC Converters

Due to practical considerations, the voltage conversion ratio (VCR), defined as the ratio of the output voltage to the input voltage of a converter, is limited to six in conventional boost converter topologies [46]. This requires the use of an extremely high duty cycle (D) which leaves no scope for voltage regulation to compensate for load and line changes. An extremely high duty cycle in a boost converter also means that the diode sustains a high amplitude current with a short pulse width, resulting in severe

reverse recovery transients, which cause high electromagnetic interference (EMI) issues [46, 47]. These EMI issues affect system efficiency, cost and size. Thus, the use of high frequency SiC multilevel converters can find applications where a high boost ratio in a transformer-less DC-DC converter is required and the weight and power density are critical design parameters.

One of the challenges in PV systems is to link the DC renewable energy source with a multilevel inverter. It is desired that such links are self-balanced to avoid complex control strategies [48, 49]. To achieve a transformer-less DC-DC converter, a high voltage conversion ratio (VCR) is also desired. For renewable applications based on multilevel inverters, it is therefore required to design a DC-DC converter to overcome such issues by connecting the input PV array to the multilevel inverter with a self-balancing output voltage, unidirectional current flow and high VCR. An all SiC transformer-less DC-DC multilevel converter based on a traditional boost converter and the Cockcroft-Walton voltage multiplier [50-52] has been realised and the experimental results for the power loss and efficiency for a 3-level converter utilising SiC devices are presented.

3.3.1 The N+1 Level Multilevel DC-DC Converter

The schematic for an N+1 level multilevel converter proposed in [52] is shown in figure 3.23. The converter offers self-balancing that maintains the same output at all output levels, reducing the complexity of the control strategy [52, 53]. The proposed multilevel converter comprises a switching device, an inductor, 2N-1 capacitors and 2N-1 diodes.

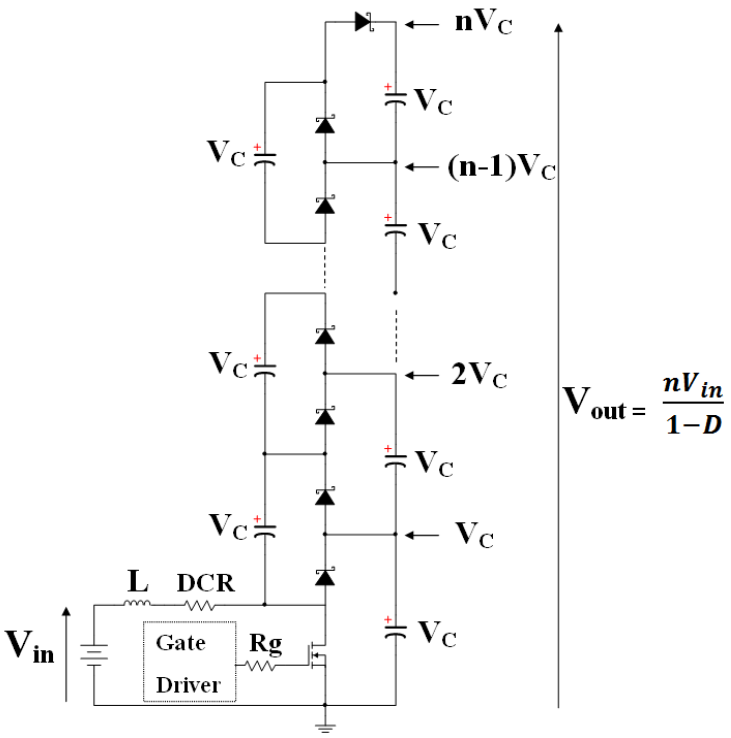


Figure 3.23: Schematic of the N+1 level DC-DC converter

To explain the principle of the converter operation, a 5-level boost converter is shown in figure 3.24. When the switch is on, if the voltage across C7 is greater than the voltage across C6, C6 is clamped by C7 via D6 and the switching device. Similarly, the voltage across C4+C6 is clamped by C5+C7 via D4 and the switch. When the switch is off, D7 conducts and C7 is charged. Now the voltage across C5+C7 is clamped by the sum of voltages across the inductor, C6 and the input voltage via D5. Similarly, the voltage across C3+C5+C7 is clamped by the sum of voltages across the inductor, C4+C6 and the input voltage via D3.

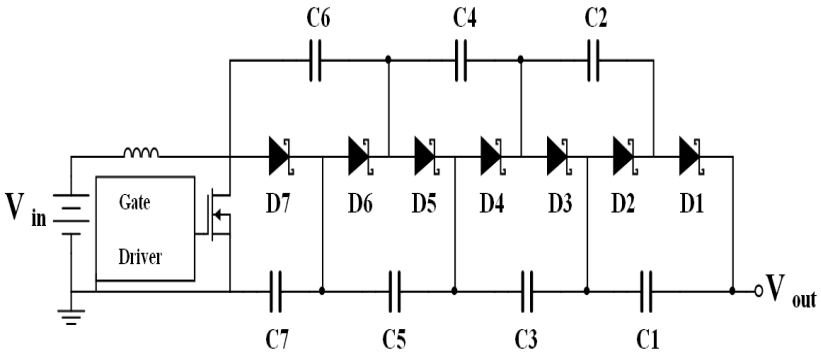


Figure 3.24: Schematic of the 5 level DC-DC converter

3.3.2 All SiC Multilevel DC-DC Converter

In this design, a 3-level multilevel converter is connected to a 3-level diode-clamped inverter as shown schematically in figure 3.25. The 3-level multilevel boost converter (MBC) is based on an inductor, a SiC MOSFET, 3 SiC Schottky diodes and 3 polypropylene film capacitors. The specifications of the 500W multilevel converter are shown in table 3.4.

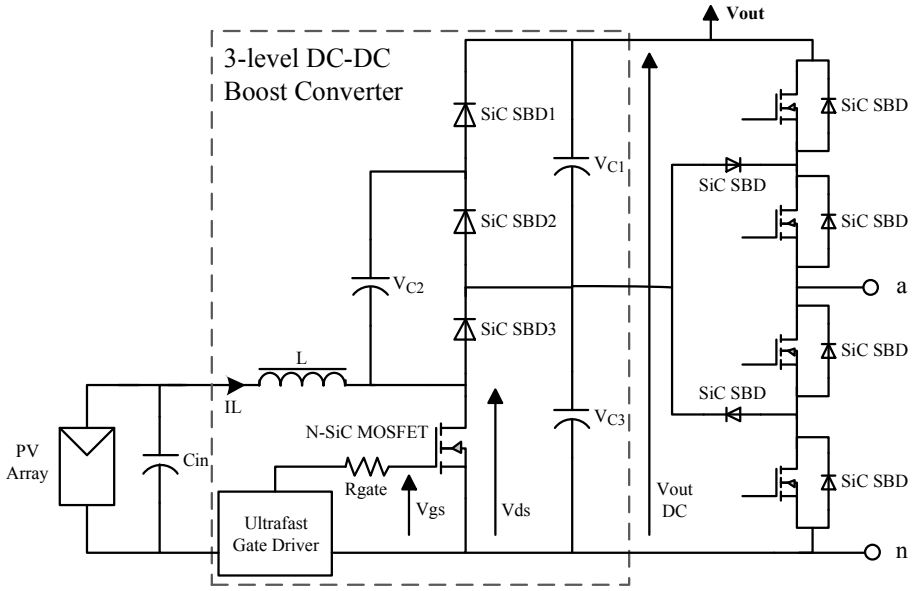


Figure 3.25: 3-level grid-connected PV inverter system

Converter Parameter	Value	Converter Parameter	Value
Input Voltage	105 V_{DC}	Switching Frequency	100 kHz
Output Voltage	400 V_{DC}	Input Inductor Value	250 µH
Output Power	500 W	Output Capacitors	3×5µF
Inductor Current Ripple	20% of $I_{L,\,avg}$	Max. Ambient/Junction Temperature	25°C/125°C
Output Voltage Ripple	2% of $V_{out,\,avg}$	External Cooling Requirements	None

Table 3.4: Summary of design requirements and passive power component values

The experimental realisation of the 105V-400V, 500W converter is shown in figure 3.26. Here, 3 600V, 8A SiC Schottky diodes (STPSC806) from ST Microelectronics were used to minimise reverse recovery charge and enable high switching speeds. As the reverse recovery current passes through the switching device during turn-on, the use of a diode with low reverse recovery charge minimises the turn-on power loss of the MOSFET and results in a lower overall power loss of the device. The gate voltage and current waveforms for the SiC MOSFET during the

turn-on and turn-off transitions at 100 kHz switching frequency are shown in figures 3.27 (a) and 3.27 (b), respectively. The ultrafast driver with gate pulse voltage of -2V to 20V was used for the SiC MOSFET to achieve very fast switching.

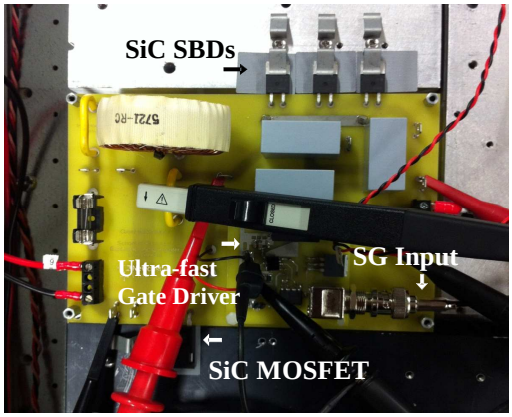


Figure 3.26: 3-level converter experimental setup

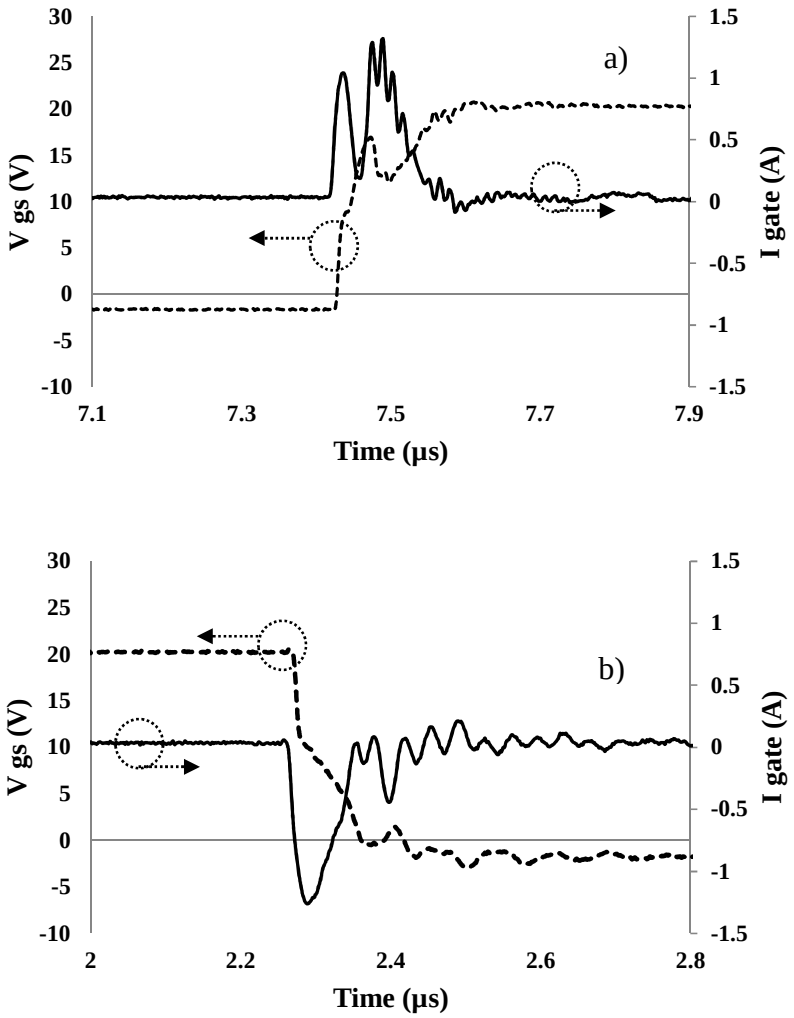


Figure 3.27: SiC MOSFET gate current and gate-source voltage waveforms during turn-on (a) and turn-off (b) transitions at 100 kHz switching frequency

The multilevel converter voltage and current waveforms are shown by the data in figure 3.28. In figure 3.25, when the SiC MOSFET is off, V_{C3} is charged via SBD3. The voltage across V_{C1} and V_{C3} is clamped via SBD1. When the MOSFET is on, V_{C2} is clamped by V_{C3} through SBD1 to the output. During the transition when the SiC MOSFET is turning on, the charging current of C2 via SBD2 imposes a current overshoot on the FET. In addition, both SBD1 and SBD3 are turning off during this transition hence the reverse recovery currents of these diodes will be added to the MOSFET turn-on current, resulting in a further increase in the turn-on power losses. The current pulse at the turn-on of the switch is likely due to the parasitic inductance in the circuit; resulting in resonance between the circuit parasitics and the sinusoidal shape of the current waveform at turn-on. The drain-source current of the MOSFET in figure 3.28 shows this overshoot in the current waveform. This demonstrates the benefits of using SiC diodes in this multilevel boost converter topology especially at higher number of levels. Figure 3.29 shows the thermal image of the multilevel converter at 105V input voltage and 100 kHz switching frequency.

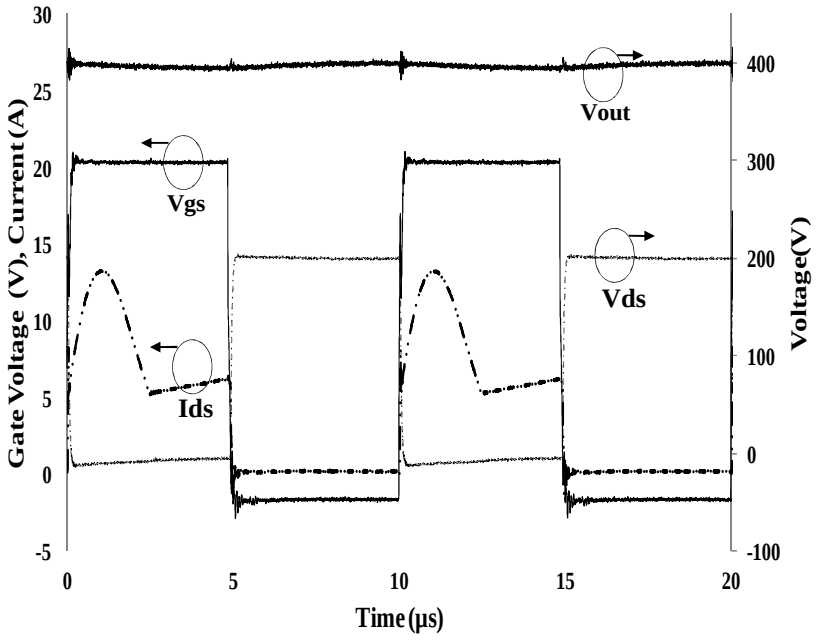


Figure 3.28: SiC converter current and voltage waveforms at 100 kHz

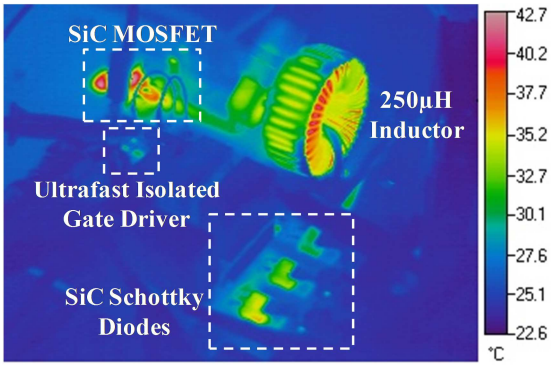


Figure 3.29: Thermal image of the SiC 3-level converter at 100 kHz

The SiC MOSFET power losses, efficiency and case temperature as a function of input voltage at 100 kHz switching frequency and 320 Ω load are shown by the data in figure 3.30. The large increase in MOSFET turn-on power losses is due to the increased reverse recovery loss of the SiC diodes as a result of the increased voltage and current, resulting in the junction temperature of the switch increasing from 30 °C to 40 °C. The increase in on-resistance with temperature results in a gradual increase in the converter conduction loss due to the increased on-resistance of the SiC MOSFET and the system efficiency decreases by 1% when increasing the input voltage from 55V to 115V.

The data in figure 3.31 shows the efficiency, SiC MOSFET power loss and case temperature measurements as a function of switching frequency at 105V input voltage and 320 Ω load. Increasing the switching frequency from 100 kHz to 250 kHz resulted in a steady increase in the FET turn-on power losses, resulting in the junction temperature increasing from 34 °C to 58 °C. This results in an increase in the turn-off power losses and so the 3-level converter power efficiency decreases from 95% to 90%. In addition to the reverse recovery current of SBD1 and SBD3, the charging current through C2 at turn-on, imposes a high level of stress on the FET, resulting in a further increase in the turn-on power losses as shown in figure 3.31.

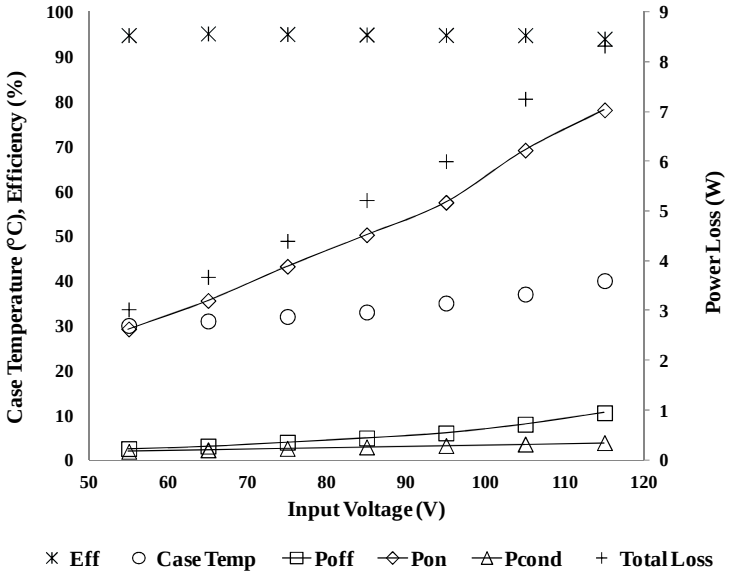


Figure 3.30: Power efficiency vs. input voltage

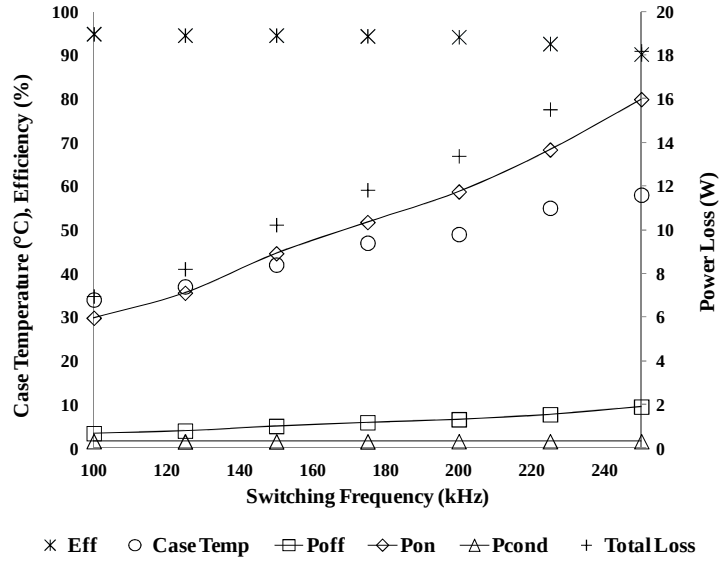


Figure 3.31: Power efficiency vs. switching frequency

Increasing the input voltage from 55V to 115V resulted in a decrease in efficiency from 95% to 94%, due to the increased turn-on loss of the MOSFET related to the increased reverse recovery loss of the SiC diodes by the increased input voltage. This resulted in 10 °C temperature rise in the switch junction temperature and 1% decrease in efficiency. Increasing the switching frequency from 100 kHz to 250 kHz

leads to an increase in the FET total power loss resulting in a 24 °C increase in MOSFET junction temperature and efficiency decreases by 5%.

3.4 Electromagnetic Interference in Si and SiC DC-DC Converters

DC-DC converters are a potential source of high frequency noise and power designers attempt to minimise and contain this noise around the converter to avoid affecting other systems or components. Therefore the allowable radiated emissions from electronic systems are controlled by regulatory agencies. Modular power products need to pass CISPR (international special committee on radio interference) standards that relate to EMC (electromagnetic compatibility). Here, the EMI measurements were taken to compare equivalent source strength of the converters rather than their capability to meet specific standards.

An Agilent E4403B ESA-L spectrum analyser with a frequency range of 9kHz-3GHz has been used for testing the radiated noise emissions. The receiver was used in the peak detector mode and with a step size of 50 kHz. Here, the frequency range of interest was selected between 20 MHz to 60 MHz. This range was selected in order to evaluate the radiated noise of the converters which is typically measured above 30 MHz [54, 55], and also to include the current and voltage ringing frequencies of the power converters under test during switching cycles.

The radiated EMI was measured with a broadband antenna from a distance of 2.5m. The near to far field transition occurs approximately at one-sixth of a wavelength from the receiving antenna [56]. Therefore, for the test frequency range of 20MHz-60MHz, a minimum distance of 2.5m is required. Before the start of noise measurement for each converter, a noise floor sweep was performed to try and evaluate the external interference onto the converter and ensure the noise at the point of receiver is similar for all the converters. Figure 3.32 shows the noise measurements with the high voltage power supply off and only the gate driver on.

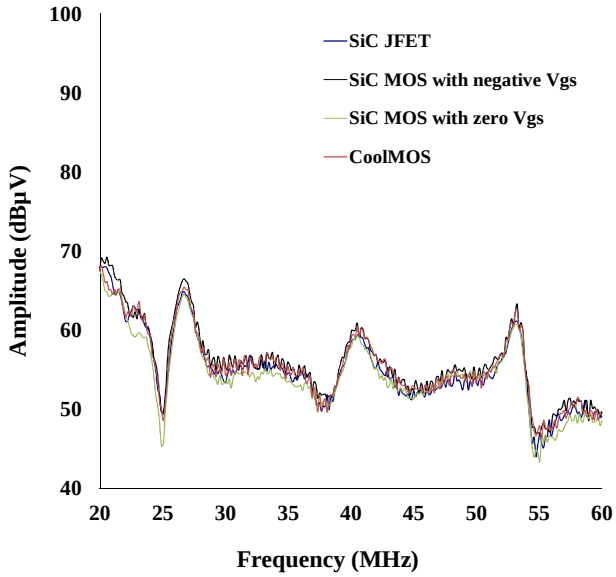


Figure 3.32: Radiated noise comparison of SiC JFET, SiC MOSFET and Si CoolMOS based DC-DC power converters at 100 kHz, only the gate drivers are powered

The data shows the noise floor for the converters based on Si CoolMOS, SiC JFET and SiC MOSFET with zero and negative gate bias at 100 kHz. As the high voltage power supply is off at this stage, there are no high di/dt and dv/dt and the noise levels are lower and are to do with the gate drive circuitry, characteristics of switching devices, stray inductance and capacitance in the circuit and the background noise.

A comparison of the radiated noise for SiC converters versus CoolMOS-SiC JBS diode based design at 100 kHz and 200 kHz switching frequencies is shown by the data in figures 3.33 and 3.34, respectively. The ringing frequency of the SiC JFET current waveform during the turn-on transition was measured as 54.1 MHz at 100 kHz and 54.5 MHz at 200 kHz switching frequency. The ringing frequency of the SiC MOSFET current-waveform during the same transition was measured as 53.5 MHz at 100 kHz and 53.1 MHz at 200 kHz switching frequency. During the turn-off transition, the SiC JFET ringing frequency was measured as 33.3 MHz and 32.2 MHz at 100 kHz and 200 kHz switching frequencies, respectively. During the same transition, the SiC MOSFET ringing frequency was measured as 27.8 MHz and 27 MHz at 100 kHz and 200 kHz switching frequencies, respectively. The SiC JFET current waveform at 100 kHz switching frequency is shown in figure 3.35. Both the turn-on and turn-off transitions with their respected ringing frequency are shown as well. Figure 3.36 shows the fast Fourier transform (FFT) of the SiC JFET current waveform in decibel (dB). As

can be seen both the turn-on and turn-off ringing frequencies of 54.1 MHz and 33.3 MHz, respectively, are clear in the frequency spectrum as shown in the figure inset.

These ringing frequencies shown in the noise graph lift the noise spectrum at these certain frequencies. These agree very closely with the highest noise level in the graph particularly in the 25-35 MHz range. The rate of current change dI_d/dt for the SiC JFET during the turn-on transition is the highest; 511A/µs at 100 kHz as opposed to 330A/µs for the SiC MOSFET without the negative bias. The rate of current change dI_d/dt for the SiC JFET during the turn-off transition is the highest as well; -405A/µs at 100 kHz as opposed to -313A/µs for the SiC MOSFET without the negative bias. This has resulted in higher radiated noise for the SiC JFET based converter. The SiC JFET with up to 20 dBµV higher radiated noise clearly shows the trade-off between radiated noise and power dissipation loss due to the increased dI_d/dt in comparison to MOS devices. The use of a -2V gate voltage for the SiC MOSFET also introduces up to 6 dBµV increase in the noise. The lowest observed noise for the SiC MOSFET can be explained by the lower gate capacitance of the device while using identical 7.5 Ω external gate resistors to achieve fastest switching and fair radiated noise comparison; as a slightly higher gate resistor for the CoolMOS could greatly reduce the radiated noise. Therefore the SiC MOSFET based converter shows the best trade-off between radiated noise and power dissipation loss.

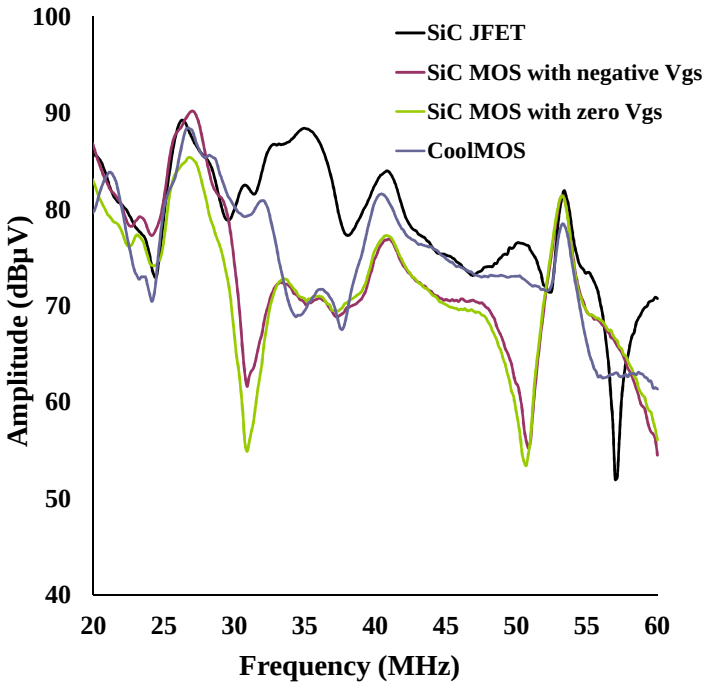


Figure 3.33: Radiated noise comparison of SiC JFET, SiC MOSFET and Si CoolMOS based DC-DC power converters at 100 kHz switching frequency

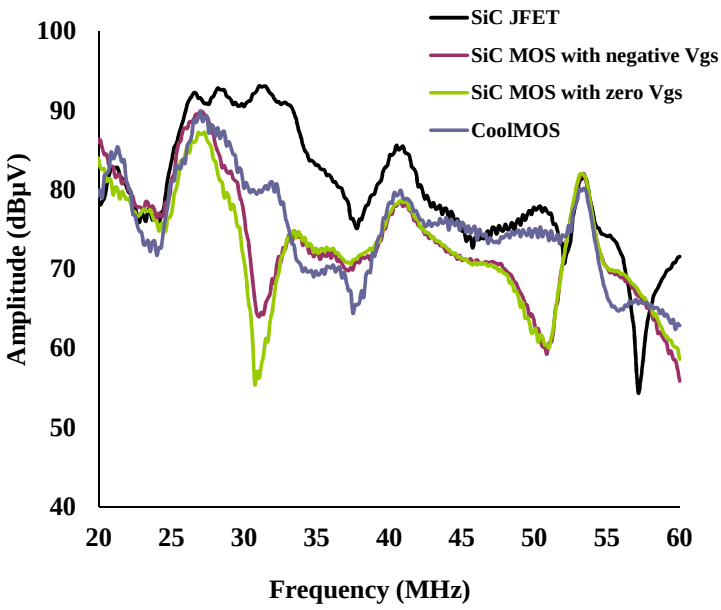


Figure 3.34: Radiated noise comparison of SiC JFET, SiC MOSFET and Si CoolMOS based DC-DC power converters at 200 kHz switching frequency

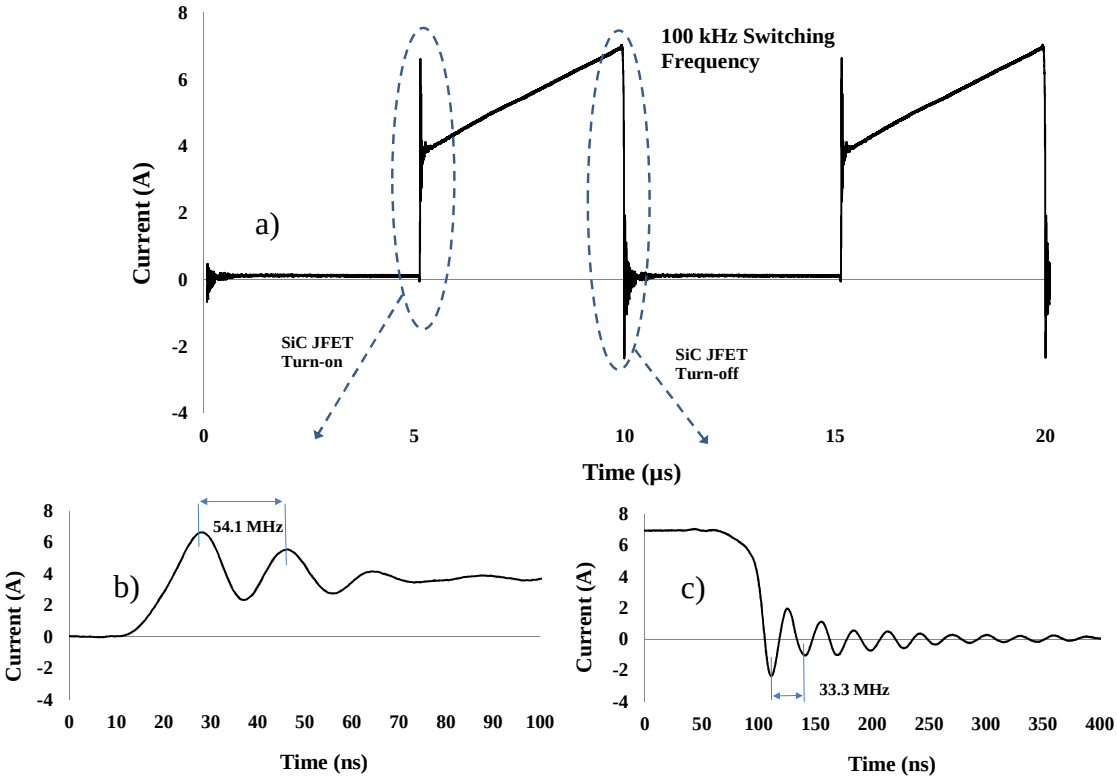


Figure 3.35: SiC JFET current waveform at 100 kHz switching frequency (a) and the ringing frequencies during turn-on (b) and turn-off (c)

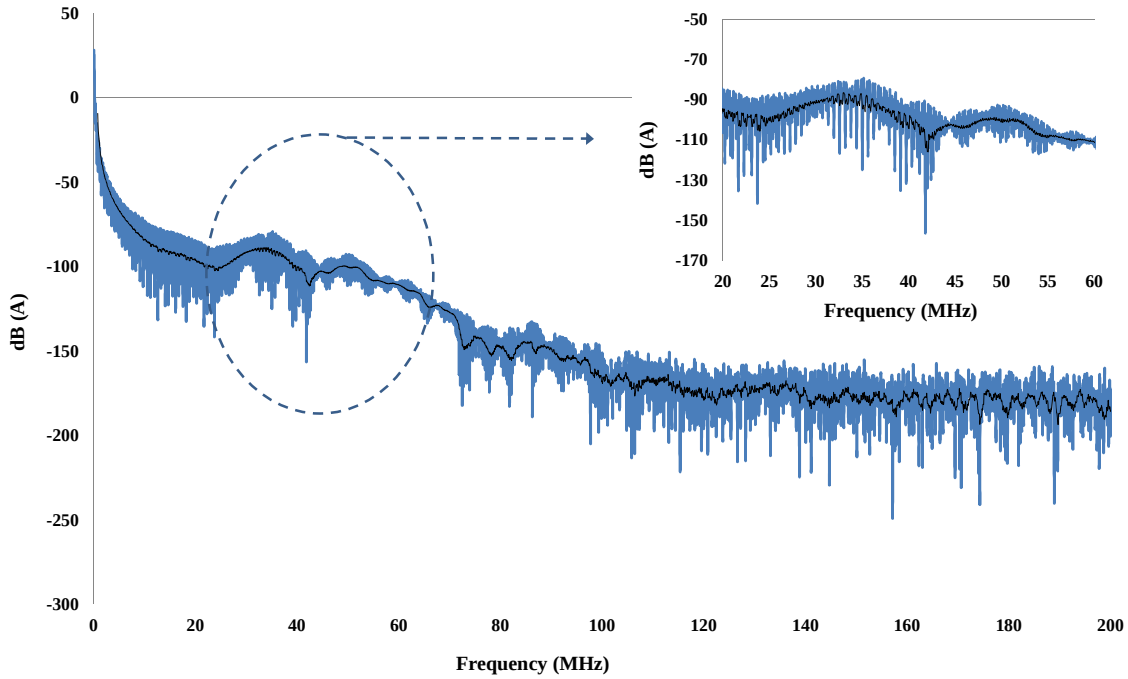


Figure 3.36: FFT of the SiC JFET current waveform in dB at 100 kHz switching frequency in blue, and the FFT average trace in black

To evaluate the noise spectrum of the 3-level boost converter, three 500W DC-DC converters were realised. As shown in table 3.5, three 500W DC-DC converters operating at 100 kHz switching frequency with a 400V output voltage have been evaluated. All the converters were based on SiC MOSFETs and SiC Schottky diodes used in the previous experiments. The gate driver has a negative bias of -2V during the turn-off for the SiC MOSFETs in all cases. Before the start of noise measurement for each converter, a noise floor sweep was performed to ensure the noise at the point of receiver is identical for all 3 converters.

	Test Combinations		
	I	II	III
Converter	Conventional Boost	Conventional Boost	3-Level Boost
Pout/ Vin /Vout	500W/ 210V/ 400V	500W/ 105V/ 400V	500W/ 105V/ 400V
VCR	1.9	3.9	3.9

Table 3.5: Test combinations used in noise evaluation of multilevel converter

The data in figure 3.37 shows the noise measurement results for the all-SiC converters. All three converters operate at 100 kHz switching frequency, have an output voltage of 400V and deliver 500W output power to a 320 Ω power resistive-load. The conventional boost converter with an input voltage of 105V has the highest radiated noise. For the same output power, this converter has the highest duty cycle of 75.2% to achieve 400V output voltage. Consequently, the input current increases that means the SiC MOSFET will have a higher drain current for the same drain-source voltage (400V) during switching transitions and therefore a higher radiated noise. The conventional boost converter with an input voltage of 210V operating at 48.6% duty cycle, has a 5 dBµV lower radiated noise than that of the converter with a 105V input.

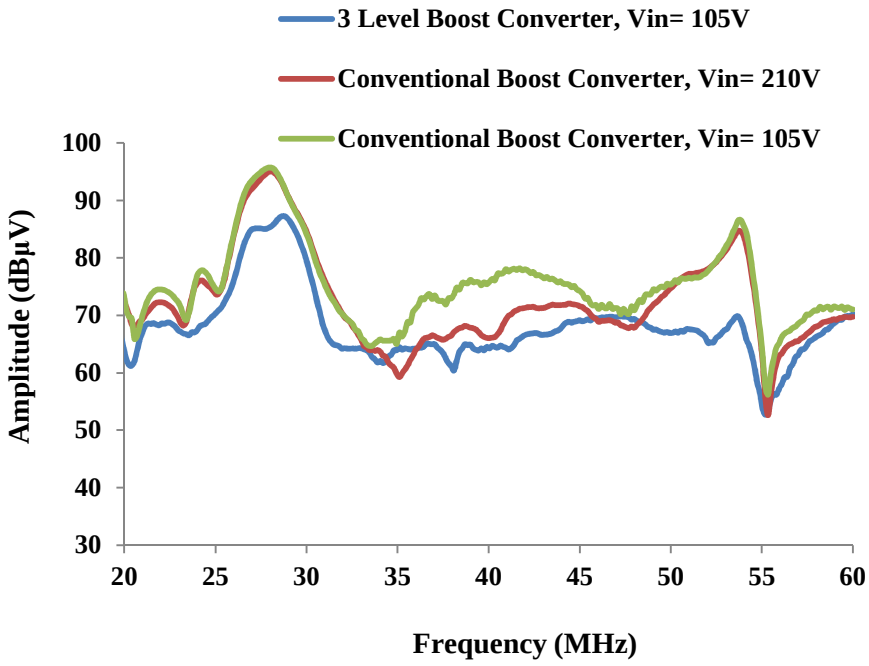


Figure 3.37: Radiation noise for 500W conventional and multilevel boost converters operating at 100 kHz and supplying the 500W load

The 3-level boost converter has the lowest noise level at 100 kHz switching frequency among the 500W power converters. The 3-level boost converter has a 15 dBµV lower radiated noise compared to both conventional boost converters. Although the 3-level converter operates at 49.1% duty cycle which is comparable with that of the conventional boost converter with 210V input voltage, the SiC MOSFET only experience 50% of the output voltage across the drain-source of the device during switching transitions and so has a lower noise level. Therefore the 3-level SiC boost

converter has twice the voltage conversion ratio and lower radiated noise compared to the conventional SiC boost converter with a 210V input voltage. Therefore, in PV inverter systems where the input voltages maybe lower, the use of the single-switch SiC based multilevel converter is a great choice; due to the high efficiency, high voltage conversion ratio, reduced noise, self-balancing output voltage and simplicity of the gate drive requirement.

3.5 Conclusions

The performance of SiC switches has been compared with ultra-high speed CoolMOS semiconductor switches in a 1kW PV pre-regulator DC-DC converter application. The high voltage, high frequency operation of the silicon carbide devices showed smaller switch overall power losses and junction temperatures. The converters based on SiC JFET and SiC MOSFET have shown overall efficiencies of 96% and 95.5%, respectively. This efficiency shows only a weak frequency dependence, in contrast to the CoolMOS/SiC JBS diode combination which demonstrated an efficiency drop from 95% to 92.5% when increasing the frequency from 100 kHz to 250 kHz. This is due to the rapid increase in switching and conduction power losses in the Si CoolMOS.

Even though the SiC JFET demonstrated 0.5% efficiency improvement, the larger current requirements at turn-on imposes a higher stress on the external gate resistor as well as the more complicated driver design requirements. A comparison of the radiated noise showed the highest noise signature for the SiC JFET and lowest for the SiC MOSFET in the 20MHz-60MHz range. The negative gate voltage requirement of the SiC MOSFET also introduces up to 6 dBµV increase in radiated noise, due to the induced current in the high frequency resonant stray loop in the negative power plane of the gate drive. The converter based on SiC MOSFET and SiC Schottky diode offers the best compromise between the converter efficiency and radiated noise.

In addition, a 500W all SiC transformer-less 3-level DC-DC converter was realised and the experimental data for the power losses and efficiency presented. The SiC MOSFET based 3-level converter has a 95% efficiency at a switching frequency of 100 kHz. This high efficiency transformer-less multi-level converter is suitable for renewable applications based on multilevel inverters. This design connects the input PV

array to the multilevel inverter with a self-balancing output voltage and unidirectional current flow. Three 500W 400V output converters based on SiC MOSFETs and SiC Schottky diodes were tested to evaluate the converter performance in terms of the radiated noise. The 3-level SiC boost converter showed a reduced noise of 15 dBμV in the test frequency range of 20MHz-60MHz. The high voltage conversion ratio of this SiC based multilevel converter topology without an excessively large duty cycle, reduced noise and high efficiency make it a great design choice for applications where both the performance and noise compliance are of great importance. In addition, the use of high frequency SiC multilevel converters in the transformer-less DC-DC converter is well suited for applications where the weight and power density are also critical design requirements.

3.6 References

[1] Z. Hui, et al., "Impact of SiC Devices on Hybrid Electric and Plug-In Hybrid Electric Vehicles," Industry Applications, IEEE Transactions on, vol. 47, pp. 912-921, 2011.

[2] M. S. Agamy, et al., "A High-Power-Density DC-DC Converter for Distributed PV Architectures," Photovoltaics, IEEE Journal of, vol. 3, pp. 791-798, 2013.

[3] L. Rixin, et al., "A High-Power-Density Converter," Industrial Electronics Magazine, IEEE, vol. 4, pp. 4-12, 2010.

[4] J. Biela, et al., "SiC versus Si-Evaluation of Potentials for Performance Improvement of Inverter and DC-DC Converter Systems by SiC Power Semiconductors," Industrial Electronics, IEEE Transactions on, vol. 58, pp. 2872-2882, 2011.

[5] B. Whitaker, et al., "A High-Density, High-Efficiency, Isolated On-Board Vehicle Battery Charger Utilizing Silicon Carbide Power Devices," Power Electronics, IEEE Transactions on, vol. 29, pp. 2606-2617, 2014.

[6] M. Pavlovsky, et al., "Pursuing high power-density and high efficiency in DC-DC converters for automotive application," in Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, 2008, pp. 4142-4148.

[7] N. Puqi, et al., "High-Temperature Hardware: Development of a 10-kW High-Temperature, High-Power-Density Three-Phase ac-dc-ac SiC Converter," Industrial Electronics Magazine, IEEE, vol. 7, pp. 6-17, 2013.

[8] H. Kosai, et al., "Design and Performance Evaluation of a 200 ºC Interleaved Boost Converter," Power Electronics, IEEE Transactions on, vol. 28, pp. 1691-1699, 2013.

[9] U. Badstuebner, et al., "Power density and efficiency optimization of resonant and phase-shift telecom DC-DC converters," in Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE, 2008, pp. 311-317.

[10] A. M. Abou-Alfotouh, et al., "A 1-MHz hard-switched silicon carbide DC-DC converter," Power Electronics, IEEE Transactions on, vol. 21, pp. 880-889, 2006.

[11] J. W. Kolar, et al., "PWM Converter Power Density Barriers," in Power Conversion Conference - Nagoya, 2007. PCC '07, 2007, pp. P-9-P-29.

[12] Y. Xibo, et al., "EMI Generation Characteristics of SiC and Si Diodes: Influence of Reverse-Recovery Characteristics," Power Electronics, IEEE Transactions on, vol. 30, pp. 1131-1136, 2015.

[13] G. Xun and J. A. Ferreira, "Comparison and Reduction of Conducted EMI in SiC JFET and Si IGBT-Based Motor Drives," Power Electronics, IEEE Transactions on, vol. 29, pp. 1757-1767, 2014.

[14] R. Redl, "Electromagnetic environmental impact of power electronics equipment," Proceedings of the IEEE, vol. 89, pp. 926-938, 2001.

[15] B. J. Baliga, "Trends in power semiconductor devices," Electron Devices, IEEE Transactions on, vol. 43, pp. 1717-1731, 1996.

[16] T. P. Chow, and R. Tyagi, “Wide bandgap compound semiconductors for superior high-voltage unipolar power devices,” IEEE Trans. Electron Devices, vol. 41, no. 8, pp. 1481-1483, Aug. 1994.

[17] P.G. Neudeck, et al., " Characterization of 6H-SiC JFET Integrated Circuits Over A Broad Temperature Range from -150 °C to +500 °C," Materials Science Forum, pp. 645- 648, 2010.

[18] M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and Si for power devices," Electron Devices, IEEE Transactions on, vol. 40, pp. 645-655, 1993.

[19] H. Morkoc, et al., "Large-band-gap SiC, III-V nitride, and II-VI ZnSe-based semiconductor device technologies," Journal of Applied Physics, vol. 76, pp. 1363-1398, 1994.

[20] R. Singh, et al., "SiC power Schottky and PiN diodes," Electron Devices, IEEE Transactions on, vol. 49, pp. 665-672, 2002.

[21] M. M. Hernando, et al., "Comparing Si and SiC diode performance in commercial AC-to-DC rectifiers with power-factor correction," Industrial Electronics, IEEE Transactions on, vol. 53, pp. 705-707, 2006.

[22] B. Ozpineci and L. M. Tolbert, "Characterization of SiC Schottky diodes at different temperatures," Power Electronics Letters, IEEE, vol. 1, pp. 54-57, 2003.

[23] A. Elasser, et al., "A comparative evaluation of new silicon carbide diodes and state-of-the-art silicon diodes for power electronic applications," Industry Applications, IEEE Transactions on, vol. 39, pp. 915-921, 2003.

[24] B. Ozpineci, et al., "A 55 kW three-phase inverter with Si IGBTs and SiC Schottky diodes," in Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE, 2006, p. 7 pp.

[25] R. Hefner, Jr., et al., "SiC power diodes provide breakthrough performance for a wide range of applications," Power Electronics, IEEE Transactions on, vol. 16, pp. 273-280, 2001.

[26] L. Bing, et al., "IPEM based high frequency PFC," in Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE, 2004, pp. 1200-1205 vol.2.

[27] L. Bing, et al., "Performance evaluation of CoolMOS/sup /spl trade// and SiC diode for single-phase power factor correction applications," in Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE, 2003, pp. 651-657 vol.2.

[28] B. Ray, et al., "High temperature operation of a dc-dc power converter utilizing SiC power devices," in Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE, 2005, pp. 315-321 Vol. 1.

[29] A. Agarwal, et al., "Advanced HF SiC MOS devices," in Power Electronics and Applications, 2009. EPE '09. 13th European Conference on, 2009, pp. 1-10.

[30] L. Rixin, et al., "A Shoot-Through Protection Scheme for Converters Built With SiC JFETs," Industry Applications, IEEE Transactions on, vol. 46, pp. 2495-2500, 2010.

[31] C. J. Cass, R. Burgos, F.Wang, and D. Boroyevich, “Three-phase ac buck rectifier using normally-on SiC JFETS at 150 kHz switching frequency,” in Proc. Power Electron. Spec. Conf., 2007, pp. 2162–2167.

[32] R. L. Kelley, et al., "Power factor correction using an enhancement-mode SiC JFET," in Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, 2008, pp. 4766-4769.

[33] M. S. Mazzola and R. Kelley, "Application of a Normally OFF Silicon Carbide Power JFET in a Photovoltaic Inverter," in Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE, 2009, pp. 649-652.

[34] S. B. Kjaer, et al., "A review of single-phase grid-connected inverters for photovoltaic modules," Industry Applications, IEEE Transactions on, vol. 41, pp. 1292-1306, 2005.

[35] L. Quan and P. Wolfs, "A Review of the Single Phase Photovoltaic Module Integrated Converter Topologies With Three Different DC Link Configurations," Power Electronics, IEEE Transactions on, vol. 23, pp. 1320-1333, 2008.

[36] J. L. Agorreta, et al., "Fuzzy Switching Technique Applied to PWM Boost Converter Operating in Mixed Conduction Mode for PV Systems," Industrial Electronics, IEEE Transactions on, vol. 56, pp. 4363-4373, 2009.

[37] N. Femia, et al., "A Technique for Improving P&O MPPT Performances of Double-Stage Grid-Connected Photovoltaic Systems," Industrial Electronics, IEEE Transactions on, vol. 56, pp. 4473-4482, 2009.

[38] Y. Bo, et al., "Design and Analysis of a Grid-Connected Photovoltaic Power System," Power Electronics, IEEE Transactions on, vol. 25, pp. 992-1000, 2010.

[39] R. J. Callanan, et al., "Recent progress in SiC DMOSFETs and JBS diodes at Cree," in Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE, 2008, pp. 2885-2890.

[40] B. Callanan, "Application Considerations for Silicon Carbide MOSFETs," CREE Application Note: CPWR-AN08, Jan, 2011.

[41] M. Gurfinkel, et al., "Characterization of Transient Gate Oxide Trapping in SiC MOSFETs Using Fast I-V Techniques," Electron Devices, IEEE Transactions on, vol. 55, pp. 2004-2012, 2008.

[42] R. Kelley, et al., "Improved two-stage DC-coupled gate driver for enhancement-mode SiC JFET," in Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE, 2010, pp. 1838-1841.

[43] C. Xing-Bi and J. K. O. Sin, "Optimization of the specific on-resistance of the COOLMOS," Electron Devices, IEEE Transactions on, vol. 48, pp. 344-348, 2001.

[44] L. Lorenz, et al., "COOLMOS-a new milestone in high voltage power MOS," in Power Semiconductor Devices and ICs, 1999. ISPSD '99. Proceedings., The 11th International Symposium on, 1999, pp. 3-10.

[45] B. Wrzecionko, et al., "Novel AC-Coupled Gate Driver for Ultrafast Switching of Normally Off SiC JFETs," Power Electronics, IEEE Transactions on, vol. 27, pp. 3452-3463, 2012.

[46] E. H. Ismail, et al., "High Conversion Ratio DC-DC Converters With Reduced Switch Stress," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 55, pp. 2139-2151, 2008.

[47] L. Huber and M. M. Jovanovic, "A design approach for server power supplies for networking applications," in Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE, 2000, pp. 1163-1169 vol.2.

[48] R. Davoodnezhad, et al., "A Novel Three-Level Hysteresis Current Regulation Strategy for Three-Phase Three-Level Inverters," Power Electronics, IEEE Transactions on, vol. 29, pp. 6100-6109, 2014.

[49] J. Rodriguez, et al., "A Survey on Neutral-Point-Clamped Inverters," Industrial Electronics, IEEE Transactions on, vol. 57, pp. 2219-2230, 2010.

[50] B. Axelrod, et al., "Diode-capacitor voltage multipliers combined with boost-converters: topologies and characteristics," Power Electronics, IET, vol. 5, pp. 873-884, 2012.

[51] Y. Chung-Ming, et al., "Cascade Cockcroft-Walton Voltage Multiplier Applied to Transformerless High Step-Up DC-DC Converter," Industrial Electronics, IEEE Transactions on, vol. 60, pp. 523-537, 2013.

[52] J. C. Rosas-Caro, et al., "Novel DC-DC Multilevel Boost Converter," in Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, 2008, pp. 2146-2151.

[53] J. C. Rosas-Caro, et al., "Voltage balancing in DC/DC multilevel boost converters," in Power Symposium, 2008. NAPS '08. 40th North American, 2008, pp. 1-7.

[54] N. Oswald, et al., "An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation With Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations," Power Electronics, IEEE Transactions on, vol. 29, pp. 2393-2407, 2014.

[55] B. Drury, The Control Techniques Drives and Controls Handbook. Lon-don, UK: Inst. Eng. Technol., 2009.

[56] EMC Design Guide for Printed Circuit Boards, 2002. Available: http://www.fordemc.com/.

Chapter 4. A SiC/SOI Based PWM Generator

4.1 Introduction

Recent developments in applications such as oil well exploration and aerospace have identified the need for high density, high temperature power electronic modules. Operating in environments beyond those possible using conventional silicon-based technology, the ability to control electrical systems will be a key enabler for future technology enhancements [1-6]. High temperature DC-DC converters have great potential for deployment in such environments. To realise these power modules, the relevant control circuitry also needs to operate at elevated temperatures. Any operating temperature outside the conventional temperate range of -55 ºC to 125 ºC, is unsuitable for the majority of integrated circuits used in industrial electronics or even military applications. For this goal to be achieved, these parts need to be able to operate at temperatures exceeding 175 ºC without or with limited cooling strategies [7-13]. As explained in chapter 2, the WBG materials and particularly SiC, have emerged as potential replacement semiconductors for Si, that has reached its theoretical limits. They are reports showing that SiC based devices can function at temperatures exceeding 500 ºC [14-18].

A gate driver is an essential part of any power electronic circuitry to control the switching of the power semiconductor devices by controlling the turn-on and turn-off operations of the semiconductor switching devices. The desire to place the gate driver physically close to the SiC power switches in the converter, leads to the necessity of a temperature resilient PWM generator to control the power electronics module [19-22]. As far as the gate driver is concerned, traditional complementary CMOS integrated circuits based on Silicon, can only operate reliably at temperatures below 125 ºC. The development and realisation of integrated converter modules capable of high temperature operation is therefore quite challenging. SiC based devices are promising to meet these challenges due to their higher thermal conductivity and increased operating temperature. Among the available SiC semiconductor devices, SiC MOSFETs are preferred the most; due to their enhancement mode of operation and compatibility with the design of Silicon gate-drive circuitry. The power modules based on SiC MOSFET

have been already commercialised, however, they are not high-temperature power modules. The high temperature modules based on SiC technology are still at the research level. Multi-chip modules based on SiC diodes and SiC MOSFETs reported operating at 200 ºC [23]. SiC JFET with various packaging techniques have also been used in power modules to effectively utilise high temperature capability of Silicon Carbide devices [24-27]. All these power modules are capable of functioning at temperatures exceeding 200 ºC thanks to the advancement in high-temperature packaging, however, to fully utilise the potential of these power modules, the gate driver needs to be located very close to the switching devices within the module. That is to reduce the parasitic effects, reduce the product volume and to achieve fastest switching speeds. Consequently, the gate-drive circuitry need to reliably function at elevated temperatures.

Researchers have implemented the gate-driver inside a SiC module using SOI active devices [28-31] and high temperature passives, enabling high temperature operation at 250 ºC. SiC inverters were similarly implemented based on SiC for high temperature operation; however, they are limited to the fact that only the buffer stage, the totem-pole output was realised using SOI semiconductors. Silicon-on-insulator (SOI) technology is also an attractive candidate for high temperature electronics due to the improved latch-up immunity, which enhances the HT operation reliability. It also provides reduced junction leakage currents due to the dielectric isolation [32]. The novelty of this work is in the first demonstration of a SiC based PWM and control circuit with SiC power semiconductor devices, which can demonstrate a full range of duty cycle. The proposed PWM circuit consists of several functional blocks that use SiC JFETs, in the oscillator and current source stages. The two SOI MOSFETs used in the amplification and control stages will be replaced by future high current SiC JFETs with minor modification to the circuitry. Figure 4.1 shows the block diagram of the proposed PWM generator circuit, including the SiC current source and ring oscillator stages.

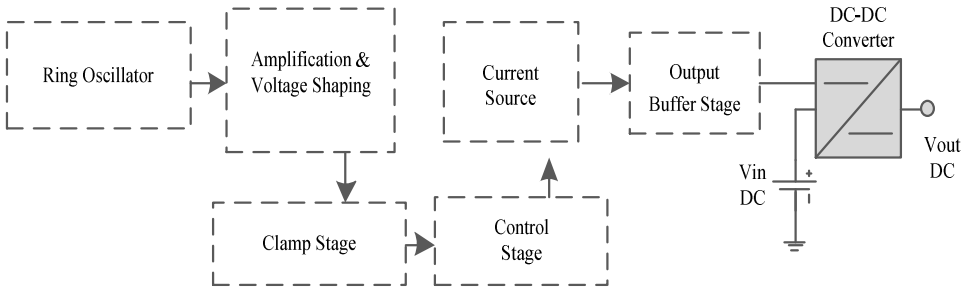


Figure 4.1: Schematic of the proposed gate driver comprising of six functional blocks

4.1.1 Silicon Carbide JFETs

Epitaxial 4H-SiC JFET devices were formed on wafers obtained from CREE [33]. The epitaxial layers were formed on highly doped N-type substrate, with a P (2×10^{15}, 7µm), N (1×10^{17}, 300nm) and P+ (2×10^{19}, 200nm) epitaxial structure. Following cleaning and isolation trench etching, high dose Nitrogen implants were made to form low-resistance contact areas in the N type region. A 30 minute, 1600˚C anneal was used to activate the implanted species, using a graphite cap to protect the surface [34]. A second etch step was then used to reveal the highly doped regions in the N type epitaxy and define the gate regions in the highly doped P type epitaxy. Following a dry oxidation process (6 hour, 1100˚C), Ti/Ni contacts were deposited on the N type epitaxy by E-beam and patterned by lift off. These were annealed in a vacuum (300s, 1050˚C) to form ohmic contacts. Ti/Al/Ti contacts were then deposited on the P type epitaxial structures by E-beam and patterned by lift off. These were annealed in a vacuum (300s, 950˚C) to form ohmic contacts. Gold contacts were then patterned onto the surface of all the contacts to facilitate wire bonding.

Low power normally-on, epitaxial SiC-JFETs with a gate width (W) and length (L) of 200µm and 9µm respectively, were fabricated at Newcastle University as described above. These devices show turn-off voltages of -3V at room temperature. The cross-section and I-V characteristic of the device are shown in figures 4.2 and 4.3, respectively.

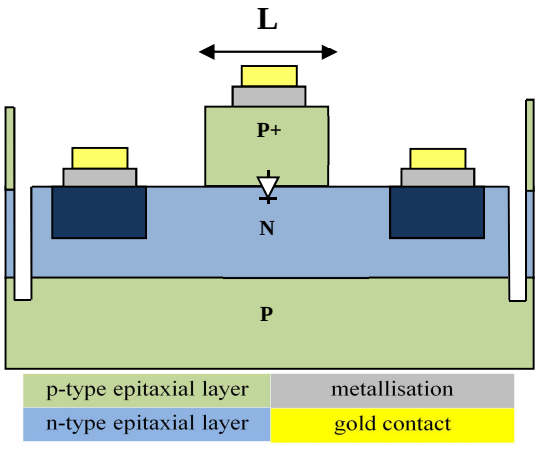


Figure 4.2: Cross section of the normally-on epitaxial n-channel SiC JFETs

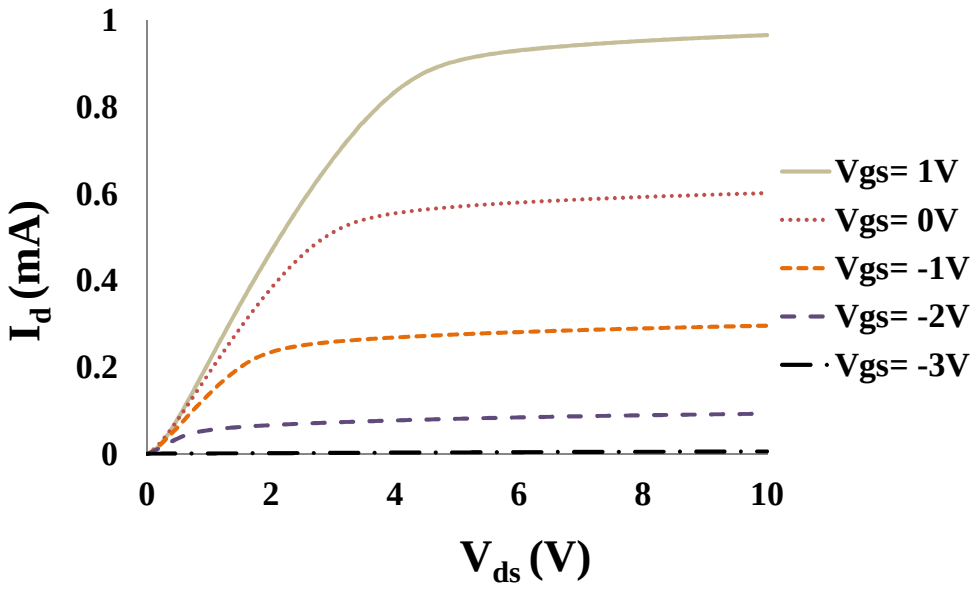


Figure 4.3: I-V characteristic of the normally-on epitaxial n-channel SiC JFETs at gate voltages of -3,-2,-1, 0 and 1V

4.1.2 The Ring Oscillator

Ring oscillators (RO) have become an essential part of many digital and communication systems due to their integrated nature. They find their applications as voltage-controlled oscillators (VCO), in disk-drive read channels, on-chip clock distribution and clock recovery circuits for serial data communications. Even though they are not commonly used in radio frequency (RF) applications, they can be used for some lower level RF systems [35]. An RO comprises of several gain stages in a unity gain feedback loop. The circuit must conform to the Barkhausen's criteria to achieve oscillation. It means that the gain and phase shift of the feedback loop must be 1 and 2π, respectively [36]. Figure 4.4 shows an RO consisting of N inverter stages.

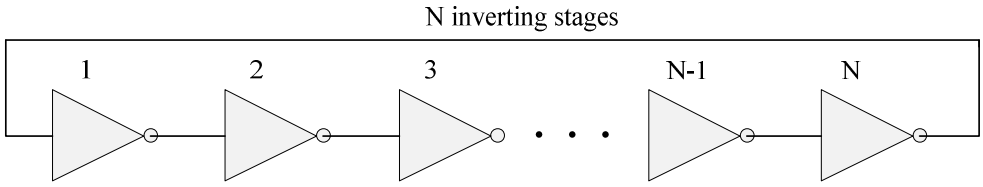


Figure 4.4: N-stage ring oscillator consisting N inverting stages with feedback loop

Each stage introduces a delay of t_d therefore with the total phase shift of 2π, the oscillation frequency is given in equation 4.1. N is the number of stages and is an odd number, which results in a self-oscillating circuit.

$$f = \frac{1}{2N \times t_d} \text{ [Hz]} \tag{4.1}$$

Since the oscillation frequency is determined by the delay in each stage and number of stages in the loop, frequencies in the MHz to GHz range are generally obtained. To use this ring oscillator to drive a power device in a DC-DC converter, frequencies in the range of hundreds of kHz are desired. To achieve this, one option would be to increase the number of stages in which case the number of stages would be unacceptably large and the other option would be to increase the delay for each stage. Much research has been done to increase the delay in each stage [37, 38]. If the delay can be voltage controlled, then an RO with variable frequency can be achieved. In [39] a dual ring oscillator is proposed that changes the number of inverter stages using a control voltage which is still unsuitable for low frequency applications. Here, the ring oscillator has been selected for our circuit design to avoid the use of bulky inductors hence the ease of integration, and their limited temperature range. SiC JFETs are used in the ring oscillator circuit and the oscillation frequency is tuned to a level suitable for the operation of DC-DC converters.

A 20V supply, a 22kΩ drain resistor, a 1nF decoupling capacitor between inverter stages and a 1nF capacitor between the gate and source of the JFET were used to construct a 3-stage ring oscillator as shown in figure 4.5. The simulation results for the ring oscillator are shown in figure 4.6. V(g) shows the gate voltage and V(d) shows the drain voltage of each inverting stage. The oscillation frequency of the RO is 26 kHz. The oscillation happens when the overall phase-shift is 180º; therefore each stage has a 60º phase-shift contribution. The waveform at each node is 120º out of phase with respect to its neighbouring nodes. Due to the signal inversion from the gate to the drain, each common source stage exhibits a phase shift of 180º. The time difference between the gate and drain voltages for each stage, as shown below, is due to the delay of the inverting stage.

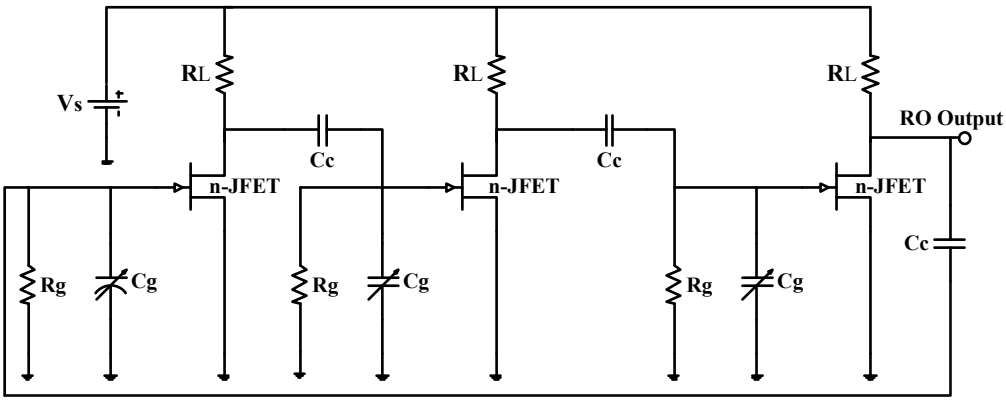


Figure 4.5: 3-stage ring oscillator consisting 3 inverting stages

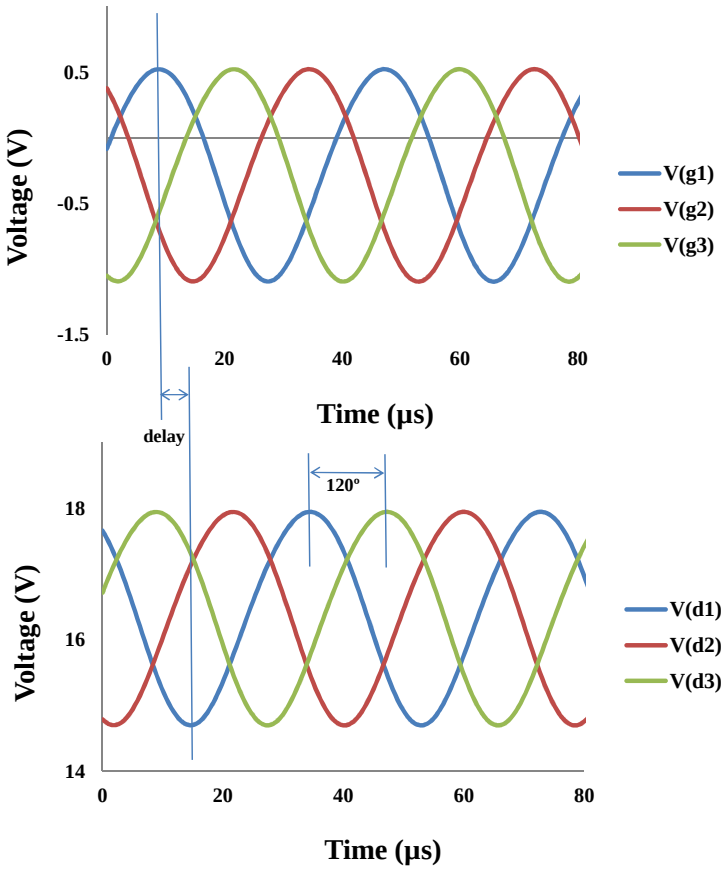


Figure 4.6: 3-stage ring oscillator consisting 3 inverting stages, gate and drain voltage waveforms are shown at the oscillation frequency of 26 kHz

Figure 4.7 shows the simulation result for the gate voltage of the first inverting stage for 3 different external gate-source capacitors to alter the delay of each inverter stage hence change the ring oscillator frequency to a level suitable for a DC-DC converter operation. Reducing the external gate capacitance from 1nF to 560pF and

100pF resulted in an increase in oscillator frequency from 26 kHz to 34 kHz and 111 kHz, respectively.

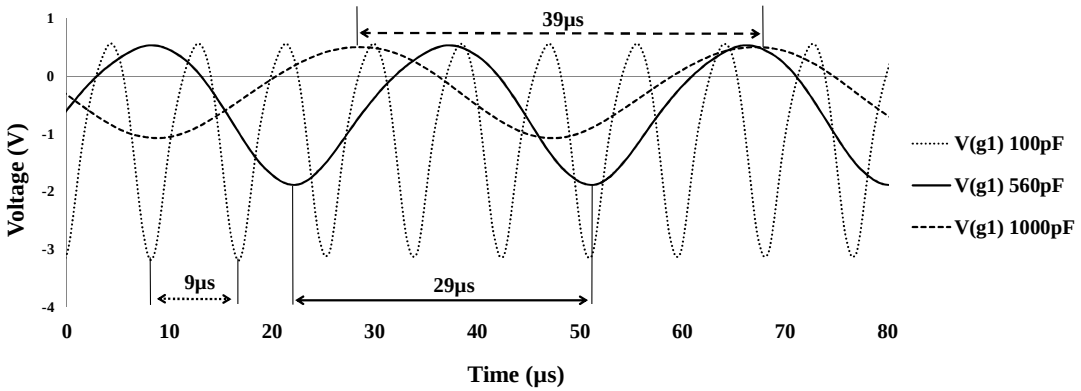


Figure 4.7: 3-stage ring oscillator frequencies with 3 different external gate-source capacitances of 100pF, 560pF and 1000pF

4.2 The Constant Current Source and the Adjustable Waveform Generator

Figure 4.8 shows a self-biased JFET based current source. At start-up when Vs is first applied, there is no drain current hence the gate-source voltage is zero and current starts to flow through the depletion mode device. As the current increases, so does the voltage drop across the source resistor, therefore the gate will be negatively biased with respect to the source. This reduces the current through the JFET and this cycle continues until equilibrium is established. If the drain current were to increase or decrease, the circuit regulates itself by negatively feeding back the output to the input. Equation 4.2 shows the relationship between the JFET current and gate-source voltage and gives the transfer characteristic of the JFET. I_{dss} is the drain to source saturation current when the V_{gs}= 0V and V_p is the pinch-off voltage of the device.

$$I_d = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2 \text{ [A]} \tag{4.2}$$

The intersection of the JFET transfer characteristic and the load line of the source resistor gives the DC bias point. The transfer characteristic curve of the epitaxial SiC JFET is shown in figure 4.9. The load lines for three source resistors are also plotted that demonstrate the current source operating points. By varying the source

resistor from 20kΩ to 5kΩ, the current source level can be adjusted between 80μA and 210 μA.

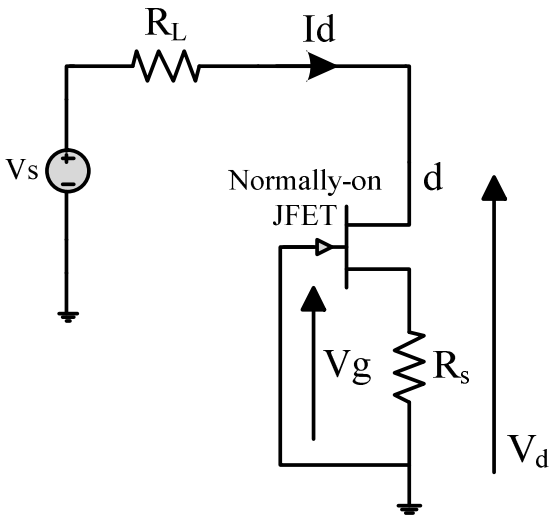


Figure 4.8: The self-biased JFET based current source

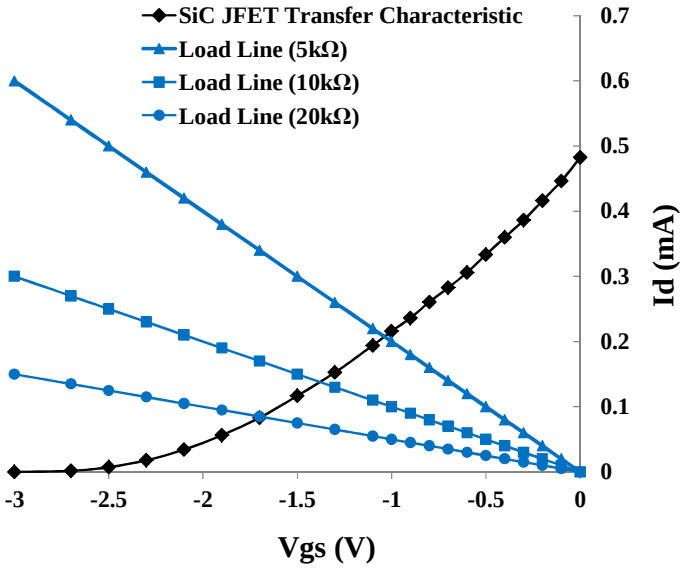


Figure 4.9: The transfer characteristic of the SiC JFET and the load lines for 3 different source resistors corresponding to three current source levels

As shown in equation 4.3, the slope of the transfer-characteristic curve is the transconductance of the SiC JFET. Substituting 4.2 into 4.3 and differentiating the result gives a linear relationship between the transconductance and gate-source voltage at a given drain-source voltage. The transconductance of the SiC JFET is shown in

figure 4.10. At V_{gs}=0V the transconductance equates to $2I_{dss}/|V_{p|}$ and at zero transconductance the gate-source voltage equates to the pinch-off voltage of the SiC JFET which is -3V.

$$g_m = \frac{dI_d}{dV_{gs}} = -2\,\frac{I_{dss}}{V_p}\left(1 - \frac{V_{gs}}{V_p}\right)\ [S] \tag{4.3}$$

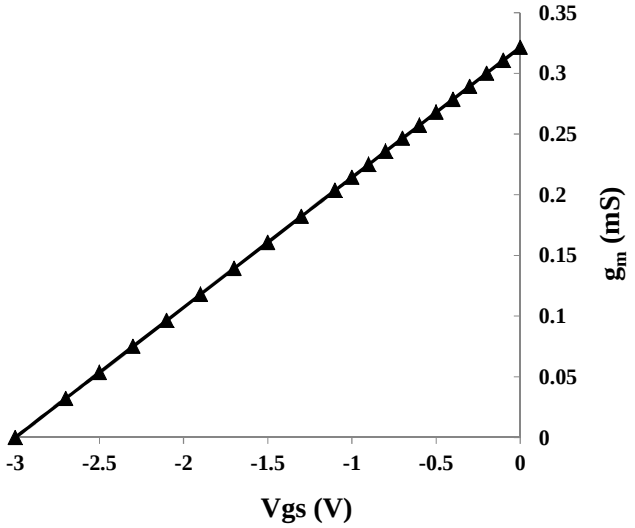


Figure 4.10: The transconductance characteristic of the SiC JFET

The proposed adjustable triangular waveform generator is shown in figure 4.11. It utilises a depletion mode SiC JFET, an enhancement mode SOI MOSFET, three resistors and a capacitor. The SiC JFET is configured as a constant current source (CCS) charging capacitor Cout. R_CCS sets the level of the constant current source and also introduces a negative feedback to regulate the desired source current of the JFET. Therefore the capacitor voltage will be a voltage ramp generated by the CCS. Vin turns on the n-MOS to reset the voltage across the output capacitor. The ramp voltage across the capacitor is discharged through R_LIM to ground. To operate the n-MOS in its safe operating area, R_LIM sets the suitable level for the capacitor discharge current. The output capacitor value needs to be selected carefully. If this value is too large a significant amount of energy needs to be charged and discharged and in case the value is too small then the stray capacitance in the circuit as well as the output load level will introduce unacceptable error in the charge-discharge functionality. Based on the voltage ramp design requirement, rate of voltage change in time, we have:

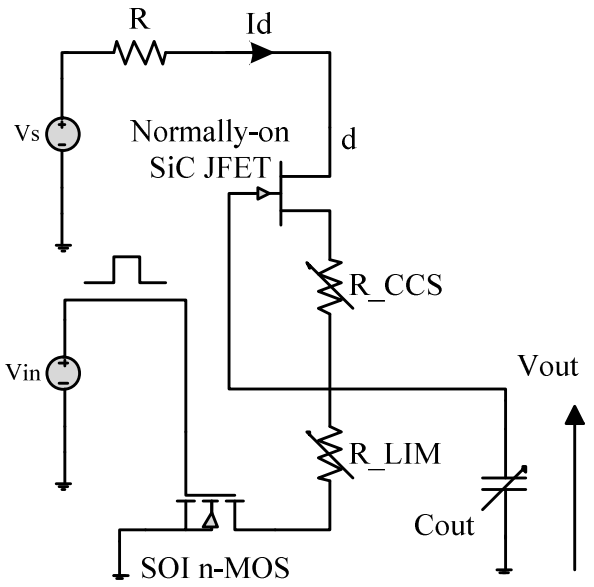


Figure 4.11: The adjustable triangle waveform generator

$$I_{Cout} = Cout\frac{dVout}{dt} \ [A] \tag{4.4}$$

Assuming an output capacitor of 270pF and a desired ramp of 0.5V/µs, a 135µA charging current through the output capacitor is required.

For the n-JFET we have

$$V_{gs} = -I_d \times R\_CCS \ [V] \tag{4.5}$$

Therefore substituting onto the equation 4.2 and solve for R_CCS we have:

$$R\_CCS = \frac{V_p}{I_d}\left(\sqrt{\frac{I_d}{I_{dss}}} - 1\right) \ [\Omega] \tag{4.6}$$

Solving for R_CCS with a pinch-off voltage of -3V and a saturation current of 0.5mA for the SiC JFET, an R_CCS of 10.6kΩ is calculated.

The n-MOS resets the output capacitor through R_LIM. The output capacitance of the selected n-MOS should have a very low capacitance in order not to add extra capacitance to the effective Cout. To rapidly discharge the output capacitor to produce a ramp generator, a minimum R_LIM needs to be selected considering the safe operating area (SOA) of the n-MOS device at maximum drain current. In the design, R_LIM is selected to produce a triangular waveform generator. The default design parameters used for the circuit simulation are shown in table 4.1.

Circuit Parameter	Value	Circuit Parameter	Value
Input Voltage Vs	10V	Vin Peak-Peak Voltage	$5V_{pp}$
Output Capacitor C_{out}	270 pF	Vin Switching Frequency	200 kHz
Drain Resistor R	10kΩ	Vin Duty Cycle	50%
R_CCS	5kΩ	R_LIM	10kΩ

Table 4.1: Default design parameters used for the circuit operation evaluation

Figure 4.12 (a) shows the voltage across the output capacitor for different R_CCS values ranging from 1kΩ to 10kΩ. Changing the bias resistor in the source of the JFET adjusts the load line associated with the gate-source voltage, hence changing the bias point of the constant-current source. A Vs of 10V supplies the JFET through R and the n-MOS switches at 200 kHz switching frequency with a 50% duty cycle, to reset the voltage across the output capacitor. A 10kΩ R_LIM set resistor is selected to control the discharge envelope in a linear manner. Varying R_CCS changes the bias point for the constant current source that results in a change in the rate of voltage rise on the output waveform. When reducing R_CCS from 10kΩ to 1kΩ, the offset voltage of the triangular waveform generated across the output capacitor also increases from 0.8V to 2.2V, this is because at the switching frequency of 200 kHz, the voltage across the capacitor does not fully discharge, and this is the case for switching frequencies in the hundreds of kHz range which is the most suitable frequency range for the DC-DC converter operation.

The effect of varying R_CCS on the operation of the waveform generator circuit is shown in figure 4.12 (b). When the output capacitor is charging, the current through the capacitor increases and eventually settles at the constant-current-source level that determines the rate of voltage rise across the capacitor. During this state, the current through the n-MOS is decreasing exponentially through R_LIM as shown in figure 4.12 (c). When the n-MOS turns on, the voltage across the capacitor discharges and the current in the capacitor reverses and flows through R_LIM to ground. At the point when the n-MOS turns on, there is a current spike in the current waveform of the output capacitor; due to the rapid voltage change across the device.

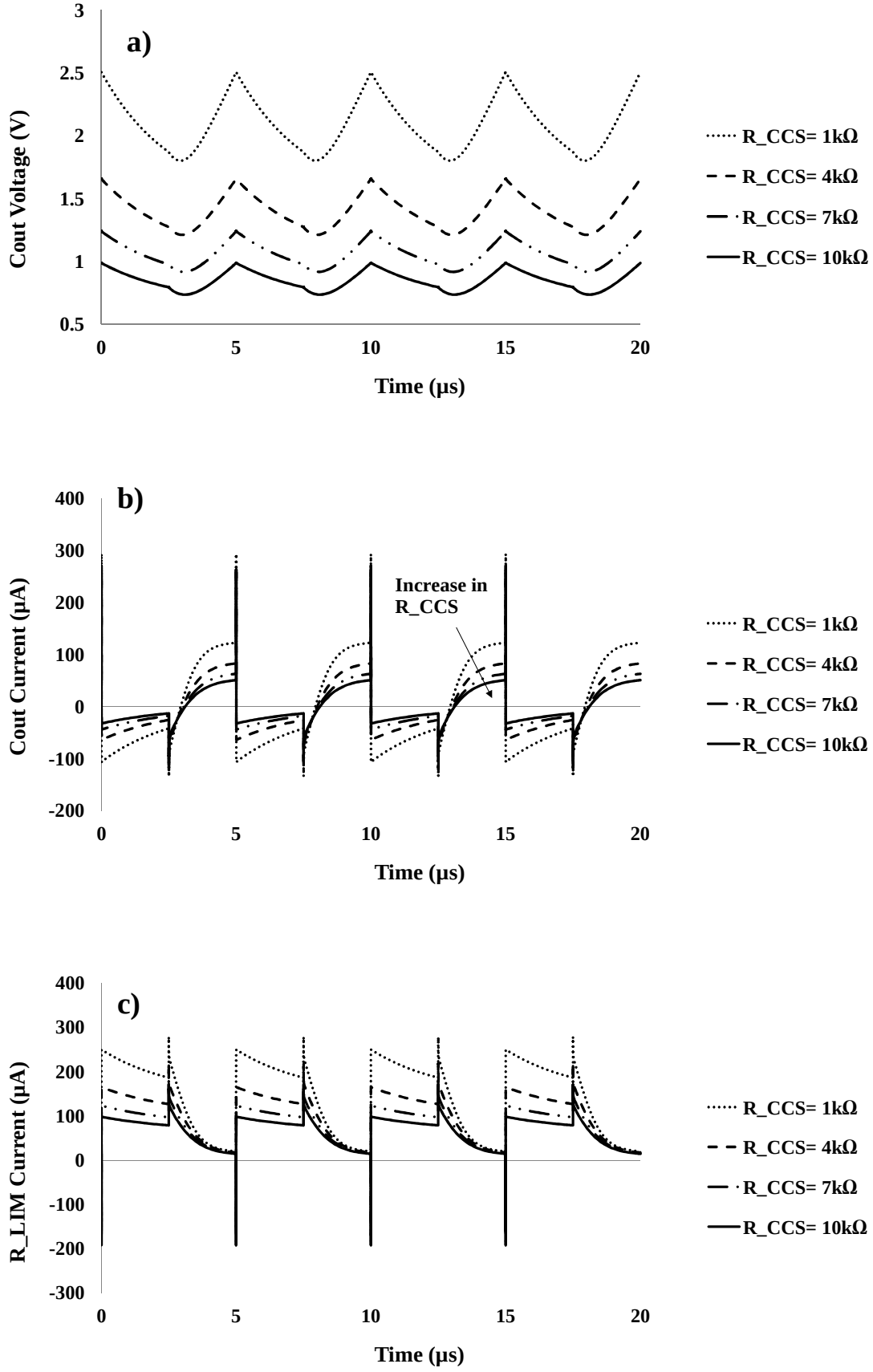
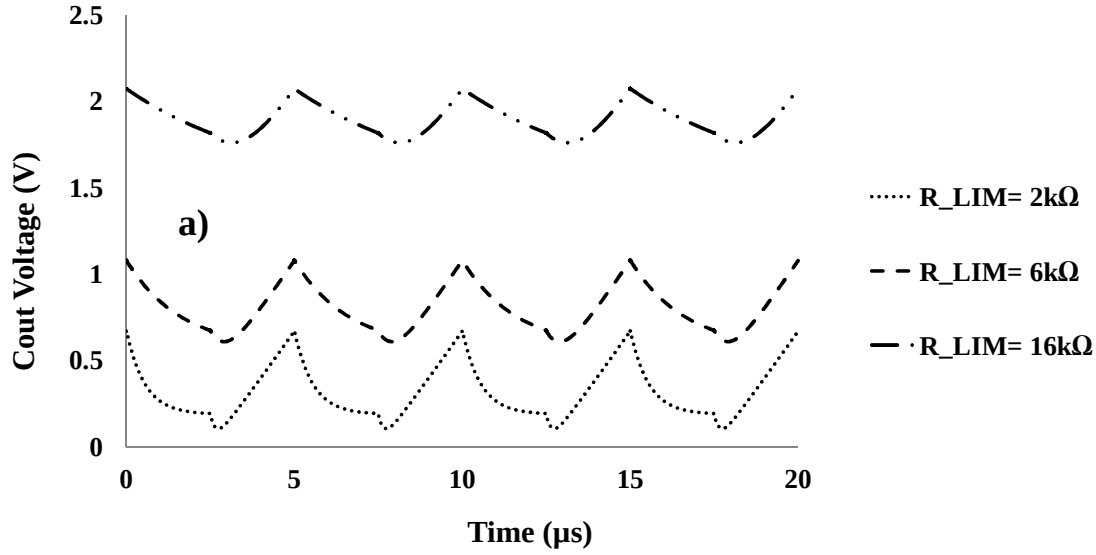


Figure 4.12: The effect of varying R_CCS on the circuit operation

The effect of varying R_LIM on the waveform generator is shown in figure 4.13 (a). A 5kΩ R_CCS bias resistor in the source of the JFET was selected to set the bias point of the constant-current source.

The value of R_LIM affects the discharge phase of the output capacitor. Here, the minimum value for R_LIM is desired that results in a linear discharge phase. As can be seen in figure 4.13 (a), with a 2kΩ R_LIM resistor the discharge phase is a faster discharge of the output voltage across the 270 pF capacitor. As the resistor increases the discharge phase slows down until it becomes a linear phase. The change of R_LIM reset resistor results in an offset change of the voltage across the output capacitor. When increasing R_LIM from 2kΩ to 6kΩ and 16kΩ, the DC offset of the output voltage waveform increases from 0.3V to 0.8V and 1.85V, respectively. As can be seen in figure 4.13 (b), the maximum acceptable current spike though the n-MOS during the phase-change is another factor to consider when selecting the R_LIM value.

When the FET turns on, the voltage across the capacitor discharges and the current in the capacitor reverses and flows through R_LIM to ground. With a 2kΩ R_LIM, current overshoots are the highest during switching transitions, due to the reduced time-constant during the discharge phase. With a 16kΩ R_LIM, current overshoots are the lowest during switching transitions, and the output voltage linearly discharges as well.



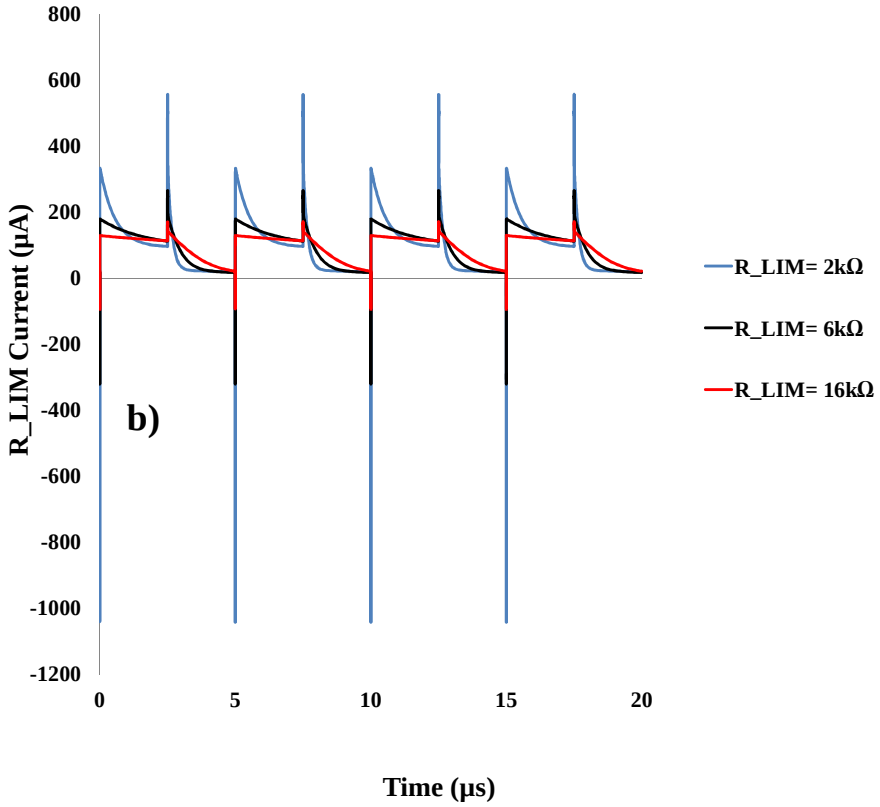


Figure 4.13: The effect of varying R_LIM on the circuit operation

The effect of varying the source voltage on the waveform generator at different R_CCS values is shown in figure 4.14. As can be seen from the data, when the source voltage is varied from 8V to 12V, the change in output capacitor voltage is insignificant due to the use of the JFET current source, unlike R_CCS that has a more significant impact on the capacitor voltage.

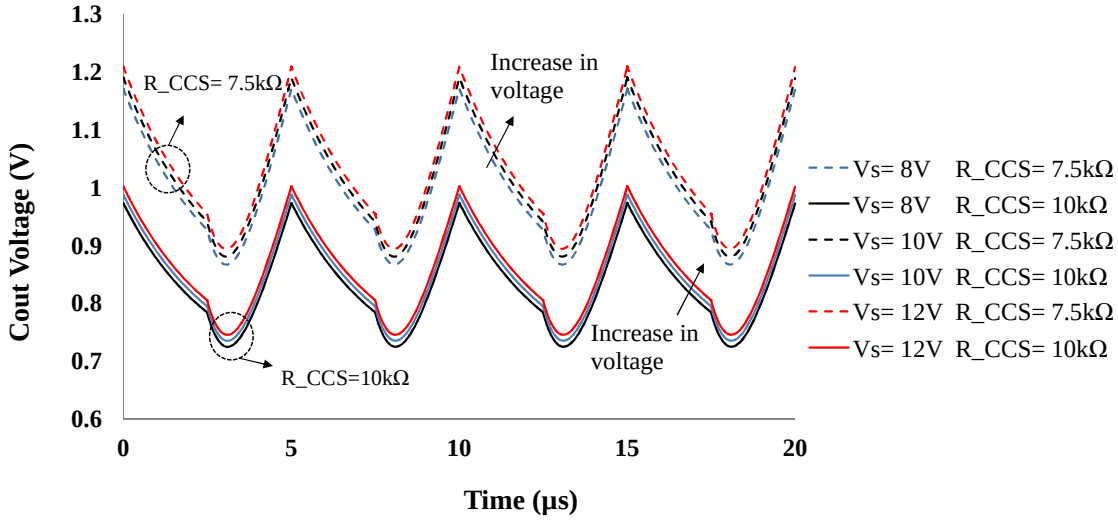


Figure 4.14: The effect of varying source voltage on the circuit operation

4.3 The Circuit Functional Blocks

The proposed circuit is composed of six functional blocks: SiC-based ring oscillator, SOI-based amplification and voltage shaping stage, SiC-based clamp, SiC-based current source, SOI-based control and a push pull buffer. Two normally-off high-temperature SNMOS80 SOI-MOSFETs from CISSOID are used in the amplification and control stages, because of their high gain. These will be replaced by future high current SiC-JFETs with only minor modification to the clamp-stage circuit design. Figure 4.15 shows the block diagram of the proposed PWM generator circuit, including the SiC current source and ring oscillator stages.

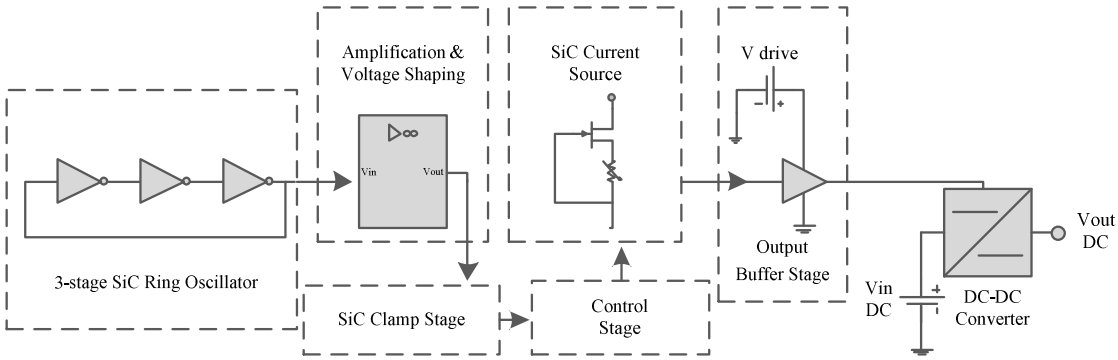


Figure 4.15: Schematic of the proposed gate driver comprising of six functional blocks to form a SiC/SOI based PWM generator based on a current source technique

As shown in figure 4.16, to drive Vg3, the gate voltage of the reset MOSFET, a SiC based pulse generator based on SiC JFETs and SiC diode was designed. The simulation results of the circuit are shown in figure 4.17. The oscillation frequency of the SiC JFET based oscillator was tuned to 100 kHz when loaded. The ring oscillator frequency drops slightly when loaded by the rest of circuit including the amplification stage; due to the increased effective capacitance seen by each inverting stage. V_{tri} was then fed to a high gain amplifier with a 1.6V reference, representing the threshold voltage of a buffer stage. It means that instead of comparing a ramp signal with a variable DC voltage reference, the circuit uses a variable-offset triangular waveform that is compared with a fixed DC voltage which is the threshold-voltage of the buffer stage. This design enables us to directly drive the high temperature buffer proposed in [29] where the SOI Schmitt trigger buffer with hysteresis, functions across the

temperature range of -60 ºC to 250 ºC. Therefore the SiC/SOI signal generator proposed here can be used as an input to the recently proposed high-temperature buffer stage to realise a complete SiC/SOI gate driver unit to power SiC based power devices in high-temperature environments.

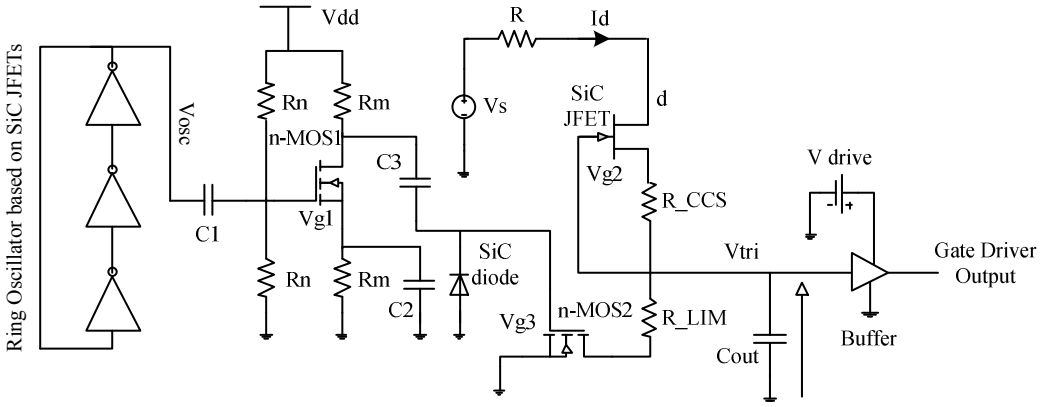
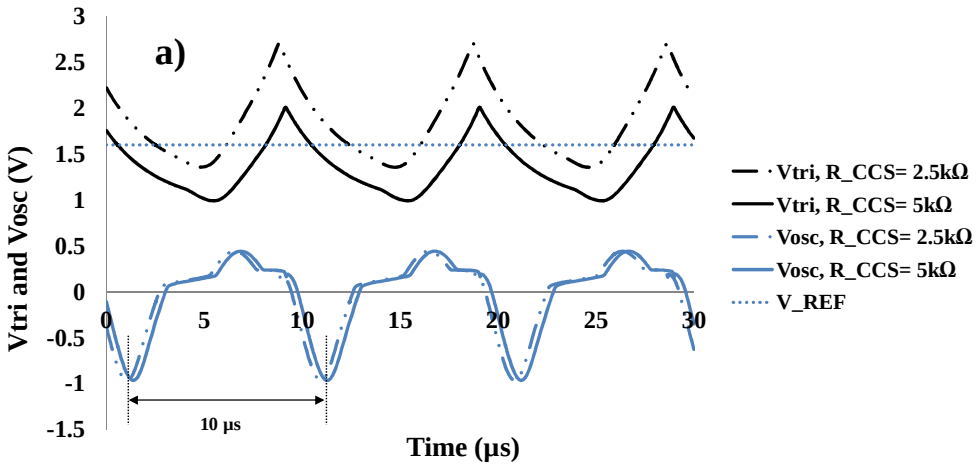


Figure 4.16: The circuit diagram of the SiC/n-MOS based PWM waveform generator

Figure 4.17 (a) shows the 3-stage ring oscillator output waveforms and the triangular waveforms across the output capacitor at 2.5kΩ and 5kΩ R_CCS values. The constant current source resistor, R_CCS, sets the current source level. A 10kΩ R_LIM value and a 10V Vs supply were used for the circuit simulation. The limit resistor, R_LIM, adjusts the output voltage waveform during the discharge phase. Figure 4.17 (b) shows the gate voltage of the bottom FET, Vg3, and the output waveforms of the amplifier demonstrating a symmetric duty cycle change corresponding to the current-source, current-bias change.



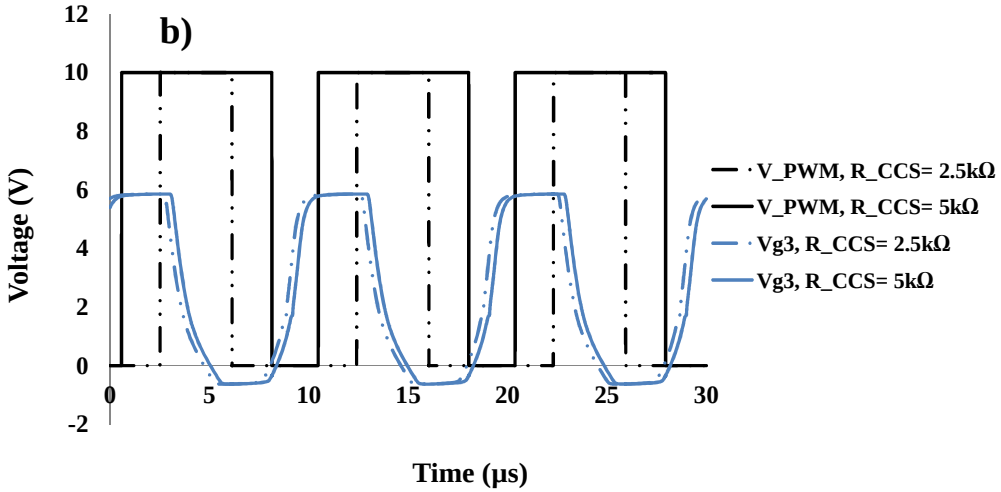


Figure 4.17: The circuit waveforms for two R_CCS values resulting in a symmetric duty cycle change

4.3.1 Feasibility of An All SiC Signal Generator

The circuit proposed in figure 4.16 can be modified so that it only uses the SiC JFETs as shown in figure 4.18. Figure 4.19 (a) shows the 100 kHz 3-stage ring oscillator output waveforms and the triangular waveforms across the output capacitor at 15kΩ and 17.5kΩ R_CCS values. A 10kΩ R_LIM value and a 10V Vs supply were used for the circuit simulation. Figure 4.19 (b) shows the gate voltage of the bottom JFET, Vg3, and the output waveforms of the JFET-based amplifier demonstrating a symmetric duty cycle change corresponding to the current-source, current-bias change.

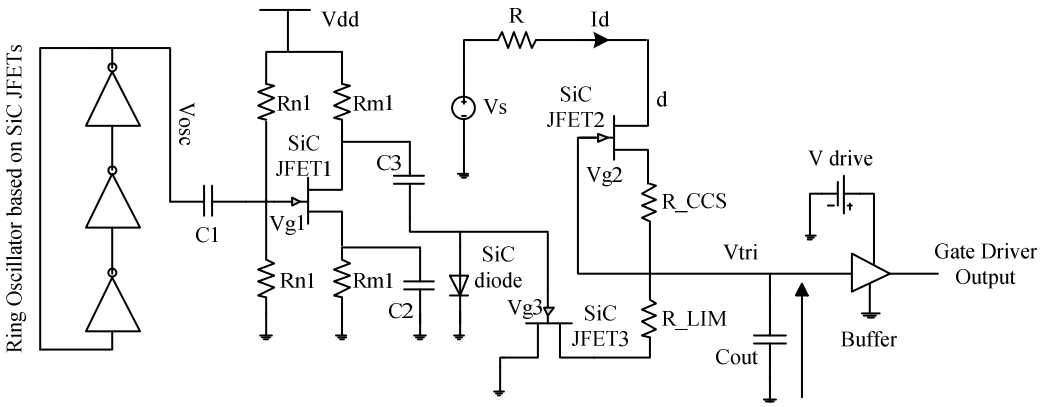


Figure 4.18: The circuit diagram of the all-SiC based PWM waveform generator

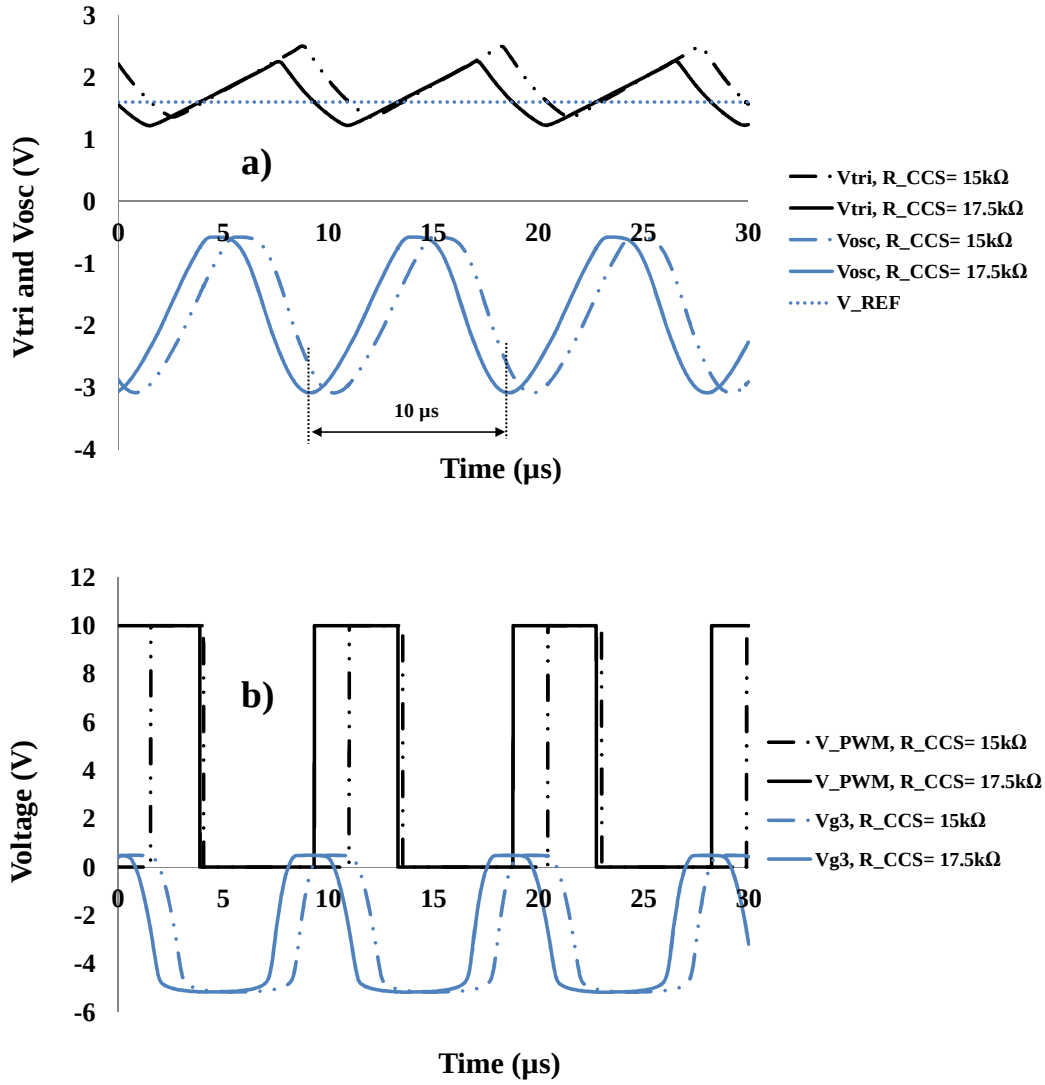


Figure 4.19: The circuit waveforms at two R_CCS values resulting in a symmetric duty cycle change. The Ring oscillator and triangular waveform generator (a), gate control signal and PWM output signal (b)

V_{tri} was fed to a high gain amplifier with a 1.6V reference, representing the threshold voltage of a buffer stage. R_CCS was readjusted to result in a similar duty cycle increase for the same reference voltage, representing the threshold voltage of the buffer stage that is shown in section 4.3. The amplification stage was redesigned for the SiC JFET1 by adjusting the value of resistors Rn1 and Rm1. The gate voltage requirement of the control switch, JFET3 in this case, was satisfied by reversing the SiC diode polarity in the clamp stage. The phase-shift between the circuit waveforms are due to the ring oscillator inverting stages acting as phase-shift amplifiers. This will be affected by the input impedance seen from the input of the amplification stage, as well as the drain-gate capacitance between the oscillator inverting-stages. Due to the periodic

nature of the waveforms, this does not affect the way the circuit operates. Although if this capacitance is changed from 1nF to 100pf, the phase shift between the ring oscillator waveforms will be negligible. In the experimental realisation of the circuit, SOI MOSFETs were used for the amplifier and the control stages, due to the high-level of parasitics and low transconductance of the SiC JFETs used in the circuit.

4.4 Experimental Results

Figure 4.20 shows the prototype of the SiC/SOI-based PWM generator based on a SiC ring oscillator, SiC current source and SOI control and amplification stages. The AlN packages used to bond the SiC JFETs, and a microphotograph of the SiC chips are shown in figure 4.21 (a). The first stage of the circuit is a ring oscillator utilising 3 depletion mode SiC-JFETs bonded on the AlN ceramic DIL package and is shown in the figure 4.21 (b). Figure 4.21 (c) shows a PCB including the other JFETs bonded in a SOIC AlN ceramic package, used in the current source stage. Two SiC test-chips are used in the two stages. The JFETs highlighted in black circles were bonded onto the DIL package and the JFETs highlighted in red circles were bonded onto the SOIC package.

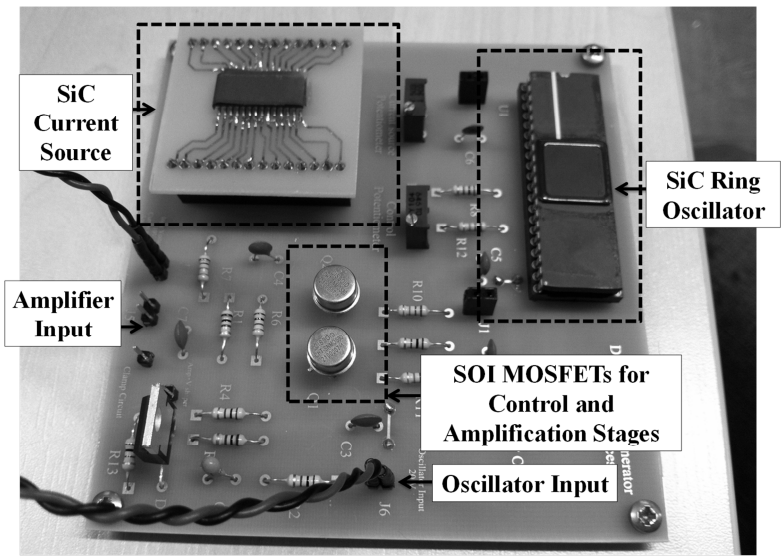


Figure 4.20: Prototype of the SiC/SOI-based PWM generator based on a SiC ring oscillator, SiC current source and SOI control and amplification stages

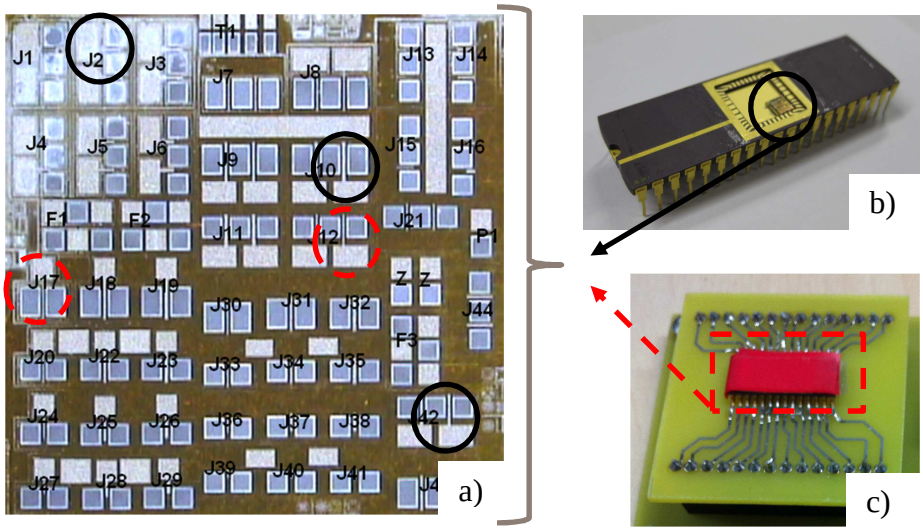


Figure 4.21: Microphotograph of the SiC test-chip (a), SiC current source-source stage (b) and the ring oscillator based on SiC JFETs (c)

As shown in figure 4.22, the proposed design uses a tri inverter ring oscillator (TIRO) comprising 3 SiC-JFETs as the main switches of the inverting stages. The centre frequency was tuned to 100 kHz. Frequency tuning is controlled by the time delay in each inverting stage by means of two small ceramic tuning capacitors. The experimental results for the oscillator frequency spectrum and output waveform are shown in figure 4.23.

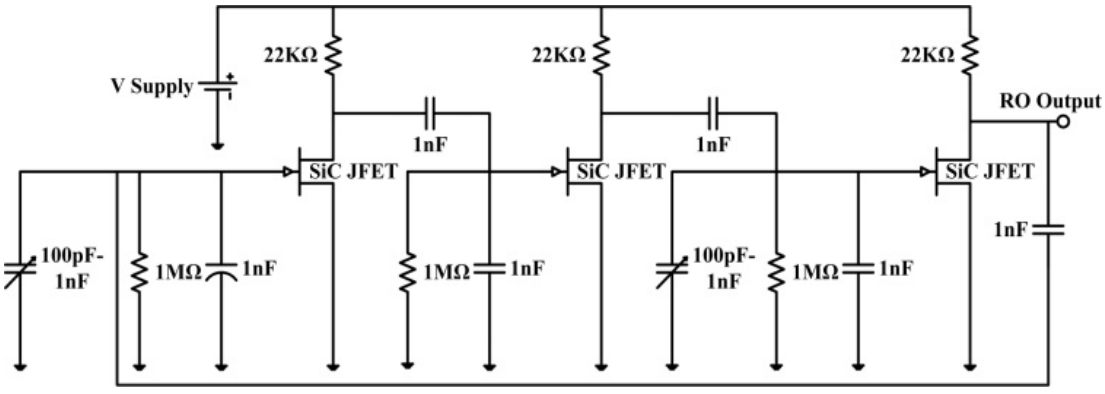


Figure 4.22: Schematic of the 3-stage ring oscillator based on normally-on Low Power SiC JFETs

The amplification/voltage-shaping and control stages use two CHT-Jupiter signal SOI MOSFETs from CISSOID in TO-39 packages. The amplification/voltage shaping stage amplifies the oscillator output voltage and produces a 50% duty cycle pulse to provide the signal to the clamp stage.

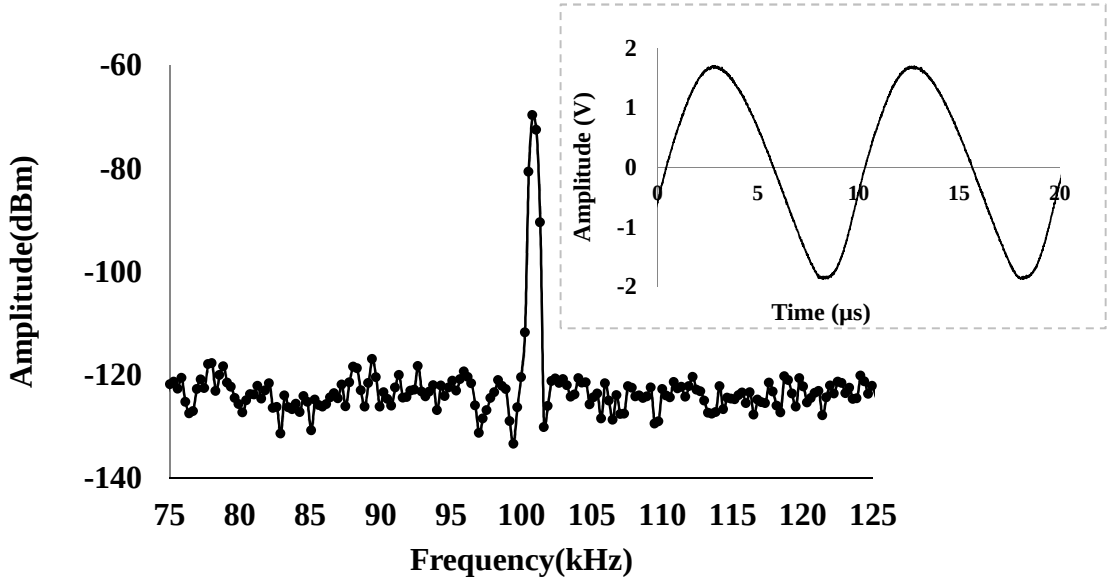


Figure 4.23: Frequency spectrum of SiC JFET based ring oscillator and the 100 kHz ring oscillator output voltage waveform as the figure inset, the RO is unloaded

The clamp stage provides the gate voltage by which an SOI MOSFET switches the voltage across the current source output capacitor in the control stage. The current source stage utilises SiC-JFETs bonded on an AlN ceramic SOIC package. The SiC-based current-source along with the SOI MOSFET control stage are used to produce the adjustable triangular waveform for variable duty cycle PWM generation, as discussed in previous section. The adjustable triangular waveform generator shown in figure 4.24 utilises a SiC JFET, a resistor R1 acting as negative feedback and a capacitor Cout. The SiC JFET is configured as a constant current source charging Cout, as discussed previously.

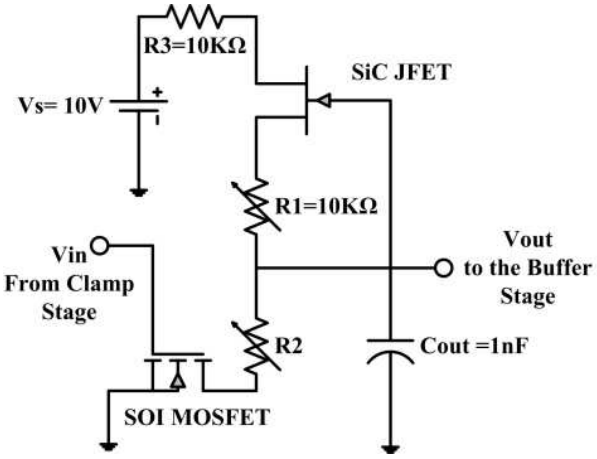


Figure 4.24: SiC current source and the SOI control stages to form the triangular waveform generator for the PWM operation

R1 sets the desired constant current value and acts as a negative feedback to maintain the constant current through the SiC JFET. A voltage ramp is generated across Cout when the SiC constant current source charges Cout =1nF. The SOI MOSFET is turned on with the clamp stage output signal to discharge the capacitor Cout with a time constant of R2Cout and resets the ramp voltage. The R2 value is calculated to utilise the SOI MOSFET in its safe operating area by limiting the discharge current through the device. Figure 4.25 shows the ring oscillator output waveform at 100 kHz, the SOI MOSFET gate voltage and the triangular voltage waveform generated across the output capacitor.

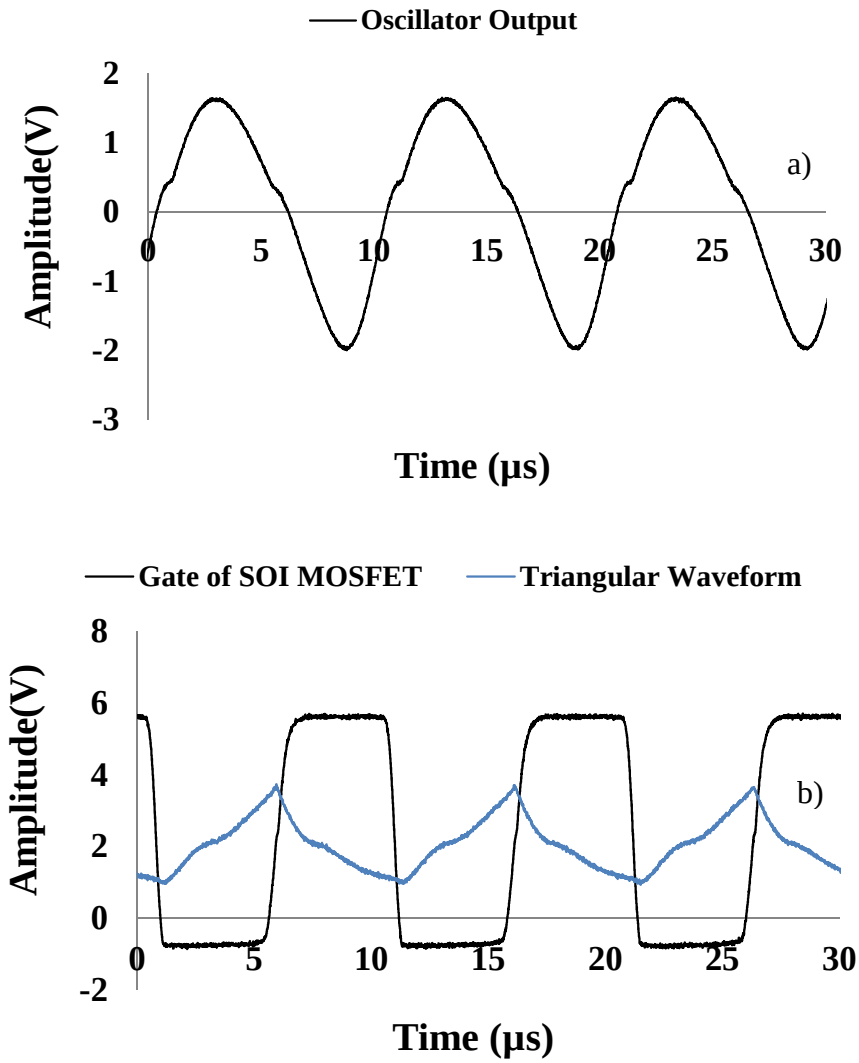


Figure 4.25: The ring oscillator output voltage (a), the SOI MOSFET gate voltage and the voltage across the output capacitor (b) at 100 kHz oscillating frequency

The centre frequency of the ring oscillator was then tuned to 200 kHz to take advantage of the dynamic properties of SiC in the corresponding DC-DC converter.

This was achieved using two 100pF ceramic capacitors instead of the variable capacitors shown in figure 4.22. The experimental results for the oscillator frequency spectrum and output waveform are shown in figure 4.26. The ring oscillator frequency and input current variations as a function of supply voltage for the oscillator are shown in figure 4.27. The ring oscillator shows a frequency stability of ±1% with variations in the supply voltage of ±10%.

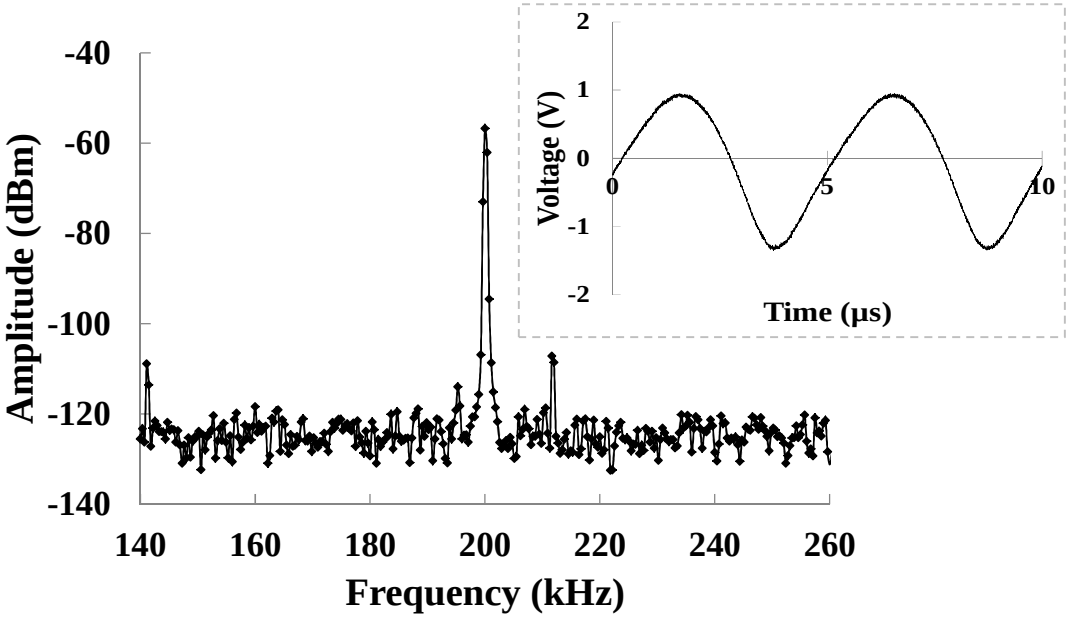


Figure 4.26: Frequency spectrum of SiC JFET based 3-stage ring oscillator and the 200 kHz ring oscillator output voltage waveform as the figure inset, the RO is unloaded

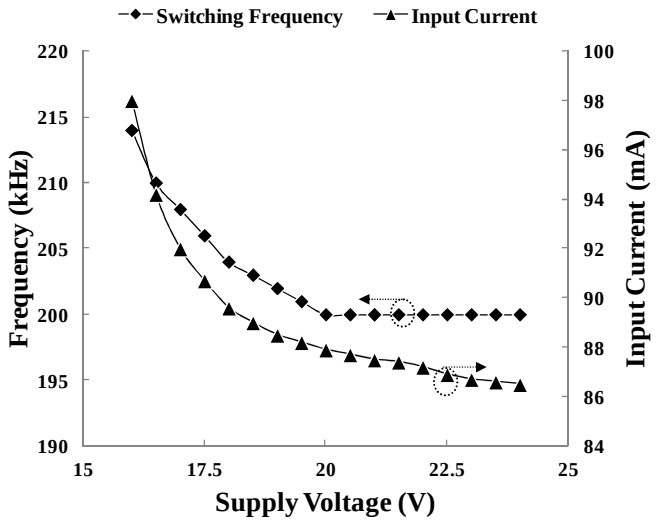
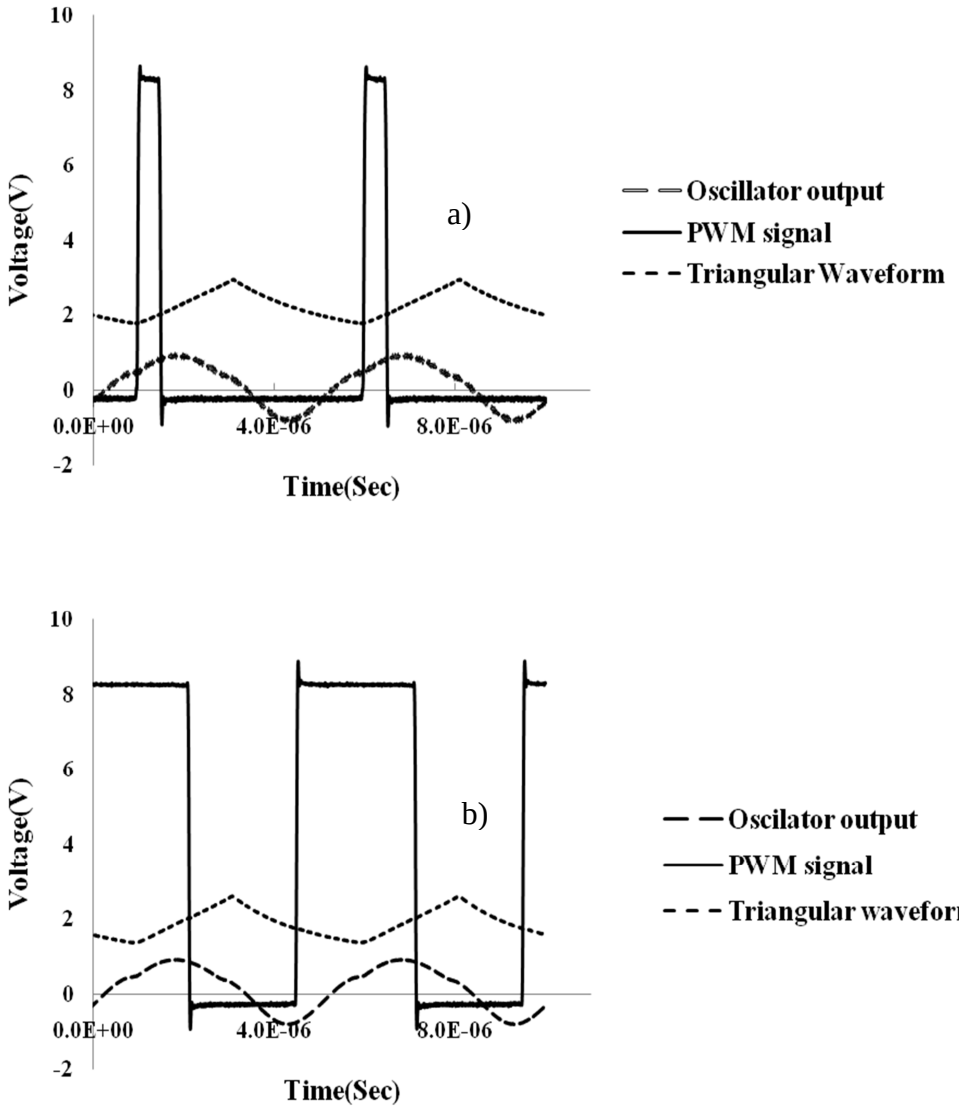


Figure 4.27: Frequency/current variation as a function of supply voltage variation

The output of the SiC-based current source is then buffered with a complementary symmetrical push-pull stage to produce the variable duty cycle pulse width modulation as shown in figure 4.28. The buffer stage is required to isolate the pulse generator from any output load variation. The buffer stage also provides the required voltage and current for the subsequent power converter circuit. In the proposed design, the duty cycle can be varied from 10% to 90% by varying the DC offset of the voltage across the current source output capacitor; this was achieved by adjusting the R_CCS resistor to set the current source level. Changing the bias resistor in the source of the JFET adjusted the load line associated with the gate-source voltage, hence changing the bias point of the constant-current source to achieve the desired PWM duty cycle. This may be realised by the use of 200µm gate-width SiC JFETs with an R_{ds}(on) of up to 10 kΩ during on-state. Figure 4.29 shows the R_{ds}(on) of the SiC JFETs with gate lengths of 9µm,15µm and 21µm.



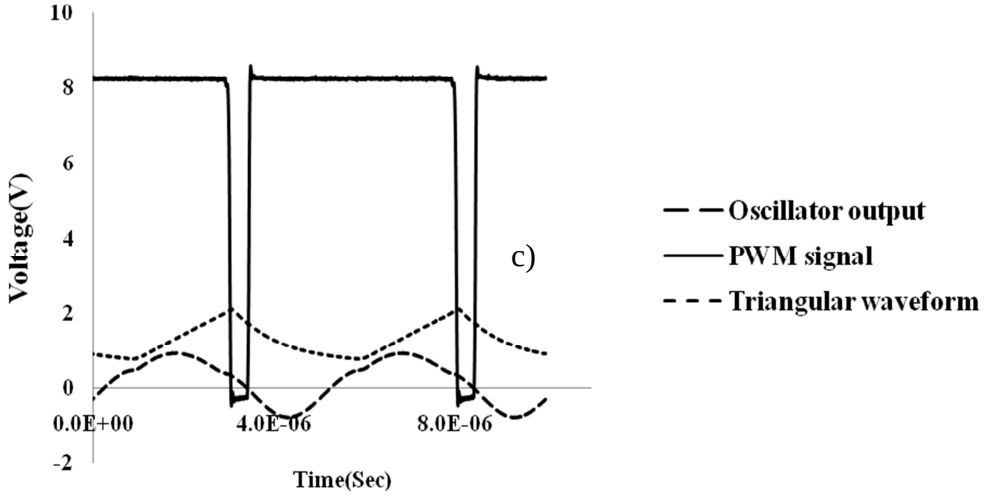


Figure 4.28: Experimental results for the proposed PWM generator for 10% (a), 50% (b) and 90% (c) duty cycles at an 8V buffer bus voltage

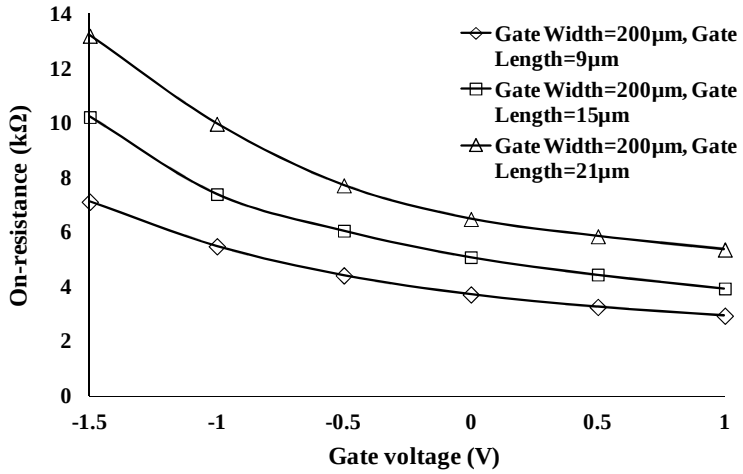


Figure 4.29: SiC JFET on-resistance Vs. gate voltage for different gate lengths of 9µm, 15µm and 21µm

To evaluate the performance of the proposed PWM generator, a 200 kHz SiC-based step-up DC-DC converter utilising a 2A CREE SiC Schottky diode has been realised. The design criteria of the converter are based on the requirement for steady-state operation of the semiconductor devices at the desired switching frequency. The converter is operated at an input DC voltage of 5V and an output voltage of 24V. The output capacitor is selected as a 5µF capacitor so that the output voltage ripples are limited to 2% under full load conditions. A 150µH inductor is used to ensure continuous

conduction mode operation (CCM) and to limit the inductor current ripple to 20%.The schematic of the converter module is shown in figure 4.30. The voltage and current waveforms of the converter are shown in figure 4.31; the efficiency of the converter is measured to be 91% at 81% duty cycle. All of the active components used in the PWM generator circuit have the ability to operate at elevated temperatures for prolonged periods of time. After suitable packaging advancement, it is anticipated that a similar circuit will be designed and constructed to operate at higher temperatures to demonstrate the extreme versatility of these devices.

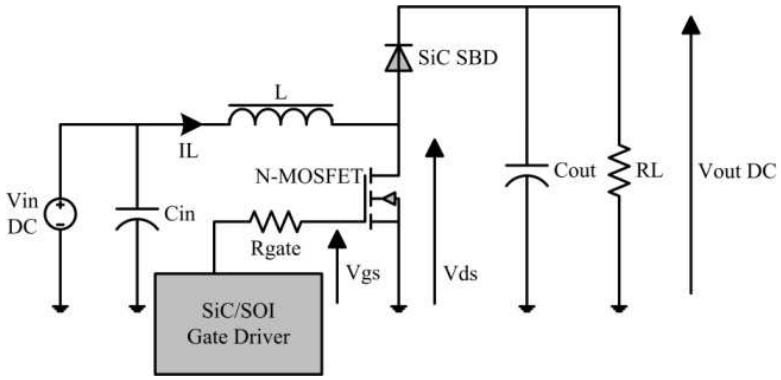


Figure 4.30: Schematic of the step-up converter used for the PWM generator performance evaluation

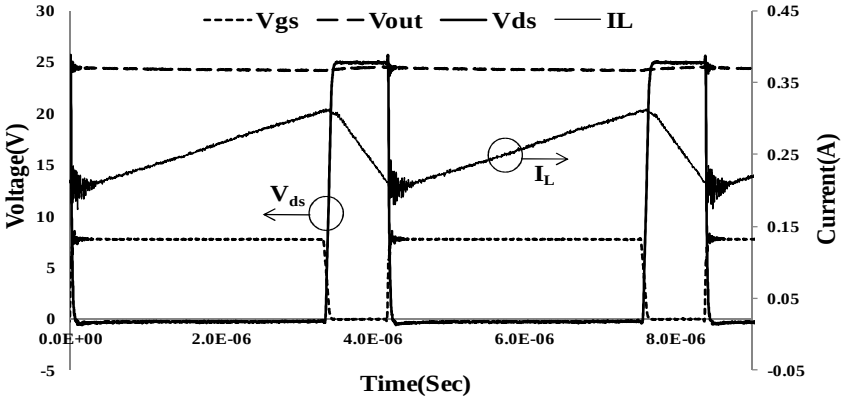


Figure 4.31: Step-up converter drain-source voltage, gate-source voltage and the inductor current waveforms at 81% duty cycle

4.5 Conclusions

A SiC/SOI-based PWM generator based on a SiC current source, a ring oscillator, an amplification/clamp stage, control stage and output buffer stage has been proposed and realised. The ring oscillator enables a wide range of frequency tuning suitable for the operation of SiC-based DC-DC converters. A SiC based constant current source was used as part of the triangular waveform generating stage with adjustable offset. Both the current source bias-resistor as well as the SOI MOSFET current limiting resistor can be used to adjust the dc offset of the generated waveform. The simulation results for the circuit utilising SiC JFETs in the ring oscillator and the current source stage and SOI MOSFETs in the amplification and control were detailed. Both the SOI MOSFETs can be replaced with future high-current SiC JFETs with minor modification to the control and amplification stages. The centre frequency has been tuned to 200 kHz to take advantage of the SiC dynamic properties in the corresponding step-up DC-DC converter. The 91% efficient step-up converter operated at 81% duty cycle and 200 kHz switching frequency. The proposed design also enables the duty cycle control from 10% to 90%. As the design only used SiC/SOI switching devices, the gate drive circuitry can be placed close to high power SiC power switching devices in the converter which is in exposure of higher ambient temperatures than a standard silicon-based PWM generator can tolerate.

4.6 References

[1] C. Brunson, et al., "Open-Circuit Fault Detection and Diagnosis in Matrix Converters," Power Electronics, IEEE Transactions on, vol. 30, pp. 2840-2847, 2015.

[2] B. Wrzecionko, et al., "High-Temperature (250 ºC / 500 ºF) 19000 min-1 BLDC Fan for Forced Air-Cooling of Advanced Automotive Power Electronics," Mechatronics, IEEE/ASME Transactions on, vol. 20, pp. 37-49, 2015.

[3] M. Ohadi and Q. Jianwei, "Thermal management of harsh-environment electronics," in Semiconductor Thermal Measurement and Management Symposium, 2004. Twentieth Annual IEEE, 2004, pp. 231-240.

[4] R. Khazaka, et al., "Survey of High-Temperature Reliability of Power Electronics Packaging Components," Power Electronics, IEEE Transactions on, vol. 30, pp. 2456-2464, 2015.

[5] J. J. den Boer, "The use of high temperature electronics in downhole applications," in High Temperature Electronics, 1999. HITEN 99. The Third European Conference on, 1999, pp. 149-152.

[6] S. Zhenzhen, et al., "SiC Power Device Die Attach for Extreme Environments," Electron Devices, IEEE Transactions on, vol. 62, pp. 346-353, 2015.

[7] K. Rajashekara, "Present Status and Future Trends in Electric Vehicle Propulsion Technologies," Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol. 1, pp. 3-10, 2013.

[8] N. Puqi, et al., "High-Temperature Hardware: Development of a 10-kW High-Temperature, High-Power-Density Three-Phase ac-dc-ac SiC Converter," Industrial Electronics Magazine, IEEE, vol. 7, pp. 6-17, 2013.

[9] X. Zhuxian, et al., "Investigation of Si IGBT Operation at 200 ºC for Traction Applications," Power Electronics, IEEE Transactions on, vol. 28, pp. 2604-2615, 2013.

[10] W. Zhiqiang, et al., "A High Temperature Silicon Carbide mosfet Power Module With Integrated Silicon-On-Insulator-Based Gate Drive," Power Electronics, IEEE Transactions on, vol. 30, pp. 1432-1445, 2015.

[11] M. A. Huque, et al., "Silicon-on-insulator-based high-voltage, high-temperature integrated circuit gate driver for silicon carbide-based power field effect transistors," Power Electronics, IET, vol. 3, pp. 1001-1009, 2010.

[12] W. Ruxi, et al., "A High-Temperature SiC Three-Phase AC - DC Converter Design for ›100/spl deg/C Ambient Temperature," Power Electronics, IEEE Transactions on, vol. 28, pp. 555-572, 2013.

[13] E. Cilio, et al., "Design and Fabrication of a High Temperature (250 Â°C Baseplate), High Power Density Silicon Carbide (SiC) Multichip Power Module (MCPM) Inverter," in IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on, 2006, pp. 1822-1827.

[14] P.G. Neudeck, et al., " Characterization of 6H-SiC JFET Integrated Circuits Over A Broad Temperature Range from -150 °C to +500 °C," Materials Science Forum, pp. 645- 648, 2010.

[15] R. Ghandi, et al., "Silicon Carbide Integrated Circuits With Stable Operation Over a Wide Temperature Range," Electron Device Letters, IEEE, vol. 35, pp. 1206-1208, 2014.

[16] P. G. Neudeck, et al., "Stable Electrical Operation of 6H-SiC JFETs and ICs for Thousands of Hours at 500 ºC," Electron Device Letters, IEEE, vol. 29, pp. 456-459, 2008.

[17] S. L. Garverick, et al., "SiC JFET integrated circuits for sensing and control at temperatures up to 600 ºC," in Energytech, 2012 IEEE, 2012, pp. 1-6.

[18] S. Singh and J. A. Cooper, "Bipolar Integrated Circuits in 4H-SiC," Electron Devices, IEEE Transactions on, vol. 58, pp. 1084-1090, 2011.

[19] J. Valle-Mayorga, et al., "High-Temperature Silicon-on-Insulator Gate Driver for SiC-FET Power Modules," Power Electronics, IEEE Transactions on, vol. 27, pp. 4417-4424, 2012.

[20] H. Kosai, et al., "Design and Performance Evaluation of a 200 ºC Interleaved Boost Converter," Power Electronics, IEEE Transactions on, vol. 28, pp. 1691-1699, 2013.

[21] S. Waffler, et al., "High temperature (200°C) isolated gate drive topologies for Silicon Carbide (SiC) JFET," in Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE, 2008, pp. 2867-2872.

[22] V. Bondarenko, et al., "SiC devices for converter and motor drive applications at extreme temperatures," in Aerospace Conference, 2006 IEEE, 2006, p. 6 pp.

[23] C. Zheng, et al., "A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications," Power Electronics, IEEE Transactions on, vol. 29, pp. 2307-2320, 2014.

[24] R. Wang, et al., "A Novel Hybrid Packaging Structure for High-Temperature SiC Power Modules," Industry Applications, IEEE Transactions on, vol. 49, pp. 1609-1618, 2013.

[25] S. Tanimoto and K. Matsui, "High Junction Temperature and Low Parasitic Inductance Power Module Technology for Compact Power Conversion Systems," Electron Devices, IEEE Transactions on, vol. 62, pp. 258-269, 2015.

[26] S. Kuang, "Maximum Junction Temperatures of SiC Power Devices," Electron Devices, IEEE Transactions on, vol. 56, pp. 337-342, 2009.

[27] N. Puqi, et al., "A Novel High-Temperature Planar Package for SiC Multichip Phase-Leg Power Module," Power Electronics, IEEE Transactions on, vol. 25, pp. 2059-2067, 2010.

[28] N. Ericson, et al., "A 4H Silicon Carbide Gate Buffer for Integrated Power Systems," Power Electronics, IEEE Transactions on, vol. 29, pp. 539-542, 2014.

[29] M. A. Huque, et al., "A 200 ºC Universal Gate Driver Integrated Circuit for Extreme Environment Applications," Power Electronics, IEEE Transactions on, vol. 27, pp. 4153-4162, 2012.

[30] J. M. Hornberger, et al., "A High-Temperature Multichip Power Module (MCPM) Inverter utilizing Silicon Carbide (SiC) and Silicon on Insulator (SOI) Electronics," in Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE, 2006, pp. 1-7.

[31] J. Hornberger, et al., "High-temperature integration of silicon carbide (SiC) and silicon-on-insulator (SOI) electronics in multichip power modules (MCPMs)," in Power Electronics and Applications, 2005 European Conference on, 2005, pp. 10 pp.-P.10.

[32] B . A. Chen, et al., "0.25 µm low power CMOS devices and circuits from 8 inch SOI materials," in Solid-State and Integrated Circuit Technology, 1995 4th International Conference on, 1995, pp. 260-262.

[33] CREE Silicon Carbide Substrates and Epitaxy. Available: http://www.cree.com/LED-Chips-and-Materials/Materials/.

[34] K.V. Vassilevski, et al., "Protection of selectively implanted and patterned silicon carbide surfaces with graphite capping layer during post-implantation annealing," Journal of Semiconductor Science and Technology, vol. 20, pp. 271-278, 2005.

[35] A. Hajimiri, et al., "Jitter and phase noise in ring oscillators," Solid-State Circuits, IEEE Journal of, vol. 34, pp. 790-804, 1999.

[36] P. M. Farahabadi, et al., "Closed-Form Analytical Equations for Amplitude and Frequency of High-Frequency CMOS Ring Oscillators," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 56, pp. 2669-2677, 2009.

[37] N. Retdian, et al., "Voltage controlled ring oscillator with wide tuning range and fast voltage swing," in ASIC, 2002. Proceedings. 2002 IEEE Asia-Pacific Conference on, 2002, pp. 201-204.

[38] O. T. C. Chen and R. R. B. Sheen, "A power-efficient wide-range phase-locked loop," Solid-State Circuits, IEEE Journal of, vol. 37, pp. 51-62, 2002.

[39] S. K. Enam and A. A. Abidi, "A 300-MHz CMOS voltage-controlled ring oscillator," Solid-State Circuits, IEEE Journal of, vol. 25, pp. 312-315, 1990.

Chapter 5. High Temperature Self-oscillatory DC-DC Converter

5.1 Introduction

In recent years there has been increasing demand to investigate and monitor ever more hostile environments including those containing high temperatures and/or extreme radiation flux [1-3]. Silicon carbide (SiC) boasts a much higher band gap than conventional silicon and is therefore more chemically stable allowing electronic circuits made from this material to be deployed in environments where conventional silicon based electronics cannot function. These high temperature environments are incompatible with standard battery technologies, and so, energy harvesting is a suitable technology when remote monitoring of these extreme environments is performed through the use of wireless sensor nodes (WSNs) [4-6]. There are now a variety of energy harvesting devices available which are capable of producing sufficient energy from the ambient surroundings to intermittently power a WSN [7-9].

Energy harvesting devices often produce voltages which are unusable directly by electronic loads and so require power management circuits to convert the electrical output to a level which is usable by monitoring electronics and sensors. Therefore a DC-DC step-up converter that can handle low input voltages is required [10, 11]. The required gate-drive circuitry for these converters need to be placed next to the switches to minimise system complexity, however, the successful operation of the gate drivers, especially with no heatsink in hostile environments will increase the power density for DC-DC converter modules. The advantages of SiC based power devices in terms of high current densities, faster switching speeds and high temperature capabilities have already been discussed in chapter 2. To fully utilise the benefits of SiC devices in DC-DC converters used in harsh environments, the gate drive design requires special attention. To match the high temperature capabilities of SiC devices, the gate drivers also need to be capable of operation at these elevated temperatures [12, 13].

SiC based switches such as SiC JFETs are capable of tolerating these elevated temperatures, however, various other components such as passives, magnetics or amplifiers will make this task rather challenging. From a system point of view, the gate drive requirements of normally-on SiC JFETs are a significant challenge. The issue with

the start-up process in addition to the differences in the gate voltage requirements make them less desirable for power designers [14, 15]. However, the specific on-resistance of normally-off (enhancement-mode) JFETs is almost 15% higher than their normally-on counterparts [16]. Therefore in a circuit where on-state losses are expected to be the dominant power losses, the normally-on (depletion-mode) JFETs are better alternatives. Another disadvantage of normally-off SiC JFETs is that in order to keep the device in the on-state, the gate-source junction must be forward biased [17]. This implies that similar to SiC based BJTs, there is a considerable drive current requirement, which undesireable.

5.2 Power Sources for Wireless Sensor Nodes

Wireless sensor networks have become a very popular enabling technology and have already entered the market place in a number of sectors. The majority of these platforms are powered by limited-life batteries. Hence alternative power sources are being continuously investigated and employed [18].

The rapid reduction in the size and power consumption of electronic components has helped speed up the research on communication nodes and wirless sensors. As the size of these WSNs decreases, their use becomes more widespread in the automobile industry, industrial environments and aerospace industry. However, their respective power supply has become a major issue, because the size reduction in CMOS electronics has significantly outpaced the enegy density improvements in batteries which are the most commonly used power sources. Consequently, the power supply, usually a battery, is the limiting factor on both the size and liftime of the sensor node. Energy reservoir power sources such as micro-scale batteries, micro-fuel cells, ultra capacitors are characterised by their energy density and can be used to power WSNs but at the cost of increased size and redued life-time. Power scavenging sources are an alternative power source. Unlike energy reservoirs, power scavenging sources are characterised by their power density; the energy provided from these sources depends on the amount of time each source is in operation [18-21]. One of the popular power scavenging sources is via temperature gradients [22, 23]. Energy can be scavenged from the environment using the temperature variations that naturally occur. The maximum

power-conversion efficiency from a temperature difference, the Carnot efficiency is given below in equation 5.1, where the temperature are in Kelvin:

$$\eta = \frac{(T_{\text{high}} - T_{\text{low}})}{T_{\text{high}}} \tag{5.1}$$

Assuming a room temperature of 27 °C and for a source 5 °C above room temperature, the maximum efficiency is 1.64% and for a source 10 °C above room temperature is maximum efficiency is 3.22%. At low temperature differences and small scales, conduction will dominate and convection and radiation can be neglected. The heat flow through conduction is given by equation 5.2, where L is the length of material that the heat is flowing through and k is the thermal conductivity of the material used:

$$q' = k\frac{(\Delta T)}{L} \tag{5.2}$$

Assuming a length of 1cm and a temperature difference of 10 °C, the heat flow (power) for silicon with a thermal conductivity of 140 W/mK is 14W/cm^2. Assuming that Carnot efficiency could be achieved, the output power would be 451mW/cm^2 which is significantly higher than comparable power sources. In practice, the efficiencies for this type of energy harvester are well below the Carnot efficiency. One of the most common ways to convert the generated power from temperature differences to electricity is by using thermoelectric generators.

5.3 Thermoelectric Generators

Driving a wireless sensor node from ambient is attractive as it eliminates the need for wires or batteries. Despite the clear advantages of energy harvesting, these systems require a suitable power-management strategy to convert the low voltage levels to a level usable by the wireless sensor systems. Many WSNs monitor physical quantities, which change slowly and therefore the measurements can be taken and transmitted less frequently. This means lower operating duty cycle and therefore many wireless sensor systems consume very low average power, hence they are suitable candidates for energy harvesting power sources.

Thermoelectric generators (TEGs) are energy harvesting devices capable of producing large amounts of current at low voltages from a thermal gradient across the device; through a phenomenon known as the Seebeck effect [24]. Modern TEG's are constructed out of p-n junctions of different semiconductor materials depending on their operational requirements, but commonly bismuth telluride (Bi_2Te_3). The mechanical construction of a TEG is shown in figure 5.1.

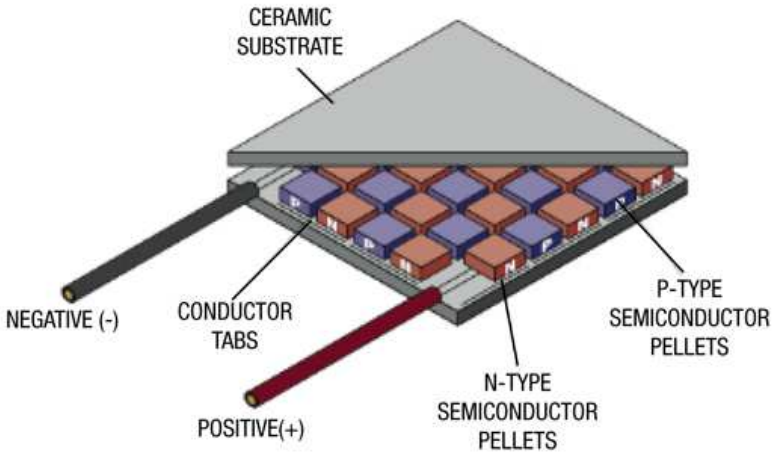


Figure 5.1. Construction of a thermoelectric generator [25]

In this work a standard off-the-shelf TEG manufactured by Marlow (product number TG 12-801L) was characterised in terms of the electrical output as a function of temperature difference between the two surfaces. A ceramic hotplate controlled by a Lakeshore temperature controller was used to provide a controlled temperature heat source whilst a thermocouple embedded into the base of a heat sink and fan provided the cooler side thus creating a measurable temperature difference across the device. The electrical characteristics for the unit used in this study are shown by the experimental data in figure 5.2 for a range of temperature differences. The higher the temperature difference, the greater the output voltage becomes at any given current. Figure 5.3 shows the output power of the thermoelectric generator as a function of the output voltage. The solid line intersects with the waveforms where the maximum output power is at the optimum output voltages. The optimum voltage for the TEG is generally below 1.3V and needs to be boosted in order to supply the drive for remote sensor applications.

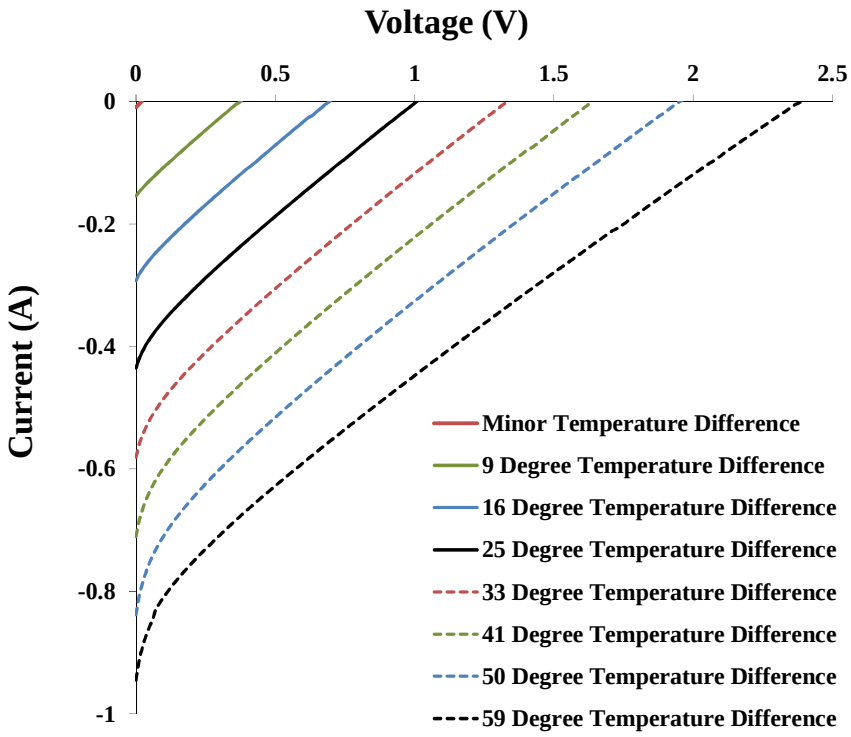


Figure 5.2: Electrical characteristics of the thermoelectric generator for various temperature differences

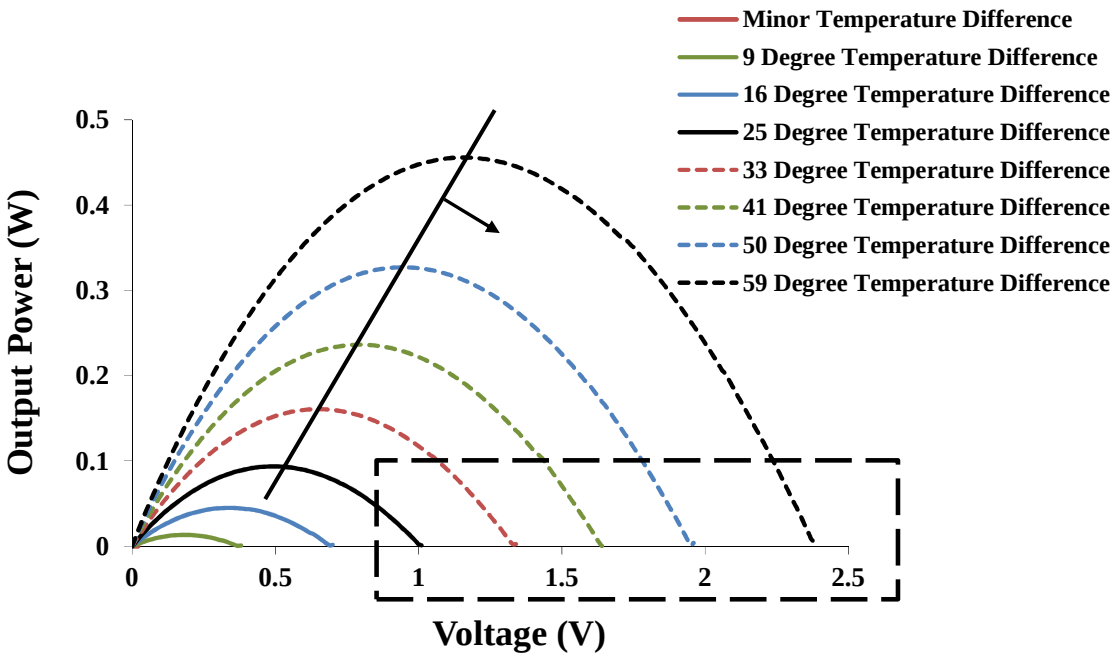


Figure 5.3: Output power as a function of voltage for the thermoelectric generator for various temperature differences

5.4 Need for a DC-DC Converter with a High Voltage Conversion Ratio

As previously discussed, the output voltage of the thermoelectric generator is directly proportional to the temperature difference between its junctions. In practical applications, this low voltage is insufficient to support the drive for remote sensor applications. Therefore a step-up DC-DC converter is usually used to boost the output voltage of the thermoelectric generator to a desired level. Figure 5.4 shows a simplified block diagram of a TEG powered wireless sensor system.

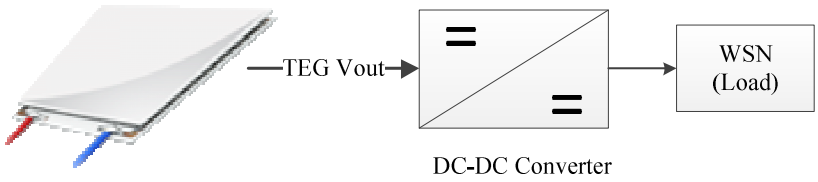


Figure 5.4: Simplified TEG powered wireless sensor system

A conventional boost converter is shown in figure 5.5 (a). The overall power losses including the break-down of the switching losses in the converter were discussed in detail in chapter 3. In [26], the voltage conversion ratio of the boost and N+1 level boost converters as a function of duty cycle and the inductor DCR are presented. Here, the relationship between the voltage conversion ratio and efficiency of the conventional and N+1 level boost converters as a function of duty cycle, inductor DCR, diode forward voltage, input voltage, the MOSFET voltage drop and the load is obtained. A LabVIEW program was written to plot the voltage conversion ratio and efficiency of the conventional and 3-level boost converters as function of duty cycles for various load, line, voltage drops and DC resistances.

As in this application a high voltage conversion ratio and efficiency are key requirements, let us consider the conduction power losses and assume the current and voltage ripples are negligible, for the CCM we can write:

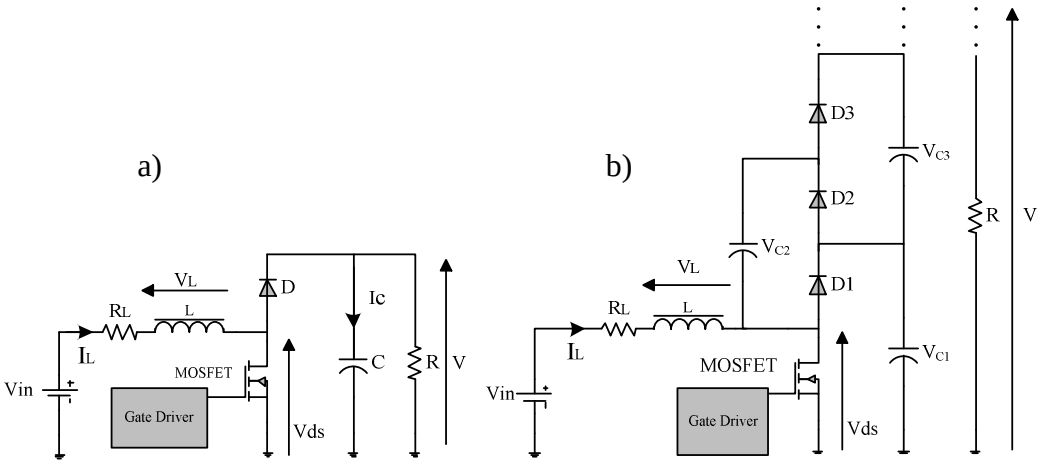


Figure 5.5: Conventional boost converter (a) and N+1 level boost converter (b)

During on-state

$$v_L(t) = V_{in} - R_L i_L(t) - R_{ds} i_L(t) \tag{5.3}$$

$$i_C(t) = -\frac{V_c(t)}{R} \tag{5.4}$$

Where R_{ds} is the on resistance of the FET and R_L is the DC resistance of the inductor

Now applying the small ripple approximation method:

$$v_L(t) = V_{in} - (R_L + R_{ds}) I_L \tag{5.5}$$

$$i_C(t) = -\frac{V}{R} \tag{5.6}$$

During off-state

$$v_L(t) = V_{in} - R_L i_L(t) - V_F - V_c(t) \tag{5.7}$$

$$i_C(t) = i_L(t) - \frac{V_c(t)}{R} \tag{5.8}$$

Where V_F is the voltage drop of the diode.

Now applying the small ripple approximation method:

$$v_L(t) = V_{in} - R_L I_L - V_F - V \tag{5.9}$$

$$i_C(t) = I_L - \frac{\mathrm{V}}{\mathrm{R}} \tag{5.10}$$

When the boost converter operates in steady state, the DC component of the voltage across the inductor and the current in the capacitor is zero:

$$D\,(V_{in} - (R_L + R_{ds})I_L) + (1-D)\,(V_{in} - R_L I_L - V_F - V) = 0 \tag{5.11}$$

$$D\left(-\frac{V}{R}\right) + (1-D)\left(I_L - \frac{V}{R}\right) = 0 \tag{5.12}$$

Solving the above equations results in the following:

$$\mathrm{I_L} = \frac{\mathrm{V}}{\mathrm{R}(1-\mathrm{D})} \tag{5.13}$$

$$\mathrm{V_{in}} + (\mathrm{D}-1)\mathrm{V_F} + (\mathrm{D}-1)\mathrm{V} - (\mathrm{R_L} + \mathrm{DR_{ds}})\mathrm{I_L} = 0 \tag{5.14}$$

Now substituting $\mathrm{I_L}$ into equation 5.14:

$$\mathrm{V_{in}} + \left((\mathrm{D}-1) + \frac{(-\mathrm{DR_{ds}} - \mathrm{R_L})}{\mathrm{R}(1-\mathrm{D})}\right)\mathrm{V} + (\mathrm{D}-1)\mathrm{V_F} = 0 \tag{5.15}$$

$$\mathrm{V}(\mathrm{D}, \mathrm{V_F}, \mathrm{R_{ds}}, \mathrm{R_L}) = \frac{(1-\mathrm{D})\mathrm{V_F} - \mathrm{V_{in}}}{(\mathrm{D}-1) + \frac{(-\mathrm{DR_{ds}} - \mathrm{R_L})}{\mathrm{R}(1-\mathrm{D})}} \tag{5.16}$$

Now the efficiency of the converter can be obtained

$$\eta = \frac{\mathrm{P_{out}}}{\mathrm{P_{in}}} = \frac{\mathrm{V^2}/\mathrm{R}}{\mathrm{V_{in}I_{in}}}\text{ , where } \mathrm{I_{in}} = \mathrm{I_L} \tag{5.17}$$

$$\eta = \frac{(1-\mathrm{D})\mathrm{V}}{\mathrm{V_{in}}} \tag{5.18}$$

For the N+1 level multilevel boost converter shown in figure 5.5 (b) we can write:

During on-state and assuming the capacitor charging current is negligible:

$$v_L(t) = V_{in} - R_L i_L(t) - R_{ds} i_L(t) \tag{5.19}$$

Where $\mathrm{R_L}$ the DC resistance of the inductor.

Now applying the small ripple approximation method:

$$v_L(t) = V_{in} - (R_L + R_{ds})I_L \tag{5.20}$$

During off-state

$$v_L(t) = V_{in} - R_L i_L(t) - V_F - V_C(t) \tag{5.21}$$

Now applying the small ripple approximation method:

$$v_L(t) = V_{in} - R_L I_L - V_F - V_C \tag{5.22}$$

When the boost converter operates in steady state, the DC component of the voltage across the inductor is zero therefore:

$$D\,(V_{in} - (R_L + R_{ds})I_L) + (1\text{-}D)\,(V_{in} - R_L I_L - V_F - V_C) = 0 \tag{5.23}$$

In addition:

$\frac{V_c}{V_{in}} = \frac{1}{1-D}$ so $\frac{V}{V_{in}} = N\frac{1}{1-D}$ therefore as $I_{in} = I_L$ so we have:

$$I_L = \frac{N^2 V_c}{R(1-D)} = \frac{NV}{R(1-D)} \tag{5.24}$$

Solving the above equations results in the following:

$$V_{in} + (D-1)V_F + (D-1)V_c - (DR_{ds} + R_L)I_L = 0 \tag{5.25}$$

Now substituting I_L into equation 5.25:

$$V_{in} + (D-1)V_F + \frac{(D-1)V}{N} - \frac{(DR_{ds} + R_L)NV}{R(1-D)} = 0 \tag{5.26}$$

$$V_{in} + (D-1)V_F + \left(\frac{(D-1)}{N} - \frac{(DR_{ds} + R_L)N}{R(1-D)}\right)V = 0 \tag{5.27}$$

$$V(D, V_F, R_{ds}, R_L) = \frac{(1-D)V_F - V_{in}}{\frac{(D-1)}{N} - \frac{(DR_{ds} + R_L)N}{R(1-D)}} \tag{5.28}$$

Now the efficiency of the converter can be obtained

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V^2/R}{V_{in}I_{in}}, \text{where } I_{in} = I_L \tag{5.29}$$

$$\eta = \frac{V(1-D)}{V_{in}N} \tag{5.30}$$

For a 3-level boost converter we have:

$$V(D, V_F, R_{ds}, R_L) = \frac{(1-D)V_F - V_{in}}{\frac{(D-1)}{3} - \frac{3(DR_{ds} + R_L)}{R(1-D)}} \tag{5.31}$$

$$\eta = \frac{V(1-D)}{3V_{in}} \tag{5.32}$$

To understand how each of these non-ideal parameters affects the voltage conversion ratio (VCR) and efficiency of the converter, the VCR and efficiency of the boost converter and 3-level converter are plotted against the duty cycle whilst varying

one parameter at a time. A 5V input voltage, 100mΩ DCR for the inductor, 200mΩ Rds for the MOSFET, 1V diode forward voltage-drop and a 20Ω load are the design parameters used for the conventional and 3-level boost converter; each plot demonstrates the effect of varying one parameter retaining the other design specifications.

The data in figures 5.6 and 5.7 show the conventional boost converter and 3-level boost converter VCR and efficiency as a function of duty cycle for different diode voltage-drops. The increased diode forward voltage-drop results in lower VCR and efficiency for both converters particularly at lower duty cycles. The 3-level converter has higher VCRs throughout the duty cycle range, although due to the two additional diode voltage-drops, the converter has lower efficiencies at any given duty cycle when compared to the conventional boost converter. It becomes quite critical when the design specifications demand a very high VCR as this directly demands an increased duty cycle on the FET and very low duty cycle on the diode that results in the consequences described in section 3.3.

For a given high VCR requirement in a closed loop converter, the 3-level converter operates with a lower duty cycle compared to that of the conventional converter leaving more scope for voltage regulation to compensate load and line changes. However, to achieve a very high VCR, the conventional converter is no longer

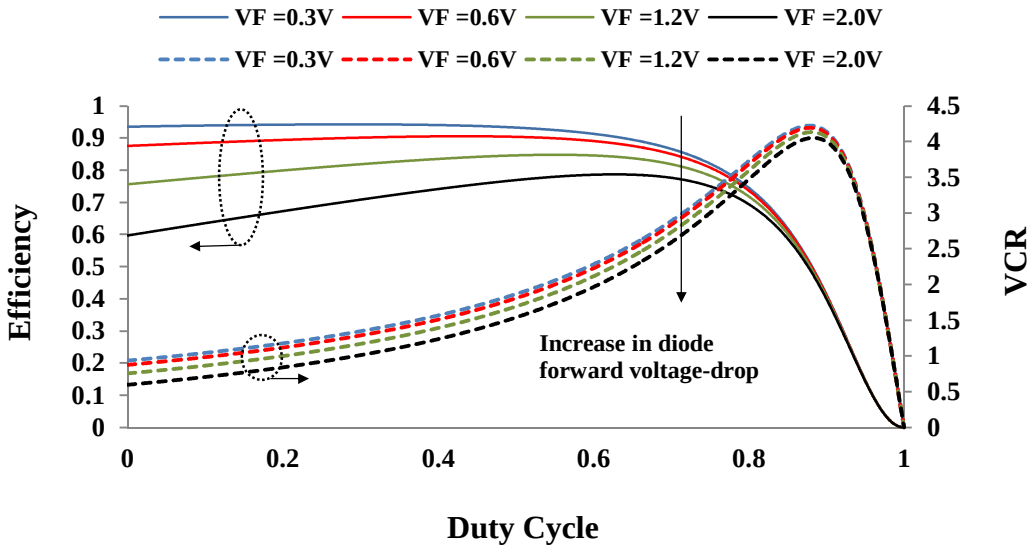


Figure 5.6: VCR and efficiency against duty cycle at different V_F for conventional boost converter

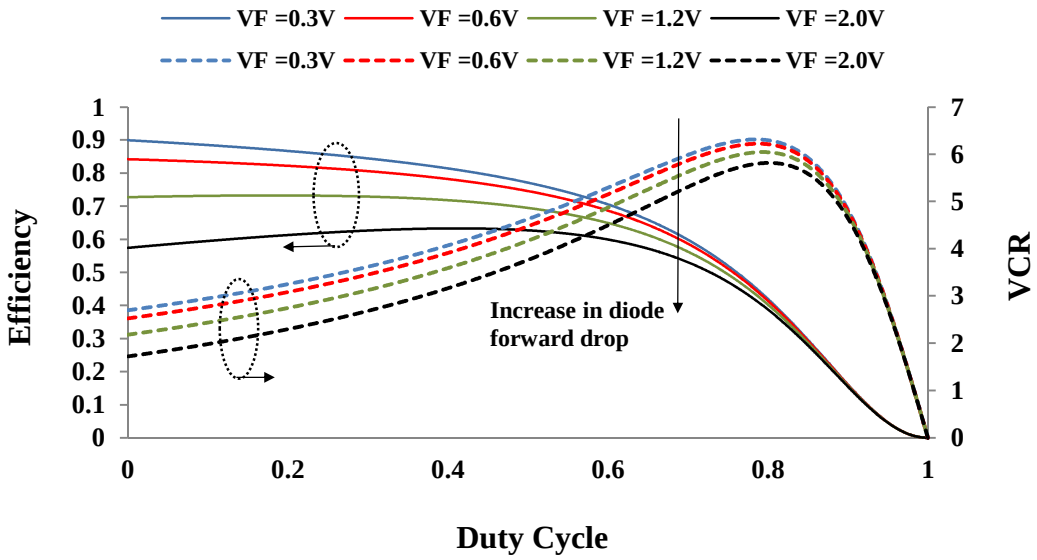


Figure 5.7: VCR and efficiency against duty cycle at different V_F for 3-level boost converter

the optimal solution. If the converter is not closed loop and operates with a very high duty cycle at any switching frequencies or any input voltages; then depending on the design requirements, the suitability of a conventional or multilevel converter topology needs to be investigated in greater detail. In section 5.6, a self-starting converter is proposed that boosts the output voltage of a thermoelectric generator to power a wireless sensor node. Depending on the output voltage requirements either a boost or 3-level boost converter may be used.

The data in figures 5.8 and 5.9 show the conventional boost converter and 3-level boost converter VCR and efficiency as a function of duty cycle for different input voltages. The higher the input voltage is, the higher the VCR and efficiency of both converters are at all duty cycles. A change in input voltage at low duty cycles has a larger impact on the efficiency than the VCR of the conventional converter. In addition, at high duty cycles the change in the input voltage has a larger impact on the VCR of the 3-level converter. Here again if both converters were to operate from a 5V input voltage and at a given duty cycle of 60%, the 3-level converter shows a higher VCR and a comparable efficiency when compared to the conventional converter.

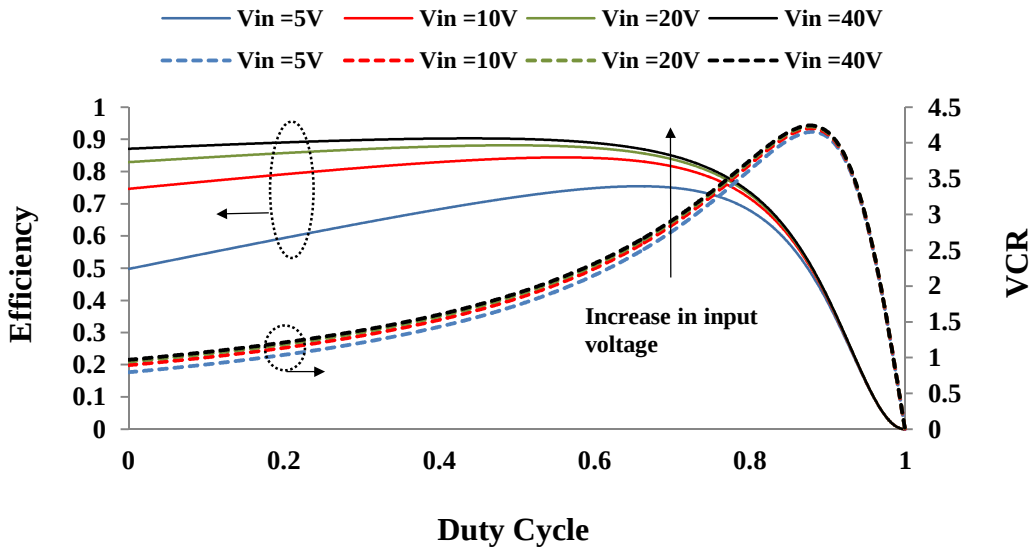


Figure 5.8: VCR and efficiency against duty cycle at different V_{in} for conventional boost converter

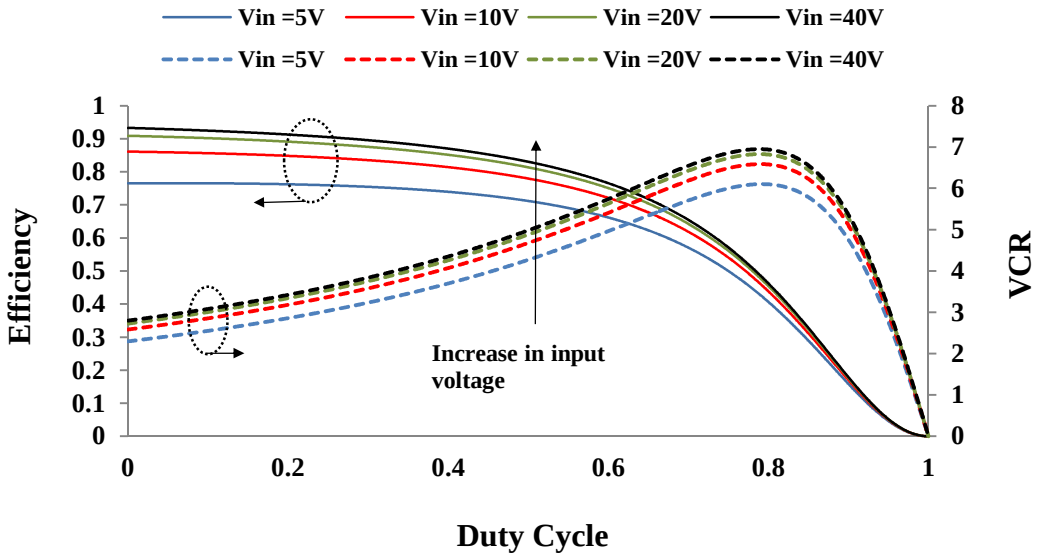


Figure 5.9: VCR and efficiency against duty cycle at different V_{in} for 3-level boost converter

The data in figures 5.10 and 5.11 show the conventional boost converter and 3-level boost converter VCR and efficiency as a function of duty cycle for different load resistances. Higher load resistance, results in increased efficiency and VCR for both converter topologies. As can be seen from the data, at high duty cycles the impact of load level on the VCR and efficiency of the converters are more pronounced. The 3-level converter shows more variation in both VCR and efficiency at different load levels when compared with the case for the conventional converter. At very high duty

cycles both converters show reduced efficiencies and highest VCRs that peak within a narrow duty cycle range. Here, if the converter was to operate at a fixed high duty cycle, depending on the load level, the duty cycle and the desired VCR, the more suitable boost converter topology would be determined.

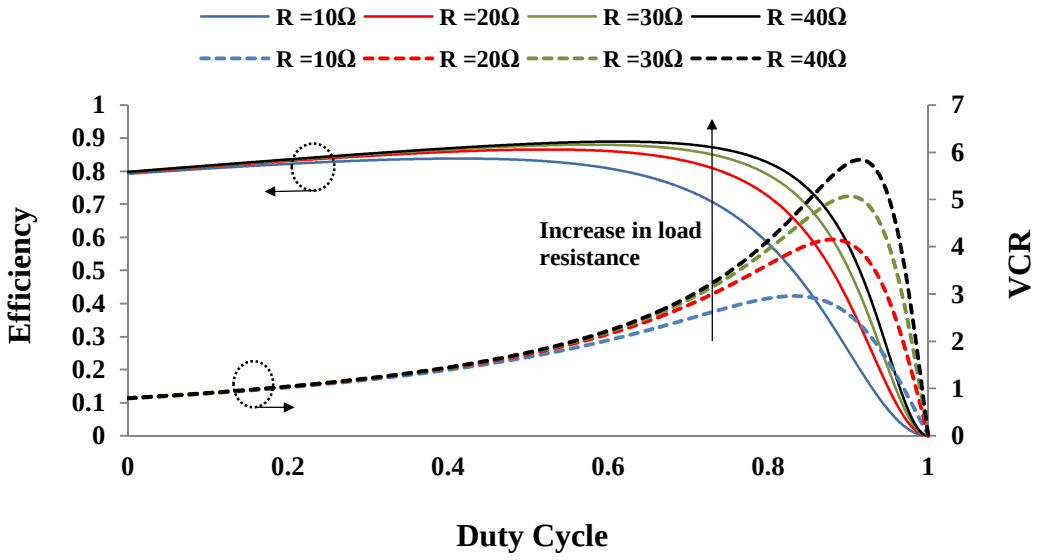


Figure 5.10: VCR and efficiency against duty cycle at different load resistors for conventional boost converter

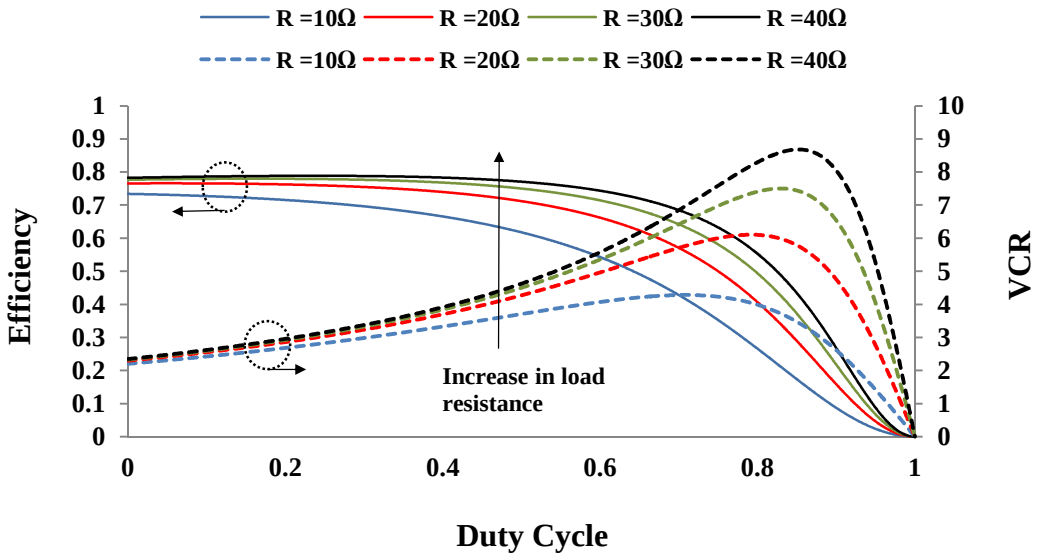


Figure 5.11: VCR and efficiency against duty cycle at different load resistors for 3-level boost converter

The data in figures 5.12 and 5.13 show the conventional boost converter and 3-level boost converter VCR and efficiency as a function of duty cycle for different DC resistances of the input inductor. It can be seen that the DC resistance of the input inductor limits the output voltage of the boost converter and the fact that a large voltage conversion ratio requires a small winding resistance. The efficiency is higher at low duty cycles and as the duty cycle and the inductor DC resistance increase, the efficiency decreases dramatically, due to power losses in the inductor windings.

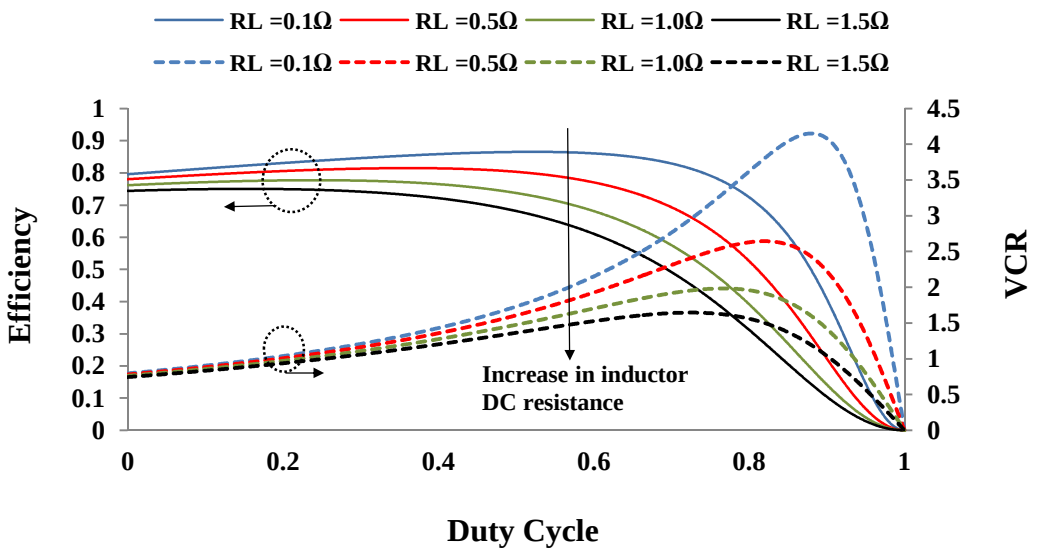


Figure 5.12: VCR and efficiency against duty cycle at different R_L for conventional boost converter

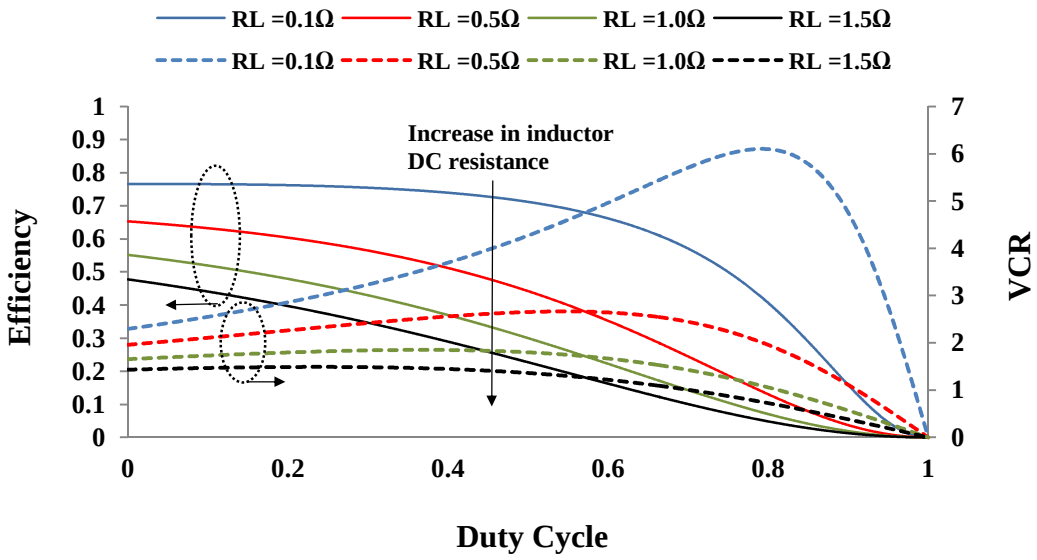


Figure 5.13: VCR and efficiency against duty cycle at different R_L for 3-level boost converter

The data in figures 5.14 and 5.15 show the conventional boost converter and 3-level boost converter VCR and efficiency as a function of duty cycle for different drain-source resistance (R_{ds}) values for the conventional and 3-level boost converters, respectively. The efficiency of the converters decreases as the duty cycle increases, whereas the VCR peaks at high duty cycles. In the 3-level boost converter both the VCR and efficiency of the converters are affected by the drain-source voltage drop for mid-range duty cycles. For the conventional converter however, both the VCR and efficiency drop significantly at high duty cycles.

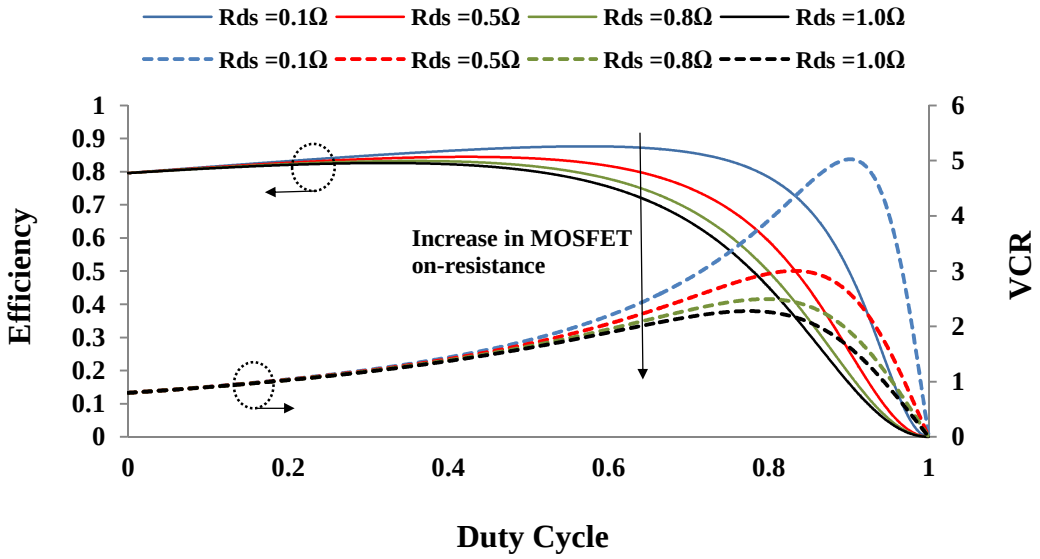


Figure 5.14: VCR and efficiency against duty cycle at different R_{ds} for conventional boost converter

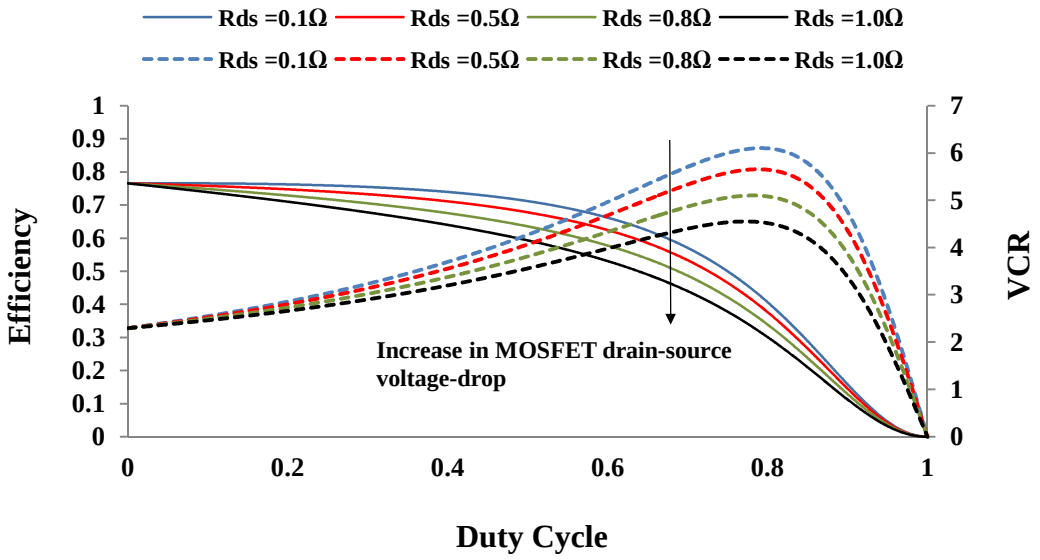


Figure 5.15: VCR and efficiency against duty cycle at different R_{ds} for 3-level boost converter

5.5 The Need for a High Temperature Self-starting DC-DC Converter

In addition to the VCR requirements, operating in a very high temperature environment (up to 300 °C) to supply a SiC sensor circuit, demands a high temperature step-up DC-DC converter. In addition to the power stage of the converter, the gate drive circuitry is also required to operate at elevated temperatures. To eliminate the need for a high temperature gate driver and also to reduce the size of the power management circuitry, a self-starting DC-DC converter is desired. Here, a self-starting DC-DC converter was designed to boost the low DC output voltage of a thermoelectric generator to a level sufficient to run a SiC sensor circuit for wireless monitoring of inhospitable environments [27-29]. These environments may be subject to high temperatures in the case of exhaust gas monitoring in turbine engines or oven environments, they may also be subject to radiation in the nuclear industry whether they are used in power generation or waste monitoring. The proposed DC-DC converter does not need an auxiliary power supply to drive the normally-on JFET. The converter self-starts and does not suffer from a start-up shoot through. The requirement of self-oscillation needs a depletion mode device (e.g. normally-on JFET) as there will be no current flowing at start otherwise.

5.5.1 Driving the SiC JFET

For the safe operation of normally-on SiC JFETs in the off-state, the gate-drive supply voltage must be more negative than the JFET pinch-off voltage and it must be less negative than the gate-junction reverse break-down voltage. If the latter voltage level is exceeded, depending on the JFET type, an avalanche or punch-through condition will occur. There are several approaches used in the literature to drive normally-on SiC JFETs [30-32]. One solution is use a cascode structure that uses a low voltage Silicon MOSFET to drive the normally-on SiC JFET as a normally off switch. The extra voltage drop across the Silicon MOSFET will contribute to the conduction losses. In addition, to operate successfully the Si MOSFET and SiC JFET must match and also the final structure temperature capability will be limited due to the use of Silicon MOSFET [33]. Alternatively, in [34] a protection circuit was proposed that utilises the start-up inrush current to turn off the JFET in a grid-connected switch-mode power supply.

The gate driver needs to address these design constraints, and also enables fast switching speeds of the device at high temperature. However, to operate DC-DC converters in high temperature environments, the gate driver needs to rectify the short circuit issue with the SiC JFET start-up and also drive the switch during normal running conditions at elevated temperatures.

5.6 The Self-starting DC-DC Converter

Figure 5.16 shows the circuit diagram of the proposed self-starting DC-DC converter designed for boosting low level voltages from the TEG, denoted in the figure as V_{in}. The input capacitance of the circuit, C_{in}, represents the capacitance of the p-n junctions of the TEG. Based upon a standard boost converter topology and a blocking oscillator, the key aspect of the design is the use of a counter-wound secondary winding in conjunction with a normally-on device which is used to provide the self-oscillatory behaviour, thus eliminating the need for an external gate drive. The elimination of a separate gate drive is crucial for the successful commissioning of a silicon carbide energy harvesting system designed for use with low voltage DC sources such as solar cells and thermo generators. The voltages provided by these sources are magnitudes smaller than the voltages required to start-up and run a silicon carbide oscillator therefore a self-oscillating design becomes the only viable option.

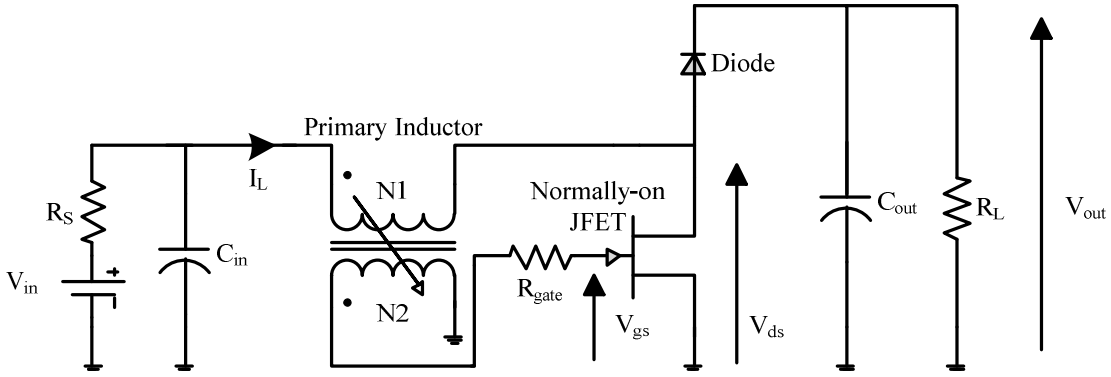


Figure 5.16: The proposed self-starting boost converter

The simplicity of the design is also important when considering the availability of high temperature components. At present, commercially available SiC components

are limited in their functionality and these are aimed at the power markets where the ability of silicon carbide to operate at high frequencies is utilised for space saving techniques. Here it is demonstrated that the ability to operate at these high temperatures can be harnessed for the production of a step-up converter with the ability to power circuits within the high temperature environment itself, with minimum component count, thus reducing the overall cost of a high temperature energy harvesting system.

5.6.1 Operation Principle

As shown in figure 5.17, the proposed circuit uses a depletion mode JFET and a Schottky diode in a boost configuration wherin coupled inductors are used to feed the gate-source of the SiC based switching device and act as a start-up circuit to start the oscillation. The operation of the circuit is as follows; at start up and as the input voltage rises, the SiC JFET as a normally-on device conducts at start-up and the current flows through the device. The current in the primary winding of the coupled inductor increases exponentially and the voltage across the winding decreases exponentially therefore a positive voltage is induced on the secondary winding of the transformer due to the change in the primary current and C1 is charged to a negative voltage until the input voltage has reached its maximum value at which the current of the primary winding becomes constant. At this point the voltage over the secondary winding of the coupled inductor becomes zero and the negative voltage across the capacitor will be across the gate source of the SiC JFET. Here, if this negative voltage is large enough, it will pinch off the switching device. The current in the primary winding of the transformer decreases and a negative voltage is induced across the secondary winding and as a result a negative voltage will be across the gate of the SiC JFET. The JFET has a high on-resistance so the primary current decreases further and the current flows through the diode D1 and the JFET turns off. When the current in the primary winding becomes zero, the voltage on the secondary winding reaches zero as well and C1 is discharged through the resistor R1 to the ground level therefore the switch conducts again and the circuit operation repeats. The switching frequency of the converter is determined by the gate-source capacitance of the SiC JFET and the inductance of the primary side of the drive transformer.

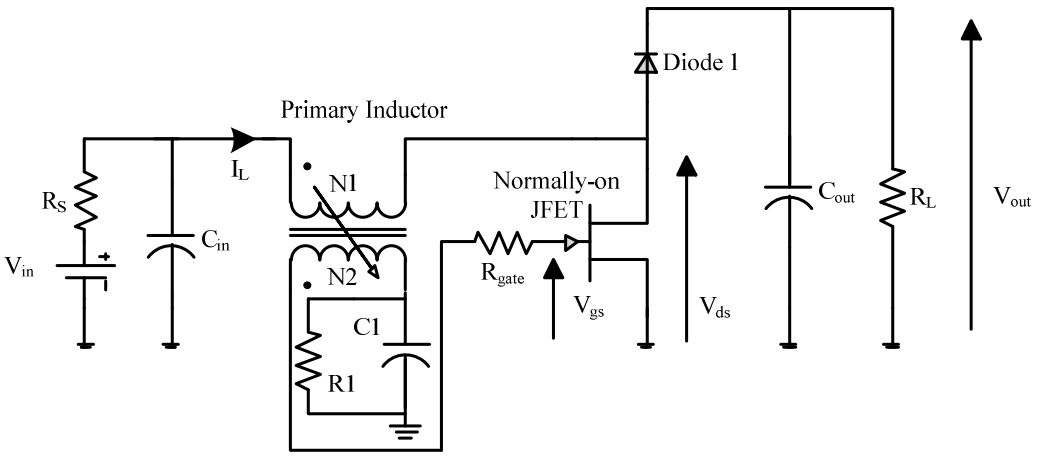


Figure 5.17: The self-starting step-up converter with the paralleled RC

As shown in figure 5.18 the parallel connection of the RC circuit can be removed and the secondary winding is directly connected to the ground. The stray capacitance of the primary winding is sufficient to make the self-oscillation occur and the converter operates without the inclusion of the external RC components.

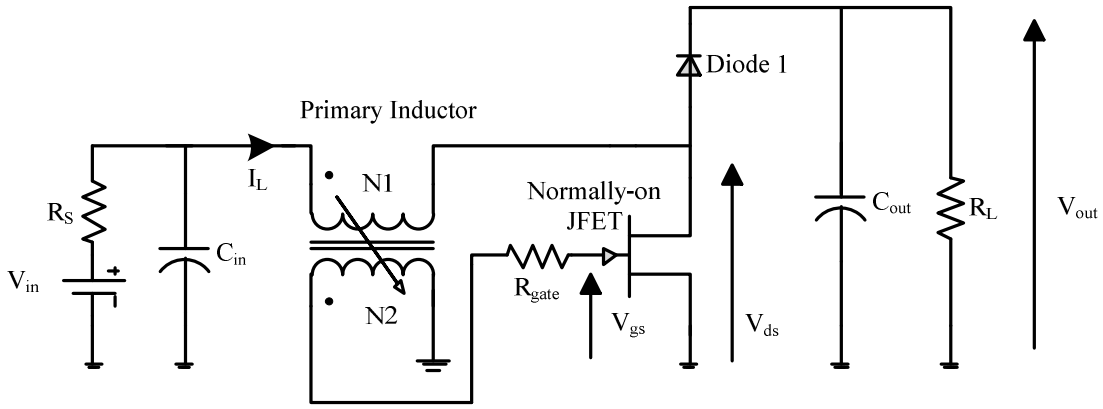


Figure 5.18: The self-starting step-up converter without the paralleled RC

When the normally-on silicon carbide JFET conducts, current begins to flow through the primary winding of the transformer and the channel of the JFET to ground, this induces a negative bias in the secondary winding. As the current flowing through the primary winding increases, the negative voltage on the secondary winding increases in magnitude and the channel of the JFET is progressively pushed towards pinch-off. Once the magnitude of the voltage on the secondary winding reaches the threshold

voltage of the JFET, the JFET becomes non-conducting. This causes the magnetic field contained in the ferrite core of the transformer to collapse and the voltage in the primary winding increases as is observed in a standard boost converter topology. Whilst the JFET is non-conducting, power is transferred to the output through the silicon carbide Schottky diode at a higher voltage level. The voltage induced on the secondary winding then drops due to reduced current flow in the primary and the JFET transistor becomes conducting again to complete the switching cycle.

Due to the use of the coupled inductor and self-oscillation, the converter module operates in the boundary between the CCM (Continuous Conduction Mode) and DCM (Discontinuous Conduction Mode) known as critical conduction mode. Whilst the JFET is non-conducting, the voltage induced on the secondary winding decreases due to reduced current flow in the primary. Therefore the JFET becomes fully conducting again when the inductor current has reached zero, which results in a zero voltage on the gate of the normally-on JFET. The schematic in figure 5.19 demonstrates the Critical conduction mode in a switching power supply; during on time the inductor charges and during the off-state the inductor fully discharges just as the switching period ends. Here the I_{avg} is 0.5Ipeak and the peak current is a product of the charging and discharging interval and the slope.

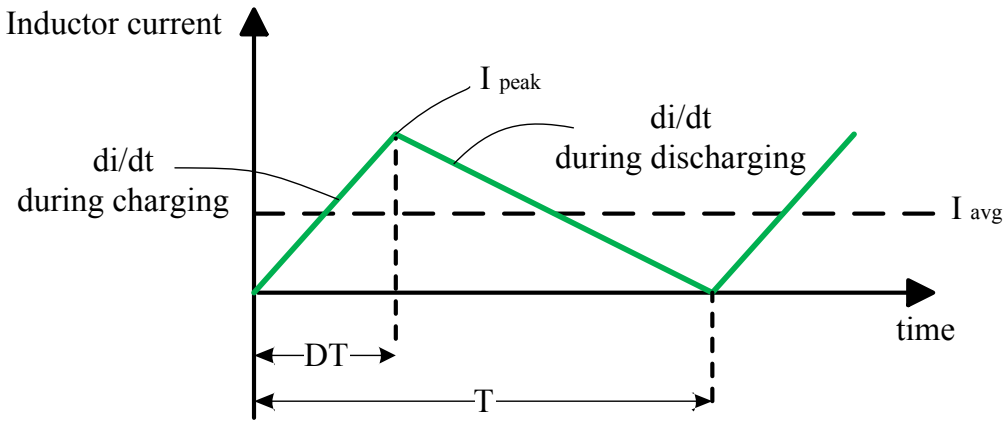


Figure 5.19: The critical mode of operation, boundary between CCM and DCM

5.6.2 Self-starting Converter Simulation Results

The design criteria of the converter are based on the requirement for steady-state operation of the semiconductor devices at the desired switching frequency. The converter is operated at an input DC voltage of 1V-2.5V. The output capacitor is selected as three 1µF capacitors, and the primary inductor is 400µH coupled with a 1mH secondary inductance. Table 5.1 show the converter design parameters for the self-oscillating boost without the paralleled RC circuit.

Converter Parameter	**Value**	**Converter Parameter**	**Value**
Input Voltage	1V-2.5V	Coupled Inductor Pri. Inductance	400µH
Input Capacitance	1µF	Output Filter Capacitors	3×1µF
Output Load	10kΩ	Coupled Inductor Sec. Inductance	1mH
Inductor Coupling Coefficient	0.99	Source Resistance	2.5Ω
Output Capacitor ESR	10mΩ	The Primary inductor DCR	50mΩ

Table 5.1: Self-starting boost DC-DC converter design parameters

The converter voltage and current waveforms at 1V input voltage are shown in figure 5.20. In the upper trace, V (gate) is the gate-source voltage of the n-channel JFET and V (in, drain) is the primary inductor voltage. On the second trace V(in) is the input voltage of the converter, V (out) is the output voltage and V(drain) is the drain-source voltage of the n-JFET. On the last trace, I(L) is the primary inductor current. The self-starting DC-DC converter has a switching frequency of 167 kHz. The voltage source resistance was set to 2.5Ω which is typical of the resistance for commercial TEG devices.

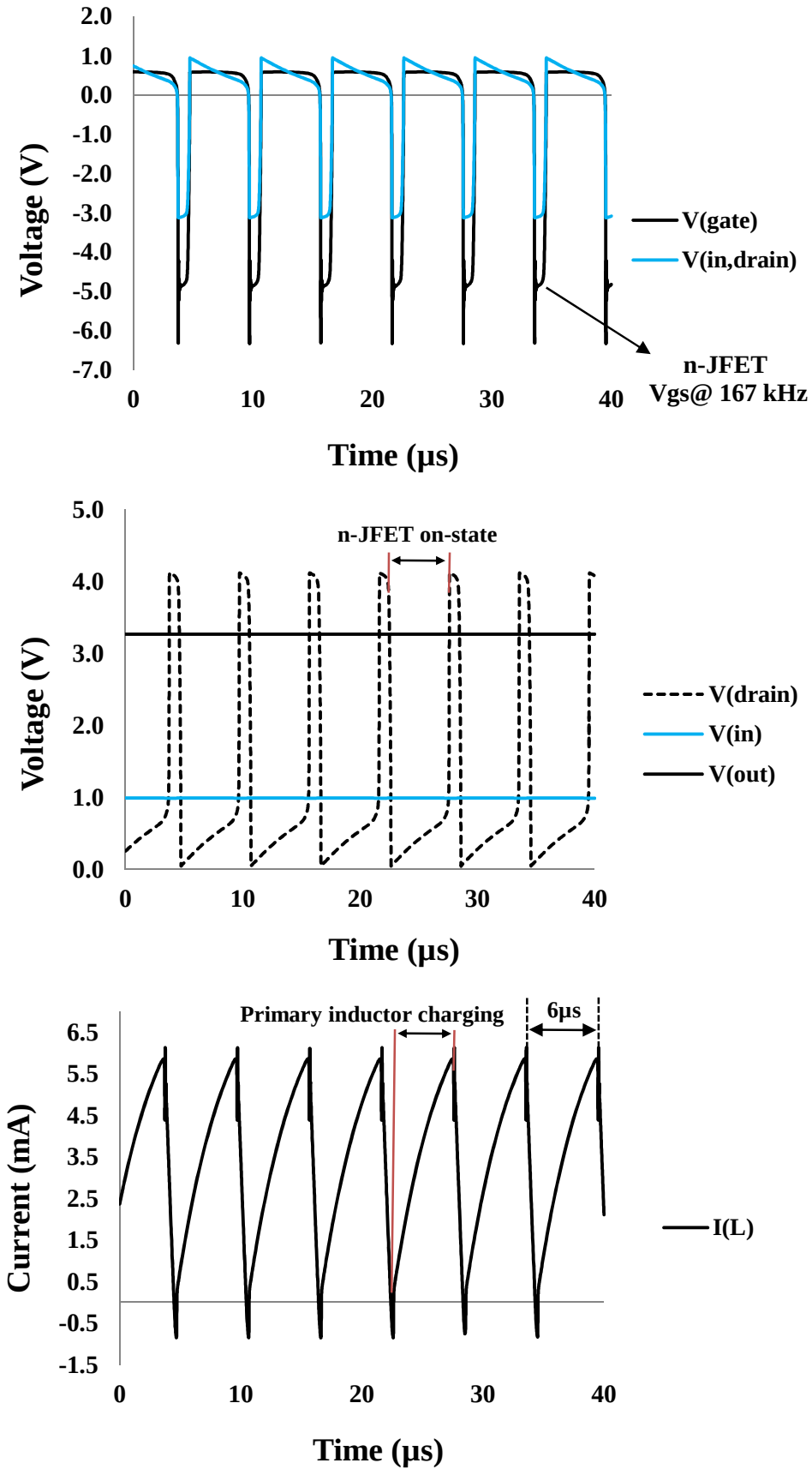


Figure 5.20: The converter voltage and current waveforms

The effect of the primary-winding inductance on the switching frequency of the converter is shown by the data in figure 5.21. The waveforms show the gate voltage of the JFET, the primary inductor current, the JFET current and the diode current at 125µH, 250µH and 500µH. The gate voltage of the JFET shows the effect of 3 different inductor values on switching frequency and gate-source voltage at turn-off. The gate voltage at turn-off varies between -7V and -4V and the switching frequency changes from 320 kHz to 140 kHz when changing the primary inductor from 125µH to 500µH. The inductor current demonstrates the critical mode of operation between continuous and discontinuous conduction modes. With 500µH primary inductance the on-time is maximum resulting in the largest switching period for the converter. The peak reverse recovery current of the diode at turn-off is clearly demonstrated at JFET turn-on current waveform.

The higher the inductance of the primary winding, the longer it takes for the inductor current to rise. The periods are larger hence smaller switching frequencies are achieved. This also reduces the level of gate-source negative-bias at turn-off. Depending on the threshold of the n-JFET under the test, the acceptance criteria varies. The turn-on time depends on the input voltage and the primary inductance, the period of the switching cycle depend on the primary inductance, n-FET gate capacitance and other stray inductance and capacitances in the circuit.

Figure 5.22 shows the simulation results for the converter with 400µH primary inductance when the input voltage was increased from 1V to 2.5V. The higher the input voltage is, the higher the voltage on the secondary winding of the coupled coil becomes. Depending on the threshold voltage of the normally-on JFET, the start-up capability of the converter at low input voltages would be determined. Considering the effect of temperature on both the threshold voltage of the JFET and the magnetic properties of the coupled inductor, the minimum start-up voltage-level can be determined. The turns ratio of the coupled inductor would also directly affect this; however, there will be a coil size-penalty for the increased turns ratio. In contrast, increasing the inductor turns ratio may have another penalty. As can be seen from the simulation results, at the high end of the input voltage range and the increased turns ratio, to address the low input voltage power-up capability, the increased negative-bias on the gate of the JFET can potentially exceed the maximum gate-source voltage rating of the device.

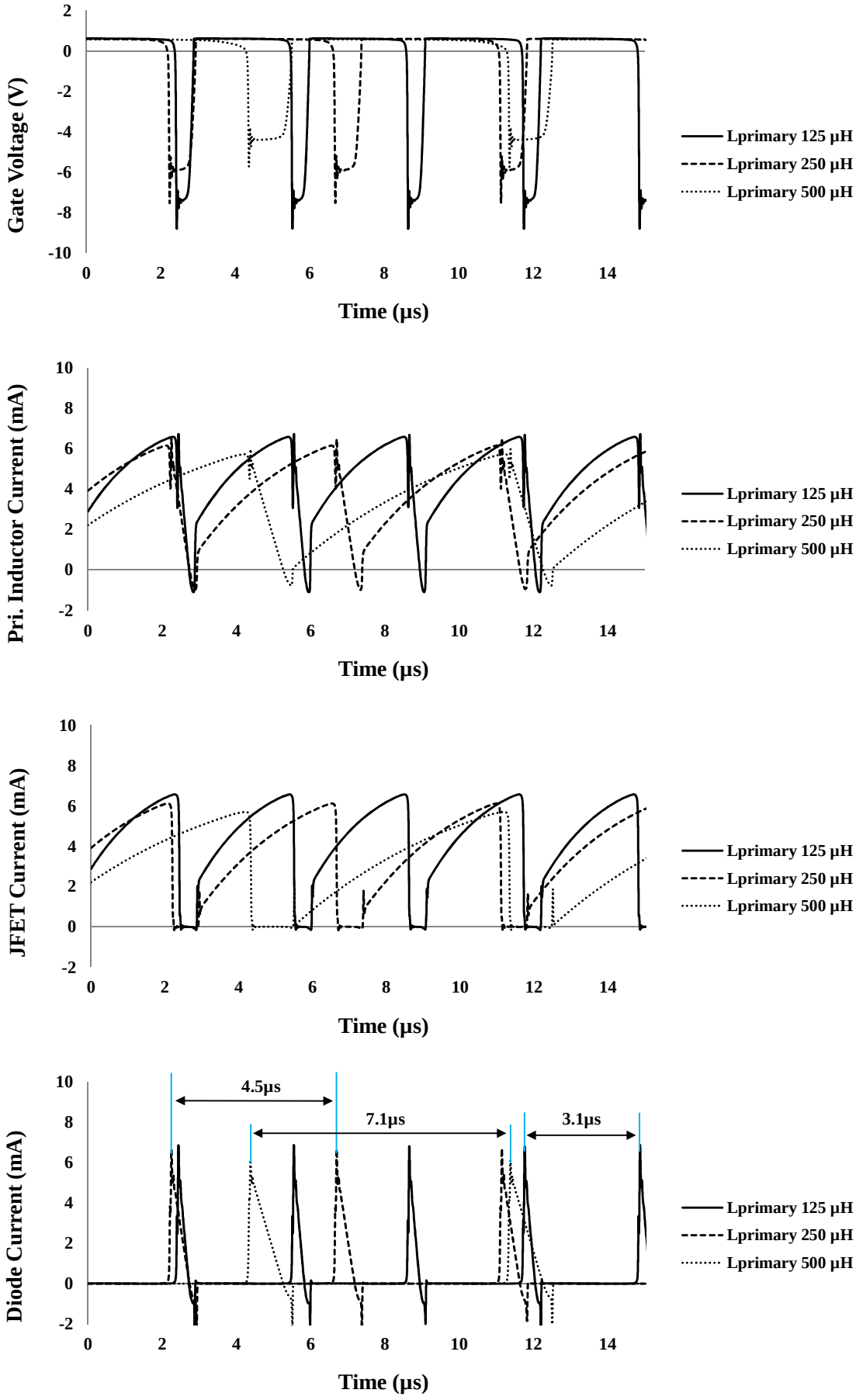


Figure 5.21: The converter voltage and current waveforms at different primary inductance values

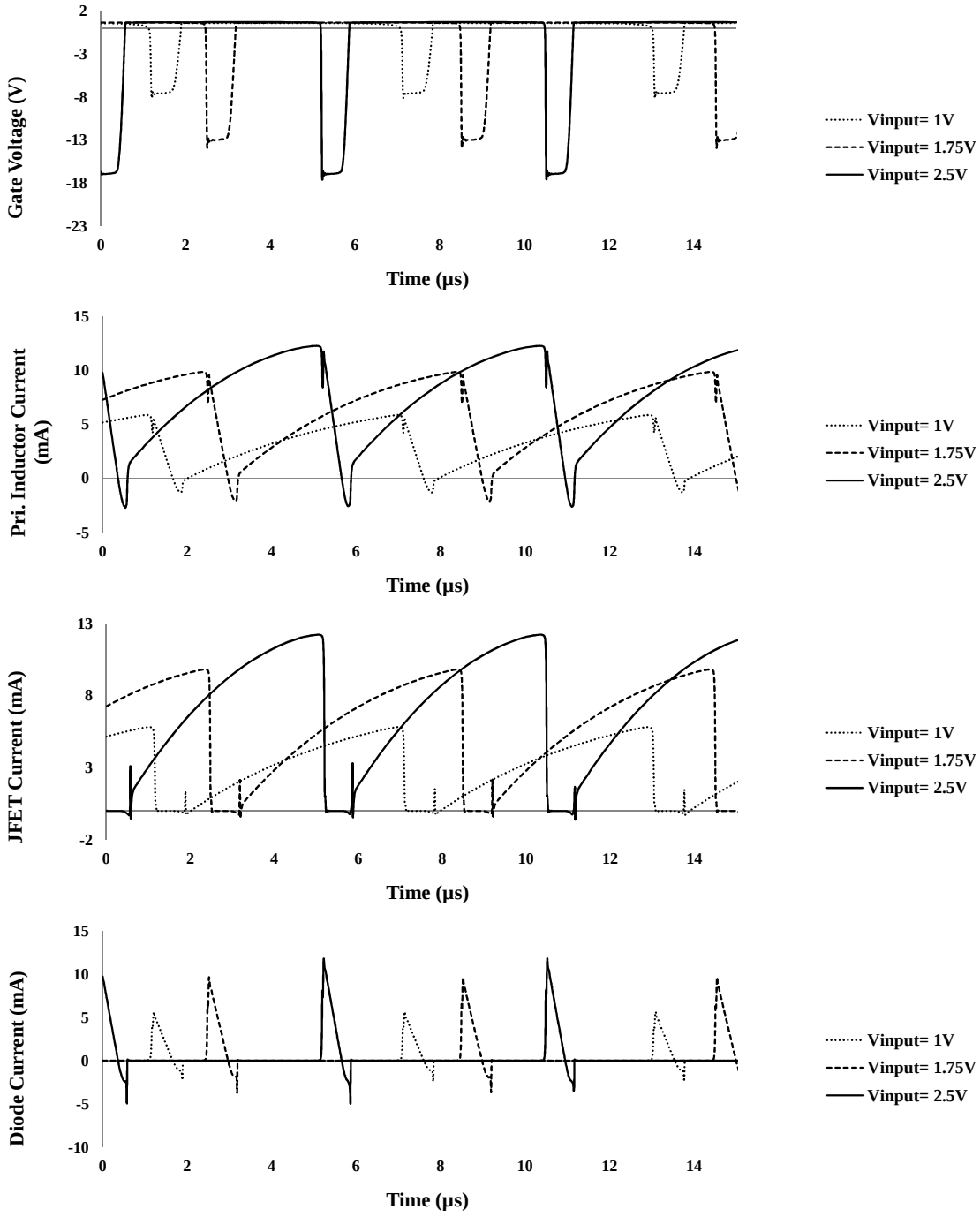


Figure 5.22: The converter voltage and current waveforms at different input voltages

During the on-time, the increased input voltage-level results in an increased rate of current change for the same primary inductance. This will determine the current levels on both the JFET and the free-wheeling diode. When the input voltage was increased from 1V to 1.75V and 2.5V, the output voltage of the converter increased from 5V to 9.2V and 12.4V, respectively, when supplying a 100 kΩ load.

5.6.3 Self-oscillating Multilevel Converter

To achieve higher voltage conversion ratios, the multilevel boost converter discussed in chapter 3 can be used in a self-starting multilevel boost configuration to achieve higher voltage conversion ratios. The schematic of the self-starting 3-level boost converter is shown in figure 5.23. Table 5.2 show the converter design parameters for the multi-level self-oscillating boost converter.

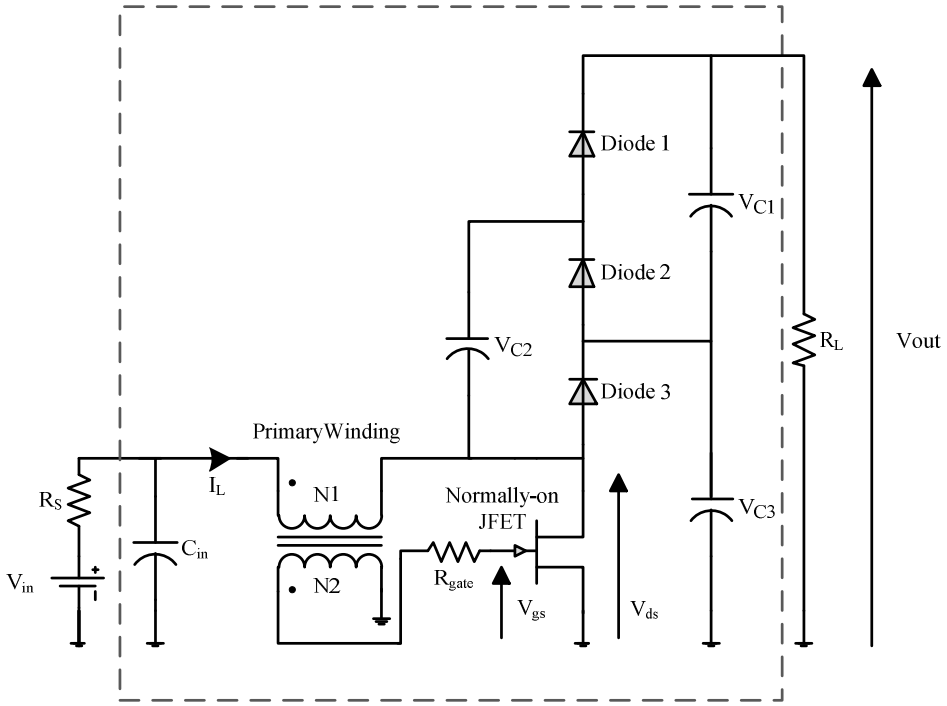
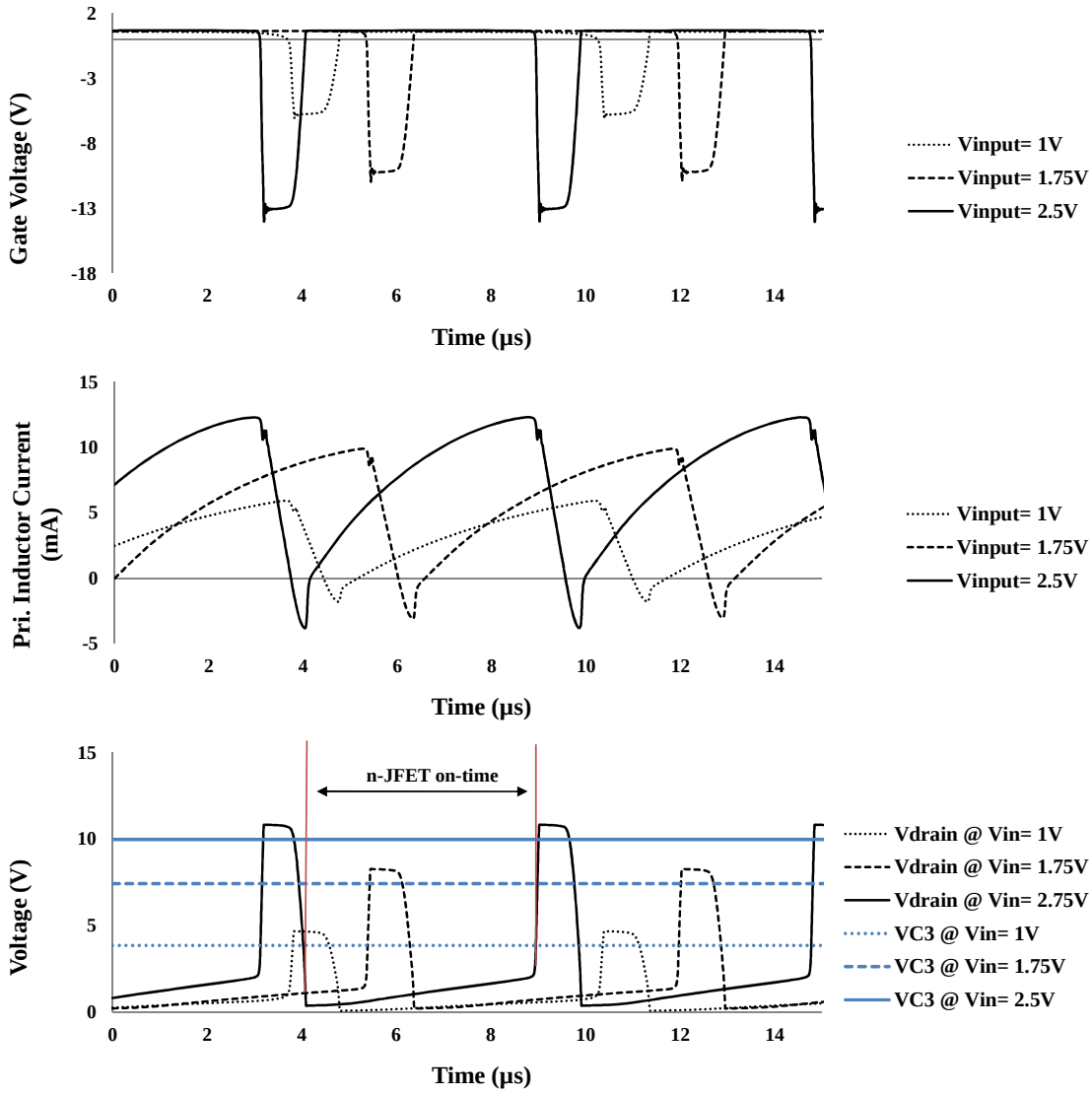


Figure 5.23: The 3-level self-starting boost converter

Converter Parameter	Value	Converter Parameter	Value
Input Voltage	1V-2.5V	Coupled Inductor Pri. Inductance	400µH
Input Capacitance	1µF	Filter Capacitors	3× (3×1)µF
Output Load	100kΩ	Coupled Inductor Sec. Inductance	1mH
Inductor Coupling Coefficient	0.99	Source Resistance	2.5Ω
Output Capacitor ESR	10mΩ	The Primary inductor DCR	50mΩ

Table 5.2: 3-level self-starting boost converter design parameters

Simulation results for the 3-level self-oscillating DC-DC boost converter are shown by the data in figure 5.24. For the primary and secondary inductances specified in table 5.2, the input voltage directly determines the gate-source voltage across the normally-on JFET. The inductor current rises during the on-state and the rate of current change is directly proportional to the line voltage. The drain voltage of the JFET and the output voltage of the first stage of the converter, $V_{C3,}$ are plotted at 3 input voltage levels. The drain voltage across the JFET rises during the off-state and the inductor stored energy is transferred to the 3 output capacitors through the free-wheeling diodes as described in chapter 3.



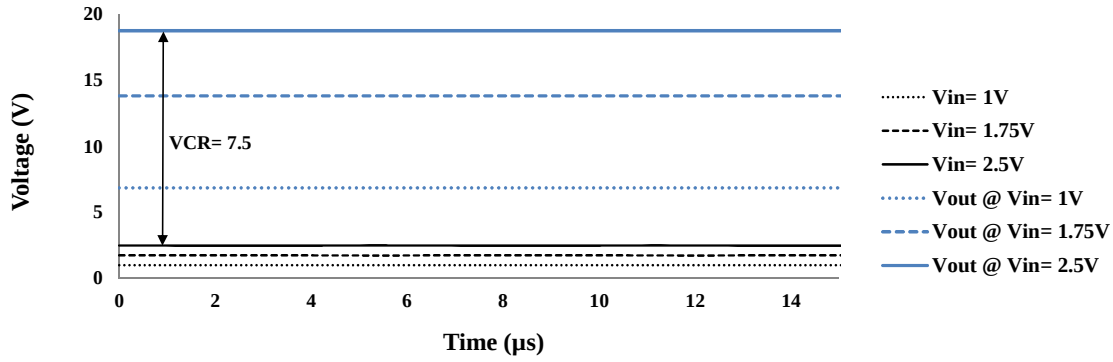


Figure 5.24: The 3-level self-oscillating converter voltage and current waveforms at different input voltages

For an input voltage of 1V, the voltage across the bottom capacitor, VC3, is 3.9V, which is lower than the output voltage gained by the single stage self-oscillating converter discussed in previous section (5V) for the same design specifications. In addition to the added switching losses, the additional free-wheeling diodes will directly affect the voltage conversion ratio of the converter.

As can be seen from the results, the output voltage of the 3-level converter, indicated as VC1+VC3, increases from 6.9V to 18.7V when increasing the input voltage from 1V to 2.5V. Even though the single-stage voltage gain of the multilevel converter is less than the equivalent boost converter, due to the added power loss of the additional components, the overall VCR is still is considerably higher. When the input voltage was increased from 1V to 2.5V, the voltage conversion ratio of the converter increased by 38% and 51%, respectively, compared to the single-stage self-oscillating converter.

5.7 Experimental Results for the Self-starting DC-DC Converter

5.7.1 High Temperature Coupled Inductor

The design of the high temperature transformer is crucial to the operation of this circuit topology. The primary inductance controls both the operating frequency and the observed voltage boost of the converter. In addition, the secondary winding must be of a ratio sufficient to produce a negative bias with a magnitude exceeding the threshold voltage of the JFET, in order for the converter to operate. The high temperature

transformer was wound using high temperature wire on a ferrite core with an appropriate Curie temperature. Here 4C65 grade ferrite material has been used, manufactured by Ferroxcube, which was selected due to the high Curie temperature, which is reported to be greater than 350 °C. The coupled inductor used in the converter is shown in figure 5.25. The characteristics of the inductor are shown in figure 5.26.

Figure 5.25: The coupled inductor wound on a high temperature toroid

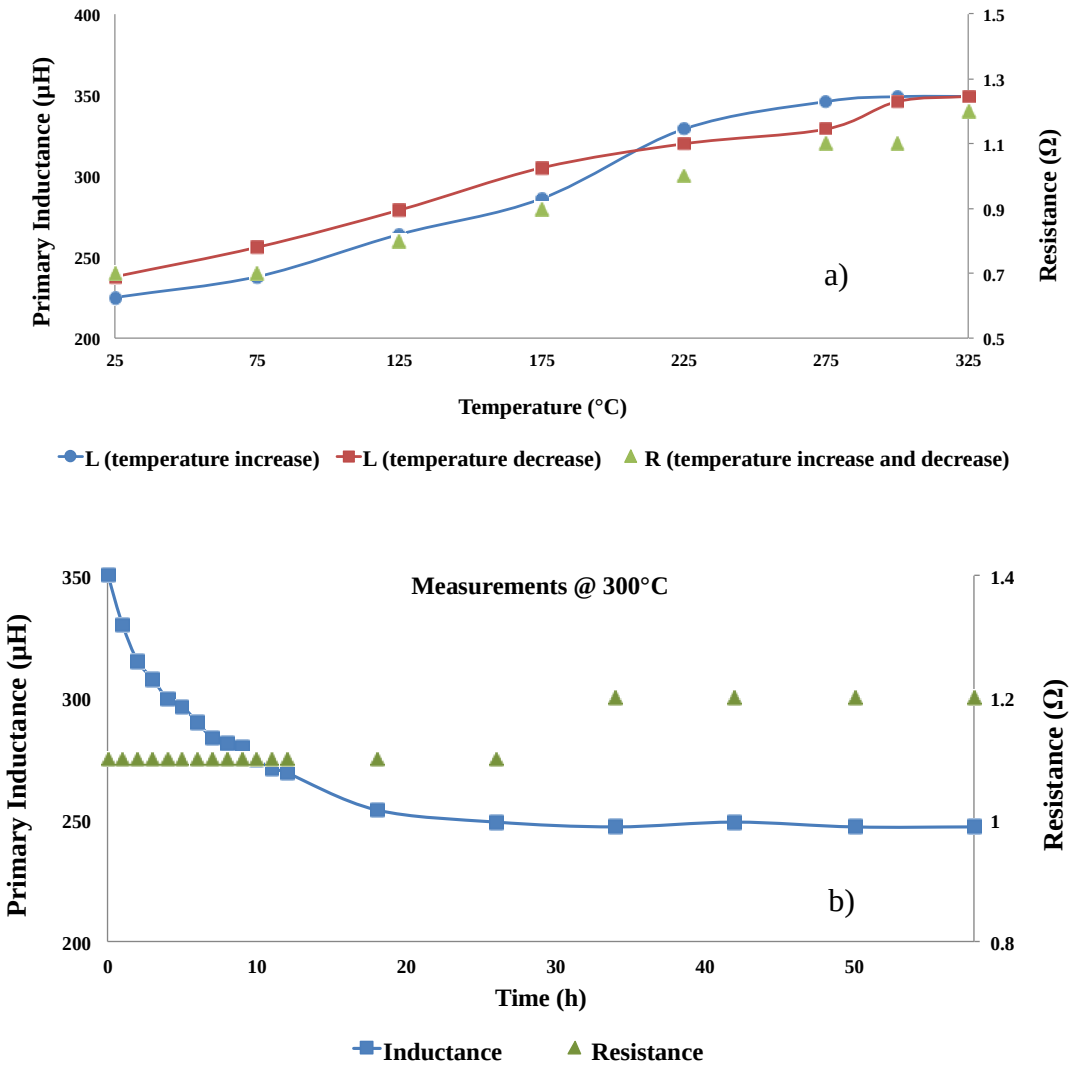


Figure 5.26: Primary winding inductance and DC resistance as a function of temperature (a) and time (b)

The inductance and DC resistance of the primary winding was measured as a function of temperature as shown in figure 5.26 (a). The temperature was swept between room temperature and 325 °C in 50 ° steps both in the upward and downward trends. The inductance of the primary winding increased from 225µH to 350µH while increasing the ambient temperature from 25 °C to 325 °C. The temperature was then reduced in 50 ° steps back to room temperature resulting in a reduction in inductance from 350µH down to 238µH. The DC resistance of the primary winding increased from 0.7Ω to 1.1Ω whilst increasing the temperature form room temperature to 325 °C. As shown by the data in figure 5.26 (b), the primary inductance of the coil was also measured as a function of time at the maximum ambient temperature of 300 °C to ensure the high temperature capability of the coil with ageing. The inductance measurements were carried out over a 60-hour time period that showed a reduction in the inductance value from 350µH to approximately 250µH and an increase in the coil resistance from 1.1Ω to 1.2Ω. The values after 60 hours were used in the SPICE simulation to more accurately evaluate the long-term converter performance.

The inductance change directly affects the switching frequency, voltage conversion ratio and efficiency of the converter while the DC resistance of the primary coil affects the voltage conversion ratio and the efficiency of the self-oscillating DC-DC converter. Figure 5.27 shows the increase in initial permeability of the core as a function of temperature up to 325 °C as reported by Ferroxcube. 325 °C is close to the Curie temperature of the ferrite core where the ferromagnetic properties are lost and the permeability of the material will fall significantly. During inductor testing the temperature was increased to 325 °C, however during the DC-DC converter experimental realisation the temperature was kept to 300 °C, as any sudden change to the magnetic properties of the core would have destructive consequences on the SiC switching devices. At this temperature, the permeability of the core falls abruptly, the inductance of the primary drops immediately and the converter switching frequency will increase significantly as a result that directly affects the SiC active semiconductors. In addition, as explained previously, at higher switching frequencies the secondary gate voltage drops with frequency that means that during the sudden inductance drop if the gate voltage of the JFET is less than the threshold level, the device remains on which can be destructive.

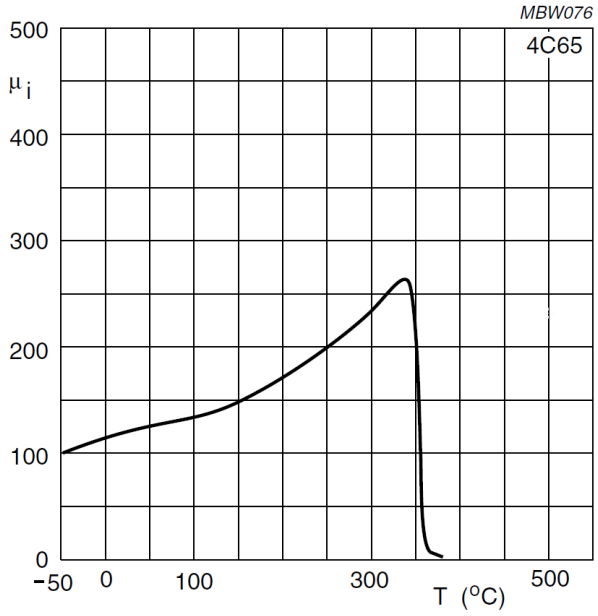


Figure 5.27: Initial permeability as a function of temperature [35]

5.7.2 Experimental Results for the SiC-based Converter

The SiC JFET and SiC Schottky diode were packaged in high temperature metallic packages and the circuit was placed in a temperature controlled Carbolite oven. The SiC Schottky diode was manufactured at Newcastle University. The SiC JFET used was a development part from Infineon. The I-V characteristics of the SiC JFET are shown in figure 5.28. As shown in figure 5.29, a 100 kΩ resistor was used as the load to mimic a wireless sensor node designed for high temperature energy harvesting applications. Typically due to the low amounts of energy supplied by an energy harvesting device sensor nodes are designed to intermittently use the power produced thus reducing power draw over time as there is insufficient power generated to continuously run a sensor node specifically the wireless transmission of data [36].

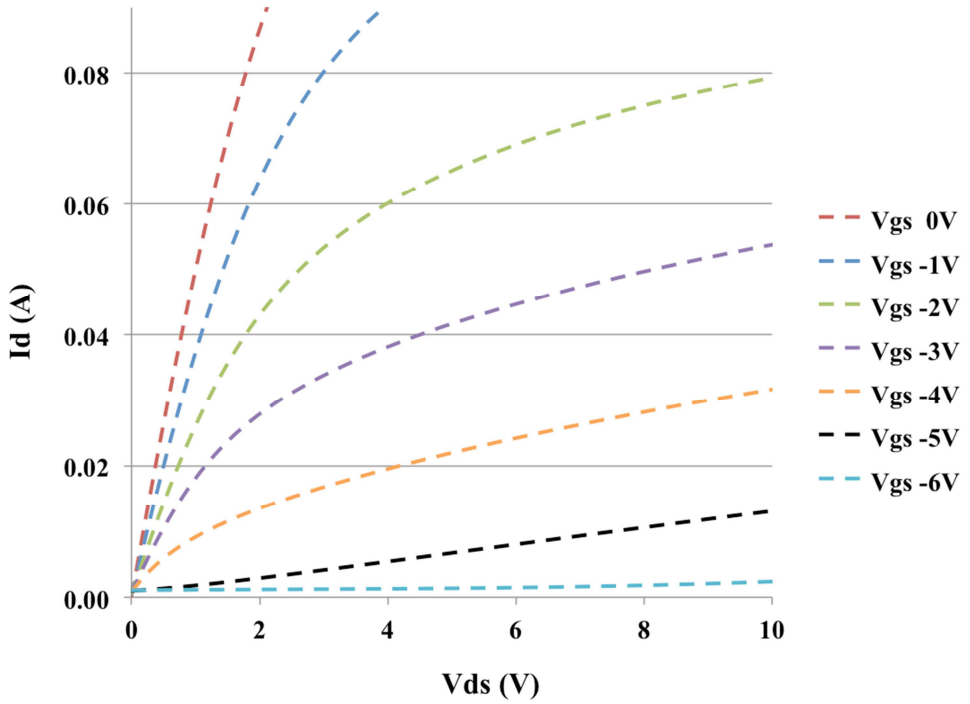


Figure 5.28: I-V characteristics of the SiC JFET used in the converter at 25 ºC

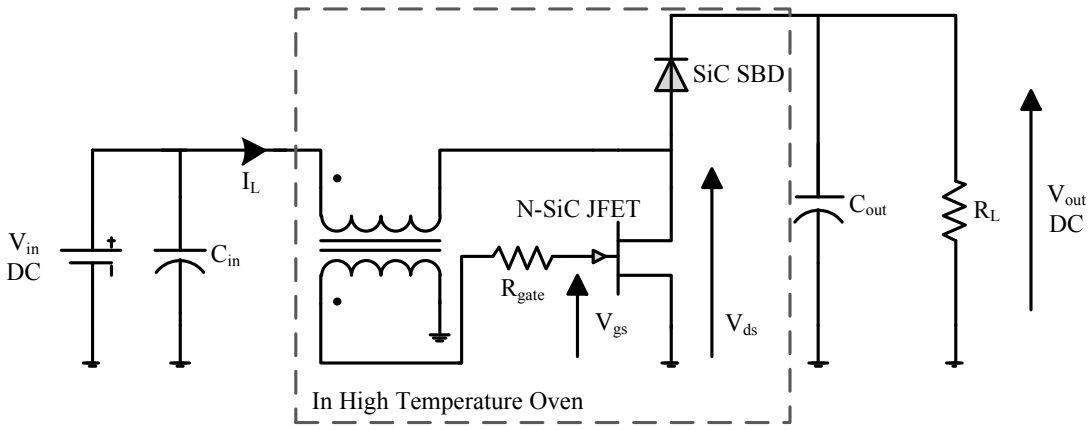


Figure 5.29: Schematic of the SiC self-starting DC-DC converter

Figure 5.30 depicts the voltage waveforms seen at the gate and the drain of the SiC JFET during operation at room temperature at 1V input supply. Figure 5.31 shows the primary current of the coupled coil pulsing at an 8µs period, equivalent to a 125 kHz switching frequency when the converter is running at room temperature.

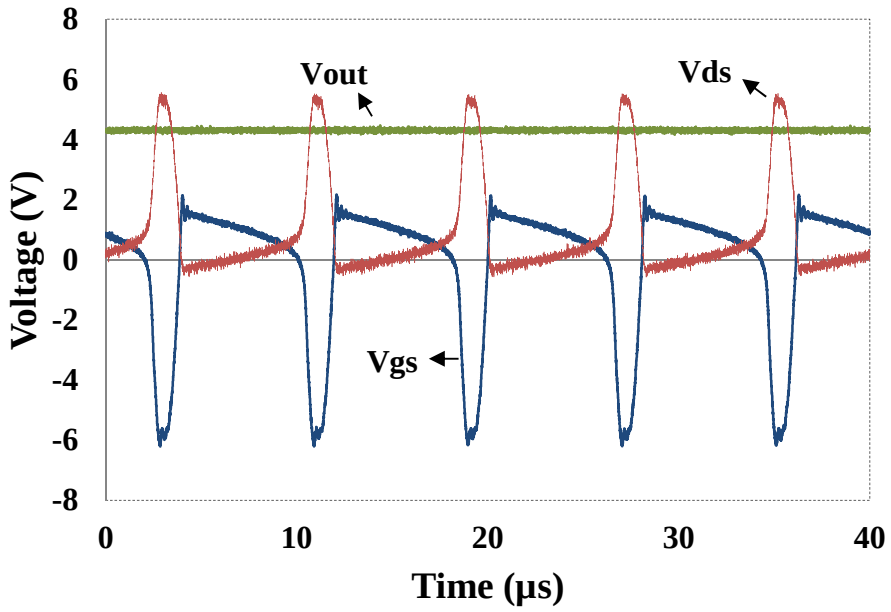


Figure 5.30: Voltage waveforms of the self-starting boost converter

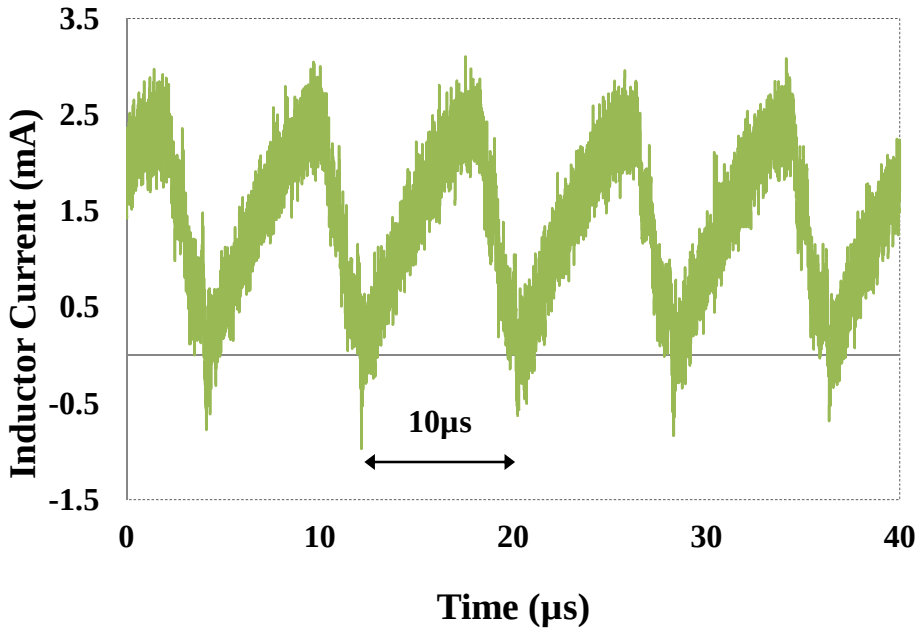


Figure 5.31: The primary winding current waveform

The data in figure 5.32 shows the variation in converter output voltage as a function of temperature. It can be seen that the boost converter can successfully operate at input voltages from 1.3V to 2.5V over the full 300 °C range demonstrating boost capabilities of up to 4.5 times the input voltage. At higher temperatures, the output voltage drops due to the increased SiC diode forward voltage-drop, increased JFET on-resistance and increased copper loss in the inductor windings. These effects were also shown in figures 5.6, 5.12 and 5.14. At input voltages below 1.2V, the converter

did not self-start at high temperatures. At input voltages of 1V, 1.1V and 1.2V the converter failed to self-start at temperatures above 150 °C, 200 °C and 250 °C, respectively. At low input voltages and high temperatures, the current increase in the primary winding will be lower, due to the increased primary inductance with temperature. Therefore the voltage induced in the secondary as a result of this current change will be lower. If the induced voltage on the secondary winding, i.e. the voltage across the gate-source of the n-JFET does not reach the threshold voltage of the device, the converter would not start.

Operation at lower input voltages can be achieved by increasing the ratio of turns between the primary and secondary coils of the transformer. These were not investigated during this work due to the physical size of the commercial ferrite core. From the results shown in figure 5.2, it can be seen that this converter would begin to oscillate and boost voltages with approximately a 40 °C temperature difference across the thermo generator, alternatively two thermo generators could be used connected electrically in series but thermally in parallel to allow the boost converter to operate at a lower thermal difference.

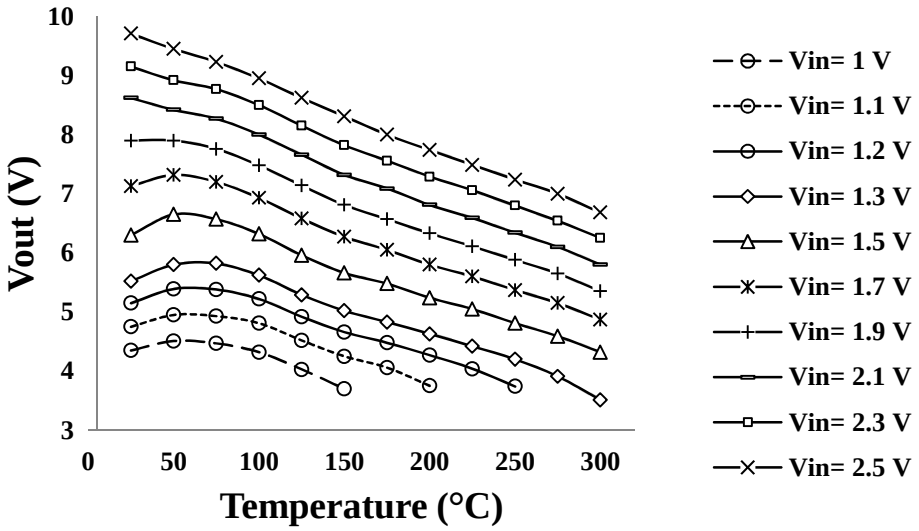


Figure 5.32: Output voltage as a function of temperature

The results in figure 5.33 show the effect of temperature on the operating frequency of the circuit. As discussed previously, the frequency of operation is determined by the inductance of the primary winding of the transformer and the input

voltage from the thermo generator. This is directly related to the material properties of the ferrite core with increasing temperature. As the temperature increases, the permeability of the selected ferrite core increases thus increasing the magnitude of the inductance of the primary winding as shown in figure 5.26. Therefore increasing the ambient temperature from 25 °C to 300 °C, results in the switching frequency of the converter decreasing from 183 kHz to 161 kHz and from 143 kHz to 107 kHz at input voltages of 2.5V and 1.3V, respectively. As can be seen in figure 5.33, the switching frequency also increases with input voltage when increasing the supply from 1V to 2.5V.

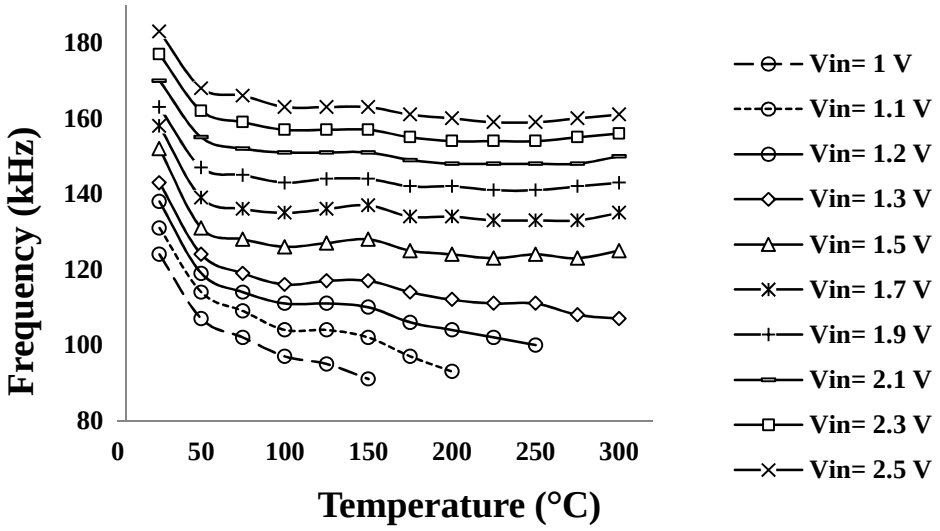


Figure 5.33: Switching frequency as a function of temperature

The converter overall power losses and efficiency as a function of temperature are shown in figures 5.34 and 5.35, respectively. As can be seen the efficiency is lower at higher temperatures this is to be expected due to the increased resistance of both the JFET channel and the increased resistance of the windings within the transformer itself. The diode voltage drop of the SiC Schottky diode also increases with temperature, so the overall conduction loss in the circuit increases. The higher the input voltage, the higher the power losses, due to the increased reverse voltage across the SiC JFET during switching. The current ripple in the inductor will also increase, which increases the conduction losses in the inductor, due to the increased RMS current. As the output voltage changes with temperature, the output power transferred to the constant resistive load also changes with temperature. The relationship between the converter efficiency, total power losses, output voltage and load is shown is equations 5.33 and 5.34.

$$\eta = \frac{P_{\text{out}}}{(P_{\text{out}}+P_{\text{Losses}})} \times 100 \tag{5.33}$$

$$\eta = \frac{\frac{{V_{out}}^2}{R_L}}{(\frac{{V_{out}}^2}{R_L}+P_{\text{Losses}})} \times 100 = \frac{{V_{out}}^2}{({V_{out}}^2+R_L P_{\text{Losses}})} \times 100 \tag{5.34}$$

As can be seen in figure 5.34, as the temperature increases the overall power losses drop; which can be explained by the reduced load current due to the reduced output voltage at higher temperatures. The overall converter losses decrease due to the reduction in the JFET on-resistance loss, SiC diode voltage-drop loss and the inductor primary DCR loss. The reduction in the output voltage with temperature results in a reduced drain-source voltage for the JFET, which pushes the device into its linear operating region. Hence the SiC JFET acts more like a resistor at temperatures above 275 ºC and the power losses start to increase with temperature. This can be seen in figure 5.34 for the data for input voltages of 1V and 1.1V. As the converter output power is very low, the losses in the circuit will play a significant role in the overall efficiency of the converter resulting in a low converter efficiency.

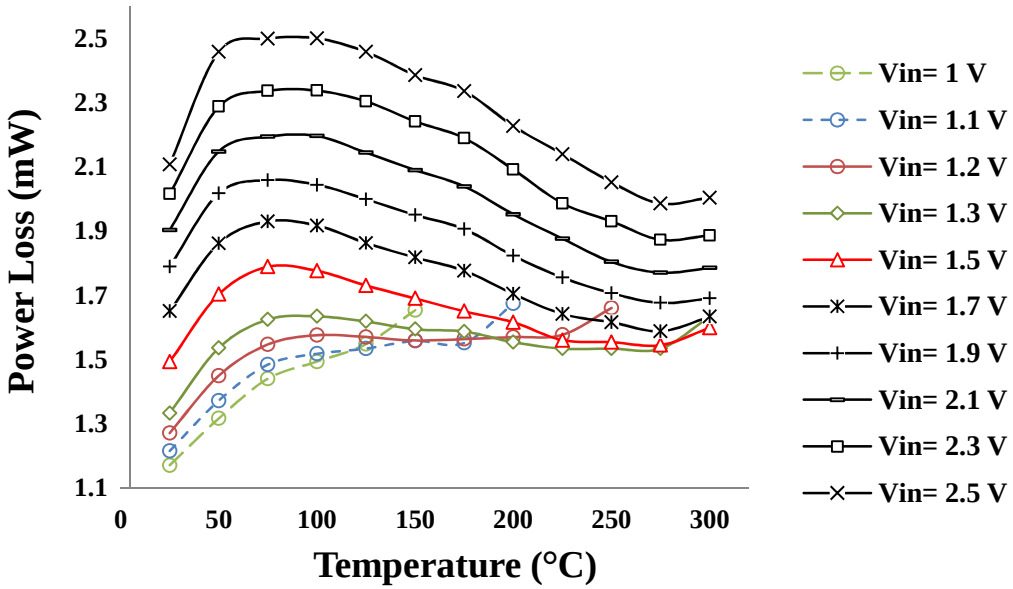


Figure 5.34: Power losses as a function of temperature

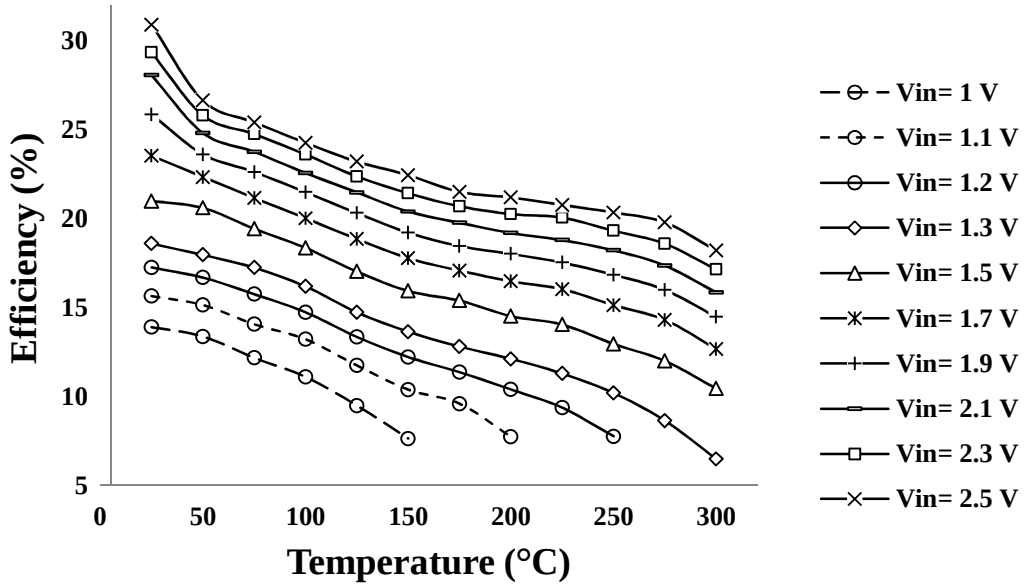


Figure 5.35: Efficiency of boost converter as a function of temperature

To assess the converter performance at higher output currents, a 10kΩ load was connected to the output and the converter was characterised for different input voltages and temperatures. The converter output voltage as a function of temperature for a range of input voltages is shown in figure 5.36. As can be seen from the data, the output voltage of the converter decreases as the temperature increases, in a manner similar to that shown in figure 5.32. At higher output current levels, the overall conduction and switching losses increase in the converter resulting in a drop of the output voltage. As the load current has increased (10kΩ), the output voltage of the converter is lower when compared to the case with a 100kΩ load, due to the increased conduction losses.

Similarly to the operation of the converter with the 100kΩ output resistor, at input voltages below 1.3V, the converter did not self-start at high temperatures. At input voltages of 1V, 1.1V,1.2V and 1.3V the converter did not self-start at temperatures above 125 °C, 175 °C, 200 °C and 250 °C, respectively. At a higher output current, the effective voltage across the primary inductor is lower; due to the increased voltage drop across the inductor DCR, resulting in a lower induced voltage in the secondary winding. If this secondary voltage across the gate-source of the JFET does not reach the threshold voltage of the device, the converter does not start. Hence for the higher output current (10kΩ load) the converter exhibits a start-up issue at lower temperatures when compared to the case with a 100kΩ load resistor.

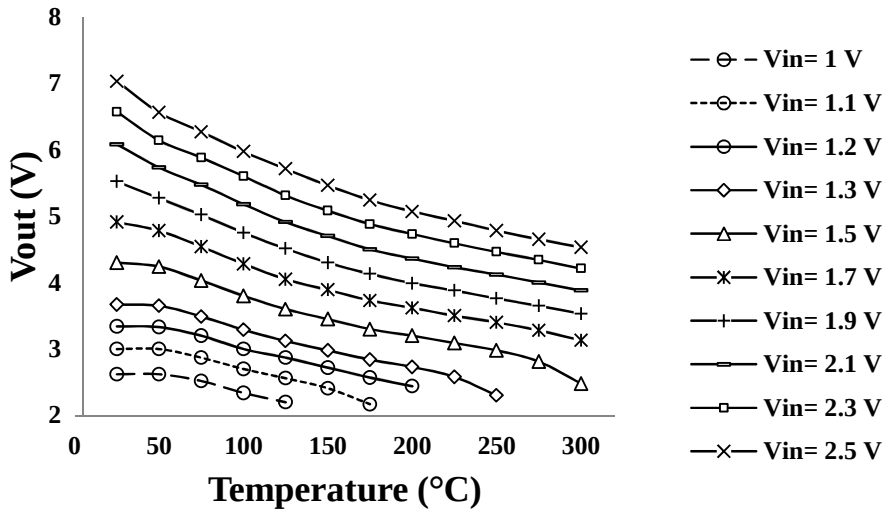


Figure 5.36: Output voltage as a function of temperature

The converter overall efficiency as a function of temperature is shown in figure 5.37. As can be seen the efficiency of the converter is approximately twice that of the converter supplying a 100kΩ load. Similarly, at higher temperatures the increased resistance of both the JFET channel and the windings within the transformer itself result in a reduction in efficiency. The SiC diode voltage-drop also increases with temperature, so the overall conduction loss in the circuit increases as a consequence. As can also be seen that the efficiency decrease with temperature is not as steep as that of the converter with the lower load. As the converter output power is significantly higher, the power losses in the circuit will play a less significant role in the overall efficiency of the converter hence the converter efficiency is higher.

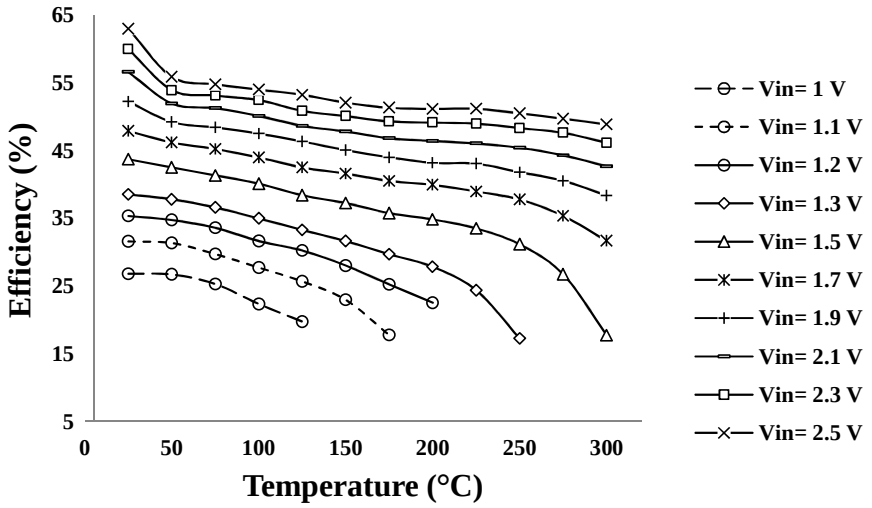


Figure 5.37: Efficiency of boost converter as a function of temperature

5.8 Conclusions

A novel self-starting converter technology was demonstrated for energy harvesting and powering wireless sensor nodes, constructed from silicon carbide devices and proprietary high temperature passives for deployment in hostile environments. The operation principle of the self-starting converter was detailed for two configurations. The effect of input voltage and primary inductance on the converter operation and switching frequency was explained by simulation results. A 3-level self-starting boost converter was also proposed and supported by simulation results.

The SiC JFET and SiC Schottky diode used in the converter were packaged in high temperature metallic packages and the circuit was placed in a temperature controlled Carbolite oven. Experimental results for the self-starting converter operating from room temperature up to 300 ºC were presented. The converter output voltage, switching frequency, total power loss and efficiency were presented at temperatures up to 300 ºC. A 100 kΩ resistor was used as the load to mimic a wireless sensor node designed for high temperature energy harvesting applications. The self-starting DC-DC converter was also tested at a higher load (10 kΩ). The converter with a higher load showed an improved efficiency with lower output voltages.

The commercial availability of more appropriate ferrite material for high temperature environments would result in higher efficiency power management circuits. However, the self-oscillating nature of the circuit along with high temperature capability result in reduced component count and hence a more reliable approach for powering SiC based WSNs for hostile environments.

5.9 References

[1] F. Issa, et al., "Radiation Silicon Carbide Detectors Based on Ion Implantation of Boron," Nuclear Science, IEEE Transactions on, vol. 61, pp. 2105-2111, 2014.

[2] J. Hornberger, et al., "Silicon-carbide (SiC) semiconductor power electronics for extreme high-temperature environments," in Aerospace Conference, 2004. Proceedings. 2004 IEEE, 2004, pp. 2538-2555 Vol.4.

[3] J.M. McGarrity, et al., "Silicon carbide JFET radiation response," Nuclear Science, IEEE Transactions on, vol. 39, pp. 1974-1981, 1992.

[4] S. Gopi Nambiar and P. Ranjan, "Energy harvesting system for deployment of Wireless Sensor Networks in Nuclear Fusion Reactor," in Green Technologies (ICGT), 2012 International Conference on, 2012, pp. 288-292.

[5] L. Xin and Y. Shuang-Hua, "Thermal energy harvesting for WSNs," in Systems Man and Cybernetics (SMC), 2010 IEEE International Conference on, 2010, pp. 3045-3052.

[6] S.S. Zhang, et al., " LiBOB-based gel electrolyte Li-ion battery for high temperature operation ", Journal of Power Sources, vol. 154, pp. 276-280, 2006.

[7] R. Gomez Cid-Fuentes, et al., "Energy Buffer Dimensioning Through Energy-Erlangs in Spatio-Temporal-Correlated Energy-Harvesting-Enabled Wireless Sensor Networks," Emerging and Selected Topics in Circuits and Systems, IEEE Journal on, vol. 4, pp. 301-312, 2014.

[8] L. Yibin, et al., "Energy-prediction scheduler for reconfigurable systems in energy-harvesting environment," Wireless Sensor Systems, IET, vol. 4, pp. 80-85, 2014.

[9] J. A. R. Azevedo and F. E. S. Santos, "Energy harvesting from wind and water for autonomous wireless sensor nodes," Circuits, Devices & Systems, IET, vol. 6, pp. 413-420, 2012.

[10] K. Jungmoon and K. Chulwoo, "A DC-DC Boost Converter With Variation-Tolerant MPPT Technique and Efficient ZCS Circuit for Thermoelectric Energy Harvesting Applications," Power Electronics, IEEE Transactions on, vol. 28, pp. 3827-3833, 2013.

[11] C. Xinping, et al., "Electromagnetic Energy Harvesting Circuit With Feedforward and Feedback DC-DC PWM Boost Converter for Vibration Power Generator System," Power Electronics, IEEE Transactions on, vol. 22, pp. 679-685, 2007.

[12] J. Valle-Mayorga, et al., "High-Temperature Silicon-on-Insulator Gate Driver for SiC-FET Power Modules," Power Electronics, IEEE Transactions on, vol. 27, pp. 4417-4424, 2012.

[13] M. A. Huque, et al., "A 200 ºC Universal Gate Driver Integrated Circuit for Extreme Environment Applications," Power Electronics, IEEE Transactions on, vol. 27, pp. 4153-4162, 2012.

[14] K. Mino, et al., "A gate drive circuit for silicon carbide JFET," in Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE, 2003, pp. 1162-1166 Vol.2.

[15] S. Round, et al., "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter," in Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005, 2005, pp. 410-416 Vol. 1.

[16] J. B. Casady, D. C. Sheridan, R. L. Kelley, V. Bondarenko, and A. Ritenour, “A Comparison of 1200 V Normally-OFF & Normally-on Vertical Trench SiC Power JFET Devices,” Material Science Forum, vol. 679-680, pp. 641–644, Mar. 2010.

[17] K. Norling, et al., "An Optimized Driver for SiC JFET-Based Switches Enabling Converter Operation With More Than 99% Efficiency," Solid-State Circuits, IEEE Journal of, vol. 47, pp. 3095-3104, 2012.

[18] J. M. Dilhac and M. Bafleur, "Energy harvesting in aeronautics for battery-free wireless sensor networks," Aerospace and Electronic Systems Magazine, IEEE, vol. 29, pp. 18-22, 2014.

[19] J. A. Paradiso and T. Starner, "Energy scavenging for mobile and wireless electronics," Pervasive Computing, IEEE, vol. 4, pp. 18-27, 2005.

[20] R. Vyas, et al., "Inkjet Printed, Self Powered, Wireless Sensors for Environmental, Gas, and Authentication-Based Sensing," Sensors Journal, IEEE, vol. 11, pp. 3139-3152, 2011.

[21] Y. Li, et al., "Hybrid Micropower Source for Wireless Sensor Network," Sensors Journal, IEEE, vol. 8, pp. 678-681, 2008.

[22] J. P. Carmo, et al., "Thermoelectric Microconverter for Energy Harvesting Systems," Industrial Electronics, IEEE Transactions on, vol. 57, pp. 861-867, 2010.

[23] S. Dalola, et al., "Autonomous Sensor System With Power Harvesting for Telemetric Temperature Measurements of Pipes," Instrumentation and Measurement, IEEE Transactions on, vol. 58, pp. 1471-1478, 2009.

[24] A. Prijic, et al., "Thermal Energy Harvesting Wireless Sensor Node in Aluminum Core PCB Technology," Sensors Journal, IEEE, vol. 15, pp. 337-345, 2015.

[25] D. Salerno, "Ultralow Voltage Energy Harvester Uses Thermoelectric Generator for Battery-Free Wireless Sensors," in Journal of Analog Innovation vol. 20, ed: Linear Technology, 2010.

[26] J. C. Rosas-Caro, et al., "Novel DC-DC Multilevel Boost Converter," in Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, 2008, pp. 2146-2151.

[27] K. Vassilevski, et al., "Silicon Carbide Vertical JFET Operating at High Temperature", Materials Science Forum, vol. 600-603, pp. 1063-1066, 2008.

[28] A.C. Patil, et al., "Characterization of Silicon Carbide Differential Amplifiers at High Temperature," in Compound Semiconductor Integrated Circuit Symposium, 2007. CSIC 2007. IEEE, 2007, pp. 1-4.

[29] N.G. Wright, et al., "SiC sensors: a review", J. Phys. D., vol. 40, 6345-6354, 2007.

[30] T. Friedli, et al., "Design and Performance of a 200-kHz All-SiC JFET Current DC-Link Back-to-Back Converter," Industry Applications, IEEE Transactions on, vol. 45, pp. 1868-1878, 2009.

[31] L. Rixin, et al., "A Shoot-Through Protection Scheme for Converters Built With SiC JFETs," Industry Applications, IEEE Transactions on, vol. 46, pp. 2495-2500, 2010.

[32] A. Rodriguez Alonso, et al., "Switching Performance Comparison of the SiC JFET and SiC JFET/Si MOSFET Cascode Configuration," Power Electronics, IEEE Transactions on, vol. 29, pp. 2428-2440, 2014.

[33] S. Kumar Singh, et al., "Comparative switching behaviour of silicon transistors and practical silicon carbide transistors," in Power Electronics and Drive Systems, 2009. PEDS 2009. International Conference on, 2009, pp. 585-590.

[34] K. Jong-Hyun, et al., "Protection circuit of normally-on SiC JFET using an inrush current," in Telecommunications Energy Conference, 2009. INTELEC 2009. 31st International, 2009, pp. 1-4.

[35] 4C65 Material Specification, Available: http://www.ferroxcube.com/.

[36] G.Yang,V.Y. F. Tan,C.K.Ho, S. H. Ting, and Y. L. Guan, “Wireless compressive sensing for energy harvesting sensor nodes,” IEEE Trans. Signal Process., vol. 61, no. 18, pp. 4491–4505, Sep. 15, 2013.

Chapter 6. Conclusion

6.1 Summary

One of the objectives of this thesis was to investigate the applications of SiC devices in high power density applications considering high frequency operation, thermal performance, efficiency and noise evaluation. Therefore the performance evaluation of SiC devices in a high power density power converter was required with a detailed comparison to the Si based design. To evaluate the performance of Si and SiC devices in a high efficiency high power density application, a 1kW DC-DC converter was designed and realised. The gate drivers for Si and SiC devices were designed considering the drive requirements of the semiconductor switches in the power converter. The Silicon and Silicon carbide DC-DC power converters were designed and tested under continuous conduction mode of operation in the frequency range of 100-250 kHz. Different device combinations were considered to evaluate the performance of the SiC MOSFETs, SiC JFETs and SiC Schottky diodes in comparison with their state-of-the-art Si counterparts. The SiC converter power efficiency, switch power loss and temperature measurements were experimentally evaluated and compared with those of the converter based on Si devices. An ultrafast isolated gate driver was designed and used for the Si and SiC MOSFETs and a two-stage DC-coupled gate driver was used to drive the enhancement mode SiC JFET.

For the converter based on Si CoolMOS and SiC Schottky diode, when the switching frequency was increased from 100 kHz to 250 kHz, the MOSFET total losses increased from 13.4W to 42.6W and the converter efficiency dropped from 95% to 92.5%. The converter based on SiC MOSFET and SiC Schottky diode was driven with a 20V gate-source voltage during on-state and 0V and -2V during the off-state. The use of a negative gate-voltage at turn-off minimises both the turn-on and turn-off power losses of SiC MOSFET. The turn-on losses are reduced from 8.1W to 7.8W and from 23.3W to 22.4W at 100 kHz and 250 kHz, respectively. The turn-off losses show a greater reduction and are reduced from 3.3W to 2.3W and from 8.2W to 5.3W at 100 kHz and 250 kHz, respectively. The overall power losses are reduced and the SiC MOSFET case temperature drops from 49 ºC to 43 ºC and from 108 ºC to 98 ºC at 100

kHz and 250 kHz, respectively. As the elevated temperature does not greatly increase the total power losses in the SiC MOSFET, the observed converter power efficiency does not decrease significantly and remains at approximately 95.5%. Even though a negative gate voltage was utilised to allow gate immunity at higher temperatures, the results showed a 10 ºC temperature drop in the SiC MOSFET when using a -2V gate-source voltage during off-time. The SiC JFET based converter efficiency peaked at 96% demonstrating a 0.5% efficiency improvement over the SiC MOSFET based converter. Similar to the case for the converter based on SiC MOSFET, efficiency showed only a weak frequency dependence.

A comparison of the radiated noise showed the highest radiated noise for the SiC JFET and lowest for the SiC MOSFET in the 20MHz-60MHz range. The negative gate voltage requirement of the SiC MOSFET also introduced up to 6 dBµV increase in radiated noise. The converter based on SiC MOSFET and SiC Schottky diode offered the best compromise between the converter efficiency and radiated noise.

A 500W 3-level SiC DC-DC converter was realised and the experimental data for the power losses and efficiency results were presented. The SiC MOSFET based 3-level converter had a 95% efficiency at 100 kHz switching frequency. This high efficiency transformer-less multilevel converter is suitable for renewable applications based on multilevel inverters; this design connects the input PV array to the multilevel inverter with a self-balancing output voltage and unidirectional current flow. In addition, three 500W SiC converters (a 3-level multilevel boost converter and two conventional boost converters) with a 400V output voltage and based on SiC MOSFETs and SiC Schottky diodes were designed and tested to evaluate the converter performance in terms of the radiated noise. The 3-level SiC converter showed a noise reduced by 15 dBµV in the test frequency range of 20MHz-60MHz compared to both conventional boost converters. The SiC MOSFET in the 3-level converter only experience 50% of the output voltage across the drain-source of the device during switching transitions and so has a lower noise level.

The high voltage conversion ratio of this SiC based multilevel converter topology without an excessively large duty cycle, reduced noise and high efficiency make it a great design choice for applications such as renewable applications where both the performance and noise compliance are of great importance. In addition, the use of SiC power devices at high switching speeds in the transformer-less DC-DC converter

is also suitable for applications where the weight and power density are critical design parameters.

As power converters are miniaturised, the gate driver and associated passive components are placed closer to the power semiconductor devices. Therefore the driver circuits will be exposed to similar environmental conditions as the power devices. Consequently, a temperature resilient PWM generator is desired in order to control the SiC devices operating at elevated temperatures. The objective was to realise a demonstrator circuit using high temperature switching devices offering a wide duty cycle range. Therefore, a SiC/SOI-based PWM generator was proposed and realised. The proposed circuit is composed of six functional blocks: SiC-based ring oscillator, SOI-based amplification and voltage shaping stage, SiC-based clamp, SiC-based current source, SOI-based control and a push pull buffer. The 3-stage ring oscillator enables a wide range of frequency tuning suitable for the operation of SiC-based DC-DC converters.

A SiC based constant current source was used as part of the triangular waveform generating stage with adjustable offset. Both the current source bias-resistor as well as the SOI MOSFET current limiting resistor can be used to adjust the dc offset of the generated waveform. The simulation results for the circuit utilising SiC JFETs in the ring oscillator and the current source stage and SOI MOSFETs in the amplification and control were detailed. It was shown that both the SOI MOSFETs can be replaced with SiC JFETs with minor modification to the control and amplification stages. The centre frequency was tuned to 200 kHz to take advantage of the SiC dynamic properties in the corresponding DC-DC converter. The 91% efficient step-up converter operated at 81% duty cycle and 200 kHz switching frequency. The proposed design also enabled the duty cycle control from 10% to 90%. As the design only uses SiC/SOI switching devices, the gate drive circuitry can be placed close to high power SiC power switching devices in the converter which is in exposure of higher ambient temperatures than a standard silicon-based PWM generator can tolerate.

To fully utilise the high-temperature capability of SiC devices in hostile environment where the converter needs to supply a wireless sensor node from a thermoelectric generator, a high-temperature DC-DC converter with large voltage conversion ratio is desired. The objective was to design and realise a high-temperature DC-DC converter module that is self-starting without a need for control electronics, to achieve small size and high reliability.

The output voltage of the thermoelectric generator is directly proportional to the temperature difference between its junctions. In practical applications, this low voltage is insufficient to support the drive for remote sensor applications. Consequenctly, a DC-DC step-up converter that can handle low input voltages is required. Therefore, a novel self-starting boost converter topology was demonstrated for energy harvesting and powering wireless sensor nodes, commissioned from silicon carbide devices and high temperature passives for deployment in hostile environments. The operation principle of the self-starting converter was detailed for two configurations. The effect of input voltage and primary winding inductance on the converter operation and switching frequency was shown by simulation results. In addition, a 3-level self-starting boost converter was proposed and the converter operation was presented by simulation results.

The SiC JFET and SiC Schottky diode used in the converter were packaged in high temperature metallic packages and the circuit was placed in a temperature controlled Carbolite oven. Experimental results for the self-starting converter operating from room temperature up to 300 ºC were presented. The converter output voltage, switching frequency, total power loss and efficiency were presented at temperatures up to 300 ºC. A 100 kΩ resistor was used as the load to mimic a wireless sensor node designed for high temperature energy harvesting applications. The boost converter could successfully operate at input voltages from 1.3V to 2.5V over the full 300 °C range demonstrating boost capabilities of up to 4.5 times the input voltage. At higher temperatures, the output voltage dropped due to the increased SiC diode forward voltage-drop, increased JFET on-resistance and increased copper loss in the inductor windings. Increasing the ambient temperature from 25 °C to 300 °C, resulted in the switching frequency of the converter decreasing from 183 kHz to 161 kHz and from 143 kHz to 107 kHz at input voltages of 2.5V and 1.3V, respectively. Operation at lower input voltages can be achieved by increasing the ratio of turns between the primary and secondary coils of the transformer.

The self-starting DC-DC converter was also tested at a higher load (10 kΩ). The converter with a higher load showed an improved efficiency. As the converter output power is significantly higher, the power losses in the circuit will play a less significant role in the overall efficiency of the converter hence the converter efficiency was approximately twice that of the converter supplying a 100kΩ load. The self-oscillating nature of the circuit along with high temperature capability result in reduced component

count and hence a more reliable approach for powering SiC based WSNs for hostile environments.

Finally, in order for SiC power devices to be commercially viable in power switching applications, component cost must be traded off against system level benefits such as smaller profile, lighter final design and increased power efficiency. For SiC, the chip cost is primarily determined by the cost of the starting material and material defect density that is high. Until major breakthroughs are realised in material growth technology, this situation is unlikely to change. Therefore the applications of SiC devices in low and medium voltage applications are only suitably viable in niche applications, where either the use of Si devices are impractical such as very high temperature environments (similar to those discussed in chapters 4 and 5) or where the Si devices do not provide sufficiently efficient solutions such as renewable applications (similar to those discussed in chapter 3) where the higher cost of SiC devices can be offset by the increased energy efficiency, robustness benefits and system-level cost.

6.2 Future Work

This work has demonstrated the application of Si and SiC devices in high frequency high power DC-DC Converters. The performance evaluation of Si and SiC devices and their associated radiated emissions were detailed. Higher switching speeds leads to smaller value inductors and capacitors hence high power density converters. Assuming that the power density of the converters has doubled with an increase in switching frequency by a factor of 10, the gate drivers used to drive SiC devices need to be improved to enable higher switching frequencies up to a few MHz in order to increase the power density of the SiC based power conversion system.

To fully utilise the volumetric improvements offered by the use of SiC devices, the design also requires a closer coupling of the passive components. The gate driver also needs to be placed as close to the SiC power devices as possible. The gate driver proposed in chapter 4 needs to be realised using high temperature passive components and to be tested at elevated temperatures in conjunction with the previously proposed high-temperature buffer stage in the literature. The frequency drift of the gate driver oscillating frequency also needs to be evaluated at elevated temperatures. The variable resistors used in the constant current source and the control stages need to be replaced

by SiC JFETs used as variable resistors to enable a variable duty cycle utilising only high temperature devices. The two SOI MOSFETs used in the amplification and waveform generating stages will be replaced by future high current SiC JFETs. As shown in chapter 4, this can be achieved with minor modification to the driver circuitry. The high temperature gate driver can then be placed very close to the SiC MOSFETs in the high frequency conventional or multilevel converter designs presented in chapter 3.

The parallel operation of SiC devices for higher power designs in the conventional and 3-level boost converters needs to be investigated and the converter performance in terms of efficiency and electromagnetic interference needs to be evaluated and compared to that of the converter using paralleled Si power devices. The effect of switching noise on both the power stage and gate driver of the converter needs to be investigated for the paralleled operation of the SiC devices at elevated temperatures. It is desired to investigate the effect of current mismatch of the paralleled devices on the converter noise emissions. The effect of the gate drive external resistor on the noise signature of the Si and SiC based converters using paralleled power devices, also needs to be investigated.

The proposed self-starting converter in chapter 5 can be optimised for efficiency, size and temperature. This can be done by utilising improved SiC devices with lower on-state losses, optimising the coupled coil design in terms of high temperature capability, mutual coupling and winding resistance. These performance improvements in addition to the increased turns ratio of the coupled inductor enables the converter to self-start at sub 1V input voltages, generated by very low thermal gradients across the thermoelectric devices, at temperatures beyond 300 ºC and provides larger voltage conversion ratios and increased converter efficiency. The proposed converter can also be used to power the SiC based oscillator presented in chapter 4. This combination allows the realisation of a self-powered high temperature gate drive without a need for any external power supply.