CHARACTERISATION OF SILICON CARBIDE CMOS DEVICES FOR HIGH TEMPERATURE APPLICATIONS

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Abstract

In recent years it has become increasingly apparent that there is a large demand for resilient electronics that can operate within environments that standard silicon electronics cease to function such as high power and high voltage applications, high temperatures, corrosive atmospheres and environments exposed to radiation. This has become even more essential due to increased demands for sustainable energy production and the reduction in carbon emissions worldwide, which has put a large burden on a wide range of industrial sectors who now have a significant demand for electronics to meet these needs including; military, space, aerospace, automotive, energy and nuclear. In extreme environments, where ambient temperatures may well exceed the physical limit of silicon-based technologies, SiC based technology offers a lower cost and a smaller footprint solution for operation in such environments due to its advantageous electrical properties such as a high breakdown electric field, high thermal conductivity and large saturation velocity. High quality material on large area wafers (150 mm) is now commercially available, allowing the fabrication of reliable high temperature, high frequency and high current power electronic devices, improving the already optimised silicon based structures. An important advantage of SiC is that it is the only wide band gap compound semiconductor that can be thermally oxidised to grow insulating, high quality SiO_2 layers, which makes it an ideal candidate to replace silicon technologies for metal-oxide-semiconductor applications, which is the main focus of this research. Although the technology has made a number of major steps forward over recent years and the commercial manufacturing process has advanced significantly, there still remains a number of issues that need to be overcome in order to fully realise the potential of the material for electronic applications.

This thesis describes the characterisation of 4H-SiC CMOS structures that were designed for high temperature applications and fabricated with varying gate dielectric treatments and process steps. The influence of process techniques on the characteristics of metal-oxide-semiconductor (MOS) devices has been investigated by means of electrical characterisation and the results have been compared to theoretical models. The C-V and I-V characteristics of both MOS capacitor and MOSFET structures with varying gate dielectrics on both n-type and p-type 4H-SiC have been analysed to explore the benefits of the varying process techniques that have been employed in the design of the devices.

The results show that the field effect mobility characteristic of 4H-SiC MOSFETs are dominated at low perpendicular electric fields by Coulomb scattering and at high electric fields by low surface roughness mobility, which is due to the rough SiC-SiO_2 interface. The findings also show that a thermally grown SiO_2 layer at the semiconductor-dielectric interface is a beneficial process step that enhances the interfacial characteristics and increases the channel mobility of the MOSFETs. In addition to this it is also found that this technique provides the most beneficial characteristics on both n-type and p-type 4H-SiC, which suggests that it would be the most suitable treatment for a monolithic CMOS process.

The impact of threshold voltage adjust ion implantation on both the MIS capacitor and MOSFET structures is also presented and shows that the increasing doses of nitrogen that are implanted to adjust the threshold voltage act to improve the device performance by acting to modify the charge at the interface or within the gate oxide and therefore increase the field effect mobility of the studied devices.

Acknowledgements

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A great deal of thanks is directed at Raytheon UK as all of the devices, which were investigated throughout this thesis were fabricated and supplied by their facility in Glenrothes, Fife, UK and without which this investigation would have been impossible.

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List of Publications

[1] L. C. Martin, H. K. Chan, M. H. Weng, R. F. Thompson, D. T, Clarke, E. P. Ramsay, N. G. Wright, A. B. Horsfall,“The impact of interface characteristics on the 1/f noise in SiC CMOS”, Physics and Chemistry of Surface and Interfaces, Salt Lake City, Utah, January 2015 (abstract submitted)

[2] L. C. Martin, H. K. Chan, D. Clark, E. P. Ramsay, A. E. Murphy, D. A. Smith, R. F. Thompson, R. A. R. Young, J.P. Goss, N. G. Wright, A. B. Horsfall,“Low frequency noise analysis of monolithically fabricated 4H-SiC CMOS field effect transistors,” Materials Science Forum, vol. 778-780 , p. 428-431, 2014.

[3] L. C. Martin, D. Clark, E. P. Ramsay, A. E. Murphy, R. F. Thompson, D. A. Smith, R. A. R. Young, J. D. Cormack, N. G. Wright, A. B. Horsfall,“Charge pumping analysis of monolithically fabricated 4H-SiC CMOS structures,” Material Science Forum, vol. 740-742, p. 891, 2013.

[4] L. C. Martin, D. Clark, E. P. Ramsay, A. E. Murphy, R. F. Thompson, D. A. Smith, R. A. R. Young, J. D. Cormack, N. G. Wright, A. B. Horsfall,“Comparison of oxide quality of monolithically fabricated SiC CMOS structures,” Material Science Forum, vol. 717-720, p. 773, 2012.

[5] R. F. Thompson, D. T. Clark, A. E. Murphy, E. P Ramsay, D. A Smith, R. A. R. Young, J. D. Cormack, J. McGonigal, J. Fletcher, C. Zhu, S. Finney, L. C. Martin, A. B. Horsfall,“High Temperature Silicon Carbide CMOS Integrated Circuits,” presented at the International Conference and Exhibition on High Temperature Electronics Network (HiTEN), Oxford, United Kingdom, 2011

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Chapter 1

Introduction

1.1 Introduction

Due to recent technological advances it has become increasingly apparent that there is a large demand for resilient electronics that can operate within environments that standard silicon electronics cease to function such as high power and high voltage applications, high temperatures, corrosive ambients and environments exposed to radiation. For such applications wide band gap semiconductors are a viable alternative solution. Silicon carbide (SiC) is an attractive semiconductor for such applications as it is a wide band gap semiconductor, has a high breakdown electric field, high carrier mobility and high electron saturation drift velocity. The intrinsic electronic properties of SiC coupled with its high thermal conductivity and stability and the commercial availability of high quality 150 mm wafers make it the ideal semiconductor to replace silicon (Si) for high temperature applications.

An enabling technology to meet these demands is that of SiC complementary metal-oxide-semiconductor (CMOS) technology which is compatible with current commercial silicon processing techniques and is the underpinning building block for many electronic systems for both digital and analogue applications for use in hostile environments [1]. Significant advances have been achieved within the technology over the last decade, however, there still remains a number of fundamental challenges within SiC CMOS and commercial signal level devices are not widely available [2]. Raytheon UK has focussed on silicon carbide research and development over the past decade and is currently looking to commercialise silicon carbide devices and integrated circuits, which rely on SiC CMOS technology, therefore, it is of fundamental importance to Raytheon UK to overcome some of the key issues and challenges within the technology in order to maximise on the current market opportunities, which will be discussed in further detail in chapter 2.

The investigations presented within this thesis are part of a concerted effort between the Emerging Technology and Materials research group at Newcastle University and Raytheon UK. This project focuses on the characterisation and understanding of 4H-SiC CMOS devices

that were designed and manufactured by Raytheon UK as part of the UK Technology Strategy Board 'Materials for Energy' scheme. A 4H-SiC 4 inch wafer fabricated with CMOS devices by Raytheon UK at their Silicon Carbide Foundry in Glenrothes, Fife, UK. All of the experimental results and data extracted from the devices discussed in this thesis were conducted at Newcastle University by the author of this thesis unless stated otherwise.

Raytheon UK is a technology and innovation leader specialising in defence, national security and other government and commercial markets around the world and designs, develops and manufactures a wide range of high technology electronic components and systems [3].

1.2 Motivation

There is significant industrial demand for electronics that are capable of high temperature operation, the deamdn stemming from two main motivations. Firstly high performing electronics that can operate reliably at elevated temperatures will remove the need for thermal management systems such as cooling and heating sinking components, which currently provides a significant overhead which can have a negative impact on the system as a whole such as size, weight and financial cost. Secondly the development of high temperature electronics which can operate in more demanding environments will allow the control and monitoring of environments that up until now have been inaccessible such as deep well drilling for the oil and gas industry and the monitoring of nuclear energy generation [2]. High temperature electronics would also lead to increased device reliability at more moderate temperatures (200 ^{o}C) where early failure of silicon devices is currently an issue such as in the oil and gas drilling where companies lose half a million US dollars for each day that is required to replace failed electronic components from the drill. The developed technology would have a significant impact across several industries including aerospace, automotive, communications, oil and gas, space and more generally in any harsh industrial environment.

Silicon carbide (SiC) technologies provide a viable solution to address all of the challenges outlined above. SiC is suited to high temperature operation and allows a significant reduction in the thermal management and heat-sinking requirements of electronics. In extreme environments, where ambient temperatures may well exceed the physical limit of silicon-based technologies, SiC based technology offers a lower cost and a smaller footprint solution for operation in such environments.

SiC is a wide band gap semiconductor with advantageous electrical properties such as low intrinsic carrier concentration, high breakdown electric field, high thermal conductivity and large saturation velocity [4]. High quality material on large area wafers (150 mm) is now commercially available, allowing the fabrication of reliable high temperature, high fre-

quency and high current power electronic devices, improving the already optimised silicon based structures. The increased demand for SiC as it is a potential solution for a variety of application areas such as high power, high radiation and high frequency applications as well as high temperature environments could also make the technology more economically viable in line with increased demand and production worldwide. An important advantage of SiC is that it is the only wide band gap compound semiconductor that can be thermally oxidised to grow insulating, high quality SiO_2 layers [5], which makes it an ideal candidate to replace silicon technologies for metal-oxide-semiconductor applications, which is the main focus of this research.

The commercial availability of single crystalline 4H-SiC wafers over the past 20 years has created a great deal of interest in SiC device applications. Wafer quality has gradually increased along with wafer diameter and there has also been a significant increase in the processing technology for 4H-SiC, which will be discussion further in chapter 2 and offers a significant opportunity for the development and manufacture of commercial devices and circuits [6].

The market forecasts for sales of silicon carbide power devices, integrated circuits and power modules are anticipated to be in excess of $100 million worldwide by 2020. As the only open European based silicon carbide fabrication facility, Raytheon UK is seeking to address both the power device and harsh environment markets in silicon carbide. Raytheon Semiconductors aims to double its revenue in the next 8 years through its involvement in these markets. The material properties of silicon carbide support high efficiency power, electric vehicles and photovoltaics and will act as an enabler for the sustainable, green economy. Raytheon UK is currently leveraging its 10 year history in silicon carbide research and development to focus on two product lines; firstly offering silicon carbide to manufacturing services to power device original equipment manufacturers (OEMs). The second area of interest is the design and manufacture of silicon carbide integrated circuits, building on its existing proven Si CMOS experience, this market is expected to be worth $400 million in the next 5 years [7].

The motivation behind the collaboration between the Emerging Technology and Materials research group at Newcastle University and Raytheon UK is to aid the commercialisation of the technology through overcoming some of the more fundamental physical challenges that are currently inhibiting 4H-SiC CMOS device performance. Newcastle University has significant expertise in the area of SiC device fabrication and characterisation and has in-house capabilities such as a high temperature electrical probe station along with a Keithley 4200 SCS Semiconductor Parameter Analyser, low frequency noise capabilities and atomic force microscopy capabilities that allow the characterisation and scientific investigations to be undertaken that can then be correlated with Raytheon UK's industrial scale fabrication fa-

cilities in order to optimise the device characteristics. The investigation is also of significant benefit to Newcastle University as it allows access to a large device sample size for investigation and also provides an opportunity to gain an insight into the impact of the commercial fabrication process on device performance.

1.3 Thesis outline

The main objective of this study is to gain an in depth understanding of the impact of process variations in both 4H-SiC Ohmic contacts and dielectrics that are employed in 4H-SiC CMOS devices in order to facilitate performance and stability improvements in devices such as the MOSFET used in integrated circuits. This study is therefore divided into several chapters:

Chapter 2: A review of 4H-SiC CMOS for high temperature applications

This investigation begins with a detailed overview of the current status of 4H-SiC MOSFET technology given in chapter 2. This includes an overview of SiC CMOS technology for high temperature applications; key issues and challenges in the technology; and the future potential of 4H-SiC CMOS. The key issues and challenges that are discussed include the material and epitaxial growth, dopant incorporation, oxide growth and Ohmic contact formation as well as device operating concerns such as oxide reliability, reduced channel mobility and threshold voltage instability.

Chapter 3: Analysis of Ohmic metal contacts on n and p-type 4H-SiC

The first technical investigation of this thesis is discussed in chapter 3. This involves a study into the performance of the Ohmic contacts that have been employed on both the n and p-type 4H-SiC structures that are analysed throughout this thesis. This investigation involves both electrical and physical characterisation across a large temperature range of the contacts including current-voltage measurements on two-terminal resistor structures, four-terminal cross-bridge Kelvin resistor structures and four-terminal van der Pauw structures as well as atomic force microscopy (AFM) in order to extract the resistance, specific contact resistance, sheet resistance and surface morphology of the contact metallisation samples. The results are then compared to published performance characteristics of comparable 4H-SiC Ohmic contacts and a discussion is presented into ways in which the processing and the performance of the contacts could be improved.

Chapter 4: Impact of dielectric formation and processing on the operation of 4H-SiC MIS structures

The next study that is discussed in this thesis is presented in chapter 4 and is focussed on understanding the impact of dielectric formation and processing on the operation of 4H-SiC MIS capacitor structures. In this investigation 3 gate dielectrics on both n and p-type 4H-SiC that have undergone differing process treatments are examined using electrical characterisation of MIS capacitor structures that were fabricated monolithically with the MOSFET devices that are discussed in chapter 5. This includes measurement of the capacitance-voltage and current-voltage characteristics between 298 K and 448 K in order to extract the temperature dependent flatband voltage (V_{FB}), oxide capacitance (C_i), oxide thickness (t_i), mobile oxide charge (Q_m), interface trapped charge (Q_{it}), fixed oxide charge (Q_f), oxide trapped charge (Q_{ot}) and the acceptor/donor concentration ($N_{A/D}$). The characteristics are then compared and a potential solution for a monolithic process for both n and p-type 4H-SiC MIS is discussed.

Chapter 5: Impact of dielectric formation and processing on the operation of 4H-SiC MOSFETs

The final technical investigation that is discussed in this thesis is in chapter 5 and is focussed on understanding the impact of dielectric formation and processing on the operation of 4H-SiC MOSFETs. This study involves the characterisation and analysis of the performance of the 3 dielectrics that were discussed in chapter 4 used in both n and p-channel 4H-SiC MOSFETs. This includes the measurement of the electrical characteristics of the devices between 298 K and 448 K in order to examine the variation in threshold voltage (V_{TH}), subthreshold slope (SS), interface trap density (D_{it}) and the field effect mobility (μ_{FE}) characteristics across the measured temperature range. This investigation also includes a comparison of the measured mobility characteristics to the modelled characteristics in order to understand the dominating mobility effects within the devices. An investigation is also conducted into the impact of the gate dielectric on the low frequency noise characteristics of the MOSFETs. Finally an investigation is conducted into the impact of a threshold voltage adjust ion implantation on the MOSFET characteristics for one of the studied dielectrics on n-channel MOSFETs with varying implantation doses.

Chapter 6: Conclusions and future work

In the final chapter (chapter 6), of this thesis the key findings from the technical investigations are summarised and future work and challenges are discussed.

1.4 Key contributions

The investigations that have been carried out within this thesis provide several key contributions to the research community including:

- Extraction of the temperature dependence of the interface trap density of both n and p-type 4H-SiC MIS capacitors with varying gate dielectrics treatments.
- Experimental measurement of the temperature dependence of the field effect mobility of both n and p-type 4H-SiC MOSFETs with varying gate dielectric treatments.
- Modelling of the mobility characteristics of both n and p-channel 4H-SiC MOSFETs with varying gate dielectric treatments.
- Low frequency noise analysis of both n and p-channel 4H-SiC MOSFETs with varying gate dielectrics.
- Analysis of the impact of threshold voltage adjust ion implantation on the performance of 4H-SiC MOSFETs with varying implantation doses.
- A comparison study of the performance of thermally grown SiO_2 and deposited SiO_2 as the gate dielectric in both n and p-channel 4H-SiC MOSFETs.
- Analysis of Ohmic metal contacts on both n and p-type 4H-SiC including the current transport mechanisms of each.

Chapter 2

A review of 4H-SiC CMOS for high temperature applications

2.1 Introduction

In recent years it has become increasingly apparent that there is a large demand for resilient electronics that can operate within environments that standard silicon electronics cease to function such as high power and high voltage applications, high temperatures, corrosive ambients and environments exposed to radiation. This has become even more essential due to increased demands for sustainable energy production and the reduction in carbon emissions worldwide, which has put a large burden on a wide range of industrial sectors who now have a significant demand for electronics to meet these needs including; military, space, aerospace, automotive, energy and nuclear. Examples of where technology could be utilised to meet user demands include:

- The development of more efficient aero engines where electronic monitoring and control can be developed to operate in harsher areas of the engine.
- The transition from hydraulic to electric brakes where higher temperature capable power and control electronics can be co-located with the brake actuators.
- The development of electronics capable of withstanding $300\,^oC$ for the oil and gas industry as this will make accessing deep reserves economically viable whereas currently it is a problematic process. Currently state of the art drilling tools can only withstand $300\,^o$C.
- The development of circuitry capable of continuous operation at $300\,^oC$ is very desirable for geothermal explorations and plant operation.
- The need to increase fuel efficiency and lower emissions through lowering the weight of aircraft and new engine architectures. SiC technologies offer the potential of lightweight power through air-cooling.

Silicon carbide (SiC) technologies provide a viable solution to address all of the challenges outlined above. SiC is suited to high temperature operation and allows a significant reduction in the thermal management and heat-sinking requirements of electronics. In extreme environments, where ambient temperatures may well exceed the physical limit of silicon-based technologies, SiC based technology offers a lower cost and a smaller footprint solution for operation in such environments.

SiC is a wide band gap semiconductor with advantageous electrical properties such as a high breakdown electric field, high thermal conductivity and large saturation velocity [4]. High quality material on large area wafers (150 mm) is now commercially available, allowing the fabrication of reliable high temperature, high frequency and high current power electronic devices, improving the already optimised silicon based structures. An important advantage of SiC is that it is the only wide band gap compound semiconductor that can be thermally oxidised to grow insulating, high quality SiO_2 layers [5], which makes it an ideal candidate to replace silicon technologies for metal-oxide-semiconductor applications, which is the main focus of this research.

Although the technology has made a number of major steps forward over recent years and the commercial manufacturing process has advanced significantly, there still remains a number of issues that need to be overcome in order to fully realise the potential of the material for electronic applications. This chapter aims to act as an introduction into the key concepts of 4H-SiC MOS technology as well as outlining some of the major challenges that are facing and inhibiting the development of 4H-SiC CMOS. This includes examining process issues such as material and epitaxial growth, dopant incorporation, oxide growth and Ohmic contact formation as well as device operating concerns such as oxide reliability, threshold voltage instability and reduced channel mobility.

2.2 Overview of CMOS technology

The majority of the semiconductor industry exhibits rapid development due to the demand for faster, smaller and cheaper microprocessors. In 1965, the Intel co-founder Gordon Moore predicted that every 18 to 24 months the number of transistors that could fit into a new chip would double [8] and over the previous four decades this has proven true as shown in Figure 2.1 as the majority of the semiconductor industry has been almost entirely focussed on meeting this goal. However, the technology developed for this market does not provide a suitable solution for electronics, which can be utilised in more harsh environments. Standard silicon electronics cease to operate at temperatures over $175\,^oC$ and the most advanced silicon-on-insulator technologies cannot operate beyond $300\,^oC$ [9]. To provide suitable signal level devices for temperatures exceeding $300\,^oC$ an alternative solution is required. Sil-

icon carbide along with its material properties can provide a viable solution to meet this demand.

The market forecasts for silicon carbide power devices, integrated circuits and power modules are anticipated to be in excess of $100 million worldwide by 2020. As the only European based silicon carbide fabrication facility, Raytheon is seeking to address both the power device and harsh environment markets in silicon carbide. Raytheon Semiconductors aims to double its revenue in the next 8 years through its involvement in these markets. The material properties of silicon carbide support high efficiency power, electric vehicles and photovoltaics and will act as an enabler for the sustainable, green economy. Raytheon Semiconductors is currently leveraging its 10 year history in silicon carbide research and development to focus on two product lines; firstly offering silicon carbide to manufacturing services to power device OEMs. The second area of interest is the design and manufacture of silicon carbide integrated circuits, building on its existing proven Si CMOS experience, this market is expected to be worth $400 million in the next 5 years [7]. The main focus of the technologies in this project is for the development of silicon carbide integrated circuits through the development and optimisation of a 4H-SiC monolithic CMOS process for the fabrication and development of integrated circuits using the material.

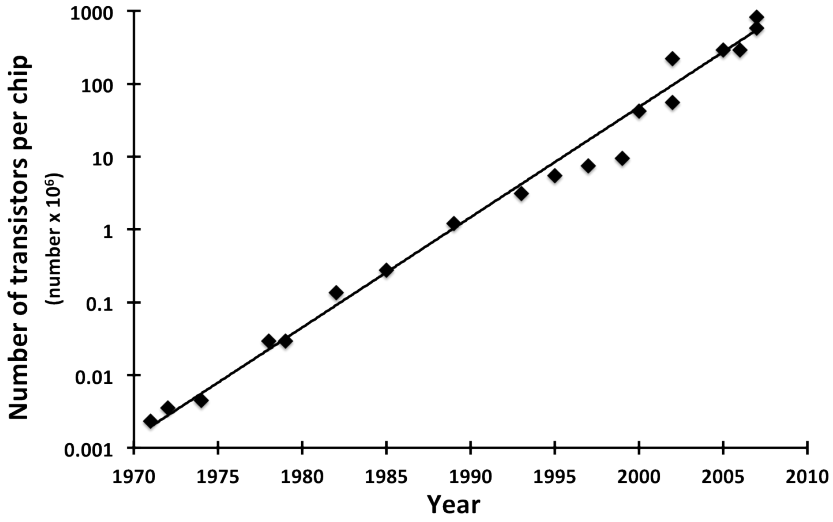


Figure 2.1: The number of transistors on each generation of Intel processors [10].

High temperature integrated circuits (ICs) are not a new project but due to the recent advances in material quality and wafer size of 4H-SiC the prospect of commercial SiC ICs is much more promising. Both NMOS [11] and CMOS [12] have been investigated in 6H-SiC at an early research stage, however, Raytheon UK are the first to explore commercial grade monolithic 4H-SiC CMOS for large scale manufacture [13].

2.3 SiC CMOS for high temperature applications

Due to the inherent material properties of SiC such as the low intrinsic carrier concentration, wide bandgap, native thermal oxide and the availability of high quality commercial 150 mm wafers, SiC is a prime candidate to become the market leader for electronics for high temperature and high power applications.

Silicon carbide comprises equal fractions of silicon and carbon atoms. Each silicon atom is surrounded by four neighbouring carbon atoms and four silicon atoms surround each carbon atom. Silicon carbide exists in many different structural formations, these differing structural formations are known as polytypes. Polytypes are described depending on their bonding structure and the pattern of atoms within them. The most commonly used polytypes within silicon carbide are hexagonal and cubic. They are known as the 4H, 6H and 3C polytypes with the H and C representing hexagonal and cubic, respectively, as shown in Figure 2.2.

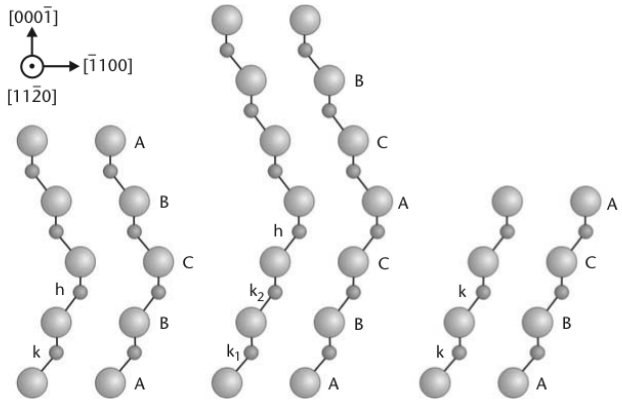


Figure 2.2: The three most common polytypes in SiC viewed in the [11$\bar{2}$0] plane. From left to right, 4H-SiC, 6H-SiC, and 3C-SiC; k and h denote stacking sequences that are cubic and hexagonal, respectively [14].

Each SiC polytype exhibits different electrical, optical and thermal properties due to the difference in the stacking sequence of the material lattice structure [15]. The variation in lattice structure of the polytypes results in varying characteristics including the electron mobility, bandgap energy, thermal conductivity and critical electric field as shown in Table 2.1.

Property	**Si**	**4H-SiC**	**6H-SiC**	**3C-SiC**	**C**	**GaN**
Bandgap, E_g (eV)	1.1	3.2	3.0	2.3	5.5	3.5
Electron mobility, μ_n, at $N_D = 10^{16}$ cm^{-3} (cm^{2}V^{-1}s^{-1})	1200	//c-axis: 800 $\perp$c-axis: 800	//c-axis: 60 $\perp$c-axis: 400	750	2200	1250
Hole mobility, μ_p, at $N_A = 10^{16}$ cm^{-3} (cm^{2}V^{-1}s^{-1})	420	115	90	40	850	850
Intrinsic carrier concentration, n_i (cm^{-3}) at 300 K	1.5×10^{10}	$\sim 10^{-7}$	$\sim 10^{-5}$	$\sim$10		$\sim 10^{-10}$
Breakdown field, $N_D = 10^{16}$ cm^{-3} (MVcm^{-1})	0.6	//c-axis: 3.0 $\perp$c-axis: 2.5	//c-axis: 3.2 $\perp$c-axis: $>$1	1.8	10	2
Thermal conductivity (Wcm^{-1}K^{-1})	1.5	3-5	3-5	3-5	22	1.3
Saturated electron velocity (10^7 cms^{-1})	1.0	2	2	2.5	2.7	2.2
Donor dopants and shallowest ionisation energy (meV)	P: 45 As: 54	N: 45 P: 80	N: 85 P: 80	N: 50	N: 1700 P: 520	Si: 15
Acceptor dopants and shallowest ionisation energy (meV)	B: 45	Al: 200 B: 300	Al: 200 B: 300	Al: 270	B: 370	Mg: 160

Table 2.1: Comparison of the material properties of Si, 4H-SiC, 6H-SiC, 3C-SiC, C and GaN at 300 K. Data compiled from references [1, 16, 17, 18, 19, 20, 21] and references therein. The defect concentration for the quouted shallow donor and acceptor levels was not given in the references.

A comparison of the materials properties of 4H-SiC along with other commonly used semiconductor materials including Si, 6H-SiC, 3C-SiC, C (diamond) and GaN is presented in Table 2.1. As shown in the table, diamond has the largest bandgap energy, electron and hole mobility, thermal conductivity and saturated electron velocity out of the examined materials at room temperature, which theoretically makes it the ideal choice for high temperature applications. However, in comparison to both GaN and 4H-SiC technology the development of diamond electronics is still in its infancy and coupled with the fact that diamond does not produce SiO_2 as its native oxide it would not be compatible with current Si CMOS processing techniques. Therefore, the technology is not suitable for current commercial applications or widespread semiconductor processing capabilities.

GaN exhibits the second largest bandgap energy, electron and hole mobility and a low intrinsic carrier concentration at room temperature, which would theoretically make it an ideal choice for high temperture applications behind diamond. However, the relatively poor thermal conductivity of GaN makes heat management for GaN devices a challenge and GaN material quailty is currently less advanced than 4H-SiC material quality. 4H-SiC is also often utilised in preference to GaN as SiC devices can be fabricated in a way that is analogous to silicon in that a SiC epitaxial layer is formed on SiC substrate. The result is a good crystallographic match between the epitaxy and substrate and an electrically conductive path from the top to the bottom of the wafer. Production processes for epitaxy ready GaN sustrates of high quality are still in the early stages and are much less mature than 4H-SiC.

4H-SiC devices fit very well into the markets and applications that are already widespread across the semiconductor industry due to its compatability with many Si processing techniques. This, therefore, means that SiC technologies require a lower upfront investment than some of the other high temperature material solutions and the path to profitable growth for many companies is therefore shorter with SiC than GaN.

Several figures of merit also highlight the beneficial uses of 4H-SiC including Baliga's, Keyes' and Johnson's figures of merit. In each case a higher value equates to a more desirable material for a particular application and Si has been used as the reference technology to demonstrate the improvements that can be gained by replacing Si devices with 4H-SiC devices in the future. Baliga's figure of merit (BFM) defines the material parameters to minimise the conduction loss in low-frequency unipolar transistors and, therefore, defines the performance of a material for high voltage unipolar device applications [22]. This can be calculated using Equation 2.1,

$$BFM = \varepsilon_s \mu E_g^3 \tag{2.1}$$

where ε_s is the dielectric constant, μ is the mobility and E_g is the bandgap energy of

the semiconductor. SiC has the largest BFM out of the materials compared as SiC shows the highest breakdown field and saturated electron velocity in Table 2.1. A comparison of material figures of merit shows that 4H-SiC has a BFM of 290 times that of Si [23].

Keyes' figure of merit (KFM) outlines the potential of a device for high power and high voltage applications [24]. KFM can be calculated using Equation 2.2,

$$KFM = k\sqrt{\frac{cv_s}{4\pi\varepsilon_s}} \tag{2.2}$$

where k is the thermal conductivity, c is the velocity of light and v_s is the saturated electron velocity. A comparison of material figures of merit shows that 4H-SiC has a KFM of 5.1 times that of Si [23].

Johnson's figure of merit (JFM) addresses the potential of a material for high frequency and high power applications and can be calculated using Equation 2.3[25],

$$JFM = \frac{(E_B^2 v_s^2)}{4\pi^2} \tag{2.3}$$

where E_B is the critical electric field for breakdown. A comparison of material figures of merit shows that 4H-SiC has a JFM of 410 times that of Si [23].

N-type 4H-SiC has a substantially higher carrier mobility and shallower dopant ionisation energies compared to 6H-SiC, making it the polytype of choice for electronic devices provided that all other device processing, performance and cost related issues are comparable for both polytypes [19]. 4H-SiC unlike 6H-SiC does not exhibit electron mobility anisotropy as shown in Table 2.1, which also makes it ideal for vertical power device applications [15]. Also, specifically for high temperature applications, the wider bandgap and lower intrinsic carrier concentration of 4H-SiC, as shown in Table 2.1 theoretically permits device operation to higher temperatures than the 6H polytype. A plot of the theoretical temperature dependence of bandgap energy and intrinsic carrier concentration for 4H-SiC is shown in Figure 2.3.

4H-SiC is the polytype of choice for electronic devices as it has the widest bandgap of the SiC polytypes and a bulk electron mobility of 800 cm^2/Vs, which is double the mobility of the 6H polytype so has a much greater potential for electronic applications [26]. This high bulk electron mobility combined with the wide bandgap, and high breakdown field, makes this polytype ideal for high temperature, high frequency and high power applications. However due to the high interface trap density at the 4H-SiC/SiO_2 interface dramatically reducing the channel mobility of 4H-SiC MOSFETs, the true potential of the material within MOSFET applications is yet to be realised.

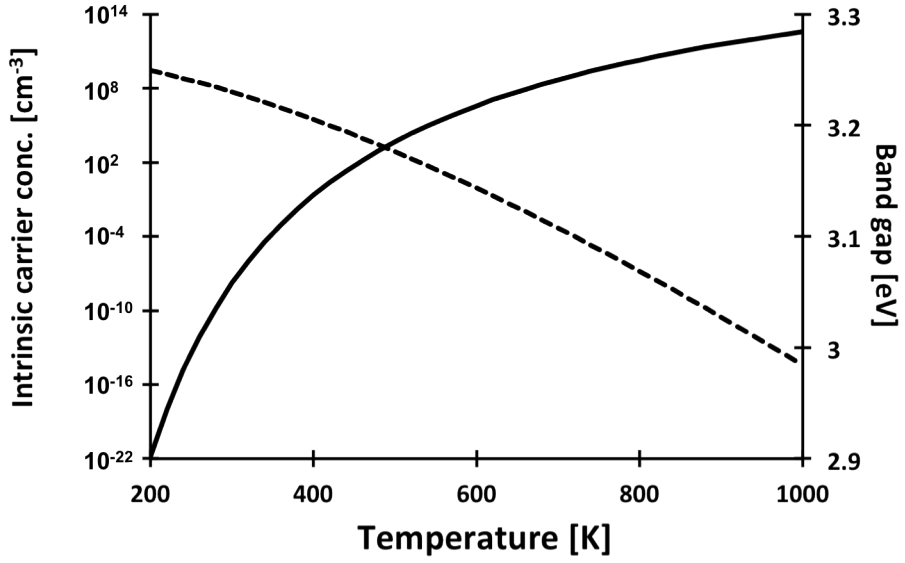


Figure 2.3: Variation of intrinsic carrier concentration (solid line) and bandgap (dashed line) with temperature in 4H-SiC.

The development of the 4H-SiC CMOS devices in this project will directly enable high temperature ($> 300\,^{o}$C) signal-level devices but will also have an impact on other commercial markets as the developed process is transferrable and can be implemented to the fabrication of 4H-SiC integrated high power switching devices and RF devices.

2.4 Key issues and challenges within the technology

As the manufacturing technology of 4H-SiC electronics applications is still in its infancy a number of material and device level issues, which inhibit rapid progress in the commercialisation of semiconductor devices, remain. The main issues and recent advances are discussed in the following sections, with a particular focus on the issues and challenges within the technology that directly impact on the fabrication and operation of 4H-SiC MOSFETs.

2.4.1 *Current status of 4H-SiC material quality*

The seeded sublimation growth method, also known as the modified Lely process, which was first implemented in 1978 by Tairov and Tsvetkov [27], is the favoured technique for industrial volume production of silicon carbide wafers. This process is almost exclusively used for the production of silicon carbide, however, control of the process is very complex and can lead to large number of defects within the wafers, particularly device yield limiting defects such as micropipes [28]. Micropipes are hollow core defects that can be caused by inclusions and screw dislocations [29], with typical diameters of 1-10 μm [30]. Therefore,

much effort has been put into improving the process and enhancing wafer quality over the past several decades in order to make the technology suitable for commercial device production.

The seeded sublimation growth method involves a graphite crucible surrounded by a water-cooled quartz reactor enclosure. The crucible has a diameter slightly larger than the wafer that is to be grown in the crucible and is partially filled with SiC powder. A seed is attached to the lid of the crucible. The distance between the seed and the SiC source is typically between 1 and 20 mm. The crucible is heated up to temperatures of around 2000 ^{o}C, which is when SiC begins to sublime [14] to produce vapour constituents of Si, Si_2 and SiC_2. A thermal gradient is created so that the seed is slightly colder than the powder source so that material will transport from the source and condense on the seed to form SiC. Growth rate is very dependent on temperature distribution, pressure and source to seed distance [31] so slight variations in any of these factors can have a large impact on the wafers that are produced. For example, 4H-SiC grows at relatively low temperatures and pressures, whilst 6H-SiC is preferably grown at higher temperatures and pressures [32]. Also the face of the seed crystal is very important in determining the polytype of SiC, which will be produced [33].

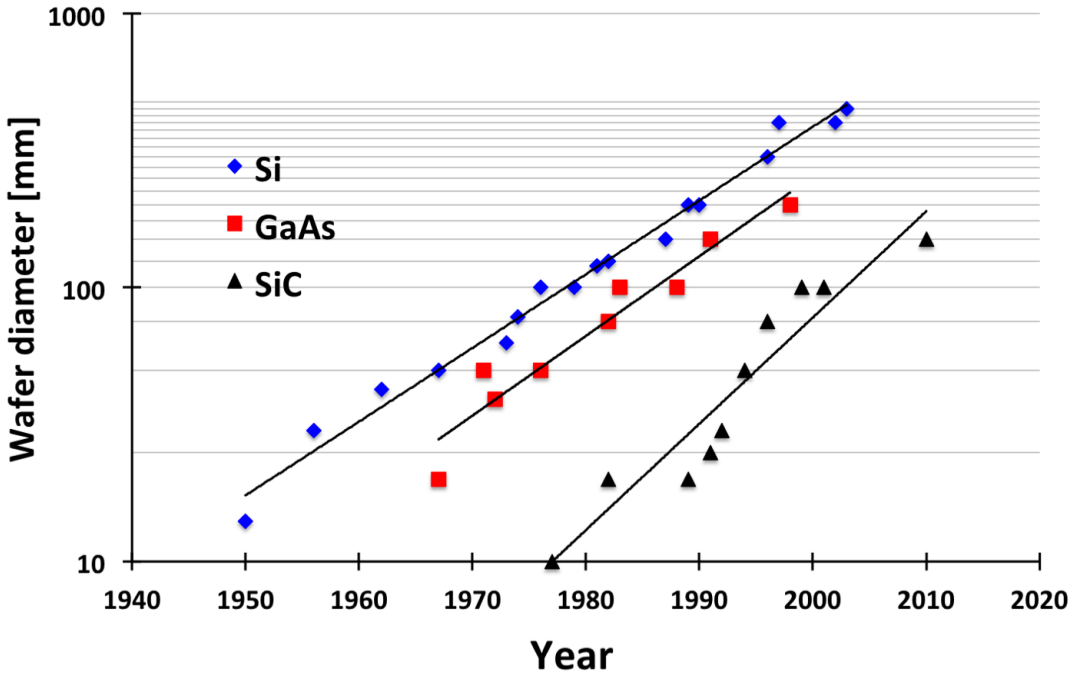


Figure 2.4: The history of wafer diameter progression of SiC [34] [35] compared to Si [36] [37] [38] and GaAs [34] [39] grown by the Czochralski method. Two data points at the same diameter indicate the first published demonstration followed by a wider spread technology adaptation for commercial production. Note for SiC: first demonstration of 100 mm 6H-SiC in 1999, first demonstration of 100 mm 4H-SiC in 2001 [40].

Figure 2.4 shows the SiC wafer diameter progression as a comparison of the equivalent historical progress of silicon (Si) and gallium arsenide (GaAs) grown from the melt by the Czochralski method. This shows that great advances have been undertaken in the last

30 years and, if current trend continues, 500 mm SiC wafers could potentially be available for commercial device production by 2020. Alongside this it can also be seen in Figure 2.5 that in recent years the median micropipe density (MPD) has dramatically reduced due to advances in the manufacturing techniques of SiC wafers. As of January 2011 the median MPD has stabilised at less than 0.1 cm^{-2} for both 76 mm and 100 mm n-type 4H-SiC wafers, which suggests that larger wafers that are produced in the future will also have a low density of defects if progression continues at its current rate. Cree have produced zero micropipe 100 mm 4H-SiC wafers since 2008 [41] and Dow Corning have demonstrated micropipe free material over a full 100 mm diameter, which has been confirmed by Synchrotron White Beam X-ray Topography (SWBXRT), and 150 mm wafers have been demonstrated with micropipe densities of less than 1 cm^{-2} [40]. Since 2012, commercial standard 150 mm 4H-SiC wafers with epitaxial layers of up to 100 μm have been available with reported median micropipe densities of less than 0.1 cm^{-2} [42], which help meet the defect requirements for commercial power device production.

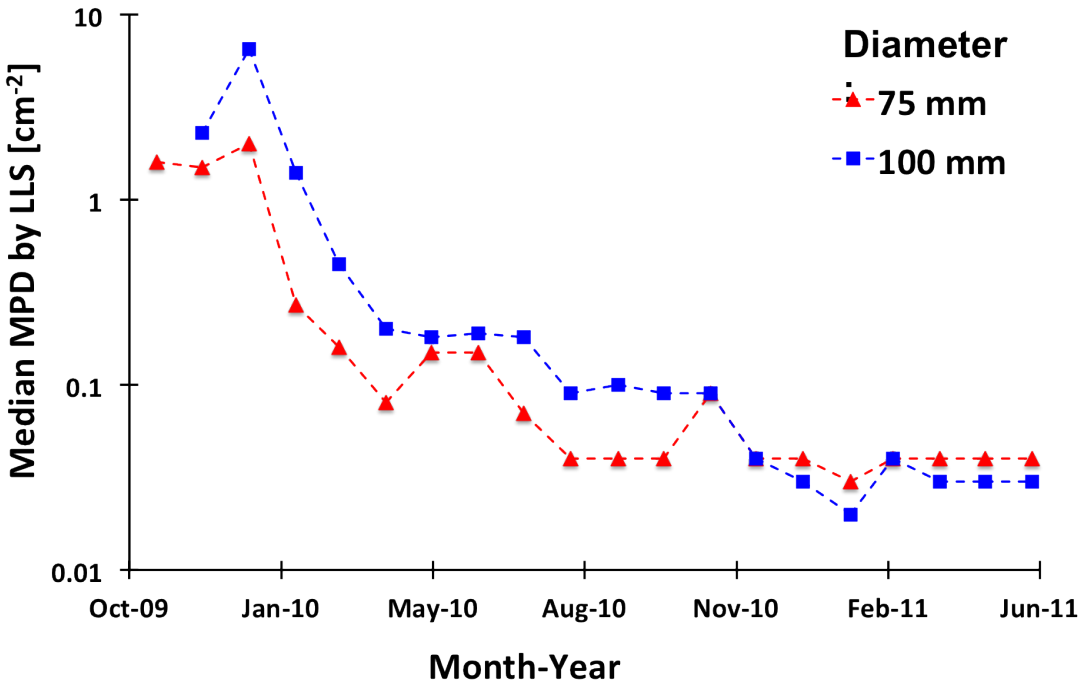


Figure 2.5: Median micropipe densities in Dow Corning 76 mm and 100 mm n-type 4H-SiC production wafer vs time [40].

The dramatic reduction in micropipe density that has been witnessed over the last 3 years, as shown in Figure 2.5, is due to optimisation of the seeded sublimation growth method. This has been implemented by precise control of heat and mass transfer conditions during growth and by implementing modelling techniques to numerically simulate the impact that changing conditions will have on material growth. As micropipe densities are now sufficiently low enough to not limit device yield, significant effort is now being put into reducing elementary dislocations in SiC such as the 1c-screw and basal plane dislocations, which are known

to cause device operation limiting issues in p-n diodes [43] and bipolar devices [44], respectively. Another enhancement to wafer technology that has been undertaken is the optimisation of the epitaxy process to consistently produce surface roughnesses, on 4^{o} off-axis wafers, of less than 1 nm as determined by atomic force microscopy (AFM) measurements [40].

2.4.2 *Epitaxial growth quality and issues*

Most electronic devices are fabricated in epitaxial SiC layers rather than directly in sublimation-grown wafers due to the superior electrical properties, including dopant incorporation, and higher crystal quality than is provided by bulk wafers. Therefore, the quality of 4H-SiC epitaxial layers is of great importance in the development of electronic devices using the material.

There has been a great deal of research into growth methodologies of SiC epitaxial layers including molecular beam epitaxy, liquid-phase epitaxy and chemical vapour deposition (CVD) [45][46]. However, CVD is the most commonly used technique for commercial production at it provides a high degree of epilayer reproducibility, quality and throughputs, which are all of fundamental importance for mass production. SiC CVD involves heating SiC substrates in a reactor (chamber) with flowing silicon and carbon containing gases that decompose and deposit Si and C on to the wafer allowing an epilayer to grow in a well ordered single-crystal structure. By modifying the growth conditions such as, silicon and carbon source gas flows, temperature, pressure and reaction chemistries the growth conditions can be optimised to control doping uniformity, thickness uniformity and morphological defects. Growth temperatures between $1400\,^{o}$C and $1600\,^{o}$C at pressures from 0.1 to 1 atm result in growth rates of approximately a few micrometres per hour [45] but growth environments using higher temperature (up to $2000\,^{o}$C) and halide based growth chemistries produce epilayer growth rates in the order of hundreds of micrometres per hour which is very beneficial for thicker epitaxial layers which are a requirement of high voltage power device designs [47][48][49].

In situ doping is carried out during CVD epitaxial growth and is achieved through the introduction of nitrogen (N_2) for n-type and aluminium (trimethyl- or triethylaluminium) for p-type epilayers during the growth process. Variations in epilayer doping can be achieved by controlling the flow of gases or alternatively through the site-competition doping methodology, which has enabled a broader range and a more repeatable and reliable SiC epilayer doping process to be achieved [50]. The methodology relies on the fact that dopants of SiC preferentially incorporate into Si or C lattice sites. For example nitrogen preferentially incorporates in to sites that are normally occupied by carbon whilst aluminium prefers the Si lattice site of SiC. By varying the ratio of Si and C during the CVD growth the incorporation

of dopants can be increased or reduced to achieve the required doping concentration of the material. The surface orientation of the wafer can also impact on the efficiency of dopant incorporation during CVD growth [51].

Due to the optimisation of the CVD epitaxial growth process SiC epilayer doping ranging from 9×10^{14} to 1×0^{19} cm^{-3} on commercial wafers is currently available with tolerances of $\pm25\%$ and $\pm50\%$ for n and p-type, respectively [42]. Epitaxial layers on the (0001) silicon face are available with a thickness ranging from 0.2 to 50 μm with a tolerance of $\pm10\%$ for both n and p-type epilayers [42].

If growth conditions are not properly controlled and SiC surfaces are inadequately prepared, such as surfaces that are polished to within 1^o of the (0001) basal plane, growth adatoms island nucleate and bond in the middle of terraces instead of at the steps. Uncontrolled terrace nucleation on SiC surfaces can lead to heteroepitaxial growth of poor-quality 3C -SiC [52][53]. To prevent terrace nucleation of 3C-SiC during epitaxial growth most commercial 4H and 6H substrates are polished to tilt angles of 8^o and 4^o off the (0001) basal plane. Most commercial SiC electronics rely on homoepitaxial layers that are grown on off axis (0001) c-axis SiC wafers.

Crystal defect	**Comments**
Micropipe (Hollow-core axial screw dislocation	Known to cause severe reduction in power device breakdown voltage and increase in off-state leakage
Closed-core axial screw disclocation	Known to cause a reduction in device breakdown voltage, increase in leakage current and a reduction in carrier lifetime
Basal plane dislocation	Known nucleation source of expanding stacking faults leading to bipolar power device degradation and a reduction in carrier lifetime.
Threading-edge dislocation	Impact not well known
Stacking faults (disruption of stacking sequence)	Faults known to degrade bipolar power device and reduce carrier lifetimes
Carrot defects	Known to cause a severe reduction in power device breakdown voltage and increase in off-state leakage
Low-angle grain boundaries	Usually more dense near the edges of wafers and the impact is not well known

Table 2.2: Major types of crystal defects reported in SiC wafers and epilayers [19].

To obtain SiC epilayers with minimal dislocation defects it is essential that the wafer is processed to remove residual surface contamination and defects left over from wafer cutting and polishing. Techniques that have been implemented to achieve this include dry etching,

chemical mechanical polishing (CMP)[54] and a pre-growth gaseous etch, which is carried out at high temperature using H_2 and/or HCl, to further eliminate surface contamination and defects [55][56].

A summary of the major types of extended crystal defects that have been reported in SiC wafers and epilayers is given in Table 2.2 along with a description of the impact that the defects can have on electronic devices.

2.4.3 *Selective doping techniques*

Conventional dopant diffusion, which is widely used in the manufacture of silicon microelectronics, is unsuitable for most doping processes in SiC technology as the diffusion coefficients of most SiC dopants are negligibly small at temperatures $< 1800\,^{o}$C. This is a very useful characteristic in maintaining device junction stability but makes the doping process significantly more complex.

Ion implantation has advantages over other doping techniques as all stable elements of the periodic table can be implanted and lateral structuring and doping selected areas is possible through masking techniques. To tailor the electrical properties of device areas, the knowledge of lateral and depth distribution as well as the electrical properties of impurities and defects are important issues. Ion implantation in SiC crystals is not different from the one commonly used in other semiconductor processing. The difference is in the process for dopant activation and re-crystallisation, which requires a much higher thermal budget than that of silicon processing in order to achieve acceptable dopant implant electrical activation.

Shallow acceptor species	**Ionisation energy of the acceptor, ΔE_A (meV)**
Aluminium	200
Boron	285

(a) Ionisation energies of shallow acceptor impurities in 4H-SiC.

Shallow donor species	**Ionisation energy of the hexagonal donor, ΔE_{Dh} (meV)**	**Ionisation energy of the cubic donor, ΔE_{Dk} (meV)**
Nitrogen	50	92
Phosphorus	53	93

(b) Ionisation energies of shallow donor impurities in 4H-SiC. Two ionisation energies are given for donor impurities, representing electrically observed hexagonal and cubic lattice sites.

Table 2.3: Ionisation energies of shallow acceptor and donor impurities in 4H-SiC [6]. The site at which the impurity lies (i.e. Si or C site) was not provided in the reference.

Ion implantation in SiC is generally carried out at temperatures ranging from room temperature to $800\,^{o}$C as elevated temperatures act to promote lattice self-healing during the implant to reduce damage and the segregation of carbon and silicon atoms, which can be-

come excessive in the high dose implants used for Ohmic contact regions. Doping is carried out on selected areas through masking techniques and lateral structuring is avoided with wet and dry etching. The masking can be done on either deposited metals with a high mass (e.g. gold) or thermally grown or deposited silicon dioxide. Masking films must be thicker than the maximum travelling distance of the implanted ions in the film and depend on the applied acceleration energies. The mask should not consist of element species that are dopants or recombination centres (crystal lattice imperfection or impurity whose energy level is situated in the forbidden band of the semiconductor and which enables conduction electrons and holes to recombine) in SiC. Patterning of the mask is carried out by common lithography techniques.

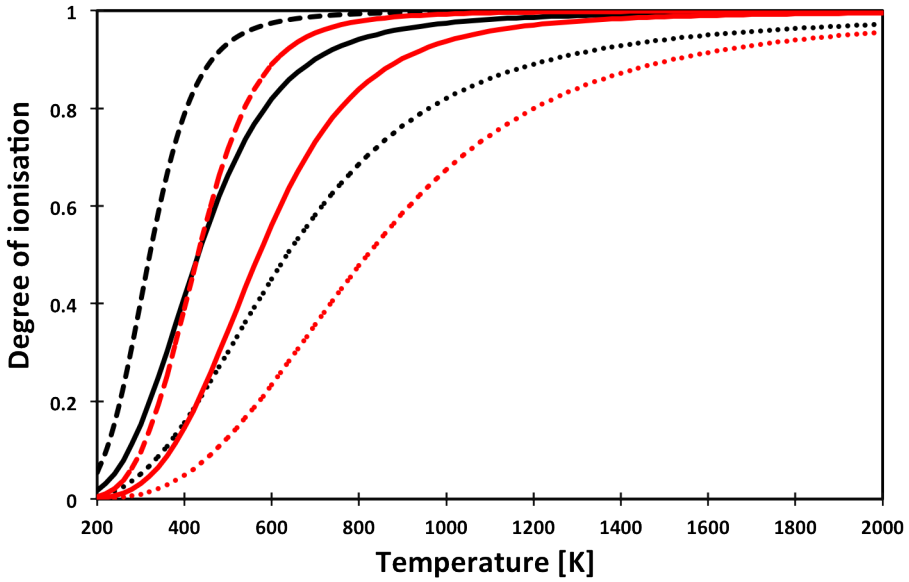


Figure 2.6: Ionization degree of acceptors Al (black) and B (red) in 4H-SiC as a function of temperature at different doping concentrations. $N_A = 10^{16}\,cm^{-3}$ (dashed lines), $N_A = 10^{17}\,cm^{-3}$ (solid lines), $N_A = 10^{18}\,cm^{-3}$ (dotted lines). Arrow indicates the direction of increasing acceptor concentration.

After implantation the mask is removed and high temperature annealing (approximately 1200 to 1800 ^oC) is applied to activate the dopants and remove the irradiation-induced damage. The anneal is essential so that the maximum electrical activation of the dopants is achieved from ion implanted layers but can, however, act to seriously degrade the SiC surface morphology [57][58]. Research strongly suggests that the electrical properties and defect structure of 4H-SiC doped by ion implantation and annealing is generally inferior to that of SiC doped during epitaxial growth [59][60]. The reduced crystal quality due to ion implantation has been observed to degrade carrier mobilities and minority carrier lifetimes, which can cause severe degradation to electrical device performance [61][62]. Some techniques employed to reduce surface degradation during the high temperature anneal include annealing in silicon overpressures, which are achieved by annealing in a silane (SiH_4)-containing atmosphere [63], and the use of robust capping layers such as AlN and graphite used during the anneal have proven effective at preserving the SiC surface morphology [64][65][66].

The most commonly used dopants in 4H-SiC are nitrogen and phosphorus as donor impurities and boron and aluminium as acceptor impurities. Table 2.3 shows the dopant activation energies for shallow donor and acceptor impurities in 4H-SiC and Figure 2.6 and Figure 2.7 show the degree of ionisation for acceptor and donor dopants, respectively, as a function of temperature. The donor energy level arises from the potential, which is the sum of the host and the impurity potentials. Donor potentials in SiC vary dramatically between polytypes as they are a product of the band structure, in particular the location of the conduction band edge and the effective electron mass (m^*). Donors in 4H-SiC have 2 energy levels - a shallower level attributed to the impurity residing on the hexagonal lattice site and a deeper level attributed to the impurity of the cubic lattice site. N preferentially occupies carbon lattice sites and P occupies silicon lattice sites. Aluminium is the most commonly used p-type dopant in 4H-SiC epitaxial layers as it has a substantially higher degree of ionisation than boron at room temperature, as shown in Figure 2.6, however, for ion implantation boron is preferential as it is smaller so a deeper implant can be achieved, which will also create less damage in the implanted layer.

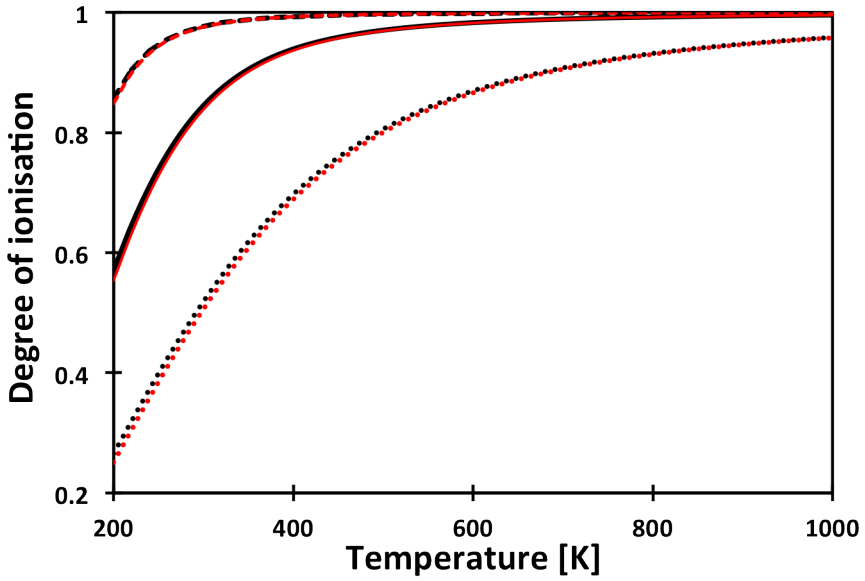


Figure 2.7: Ionization degree of donors N (black) and P (red) in 4H-SiC as a function of temperature at different doping concentrations. $N_D = 10^{16}$ cm^{-3} (dashed lines), $N_D = 10^{17}$ cm^{-3} (solid lines), $N_D = 10^{18}$ cm^{-3} (dotted lines) . Arrow indicates the direction of increasing donor concentration.

2.4.4 *Ohmic contacts to 4H-SiC*

The wide bandgap of 4H-SiC results in increased Schottky barriers, which is advantageous for fabricating Schottky diodes for power applications such as the devices that are currently commercially available [67], but not for making low resistance Ohmic contacts. Therefore, a major factor that has hindered advances within the development of SiC devices is the for-

mation of Ohmic contacts on both n and p-type SiC. Over the past few decades this has been a key area of research and great advances have been achieved, particularly with contacts on n-type 4H-SiC. For example, Ohmic contacts formed on n-type 4H-SiC using a combination of tungsten and nickel have recently been demonstrated that performed successfully for 15 hours at 1000 ^{o}C in an argon environment [68].

A wide variety of materials and processing techniques have previously been used to form Ohmic contacts on 4H-SiC and a variation of techniques have been employed for n and p-type 4H-SiC [69]. Several materials have been reported to form Ohmic contacts to 4H-SiC including titanium/tungsten alloys [70], titanium carbide [70], nickel [71], palladium [71], nichrome (80/20 weight precent Ni/Cr)[72] and various metal stacks [73] such as Au/Ti/Al [74], Si/Pt [75] and Ti/Al [76]. Specific contact resistivity ranges from 10^{-3} to 10^{-7} Ω.cm^2 and the lowest resistance contacts are usually formed on highly or degenerately doped material (particularly for p-type 4H-SiC) and require a high temperature annealing process at temperatures of around 1000 ^{o}C after metallisation.

Metals that form carbides are the most beneficial for Ohmic contact formation to 4H-SiC as they will eliminate the possibility of carbon clustering and the formation of carbon interstitials at the interface during high temperature annealing, which has been reported to occur in Ni silicide contacts to 4H-SiC [77]. Carbon interstitials act to increase the specific contact resistance and affect both the physical and electrical stability of the contacts. It is, therefore, beneficial to deposit a thin layer of a carbide forming metal such as titanium at the 4H-SiC interface so that during the high temperature annealing process this will react to form titanium carbide and reduce the density of carbon interstitials present in the contact [78].

As previously noted, substrate doping concentration has a significant impact on the contact resistivity of 4H-SiC Ohmic contacts with the lowest resistivities being reported for highly doped substrates [79] [80] [81]. However, the ion implantation process used for selectively doping 4H-SiC can act to modify the surface morphology of the semiconductor, which can then have a detrimental effect on the contact metallisation. A high temperature post-implantation anneal is required after ion implantation to promote the electrical activation of the dopants in substitutional lattice sites [61] [82]. Temperatures of up to 1500 ^{o}C [83] [84] and 1800 ^{o}C [79] are used for N and P n-type and Al p-type doping, respectively, which can have a detrimental effect on the surface morphology of the substrate. The increased surface roughness of the 4H-SiC substrate has been shown to increase the surface roughness and the contact resistance of the contact metallisation that is then deposited [79]. The use of carbon capping layers during the post-implantation anneal can act to improve the 4H-SiC surface morphology and, therefore, improve the contact characteristics [85] [86] [79].

The post deposition annealing conditions also have a significant impact on the contact resistivity and previous studies have shown that there is a substantial change in microstructure

during the annealing process, which is due to a solid state reaction during the annealing process and is largely dependent on the complexity of the metallisation stack that is deposited. However, the major trend is that increasing annealing temperatures can significantly reduce the specific contact resistance[71].

The thermal stability of Ohmic contacts is essential for high temperature devices, therefore, it is crucial that contacts have a high resistance to oxidation, have sufficient electrical conductivity and have appropriate interfacial electrical properties such as the contact resistance and Schottky barrier height to remain stable during high temperature operation. Ohmic contact structures typically consist of multiple metal layers in order to meet all of these requirements, which can introduce thermodynamic instabilities to the system and can lead to contact degradation through mechanisms such as electromigration, oxidation, and other electromechanical reactions in the presence of oxygen [87]. To overcome some of these issues capping and passivation layers such as WC/W have been used to prevent oxidation of the underlying metal layers and it has been shown that dramatic increases in the contact and sheet resistance values for increased annealing times directly correlated to metallurgical reactions and oxidation [88]. Diffusion barriers have also been investigated such as TiN [89] but only showed success in preventing oxidation in vacuum conditions. The investigations performed in air at elevated temperatures showed severe electrical degradation [90]. Aluminium overlayers have been demonstrated that act to prevent oxidation [91] and there have been many investigations into the formation of stable silicides that are less prone to oxidation at elevated temperature in air [73] [90] [92]. However, all of the different compositions investigated exhibited oxidation and severe degradation after 45-70 hour annealing periods with the most promising technique showing severe degradation after 250 hours [73].

The most significant recent advances for 4H-SiC Ohmic contacts for long term stability for high temperature applications include:

- the demonstration of SiC Ohmic contacts that withstand heat soaking under no electric bias at 500-600 ^{o}C for hundred or thousands of hours in non-oxidising gas or vacuum environments [93].
- the successful long term electrical operation of n-type Ohmic contacts with specific contact resistivity in the range $10^{-5}\,\Omega.\text{cm}^2$ in oxidising air ambients at temperatures between 500 and 600 ^{o}C have been demonstrated in low current density devices [94][95].
- Ohmic contacts formed on n-type 4H-SiC using a combination of tungsten and nickel have recently been demonstrated that performed successfully for 15 hours at 1000 ^{o}C in an argon environment [68]

For high temperature and other demanding applications there still remains a need for significant advancement within 4H-SiC Ohmic contact technology in order to fully realise

the potential of SiC electronics. Although there has been demonstration of long term stable n-type contacts at 600 ^{o}C [94] in air there is yet to be an equivalent demonstration of p-type technology. The durability and reliability of SiC Ohmic contacts is one of the critical factors limiting the practical high-temperature limits of SiC electronics. The main area that still requires significant progress is the realisation of Ohmic contacts to 4H-SiC that show long term temperature stability and can withstand electrical bias in an oxidising air environment at temperatures beyond 300 ^{o}C.

2.4.5 *Oxide growth and deposition on 4H-SiC*

One of the major advantages of SiC is that it forms a thermal SiO_2 when it is heated in the presence of oxygen. This means that theoretically the technology is compatible with the successful silicon VLSI (very large scale integration) technology that utilises inversion channel MOSFET based electronics as well as discrete silicon power devices [19], which will make the manufacturing process compatible with current silicon fabrication facilities.

This means that the most attractive method of oxide formation in 4H-SiC electronic is thermal growth of SiO_2. This is conventionally performed using either wet (H_2O) or dry (O_2) oxidation in a diffusion furnace. However, a major factor which has hindered progress within the technology is the high level of interface traps present at the 4H-SiC/SiO_2 interface in the 4H-SiC MOS system, which acts to reduce the inversion channel mobility in 4H-SiC MOSFETs. In order, to overcome this issue gate oxides on SiC are alternatively grown in nitric oxide (NO) or nitrous oxide (N_2O) as growth in these environments has been shown to reduce the density of interface states in comparison to gate oxides grown in the conventional way [96] [97] [98].

Thermal oxidation, the technique used to grow SiO_2 layers on SiC, results in the formation of a defective interface with a large density of interface traps (D_{it}) located within the SiC bandgap. The defects scatter and trap inversion channel carriers, resulting in very low channel mobilities in 4H-SiC MOSFETs. D_{it} varies across the bandgap and is particularly high close to the conduction and valence band edges. A suggested cause of the high density of interface states at the SiC/SiO_2 interface is the near interface traps (NITs), which due to the bandgap of 4H-SiC of 3.26 eV are located within the bandgap [99] [100] [101]. Near interface traps are considered to be native oxide defects that lie approximately 2.8 eV below the conduction band edge of SiO_2 [99]. Their energy level is considered to be within the bandgap close to the conduction band edge of 4H-SiC allowing substantial trapping of electrons whereas within the other polytypes with their lower bandgap energies, 3 eV for 6H-SiC, the near interface traps are less problematic as they are within the conduction band so do not affect carrier mobility in the inversion layer [99] [100] [101] [102]. The acceptor states

that are located at 2.8 eV below the SiO_2 conduction band edge have been observed using photon-emission electron tunnelling in oxides both on Si and SiC [99] so are a consistent issue for both technologies. However in Si as it has a much lower bandgap they are much less problematic as they are located significantly above the conduction band minimum.

Recent studies have presented that silicon interstitials or carbon dimers are a possible origin of the NITs [103] as well as the acceptor states that are located at 2.8 eV below the conduction band of SiO_2. The majority of issues witnessed in SiC MOS devices that do not fit with the trend of issues found at the Si/SiO_2 interface are believed to be due to the presence of carbon at the interface.

The cause of the high density of interface states is not completely understood and it is unknown as to whether they are intrinsic defects to the SiC/SiO_2 interface or are caused by a non-optimised thermal oxidation process [104]. Experimental methods have been explored to improve the interface trap density, including different post-oxidation annealing methods used to passivate defects such as post-oxidation annealing in hydrogen or nitrogen, or more recently the use of sodium or phosphorus in the oxidation process.

It was very quickly established that the treatments that were proven to improve D_{it} within silicon MOS did not have the same effect when used to improve the SiC/SiO_2 interface. A very successful method for silicon was post-oxidation annealing in hydrogen gas (H_2), however this method did not have an effective impact on D_{it} for SiC MOS [105]. The most dominant Si/SiO_2 interface defects are dangling bonds of silicon atoms that are back bonded to another three substrate Si atoms [106] [107]. Dangling bonds of Si at the surface are easily passivated by molecular hydrogen at 230 to 260 ^oC and become electrically inactive [108].

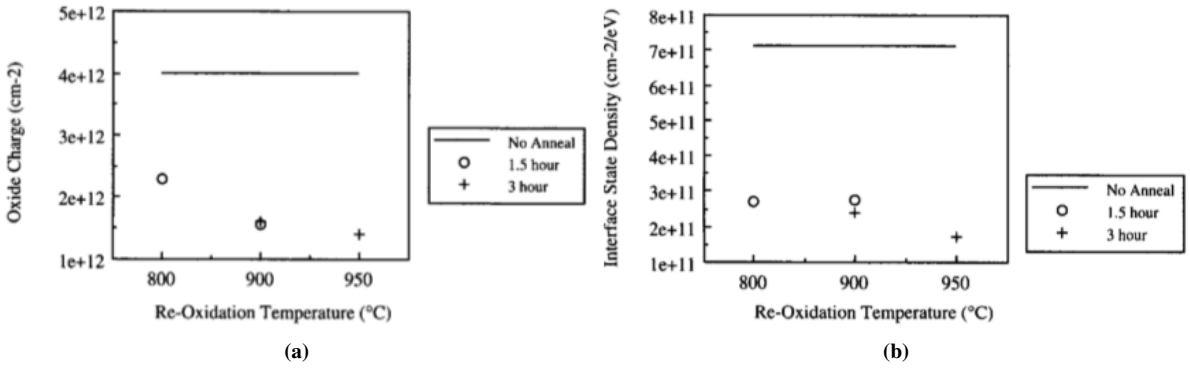


Figure 2.8: Comparison of net oxide charge densities (a) and interface trap densities (b) on oxides grown at 1100 ^oC then re-oxidised at 800, 900 or 950 ^oC [109].

A technique that was explored in 1996 by Lipkin *et al.* was a post-oxidation treatment that involved oxidation performed at a lower temperature after the bulk of the oxide had been grown on SiC [109]. This was named a re-oxidation anneal and was intended to oxidise

any impurities that remained after the original oxidation without oxidising anymore of the silicon. The temperature range used was between 800 and 1000 ^{o}C and three different re-oxidation techniques were analysed. This included wet oxidation and dry oxidation, both at 900 ^{o}C for 1.5 hours and a third technique using the slow pull procedure from the oxidation furnace, which is described by Shenoy *et al.* [110]. The experiment demonstrated that D_{it} is reduced using the slow pull procedure similar to the results found by Shenoy *et al.*, however the reduction seen after wet re-oxidation had a much greater impact as can shown in Table 2.4 by reducing both the interface trap density and the oxide charge density (Q_{OX}). Dry oxidation, as shown in Table 2.4, doubled the interface trap density compared to the result for the sample that had not been through any re-oxidation anneals. It was also found that increasing the wet re-oxidation anneal temperature allowed for Q_{OX} to be reduced even further, but did not have much effect in reducing D_{it}, as shown in Figure 2.8. The best re-oxidation anneal temperature identified during the investigation for oxides grown at 1050 ^{o}C was found to be 950 ^{o}C, as this reduced the net oxide charge density by a factor of 2, whilst reducing the interface trap density by a factor of 2.5, Figure 2.8. Although this method improved the interface trap density of the SiC/SiO_2 interface it still remained an order of magnitude larger than any D_{it} that is witnessed at the Si/SiO_2 interface so it was still important to look for different techniques to reduce the interface trap density even further in order to gain a greater channel mobility in SiC MOS devices, particularly SiC MOSFETs.

Post-Oxidation	Q_{OX} (cm^{-2})	D_{it} ($cm^{-2}eV^{-1}$)
None	4.0×10^{12}	7.1×10^{11}
Slow Pull	2.3×10^{12}	3.2×10^{11}
Wet	1.6×10^{12}	2.8×10^{11}
Dry	3.9×10^{12}	1.5×10^{12}

Table 2.4: Oxide charge and interface trap densities of oxide grown at 1100^{o}C, then processed with either the slow pull, dry or wet post-oxidation procedure.[109]

The use of nitrogen to passivate defects was another common technique used on the Si/SiO_2 interface. Early studies by Li *et al.* found that post-oxidation annealing in N_2O on the SiC/SiO_2 interface increases D_{it}, whilst post-oxidation annealing in NO improves the interface by reducing the density of interface states [111]. The exact cause of the increase in D_{it} by N_2O in the SiC/SiO_2 was unclear in this study, however, it was suggested in a study by Ellis and Buhrman [112] that it could be due to a large amount of Si-N bonds being formed in the already grown SiC/SiO_2 interface and the post-oxidation anneal in N_2O acts to remove the N with the presence of atomic oxygen, therefore deteriorating the interface.

Post-oxidation annealing using nitric oxide (NO) gas has become a very popular technique to reduce the interface trap density in the 4H-SiC/SiO_2 interface. This produces a significant reduction in the interface trap density, considerably more than any of the other techniques that have been discussed so far, and allows mobilities of up to 50 cm^2/Vs to be

achieved [96].

Chung *et al.* [113] found that annealing in NO after a standard oxidation/reoxidation process results in a significant reduction in D_{it} in the upper half of the gap for n-SiC but causes a slight increase in D_{it} in the lower section of the bandgap for p-SiC. Theoretical calculations were explored to explain these effects and it was suggested that this reaction occurred because of carbon clustering. The nitrogen acts to passivate carbon interstitials within the bandgap. Isolated C interstitials are passivated entirely because the gap level drops into the valence band as shown in Figure 2.9 after nitrogen annealing. However for clusters of interstitials, passivation by nitrogen can only drop the gap level to lower within the bandgap, depending on the size of the cluster the gap level will drop between the valence band edge and mid gap. This explains why nitrogen passivation causes a large reduction in the upper part of the bandgap in n-SiC but cause an increase in D_{it} in the lower part of the bandgap in p-SiC.

A comparison between the effect of nitrogen on the fast C-related components, as discussed above, and the slow oxide-related components of D_{it} have also be explored and it is suggested that nitrogen annealing, as well as passivating carbon defects, has a large effect on oxide related traps [114]. This investigation provides a conflicting view to that of Chung *et al.* [113] and suggests that nitridation reduces D_{it} in both the lower and upper parts of the SiC bandgap, although it does state that the decrease observed close to the valence band edge is much lower than the decrease witnessed at the conduction band edge. This suggests that depending on the analysis techniques that are used different traps are observed.

Studies have also identified that density of interface states near the conduction band edge are very consistent for different 4H-SiC crystal structures as it has been shown that nitridation has the same impact on MOS devices that are fabricated on both the (0001) 4H-SiC face and the $(11\bar{2}0)$ face [115].

Different combinations of nitrogen and hydrogen post-oxidation annealing have been explored and produce even lower values of interface trap densities at the SiC/SiO_2 interface

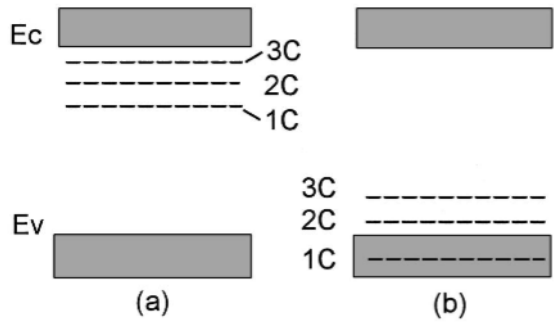


Figure 2.9: (a) Energy Levels for interstitial C and C cluster in SiC. (b) C and C cluster states in SiC following N passivation [113].

than post-oxidation nitrogen annealing. When hydrogen annealing is completed after the deposition of a platinum metal layer, the platinum causes the H_2 to break into monatomic H, which seems to have more impact on reducing D_{it} as it allows H incorporation at the SiC/SiO_2 interface [116]. This combined with nitridation has been found to reduce D_{it} and produce higher mobilities than NO treatment alone. The maximum field effect mobility of 55 cm^2/Vs for Si-face lateral MOSFETs after sequential anneals in NO and H_2 and witnessed reductions of D_{it} from approximately $10^{12}\,cm^{-2}eV^{-1}$ to $5 \times 10^{11}\,cm^{-2}eV^{-1}$ were discovered by Dhar *et al.* [117].

Wang *et al.* have explored analysis of the effects of post-oxidation nitridation followed by hydrogenation. It was found that the combination effectively passivated approximately 30% more of the interface traps near the conduction band edge compared to the NO only technique [118]. Deeper in the gap, the reduction was reported to be even more substantial, an order of magnitude lower. The investigation was also used to predict the mechanisms that are responsible for the reduction in D_{it} using a first principle study. Several mechanisms were discussed. It was hypothesised and simulated that the monatomic H acts to passivate correlated C dangling bonds on neighbouring threefold-coordinated C atoms. However, the study went on to suggest that some of the interface defect states were caused by the Si-C-O bonded interlayer and that both the H and N act to convert this structure into either Si-C-O-N or Si-C-O-N-H bonded interlayers, which acts to reduce threefold C atoms and reduce the interface states further.

A technique developed recently is post-oxidation annealing in phosphoryl chloride ($POCl_3$) [119]. First the technique was examined on MOS capacitors and involved the comparison of different annealing temperatures. All of the samples underwent dry oxidation at 1200 ^{o}C for 160 minutes followed by either no additional annealing or a 900 ^{o}C, 950 ^{o}C or 1000 ^{o}C anneal in a mixture of $POCl_3$, O_2 and N_2. The results from this investigation are shown in Table 2.5. It was found that the 1000 ^{o}C $POCl_3$ anneal produced the greatest effect and reduced D_{it} by more than 1 order of magnitude to $9 \times 10^{10}\,cm^{-2}eV^{-1}$ compared to the interface trap density of the sample that did not undergo any $POCl_3$ annealing treatment, which was 1×10^{12} $cm^{-2}eV^{-1}$.

Gate Oxide	EOT (nm)	D_{it} ($cm^{-2}eV^{-1}$)	Q_{eff}/q (cm^{-2})
Dry (1200^{o}C)	55	1×10^{12}	-2×10^{10}
Dry + NO (1200^{o}C)	58	4×10^{11}	9×10^{10}
Dry + $POCl_3$ (900^{o}C)	56	1×10^{12}	-2×10^{10}
Dry + $POCl_3$ (950^{o}C)	56	1×10^{11}	3×10^{11}
Dry + $POCl_3$ (1000^{o}C)	56	9×10^{10}	4×10^{11}

Table 2.5: Equivalent oxide thickness (EOT), interface state density (D_{it}) at 0.2 eV from E_C and effective oxide charge (Q_{eff}) for 4H-SiC MOS capacitors[119].

Gate Oxide	$\mu_{FE,max}$ (cm^2/Vs)	V_{TH} (V)	S (V/dec)	D_{it} ($cm^{-2}eV^{-1}$)
Dry (1200^{o}C)	6	7.5	1.2	8×10^{12}
Dry + NO (1250^{o}C)	26	3.4	0.6	3×10^{12}
Dry + $POCl_3$ (1000^{o}C)	89	0.0	0.1	1×10^{11}

Table 2.6: Peak field effect mobility ($\mu_{FE,max}$), threshold voltage (V_{TH}), subthreshold swing (S) and interface state density (D_{it}) for 4H-SiC MOSFETs [119].

After analysis of the response of the MOS capacitors to the $POCl_3$ treatment planar n-channel MOSFETs were also fabricated for comparison. One sample underwent dry oxidation without any post-oxidation anneal, one was annealed in NO and one in $POCl_3$. The results for this investigation are shown in Table 2.6. The device parameters were extracted using capacitance-voltage and current-voltage measurements. Table 2.6 shows that $POCl_3$ annealing at 1000 ^{o}C for 10 minutes produces a peak field-effect mobility of 89 cm^2/Vs compared to a field effect mobility of 6 cm^2/Vs and 26 cm^2/Vs for the dry gate oxide and the post oxidation in NO anneal samples respectively [119]. The $POCl_3$ annealed device also had a much lower interface trap density compared to the other samples, as shown in Table 2.6.

Further analysis into the removal of near interface traps through phosphorus incorporation was explored by Okamoto *et al.* [120]. Capacitance-voltage and thermal dielectric relaxation current (TDRC) measurements [100] were used to analyse the near interface traps of oxides prepared by dry oxidation, NO annealing and $POCl_3$ annealing in order to compare the responses of each technique. The TDRC spectra for each sample is shown in Figure 2.10. The data from the TDRC spectra was interpreted using Rudenkos interface model [100]. This assumes that near interface traps (NITs) are intrinsic interfacial defects energetically located close to the conduction band edge of 4H-SiC and the width and height of the peak is related to the density of NITs. An extremely small, shallow signal, less than 1 pA, is seen for the $POCl_3$ annealed device. This suggests that near interface traps are almost completely removed by $POCl_3$ annealing. This is very similar to the response witnessed after sodium-enhanced oxidation.

The use of sodium to reduce the interface trap density in 4H-SiC was first witnessed when it was found that the use of a sintered alumina environment during oxide growth increased the oxidation rate and reduced the number of near interface traps (NITs), which led to field effect mobilities as high as 150 cm^2/Vs [121]. The reduction in the density of near interface traps and increase in oxidation rate witnessed within this process is believed to be caused by the presence of impurities within the alumina [122]. It was concluded in a study by Allerstam *et al.* [123] that the impurity responsible for increasing the oxidation rate and causing a substantial reduction in NITs is sodium.

There are several potential explanations for the role of Na ions in reducing NITs. Tilak *et al.* [124] suggested that Na ions work to neutralise negatively charged defects in SiC by forming an interface dipole, whilst Gudjonsson *et al.* [121] predict that Na availability during growth cause a reduction in interface traps by acting to passivate defects at the interface or within the oxide. However, the underlying mechanism for this reduction in NITs is still uncertain. A density functional theory study by Tuttle *et al.* [125] suggests that the neutral Na is a spectator impurity that occupies near interfacial interstitial sites and does not actually interact with the defects and impurities at the interface. The Na ions are suggested to introduce an effective mass hydrogenic impurity band at the edge of the SiC conduction band that can explain the effects that have been observed after the introduction of sodium ions.

Even though the use of sodium in the gate oxide allows for much higher channel mobilities it does not provide a stable long-term solution particularly for high temperature operation. As the sodium ions are mobile within the interface it is a very unstable and bias-stress testing shows that very large shifts in the flatband voltages (V_{FB}) of devices that are fabricated using sodium can occur [123].

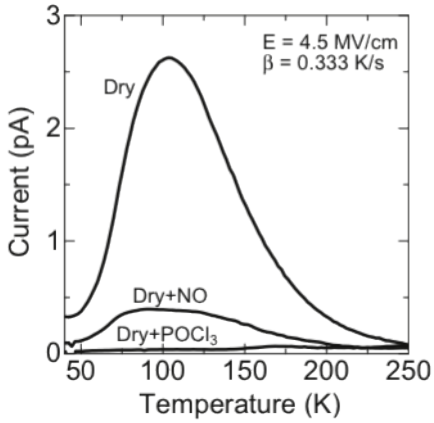


Figure 2.10: TDRC spectra for dry, NO-annealed and $POCl_3$-annealed devices [120].

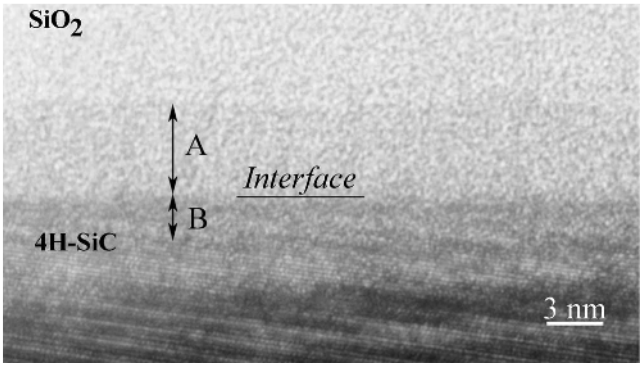


Figure 2.11: High-resolution transmission electron microscopy (HRTEM) image of the SiO_2/4H-SiC interface revealing the transition layers A (4.8 nm) and B (3.3 nm) on the SiO_2 and the SiC sides of the interface, respectively [126].

Other suggested causes of device issues are oxide trapped charge (Q_{OT}) and fixed charge (Q_F) located within the oxide, however, they have not been the main focus of research in SiC MOS to date unlike the great depth in which enhancements to the interface quality have been examined. In Si MOS fixed charge is believed to occur in the first 25 $\AA$ of the oxide from the Si interface due to structural defects such as ionized Si, however, in the case of Si MOS this fixed charge in the oxide was not believed to be in electrical communication with the Si [127]. It is believed that a similar charge will exist in SiC MOS [128] but the physical nature of this charge has not yet been identified. It has, however, recently been observed that a transition layer exists on both sides of the SiC/SiO_2 interface that extends several nanometres into each side of the interface, as shown in Figure 2.11, using transmission electron microscopy (TEM), electron energy loss spectroscopy (EELS) and X-ray photoelectron spectroscopy, which could support the theory of the existence of a fixed charge inside the oxide [126]. Similar results have also been reported about the existence of a transition layer [129] and it has been suggested this layer may be due to the presence of carbon [130], or carbon clusters, suboxide bonds, and defects that trap charge due to the topology and geometry of the SiC surface not being suitable to form an abrupt oxide interface [131]. However, further investigation is needed to support these theories.

Most recently a technique has been presented to reduce the interface trap density by control of the thermal oxidation conditions. Kikuchi *et al.* fabricated 4H-SiC MOS capacitors with almost ideal capacitance-voltage characteristics by selecting the oxidation procedure based on thermodynamic and kinetic considerations of SiC oxidation and produce capacitors with interface state densities of less than $10^{11}\,\mathrm{cm}^{-2}.\mathrm{eV}^{-1}$ at 0.1 eV below the conduction band edge of SiC [132]. In this investigation thermal oxidation was carried out at $1300\,^{o}$C followed by a post-oxidation anneal at $800\,^{o}$C in O_2 indicating that low D_{it} is achievable simply by thermal oxidation.

There has been much development over recent years within the understanding and improvement of the SiC/SiO_2 interface. The fabrication techniques have been honed to now produce much higher mobilities and to decrease the density of interface states at the 4H-SiC/SiO_2 interface. However, there are still a great deal of questions that remain unanswered. After all of these different post-oxidation annealing techniques there is still, in comparison to Si, a very high interface trap density and the device mobilities are still much lower than the potential bulk mobility for the material. This raises the question as to what other device operation limiting defects there are within SiC MOS and what would be a suitable method to eradicate these issues. However, it is also incredibly important to keep in mind that early silicon MOS technology also encountered numerous technical barriers that took many years of dedicated research to overcome and in comparison 4H-SiC MOS is most definitely in its infancy.

2.4.6 *Oxide reliability*

Although the fact that SiC forms SiO_2 when heated in the presence of oxygen potentially allows it to follow the path of the highly successful silicon MOS technology, there remains a number of important differences between both insulator quality and device processing that are currently inhibiting SiC MOSFETs from realising their full potential. Some of the major issues have already been outlined in section **??** with regards to processing technologies to increase the effective channel mobility of MOSFETs and improve the SiC/oxide interface quality. However, the focus of this section is on the examination and development of the insulator to increase stability, limit oxide failures and to minimise leakage current through the gate oxide.

SiC oxides are prone to a higher degree of leakage current and oxide failures when compared to their silicon counterparts. This is believed to be a consequence of the thermal oxide quality and interface structure of SiC MOS which causes devices to display higher levels of interface state densities, fixed oxide charges, charge trapping and carrier oxide tunnelling. As this is the case, the measured breakdown fields of thermally grown SiO_2 on 4H-SiC are in the region of $10\,\mathrm{MV.cm^{-1}}$ [2] [133].

There have been numerous studies into the transport mechanisms in dielectric films grown on 4H-SiC, however, there is a large variation in results and there is no consensus on the dominating conduction mechanisms in the insulators [133][134][135][136][137][138]. The most recent investigations conducted on n-type 4H-SiC have shown that at high electric fields Fowler-Nordheim tunnelling dominates conduction through the insulator and at low and intermediate electric fields leakage is due to trap assisted tunnelling and Ohmic conduction in both dry oxygen and nitride thermally grown oxides [139].

The wide band gap of 4H-SiC reduces the potential barrier impeding tunnelling of damaging carriers through oxides grown on 4H-SiC so that oxides cannot be expected to attain identical high reliability as thermal oxides on silicon [134]. With this being the case it is highly likely that alternative gate dielectrics will have to be utilised for the development of 4H-SiC MOSFETs for the most ambitious high-power and high-temperature applications. Multilayer dielectric stacks will likely be developed to further enhance the SiC MOS system.

2.4.7 *Low channel mobility*

As discussed in subsection 2.4.5 one of the main technological concerns in 4H-SiC MOSFET technology is that of electrically active defects in the SiO_2/SiC interface leading to a high density of interface states (D_{it}) at the conduction band edge [140][104]. One of the main issues caused by D_{it} at and near the SiC-SiO_2 interface in 4H-SiC MOSFETs is a low effective

inversion channel mobility. This acts to reduce the gain of transistors and the current carrying capability of MOSFETs, which means that the performance of 4H-SiC MOSFETs is not nearly as advantageous as it theoretically should be. The effective mobility is reduced by both Coulombic scattering by trapped charges, interface states and fixed oxide charges, which lowers the actual channel mobility and by charge trapping which decreases the number of free carriers in the channel [141][142]. It has also been observed that the interfacial charge could consist of more than just traps, which have been shown to negatively impact on the effective inversion channel mobility [96].

In order to improve the channel mobility many different passivation techniques have been investigated to reduce the high density of interface states as described in subsection 2.4.5 including thermal annealing in hydrogen [105], nitrogen-rich environments [111], sodium [121] and even more recently phosphorus passivation techniques have been employed [119], which has enable mobilities of between 20 and 100 $cm^2V^{-1}s^{-1}$ to be achieved in n-channel MOSFETs.

The data in Table 2.7 show a summary of the literature data on the characteristics of both n and p-channel 4H-SiC MOSFETs which have undergone varying gate dielectric treatments. As shown by the data in Table 2.7 the highest reported peak field effect mobility for an n-channel 4H-SiC MOSFET is 108 $cm^2V^{-1}s^{-1}$ and was extracted from a device which had undergone a post-deposition anneal in $POCl_3$ and was formed on an implanted p-type body [143]. The highest reported p-channel peak field effect mobility is 15.6 $cm^2V^{-1}s^{-1}$ and was extracted form a device which had undergone wet oxidation using the pyrogenic method followed by an anneal in argon at 1200 ^oC for 30 minutes and was formed in an epitaxial n-type body. As can be seen in the table, both the nitridation and phosphorus based processes lead to a significant increase in the field effect mobility for the n-channel devices from values as low as 4 $cm^2V^{-1}s^{-1}$ to mobility values between 30 and 108 $cm^2V^{-1}s^{-1}$, however, as substantially less research has been conducted on p-channel MOSFETs further investigations are required to demonstrate the same trend for p-channel devices.

The increase in mobility has been demonstrated to be due to the passivation of interface states through the removal of excess carbon at the interface and the saturation of dangling bonds [145]. Rozen *et al.* demonstrated that the value of the peak field-effect mobility increased with increasing nitrogen incorporation and a decreasing interface trap density. This is shown in the data in Figure 2.12, which show a plot of peak field effect mobility as a function of the nitrogen annealing time and the interface trap density [144]. A strong correlation is shown between the interface trap density, the field effect mobility and the NO anneal time and an increased NO anneal time leads to a reduction in D_{it} and, hence, an increase in peak field effect mobility which suggests that Coulomb scattering is the limiting transport mechanism at the interface and is reduced by a reduction in D_{it} [146].

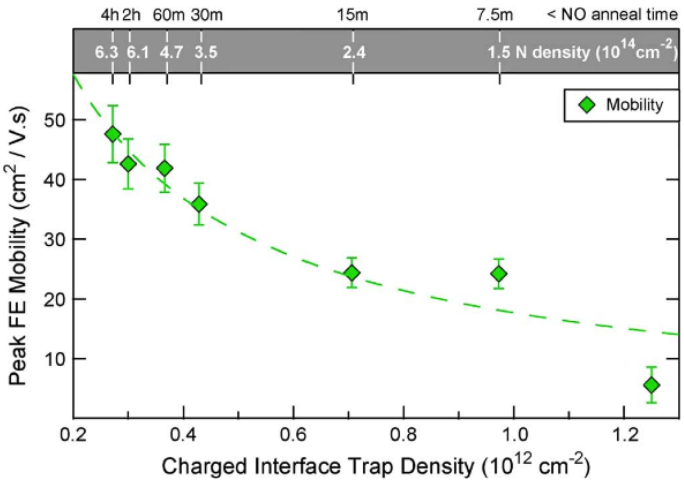


Figure 2.12: Peak field-effect mobility as a function of various NO annealing times (upper axis), which yield distinct densities of charged interface states (lower axis). The N density as the interface is measured by SIMS [144].

In additional to the reduction of D_{it} it has been suggested that during nitridation of the gate oxide nitrogen atoms are incorporated in the SiC substrate and modify its electrical properties acting as n-type shallow donors [147] [148]. If this also occurs during phosphorus passivation, the incorporation of nitrogen or phosphorus atoms in the SiC substrate can lead to a 'counter doping' effect, which acts to compensate acceptors present in the inversion channel region [149]. Swanson *et al.* qualitatively demonstrated an increase in the resistivity of p-type 4H-SiC directly exposed to the annealing atmosphere (N_2O or $POCL_3$) by scanning spreading resistance microscopy (SSRM)[150] and have recently quantified this observation using scanning capacitance microscopy (SCM). An increase in n-type doping under the SiO_2-SiC interface in MOS structures after passivation annealing in N_2 or $POCl_3$ of the deposited gate oxide was witnessed and the concentration of the sample annealed in $POCl_3$ was an order of magnitude higher than the equivalent N_2O annealed sample[151]. Under similar annealing conditions, Liu *et al.* [149] observed an incorporation of phosphorus and nitrogen atoms on the SiC surface of 1.8×10^{14} cm^2 and 5.5×10^{14} cm^2, respectively. Further investigations on this phenomena are necessary in order to understand the impact of the annealing conditions on the device characteristics and also to fully validate the recently presented findings.

As discussed, the mobility characteristics of 4H-SiC MOSFETs have increased over the last decade due to development of the post-oxidation annealing techniques which act to passivate defects at the SiO_2-SiC interface, however, the extracted mobility characteristics are still much lower than the theoretical capability of the material so further improvements are still required to fully realise the true potential of the technology. This is of particular importance for p-channel devices, which are yet to see a great deal of interest in the literature but are a key component for future CMOS applications.

Ref.	**Device**	**Gate dielectric (treatment)**	**L x W** (μm)	**Peak** μ_{FE}**(cm^{2}V^{-1}s^{-1})at 298 K**	**V**$_{TH}$ **(V)**	**t**$_{\mathrm{OX}}$ **(nm)**	**D**$_{\mathrm{it}}$ **(cm^{-2}eV^{-1})**
[152]	n-channel MOSFET	SiO_2 (pyro.) SiO_2 (pyro. +NO)	10×150 10×150	6.2 30.4	5.8 2.7	47 51	7.1×10^{11} 1.3×10^{11}
[96]	n-channel MOSFET	SiO_2 (Dry oxide) SiO_2 (Dry oxide +NO)	120×400 120×400	4 30	 5		
[153]	n-channel MOSFET	SiO_2 (Dry oxide +NO)	320×40	34		125	
[119]	n-channel MOSFET	SiO_2 ($POCl_3$ POA)	30×200	89	0	56	9×10^{10}
[143]	n-channel MOSFET	SiO_2 ($POCl_3$ PDA)		108		45	5×10^{11}
[154]	n-channel MOSFET	SiO_2 (P_2O_5 POA)	150×290	72			3×10^{11}
[144]	n-channel MOSFET	SiO_2 (N_2O POA)	150×290	55			3×10^{11}
[146, 155]	n-channel MOSFET	SiO_2 (N_2O PDA)	40×16	40		30	7.2×10^{11}
[156]	n-channel MOSFET	SiO_2 (NO POA)	140×50	49		54	
[157]	n-channel MOSFET	SiO_2 (NO) SiO_2 (2hr nitrogen plasma) SiO_2 (4 hr nitrogen plasma)	200×200 200×200 200×200	31 22 34	1.6 1.6 2.0	65 50 48	
[125]	n-channel MOSFET	SiO_2 (grown in alumina tube contaminated with Na)	400×400	90	5		
[152]	p-channel MOSFET	SiO_2 (pyro.) SiO_2 (pyro. +NO)	10×150 10×150	5.5 5.6	-8.5 -6.4	47 51	8.9×10^{11} 1.3×10^{11}
[158]	p-channel MOSFET	SiO_2 (N_2O)	100×200	10		47	1×10^{12}
[159]	p-channel MOSFET	SiO_2 (pyro + wet O_2+Argon POA)	100×150	15.6	-4.2	45	2×10^{12}
[160]	p-channel MOSFET	SiO_2 (N_2O)	4×150	5	-6 V	38	1×10^{12}

Table 2.7: Comparison of reported 4H-SiC MOSFET characteristics.

2.4.8 *Threshold voltage instability*

Another phenomenon witnessed in 4H-SiC MOSFETs is threshold voltage instability, which is also due to the presence of charges at the SiO_2-SiC interfacial region in 4H-SiC MOSFETs [161][128]. Research suggests that not all charge beyond that of interface trapped charge (Q_{IT}) is fixed charge and previous investigations propose that the shifting of V_{TH} in devices is an artefact of oxide trapped charge (Q_{OT}), which is sufficiently close to the interface to exchange charge with the channel but is time dependent [128].

By exploring the time dependence of bias-stress-induced V_{TH} instability measurements a strong trend was found between bias-stress time and V_{TH} shift for a wide range of devices from different manufacturers [128]. All trends converged at approximately 1-10 ps at the point when there would be zero V_{TH} shift, which suggests that the tunnelling transition time for SiC MOS is similar to that found in irradiated Si MOS with a similar oxide thickness, which was found to be 0.1 ps [162]. This was concluded to be due to a"tunnelling front" wherein traps were either filled or emptied depending on the applied field and those beyond it remained unaffected. It was determined to move at a rate of 2 $\mathring{A}$ per decade of time into the oxide, with the first transitions occurring at about 0.1 ps, which gave rise to a linear-with-log-time behaviour for a uniform trap distribution [163]. This"tunnelling front" was found to be dominated by electron tunnelling to the E-prime centres (a broken Si-Si bond due to an oxygen vacancy) in the oxide in irradiated Si MOS [164][165][166]. Research suggests that oxide traps in 4H-SiC MOS extend at least 32 $\mathring{A}$ into the oxide from the interface assuming that the tunnelling front of 2 $\mathring{A}$ per decade of time for Si MOS can also be applied to SiC MOS. The distance in the findings are also in agreement with the oxide transition layers for SiC MOS of 3-5 nm thickness, which have been investigated using transmission electron microscopy (TEM), electron energy loss spectroscopy (EELS) and X-ray photoelectron spectroscopy [126][130].

The effect has been witnessed across devices irrelevant of the post oxidation processing technique, however, it has been shown that although the effect still remains it can be reduced by post oxidation annealing such as an NO anneal. It was found that devices that did not have an NO anneal had a larger V_{TH} instability (about 3 times larger) than an equivalent device that had undergone an NO anneal. This suggests that the post-oxidation anneal in NO decreases the number of oxide traps that are observed, which is consistent with other work that found that an NO anneal acts to reduce the number of slow electron traps that are attributed to defects in the near-interfacial oxide layer[101] as well as reducing the number of measured interface traps [111][113][97]. These findings suggest that a post oxidation treatment that effectively passivates interface traps may also reduce the oxide trapped charge so could potentially also act to reduce the threshold voltage instability as well as increase the effective channel mobility of 4H-SiC MOSFETs.

The phenomenon could also be due to a contribution from mobile charge within the oxide (Q_M), which could be present as a result of a non-optimised growth or deposition process. This would also create a varied response across a temperature range as mobile ions may only become mobile enough to move as the temperature increases, which was found in the study by Lelis *et al.* [128]. However, the majority of devices explored showed a positive V_{TH} shift for positive bias stressing and a negative V_{TH} shift for negative bias stressing, which suggests that mobile ions were not involved in the interaction and the response was due to electrons filling or emptying near-interfacial oxide traps in response to the applied electric field.

As this phenomenon is inherent to all SiC MOSFETs, irrelevant of the gate oxide processing methodology, it is important to minimise and examine the effects, particularly across the device operating temperature range, which this will have on the device characteristics particularly for the manufacture of 4H-SiC integrated circuits (ICs).

2.5 Future potential of the technology

The development of a high temperature 4H-SiC CMOS technology would have a wide array of potential uses and applications. There is high demand from a wide range of industrial sectors for resilient electronics for a range of environmental conditions such as high temperature and corrosive ambients. Potential applications, particularly for high temperature integrated circuits, which require reduced cooling, include oil drilling, space exploration, motor drives, avionics and nuclear energy generation [2]. The development of gas sensors for combustion monitoring has created a high demand for amplifiers and analogue-to-digital converters (ADCs) to be co-located with the sensors and able to operate at elevated temperatures in order to improve signal integrity [167]. 4H-SiC CMOS can be used in unison with this technology and could be implemented as both the amplifier and the ADC. The early failure of silicon electronics used in oil and gas drilling applications currently costs companies half a million US dollars for each day that is required to replace failed electronic components from the drill. By replacing such electronics with 4H-SiC devices that are capable of operation at much higher temperatures they should offer higher reliability during prolonged operation at 200 ^{o}C for such applications [2].

An increased understanding along with the development and optimisation of process techniques for some of the issues outlined in section 2.4 such as those of selective doping, Ohmic contact formation and semiconductor/dielectric interface issues could also act to enable the development of other 4H-SiC electronics as the key challenges also impact on other devices. For example an improved ion implantation and post implantation treatment would also benefit the manufacture and performance of bipolar junction transistor (BJT), p-n junction diode and junction field effect transistor (JFET) technology. An improvement on the

interface quality between SiC and SiO_2 could also be transferred for the use in vertical power MOSFETs and MOS capacitor technology and one of the major factors that impacts on the performance and quality of all semiconductor devices is that of Ohmic contact so progress within this area will act to benefit all 4H-SiC electronic devices as well as those for high temperature applications.

The development of solutions that maximise yield and minimise the thermal budget of the manufacturing process for devices will also benefit the manufacture of other 4H-SiC devices as well as help make the technology more affordable.

2.6 Summary

To achieve high performance 4H-SiC CMOS for high temperature applications it is essential to address and optimise some of the key aspects that have been outlined within this review such as the removal/passivation of charges at the SiO_2-SiC interfacial region, which act to degrade device performance through the reduction of the effective inversion channel mobility, causing threshold voltage instability and reduced oxide reliability of 4H-SiC MOSFETs.

Currently the cost of SiC remains substantially higher than that of silicon, which is limiting the adoption and development of the technology. To fully realise the potential of the technology it is of great importance that material quality continues to improve as well as a continued growth in wafer size so that the technology can scale and become more affordable for mass adoption. Furthermore improved material quality will also help increase device yield, which will also benefit the market growth and device cost.

With a particular focus on monolithically fabricated 4H-SiC CMOS technology, which is the interest of this research, it is also of great importance to understand and optimise the production of MOSFET devices built in implanted well structures as it is widely accepted that the performance and quality of regions doped by ion implantation are inferior to that of in-situ epitaxially doped regions. This is also of great importance when the technology advances and processing is used as a tool for threshold adjustment using ion implantation in commercial transistors for both digital and analogue applications for integrated circuits and power applications. This highlights that it is incredibly important for device operation that the ion implantation process and post implantation anneal is optimised to produce material quality that is at least equivalent to that of 4H-SiC doped epilayers.

Another key area that requires attention is that of Ohmic contacts on 4H-SiC. It is important that a process is developed to produce Ohmic contacts that can withstand continuous operation at elevated temperatures for devices built for high temperature applications. For monolithic CMOS devices that are designed to operate in such environments it is incredibly

important to develop contacts on both n and p regions that do not degrade the device characteristics, have sufficiently low contact resistivities over the entire operating temperature range and ideally minimise the cost, time and thermal budget during manufacture to minimise the device cost and maximise uptake.

Chapter 3

Analysis of Ohmic metal contacts on n and p-type 4H-SiC

3.1 Introduction

The main objective of this investigation is to aid in the advancement and commercialisation of a CMOS process to enable the production of signal level 4H-SiC MOSFETs for high temperature digital and analogue applications. As discussed a key enabling technology for 4H-SiC electronics is the fabrication of high quality Ohmic contacts, therefore, the focus of this chapter is on the electrical characterisation and performance of the 4H-SiC n and p-type Ohmic contacts that were employed in the MIS devices that are analysed in chapter 4 and chapter 5. The main aim being to understand the contact characteristics and performance in order to recommend a suitable monolithic process for both n and p-type contacts for 4H-SiC CMOS.

3.2 Overview of the theoretical metal-semiconductor contact

Ohmic contacts are essential to all semiconductor devices as they are used to form connections between the semiconductor device to other circuitry and the outside world. An Ohmic contact should not significantly modify device performance and should supply the required current with a voltage drop that is sufficiently low compared to the drop across the active region of the device. However, the wide band gap of 4H-SiC results in high Schottky barriers, which makes it problematic to form low-resistance Ohmic contacts on 4H-SiC[2]. Therefore, the development of high quality Ohmic contacts on 4H-SiC is an enabling technology for the development of resilient electronics for high temperature applications.

When a metal and semiconductor are brought into contact the Fermi levels of the two materials must be equal at thermal equilibrium. For the ideal case the barrier height (ϕ_{B}) is the difference between the metal work function (ϕ_{M}) and the electron affinity of the semicon-

ductor (χ_s) and can be calculated using Equation 3.1 for an n-type semiconductor.

$$q\phi_{Bn} = q(\phi_M - \chi_s) \tag{3.1}$$

For a contact between a metal and a p-type semiconductor the barrier height (ϕ_{Bp}) is determined using Equation 3.2.

$$q\phi_{Bp} = E_g - q(\phi_M - \chi_s) \tag{3.2}$$

The most common measurement of the transport characteristics of Ohmic contacts is the specific contact resistance (ρ_c). ρ_c of an Ohmic contact is defined as the reciprocal of the derivative of the current density (J) with respect to the voltage across the interface and can be extracted from the current-voltage relationship of a test structure:

$$\rho_c = \left(\frac{\delta J}{\delta V}\right)^{-1}_{V=0}. \tag{3.3}$$

The current conduction in Ohmic contacts can be dominated by 3 different regimes. Each mechanism is dependent on temperature and doping level within the semiconductor, therefore, a comparison between the thermal energy (kT) and the interface characteristic energy (E_{00}), which is dependent on N_D can determine which mechanism is dominating the conduction process. E_{00} is calculated using Equation 3.4.

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_D}{\varepsilon_s \varepsilon_0 m^*_{tun}}}, \tag{3.4}$$

where m^* is tunnelling effective mass, q is electron charge, h is Planck's constant, ε_s is semiconductor permittivity, ε_0 is vaccuum permittivity and N_D is the donor concentration.

At low to moderate doping levels and when $E_{00} \ll kT$, thermionic-emission is the dominant conduction mechanism and ρ_c is calculated using Equation 3.5.

$$\rho_c = \frac{k}{A^{**}Tq} exp\left(\frac{q\phi_{Bn}}{kT}\right) \tag{3.5}$$

where A^{**} is effective Richardson constant and ϕ_{Bn} is the Schottky barrier height. In the thermionic-emission regime ρ_c is very sensitive to barrier height and temperature but is independent of the doping concentration.

When the doping level is higher and $E_{00} \approx kT$ thermionic-field-emission dominates con-

duction. In this condition ρ_c is calculated using Equation 3.6.

$$\rho_c = \frac{k\sqrt{E_{00}}cosh(\frac{E_{00}}{kT})coth(\frac{E_{00}}{kT})}{A^{**}Tq\sqrt{\pi q(\phi_{Bn}-\phi_n)}}exp\left(\frac{q(\phi_{Bn}-\phi_n)}{E_{00}coth(\frac{E_{00}}{kT})}+\frac{q\phi_n}{kT}\right) \tag{3.6}$$

where ϕ_n is the Fermi potential from the conduction band edge in n-type semiconductor (E_c-E_F). In the thermionic-field-emission regime ρ_c is dependent on doping concentration, temperature and barrier height.

With even higher doping, $E_{00} \gg kT$ and field-emission dominates the conduction. ρ_C is calculated using Equation 3.7 and Equation 3.8.

$$\rho_c = \frac{ksin(\pi c_1 kT)}{A^{**}\pi qT}exp\left(\frac{q\phi_{Bn}}{E_{00}}\right) \tag{3.7}$$

$$c_1 = \frac{1}{2E_{00}}log\left(\frac{4(\phi_{Bn}-V_F}{-\phi_n}\right) \tag{3.8}$$

In the field-emission regime ρ_c is dependent upon both ϕ_{Bn} and $\sqrt{N_D}$. Therefore, to obtain low values of ρ_c either high doping, low barrier height or both must be implemented.

In wide bandgap semiconductors, such as 4H-SiC, a metal does not typically exist with a low enough work function to produce a low barrier, therefore, the technique for producing Ohmic contacts on 4H-SiC involves the need for a more heavily doped surface layer to form the Ohmic contact. As discussed in subsection 2.4.4, a combination of both high doping in the substrate and high annealing temperature is required to produce an Ohmic contact to 4H-SiC alongside careful material selection for the contact metallisation. The contact metallisation is also a limitation for the maximum device operating temperature and the most promising material for high temperature Ohmic contacts that has currently been explored is platinum, which has been used in gas sensors [167].

3.3 Current status of the technology

The current status of Ohmic contacts to both n and p-type 4H-SiC was reviewed within section **??**. As previously discussed there has been a great deal of research carried out on the process techniques used for the formation of Ohmic contacts on 4H-SiC including investigations into the materials used for the contact metallisation, the doping concentration of the substrate and the post deposition annealing conditions in order to optimise the performance of the contacts for high temperature applications and to increase the long term stability and

reliability of the Ohmic contacts. However, as discussed there is still much room for further understanding as there still remains a need for significant advancement within 4H-SiC Ohmic contact technology in order to fully realise the potential of SiC electronics for high temperature and other demanding applications. Although there has been demonstration of long term stable n-type contacts at 600 ^{o}C [94] in air there is yet to be an equivalent demonstration of p-type technology. The durability and reliability of SiC Ohmic contacts is one of the critical factors limiting the practical high-temperature limits of SiC electronics and it is essential to have both n and p-type contacts that show long term temperature stability for high temperature SiC CMOS.

3.4 Fabrication techniques and process variation

In this investigation 2 different contact metallisation processes were employed for the n and p-type 4H-SiC Ohmic contacts, respectively. A description of the process for each is given in Table 3.1. In both instances a borophosphosilicate glass (BPSG) passivation layer was first deposited and windows for the contacts were opened using a dry etch followed by a wet etch to control the sidewall profile.

Contact	**Metallisation process**
n-type	A stack of Ti (37.5 nm)/Ni (76 nm) was deposited and then annealed at 650 ^{o}C in argon using a rapid thermal anneal (RTA). The unreacted nickel was then removed using a piranha etch (mixture of H_2SO_4 and H_2O_2) then another 76 nm of nickel was deposited followed by an anneal at 1050 ^{o}C in argon using an RTA. The remaining excess nickel was then removed using a pirhana etch.
p-type	A stack of Al (5 nm)/Ti (5 nm)/Ni (76 nm) was deposited followed by an anneal in argon at 950 ^{o}C using a RTA.

Table 3.1: Description of the processing steps used in the fabrication of the n and p-type 4H-SiC Ohmic contacts used in samples HV06, CR25 and CR27.

3.5 Analysis of contact performance at elevated temperatures

The two-terminal contact resistance method is commonly used to extract the total resistance from a semiconductor test structure with 2 contacts as R_{TH} can be extracted from the experimental current-voltage relationship. A cross section of a lateral two-terminal contact resistor structure is shown in Figure 3.1. For this geometry of structure the total resistance (R_{TH}) is [168]:

$$R_T = \frac{R_{SH}d}{W} + R_d + R_w + 2R_c, \tag{3.9}$$

where R_{SH} is the sheet resistance of the semiconductor, R_d is the resistance due to current crowding under the contacts, R_w is the contact width correction if Z < W, R_c is the contact resistance and d is the distance between the contacts. This technique is useful to show the contact behaviour, however, without an accurate knowledge of each of the resistance components it is not possible to extract the separate parameters such as specific contact resistance using this technique.

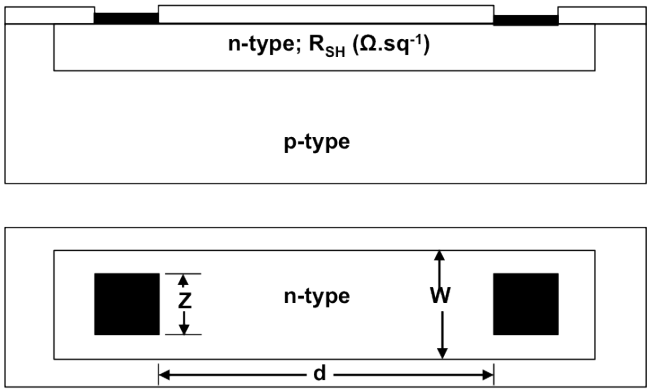


Figure 3.1: A lateral two-terminal contact resistance structure in cross section and top view.

The data in Figure 3.2 shows the current-voltage characteristics between 300 K and 600 K which were extracted from a lateral two-terminal n-type 4H-SiC resistor structure. As shown, the structure showed rectifying (non-Ohmic) behaviour as the current-voltage plot in Figure 3.2 did not exhibit a linear characteristic. This Schottky behaviour suggests that a potential barrier exists within the contact. This could be a product of a structural modification as a consequence of the two step anneal process as described in Table 3.1.

The barrier height (ϕ_B) can be extracted from a semilogarthmic plot of the current-voltage characteristics and an extrapolation of the linear region to extract I_s when V=0 using Equation 3.10.

$$\phi_B = \frac{kT}{q} ln \left(\frac{AA^*T^2}{I_s} \right) \tag{3.10}$$

Where A is the contact area and A^* is the effective Richardson's constant. The I_s value extracted from the data in Figure 3.3 was 0.65 mA and the barrier height was 0.33 V. A value of 146 A.cm^{-2}.K^{-1} was used for the effective Richardson's constant [79][169].

The data in Figure 3.4 show the total resistance extracted from the linear I-V characteristics of the n-type resistor structure in Figure 3.2 calculated by applying Ohm's law to the measured I-V characteristics. The resistance is calculated from the gradient of the current-voltage

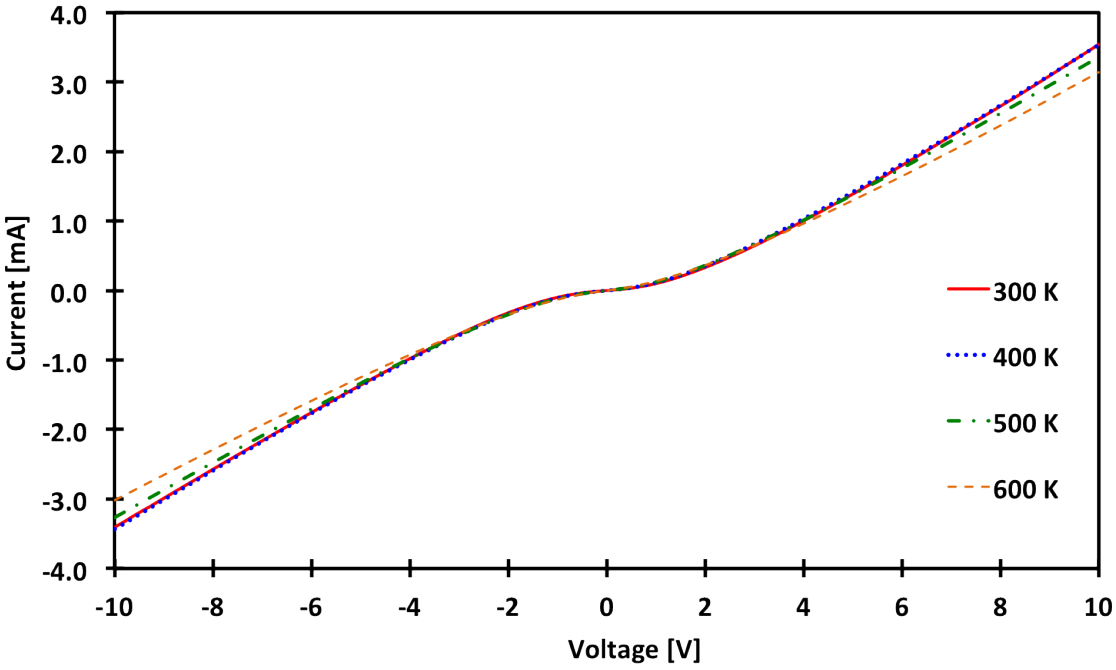


Figure 3.2: Current-voltage plot at varying temperatures of a two-terminal n-type 4H-SiC resistor structure.

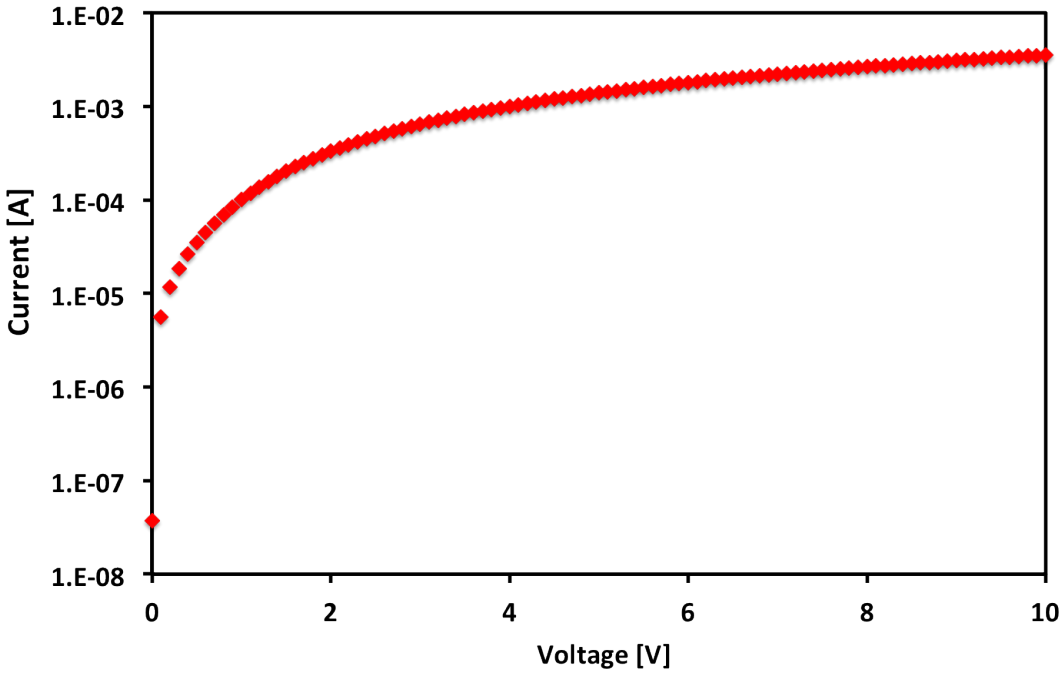


Figure 3.3: Semilogarithmic current-voltage plot of a two-terminal n-type 4H-SiC resistor structure.

data set using 2 data points to mamimise the number of calculated data points. As shown, R_{TH} increases with increasing temperature from a value of 2.40 kΩ at 300 K to 2.85 kΩ at 650 K.

The data in Figure 3.5 show the current-voltage characteristics between 300 K and 600 K

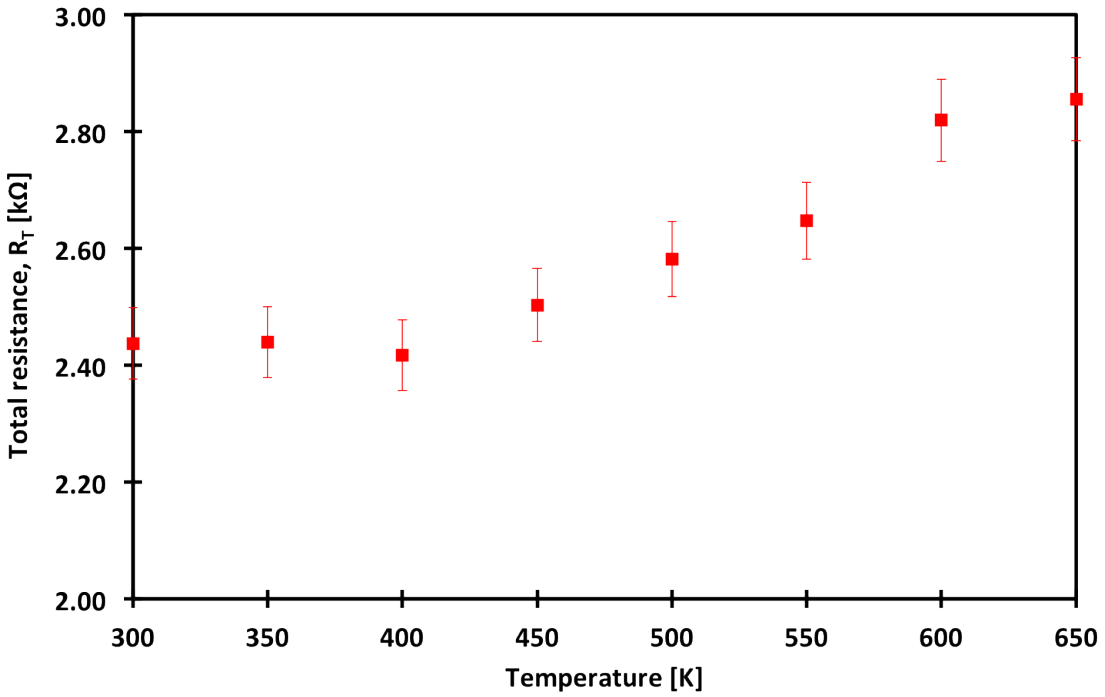


Figure 3.4: Resistance-temperature plot of a two-terminal n-type 4H-SiC resistor structure extracted under a 10 V bias in the linear region of the I-V characteristics from Figure 3.2.

which were extracted from a lateral two-terminal p-type 4H-SiC resistor structure. As shown, the structure showed an Ohmic characteristic across the measured voltage range, which is dominated by the semiconductor and could be due to low doping in the semiconductor. This can be further understood by examining the response of the semiconductor separately by extracting the semiconductor sheet resistance relationship with temperature using a four-terminal van der Pauw structure. A reduction in the total resistance with increasing temperature was also observed, as shown by the data in Figure 3.6.

To understand the mechanism that is dominating the temperature dependence of the resistance in both the n-type and p-type material it is necessary to identify the temperature dependent R_{SH} and ρ_c of the materials.

The sheet resistance (R_{SH}) for the samples was extracted from a four-terminal van der Pauw (VDP) structure [168]. The principles behind the four-terminal VDP method are that the specific resistivity of a flat sample of arbitrary shape can be measured without knowing the current pattern if the following conditions are met: (1) the contacts are at the perimeter of the sample, (2) the contacts are sufficiently small, (3) the sample is uniformly thick, and (4) the surface of sample is singly connected. For a symmetrical square sample with four equal spaced contacts along the periphery the resistance is defined:

$$R_{12,34} = \frac{V_{34}}{I_{12}}, \tag{3.11}$$

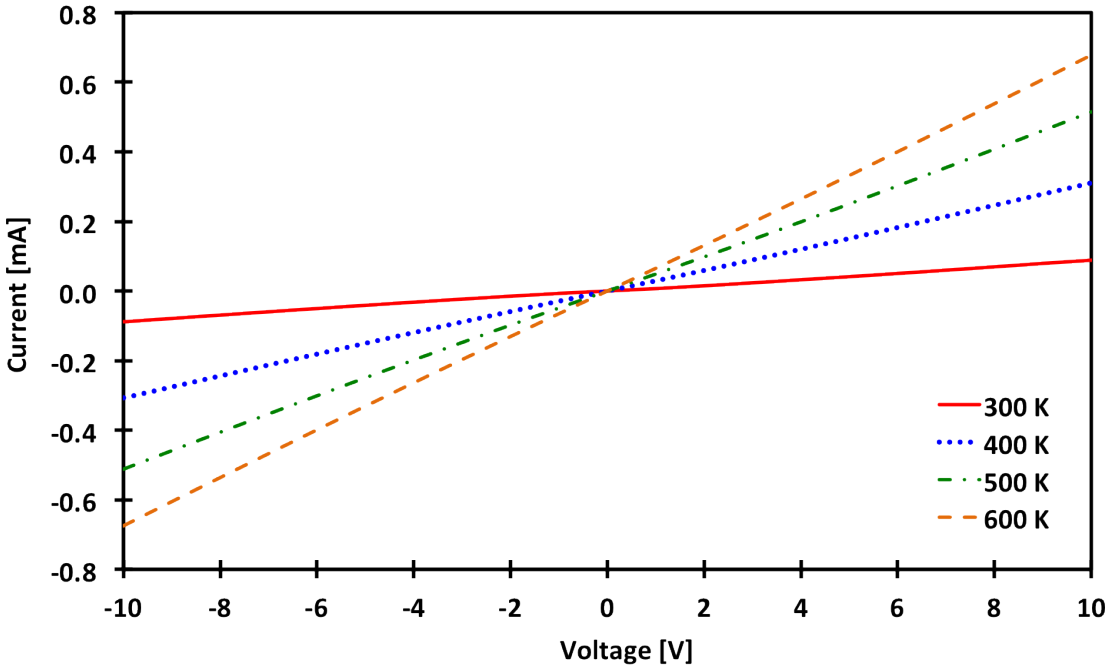


Figure 3.5: Current-voltage plot at varying temperatures of a lateral two-terminal p-type 4H-SiC resistor structure.

where the I_{12} enters the sample through contact 1 and leaves through contact 2 and the voltage (V_{34}) is the voltage difference between contact 3 and contact 4. R_{SH} is equal to Equation 3.12 for a symmetrical sample.

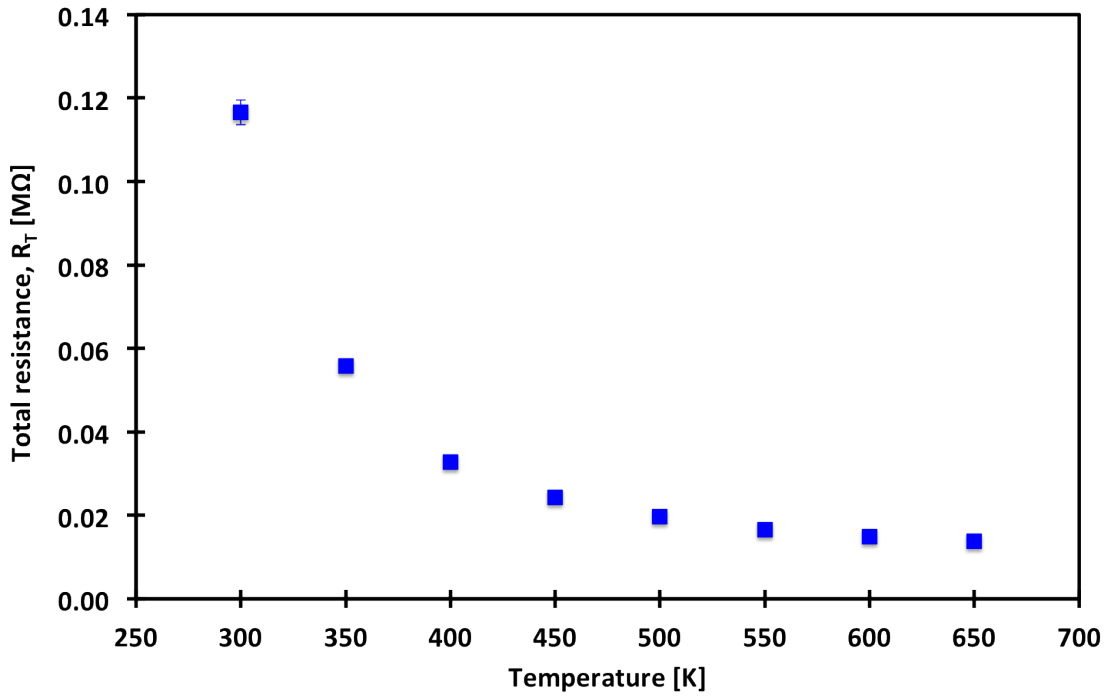


Figure 3.6: Resistance-temperature plot a two-terminal p-type 4H-SiC resistor structure with Ohmic contact behaviour.

$$R_{SH} = \frac{\pi R_{12,34}}{ln(2)} \tag{3.12}$$

The data in Figure 3.7 show the sheet resistance (R_{SH}) extracted from the four-terminal van der Pauw structure between 300 K and 650 K for both n-type and p-type contacts on heavily doped 4H-SiC. R_{SH} decreases with increasing temperature for the p-type sample. The increase in sheet resistance with increasing temperature is similar to previous experimental results [82][170]. As the ionisation energy of N is much lower than that of Al in 4H-SiC an almost complete activation is typically achieved in n-type material at room temperature as discussed in subsection 2.4.3, therefore, the highly doped n-type material behaves as a degenerate semiconductor and shows an increase in R_{SH} with increasing temperature [170]. This is, therefore, also responsible for the increase in R_{TH} with increasing temperature, which was observed in Figure 3.4.

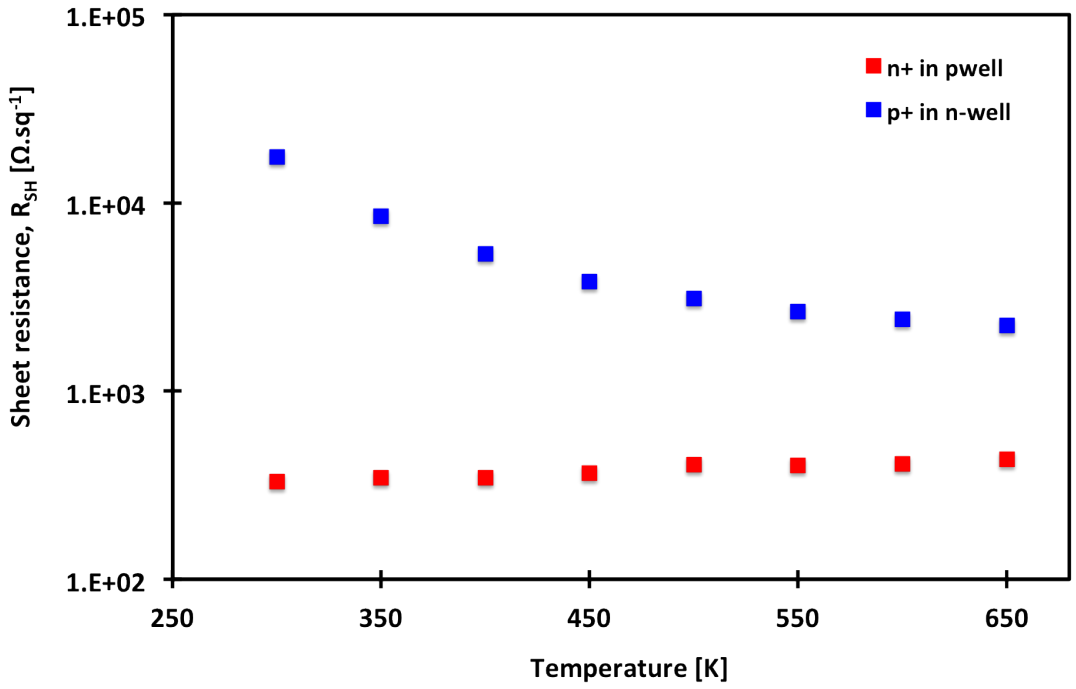


Figure 3.7: Sheet resistance (R_{SH}) vs temperature extracted from a four terminal van der Pauw structure for both heavily doped n-type and p-type 4H-SiC. Measurement error is smaller than the plotted data points.

Room temperature Hall measurements were conducted on the four-terminal VDP structures to extract the electron and hole concentrations from the n and p-type implanted samples, respectively. A uniform implanted layer thickness was assumed and a thickness of 0.3 μm for the n-type layer and 0.35 μm for the p-type layer was used. An electron concentration of 7×10^{18} cm^{-3} was extracted for n-type and a hole concentration of 5×10^{17} cm^{-3} for the p-type sample.

For p-type material the temperature dependent R_{SH} can be related to the hole concentra-

tion and the hole mobility using the relation[1]

$$R_{SH} = \frac{1}{q\mu_p pt}, \tag{3.13}$$

where q is the charge of an electron, and t is the thickness of the implanted layer. The hole concentration depends on the acceptor concentration (N_A) and the concentration of of compensating donors (N_D) and be expressed using Equation 3.14 [168].

$$p \approx \frac{(N_A - N_D)N_V}{gN_D} exp\left(\frac{-E_A}{kT}\right) \tag{3.14}$$

where g is the degeneracy factor for acceptors, E_A is the ionisation energy of acceptors and N_V is the effective density of states in the valence band and is calculated using Equation 4.51.

$$N_V = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2} \tag{3.15}$$

where h is Planck's constant and m^* is the density of state effective mass of the valence band. The hole mobility is dependent on both N_A and T and is described by Equation 3.16 [171].

$$\mu_p(T, N_A) = \mu(300, N_A)(\frac{T}{300})^{\beta(N_A)} \tag{3.16}$$

By substituting in the value of β, which is equal to 2.56 as reported in the literature for the doping conditions used in this investigation [171], and combining Equation 3.13 with Equation 3.15, 3.14 and 3.16 a relationship between R_{SH} and E_A can be derived:

$$R_{SH} = T^{1.06}\frac{gN_D}{N_A - N_D}\frac{h^3}{2(2\pi m^*)^{\frac{3}{2}}}\frac{300^{-\beta}}{qt\mu(300, N_A)} exp\left(\frac{E_A}{kT}\right). \tag{3.17}$$

Therefore, a semilogarithmic plot of $R_{SH}/T^{1.06}$ as a function of q/kT should produce an Arrhenius dependence ($k=Ae^{-E_A/kT}$) which the activation energy (E_A) can be extracted from for p-type material. Figure 3.8 shows a plot of $R_{SH}/T^{1.06}$ against q/kT determined from the data in Figure 3.7 for the p-type sample. As shown, the experimental data follows an Arrenhius law as a linear fit is produced giving an activation energy of 138 meV for the p-type sample, which is comparable to other Al doped samples reported in the literature [79][170].

The specific contact resistance was extracted from a four-terminal cross-brige Kelvin

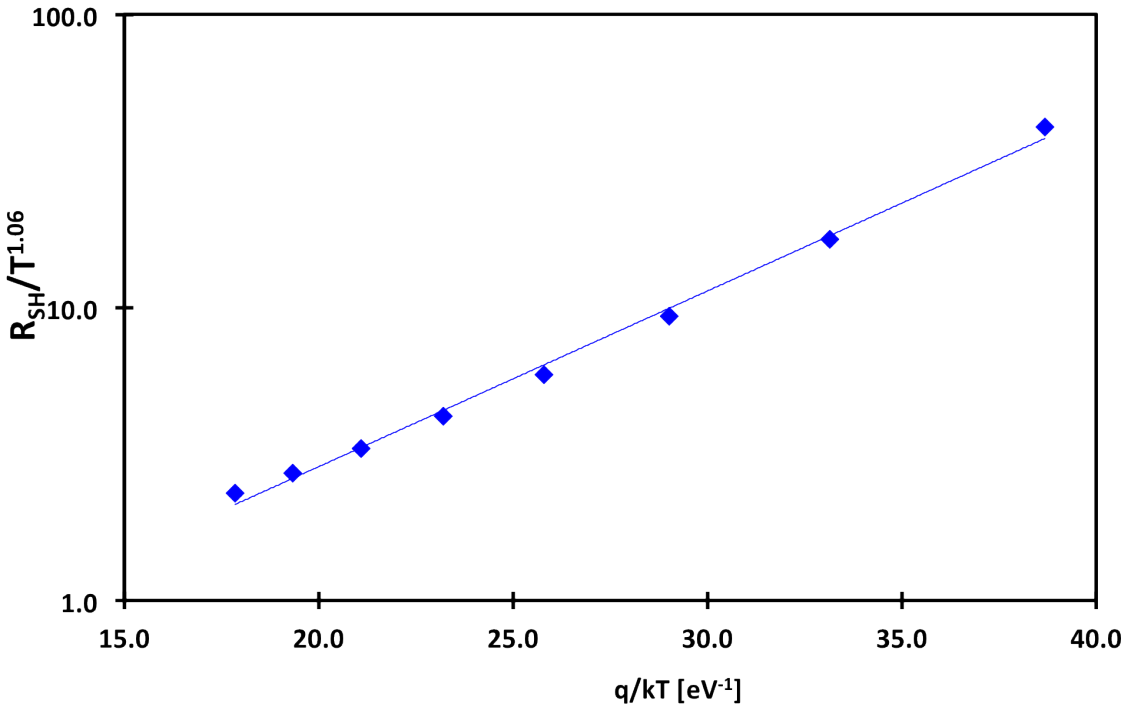


Figure 3.8: Semilogarithmic plot of $R_{SH}/T^{1.06}$ as a function of q/kT for the p-type van der Pauw structure.

resistor (CBKR) structure for each of the samples. The technique is illustrated in Figure 3.9. Current is forced between contacts 1 and 2 and the voltage is measured between contacts 3 and 4. Between contact 1 and contact 2 there are 3 voltage drops: one between contact 1 and the semiconductor; one along the semiconductor; and, one between the semiconductor and contact 2/3. A high input impedance voltmeter used for measuring the voltage between contacts 3 and 4 (V_{34}) allows very little current flow between contacts 3 and 4. The potential at contact 4 is, therefore, the same as the potential in the semiconductor directly under contact 2/3, therefore, the potential difference between contacts 3 and 4 is solely due to the drop across the contact metallisation [168]. The contact resistance is

$$R_c = \frac{V_{34}}{I} \tag{3.18}$$

and the specific contact resistivity is

$$\rho_c = R_c A_c \tag{3.19}$$

where A_c is the contact area.

The data in Figure 3.10 show the specific contact resistance as a function of temperature for both the n-type and p-type contacts on heavily doped 4H-SiC. It can be observed that both samples show a reduction in ρ_c with increasing temperature. For the p-type contact ρ_c

decreased from $2.4 \times 10^{-3}\,\Omega.\text{cm}^2$ at room temperature to $0.5 \times 10^{-3}\Omega.\text{cm}^2$ at 650 K. The n-type contact ρ_c decreased from $2 \times 10^{-3}\Omega.\text{cm}^2$ to $0.9 \times 10^{-3}\Omega.\text{cm}^2$ for the same temperature range.

The high contact resistances witnessed in the n-type 4H-SiC contacts could be a product of the two step anneal process and the extremely thick Ti layer (37.5 nm) used in the metallisation. Contacts formed by deposition of almost identical combinations of Ti and Ni can ehibit both Ohmic [172] and Schottky behaviour [173] depending on the substrate doping and the post deposition annealing temperature. This is due to the fact that the electrical properties of contacts on 4H-SiC are dominated by their structures and phase compositions, which are highly dependent on the high-temperature post-deposition treatment [174]. Therefore, the 2 stage annealing process could have acted to modify the structure or phase composition of the contact. The specific contact resistivity is comparable with the reported ρ_c values for Ni based contacts on n-type 4H-SiC [175][176]

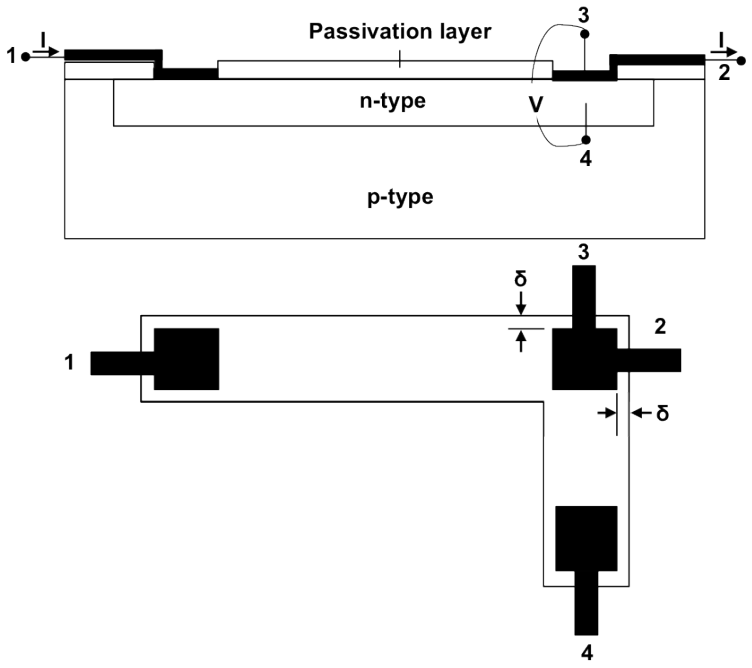


Figure 3.9: A four-terminal cross-bridge Kelvin contact resistor structure cross section and top view.

As discussed in section 3.2 the dominant transport mechanism in the metal-semiconductor interface is dependent on the difference between the interface characteristic energy (E_{00}) and kT/q. A comparison of kT/q with E_{00} calculated for the doping levels at room temperature for the n and p-type contact samples under investigation in this study using Equation 3.4 produces an E_{00} value of 2.4×10^{-4} eV for n-type and 4.2×10^{-5} eV for the p-type contact, which suggests that thermionic-emission (TE) is the dominant transport mechanism in both contacts as $E_{00} << \text{kT/q}$. Therefore, the decrease in ρ_c with increasing temperature for both samples is due to the dependency between ρ_c and 1/T as shown in Equation 3.5.

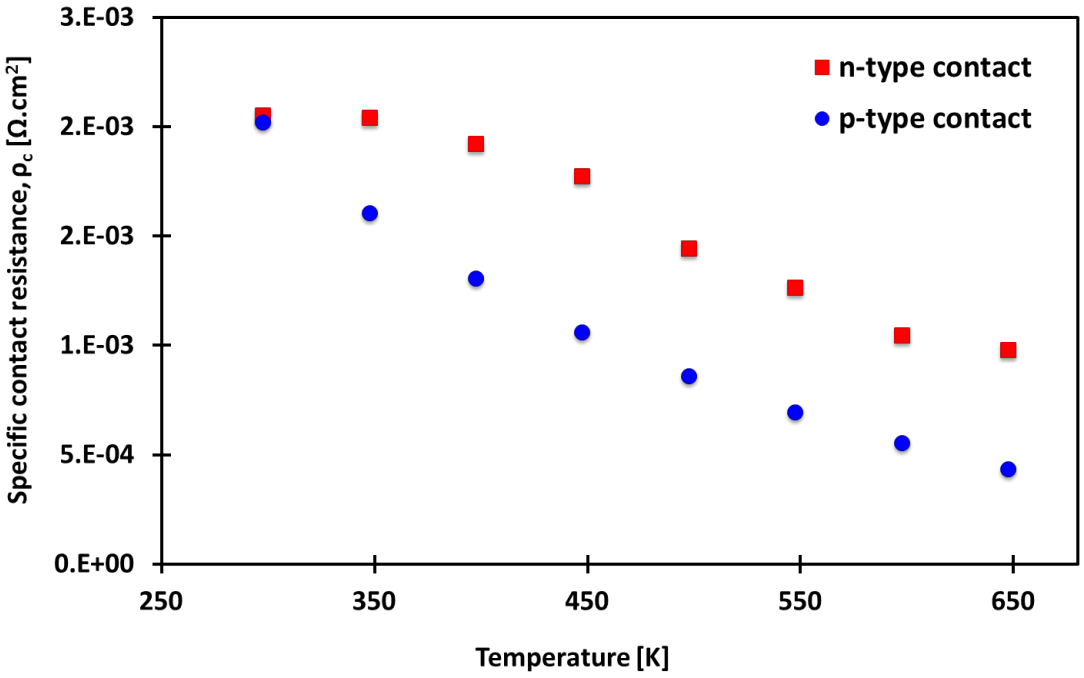
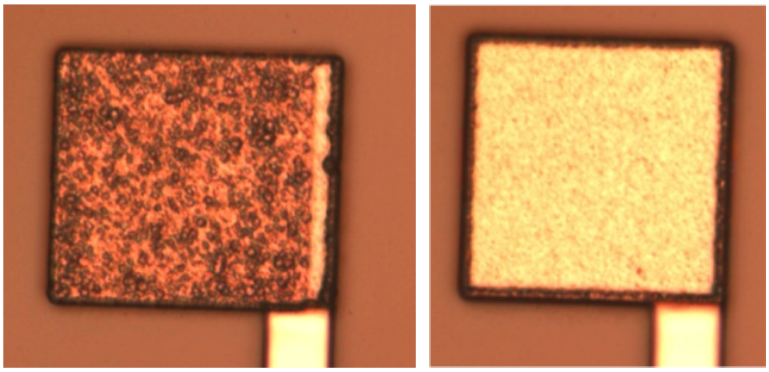


Figure 3.10: Specific contact resistance vs temperature for contacts on both heavily doped n-type and p-type 4H-SiC.

The surface morphology of the contacts was also investigated using optical microscope images and non-contact atomic force microscopy. Figure 3.11 shows an optical microscope image of the metal silicide contact on both heavily doped n-type and p-type 4H-SiC as described in Table 3.1. It is clear within the images that the n-type metallisation is much darker in appearance and has a rougher surface morphology than the p-type contact. To investigate this further a $10\,\mu\text{m} \times 10\,\mu\text{m}$ non-contact atomic force microscopy scan was conducted on each of the samples as shown in Figure 3.12 and 3.13 for the n-type and p-type contacts, respectively. The data in Figure 3.12 and 3.13 show the surface morphology of the n and p-type contacts formed on the samples. It is evident that the n-type contact metallisation has a large surface roughness (R_{RMS}), which is 45 nm and the height variation between the minimum and maximum heights is greater than 200 nm. The data in Figure 3.13 show that the p-type contact has a lower R_{RMS} than the n-type equivalent with an R_{RMS} of 8 nm and height variation between minimum and maximum of approximately 80 nm across the measured sample. The increased R_{RMS} observed for the n-type contact could be a product of the 2 stage anneal process as described in Table 3.1 and could be conistent with the Schottky behaviour of the contact, observed in Figure 3.2, is due to a structural modification of the metallisation as a consequence of the process conditions. It has previously been demonstrated that the interfacial microstructure and, therefore, the electrical performance of Ohmic contacts on 4H-SiC is strongly dependent on the R_{RMS} of the underlying 4H-SiC and also the R_{RMS} of the contact [66]. As the contact metallisations were formed on implanted regions the increased surface roughness of the n-type contact could also be due to a contribution of an increased 4H-SiC

surface roughness due to the ion implantation and post-implant annealing procedure used for the nitrogen ion implantation.



(a) (b)

Figure 3.11: (a) Optical microscope image of metal silicide Ohmic contact on heavily doped n-type 4H-SiC (b) Optical microscope image of metal silicide Ohmic contact on heavily doped p-type 4H-SiC.

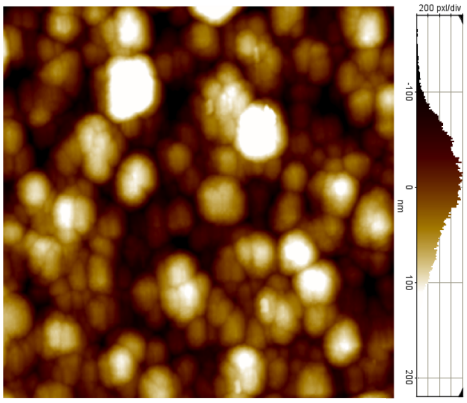


Figure 3.12: $10 \times 10\,\mu$m non-contact AFM image of the metal silicide Ohmic contact on heavily doped n-type 4H-SiC.

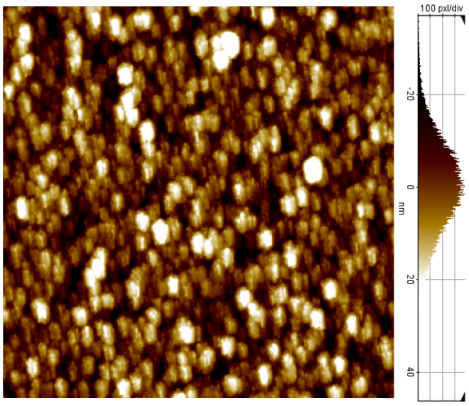


Figure 3.13: $10 \times 10\,\mu$m non-contactt AFM image of the metal silicide Ohmic contact on heavily doped p-type 4H-SiC.

3.6 Optimisation of the contact formation process and contact operation

To improve the potential of the contacts, which have been analysed in this chapter there are a number of steps which should be taken in order to understand the cause of the non-ideal characteristics and also to reduce the process steps required for manufacture.

Firstly, a key area for further investigation is the impact of the ion implantation procedure on the contact characteristics as this is the technique used for almost all SiC device manufacture as discussed in autoref subsection 2.4.3. As it has been widely reported that the ion implantation doping procedure and post-implantation anneal can significantly affect the contact characteristics it is important to explore this further for the metallisations that are under investigation in this thesis [66] as this could be a key component contributing to the high surface roughness and rectifying behaviour of the n-type contact. This could be explored by first investigating the surface morphology of 4H-SiC doped with either N or Al, for n and p-type material, respectively, with different implantation and annealing conditions both with and without a carbon capping layer. If the surface morphology was measured the implantation procedure (dose, energy, capping layer) could be correlated to the surface morphology to explore the dependency. Then the same metallisation could be performed on samples with varying surface morphologies to correlate the specific contact resistance and contact behaviour with the surface morphology of the 4H-SiC. A systematic investigation with controlled variables will allow further understanding into the relationships between process variation and contact performance. This could then be developed further to optimise the fabrication process to explore the doping concentration and surface roughness relationship of 4H-SiC to find the optimum processing conditions.

It has also been reported that the protective carbon capping layer, which is often employed during the post-implantation annealing procedure to protect the 4H-SiC surface can actually be employed as the Ohmic contacts on both n and p-type 4H-SiC, which show stable operation at temperatures up to 450^{o}C [177]. This would therefore, act to remove several process steps from the CMOS fabrication process.

A key area for further investigation is the contact process implemented to form the n-type contacts. As the process currently leads to a contact with rectifying behaviour it is important to understand the cause and, therefore, modify the process to form an Ohmic contact. This could be conducted by performing electrical characterisation of the contacts at different stages of the process. The current-voltage characteristics should be measured after deposition and before the annealing process. They should also be measured after each of the etching steps in order to establish the point at which the characteristics change. Physical investigations such as Auger profiles, TEM or XRD could also be conducted to establish the chemical

composition of the metal stack to explore the change in composition or phases of the material after each of the process steps [81][174]. This could then inform a change in the process steps to improve the contact characteristics.

Another area for further investigation is the specific contact resistance and how to reduce the contact resistivity. This could be achieved through increasing the doping concentration of both the n and p-type regions as the lowest reported contact resistivities on 4H-SiC are reported on highly or degenerately doped material [178]. A reduction in the contact resistivity could also be through an increase in the post deposition annealing temperature as this has also been shown to be beneficial in Ohmic contacts on 4H-SiC. Another option would be to explore other metallisation stack, which have been shown to produce low specific contact resistances on 4H-SiC such as titanium/tungsten alloys [70], titanium carbide [70], nickel [71], palladium [71], nichrome [72] and various metal stacks [73] such as Au/Ti/Al [74], Si/Pt [75] and Ti/Al [76].

It would be beneficial to establish a monolothic process for both n and p-type 4H-SiC to reduce the process steps for production. One way in which this could be achieved is through the use of a Ni/Al stack for both n and p-type contacts. It has previously been demonstrated that a monolithic process can succesfully be employed for both n and p-type contacts on 4H-SiC using an Ni/Al stack [179]. It was found that an optimum thickness of Al between 5 and 6 nm exhibited Ohmic contacts on both n and p-type 4H-SiC.

Finally, the long term stability of the contacts in air is yet to be investigated. Therefore, an investigation should be undertaken to explore the performance of the contacts at temperatures exceeding 300 ^{o}C in air over long timescales such as 1000 hours.

3.7 Summary

This chapter has presented the contact characteristics and performance of both n an p-type Ohmic contacts on 4H-SiC at temperatures up to 650 K. The findings present that both contacts show reliable and stable performance up to 650 K in air with observed specific contact resistances of $2.0 \times 10^{-3}\,\Omega.\text{cm}^2$ and $2.3 \times 10^{-3}\,\Omega.\text{cm}^2$ at room temperature for the n and p-type contacts, respectively.

Both the n and p-type regions had high R_{SH} across the measured temperature range, which is due to the carrier concentration of each of the samples (7×10^{18} cm^{-3} and 5×10^{17} cm^{-3} for the n and p-type material, respectively). To reduce the sheet resistance it would be beneficial to increase the doping concentration of the region, which would also help to reduce the specific contact resistance of the Ohmic contacts. However, the n-type region was shown to be degenerately doped as it exhibited metallic behaviour by showing an increase in resistance

with temperature.

As discussed in section 3.6 further investigations are required in order to explore the rectifying behaviour of the n-type contact, to reduce the specific contact resistances of both contacts and also to explore the long term performance of the contacts at elevated temperatures in air.

Chapter 4

Impact of dielectric formation and processing on the operation of 4H-SiC MIS structures

4.1 Introduction

This chapter aims to act as an overview to the key parameters from the metal-insulator-semiconductor (MIS) structures that are implemented and examined during this project. The main objective in studying the MIS system is to gain an in depth understanding of the impact of the variation in dielectric processing steps in order to facilitate performance and stability improvement in devices, such as the metal-oxide-semiconductor field-effect transistor (MOSFET) used in integrated circuits that will be discussed in further detail in Chapter 5. This information can then be correlated with the field effect mobility and electrical performance of the MOSFETs in order to aid the understanding of the impact of process variation on the MOSFET performance.

4.2 Overview of the theoretical MIS system and operation

The MIS capacitor is one of the most useful devices in the study of semiconductor surfaces, particularly in the characterisation and analysis of the MOSFET, as capacitor structures can be fabricated simultaneously with the MOSFET and numerous electrical properties can be extracted from the MIS capacitor such as [180]:

- Surface band bending and the depletion layer width in the semiconductor as a function of gate bias.
- Doping profile in the semiconductor.
- Interface trap level density as a function of energy in the bandgap.
- Oxide thickness and oxide breakdown field.

- Charge in the oxide such as oxide fixed charge and the interfacial charge between the insulators.
- Nonuniformities in the oxide charge distribution and nonuniformities of surface potential caused by the charge in the oxide.
- Dielectric constant of the semiconductor and the insulator(s).

4.2.1 Ideal MIS capacitor theory

In order to perform any analysis on the measured electrical characteristics that will be examined in this chapter, it is first important to understand the electrostatic theory in both the ideal and non-ideal MIS systems. A cross-section of a simple p-type MIS capacitor is shown, which consists of a thin insulating layer sandwiched between the bulk semiconductor material and a metal, in Figure 4.1a along with the corresponding energy band diagram under equilibrium conditions shown in Figure 4.1b.

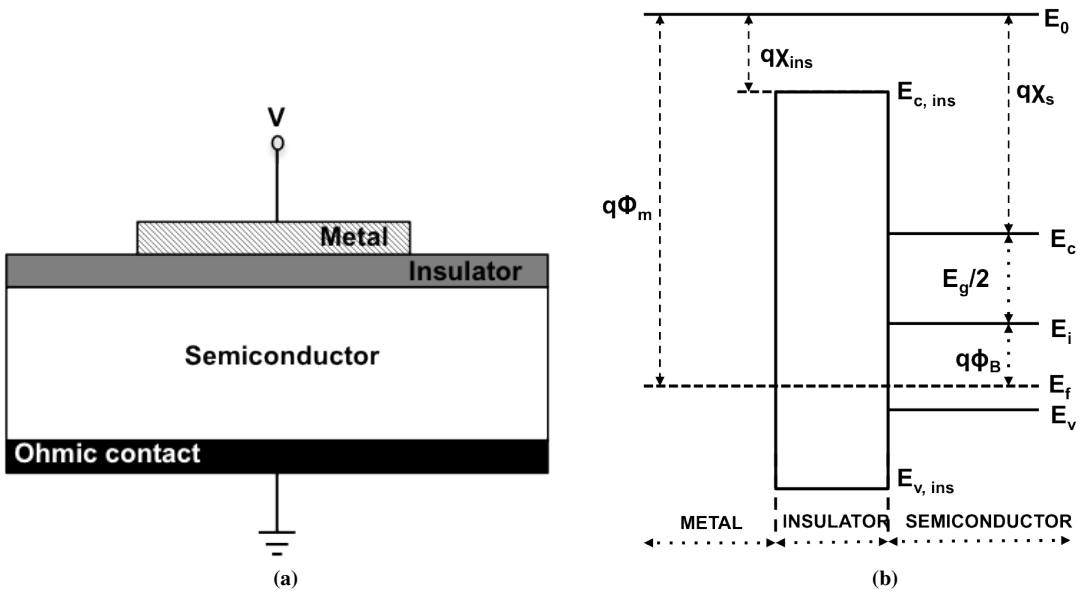


Figure 4.1: Schematic cross-section of an (a) deal p-type MIS capacitor and (b) its energy band diagram under equilibrium conditions.

In Figure 4.1b, E_0 represents the vacuum level and is the minimum energy an electron must possess to completely free itself from the material. E_F is the Fermi energy of the material and E_C and $E_{\rm V}$ are the conduction and valence energies, respectively. The energy difference between E_0 and E_F in a metal is known as the metal workfunction and is denoted by $\phi_{\rm M}$. In a semiconductor the height of the surface barrier relative to E_C is known as the electron affinity and is labelled χ_S in Figure 4.1b. $E_{\rm i}$ is the intrinsic energy level of the semiconductor and $\phi_{\rm B}$ represents the bulk potential or the energy difference between the

Fermi energy and the intrinsic energy of the semiconductor.

In an ideal MIS structure it can be assumed that [1]:

1. The only charges that can exist in the structure under any biasing conditions are those in the semiconductor and those, with an equal but opposite sign, on the metal surface adjacent to the insulator, i.e., there is no interface trap or any kind of charge within the oxide/insulator.
2. The resistivity of the insulator is infinite or there is no carrier transport through the insulator under DC biasing conditions.

Solving Poisson's equation allows the charge density, electric field, and potential to be obtained as a function of position inside the semiconductor. The standard parameters and variables such as the semiconductor doping (N_{A}, N_{D}) and the electrostatic potential can be used in this analysis, however, it is more convenient to deal in terms of normalised parameters. Therefore, common convention introduces the following quantities [180]:

1. Surface potential:
$$q\phi(x) = E_F - E_i(x) \tag{4.1}$$
2. Band bending:
$$\psi(x) = \phi(x) - \phi_B \tag{4.2}$$
3. Normalised band bending:
$$v(x) = \frac{q\psi(x)}{kT} \tag{4.3}$$
4. Normalised surface potential:
$$u(x) = \frac{q\phi(x)}{kT} \tag{4.4}$$
5. Normalised Fermi potential in n-type substrate:
$$u_B = ln\frac{N_D}{n_i} \tag{4.5}$$
6. Normalised Fermi potential in p-type substrate:
$$u_B = -ln\frac{N_A}{n_i} \tag{4.6}$$

where N_{D} is the donor doping concentration, N_{A} is the acceptor doping concentration, n_{i} is the intrinsic carrier concentration of the semiconductor, k is Boltzmann's constant, T is temperature, q is the charge of an electron, ϕ_{B} is the bulk potential, $\phi(x)$ is the potential

at position x in the semiconductor, E_F is the semiconductor Fermi energy and E_{i} is the semiconductor intrinsic energy level.

As the MIS capacitor is assumed to be a one-dimensional structure, Poisson's equation simplifies to,

$$\frac{dE}{dx} = \frac{\rho}{\varepsilon_s \varepsilon_0} = \frac{q}{\varepsilon_s \varepsilon_0}(p - n + N_D - N_A). \tag{4.7}$$

Solving the differential equation and applying the boundary conditions (at the surface (x=0), u=u_s, and in the bulk (x$\rightarrow \infty$), u=u_{B} to ensure charge neutrality [180]) Equation 4.7 becomes:

$$E = -\frac{kT}{q}\frac{dv}{dx} = Sgn(u_B - u_s)\frac{kT}{q\lambda_i}F(v_s, u_B) \tag{4.8}$$

where $F(u_s, u_B)$ is the dimensionless electric field and is calculated using:

$$F(v_s, u_B) = \left(\frac{N_D}{n_i}\right)^{\frac{1}{2}} \left[-(v_s + 1) + exp(v_s) + \left(\frac{n_i}{N_D}\right)^2 exp(-v_s)\right]^{\frac{1}{2}} \text{ for n-type,} \tag{4.9}$$

and

$$F(v_s, u_B) = \left(\frac{N_A}{n_i}\right)^{\frac{1}{2}} \left[(v_s - 1) + exp(-v_s) + \left(\frac{n_i}{N_A}\right)^2 exp(v_s)\right]^{\frac{1}{2}} \text{ for p-type.} \tag{4.10}$$

λ_{i} is the intrinsic Debye length of the semiconductor and is calculated using:

$$\lambda_i = \left[\frac{\varepsilon_s \varepsilon_0 kT}{2q^2 n_i}\right]^{\frac{1}{2}} \tag{4.11}$$

When a bias is applied to an ideal MIS capacitor 3 situations can occur at the semiconductor surface as shown in Figure 4.2. In a p-type MIS structure, as shown in Figure 4.2, when a negative voltage ($V < 0$) is applied to the metal gate, the valence band edge E_{V}, bends upward close to the surface and is closer to the Fermi level. For an ideal MIS capacitor, the Fermi level remains flat in the bulk semiconductor as it is assumed that no current flows in the structure. Since the carrier density depends exponentially on the energy difference ($E_F - E_{\mathrm{V}}$), this band bending causes an accumulation of majority carriers (holes) near

the semiconductor surface, which is known as the accumulation case.

When a small positive voltage ($V > 0$) is applied, the bands bend downward, and the majority carriers are depleted, which is known as the depletion case. When a larger positive voltage is applied, the bands bend downward more so that the intrinsic level E_{i} at the surface crosses over the Fermi level E_F. At this point the number of electrons, or minority carriers, at the surface is larger than that of the holes, therefore, the surface becomes inverted and this is the inversion case. The case for an n-type MIS structure is similar, however, the polarity of the voltage should be reversed.

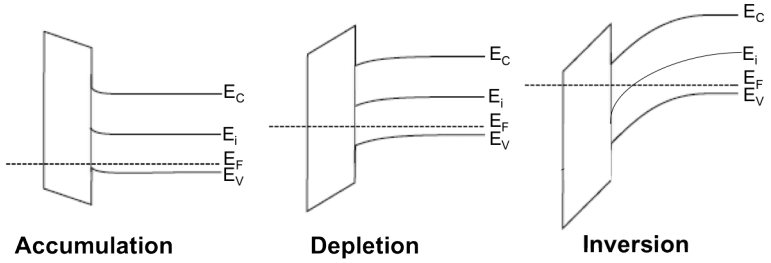


Figure 4.2: Energy band diagrams for a p-type MIS structure in accumulation, depletion and inversion.

At low frequencies it is assumed that both electron and hole distributions in the semiconductor respond instantly to the gate voltage. Therefore, at low frequencies the semiconductor surface capacitance can be calculated using:

$$C_s = \frac{C_{FBS}}{\sqrt{2}} \frac{exp(v_s) - (\frac{n_i}{N_D})^2 exp(-v_s) - 1}{\sqrt{[-(v_s+1) + exp(v_s) + (\frac{n_i}{N_D})^2 exp(-v_s)]}} \text{ for n-type,} \tag{4.12}$$

and

$$C_s = \frac{C_{FBS}}{\sqrt{2}} \frac{1 - exp(-v_s) - (\frac{n_i}{N_A})^2 exp(v_s)}{\sqrt{[(v_s-1) + exp(-v_s) + (\frac{n_i}{N_D})^2 exp(v_s)]}} \text{ for p-type.} \tag{4.13}$$

where C_{FBS} is the semiconductor flatband capacitance and is calculated using:

$$C_{FBS} = \frac{\varepsilon_0 \varepsilon_s}{\lambda_n} \text{ for n-type and } C_{FBS} = \frac{\varepsilon_0 \varepsilon_s}{\lambda_p} \text{ for p-type.} \tag{4.14}$$

λ_n and λ_p are the extrinsic Debye lengths for an n and p-type semiconductor, respectively.

$$\lambda_n = \sqrt{\left(\frac{\varepsilon_s kT}{q^2 N_D}\right)} \text{ for n-type and } \lambda_n = \sqrt{\left(\frac{\varepsilon_s kT}{q^2 N_A}\right)} \text{ for p-type.} \tag{4.15}$$

The total capacitance of the MIS structure is the sum of the semiconductor capacitance and the oxide capacitance in series, which is given in Equation 4.16.

$$C_{total} = \frac{C_s C_i}{C_s + C_i} \tag{4.16}$$

The capacitance is dominated by different terms of Equation 4.13 during each regime of operation. In the capacitance characteristics of a p-type semiconductor, as shown in Figure 4.3, in strong accumulation when $v_s < 0$ the capacitance is dominated by:

$$\frac{C_{FBS}}{\sqrt{2}} exp \frac{-v_s}{2} \tag{4.17}$$

In depletion when $2u_B > v_s > 0$ the capacitance is dominated by:

$$\frac{C_{FBS}}{\sqrt{2}} \frac{1}{\sqrt{v_s - 1}} \tag{4.18}$$

In inversion when $v_s > 2u_{\mathrm{B}}$ the capacitance is dominated by:

$$\frac{C_{FBS}}{\sqrt{2}} \frac{n_i}{N_A} exp \frac{v_s}{2} \tag{4.19}$$

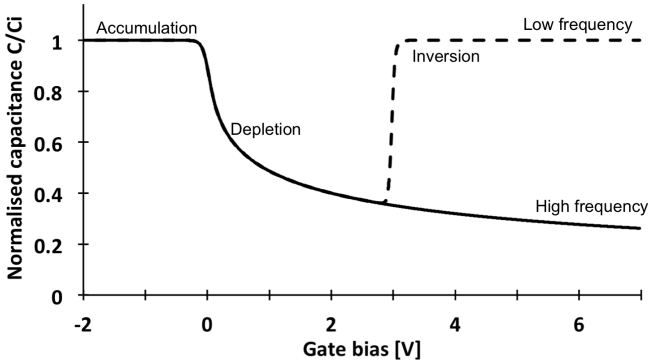


Figure 4.3: C-V curves of an ideal p-type 4H-SiC MIS capacitor with both low frequency and high frequency C-V curves.

At high frequencies minority carriers can not follow the AC voltage, therefore, at high frequencies the semiconductor capacitance simplifies to:

$$C_s = \frac{C_{FBS}}{\sqrt{2}} \frac{exp(v_s) - 1}{\sqrt{[-(v_s + 1) + exp(v_s)}} \text{ for n-type,} \tag{4.20}$$

and

$$C_s = \frac{C_{FBS}}{\sqrt{2}} \frac{1 - exp(-v_s)}{\sqrt{[(v_s - 1) + exp(-v_s)}} \text{ for p-type.} \tag{4.21}$$

An ideal high frequency C-V characteristic for a p-type 4H-SiC MIS capacitor is shown by the solid line in Figure 4.3.

4.2.2 Non-ideal MIS capacitor

In the non-ideal MIS system charges are present within the interface and the insulator, which can be caused by structural or chemical related defects and can substantially affect the electrical properties of field effect devices. Interfacial charge consists of more than just interface traps. However, it is accepted that within Si MOS technology (as shown in Figure 4.4) charge at the interface and in the gate oxide can be attributed and categorised into 4 types: fixed charge (Q_F), mobile charge (Q_M), interface trapped charge (Q_{IT}) and oxide trapped charge (Q_{OT}) [127] and it is believed that the same charges exist at the SiC/SiO_2 interface.

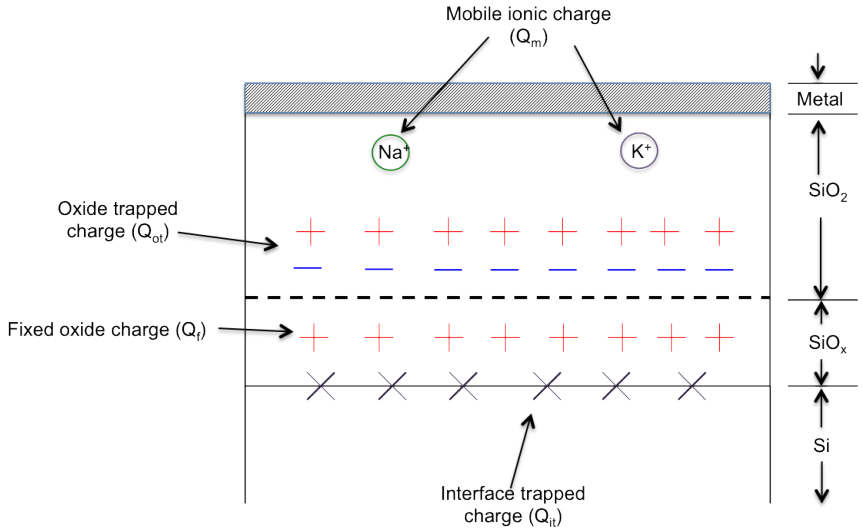


Figure 4.4: Terminology for charges in the silicon MOS system [127].

Interface trapped charges (Q_{IT}) are located at the semiconductor-dielectric interface with energy states within the semiconductor bandgap and can exchange charges with the semiconductor in a short time. Q_{IT} is also determined by the occupancy of the trap states and the position of the Fermi level so its value is bias dependent. Fixed oxide charges (Q_F) are located at or near the interface and are immobile under an applied electric field. Oxide trapped charges (Q_{OT}) are traps that are distributed within the oxide layer and can be created by X-ray radiation or hot-electron injection. Mobile ionic charges (Q_M) are charges that are mobile within the oxide under bias-temperature stress conditions and are often attributed to sodium and potassium ions in the oxide.

4.3 Current status of the technology

The current status of the 4H-SiC MIS structure was described in section **??**. As previously discussed, there has been a great deal of research carried out on the process conditions used during the growth, deposition and post oxidation annealing treatments of the 4H-SiC MIS system, with a particular interest in how each technique acts to impact on or improve the semiconductor-dielectric interface. However, as discussed there is still much room for further understanding as there still remains a high interface trap density at the semiconductor-dielectric interface that acts to dramatically reduce the channel mobility of 4H-SiC MOSFETs irrelevant of the treatment techniques.

4.4 Processing techniques for the growth and deposition of dielectrics

In this investigation 3 gate dielectrics on both n and p-type 4H-SiC that have undergone differing process treatments were examined using electrical characterisation of MIS capacitor structures that were fabricated monolithically with the MOSFET devices that will be discussed in Chapter 5. The devices studied here are identical, except for a distinctive variation in gate dielectric treatments used in their fabrication. The main aim of this investigation is to highlight the benefits and potential issues of each processing technique on the electrical performance of the devices under test.

The three distinct samples labelled as HV06, CR25 and CR27. Sample HV06 has a thermally grown, annealed oxide, sample CR25 has a deposited, annealed oxide, which was preceded by a thick, thermally grown sacrificial oxide, while sample CR27 has a thin thermal oxide left in situ under a deposited, annealed oxide. A detailed description of the dielectric growth and post oxidation treatments is given for each of the samples in Table 4.1. The quoted thicknesses were extracted by Raytheon UK using ellipsometry data during fabrication.

Sample	**Dielectric processing**
HV06	40 nm thermal oxide at 1200 ^{o}C in O_2, annealled in HCl/O_2 at 950 ^{o}C then N_2O at 1200 ^{o}C
CR25	40 nm thermal oxide at 1200 ^{o}C in O_2, Annealled in $POCl_3$ at 1000 ^{o}C, strip oxide, 40 nm deposited undoped low temperature oxide (LTO), annealed in H_2O at 875 ^{o}C, annealed in N_2 at 1100 ^{o}C
CR27	5 nm thermal oxide at 1200 ^{o}C in O_2, 40 nm deposited phosphosilicate glass (PSG) (1.5 % P), annealled in steam at 950 ^{o}C.

Table 4.1: Description of the processing steps used in the fabrication of the dielectrics in sample HV06, CR25 and CR27.

The CMOS test structures analysed within this thesis were fabricated on a 100 mm, Si face, 4^o off axis, 4H SiC n+ wafer with a doped epitaxial layer. N and p-type regions were formed by ion implantation. The implants were annealed with the surface protected by a carbon cap. A thick field oxide and a thin gate dielectric region were then formed followed by the formation of doped polysilicon gate electrodes. Nickel based contacts were then formed on the doped regions and a refractory metal interconnect was deposited and patterned. Next a thin nickel top layer was applied to protect the pads from oxidation during probe testing at elevated temperatures. Finally an oxide layer was deposited for final passivation and scratch protection and openings were made for bond pads.

4.5 Overview of the implemented device characterisation methods

To extract the device parameters from the 3 dielectrics on both and n and p-type substrates capacitance-voltage (C-V), conductance-voltage (G-V) and current-voltage (I-V) measurements were performed using a Keithley 4200-SCS semiconductor parameter analyser.

After C-V measurements are performed it is necessary to correct the results for series resistance (R_S) using the parallel equivalent model [180]. First R_S is calculated from the measured data set using Equation 4.22.

$$R_S = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{4.22}$$

where G_{ma} is the measured conductance in accumulation, C_{ma} is the measured capacitance in accumulation, and ω is the measurement frequency [180]. Once R_S is computed the corrected capacitance (C_C) and conductance (G_C) can be calculated using Equation 4.23 and 4.24.

$$C_C = \frac{(G_m^2 + \omega^2 C_m^2) C_m}{\alpha^2 + \omega^2 C_m^2} \tag{4.23}$$

$$G_C = \frac{(G_m^2 + \omega^2 C_m^2) \alpha}{\alpha^2 + \omega^2 C_m^2} \tag{4.24}$$

where C_{m} is the measured capacitance, G_{m} is the measured conductance and α is a variable that is calculated using Equation 4.25 [180].

$$\alpha = G_m - (G_m^2 + \omega^2 C_m^2) R_S \tag{4.25}$$

After the series resistance correction has been performed on the measured characteristics many of the device parameters outlined in section 4.2 can be extracted from the measured results.

In strong accumulation from the C-V characteristics, C_{i} is equal to C_{max} allowing ε_{i} and the equivalent oxide thickness or t_{i} to be extracted if the capacitor area (A) is known using:

$$C_i = \frac{\varepsilon_0 \varepsilon_i A}{t_i} \tag{4.26}$$

The ionised dopant impurity level can be extracted from the C-V characteristics in depletion using [180]:

$$N_{A,D} = \frac{2}{A_{gate} q \varepsilon_0 \varepsilon_i} \left[\frac{d}{dV} \left(\frac{1}{C^2(V)} \right) \right]^{-1} \tag{4.27}$$

Flatband voltage can be extracted from the C-V characteristics by calculating the flatband capacitance when band bending is zero ($\psi_S = 0$) using Equation 4.28 and extracting the corresponding voltage from the C-V data set for the calculated capacitance value.

$$C_{FB} = \left(\frac{C_{FBS} C_i}{\left(\frac{C_i}{A}\right) + C_{FBS}} \right) \tag{4.28}$$

$$C_{FBS} = \frac{\varepsilon_0 \varepsilon_s}{\lambda_i} \tag{4.29}$$

4.5.1 Extraction of interface trap density

With a view to understanding the techniques that will be discussed and used to extract the interface trap density it is first important to recognise the MIS equivalent circuits and equations in different operating conditions. When a bias is applied across a MIS capacitor, a change of charge in the interface traps occurs as the Fermi level at the semiconductor surface moves with respect to the interface trap levels. This change of charge affects the MIS capacitance and alters the ideal MIS curve. The basic equivalent circuit incorporating theses effects is shown in Figure 4.5a. In this figure, $\mathrm{C_i}$ and $\mathrm{C_D}$ are the insulator capacitance and the semiconductor depletion capacitance, respectively. $\mathrm{C_{it}}$ and $\mathrm{R_{it}}$ are the capacitance and resistance associated with the interface traps and are also functions of energy. The product of $\mathrm{C_{it}R_{it}}$, is defined as the interface trap lifetime τ_{it}, which determines the frequency behaviour of the interface traps and is an important parameter used in the conductance technique that will be discussed further in this section. The parallel branches of the equivalent circuit in Figure

4.5a can be converted into a frequency dependent capacitance C_p parallel with a frequency dependent conductance G_p, as shown in Figure 4.5b, where,

$$C_p = C_D + \frac{C_{it}}{1 + \omega^2 \tau_{it}^2} \tag{4.30}$$

and,

$$\frac{Gp}{\omega} = \frac{C_{it}\omega\tau_{it}}{1 + \omega^2 \tau_{it}^2}. \tag{4.31}$$

The low frequency and high frequency limits are also important and the equivalent circuits for each are shown in Figure 4.5c and4.5d. In the low frequency condition, R_{it}, is set to zero and C_D is in parallel to C_{it}. In the high frequency limit, the $C_{it}R_{it}$ is open and so can be omitted from the circuit. Physically this means that the traps are not fast enough to respond to the fast signal. The capacitance for each of these cases is given by Equation 4.32 and 4.33:

$$C_{LF} = \frac{C_i(C_D + C_{it})}{C_i + C_D + C_{it}}, \tag{4.32}$$

$$C_{HF} = \frac{C_i C_D}{C_i} + C_D. \tag{4.33}$$

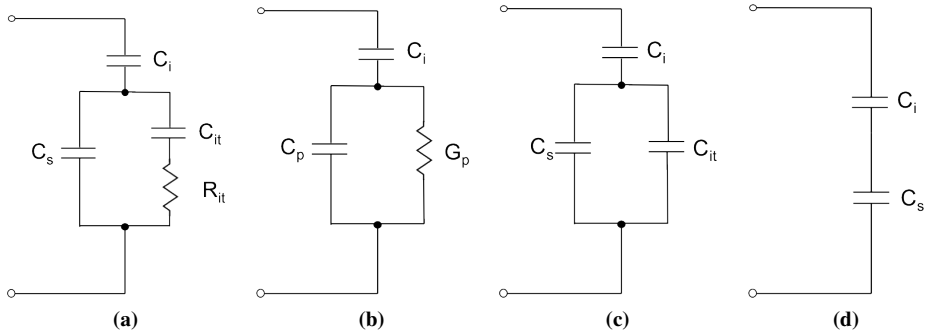


Figure 4.5: (a)-(b) Equivalent circuits including interface trap effects, $C_{\rm it}$ and $R_{\rm it}$. (c) Low frequency limit. (d) High frequency limit.

Conductance method

The conductance technique, proposed by Nicollian and Goetzberger in 1967 [181] allows the extraction of $D_{\rm it}$ in the depletion and weak inversion portion of the bandgap, the capture cross-sections for majority carriers, and information about surface potential fluctuations. The technique is based on measuring the equivalent parallel conductance of a MIS capacitor, as shown in the equivalent circuit in Figure 4.5b, as a function of bias voltage and frequency.

The interface traps are detected through the loss resulting from changes in their occupancy due to changes in the voltage bias during the AC measurement [180] and be calculated using Equation 4.34.

$$\frac{G_p}{\omega} = \frac{\omega C_i^2 G_m}{G_m^2 + \omega^2 (C_i C_m)^2} = \frac{C_{it}\omega\tau_{it}}{1+\omega^2\tau_{it}^2} \tag{4.34}$$

where G_p is the equivalent parallel conductance, ω is 2πf, G_m is the measured conductance, C_m is the measured capacitance, C_{it} is the interface trap capacitance and τ_{it} is the trap time constant, which is equal to $R_{it}C_{it}$. Once C_{it} is calculated D_{it} is obtained using the relation $D_{it}=\frac{C_{it}}{q^2}$.

High frequency capacitance method

The high frequency capacitance method also known as the Terman method [182] provides a rapid evaluation of the semiconductor-insulator interface. At a sufficiently high frequency interface traps are assumed not to respond and do not contribute any capacitance to the system as shown in Figure 4.5d. The interface traps, however, do respond to the slowly varying DC gate voltage and cause the high frequency C-V curve to stretch out along the gate voltage axis as interface trap occupancy changes with gate bias. This technique is based on the extraction of the experimental surface potential, ψ_s, versus gate voltage by comparing the experimental C_m versus V_G curve with the theoretical C vs V_G plot. The resulting ψ_s versus V_G relation is a stretched out version of the theoretical curve which contains all of the necessary information to determine D_{it}:

$$D_{it}(\psi_s) = \frac{1}{qA_{gate}}\left(C_i\left[\left(\frac{d\psi_s}{dV_G}\right)^{-1} - 1\right] - C_s(\psi_s)\right) \tag{4.35}$$

One disadvantage of this technique and the following low frequency capacitance method is that the exact doping concentration of the semiconductor must be known to calculate the C_s (ψ_s) relation.

Low frequency capacitance method

The low frequency capacitance method involves measuring a C-V curve at a constant frequency so low that interface traps respond immediately causing them to contribute an additional capacitance (C_{it}) to the measured low frequency C-V curve as shown in Figure 4.5c. D_{it} can then be extracted using:

$$D_{it}(\psi_s) = \frac{1}{qA_{gate}}\left(\left[\frac{1}{C_{LF}} - \frac{1}{C_i}\right]^{-1} - C_s(\psi_s)\right) \tag{4.36}$$

As with the high frequency technique, a theoretical calculation is necessary to find $C_s(\psi_s)$. A major disadvantage of the low frequency capacitance method is the measurement difficulty in the presence of increased DC leakage of thinner oxides.

Combined high-low frequency capacitance method

This method was developed by Castagne and Vapille [183] and involves combining both the high frequency and low frequency methods. This technique eliminates the need for a theoretical calculation of C_s, which can be complex if the doping profile is non-uniform or if the profile is unknown. D_{it} is extracted using:

$$D_{it}(\psi_s) = \frac{1}{qA_{gate}}\left(\left[\frac{C_{LF}C_i}{C_i - C_{LF}}\right] - \left[\frac{C_{HF}C_i}{C_i - C_{HF}}\right]\right) \tag{4.37}$$

To determine the energy spectrum of D_{it} either the low frequency or high frequency approach can be used to determine ψ_s.

4.5.2 Current-voltage measurements

Current-voltage measurements of MIS capacitors allow the identification of the conduction mechanism within the insulator to be established and allow the leakage current and the electrical breakdown characteristics of insulators to be observed. In an ideal MIS structure it is assumed that there is zero conduction through the insulating layer, however, in real insulators some degree of carrier conduction occurs when the electric field or temperature is sufficiently high. An estimate of the electric field in an insulator under biasing conditions can be calculated using:

$$E_i = \frac{V}{t_i} \tag{4.38}$$

where V is the voltage bias across the MIS structure and t_{i} is the thickness of the insulator. The current density per unit area can be calculated using equation Equation 4.39 where I is the measured current and A is the capacitor area.

$$J = \frac{I}{A} \tag{4.39}$$

Electrical conduction in MIS structures is temperature and voltage dependent and can be caused by different conduction mechanisms and depending on the insulator, one of the charge transport mechanisms may dominate in a certain temperature and voltage range[1]. Table 4.2 summarises the basic conduction mechanisms that are observed in insulators. Current-voltage

characteristics are used in this thesis to compare the conduction mechanisms witnessed in the 3 dielectrics (HV06, CR25 and CR27) on both n and p-type 4H-SiC.

Mechanism	**Expression**
Trap assisted tunnelling	$J = \frac{2qC_tN_texp\left[(\frac{-D}{E_i}\phi_t^{\frac{3}{2}}\right]}{3E_i}$ (4.40)
Fowler-Nordheim tunnelling	$J = \frac{q^3m}{8\pi\hbar m_{ox}\phi_B}E_i^2exp\left[-\frac{8\pi\sqrt{2m_{ox}}(\phi_B)^{\frac{3}{2}}}{3q\hbar E_i}\right]$ (4.41)
Thermionic emission	$J = A^{\star\star}T^2exp\left[\frac{-q(\phi_B-\sqrt{\frac{qE_i}{4\pi\varepsilon_i}})}{kT}\right]$ (4.42)
Frenkel-Poole emission	$J = qN_c\mu E_iexp\left[\frac{-q(\phi_t-\sqrt{\frac{qE_i}{\pi\varepsilon_i}})}{kT}\right]$ (4.43)
Ohmic conduction	$J \propto E_iexp\left(\frac{-\Delta E_{ac}}{kT}\right)$ (4.44)
Ionic conduction	$J \propto \frac{E_i}{T}exp\left(\frac{-\Delta E_{ai}}{kT}\right)$ (4.45)

Table 4.2: Basic conduction mechanisms in insulators [1]. (m = effective mass in the semiconductor, m_{ox} = effective electron mass in the insulator, $A^{\star\star}$ = effective Richardson constant, ε_i = insulator permittivity, ϕ_B = barrier height, ΔE_{ac} = activation energy of electrons, ΔE_{ai} = activation energy of ions, μ = electron mobility in the insulator, $\hbar$ = reduced Planck constant, ϕ_t = trap energy level, $C_t = \left(\frac{m_{poly}}{m_{ox}}\right)^{\frac{5}{2}}\frac{8E_1^{\frac{3}{2}}}{3\hbar\sqrt{\phi_t-E_1}}$, $D = \frac{4\sqrt{2qm_{ox}}}{3\hbar}$, E_1 = total energy of the electron in the metal, N_t = trap concentration in insulator.)

4.6 Issues with the SiC/dielectric interface and the impact of process variation

In this section the room temperature characteristics of each of the dielectrics on both n-type and p-type 4H-SiC will be extracted and compared.

4.6.1 Comparison of the impact of the variation in dielectric formation on the n-type MIS capacitor characteristics

Table 4.3 shows the extracted parameters for each of the n-type test samples HV06, CR25 and CR27. The insulator capacitance was extracted from the C-V characteristics in accumulation that were measured at a frequency of 1 MHz and corrected for series resistance. Flatband voltage (V_{FB}) was extracted from the C-V characteristics as described in section 4.5 using Equation 4.28 and 4.29. t_{i} represents the equivalent oxide thickness that was extracted for each of the samples using Equation 4.26 once C_{i} was extracted from the measured results. The relative permittivity of SiO_2 was used to perform the calculation. As shown in Table 4.3 HV06 had a much lower equivalent oxide thickness than the other 2 samples, CR25 and CR27, which had a comparable t_{i} and were approximately equal to the physical dielectric thicknesses that were extracted by Raytheon UK using ellipsometry data during fabrication, which were outlined in Table 4.1 of 40 and 45 nm, respectively. The low equivalent oxide thickness of HV06 which was extracted from the characteristics could be caused by the impact of the HCl/O_2 post oxidation anneal step that was outlined in Table 4.1, which may have acted to modify the relative permittivity of the oxide or the physical oxide thickness and therefore acts to reduce the equivalent oxide thickness. The fact that the extracted equivalent oxide thickness of the p-type HV06 MIS sample also exhibits a similar value, as shown in Table 4.4, suggests that the low equivalent oxide thickness is a product of the dielectric formation and post oxidation process as this is consistent for both the n-type and p-type samples which were fabricated monolithically on a single 4H-SiC wafer.

Sample	**Measured V_{FB} [V]**	**Theoretical V_{FB} [V]**	**C_i [$nF.cm^{-2}$]**	**t_i [nm]**	**N_D [cm^{-3}]**
HV06	3.12 $\pm$0.03	1.48	114 $\pm$1.14	30.31 $\pm$0.30	1.58×10^{17} $\pm3.16\times10^{15}$
CR25	1.90 $\pm$0.02	1.38	75.7 $\pm$0.76	45.59 $\pm$0.46	3.44×10^{15} $\pm$ 6.88×10^{13}
CR27	1.25 $\pm$0.01	1.42	75.2 $\pm$0.75	45.94 $\pm$0.46	1.70×10^{16} $\pm$ 3.40×10^{14}

Table 4.3: Extracted parameters of the n-type HV06, CR25 and CR27 MIS samples measured at room temperature.

The large variation of the extracted doping concentrations for each of the samples could be attributed to an unoptimised ion implantation doping procedure as all of the n-type structures were formed in implanted regions as outlined in section 4.4. The variation in doping concentration across the epitaxial layer of the original wafer is also a contributing factor to this as the Cree wafers used in this study have a doping tolerance of $\pm50\%$ across the wafer

[42].

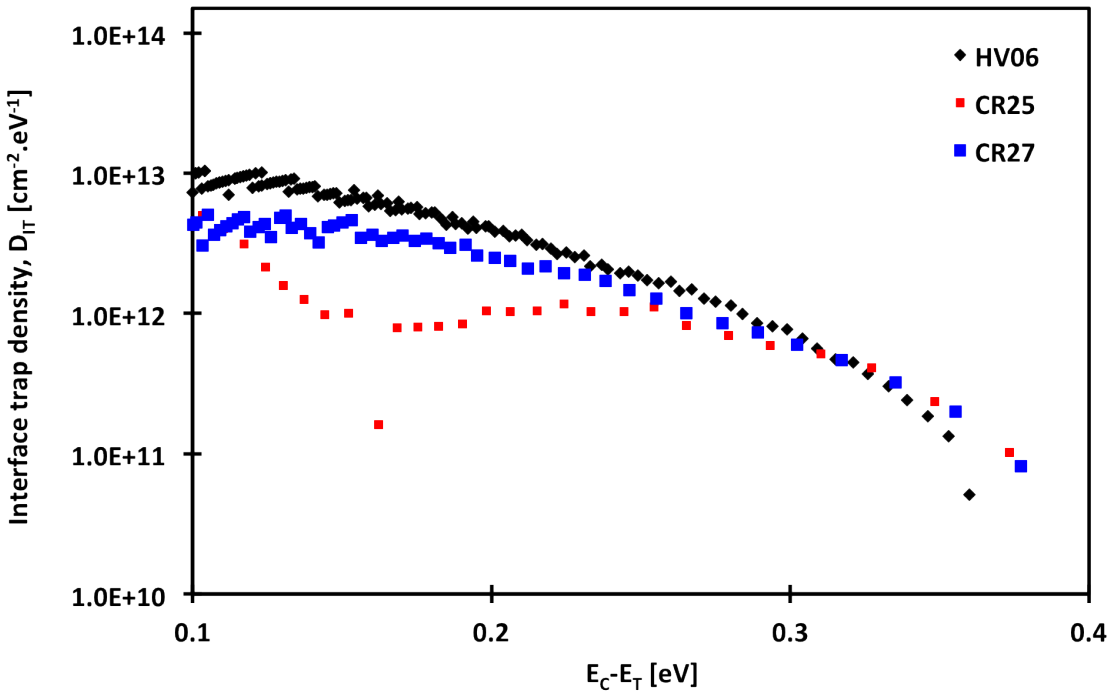


Figure 4.6: Interface trap density as a function of energy at 298 K for the HV06, CR25 and CR27 n-type MIS capacitor structures.

The data in Figure 4.6 show the interface trap density between 0.1 and 0.4 eV from the conduction band edge of the 4H-SiC band gap for each of the samples, which was extracted using the high frequency C-V technique, as outlined in Equation 4.35. As the energy level approaches the conduction band edge it can be seen that HV06 has the highest density of interface traps followed by CR27 and then CR25. All of the devices exhibit a similar interface trap distribution across the energy range and show a rise in D_{it} as the conduction band edge is approached as seen in other reports [120][105][104]. However, CR25 shows a reduction in D_{it} at 0.15 eV below the conduction band edge, which could suggest that traps at this energy level have been passivated in some way during the dielectric growth and post oxidation treatment. This reduction could be attributed to the $POCl_3$ anneal at 1000 ^oC described in Table 4.1as a similar effect was observed in a previous study by Okamoto *et al.* [119].

4.6.2 Comparison of the impact of the variation in dielectric formation on the p-type MIS capacitor characteristics

The data in Table 4.4 show the extracted parameters for each of the p-type test samples HV06, CR25 and CR27. The insulator capacitance was extracted from the C-V characteristics in accumulation that were measured at a frequency of 1 MHz and corrected for series resistance. Flatband voltage (V_{FB}) was extracted from the C-V characteristics as described

in section 4.5 using Equation 4.28 and 4.29. t_{i} represents the equivalent oxide capacitance that was extracted for each of the samples using Equation 4.26 once C_{i} was extracted from the measured results. The relative permittivity of SiO_2 was used to perform the calculation. As shown in Table 4.4 there is a large variation between the equivalent oxide thicknesses for each of the samples. HV06 exhibits the lowest t_{i} of 33 nm, CR25 has a t_{i} of 42 nm and CR27 has an equivalent oxide thickness of 51 nm. The physical thickness as described for each in Table 4.1 that was extracted by Raytheon UK using ellipsometry data during fabrication was 40 nm, 40 nm and 45 nm for HV06, CR25 and CR27, respectively. As both the n and p-type HV06 MIS capacitor samples demonstrated consistently low equivalent oxide thicknesses this suggests that this is a product of the HCl/O_2 post oxidation annealing treatment as discussed in subsection 4.6.1, which acts to modify the dielectric permittivity of the HV06 dielectric.

There is a large difference between $\mathrm{V_{FB}}$ of each of the devices, which is shown by the data in Table 4.4. This variation is a result of the different dielectric processing treatments that were discussed in Table 4.1 and highlights that the different techniques can cause a variation in the charge present within the oxide, which is a combination of $\mathrm{Q_f}$, $\mathrm{Q_m}$ and $\mathrm{Q_{ot}}$ and can have a significant impact on $\mathrm{V_{FB}}$ as shown in Equation 4.46. The oxide charge ($\mathrm{Q_f}$+$\mathrm{Q_m}$+$\mathrm{Q_{ot}}$) in each of the devices is estimated to be $4.64 \times 10^{12}\,\mathrm{cm^{-2}}$, $1.38 \times 10^{13}\,\mathrm{cm^{-2}}$ and $5.19 \times 10^{12}\,\mathrm{cm^{-2}}$ for HV06, CR25 and CR27, respectively calculated from V_{FB}, which was extracted from the measured C-V characteristics. This analysis could infer that the large $\mathrm{V_{FB}}$ witnessed in sample CR25 is due to the increased oxide charge that is present within the dielectric compared to both HV06 and CR27, which have a very similar oxide charge. This could be due to the oxide formation process. Both HV06 and CR27 have a thermally grown dielectric layer at the SiO_2/4H-SiC interface, whereas CR25 is a deposited oxide. This would also suggest that a thermally grown oxide produces a higher quality interface on 4H-SiC, which supports previously reported results that demonstrated that a thin thermally grown film of SiO_2 at the interface produced a significant improvement in the breakdown field and a reduction in $\mathrm{V_{FB}}$ of 4H-SiC MIS devices [184].

The observed variation in the extracted doping concentrations for the p-type MIS samples, as shown by the data in Table 4.4, is smaller than for the equivalent n-type samples which were shown by the data in Table 4.3 and the values measured are much closer to the expected levels than those of their n-type counterparts.

Figure 4.7 shows the interface trap density across the bandgap for each of the samples. As the energy level approaches the valence band edge it can be seen that CR27 has the highest density of interface traps followed by CR25 and then HV06, although they all show a comparable proportion and distribution of interface traps across the band gap. This suggests that the variation in dielectric between the samples has very little impact on the proportion of

Sample	Measured V_{FB} [V]	Theoretical V_{FB} [V]	C_i [nF.cm^{-2}]	t_i [nm]	N_A [cm^{-3}]
HV06	-7.90 ±0.08	-1.47	105±1.1	32.85 ±0.33	$1.33\times10^{17} \pm 2.34\times10^{15}$
CR25	-26.65 ±0.27	-1.52	83.1 ±0.83	41.53 ±0.42	$4.33\times10^{17} \pm 8.66\times10^{15}$
CR27	-10.95 ±0.11	-1.48	67.8 ±0.68	50.90 ±0.51	$1.17\times10^{17} \pm 2.34\times10^{15}$

Table 4.4: Extracted parameters of the p-type HV06, CR25 and CR27 MIS samples measured at room temperature.

interface traps at the valence band edge in the p-type MIS structures.

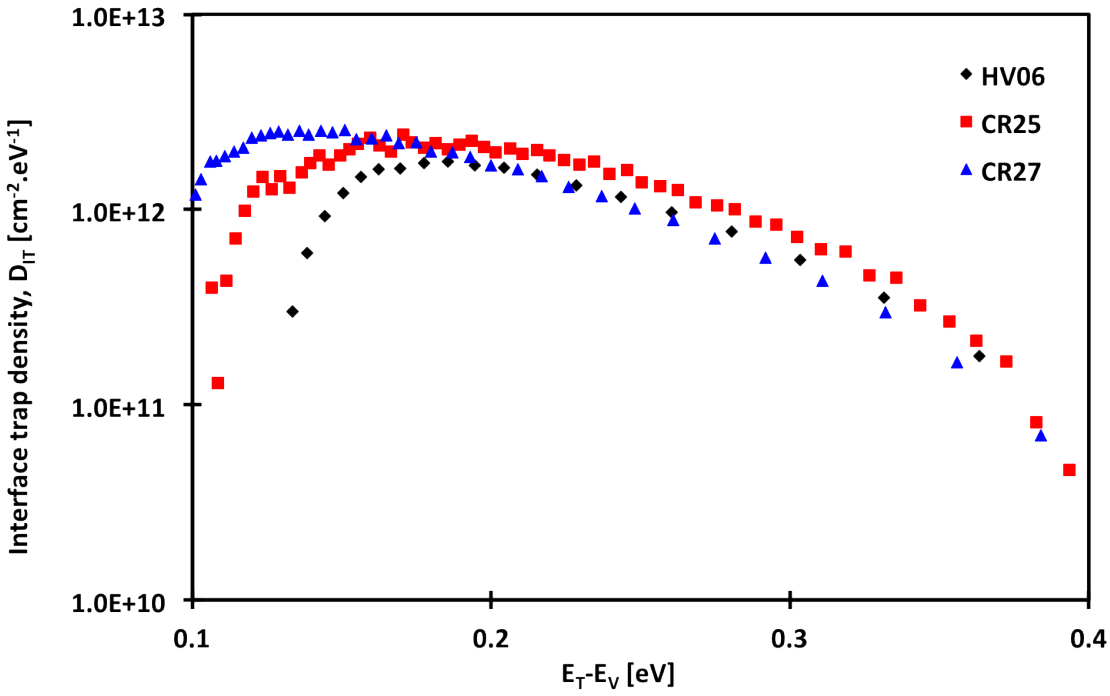


Figure 4.7: Interface trap density as a function of energy at 298 K for the HV06, CR25 and CR27 p-type MIS capacitor structures.

4.7 Impact of elevated temperature operation on the MIS system

The temperature dependence of the electrical characteristics of each of the dielectrics on both n-type and p-type 4H-SiC will be examined in this section in order to examine the impact of dielectric process variation on the operation of the MIS structures at elevated temperatures.

4.7.1 Temperature dependent characteristics of n-type MIS capacitors

Capacitance density-voltage measurements were conducted at 1 MHz on each of the n-type samples, HV06, CR25 and CR27 between 298 K and 498 K and the results, after the series resistance correction was performed as discussed in section 4.5, are shown in Figure 4.8, 4.9 and 4.10, respectively.

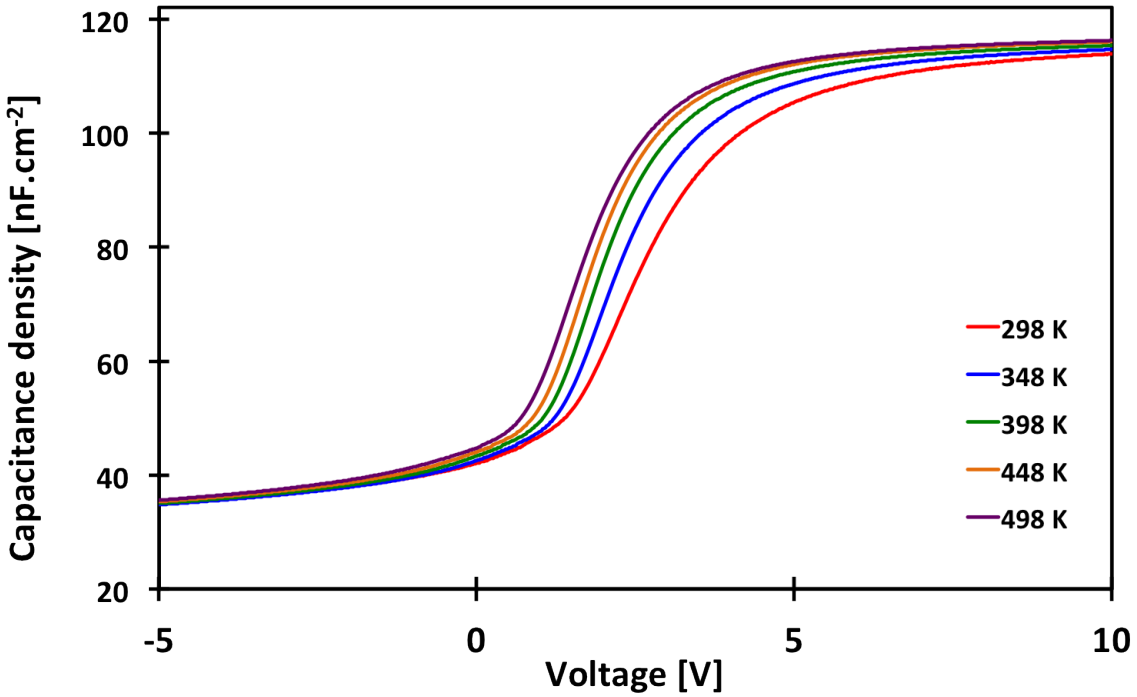


Figure 4.8: Capacitance density-Voltage characteristics for a HV06 n-type MOS capacitor from 298 K to 498 K measured at 1 MHz.

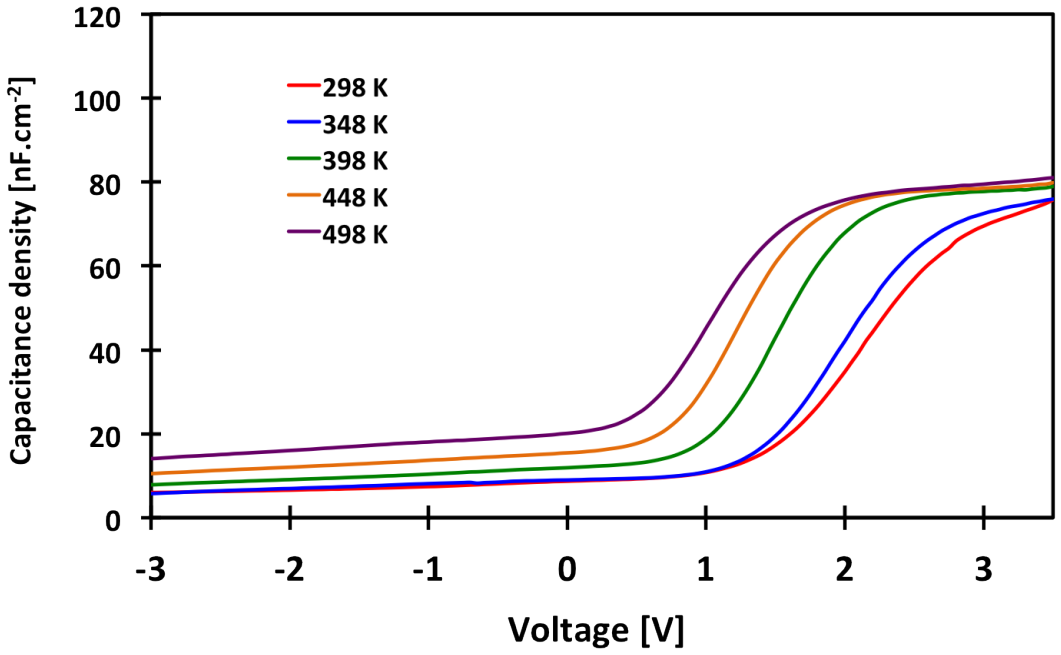


Figure 4.9: Capacitance density-Voltage characteristics for a CR25 n-type MOS capacitor from 298 K to 498 K measured at 1 MHz.

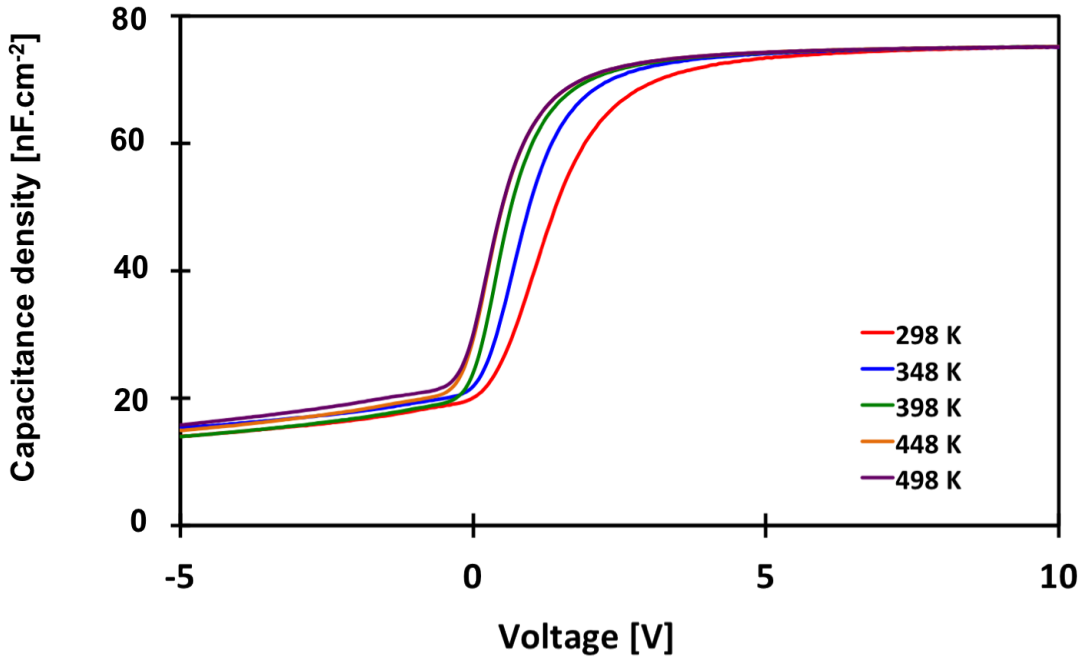


Figure 4.10: Capacitance density-Voltage characteristics for a CR27 n-type MOS capacitor from 298 K to 498 K measured at 1 MHz.

The flatband voltage at each temperature was extracted using the method discussed in section 4.5 using Equation 4.28 and Equation 4.29. Figure 4.11 shows V_{FB} as a function of temperature for each of the samples. As shown in the data, all of the samples exhibit the same trend with temperature and the flatband voltage reduces towards 0 V as the temperature increases. A theoretical expression for flatband voltage is given in Equation 4.46,

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_i} \tag{4.46}$$

where ϕ_{ms} is the metal-semiconductor work function difference, Q_f is the fixed oxide charge, Q_m is the mobile oxide charge within the oxide, Q_{ot} is the oxide trapped charge, and C_i is the insulator/oxide capacitance. ϕ_{ms} is calculated using Equation 4.47.

$$\phi_{ms} = \phi_m - \left(\chi + \frac{E_g}{2q} + \phi_B\right) \tag{4.47}$$

From Equation 4.46 and 4.47 it can be inferred that the change in V_{FB} over the temperature range can be influenced by the changes in ϕ_B, the oxide charges that are present (Q_f, Q_m, Q_{ot}), the insulator capacitance (C_i), the change in electron affinity (χ) and the change in bandgap energy (E_g). As several of the components within Equation 4.47 should be consistent between all 3 samples such as E_g, χ and ϕ_m as the process technique and semiconductor used was consistent between all 3 samples any difference in V_{FB} between the samples can be attributed to the oxide charge.

As all of the samples exhibit a similar trend this suggests that the main contributing factors are ϕ_B and E_g as the charges present within each sample are likely to differ more dramatically between each of the dielectrics as they have all undergone very different process conditions, however variations in trapped charge across the measured temperature range could also be a contributing factor. The band gap energy (E_g) and intrinsic carrier concentration (n_i) are temperature dependent as shown by the data in Figure 2.3. E_g decreases with increasing temperature and n_i increases with increasing temperature due Boltzmann statistics due to an increase in the density of states in the conduction and valence bands with increasing temperature, respectively. Theoretical values in 4H-SiC can be calculated using the semi-empirical formula below as quoted from [185]:

$$n_i = \sqrt{N_V N_C} exp\left(\frac{-qE_g}{2kT}\right) \tag{4.48}$$

$$E_g = E_g(0) - (0.00065)(\frac{T^2}{T + 1300}) \tag{4.49}$$

where N_C and N_{V} are the effective density of states in the conduction band and valence band, respectively, and can be calculated using Equation 4.50 and 4.51 for 4H-SiC [185].

$$N_C = 3.25\text{x}10^{15}(T^{\frac{3}{2}}) \tag{4.50}$$

$$N_V = 4.8\text{x}10^{15}(T^{\frac{3}{2}}) \tag{4.51}$$

ϕ_{B} varies with temperature as it is directly proportional to $\frac{kT}{q}$ and $ln(\frac{N_D}{n_i})$. The extracted doping concentration does not vary greatly over the entire scanned temperature range as shown in Figure 4.12. This suggests that the change in V_{FB} with temperature is dominated by the change in E_g and the change in n_{i}, however variations in trapped charge across the measured temperature range could also be a contributing factor.

The large variation in doping concentration shown by the data in Figure 4.12 and the variation in oxide capacitance will be a contributing factor to the offset between V_{FB} of each of the samples. The variation in doping concentration could be a product of the ion implantation doping procedure as discussed in subsection 4.6.1 or a consequence of the variation of the doping concentration of the epitaxial layer of each of the 4H-SiC wafers which the devices were fabricated within, which acts to compensate the implanted donors.

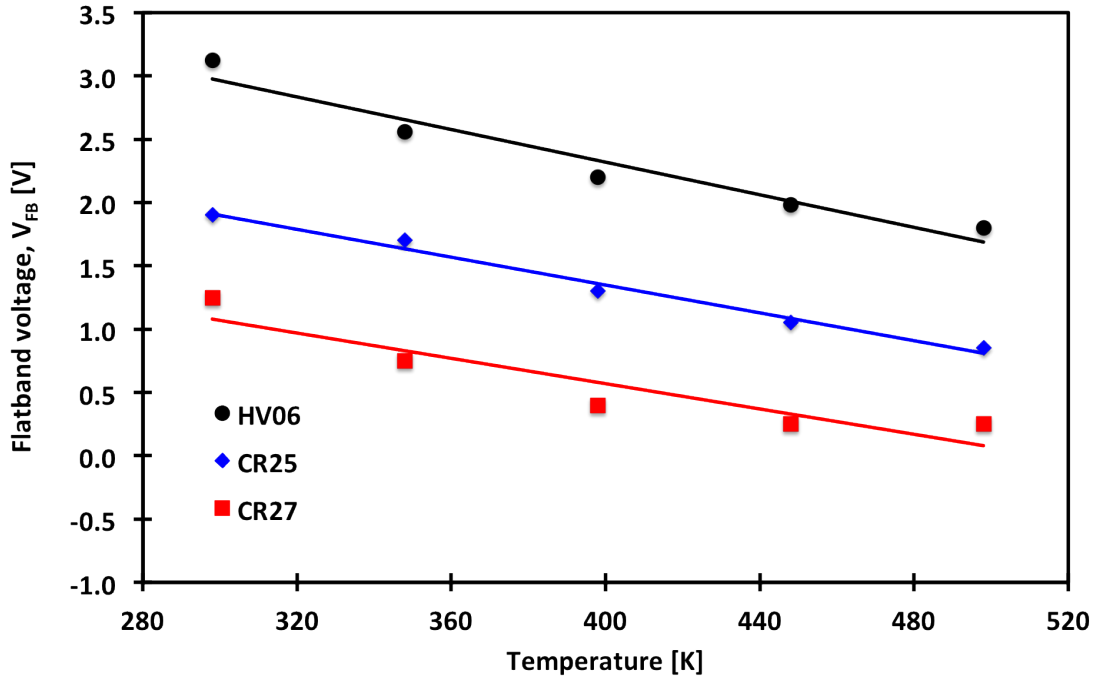


Figure 4.11: Flatband voltage as a function of temperature for HV06, CR25 and CR27 n-type MIS capacitors. Measurement error is smaller than the data points.

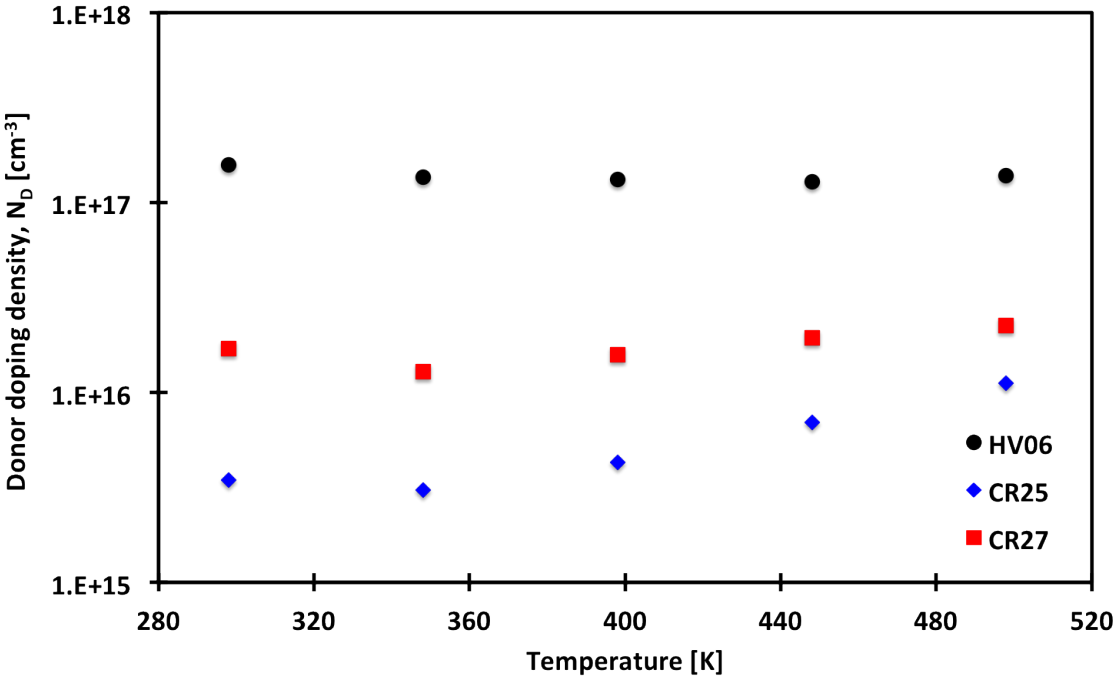


Figure 4.12: Donor doping density as a function of temperature for HV06, CR25 and CR27 n-type MIS capacitors. Measurement error is smaller than the data points.

As shown by the data in Figure 4.8, 4.9 and 4.10 the extracted oxide capacitances are constant over the scanned temperature range for HV06 and CR27, however, CR25 shows an increase in oxide capacitance with temperature. This suggests that a physical change occurs within the dielectric at elevated temperatures, which modifies either the dielectric permittivity or the dielectric thickness. This physical change could also be contributing to the extracted doping concentration in Figure 4.12 as an increase in N_D with temperature was observed for CR25.

Interface trap density as a function of energy level within the bandgap was also extracted across the measured temperature range for each of the samples using the Terman method, using Equation 4.35, as discussed in section 4.5 [182]. The Terman method was used in this investigation due to the ease and speed of extraction as it is used mainly for comparison between the 3 samples. As can be seen in Figure 4.13 and 4.15, both HV06 and CR27 show a reduction in D_{it} close to the band edge as the temperature increases. However, for sample CR25, the data in Figure 4.14 show the opposite phenomena and an increased D_{it} is observed with increasing temperature across the measured energy range. This suggests that the interface trapped charge has a temperature dependence and become electrically active at elevated temperatures. This could also suggest that the traps are mobile at the interface or have varying time constants, so only begin to interact with the semiconductor carriers at elevated temperatures. This could be a product of mobile charge in the oxide that is close to the interface, which could have been introduced to the oxide during the post oxidation treatments

as outlined in Table 4.1. The decrease in density of interface traps at the conduction band edge with an increase in temperature supports observations from previous work and is due to the bandgap narrowing effect as temperature increases [186]. As the conduction band moves closer to the valence band with increasing temperature the density of interface traps at the conduction band edge reduces. This is also in agreement to the trend that is witnessed in the Si-SiO_2 MIS system [187].

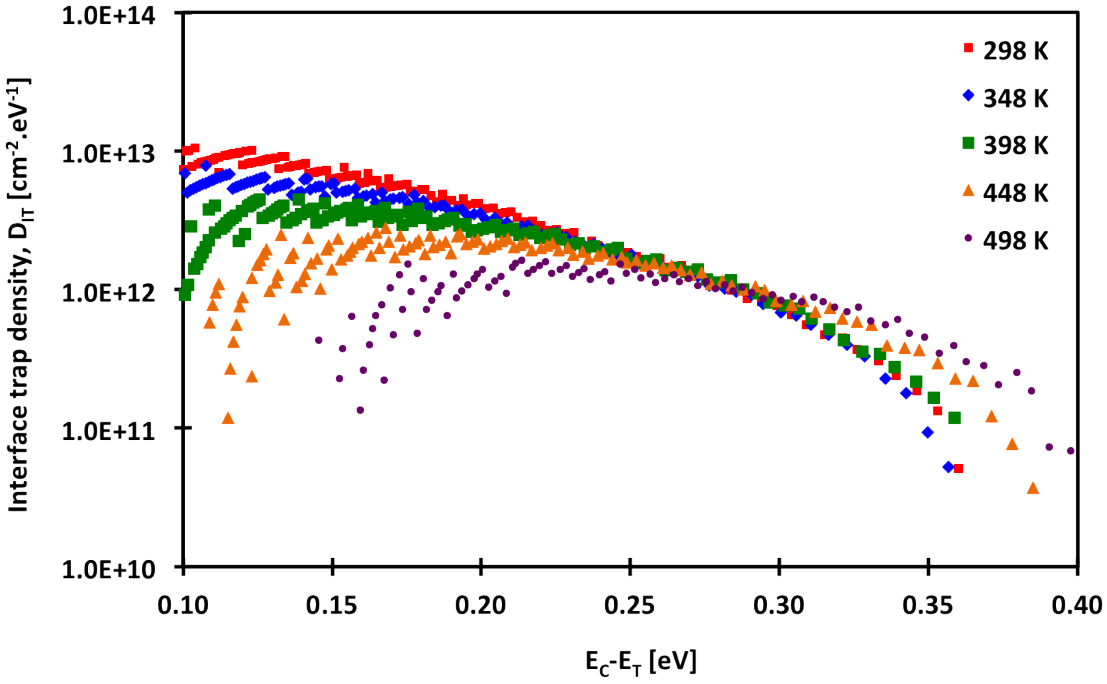


Figure 4.13: Interface trap density as a function of energy at varying temperatures for the HV06 n-type MIS capacitor structure.

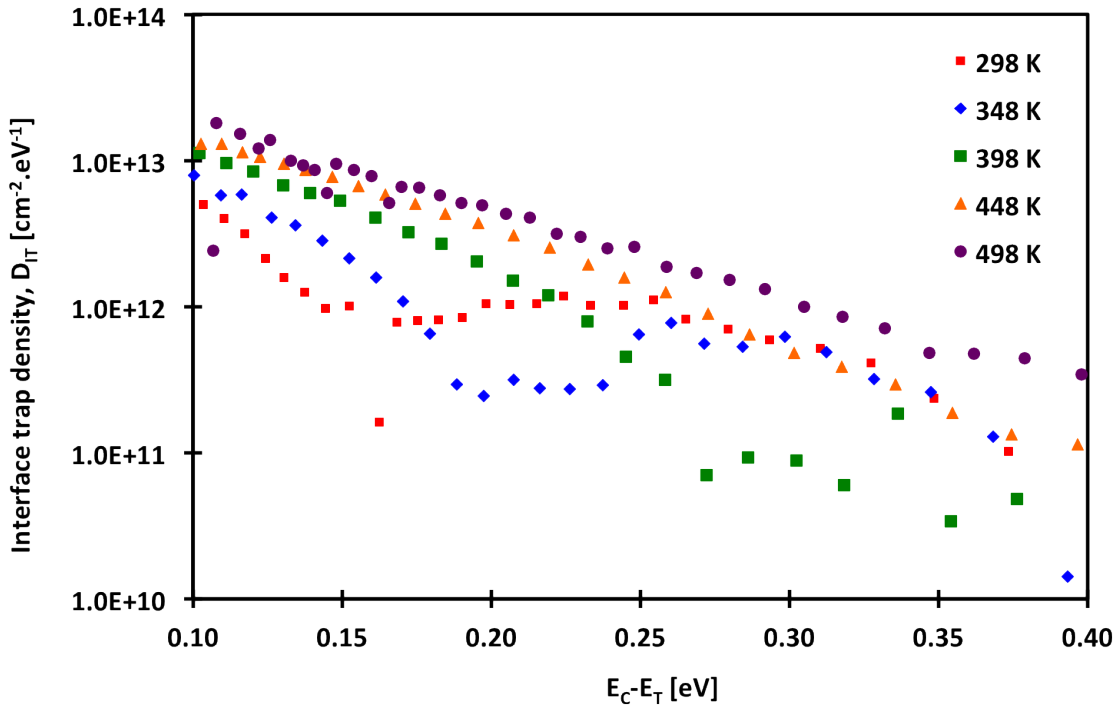


Figure 4.14: Interface trap density as a function of energy at varying temperatures for the CR25 n-type MIS capacitor structure.

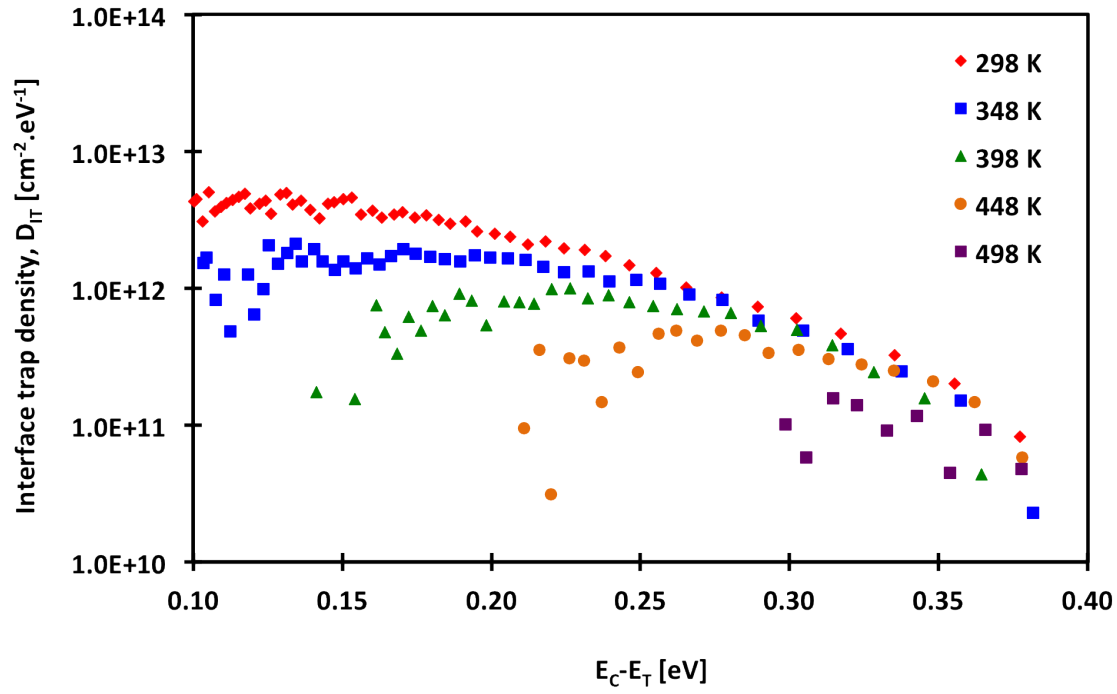
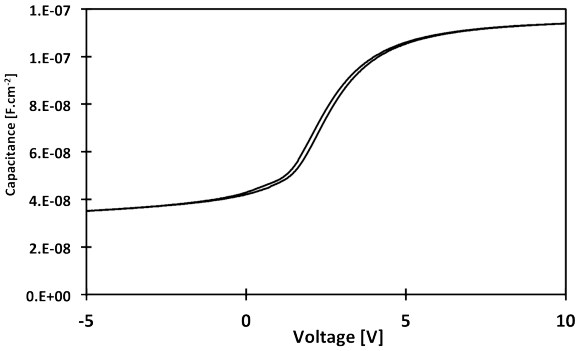
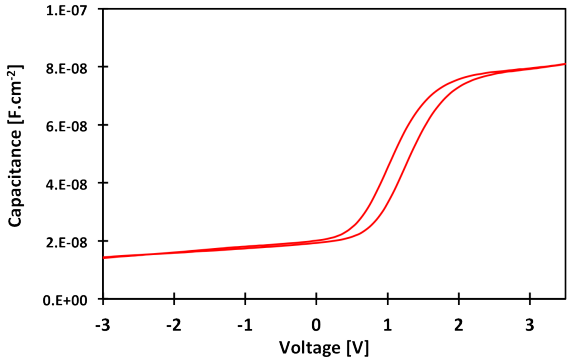


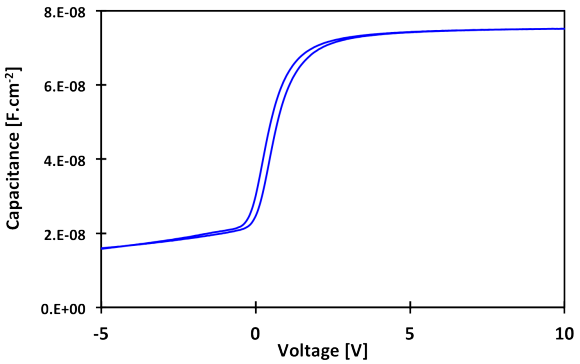
Figure 4.15: Interface trap density as a function of energy at varying temperatures for the CR27 n-type MIS capacitor structure.



(a) HV06 n-type MIS capacitor.

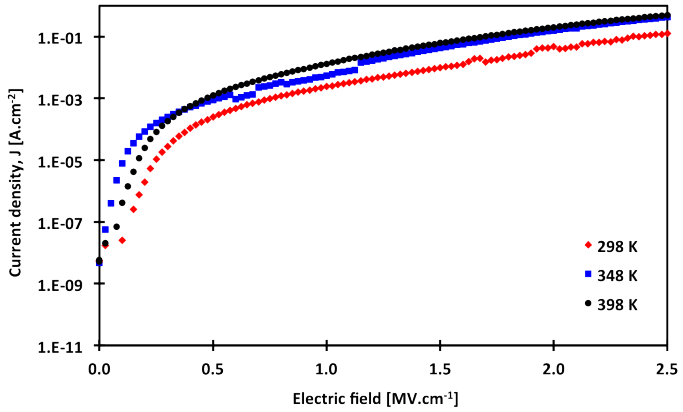


(b) CR25 n-type MIS capacitor.

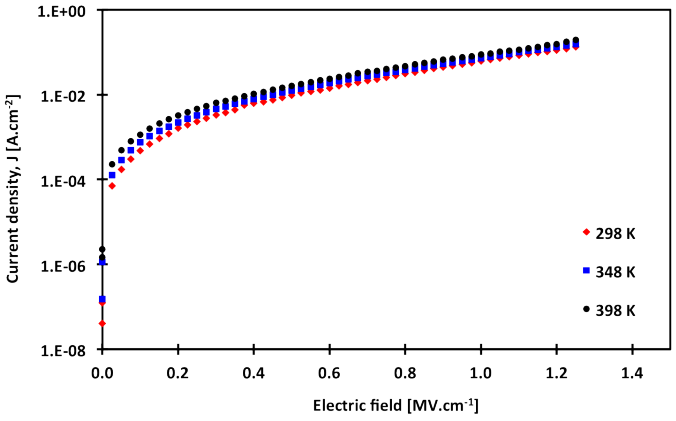


(c) CR27 n-type MIS capacitor.

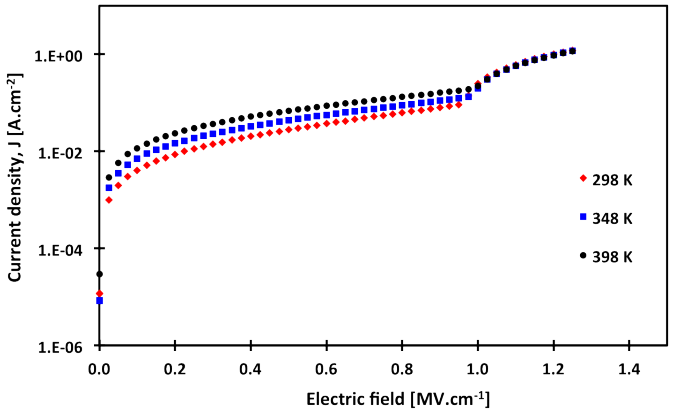
Figure 4.16: Forward and reverse sweep C-V characteristics taken at a temperature of 498 K and a frequency of 1 MHz to show the C-V hysteresis and the presence of mobile and oxide trapped charge in the gate dielectric of n-type MIS capacitors. A different measurement range was implemented for CR25 as the sample reached breakdown at voltages beyond 3 V so higher measurements were not possible.



(a) HV06 n-type MIS capacitor.



(b) CR25 n-type MIS capacitor.



(c) CR27 n-type MIS capacitor.

Figure 4.17: Current density (J) against electric field (E_{i}) for the 3 dielectrics (HV06, CR25, CR27) on n-type 4H-SiC for a range of temperatures (298 K, 348 K and 398 K).

A hysteresis test was conducted on each of the samples to examine the presence of mobile charge within each of the dielectrics. Each device was heated to 498 K and was swept from accumulation to inversion and back again. The results are shown in Figure 4.16a, 4.16b and 4.16c for HV06, CR25 and CR27, respectively. The change in flatband voltage (ΔV_{FB})

for each of the devices was extracted from the measured results using Equation 4.28. There was a minimal shift for the HV06 n-type MIS sample and ΔV_{FB} was extracted to be 0.02 V. The CR25 n-type MIS sample exhibited the largest shift with ΔV_{FB} equal to 0.35 V. ΔV_{FB} extracted for the CR27 n-type MIS sample was 0.25 V. The results are in agreement with the observation that CR25 contains the highest combination of mobile oxide charge (Q_{M}) and oxide trapped charge (Q_{OT}) as $Q_M = -C_{OX}\Delta V_{\mathrm{FB}}$ and $Q_{OT} = -C_{OX}\Delta V_{\mathrm{FB}}$ [168]. The results equate to a combined Q_{M} and Q_{OT} for each of the devices of $2.3 \times 10^{10}\,\mathrm{cm}^{-2}$, $2.7 \times 10^{11}\,\mathrm{cm}^{-2}$ and $1.9 \times 10^{11}\,\mathrm{cm}^{-2}$ for HV06, CR25 and CR27, respectively. This suggests that the dielectric processing conditions implemented to form CR25 produce the highest amount of mobile oxide charge and oxide trapped charge out of the three examined techniques that were outlined in Table 4.1.

Conduction mechanisms in n-type 4H-SiC MIS capacitors

I-V characterisation was performed to examine the conduction mechanisms in each of the MIS capacitor samples. The variation in the leakage current density of each of the samples under positive gate biases at different temperatures is shown by the data in Figure 4.17. The current density observed in CR25 (Figure 4.17b) and CR27 (Figure 4.17c) is 1 to 2 orders of magnitude higher than that of HV06 Figure 4.17a at electric fields below 1 MV.cm^{-1}. This difference may be explained by a difference in the effective barrier height values of each of the 3 dielectrics, which is linked to the difference in growth conditions and post oxidation treatments. The results in Figure 4.17 also show that very little temperature dependence is exhibited in the condcution mechanisms of each of the dielectrics shown.

The current conduction mechanisms as outlined in Table 4.2 dominate over a specific range of applied electric field. Certain conduction processes can dominate in certain temperature and electric field ranges and may not be independent of one another [1]. Several mechanisms have been reported to explain the observed characteristics of conduction in insulators as summarised in Table 4.2. In order to understand the conduction behaviours of the 3 samples under examination in this thesis the log(J)-log(E) characteristics of each of the samples at room temperature are given in Figure 4.18. This data set clearly exhibits distinguishable regions, which shows that different contributing mechanisms are dominating in different regions of the applied electric field.

To establish the conduction mechanisms that dominate the characteristics of each of the samples at different electric fields the results can be compared to the theoretical conduction mechanisms that were outlined in Table 4.2. It has previously been reported that at lower and intermediate perpendicular electric fields that conduction in SiO_2 on 4H-SiC can be dominated by trap assisted tunnelling as described in Equation 4.40 [139]. Trap assisted tunnelling is the phenomenon when charge moves through defect energy levels in the oxide

by a capture emission process or by a hopping mechanism. Equation 4.40 can be rearranged to form:

$$ln(JE) = (-D\phi_t^{\frac{3}{2}})(\frac{1}{E}) + ln(\frac{2}{3}qC_tN_t\phi_t) \tag{4.52}$$

Therefore, a plot of ln(JE) vs 1/E will allow the energy of the trap (ϕ_t) and the trap concentration in the oxide (N_t) to be estimated from the slope and intercept of the plot, respectively. A plot of ln(JE) vs 1/E is shown for each of the samples in Figure 4.19. C_t (sometimes referred to as the trap energy dependent rate constant) is a parameter associated with the effective masses of electrons in SiC and in the insulator, total energy of an electron, reduced Planck's constant ($\hbar$), barrier height between SiC and the insulator and this parameter is approximated to 1 [139] [188] and the effective electron mass in the insulator (m_{ox}) was assumed to be equal to 0.42 m_0 [139]. A linear region was observed between 0.33 and 0.75 MV.cm^{-1} for each of the samples. The trap energy level (ϕ_t) for each of the samples was extracted from Figure 4.19 and was 0.13 eV, 0.10 eV and 0.08 eV for HV06, CR25 and CR27, respectively. The trap concentration in each of the samples was 3.54×10^{22} cm^{-3}, 2.07×10^{21} cm^{-3} and 1.64×10^{21} cm^{-3} for HV06, CR25 and CR27, respectively. The reported values are 2-3 orders of magnitude greater than values that have been reported for thermally grown SiO_2 on 4H-SiC in varying N_2O ambients, which suggests that the high leakage of the dielectrics under investigation in this study is likely to be due to the increased concentration of traps at relatively low trap energy levels that act to dominate the conduction mechanisms through the insulator [138]. This unrealistically high level of traps, which is higher than the molecular density of SiO_2 (2.3×10^{22} cm^{-3}) suggests that the defects are more complicated than a simples single charge state and may be a contribution of multiple defects in the dielectric[189].

At high electric fields it has been identified that the conduction mechanism that limits current transport is Fowler-Nordheim tunnelling [190] [191]. The Fowler-Nordheim tunnelling mechanism is described by Equation 4.41. A linear trend in a plot of ln(J/E^2) vs 1/E would indicate the presence of a Fowler-Nordheim tunnelling mechanism, however, in this study no linear trends were identified in the data sets, which suggests that Fowler-Nordheim is not a dominant conduction mechanism through any of the dielectrics used in this investigation.

Another contributing mechanism that has previously been discussed is Frenkel-Poole emission, which is the term used to describe the field enhanced thermal excitation of electrons trapped inside the dielectric at an effective average energy of ϕ_t and is calculated using Equation 4.43 [1]. Rearranging Equation 4.43 shows that by plotting ln(J/E) vs $\sqrt{E}$ a linear curve fitting on the data will identify that Frenkel-Poole emission is the dominant conduction mechanism within the insulator. Equation 4.43 is rearranged to form:

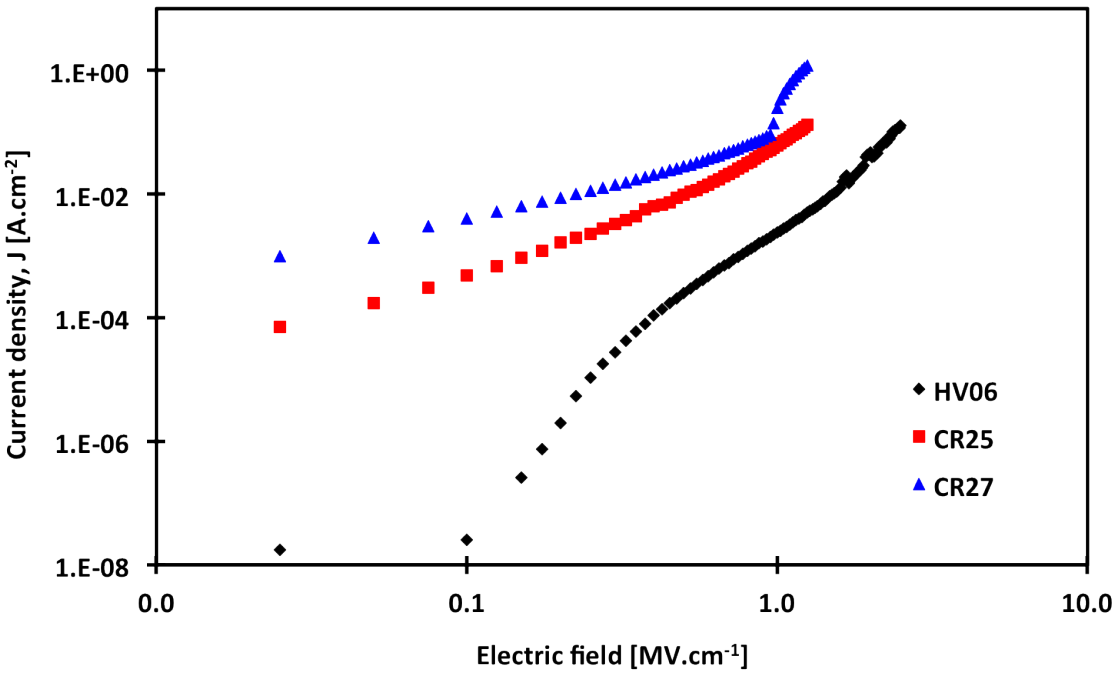


Figure 4.18: Current density (J) against electric field (E_{i}) for the 3 dielectrics samples (HV06, CR25, CR27) measured in accumulation at 298 K.

$$ln(J/E) = \frac{q}{kT}\sqrt{\frac{q}{\pi\varepsilon_0\varepsilon_r}}\sqrt{E} - \frac{q\phi_t}{kT} + ln(q\mu N_c) \tag{4.53}$$

Figure 4.20 shows a plot of ln(J/E) vs $\sqrt{E}$ for each of the samples. A linear trend is observed for each of the oxides between 0.5 and 1.7 MV.cm^{-1} and 2 different linear trends are shown for CR27 (please note the discontinuity of the CR27 data is due to the fact that only the linear trends were plotted in the figure. Data points do exist between the 2 trends, however, they have been excluded from this figure as only analysis of the linear parts of the curve were relevant for this analysis technique.), which suggests that 2 different mechanisms or trap levels are present within the CR27 dielectric. It is also important to note that all of the linear fitted trends reported in this investigation had correlation coefficients of greater than 0.98, which highlights that the characteristics showed extremely strong linear trends in the examined electric field regions. The relative permittivity of the dielectric (ε_r) and the trap energy level (ϕ_{t}) can be extracted from the gradient and the intercept, respectively. However, without an accurate knowledge of the electron mobility in the insulator it is not possible to extract the trap energy level. However, after implementing this technique the extracted relative permittivities for each of the dielectrics are 42.9 for HV06, 48.7 for CR25 and 14.9 for CR27, which are all an order of magnitude higher than the relative permittivity of SiO_2, which has previously been reported as between 2.4 and 4 for the 4H-SiC MOS system [192]. This suggests that Frenkel-Poole emission cannot be responsible for the extracted

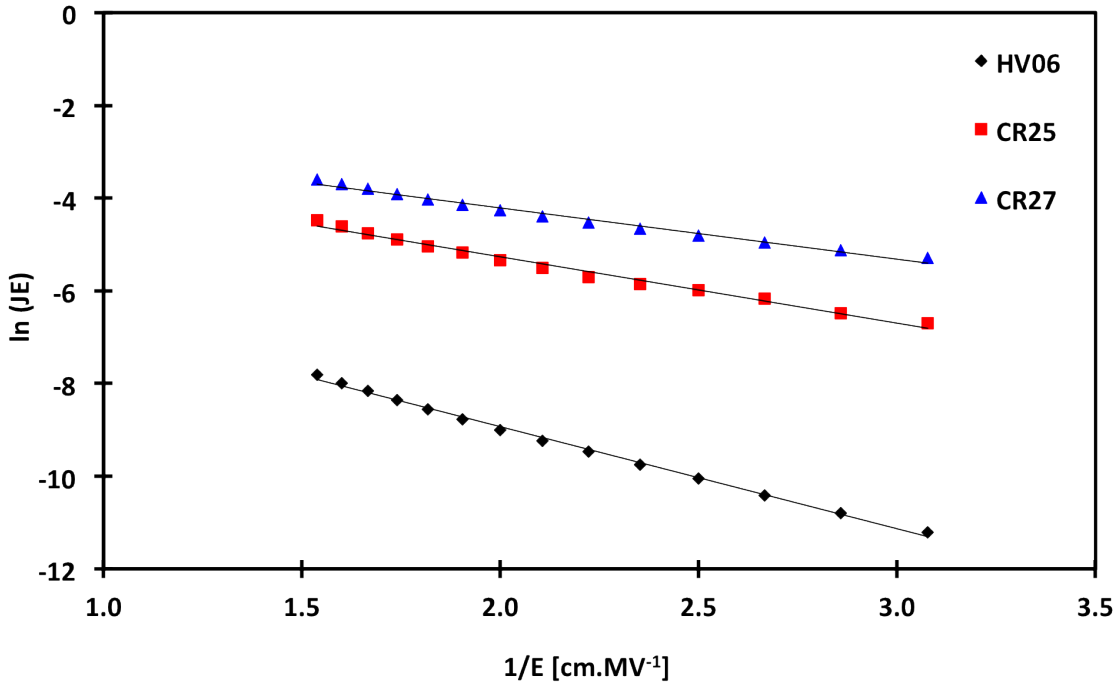


Figure 4.19: Trap assisted tunnelling plot schematic of the 3 n-type MIS capacitors at 298 K.

linear curves in this investigation. The observed trend could be due to another mechanism such as trap assisted tunnelling or Ohmic conduction.

4.7.2 Temperature dependent characteristics of p-type MIS capacitors

Capacitance density-voltage measurements were conducted at 1 MHz on each of the p-type samples, HV06, CR25 and CR27 between 298 K and 498 K and the results, after the series resistance correction was performed as discussed in section 4.5, are shown in Figure 4.21, 4.22 and 4.23, respectively. Each of the samples exhibit a constant oxide capacitance across the measured temperature range as shown in Figure 4.21, 4.22 and 4.23.

As with the n-type MOS capacitors in subsection 4.7.1 as the temperature increases all of the p-type MIS samples show a similar trend and V_{FB} shifts closer towards 0 V as shown in Figure 4.24. This shift in V_{FB} is due to the impact of the elevated temperature on the band gap of the 4H-SiC, the change in the intrinsic carrier concentration as discussed in subsection 4.7.1 and the change in charges at the interface and in the oxide across the measured temperature range.

However, as shown in Figure 4.25, there is a small variation of N_{A} between each of the samples and across the measured temperature range in each sample. The greatest change is seen in sample CR25, which shifts from a value of approximately 4.5×10^{17} cm^{-3} at 298 K to 3×10^{17} cm^{-3} at 498 K. This reduction could be attributed to an increased ionisation of the

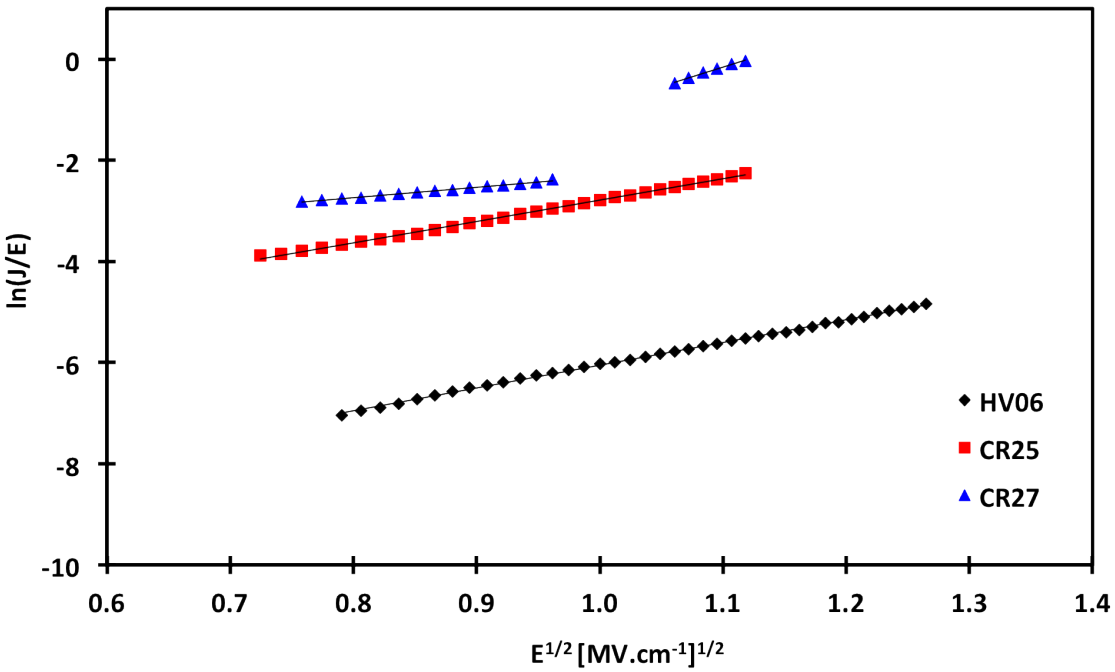


Figure 4.20: Frenkel-Poole emission plot for the 3 dielectric n-type MIS capacitors at 298 K.

nitrogen dose that is implanted for the threshold adjust implant that will be discussed further in section 4.8.

The increase of acceptor doping concentration witnessed in both CR25 and CR27 could be a product of an increased degree of ionisation of acceptor dopants at increased temperatures. As discussed in subsection 2.4.3, the degree of ionisation in p-type 4H-SiC doped with aluminium at room temperature is relatively low due to the deep acceptor level of the dopant, which is shown in Table 2.3. As temperature increases the degree of ionisation of the acceptor increases. For example at 298 K with an aluminium doping concentration of $1 \times 10^{17}\,\mathrm{cm}^{-3}$ the degree of ionisation is less than $10\,\%$ but at 498 K it increases to approximately $7\,\%$.

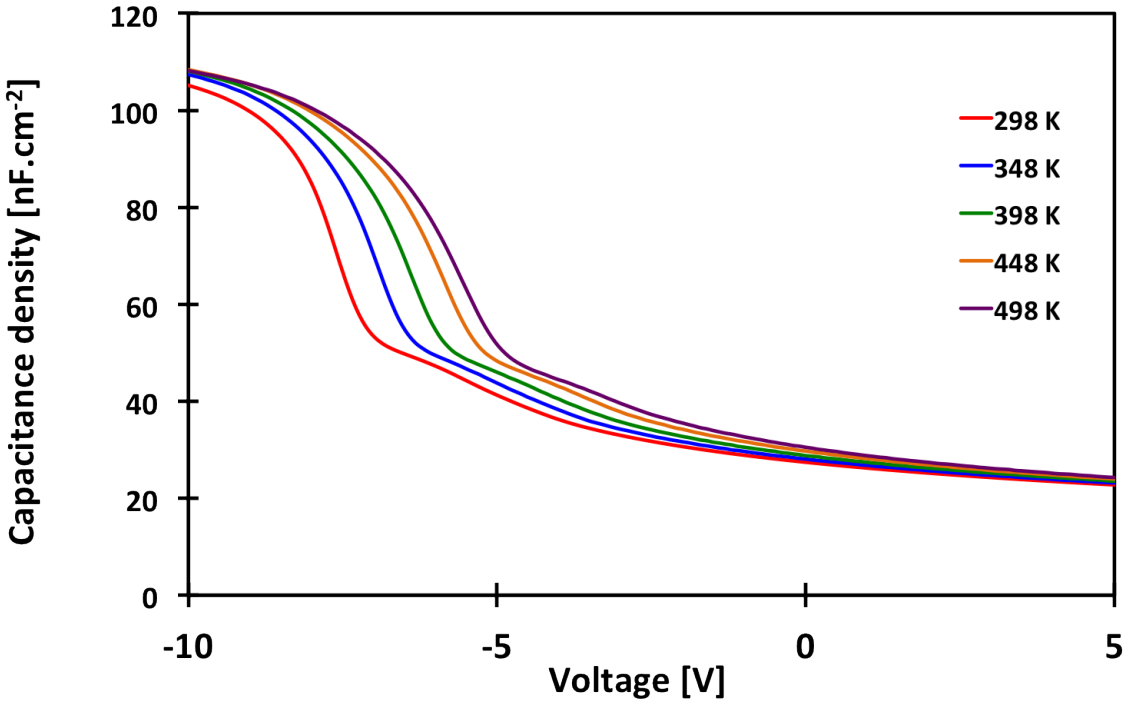


Figure 4.21: Capacitance density-Voltage characteristics for a HV06 p-type MIS capacitor from 298 K to 498 K measured at 1 MHz.

Interface trap density as a function of energy level (E_{TH}-E_V) within the bandgap was also extracted across the measured temperature range for each of the samples using the Terman method, using Equation 4.35, as discussed in section 4.5 [182]. As can be seen from the data in Figure 4.28, sample CR27 showsan reduction in D_{it} close to the valence band edge with increasing temperature. However, the opposite phenomena was observed for samples HV06 and CR25 as shown by the data in Figure 4.26 and 4.27. An increased D_{it} was observed with increasing temperature across the measured energy range. This is in agreement with the extracted n-type characteristics and suggests that either the interface trapped charge has a temperature dependence and, therefore, becomes electrically active at elevated temperatures or mobile charges are present in the oxide close the SiC-SiO_2 interface, which have varying time constants so only begin to interact with the semiconductor carriers at elevated temperatures. The mobile charge could be introduced to the oxide during the post oxidation treatments as outlined in Table 4.1. The decrease in density of interface traps at the valence band edge with increasing temperature supports previous work and is due to the bandgap narrowing effect as temperature increases [186].

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A hysteresis test was conducted on each of the samples to examine the presence of mobile charge within each of the dielectrics. Each device was heated to 498 K and was swept from accumulation to inversion and back again. The measured characteristics are shown by the data in Figure 4.29a, 4.29b and 4.29c for HV06, CR25 and CR27, respectively. The

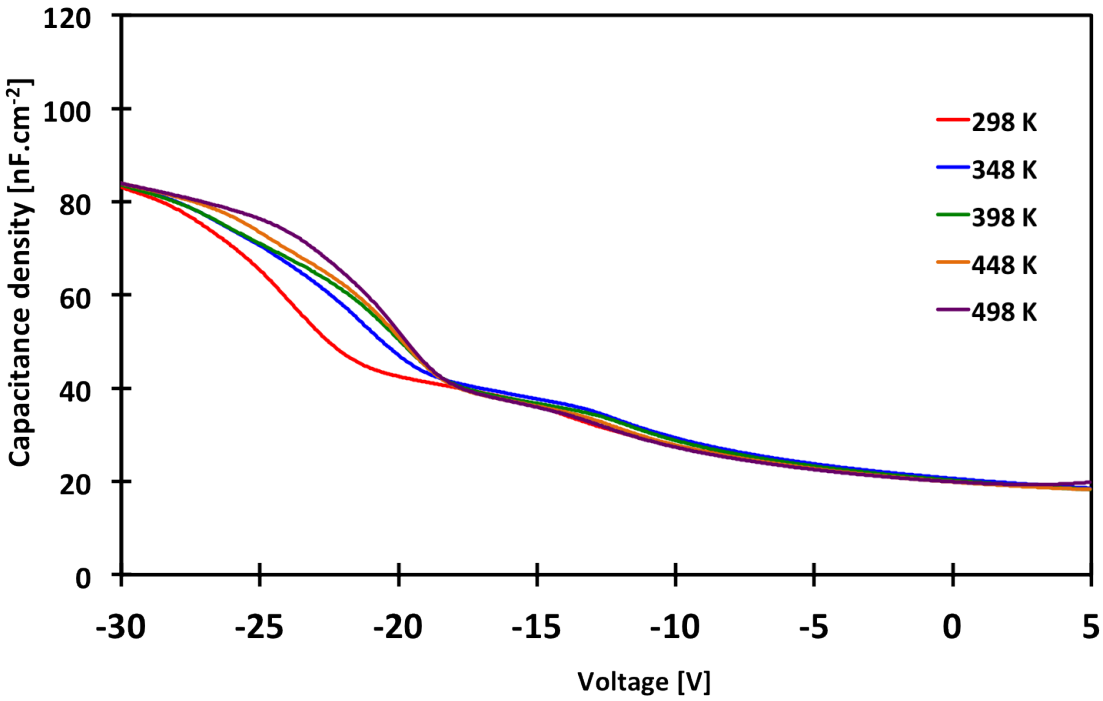


Figure 4.22: Capacitance density-Voltagee characteristics for a CR25 p-type MIS capacitor from 298 K to 498 K measured at 1 MHz.

change in flatband voltage (ΔV_{FB}) for each of the devices was extracted from the measured data using Equation 4.28. There was a very minimal shift for the HV06 p-type MIS sample and ΔV_{FB} was extracted to be 0.30 V. The CR25 p-type MIS sample exhibited the largest shift as ΔV_{FB} was equal to 6.25 V. ΔV_{FB} extracted for the CR27 p-type MIS sample was 1.00 V. The characteristics are in agreement with the extracted parameters from the n-type samples and confirm that CR25 contains the highest proportion of mobile oxide charge (Q_{M}) and oxide trapped charge (Q_{OT}) as $Q_M = -C_{OX}\Delta V_{\mathrm{FB}}$ and $Q_{OT} = -C_{OX}\Delta V_{\mathrm{FB}}$ [168]. The results equate to a combined Q_{M} and Q_{OT} for each of the devices of 3.2×10^{11} cm^{-2}, 5.2×10^{12} cm^{-2} and 6.8×10^{11} cm^{-2} for HV06, CR25 and CR27, respectively. When compared to the extracted values from the n-type MIS samples in subsection 4.7.1 it can be seen that the p-type devices have an order of magnitude more Q_{M} and Q_{OT} present within the dielectric than their n-type counterparts. This could be due to positive charges within the oxides that are neutralised by majority carriers in the n-type samples but in the p-type samples positive trapped carriers are added to the positive charges in the oxide to increase the effect. This is supported by findings by Palmieri *et al.* who witnessed a similar effect in a comparison study of three different oxidation procedures on both n and p-type 4H-SiC MOS capacitors and predicted that the charges present were due to carbon compounds close to the SiO_2/SiC interface [193].

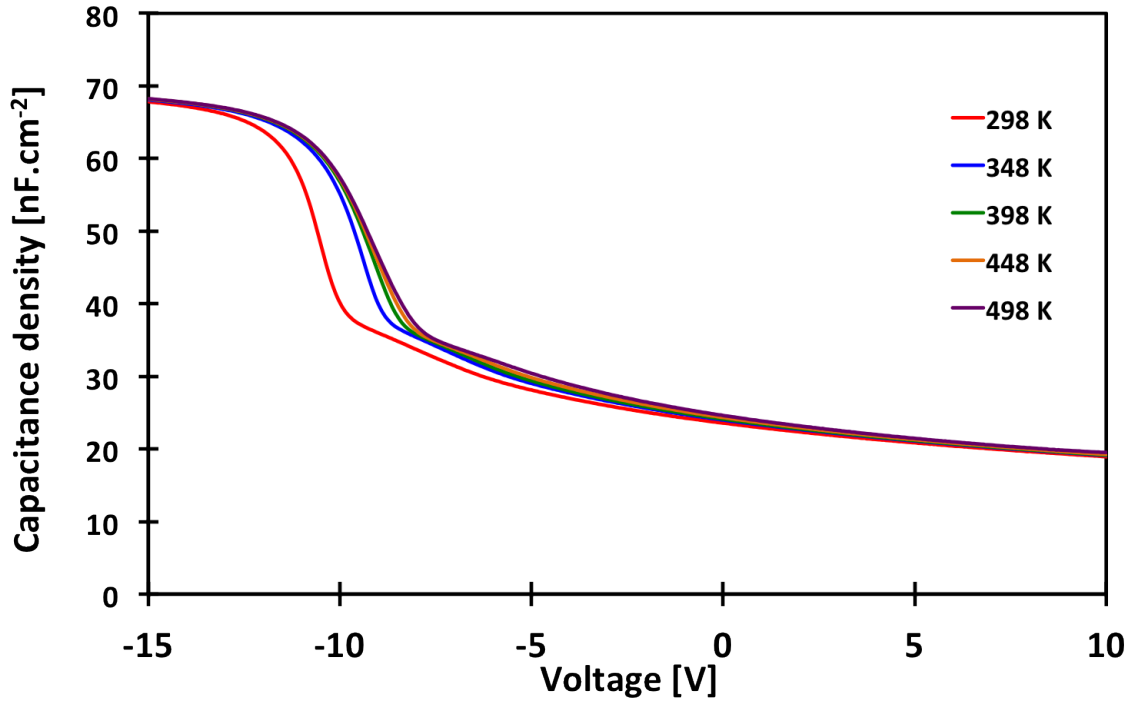


Figure 4.23: Capacitance density-Voltage characteristics for a CR27 p-type MIS capacitor from 298 K to 498 K measured at 1 MHz.

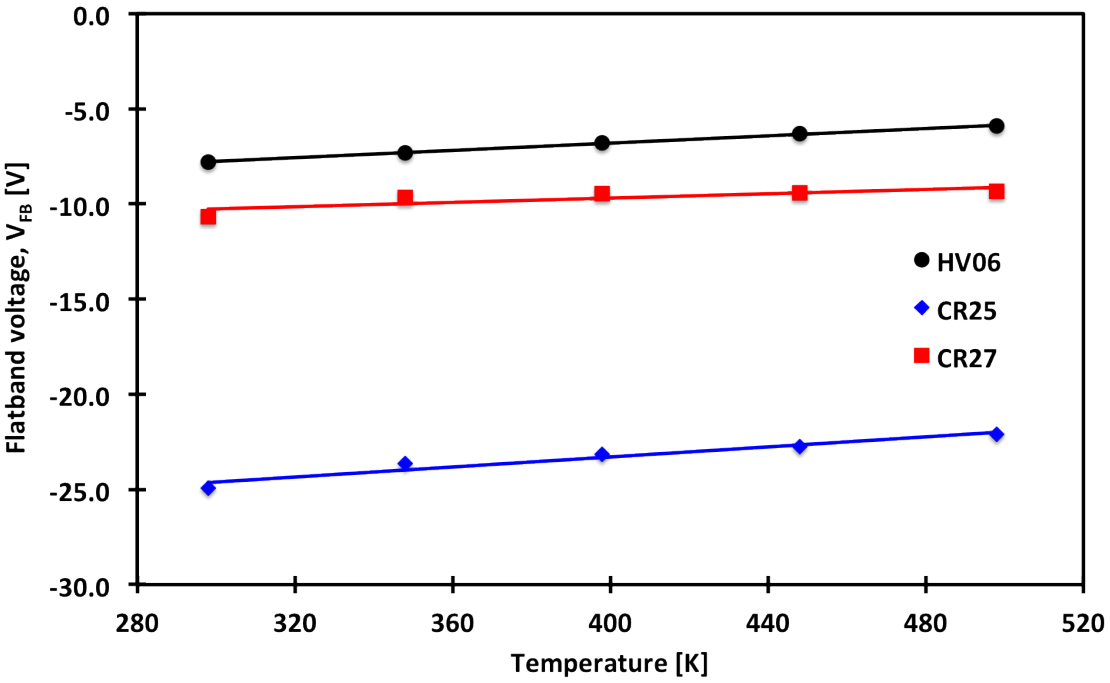


Figure 4.24: Flatband voltage as a function of temperature for HV06, CR25 and CR27 p-type MIS capacitors. Measurement error is smaller than the data points.

Conduction mechanisms in p-type 4H-SiC MIS capacitors

As with the n-type MIS samples, I-V characterisation was performed on each of the p-type MIS samples to examine the conduction mechanisms in each of the insulators. The variation

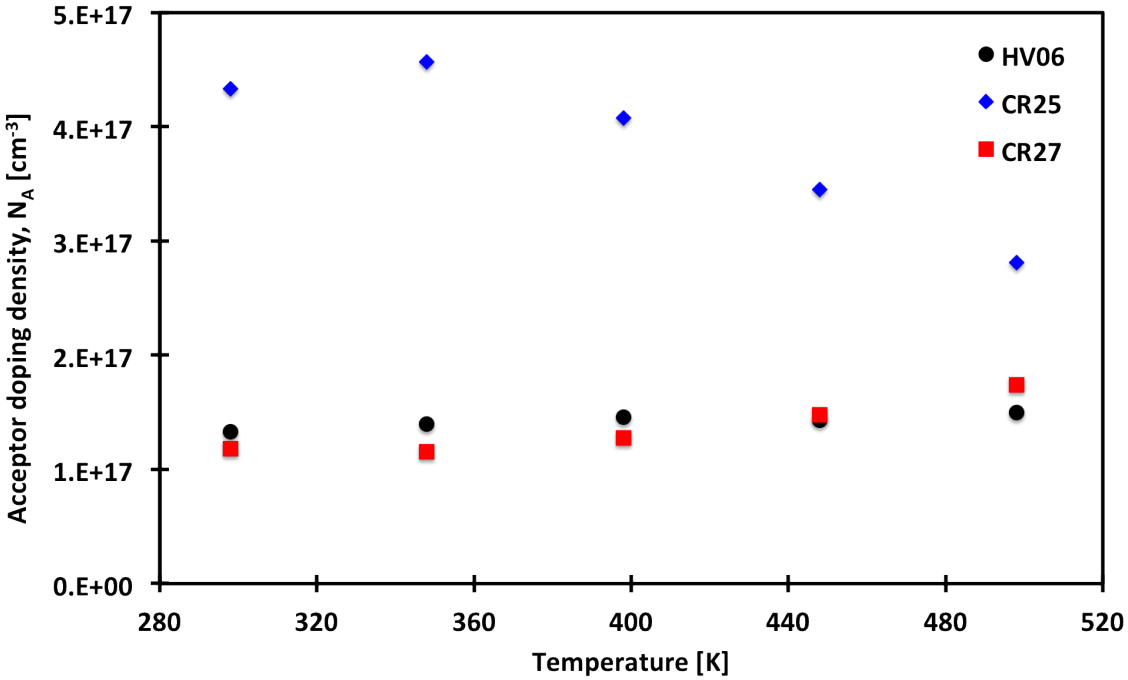


Figure 4.25: Acceptor doping density as a function of temperature for HV06, CR25 and CR27 p-type MIS capacitors. Measurement error is smaller than the data points.

of the leakage current density of each of the samples under negative gate biases at different temperatures is shown in Figure 4.30. All 3 exhibit a negligible temperature dependence, however, there is a much larger variation between the current density of the different samples over the observed electric field range than observed in their n-type counterparts that were discussed in subsection 4.7.1. The current density witnessed in HV06 (Figure 4.30a) and CR27 (Figure 4.30c) is consistently several orders of magnitude higher than that of CR25 as shown in Figure 4.30b across the entire scanned perpendicular electric field. CR25 also exhibits negligible electric field dependence, which suggests that the dielectric has a higher thickness than predicted due to the extremely low conduction. The current level exhibited by CR25 is also at the edge of the measurement capabilities of the Keithley system, which is likely to be a contributing factor to the oscillation ot the measured data set. The measured data is also inconsistent with the fact that CR25 is a deposited oxide. This difference may also be explained by a difference in barrier height values for the 3 dielectrics, which is due to the variation in growth conditions and post oxidation treatments. The results in Figure 4.30 also show that very little temperature dependence is exhibited in the conductance mechanisms of each of the dielectrics shown.

The current conduction mechanisms as outlined in Table 4.2 can vary depending on the applied electric field. Certain conduction processes can dominate in certain temperature and electric field ranges and may not be independent of one another [1]. Several mechanisms have been reported to explain the observed characteristics of conduction in insulators as given in

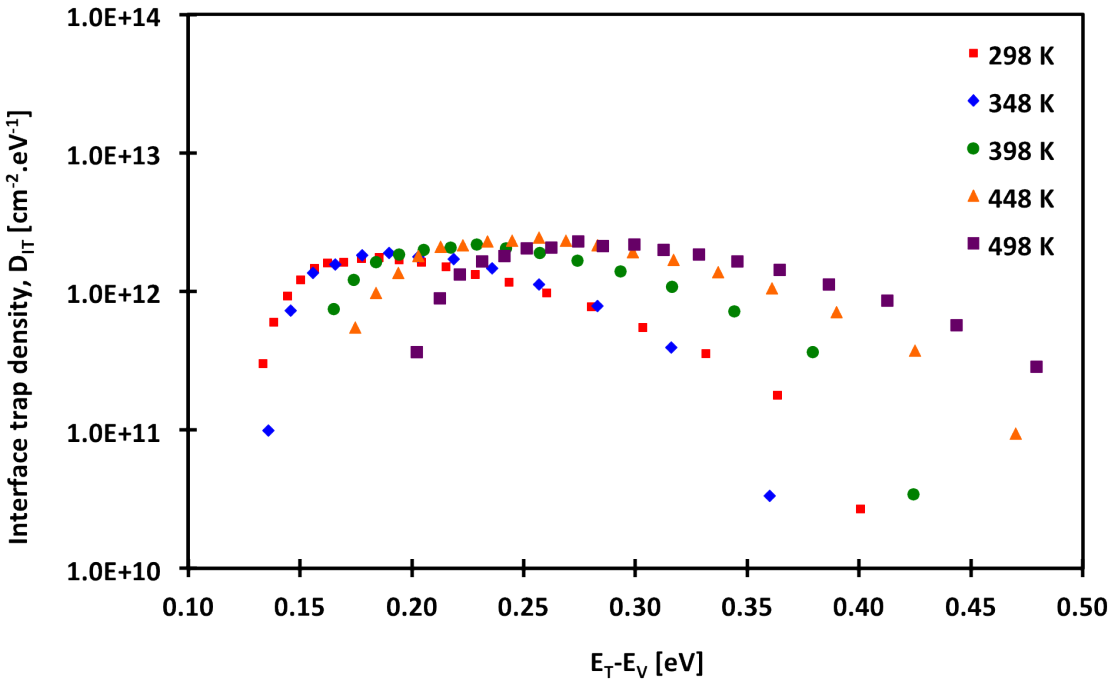


Figure 4.26: Interface trap density as a function of energy at varying temperatures for the HV06 p-type MIS capacitor structure.

Table 4.2. In order to understand the conduction behaviours of the 3 p-type MIS samples under examination in this thesis the log(J)-log(E) characteristics of each of the samples at room temperature are given in Figure 4.31. This data set clearly exhibits distinguishable regions, which shows that there are various contributing mechanisms that are dominating in different regions of the applied electric field. The current level exhibited by CR25 is also at the edge of the measurement capabilities of the Keithley system, which is likely to be a contributing factor to the oscillation ot the measured data set.

To establish the conduction mechanisms that dominate the characteristics of each of the p-type MIS samples at different electric fields the results can be compared to the theoretical conduction mechanisms that were outlined in Table 4.2. It has previously been reported that at lower and intermediate perpendicular electric fields that conduction in SiO_2 on 4H-SiC is dominated by trap assisted tunnelling as described in Equation 4.40 [139]. Trap assisted tunnelling is the phenomena when charge moves through defect energy levels in the oxide by a capture emission process or by a hopping mechanism. Therefore, a plot of ln(JE) vs 1/E will allow the energy of the trap (ϕ_t) and the trap concentration in the oxide (N_t) to be estimated from the slope and intercept of the plot, respectively using Equation 4.52. A plot of ln(JE) vs 1/E is shown for sample HV06 and CR27 in Figure 4.32. A linear region was observed between -1.00 and -1.65 MV.cm^{-1} for each of the samples. The trap energy level (ϕ_t) for each of the samples was extracted from Figure 4.32 and was 0.22 eV for both the HV06 and CR27 sample. The trap concentration (N_t) was 6.89×10^{21} cm^{-3} for HV06 and

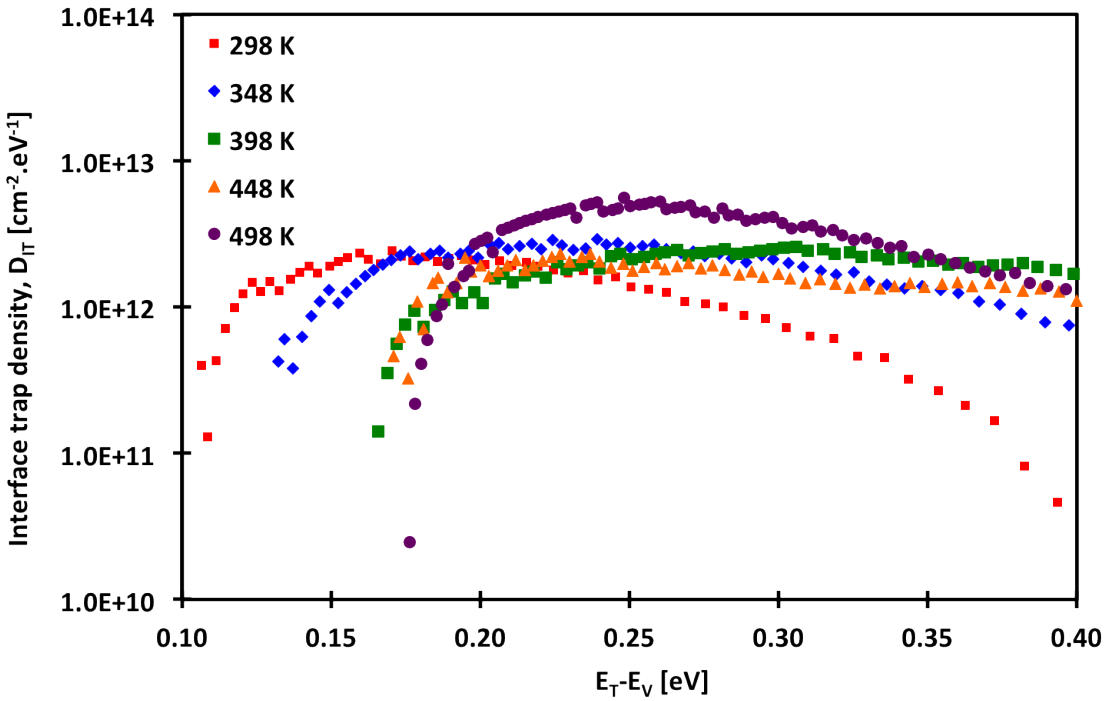


Figure 4.27: Interface trap density as a function of energy at varying temperatures for the CR25 p-type MIS capacitor structure.

1.91×10^{20} cm^{-3} for CR27. The reported values on the trap concentration are 1-2 orders of magnitude lower than their n-type counterparts, which could be a combined contribution of the trap energy level and concentration in the p-type MIS system. The p-type parameters are also much closer to those observed in nitrided thermally grown oxides on 4H-SiC as examined by Cheong *et al.* [138], however, the current density is comparable to the n-type counterparts at electric fields beyond 2 $MV.cm^{-1}$, which suggests that another mechanism such as Ohmic conduction may be dominating the leakage characteristics of both the n and p-type samples.

At high electric fields it has been identified in previous studies that the conduction mechanism that limits current transport is Fowler-Nordheim tunnelling [190] [191]. The Fowler-Nordheim tunnelling mechanism is described by Equation 4.41. A linear trend in a plot of $\ln(J/E^2)$ vs 1/E would indicate the presence of a Fowler-Nordheim tunnelling mechanism, however, in this study no linear trends were identified in the data sets, which suggests that Fowler-Nordheim is not a dominant conduction mechanism through any of the dielectrics used in this investigation.

Another contributing mechanism that has previously been discussed is Frenkel-Poole emission, which is the term used to describe the field enhanced thermal excitation of electrons trapped inside the dielectric at an effective average depth of $\phi_t$and is calculated using Equation 4.43 [1]. Equation 4.43 indicates that a plot of ln(J/E) vs $\sqrt{E}$ will produce a straight line if Frenkel-Poole emission is present in the device given by Equation 4.53. However, no

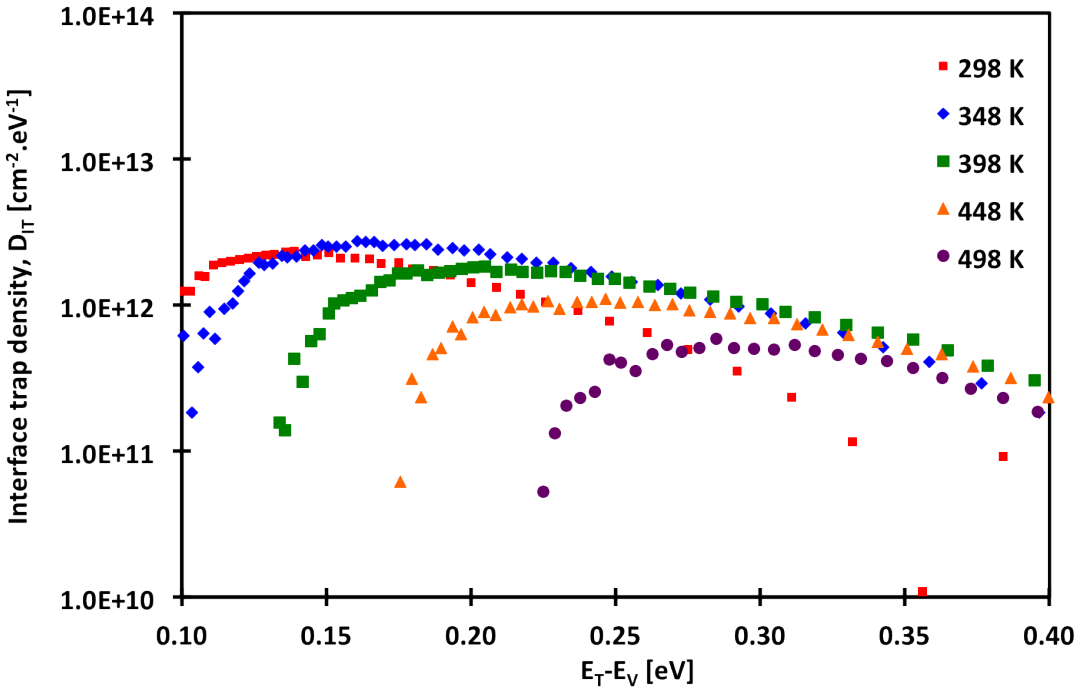


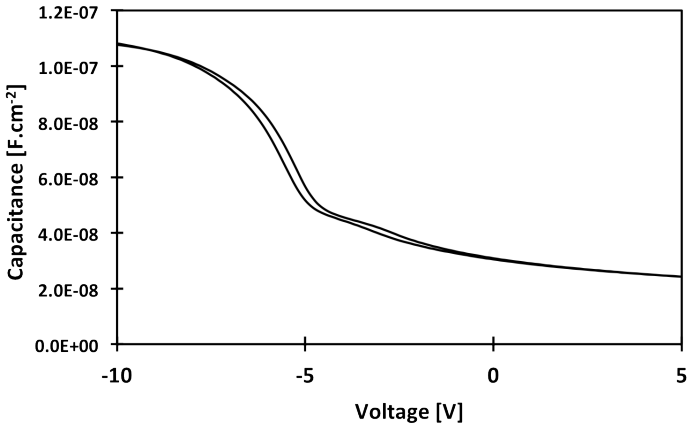
Figure 4.28: Interface trap density as a function of energy at varying temperatures for the CR27 p-type MIS capacitor structure.

linear trends were witnessed in the p-type MIS samples, which suggests that Frenkel-Poole is not a dominant conduction mechanism in this system.

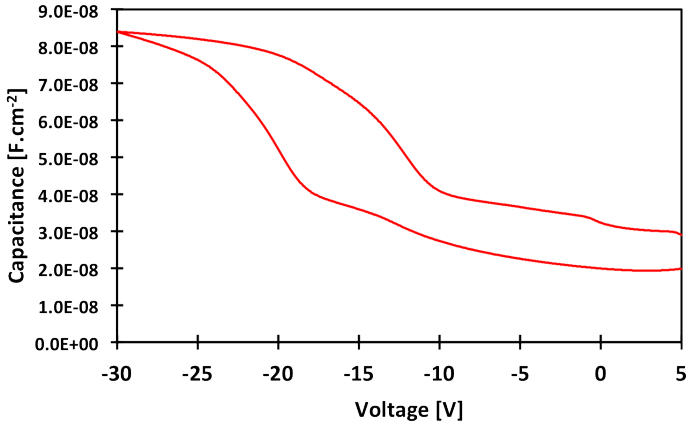
As with the n-type MIS samples, it is also important to note that all of the linear fitted trends reported in this investigation had correlation coefficients of greater than 0.98, which highlights that the characteristics showed extremely strong linear trends in the examined electric field regions.

4.8 Impact of threshold voltage adjust implantation on the characteristics of 4H-SiC MIS capacitors

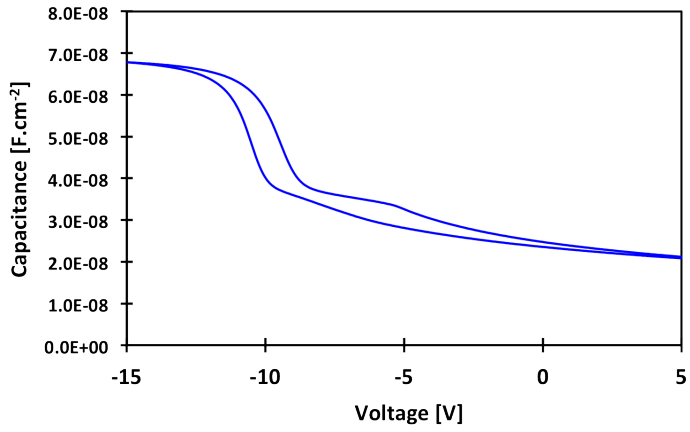
Threshold voltage adjust ion implants were applied to the p-type MIS samples and n-channel MOSFET devices to target a particular threshold voltage during operation. In order to investigate the effect of the implant on the n-channel MOSFET characteristics it is firstly important to examine the impact of the implants on the equivalent p-type MIS samples. All 3 samples that were examined in this study had undergone the same gate dielectric treatment (sample CR27 as described in Table 4.1) but had undergone varying threshold adjust implants. The samples that were examined will be referred to as NVT0, NVT1 and NVT2. NVT0, NVT1 and NVT2 had undergone increasing doses of nitrogen, which act to reduce the threshold voltage of the n-channel devices by reducing the p-well doping concentration at the semicon-



(a) HV06 p-type MIS capacitor.

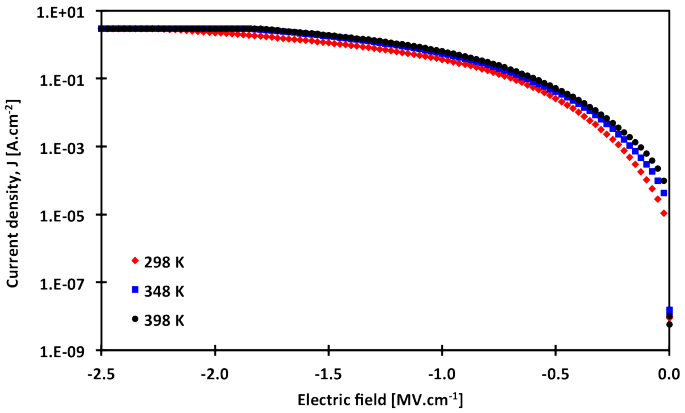


(b) CR25 p-type MIS capacitor.

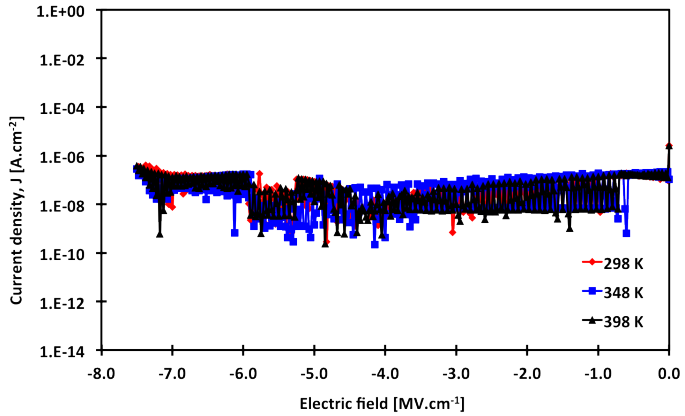


(c) CR27 p-type MIS capacitor.

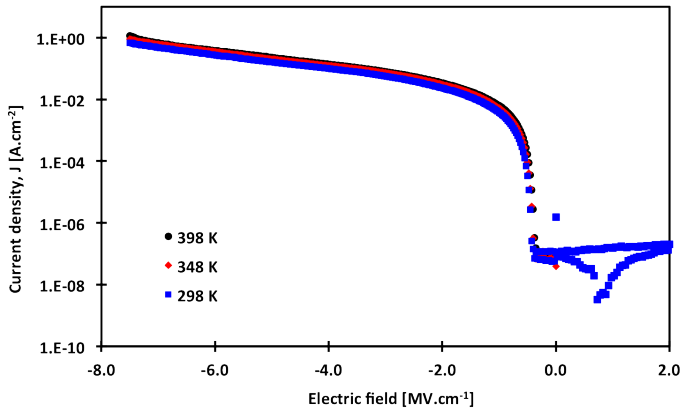
Figure 4.29: Forward and reverse sweep C-V characteristics taken at a temperature of 498 K and a frequency of 1 MHz to show the C-V hysteresis and the presence of mobile and oxide trapped charge in the gate dielectric of p-type MIS capacitors.



(a) HV06 p-type MIS capacitor.



(b) CR25 p-type MIS capacitor.



(c) CR27 p-type MIS capacitor.

Figure 4.30: Current density (J) against electric field (E_{i}) for the 3 dielectrics (HV06, CR25, CR27) on p-type 4H-SiC for a range of temperatures (298 K, 348 K and 398 K).

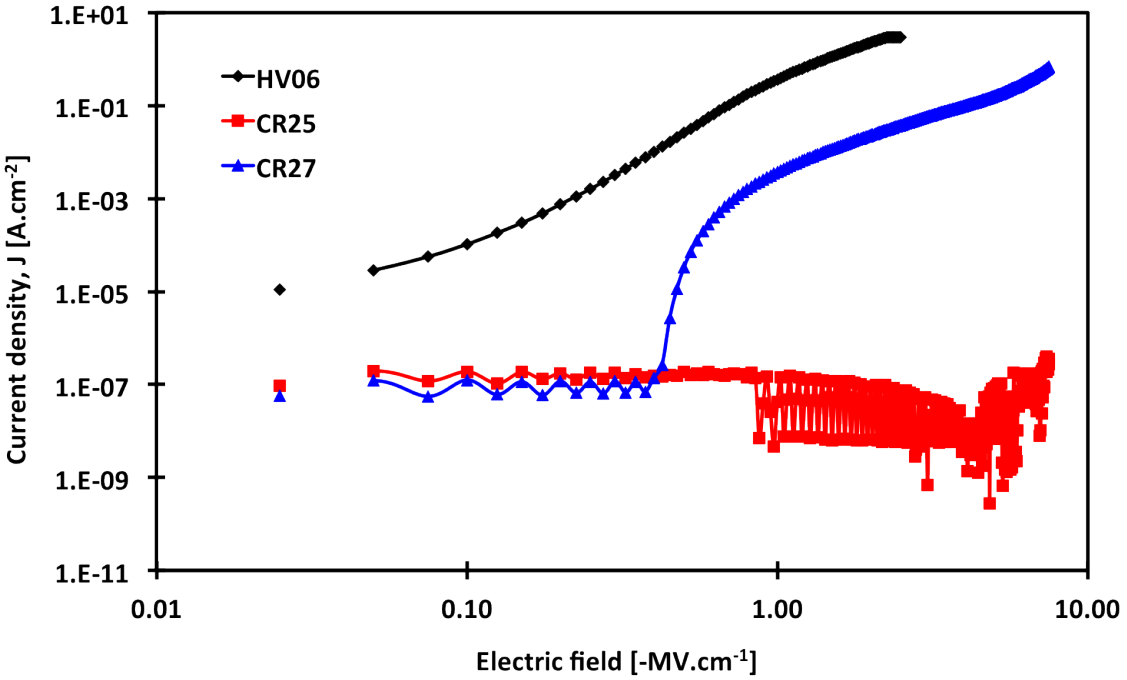


Figure 4.31: Current density (J) against electric field (E_{i}) for the 3 dielectrics samples (HV06, CR25, CR27) measured in accumulation at 298 K.

ductor surface [1]. NVT0 was implanted with 1.7×10^{12} cm^{-2}, NVT1 with a 2.4×10^{12} cm^{-2} and NVT2 with a 3.0×10^{12} cm^{-2} dose of nitrogen.

Low frequency capacitance density-voltage measurements were performed at 298 K and 1 Hz using a Keithley 4200 SCS Parameter Analyser on each of the p-type MIS samples, NVT0, NVT1 and NVT2, as shown in Figure 4.33. The extracted device characteristics for each of the samples is summarised in Table 4.5. As shown in Table 4.5, the extracted acceptor doping concentration (N_{A}) for each of the samples decreases due to the increasing dose of nitrogen and all of the samples exhibit comparable oxide capacitances and equivalent oxide thicknesses. NVT2 has the highest flatband voltage followed by NVT1 and then NVT0.

Sample	**Measured V_{FB} [V]**	**Theoretical V_{FB} [V]**	**C_i [nF.cm^{-2}]**	**t_i [nm]**	**N_A [cm^{-3}]**
NVT0	-11.2 $\pm$0.89	1.48	78.1 $\pm$6.25	44.19 $\pm$3.54	$9.28\times10^{16} \pm 9.28 \times 10^{15}$
NVT1	-12.5 $\pm$1.00	1.46	77.2 $\pm$6.18	44.72 $\pm$3.58	$7.72\times10^{16} \pm 7.72 \times 10^{15}$
NVT2	-16.0 $\pm$1.28	1.45	74.4 $\pm$5.95	46.41 $\pm$3.71	$7.44\times10^{16} \pm 7.44 \times 10^{15}$

Table 4.5: Extracted parameters of the p-type CR27 NVT0, NVT1 and NVT2 MIS capacitor samples measured at room temperature.

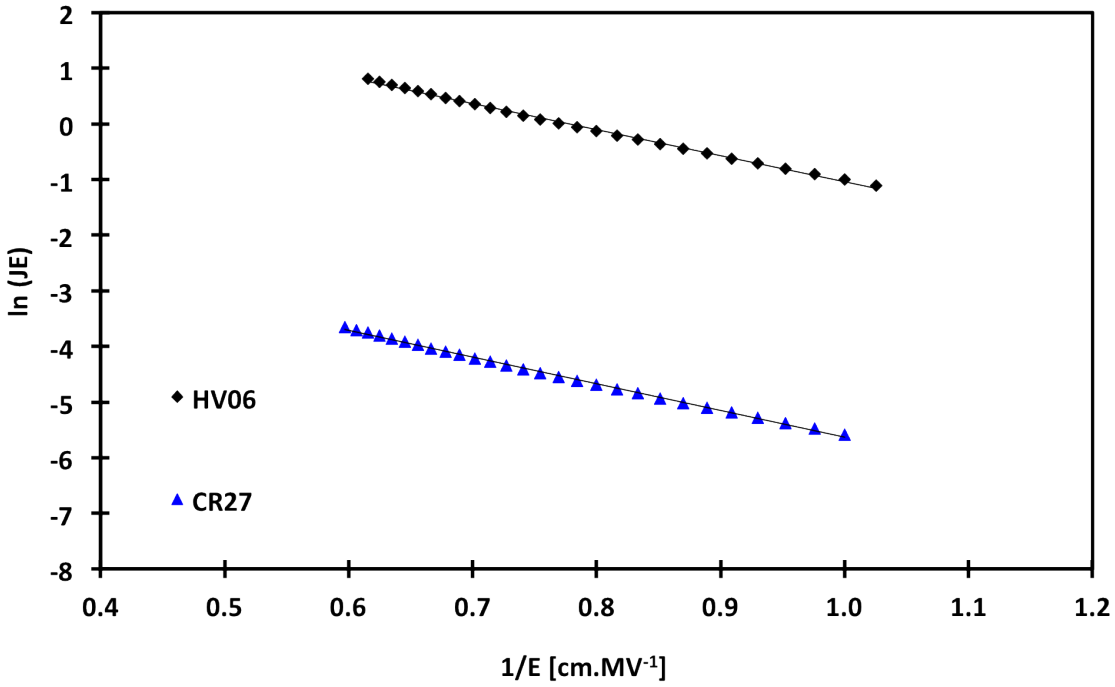


Figure 4.32: Trap assisted tunnelling plot schematic of the HV06 and CR27 p-type MIS capacitors at 298 K.

The large shift between the flatband voltage of each of the devices suggests that the charge within the oxide has been affected by the threshold voltage implantation process as the variation in doping concentration alone could not be responsible for such a large shift. If the charges within the oxide were constant for all 3 dielectrics the flatband voltage change would be due to the variation in the metal-semiconductor work function (ϕ_{ms}), which is a product of the metal workfunction, the electron infinity, the band gap energy and the built-in potential of the MIS structure as outlined in Equation 4.46 and Equation 4.47. As all 3 samples have the same polysilicon gate, the metal work function should be constant for all samples, as should the band gap energy and the electron affinity as they are all formed on the same 4H-SiC p-type material. The only variation should be in ϕ_{B}, which is linked to the doping concentration in the SiC. Table 4.5 shows the extracted doping concentration for each of the samples. If this was the only factor that contributed to the variation in flatband voltage the flatband voltage would only vary by 0.005 V between NVT0 and NVT1 and by 0.0001 V between NVT1 and NVT2 as calculated using the measured doping concentrations and Equation 4.46. Also as C_{i} has been extracted for each of the devices in Table 4.5 the combined charge within the oxide (Q_{f}, Q_{m} and Q_{ot}) of each sample can be calculated using Equation 4.46. However, it is important to note that charge extracted from low frequency C-V and high frequency C-V data is not comparable and, therefore, the results extracted from the low frequency C-V data in this section cannot only be used as a comparator against each other and not as a comparison of the high frequency C-V data in the proceeding sections of this thesis. A charge of $7.12 \times 10^{12}\,\mathrm{cm}^{-2}$, $8.05 \times 10^{12}\,\mathrm{cm}^{-2}$ and $1.04 \times 10^{13}\,\mathrm{cm}^{-2}$ is extracted for NVT0, NVT1

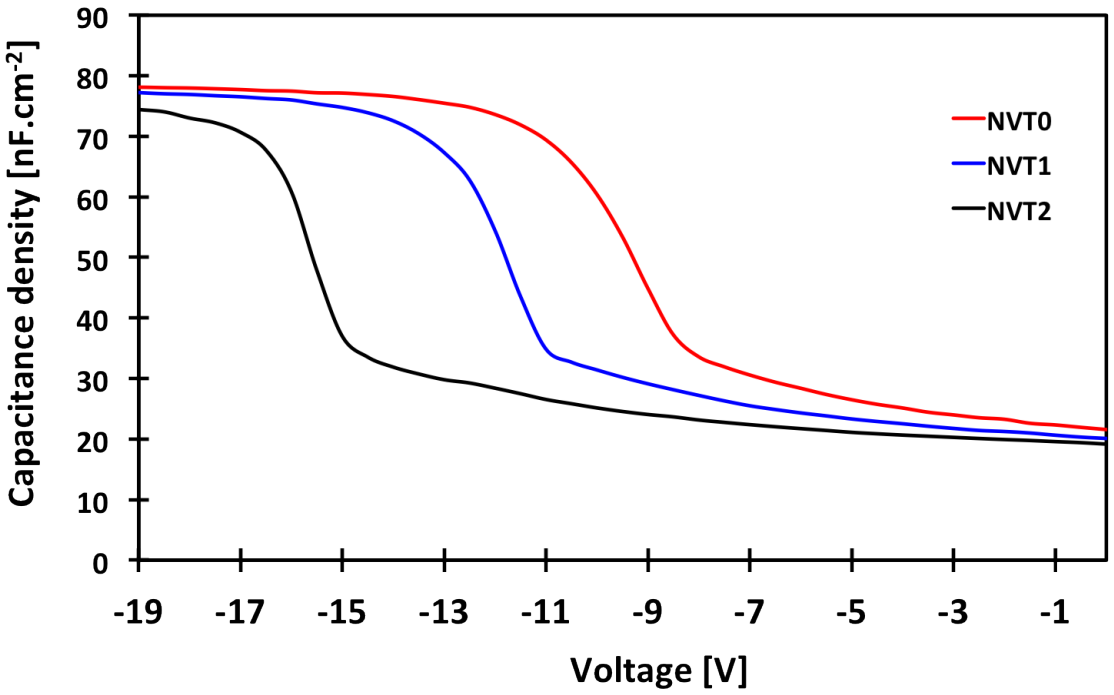


Figure 4.33: Capacitance density-Voltage characteristics of p-type CR27 MIS capacitors with an NVT0, NVT1 and NVT2 threshold voltage adjust implantation measured at 298 K and 1 Hz.

and NVT2. The slight decrease in C_i and increase in the equivalent oxide thickness (t_i) with increasing nitrogen implant dose as shown by the data in Table 4.5 also supports the idea that the nitrogen implant has acted to alter the dielectric. This is is supported by a study in which Daas *et al.* observed that there was a strong correlation between the nitrogen doping concentration in 4H-SiC and the oxide growth, as higher doping concentrations displayed higher growth rates [194]. This was reported to be due to an increase in the linear rate constant as a consequence of defects from doping-induced lattice mismatch, which are more reactive than bulk crystal regions [194].

Low frequency capacitance density-voltagemeasurements were also performed for each of the samples across a varying temperature range from 298 K to 498 K with increments of 50 K at 1 Hz. The results are shown in Figure 4.34, 4.35 and 4.36 for NVT0, NVT1 and NVT2, respectively. As shown, in Figure 4.37 all of the devices exhibit a decrease in flatband voltage with temperature, which is due to a contribution of the reduction in band gap energy, an increase in intrinsic carrier concentration as discussed in subsection 4.7.1 and a variation in the charge at the interface and in the oxide across the measured temperture range.

The data in Figure 4.38 show the extracted acceptor doping concentration for each of the samples across the temperature range. All show a very slight decrease in N_A with increasing temperature. This could be due to the increase ionisation of the implanted nitrogen dopants with temperature.

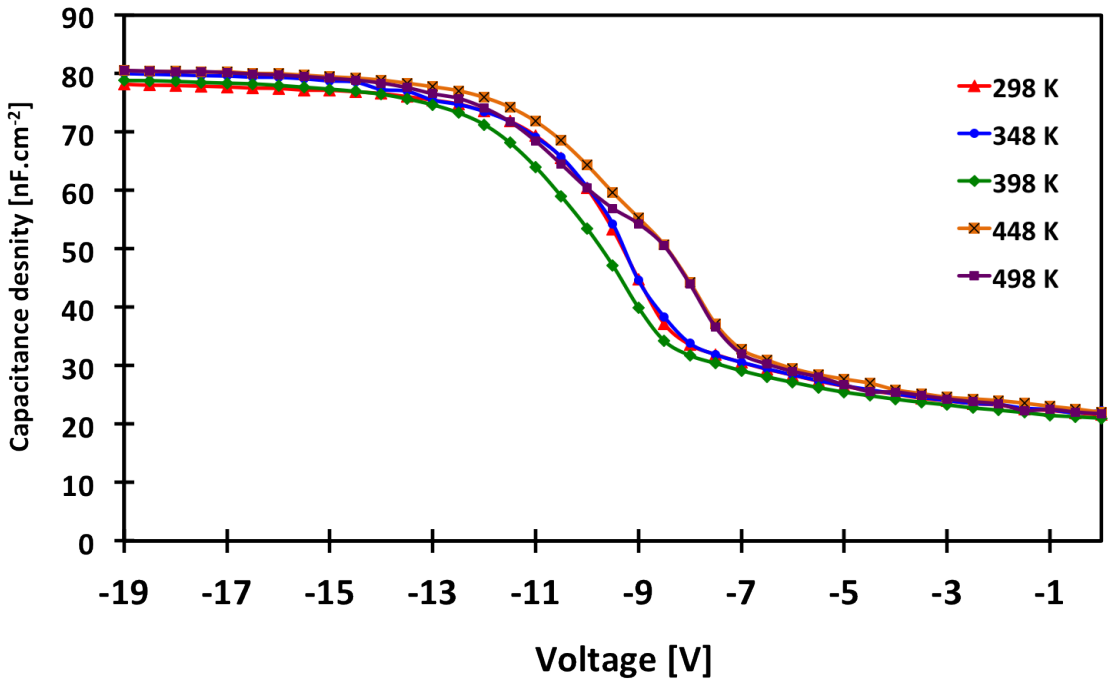


Figure 4.34: Capacitance density-Voltage characteristics of a p-type CR27 MIS capacitors with an NVT0 threshold voltage adjust implantation measured from 298 K to 498 K and 1 Hz.

Figure 4.39 shows D_{it} as a position within the band gap for each of the samples as extracted from the low frequency C-V characteristics using Equation 4.36. As shown all 3 samples show a comparable D_{it} profile and all exhibit an interface trap density of approximately $2 \times 10^{12}\,\mathrm{cm}^{-2}.\mathrm{eV}^{-1}$. This suggests that although the implant acts to alter the charge within the oxide it does not significantly alter D_{it} that is present as the semiconductor-dielectric interface.

4.9 Summary

This chapter has focussed on the characterisation of the MIS system that is under investigation in this thesis including the analysis of the varying dielectric samples (HV06, CR25 and CR27) on both n and p-type 4H-SiC at varying temperatures and the analysis of the effects of the threshold voltage adjust ion implantation process on p-type MIS capacitor structures.

In this investigation it has been demonstrated that the 3 dielectrics exhibit very similar properties on both n and p-type 4H-SiC. The CR25 MIS samples on both n and p-type 4H-SiC showed a very large variation of interface trap density with temperature and both showed an increase in D_{it} at the conduction and valence band edge, respectively with increasing temperature. This suggests that the traps have a temperature dependence and become electrically active at elevated temperatures. However, there was a large variation in the conduction mech-

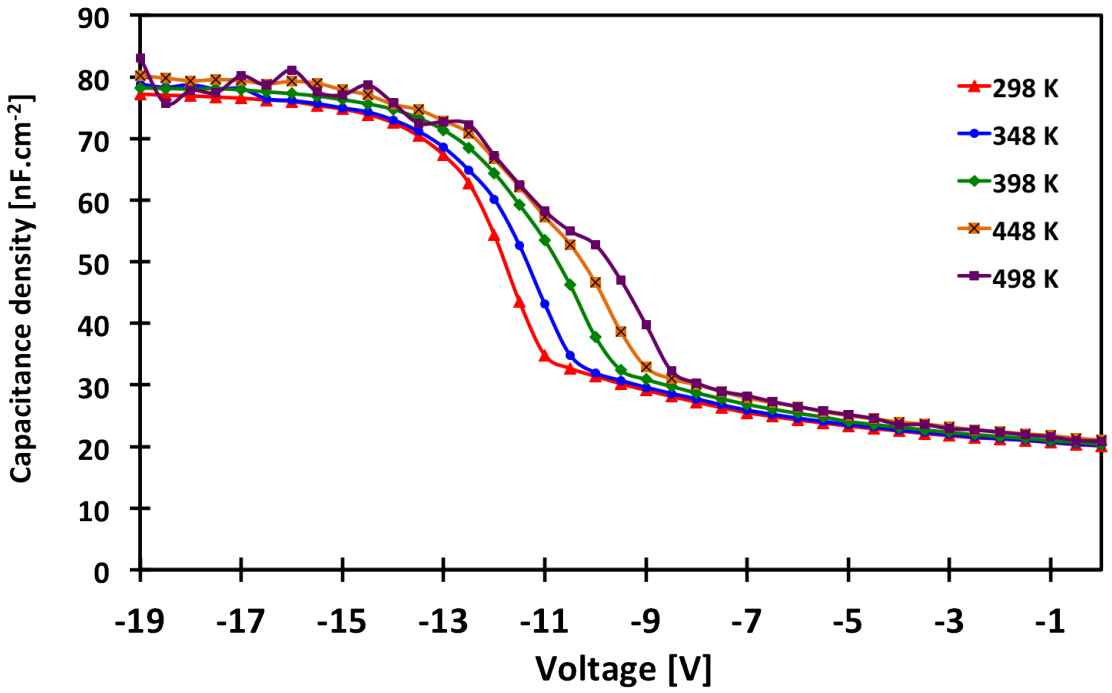


Figure 4.35: Capacitance density-Voltage characteristics of a p-type CR27 MIS capacitors with an NVT1 threshold voltage adjust implantation measured from 298 K to 498K and 1 Hz.

anisms, which were observed for n and p-type CR25 dielectric MIS samples. The n-type sample exhibited a trap assisted tunnelling conduction mechanism, whereas, the equivalent p-type sample demonstrated an extremely low leakage current and showed no electric field or temperature dependence.

CR25 has the highest mobile and oxide trapped charges out of the 3 dielectrics on both n and p-type 4H-SiC, which suggests that the dielectric processing technique produces the lowest quality dielectric. This could also be a product of the deposited oxide and the removal of the original thermally grown SiO_2 layer as outlined in Table 4.1.

HV06 has a very low equivalent oxide thickness in both the n-type and p-type sample, which could be due to a modification of the relative permittivity of the dielectric (ε_r) or due to a reduction in the physical oxide thickness due to the post oxidation anneal treatments that were carried out on this sample as described in Table 4.1.

The investigation into the impact of the threshold voltage adjust implantation on the MIS capacitor characteristics identified that a slight decrease in N_A with temperature was witnessed for all of the samples, NVT0, NVT1 and NVT2. This could be due to an increased ionisation of the implanted nitrogen dopants with temperature. It was observed that a higher implant dose leads to a a large shift in V_{FB}, therefore, suggesting the nitrogen implant acts to modify the oxide charge of each of the samples (Q_m+Q_F+Q_{ot}). However, the variation in implant dose has no impact on D_{it} as all 3 samples showed equal D_{it} for E_{TH}-E_V values of

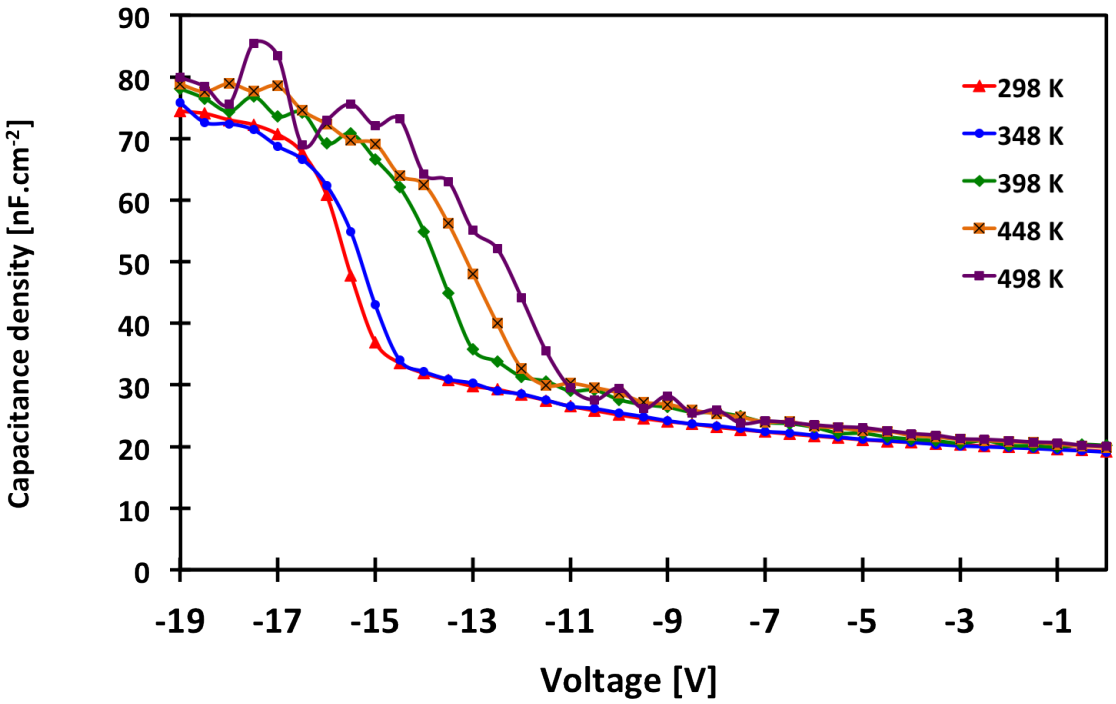


Figure 4.36: Capacitance density-Voltage characteristics of a p-type CR27 MIS capacitors with an NVT2 threshold voltage adjust implantation measured from 298 K to 498 K and 1 Hz.

0.2 to 1.6 eV.

As a solution for a complementary process for both n-type and p-type 4H-SiC MIS technology the most viable process technique of those examined is CR27. CR27 on both n-type and p-type 4H-SiC showed extremely promising characteristics with acceptable equivalent oxide thicknesses and oxide capacitances that were representative of SiO_2, the sample had the lowest oxide charge for the n-type MIS capacitor and the second lowest oxide charge for the p-type MIS sample. This supports the theory that a thin thermally grown oxide layer at the semiconductor-dielectric interface is beneficial for an enhanced interface and reduced gate leakage in a 4H-SiC MIS structure [195]. All 3 dielectrics showed comparable D_{it} values at room temperature, however, CR27 showed the largest decrease of D_{it} with temperature out of the 3 samples on both n-type and p-type 4H-SiC, which would make it the most suitable dielectric for high temperature applications.

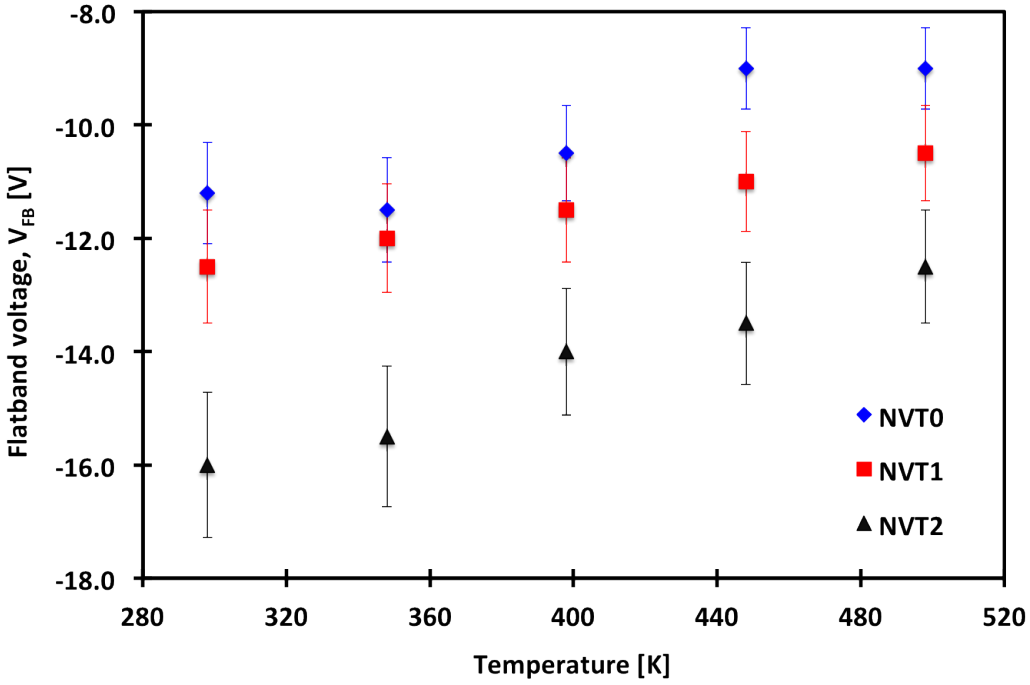


Figure 4.37: Flatband voltage as a function of temperature for NVT0, NVT1 and NVT2 p-type MIS capacitors.

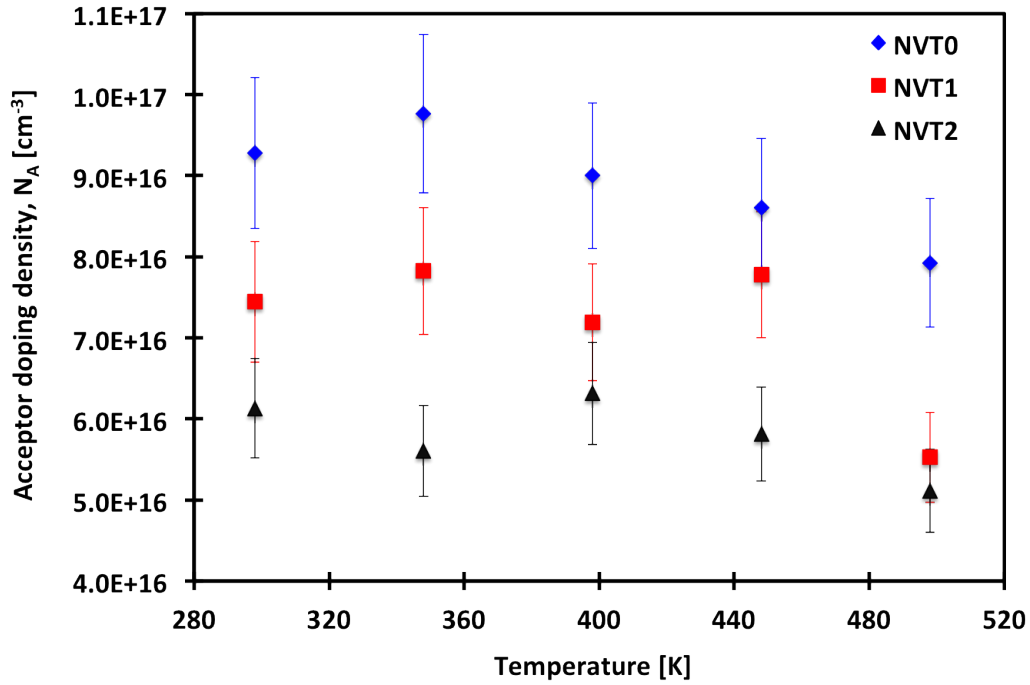


Figure 4.38: Acceptor doping concentration as a function of temperature for NVT0, NVT1 and NVT2 p-type MIS capacitors.

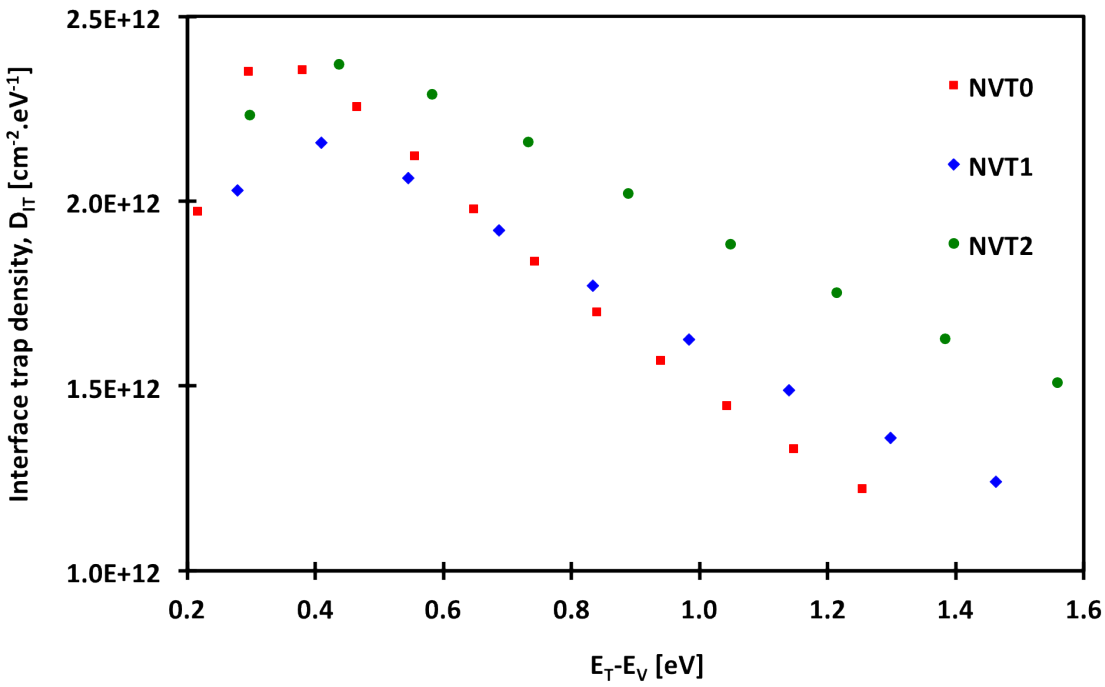


Figure 4.39: Interface trap density as a function of energy at 298 K for NVT0, NVT1 and NVT2 p-type MIS capacitors.

Chapter 5

Impact of dielectric formation and processing techniques on the operation of 4H-SiC MOSFETs

5.1 Introduction

The main objective of this study is to aid in the advancement and commercialisation of a CMOS process to enable the production of signal level 4H-SiC MOSFETs for high temperature digital and analogue applications. Therefore, the focus of this chapter is on the electrical characterisation and performance of the 4H-SiC n and p-channel MOSFETs that have undergone different dielectric process treatments (sample HV06, CR25 and CR27) which have previously been discussed in Chapter 4; with the aim to establish which technique provides the best characteristics for a complementary CMOS process.

5.2 Overview of the theoretical MOSFET

As discussed in section 2.2 the metal-oxide-semiconductor field-effect-transistor (MOSFET) is one if the most important devices for integrated circuits in microprocessors and semiconductor memories, as well as being a very important power device [1]. Due to this it is becoming increasingly important to understand and advance the characteristics of 4H-SiC MOSFETs for both power device applications and signal level devices.

MOSFETs have several attractive features, which make them ideal for use in analogue switching, high-input-impedance amplifiers, microwave amplifiers and digital integrated circuits. The features include [1]:

- Higher input impedance than bipolar transistors, which allows the input impedance to be more readily matched to the standard microwave system.
- Negative temperature co-efficient at high current levels - more uniform temperature distribution over the device area and prevents the FET from thermal runaway or second

breakdown that can occur in the bipolar transistors.

- The device is thermally stable, even when the active area is large or when many devices are connected in parallel.
- FETs do not suffer from minority carrier storage as there is no forward-biased pn junction and consequently have higher large-signal switching speeds.

The MOSFET is usually referred to as a majority carrier or unipolar device because the current in a MOSFET is predominantly transported by carriers of one polarity. As shown in Figure 5.1 a MOSFET is a four-terminal device made up of a source, drain, gate and substrate or body. Figure 5.1 shows an n-channel MOSFET, which is made up a p-type substrate into which two n+ regions are formed, the source and drain and a gate electrode which is usually made of doped polysilicon or metal and is separated from the substrate by a thin insulating film known as the gate dielectric.

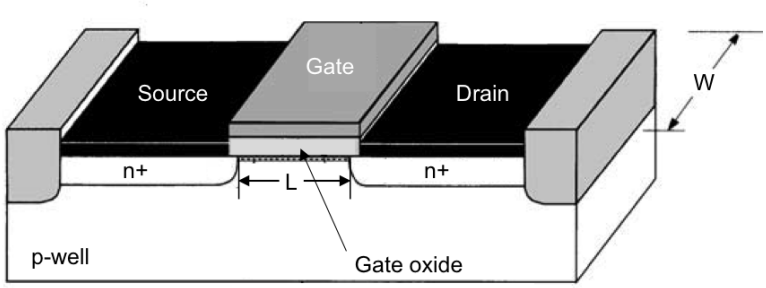


Figure 5.1: Schematic diagram of a basic n-channel MOSFET device structure.

The MOSFET behaviour is very similar to that of the MOS capacitor which was discussed in chapter 4. When a low voltage is applied to the gate electrode that is insufficient to form an inversion layer at the surface, there is no conduction in the channel, which corresponds to two p-n junctions situated back to back. This results in a high resistance and electrical isolation between the source and drain contacts. If a sufficiently large bias is applied to the gate electrode a surface inversion layer will be formed between the source and drain, which will form a conductive channel through which a current can flow. The conductance of the channel can be modulated by varying the voltage applied to the gate electrode.

Conduction in n-channel devices is based on the flow of electrons and the channel becomes more conductive with increasing positive bias on the gate whilst p-channel devices are controlled by hole conduction and are more conductive with a more negative gate bias. Enhancement mode (or normally-off) devices have a low transconductance at zero gate bias and require an applied gate voltage to form a conductive channel. Their counterpart, depletion

mode (or normally-on) devices, are conductive when a zero bias is applied to the gate of the device and a gate voltage must be applied to turn the channel off. Devices can either have a surface inversion channel or a buried channel. Buried channel devices are based on bulk conduction and are, therefore, free of surface effects such as scattering and surface defects resulting in better carrier mobility. The physical distance between the gate and the channel is larger and also dependent on gate bias leading to lower and variable transconductance.

In a long channel MOSFET, at low drain voltage and for a given gate voltage, the drain current is given by [1] [196] ,

$$I_{DS} = \frac{W}{L} q \mu_{inv} |Q_{inv}| V_{DS} \tag{5.1}$$

where W and L are the gate width and length, q is the electron charge, μ_{inv} is the average mobility of the carriers in the inversion layer, V_{DS} is the drain voltage and Q_{inv} is the average charge in the inversion layer.

The field effect mobility (μ_{FE}) is defined as [1] [196],

$$\mu_{\mathrm{FE}} = \frac{L}{W C_i V_{DS}} \left(\frac{\delta I_{DS}}{\delta V_{GS}} \right) \tag{5.2}$$

where C_{i} is the insulator capacitance per unit area and V_{GS} is the gate voltage. In 4H-SiC MOSFETs the values of the field effect mobility extracted form the V_{GS}-I_{DS} characteristics will not correspond to the true inversion mobility due to the large density of interface charge. A knowledge of Q_{inv} as a function of V_{GS}, which can be extracted from the measured V_{GS}-I_{DS} characteristics, can allow the immobile interface charge to be calculated, which includes contributions from both Q_{f} and Q_{it}. A change in gate voltage (δV_{GS}) results in a change in Q_{it} and a change in δQ_{inv} in the inversion layer as the surface Fermi level moves away from the intrinsic level towards the conduction band edge [196]. This can be summarised in Equation 5.3.

$$\delta V_{GS} = -\frac{q}{C_i} \left(\delta Q_{it} + \delta Q_{inv} \right) \tag{5.3}$$

By combining Equation 5.1 and 5.3, an expression that relates the experimental field effect mobility and the inversion carrier mobility is derived as described in [197]:

$$\mu_{\mathrm{FE}} = \mu_{inv} \frac{\left[1 + \frac{Q_{inv}}{\mu_{inv}} \frac{d\mu_{inv}}{dQ_{inv}} \right]}{1 + \frac{dQ_{it}}{dQ_{inv}}} \tag{5.4}$$

The expression in square brackets accounts for the carrier mobility with gate voltage.

5.2.1 Carrier mobility and scattering mechanisms in 4H-SiC

The conductivity (σ) of a semiconductor can be varied by the introduction of n or p-type dopants and can be represented by the expression,

$$\sigma = qn\mu \tag{5.5}$$

where μ is the carrier mobility, q is the charge of an electron and n is the number of carriers in the material. The carrier mobility is principally how quickly an electron or hole can move through a semiconductor under the influence of an applied electric field and is affected by the frequency of collisions with lattice defects and impurities. The probability of scattering is inversely proportional to the carrier mean free time and the mobility. A carrier moving through a semiconductor crystal can be scattered by a vibration of the lattice, which increases for high temperatures when the thermal agitation of the lattice becomes higher. Scattering can also be due to lattice defects (e.g. ionised impurities) and is prominent at low temperatures since atoms are less thermally agitated and the thermal motion of the carriers is also slower. Higher scattering arises because a slow moving carrier is likely to be scattered more significantly by an interaction with a charged ion than a carrier with a larger velocity.

If the carrier mobility in a material is reduced the conductivity of the material will reduce and hence the resistivity will increase and channel current will reduce. As it is widely known that 4H-SiC MOSFETs exhibit low channel mobility and hence low current it is of great importance to analyse the mechanisms that are contributing to the reduced channel mobility.

As previously reported [142] [198] [197] , the total inversion carrier mobility in 4H-SiC MOSFETs can be described by the sum of four mobility terms using Matthiessen's Rule which is often incorporated in simulation tools as the Lombardi mobility model [168][199],

$$\mu_{inv} = \left[\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{\mathrm{SR}}} + \frac{1}{\mu_C}\right]^{-1}, \tag{5.6}$$

where μ_B is the bulk mobility, μ_{AC} is the acoustic phonon mobility, μ_{SR} is the surface roughness mobility and μ_C is the Coulomb mobility of the MOSFET.

As previously stated, the measured field effect mobility will not correspond to the true inversion mobility due to the presence of interface trapped charges. However, in this thesis as the main area of interest is on the experimental device characteristics the modelled mobility mechanisms will be equated to the field effect mobility using Equation 5.7. Therefore, all of

the modelled mechanisms (μ_{AC}, μ_{SR} and μ_C) will be lower than the true value of each that would combine to from the true inversion mobility.

$$\mu_{\mathrm{FE}} \propto \left[\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{\mathrm{SR}}} + \frac{1}{\mu_C}\right]^{-1} \tag{5.7}$$

At low electric fields, the carrier mobility in a semiconductor is a function of the temperature and the total doping concentration, which is referred to as the bulk or low-field mobility, μ_{B}. To represent this phenomena an empirical model was developed by Caughey-Thomas which is shown in Equation 5.8 [200][201].

$$\mu_B = \frac{\mu_{max}\left(\frac{300}{T}\right)^{\alpha} - \mu_{min}}{1 + \left(\frac{D}{N_{ref}}\right)^{\beta}} + \mu_{min} \tag{5.8}$$

where N_{ref}, μ_{min}, μ_{max}, α and β are fitting parameters, T is temperature and D is the total doping concentration.

The second term in the Equation 5.7 is the the carrier mobility due to scattering involving acoustic phonons, μ_{AC}. Both surface phonon and bulk phonon scattering have been modelled previously [142] [202] [203]. Each show a temperature dependence and both surface and bulk phonon scattering increases with an increase in temperature. Previous research has indicated that phonon scattering has a strong effect on surface mobility in SiC MOSFETs at high gate biases and high temperatures [204] and Potbhare *et al.* showed that surface phonon mobility does not play an important role at temperatures below 200^oC [186]. Phonon scattering is calculated using Equation 5.9.

$$\mu_{AC} = \frac{B}{E} + \frac{CN_A^{\alpha 1}}{TE^{\frac{1}{3}}} \tag{5.9}$$

where B and C are fitting parameters, E is the electric field perpendicular to the MOSFET channel, $\mathrm{N_A}$ is the total doping concentration, T is temperature, and $\alpha 1$ is a factor that indicates the dependency of the mobility term μ_{AC} on the impurity concentration.

Surface roughness scattering is due to the scattering of mobile carriers by imperfections in the SiC surface and is known to cause severe degradation of the surface mobility at high electric fields [200] [205][206]. Surface roughness scattering is calculated using Equation 5.10.

$$\mu_{\mathrm{SR}} = \frac{D1}{E^{\gamma 1}} \tag{5.10}$$

where E is the perpendicular electric field, D1 and $\gamma 1$ are fitting parameters.

Coulomb scattering is a result of carrier interactions with ionized impurities, which are most commonly a product of interface traps at the semiconductor-dielectric interface. Coulomb scattering is believed to dominate carrier mobility at low electric fields and is calculated using Equation 5.11 [198].

$$\mu_C = NT^{\alpha 2}\frac{(Q_{inv})^{\beta 2}}{Q_{trap}} \tag{5.11}$$

where Q_{inv} is the inversion charge per unit area, $\beta 2$ is a fitting parameter, Q_{trap} is the trapped charge per unit area and T is the temperature. In this investigation as Q_{trap} and $\beta 2$ was unknown a simplified formula was derived that has the same functional form but could be fitted to the measure MOSFET field effect mobility characteristics, which is given in Equation 5.12.

$$\mu_C = (E - \lambda)^{\Phi} \tag{5.12}$$

where E is the perpendicular electric field, λ is the onset of mobility, i.e. the point at which the mobility begins to increase, which can be extracted directly from measured characteristics and Φ is the gradient of the increasing mobility.

Figure 5.2 shows a schematic plot of the contributions of the 3 scattering mechanisms that have been discussed (μ_{AC}, μ_{SR} and μ_C). In 4H-SiC the bulk mobility term (μ_{B}) is far higher than the other 3 contributing mechanisms so has a negligible impact on the field effect mobility characteristics of the devices. As this is the case, μ_{B} is omitted from Figure 5.2 and the analysis performed in the remainder of this chapter. As shown in Figure 5.2, Coulomb scattering is most prominent under low electric fields. Surface roughness scattering dominates the mobility characteristics under high applied electric fields as carriers are strongly attracted to the semiconductor surface under high applied biases and therefore have more interactions with the surface.

5.3 Current status of the technology

The current status of 4H-SiC MOSFET technology was outlined in chapter 2. As discussed there has been many recent advancements, however, the technology is still plagued by low channel mobility and oxide reliability issues due to issues with the 4H-SiC/dielectric interface, which is believed to be due to an unoptimised dielectric formation and post oxidation anneal procedure. There has been significant research into the effects of varying post ox-

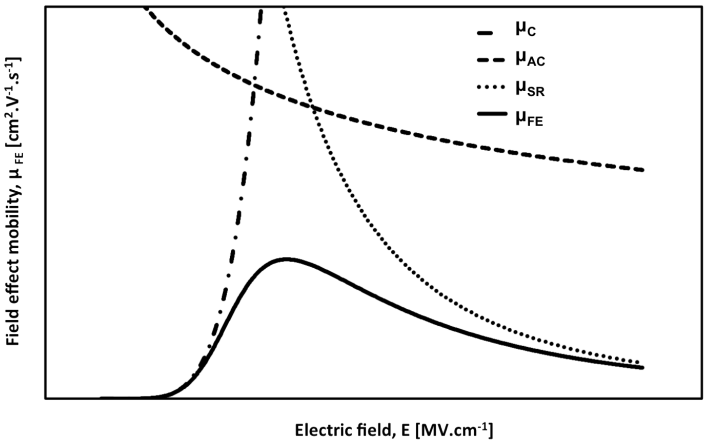


Figure 5.2: Theoretical representation of the mobility scattering mechanisms relating to carrier transport in a MOSFET channel.

idation anneal treatments including the use of hydrogen, oxygen, nitrogen and phosphorus anneal environments, which have previously been used to passivate interface traps in silicon technology. This has led to advances in the capabilities of the technology and MOSFET field effect mobilities of over $100\,\mathrm{cm}^2.\mathrm{V}^{-1}\mathrm{s}^{-1}$ at 298 K have recently been reported in n-channel MOSFETs formed in Al implanted regions after performing a post deposition anneal in $POCl_3$ [143].

5.4 Fabrication techniques and process variation

As described in Chapter 4, in this investigation 3 gate dielectrics on both n and p-type 4H-SiC that have undergone differing process treatments were examined using electrical characterisation of MOSFET structures. The devices studied here were produced using an identical process, except for a distinctive variation in gate dielectric treatments used in their fabrication. The main aim of this investigation is to highlight the benefits and potential issues of each processing technique on the electrical performance of the devices under test.

The 3 distinct samples are known as HV06, CR25 and CR27. Sample HV06 has a thermally grown, annealed oxide, Sample CR25 has a deposited, annealed oxide, which was preceded by a thick, thermally grown sacrificial oxide, while sample CR27 has a thin thermal oxide left in situ under a deposited, annealed oxide. A detailed description of the dielectric growth and post oxidation treatments is given for each of the samples in Table 4.1 in Chapter 4.

The CMOS test structures analysed within this thesis were fabricated on a 100 mm, Si face, 4^o off axis, 4H SiC n+ wafer with a doped epitaxial layer. N and p-type regions and the source and drain regions were formed by ion implantation. The implants were annealed with

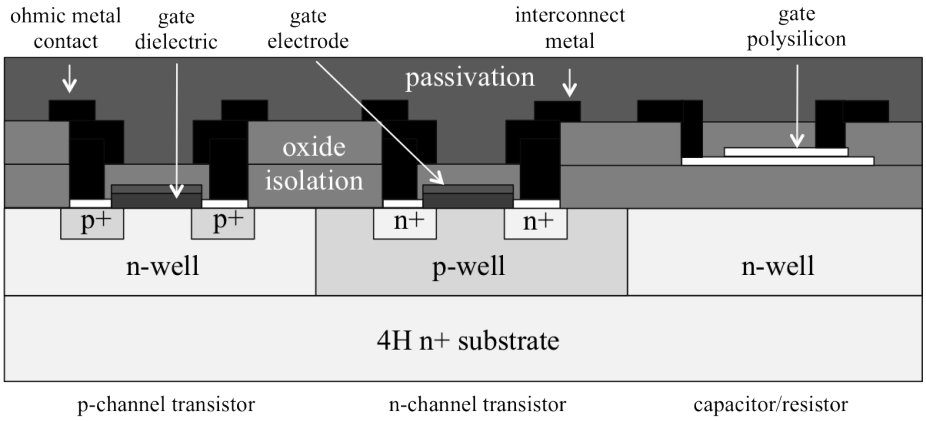


Figure 5.3: Cross-section of CMOS on 4H-SiC.

the surface protected by a carbon cap. A thick field oxide and a thin gate dielectric region were then formed and doped polysilicon gate electrodes. Nickel based contacts were then formed on the doped regions and a refractory metal interconnect was deposited and patterned. Next a thin nickel top layer was applied to protect the pads from oxidation during probe testing at elevated temperatures. Finally an oxide layer was deposited for final passivation and scratch protection and openings were made for bond pads. A schematic of the device cross-section is shown in Figure 5.3

5.5 Temperature dependent electrical characteristics of 4H-SiC MOSFETs

In the following sections the current-voltage characteristics are extracted and explored for the 3 different dielectric samples (HV06, CR25 and CR27) on both n-channel and p-channel 4H-SiC MOSFETs that were fabricated monolithically with the capacitor structures that were analysed in chapter 4. This will involve the extraction of the field effect mobility (μ_{FE}), subthreshold slope (SS) and threshold voltage ($\mathrm{V_{TH}}$) from the measured V_G-$\mathrm{I_D}$ characteristics across a temperature range from 298 K to 498 K with 50 K increments in order to understand the effect of the dielectric processing treatment on the MOSFET characteristics. The extracted field effect mobility for each of the samples is also fitted to the theoretical model for mobility using Equation 5.6 in order to predict the mobility limiting mechanisms for each of the MOSFETs and the impact of temperature on the mobility limiting mechanisms involved. All of the electrical characteristics discussed in this chapter were extracted using a Keithley 4200 SCS Parameter Analyser.

5.5.1 Temperature dependent electrical characteristics of n-channel 4H-SiC MOSFETs

The data in Figure 5.4, 5.5 and 5.6 show the V_{GS}-I_{DS} characteristics for a 400 × 1.5 μm n-channel MOSFET for sample HV06, CR25 and CR27, respectively, measured from 298 K to 498 K. The drain bias in each of the measurements was 500 mV. Each of the samples show a similar trend and there is an increase in drain current, a reduction in threshold voltage and a change in the subthreshold slope with increasing temperature. The data for HV06 in Figure 5.4b show a much higher off-state leakage current, with subthreshold drain currents consistently around 0.1 nA, whereas CR25 (Figure 5.5b) and CR27 (Figure 5.6b) show reverse leakage current of approximately 1 pA. The offstate conduction could be due to counter doping in the channel region, which could be a product of the threshold adjust implant [207]. This counter doping could have also been increased as an unwanted effect during the 1200 ^{o}C to the N_2O post oxidation anneal that was performed on the dielectric as described in Table 4.1.

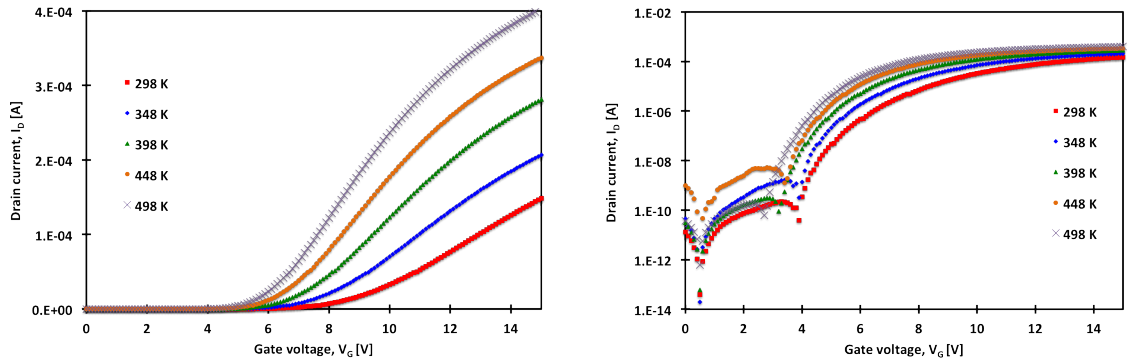


Figure 5.4: V_G-I_D characteristics of a 400 × 1.5 μm HV06 n-channel MOSFET from 298 K to 498 K.

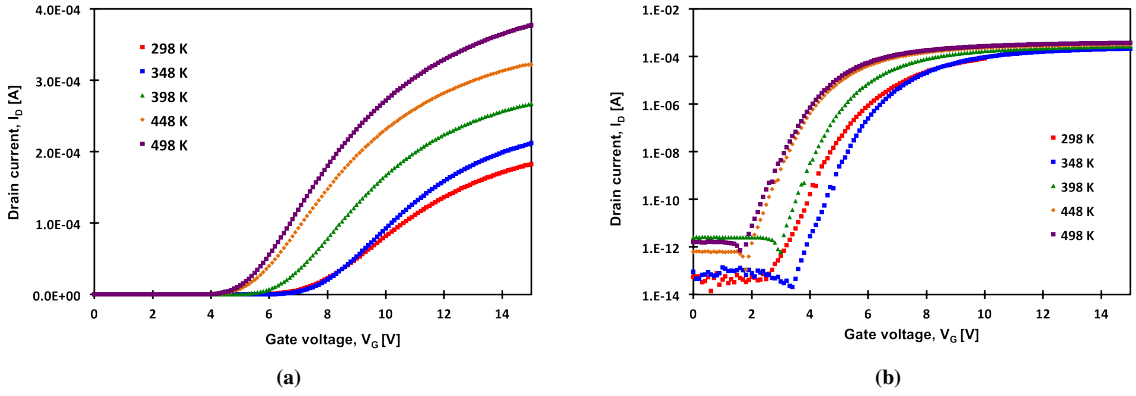


Figure 5.5: V_G-I_D characteristics of a 400 × 1.5 μm CR25 n-channel MOSFET from 298 K to 498 K.

The increase in current with temperature observed in Figures 5.4a, 5.5a and 5.6a for the 3 samples is due to the decrease of occupied interface traps with an increase in temperature,

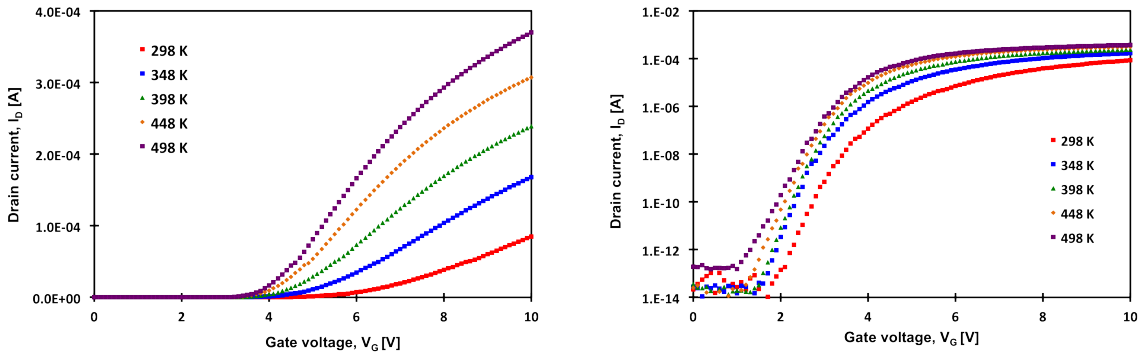


Figure 5.6: V_G-I_D characteristics of a 400 × 1.5 μm CR27 n-channel MOSFET from 298 K to 498 K.

which is an agreement with data analysed in subsection 4.7.1. As the density of interface traps decreases with increasing temperature, at a given gate voltage, more carriers are available for conduction in the channel. This finding also supports previous work conducted in the field [186].

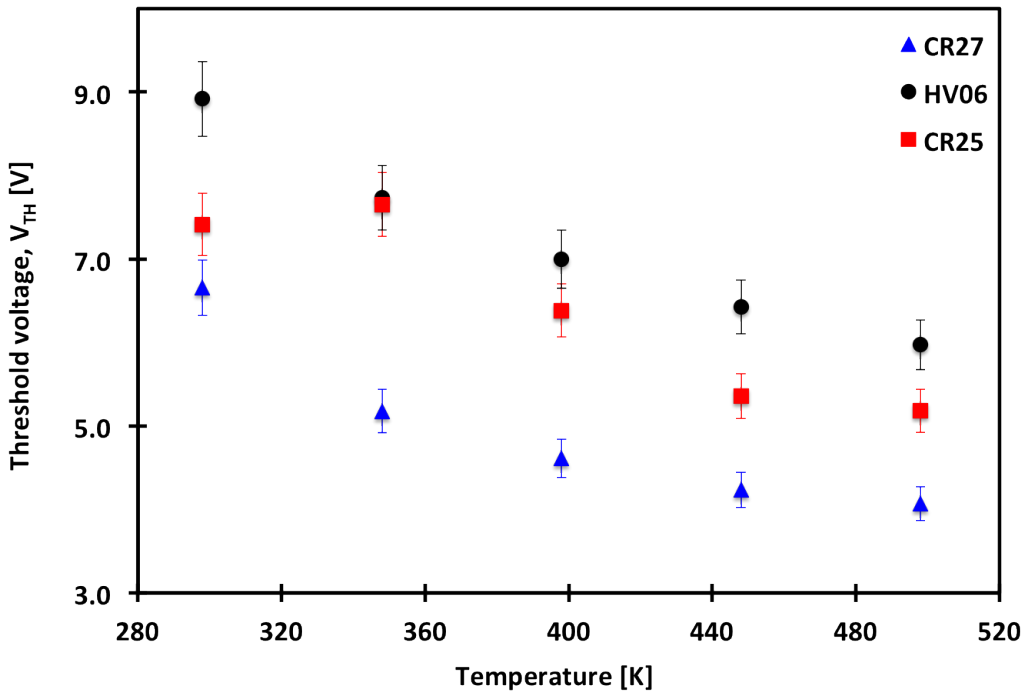


Figure 5.7: Threshold voltage (V_{TH}) against temperature for 400 × 1.5 μm HV06, CR25 and CR27 n-channelMOSFETs.

The reduction in threshold voltage with temperature is also shown for each of the transistors across the temperature range in Figure 5.7. Threshold voltage can be calculated using Equation 5.13 [1].

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{2\varepsilon_0\varepsilon_s q N_A 2\phi_B}}{C_i} \tag{5.13}$$

The V_{TH} shift with temperature is due to the reduction in the surface band bending required for inversion, which is due to the increase in thermal energy (kT/q), the increase in intrinsic carrier concentration, the increase in the effective density of states in the conduction and valence bands and the decrease in band gap energy with an increase in temperature as described in subsection 4.7.1. However, a change at the interface and within the depletion layer can also act to modify the gate voltage as V_{FB} is dependent on the oxide charges, as shown by Equation 4.46.

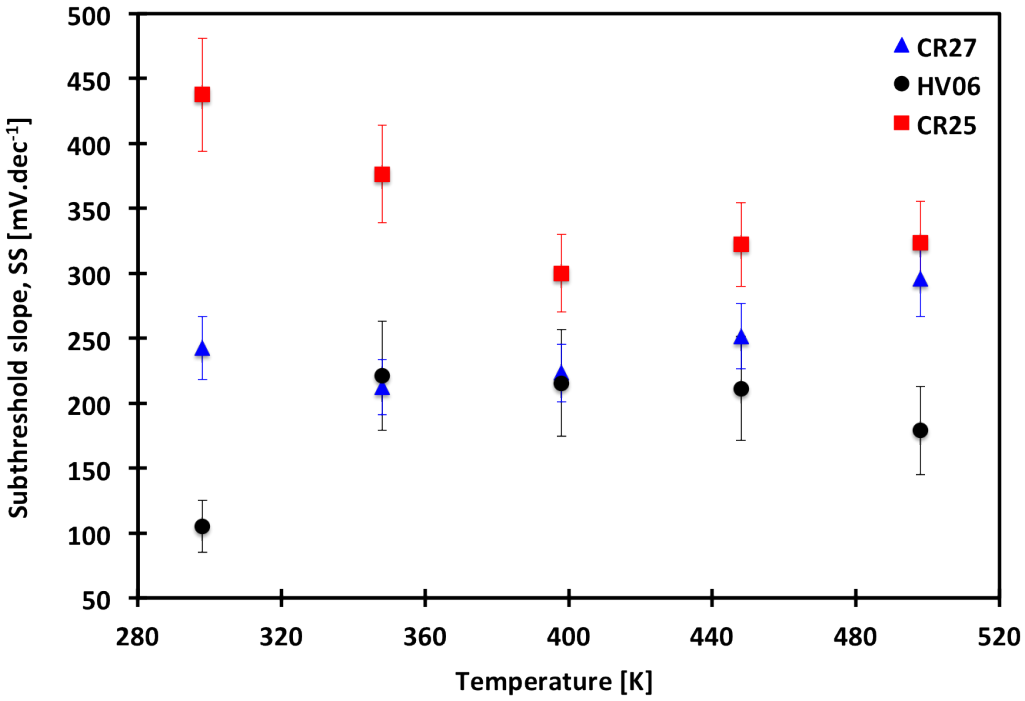


Figure 5.8: Subthreshold slope (SS) against temperature for $400 \times 1.5\,\mu$m HV06, CR25 and CR27 n-type MOSFETs.

Figure 5.8 shows the subthreshold slope (SS) against temperature for each of the samples. As shown by the data, both HV06 and CR27 show either a constant SS with T or an increase in SS with temperature, whereas CR25 shows a decrease in SS. An increase in the subthreshold slope with temperature is expected as SS is proportional to kT/q. The decrease of SS with temperature that is witnessed for CR25 suggests that there is a change in the interface trapped charge at the semiconductor dielectric interface as subthreshold slope is also dependent on the interface trap capacitance (C_{it}) as outlined in Equation 5.14, where C_D is equal to the depletion capacitance of the semiconductor [1]. However, the increase in mobility with temperature that is exhibited by the devices and the variation in the type of oxide used is inconsistent with the witnessed SS - temperature response.

$$SS = ln(10)\left(\frac{kT}{q}\right)\left(\frac{C_i + C_D + C_{it}}{C_i}\right) \tag{5.14}$$

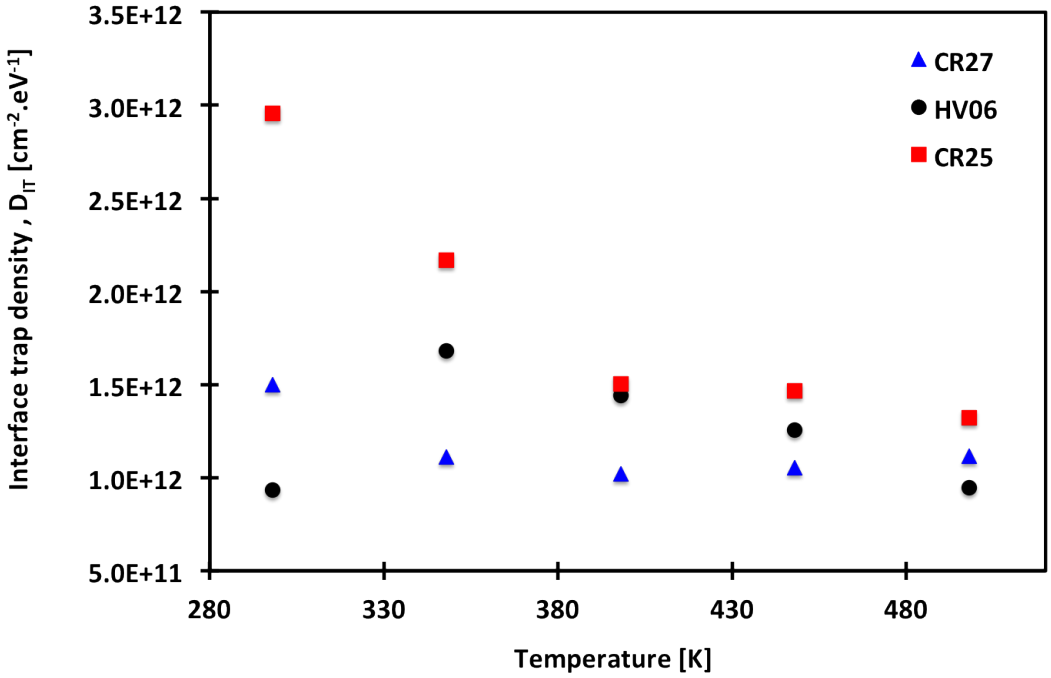


Figure 5.9: Interface trap density against temperature for 400 × 1.5 μm HV06, CR25 and CR27 n-type MOSFETs as extracted from the subthreshold slope.

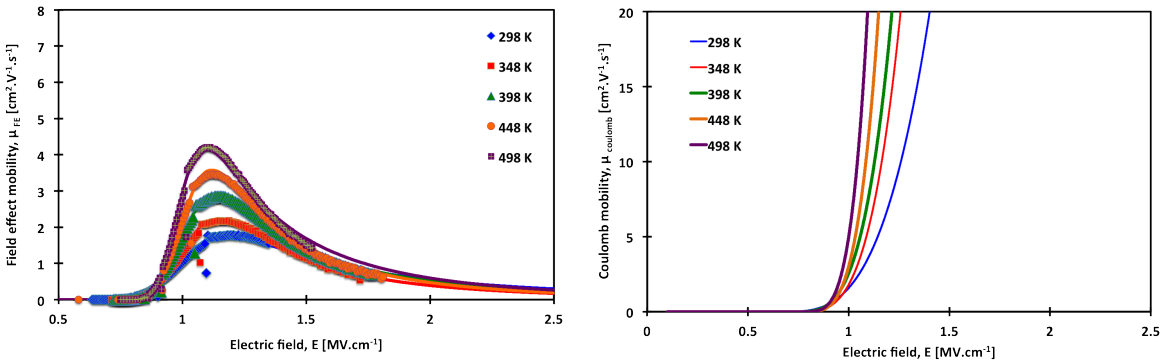


Figure 5.10: (a)μ_{FE}-E and (b) μ_{Coulomb}-E characteristics of a 400 × 1.5 μm HV06 n-channel MOSFET from 298 K to 498 K.

This is also in agreement with the change in interface trap density with temperature that was witnessed within both the CR25 n-type and p-type MIS capacitors that were analysed in section 4.7. This is most likely due to the change in D_{it} with temperature, which was observed at both the conduction band and valence band edges in the semiconductor for both the n-type and p-type CR25 MIS capacitors, respectively. The data in Figure 5.9 show a plot

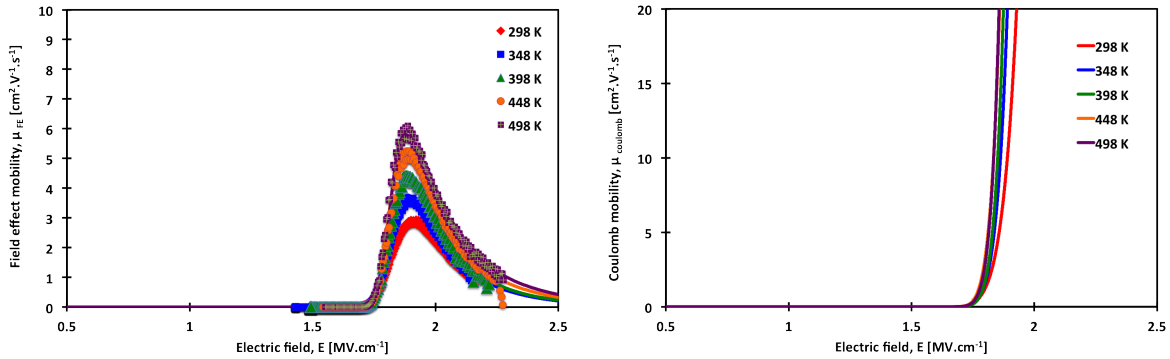


Figure 5.11: (a)μ_{FE}-E and (b) μ_{Coulomb}-E characteristics of a 400 $\times$ 1.5 μm CR25 n-channel MOSFET from 298 K to 498 K.

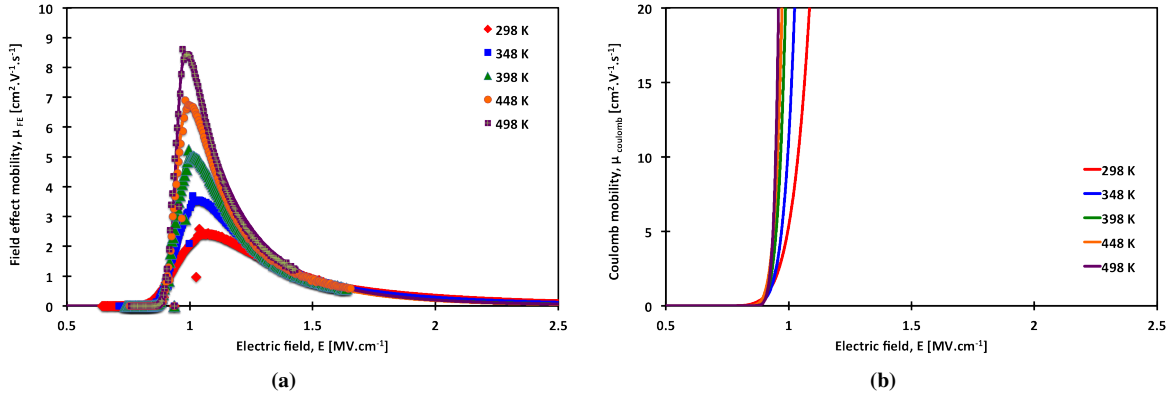


Figure 5.12: (a)μ_{FE}-E and (b) μ_{Coulomb}-E characteristics of a 400 $\times$ 1.5 μm CR27 n-channel MOSFET from 298 K to 498 K.

of D_{it} vs T as extracted from the subthreshold slope of each of the MOSFET devices using Equation 5.14. As shown, CR25 shows the greatest change with temperature and decreases from 3×10^{12} to 1.5×10^{12} cm^{-2}.eV^{-1} between 298 and 498 K.

The data in Figure 5.10, 5.11 and 5.12 show the μ_{FE}-E and the μ_{Coulomb}-E characteristics for a 400 $\times$ 1.5 μm n-channel MOSFET measured between 298 K and 498 K taken from samples HV06, CR25 and CR27, respectively. The field effect mobility was extracted from the $V_{GS} - I_{\mathrm{DS}}$ data sets in Figure 5.4, 5.5 and 5.6 using Equation 5.2. All exhibit a similar trend and show an increase in field effect mobility with increasing temperature. The data in Figure 5.12 for CR27 show the highest field effect mobility across the temperature range out of the 3 samples as supported by the data in Figure 5.16, which show the peak field effect mobility of each device against temperature.

Figures 5.10b, 5.11b and 5.12b show the extracted Coulomb mobility values that were fitted to the measured characteristics using Equation 5.11. As shown by the data, all of the devices show an increase in Coulomb mobility with increasing temperature, which suggests

that the effect of Coulomb scattering reduces with an increase in temperature.

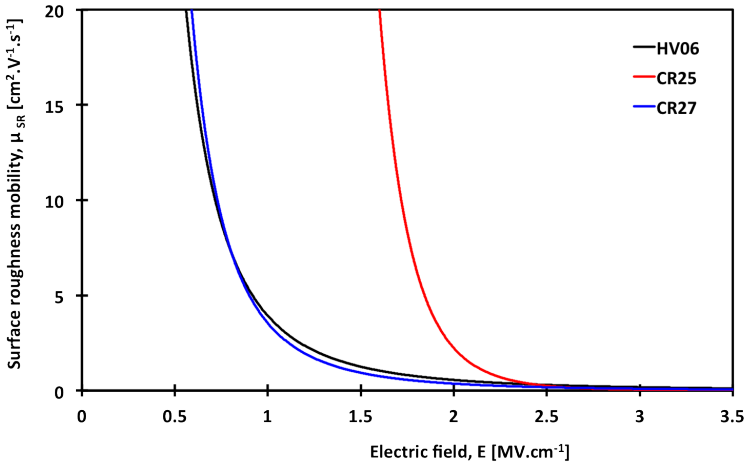
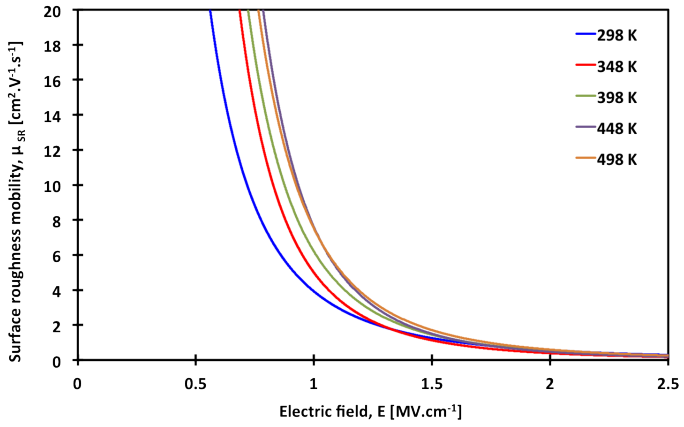
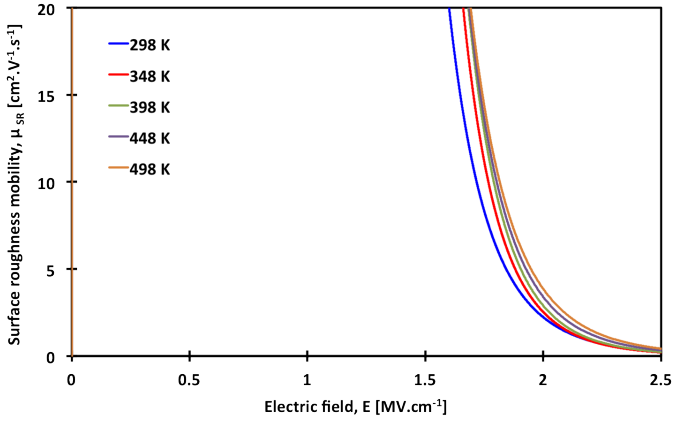


Figure 5.13: Surface roughness mobility (μ_{SR}) against electric field (E) for $400 \times 1.5\,\mu$m HV06, CR25 and CR27 n-channel MOSFETs at 298 K.

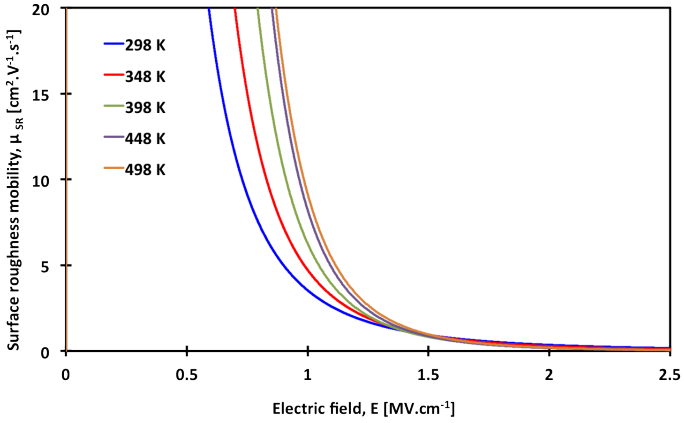
At high electric fields the extracted values of μ_{FE} for each of the devices is limited by surface roughness scattering as shown by the data in Figure 5.14, which shows the values of μ_{SR} fitted to each of the extracted MOSFET μ_{FE} characteristics between 298 K and 498 K. The data show that the experimental μ_{SR} has the same functional form as Equation 5.10 [208]. The data in Figure 5.13 show the extracted μ_{SR} as a function of electric field for each of the samples at 298 K. This clearly identifies that the observed surface roughness mobility, varies dependent on the dielectric under investigation. HV06 and CR27 show the lowest surface roughness mobility, which suggests that surface roughness scattering is higher within those devices. CR25 shows the highest surface roughness mobility, which suggests that the process techniques used in the fabrication of this sample produce the highest quality dielectric-semiconductor interface out of the 3 samples investigated.



(a)



(b)



(c)

Figure 5.14: μ_{SR}-E characteristics of a 400 $\times$ 1.5 μm (a)HV06, (b) CR25 and (c) CR27 n-channel MOSFET from 298 K to 498 K.

The data in Figure 5.15 show the theoretical acoustic phonon mobility (μ_{AC}) data that was fitted to each of the samples using Equation 5.9. The set of fitting parameters for μ_{AC} are B, C and α1. The same values for the fitting parameters were used for all 3 dielectric samples on both n-channel and p-channel devices and were equal to the values that have

been reported and used previously in the literature [200][208]. B is 1.0×10^6 cm.s^{-1}, C is 3.23×10^6 K.cm.s^{-1} and $\alpha 1$ is 0.0284. As shown, in Figure 5.15 the modelled acoustic phonon mobility is consistently above 100 cm^2.V^{-1}.s^{-1} across the scanned electric field and temperature range. As this is significantly higher than both μ_{SR} and μ_{Coulomb} it has a very small effect on the total field effect mobility in each of the devices. The characteristics are dominated at low and high electric fields by Coulomb and surface roughness scattering as shown by the data in Figures 5.10b, 5.11b, 5.12b and 5.14.

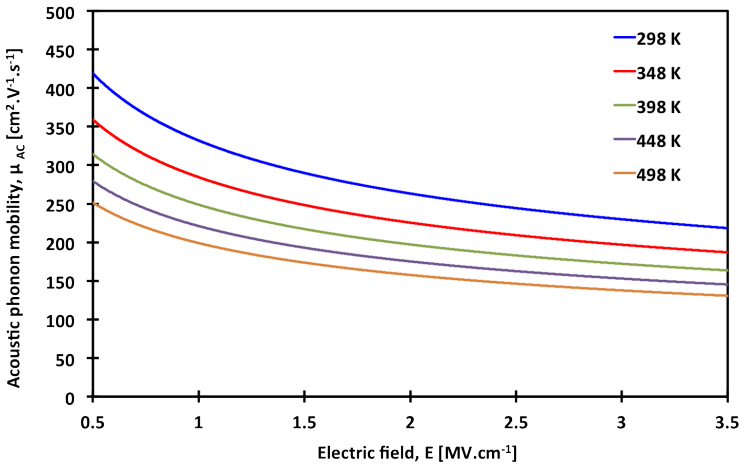


Figure 5.15: μ_{AC}-E characteristics of a 400 $\times$ 1.5 μm HV06 n-channel MOSFET from 298 K to 498 K.

The main limiting factor that is witnessed across all of the samples is that of severely low surface roughness mobility, which acts to dominate the device mobility characteristics from electric fields above 1 MV.cm^{-1}. The surface roughness mobility shown by all 3 dielectrics is up to an order of magnitude lower than other 4H-SiC MOSFETs that have previously been reported which showed field effect mobility of consistently over 20 cm^2.V^{-1}.s^{-1} at high electric fields [153, 154, 200, 209, 210]. The behaviour of mobility with temperature could also be related to the Schottky barriers in the metal contacts that were discussed in Chapter 3, therefore, further investigations to establish the contribution of the contact behaviour to the MOSFET mobility behaviour would be very useful to help improve the mobility characteristics.

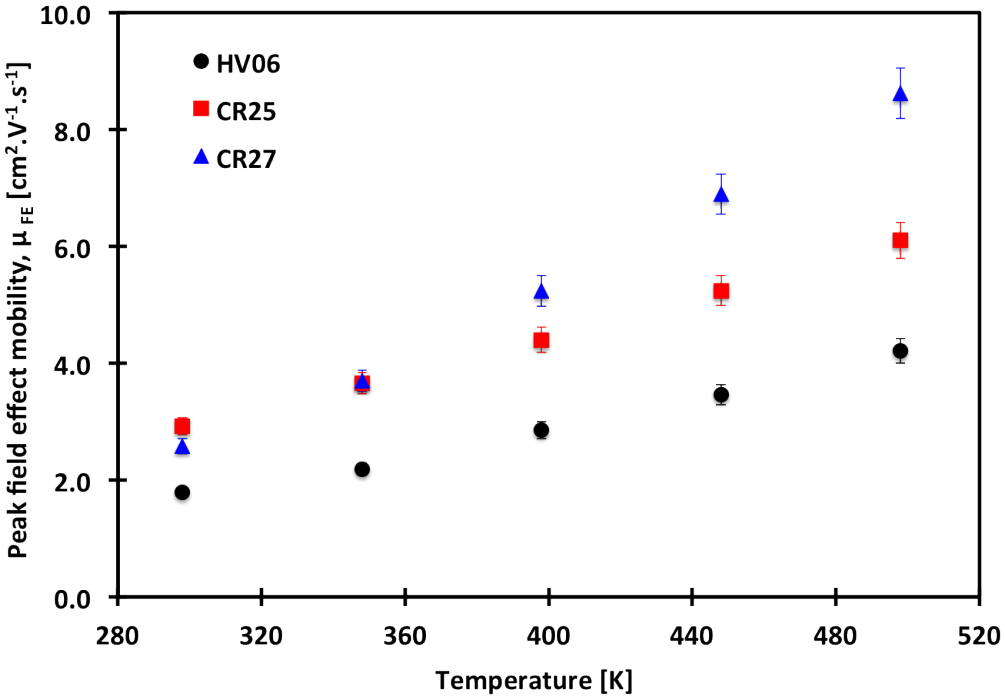
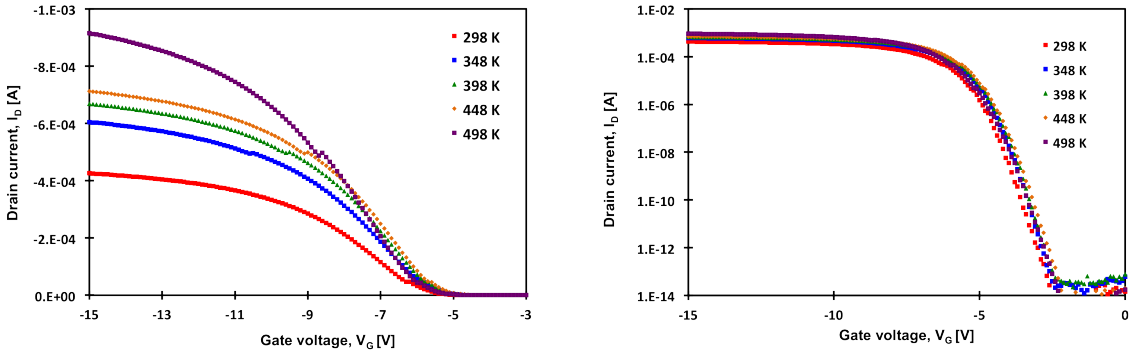


Figure 5.16: Peak field effect mobility (μ_{FE}) against temperature for $400 \times 1.5\,\mu$m HV06, CR25 and CR27 n-channel MOSFETs.

5.5.2 Temperature dependent electrical characteristics of p-channel 4H-SiC MOSFETs

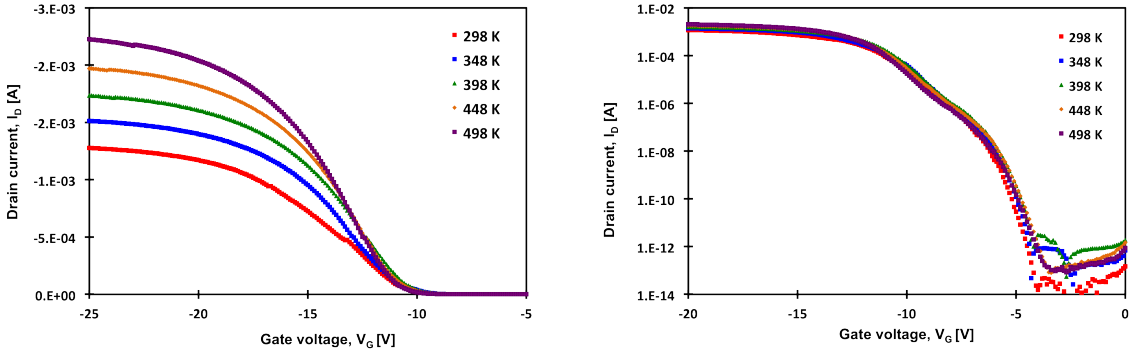
The data in Figure 5.17, 5.18 and 5.19 show the V_{GS}-I_{DS} and the V_{GS}-$log(I_{DS})$ characteristics for a 1600×1.5 μm HV06 p-channel MOSFET and a $8000 \times 1.5\,\mu$m CR25 and CR27 p-channel MOSFET, respectively, measured from 298 K to 498 K. The drain bias in each of the measurements was 500 mV. The discontinuities in Figure 5.17 and 5.19 are due to instrumentation error caused by the re-ranging of the current measurments on the Keithley 4200 SCS Parameter Analyser. The discontinuities do not affect the subsequent analysis in this chapter. As shown by the data, each of the samples exhibits a similar trend and there is an increase in drain current with increasing temperature, a change in threshold voltage and a change in the subthreshold slope across the measured temperature range. All samples exhibit a very low reverse leakage current of below 1 pA as shown in Figure 5.17b, 5.18b and 5.19b.

The change in threshold voltage with temperature is also shown for each of the transistors across the temperature range in Figure 5.20. Threshold voltage can be calculated using Equation 5.13 [1]. As with the n-channel devices CR27 shows a reduction in $\mathrm{V_{TH}}$ with temperature due to the reduction in the surface band bending required for inversion, which is due to the increase in intrinsic carrier concentration and the decrease in band gap energy with increasing temperature as described in subsection 4.7.1. HV06 and CR25 show a very minimal change in $\mathrm{V_{TH}}$ with an increase in temperature, however, CR25 may exhibit an increase in



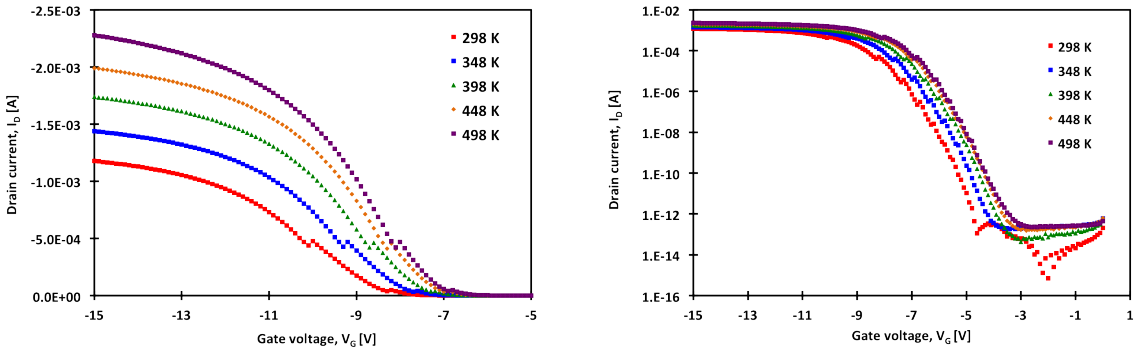
(a) **(b)**

Figure 5.17: V_G-I_D characteristics of a 1600 $\times$ 1.5 μm HV06 p-channel MOSFET from 298 K to 498 K.



(a) **(b)**

Figure 5.18: V_G-I_D characteristics of a 8000 $\times$ 1.5 μm CR25 p-channel MOSFET from 298 K to 498 K.



(a) **(b)**

Figure 5.19: V_G-I_D characteristics of a 8000 $\times$ 1.5 μm CR27 p-channel MOSFET from 298 K to 498 K.

V_{TH} with temperature. This could be due to a change in the interfacial charge or a change in the charge in the depletion layer, which can also act to modify the gate voltage as V_{FB} is dependent on the oxide charges as shown in Equation 4.46. This is likely to be due to the increase in D_{it} with temperature that was witnessed for the equivalent MOS capacitor structure in subsection 4.7.1 and the effects of mobile oxide charge present within the dielectric.

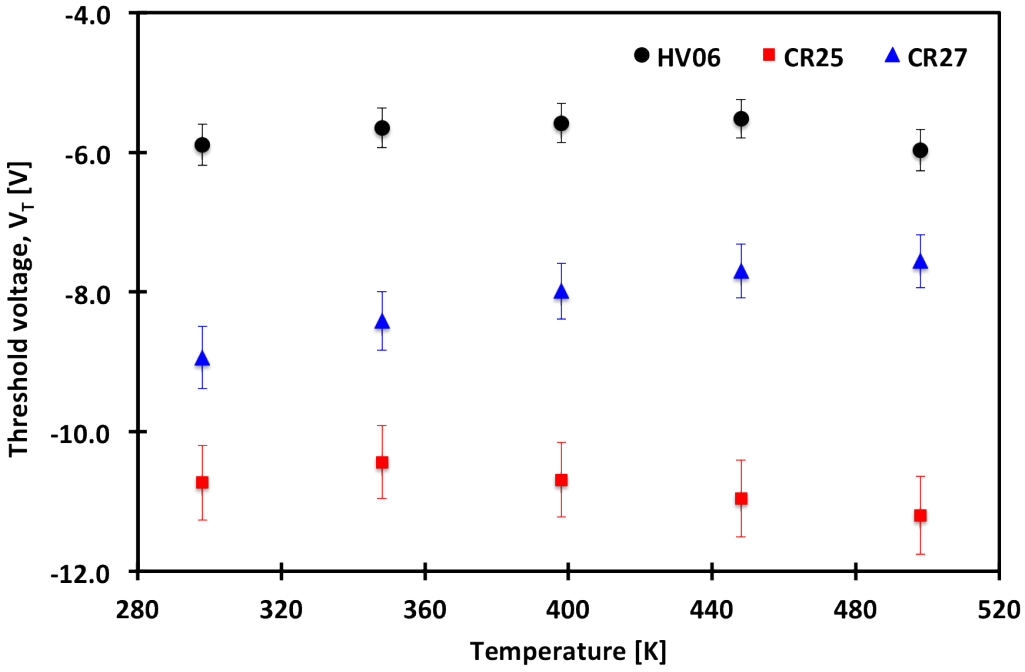


Figure 5.20: Threshold voltage (V_{TH}) against temperature for a 1600×1.5 μm HV06, and a 8000×1.5 μm CR25 and CR27 p-channel MOSFET.

The increase in current with temperature that is witnessed in Figures 5.17a, 5.18a and 5.19a for the 3 samples is due to the decrease of occupied interface traps with an increase in temperature, which is an agreement with the findings in subsection 4.7.1. As the density of interface traps decreases with increasing temperature, at a given gate voltage, more carriers are available for conduction in the MOSFET channel. This finding is in agreement with results published in the literature [186].

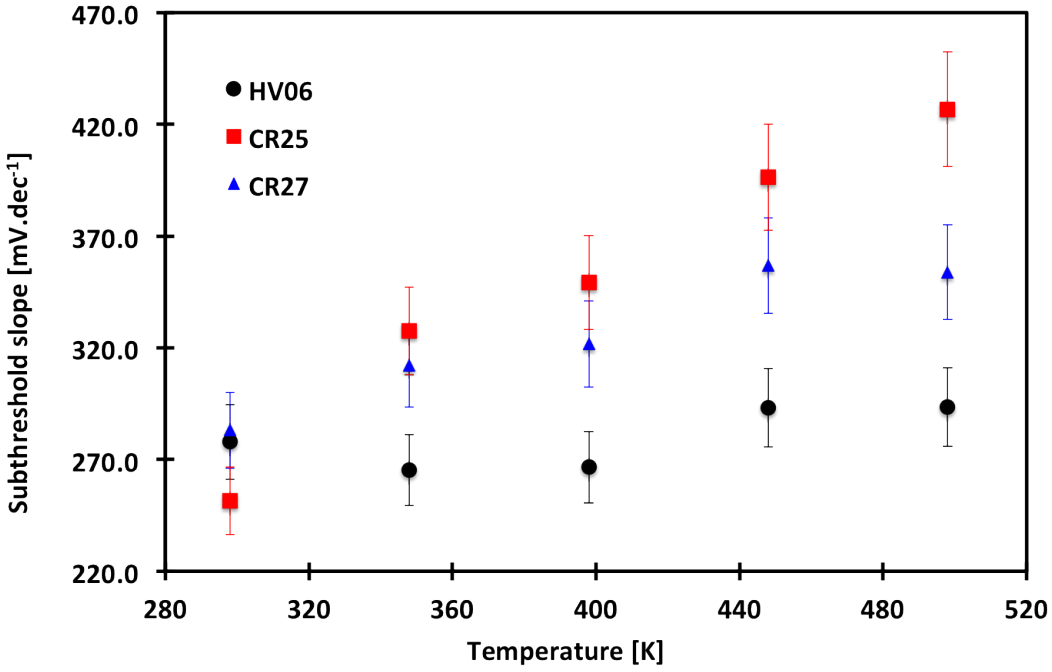
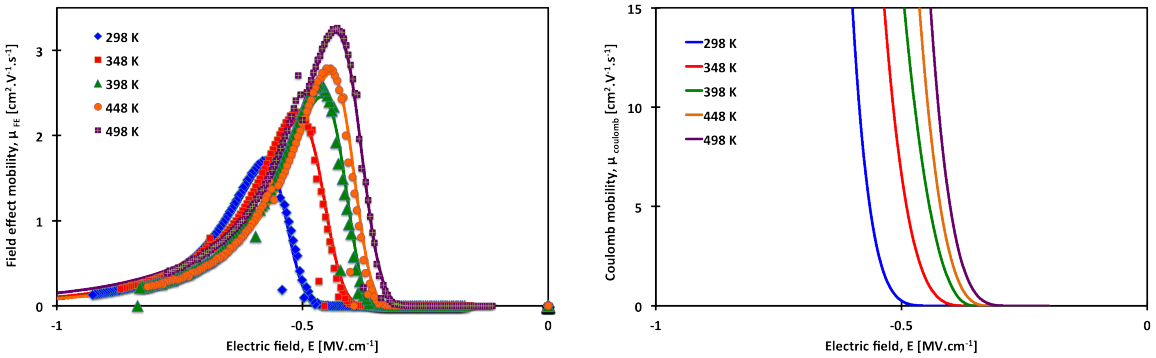


Figure 5.21: Subthreshold slope (SS) against temperature for a 1600×1.5 μm HV06, and a 8000×1.5 μm CR25 and CR27 p-channel MOSFET.

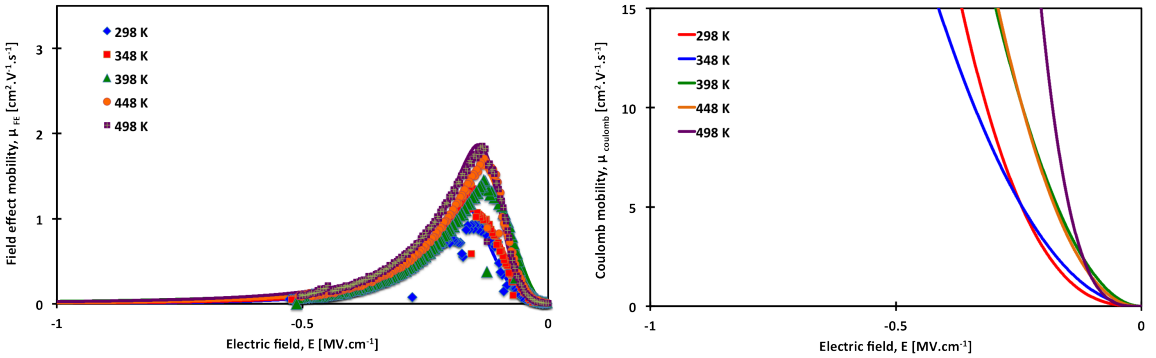
The data in Figure 5.21 show the variation in subthreshold slope (SS) with temperature for each of the samples. As shown, all 3 samples show an increase in SS with temperature. An increase in SS with temperature is expected as SS is proportional to kT/q. The variation in SS with temperature is also influenced by the interface trapped charge at the semiconductor dielectric interface as SS is also dependent on the interface trap capacitance (C_{it}) as outlined in Equation 5.14. This is in agreement with the trend witnessed for the equivalent n-channel MOSFET samples with the exception of sample CR25. The n-channel equivalent sample for CR25 showed a decrease in with SS with temperature, whereas the p-channel device exhibits an increase in SS for increasing temperature and the observed change is much smaller than that of the n-channel device. This could be due to the different variation in D_{it} over the measured temperature range, which was extracted from the equivalent MIS capacitor structures in section 4.7. However, as with the n-channel counterparts, the increase in mobility with temperature that is exhibited by the devices and the variation in the type of oxide used is inconsistent with the witnessed SS - temperature response.

The data in Figure 5.22, 5.23 and 5.24 show the μ_{FE}-E and the $\mu_{Coulomb}$-E characteristics for a 1600×1.5 μm p-channel MOSFET on HV06 and a 8000×1.5 μm p-channel MOSFET on CR25 and CR27, respectively, measured from 298 K to 498 K. All exhibit an increase in field effect mobility with increasing temperature. The data for CR27 in Figure 5.24 show the highest field effect mobility across the temperature range out of the 3 samples.



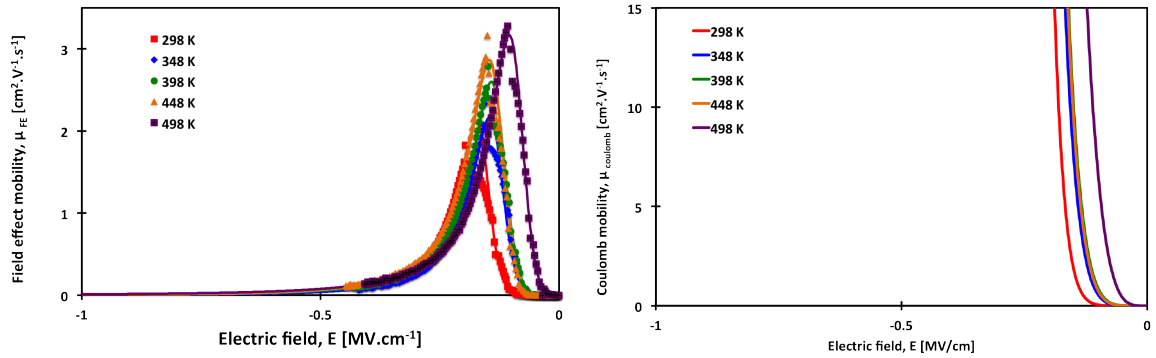
(a) (b)

Figure 5.22: (a)μ_{FE}-E and (b) μ_{Coulomb}-E characteristics of a 1600×1.5 μm HV06 p-channel MOSFET from 298 K to 498 K.



(a) (b)

Figure 5.23: (a)μ_{FE}-E and (b) μ_{Coulomb}-E characteristics of a 8000×1.5 μm CR25 p-channel MOSFET from 298 K to 498 K.



(a) (b)

Figure 5.24: (a)μ_{FE}-E and (b) μ_{Coulomb}-E characteristics of a 8000×1.5 μm CR27 p-channel MOSFET from 298 K to 498 K.

The data in Figure 5.22, 5.23 and 5.24 show the μ_{FE}-E and the μ_{Coulomb}-E characteristics for a 1600×1.5 μm p-channel MOSFET on HV06 and a 8000×1.5 μm p-channel MOSFET on CR25 and CR27, measured from 298 K to 498 K. The field effect mobility was extracted

from the V_{GS}-I_{DS} data sets shown in Figure 5.17, 5.18 and 5.19 using Equation 5.2. All devices studied exhibit a similar trend and show an increase in field effect mobility with increasing temperature. The data for CR27 shown in Figure 5.24 demonstrates the highest field effect mobility across the temperature range out of the 3 samples as supported by Figure 5.25, which shows the peak field effect mobility of each device against temperature.

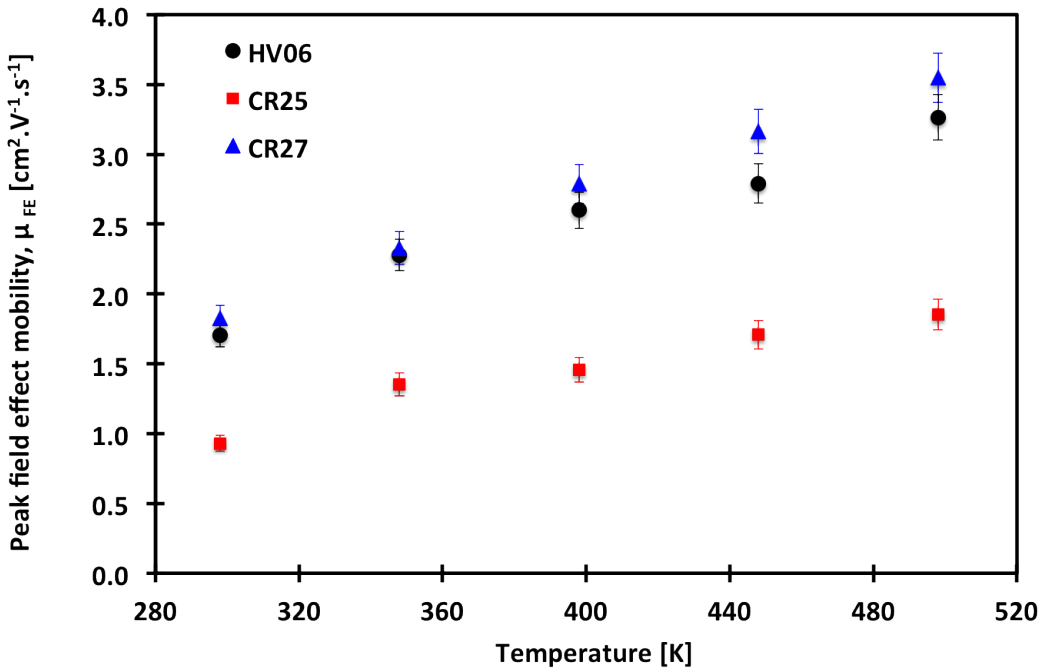


Figure 5.25: Peak field effect mobility (μ_{FE}) against temperature for a 1600×1.5 μm HV06, and a 8000×1.5 μm CR25 and CR27 p-channel MOSFET.

The data in Figure 5.22b, 5.23b and 5.24b show the Coulomb mobility mechanism that was fitted to the measured characteristics using Equation 5.11. As shown by the data in the figures, all of the devices (HV06, CR25 and CR27) show an increase in mobility with increasing temperature, which suggests that the effect of Coulomb scattering reduces with an increase in temperature due to the reduction of interface trapping effects with increasing temperature. The same phenomenon was also witnessed in the equivalent n-channel MOSFETs in subsection 5.5.1, which suggest the dominant mobility mechanisms are consistent in both the n and p-channel devices with the gate dielectrics.

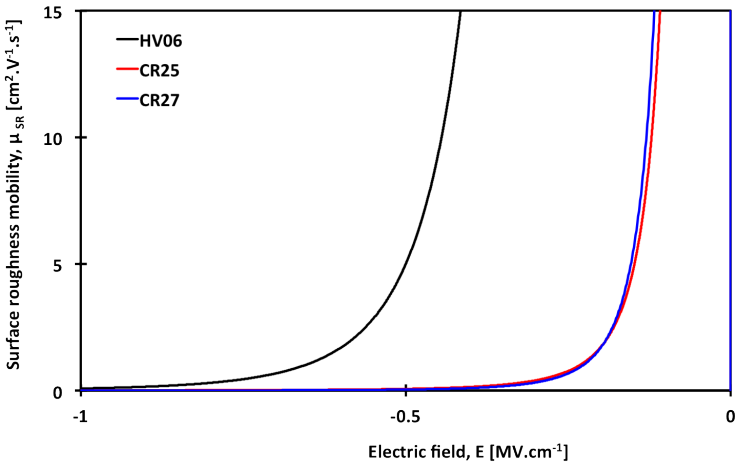
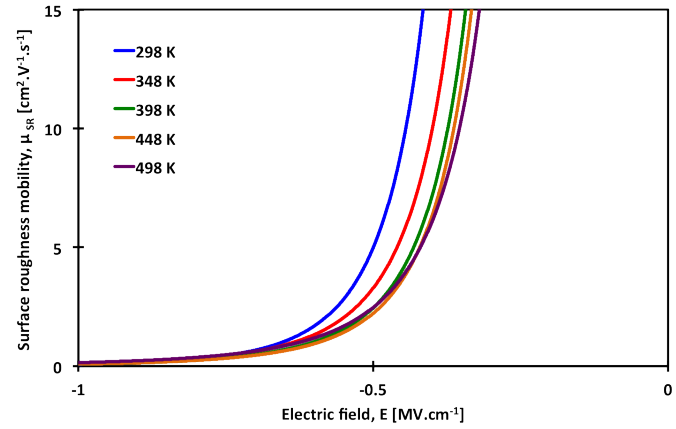
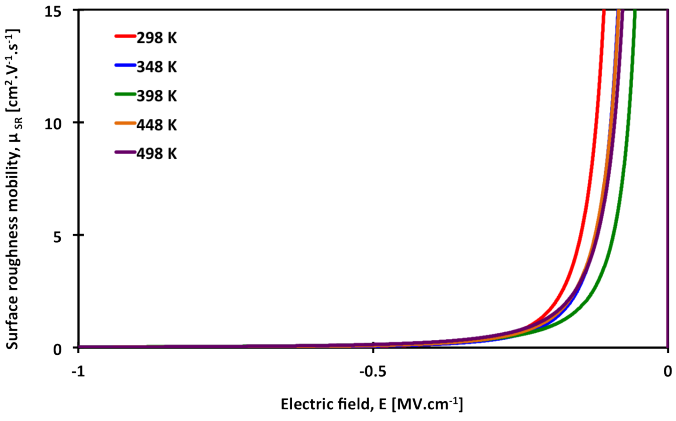


Figure 5.26: μ_{SR}-E characteristics of a 1600×1.5 μm HV06, and a 8000×1.5 μm CR25 and CR27 p-channel MOSFET at 298 K.



(a)



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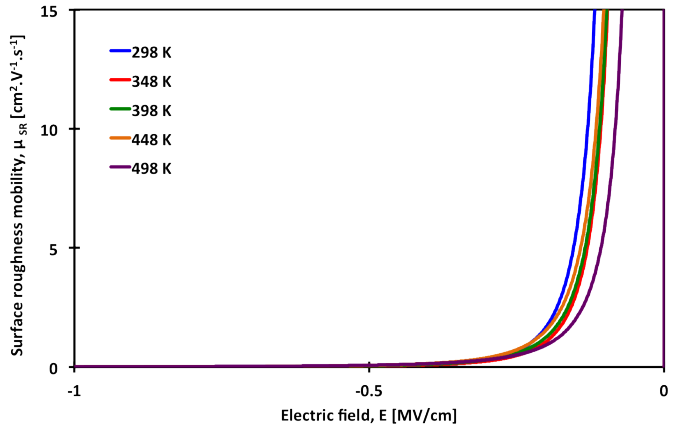

(c)

Figure 5.27: μ_{SR}-E characteristics of a 1600×1.5 μm (a)HV06, and a 8000×1.5 μm (b) CR25 and (c) CR27 p-channel MOSFET from 298 K to 498 K.

At high electric fields the μ_{FE} of each of the devices is limited by surface roughness scattering as shown by the data in Figure 5.27, which show the μ_{SR} mobility fits to each of the extracted MOSFET μ_{FE} characteristics between 298 K and 498 K.The data show that the experimental μ_{SR} has the same functional form as Equation 5.10 [208]. The data in

Figure 5.26 show the fitted μ_{SR} against electric field for each of the samples as 298 K. This clearly identifies that the surface roughness mobility is different for each of the dielectrics under investigation. HV06 shows the highest surface roughness mobility, which suggests that surface roughness scattering is lower within the device and produces the highest quality dielectric-semiconductor interface out of the 3 samples investigated. CR25 and CR27 show similar surface roughness mobility across the measured electric field range, which suggests that the process techniques used in the fabrication of those samples produce a very similar interface. However, all of the devices show very low field effect mobility at high electric fields, which is lower than recent reported field effect mobilities for 4H-SiC devices, which are given in Table 2.7. This suggests that there is something within the shared fabrication process of all of the samples that consistently acts to reduce the surface roughness mobility. This could be due to the topography of the 4H-SiC epitaxial layer that was used for the fabrication of the devices or could potentially be a contribution of surface damage due to the ion implantation doping or the post-implantation anneal process that was used to form the n-type regions that are employed across all of the p-channel devices. In order to establish if this is the true cause an investigation of the surface morphology could be conducted using atomic force microscopy techniques after the implantation and anneal process to measure the surface roughness, which could then be correlated to the measured electrical characteristics of the devices. Similar studies have previously been conducted on n-channel 4H-SiC MOSFETs to establish the impact of the morphological and electrical properties of the SiO_2/4H-SiC interface on the mobility behaviour of 4H-SiC MOSFETs, which have showed that a higher mobility can be found in rougher interfaces due to lower values of D_{it} associated to faceted surface morphologies [211]. However, limited data is available to present if there is a strong dependency between mobility and faceted surface morphologies. Further investigation on the devices, which have been analysed within this thesis could provide useful insight into this relationship. The behaviour of mobility with temperature could also be related to the Schottky barriers in the metal contacts that were discussed in Chapter 3, therefore, further investigations to establish the contribution of the contact behaviour to the MOSFET mobility behaviour would be very useful to help improve the mobility characteristics.

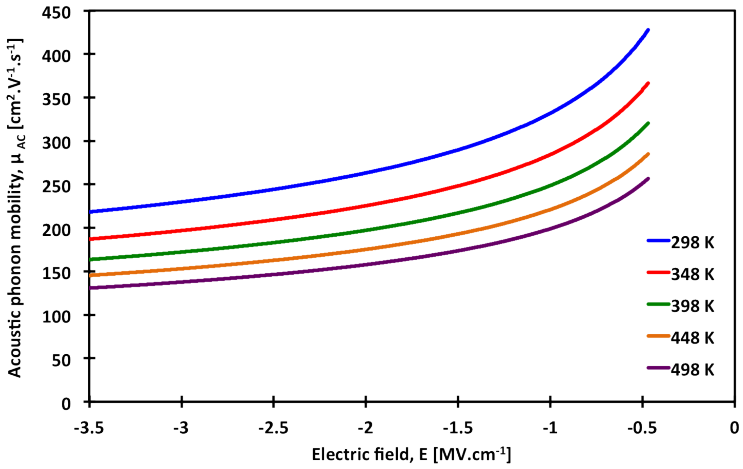

Figure 5.28: μ_{AC}-E characteristics of a 8000×1.5 μm CR25 p-channel MOSFET from 298 K to 498 K.

The data in Figure 5.28 show the acoustic phonon mobility (μ_{AC}) mechanism that was fitted to each of the samples using Equation 5.9. The set of fitting parameters for μ_{AC} are B, C and $\alpha 1$. The same values for the fitting parameters were used for all 3 dielectric samples on both n-channel and p-channel devices and were equal to the values that have been reported and used previously in the literature [200][208]. B is 1.0×10^{6} cm.s^{-1}, C is 3.23×10^{6} K.cm.s^{-1} and $\alpha 1$ is 0.0284. As shown, in Figure 5.28 the modelled acoustic phonon mobility is consistently above 150 cm^2.V^{-1}.s^{-1} across the entire scanned electric field and temperature range. As this is significantly higher than both μ_{SR} and μ_{Coulomb} it has a very small effect on the total field effect mobility in each of the devices. The characteristics are consistently dominated at low and high electric fields by Coulomb and surface roughness scattering as shown in Figure 5.22b, 5.23b, 5.24b and 5.27.

5.6 Impact of gate dielectric on the 1/f noise characteristics of 4H-SiC MOSFETs

Low frequency noise (1/f noise) measurements are used to study impurities and defects in semiconductor devices. The technique is useful to investigate device quality and reliability issues as well as the examination of the density of interface states in MOS devices. While 1/f noise dominates the low frequency region (up to 100 kHz), it can be up converted into a high frequency component affecting the phase noise characteristics of devices used for RF applications [212] as well as degrading the signal to noise ratio in analogue circuitry. Very few studies of the 1/f noise in 4H-SiC have been explored to date [213][214][215]. In this thesis low frequency noise is used to investigate how the gate dielectric influences the interface trap density and hence the characteristics of the 4H-SiC MOSFETs. The aim is to determine the impact of the interface quality and resulting noise characteristics on the device

performance.

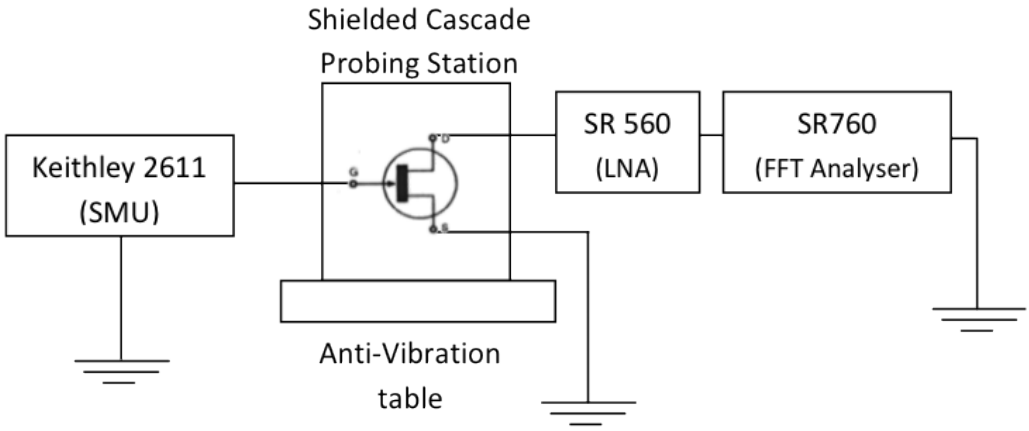

Figure 5.29: Schematic diagram of low frequency noise measurement setup.

The low frequency noise measurements were conducted using a Stanford Research 760 FFT at 298 K and the current-voltage characteristics that were used to normalise the characteristics were conducted on a Keithley 4200 SCS semiconductor analyser. A schematic of the measurement setup is shown in Figure 5.29.

The normalised 1/f noise characteristics for each of the dielectrics on the n-channel MOSFETs are shown in Figure 5.30, 5.31 and 5.32 for HV06, CR25 and CR27, respectively, which show a plot of the NNPSD at 10 Hz against V_{GS} and $\mathrm{I_{DS}}$ is shown for each of the devices. All of the devices exhibit a similar characteristic and suggest that 1/f noise is higher during weak inversion and reduces in the strong inversion regime. The observed trends for each of the devices suggests that mobility fluctuations are the main contributor to the noise characteristics. During weak inversion the $\mathrm{I_{DS}}$ - NNPSD characteristics show a linear trend as shown by the data in Figure 5.30, which suggests that carrier mobility fluctuations dominate the noise spectra. Whereas, during strong inversion and increased current levels the dependency exhibits a different trend. This suggests that during weak inversion the noise characteristics are dominated by carrier mobility fluctuations as a consequence or charge trapping at the interface due to Coulomb scattering as discussed in section 5.5, which can be described by the McWhorter model [216]. During strong inversion the noise characteristics reduce significantly due to the reduction in the effect of Coulomb scattering. The trends are also consistent with those reported by Rumyantsev *et al.* who examined the low frequency noise characteristics of n-channel 4H-SiC with varying annealing treatments in NO [215].

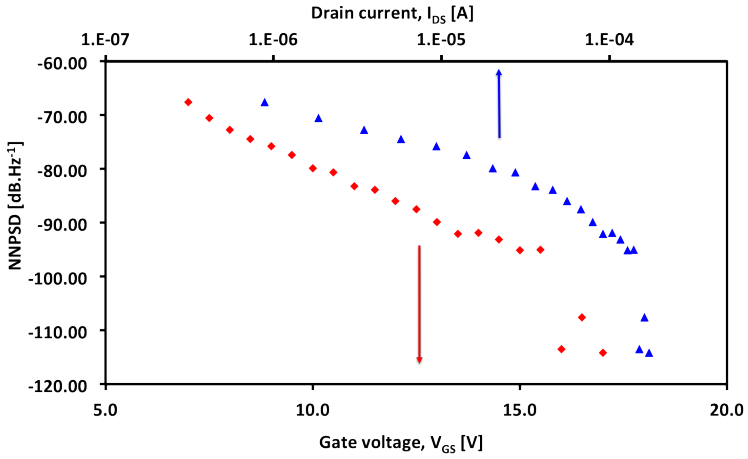

Figure 5.30: NNPSD - V_{GS} and I_{DS} characteristics of a 400×1.5 μm HV06 n-channel MOSFET at 298 K and varying V_{GS}.

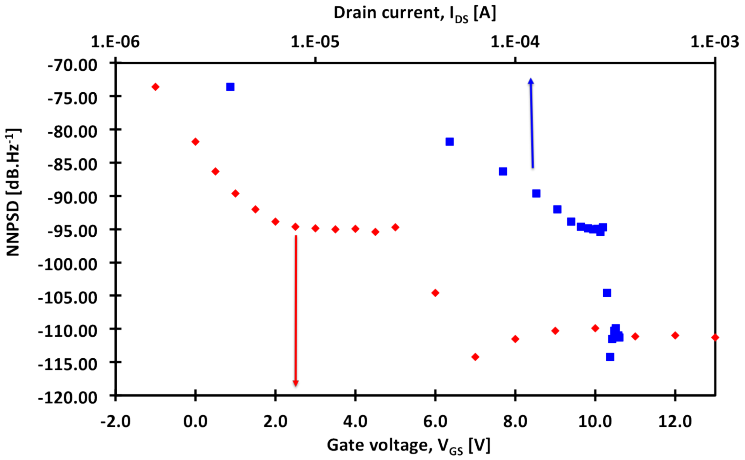

Figure 5.31: NNPSD - V_{GS} and I_{DS} characteristics of a 400×1.5 μm CR25 n-channel MOSFET at 298 K and varying V_{GS}.

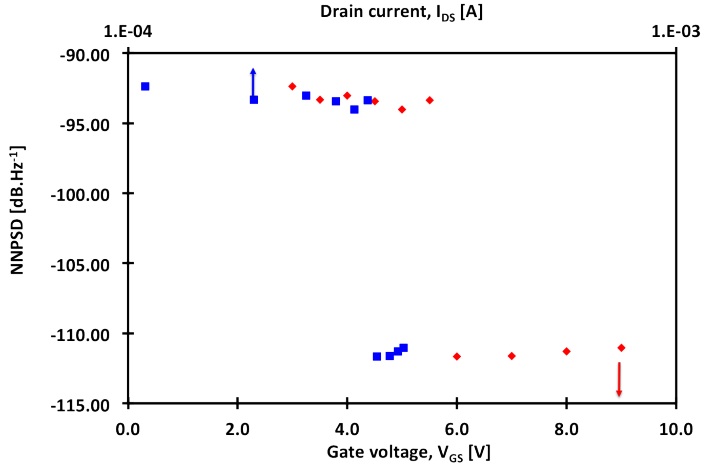

Figure 5.32: NNPSD - V_{GS} and I_{DS} characteristics of a 400×1.5 μm CR27 n-channel MOSFET at 298 K and varying V_{GS}.

CR27 exhibits the lowest noise characteristics of the 3 samples, which suggests that CR27 has the highest quality interface as there is a very low noise contribution from carrier mobility fluctuations at the interface, which suggests that the oxide also has the lowest trap density in the oxide out of the 3 dielectric samples. This is also in agreement with the findings of the CR27 MIS capacitors that were discussed in section 4.6.

The frequency exponent (α) is the value extracted from the fitted line of $\frac{1}{f^{\alpha}}$ and describes how much the trend deviates from $\frac{1}{\mathrm{f}}$. Figure 5.33 shows a plot of the frequency exponent α against gate overdrive ($V_{GS} - V_{\mathrm{TH}}$) for each of the n-channel MOSFETs, HV06, CR25 and CR27, respectively. The frequency exponent (α) was extracted from each of the data sets in Figure 5.30, 5.31 and 5.32 for HV06, CR25 and CR27, respectively. As shown all 3 devices have consistently deviated from the common low frequency noise exponent ($\alpha = 1$) and α values of between 0.5 and 1 have been extracted across the measured voltage range. The frequency exponent deviates from 1 if the trap density is not uniform in depth. As all of the α values are <1 this suggests that the trap density is higher close to the SiO_2/SiC interface and reduces further into the oxide [217].

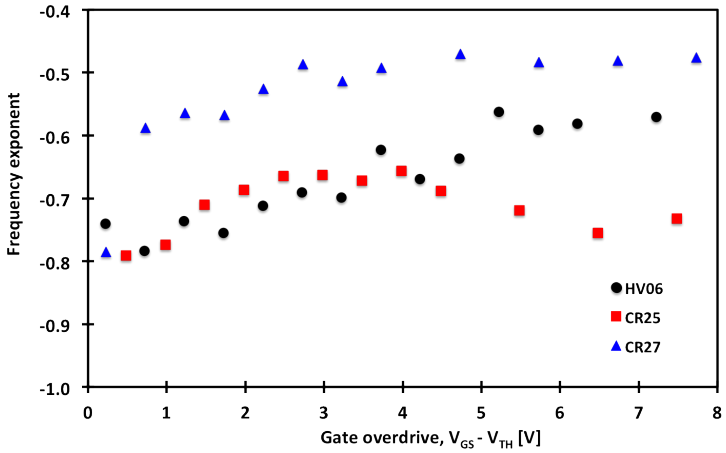

Figure 5.33: Frequency exponent (α) against gate overdrive (V_{GS}-V_{TH}) for the 400×1.5 μm HV06, CR25 and CR27 n-channel MOSFETs measured at 298 K.

The 1/f noise characteristics for each of the dielectrics on the p-channel MOSFETs are shown in Figure 5.34, 5.35 and 5.36 for HV06, CR25 and CR27, respectively, which show a plot of the normalised noise spectrum power density (NNSPD) at 10 Hz against V_{GS} and I_{DS} is shown for each of the devices. Both HV06 and CR25 exhibit a similar characteristic and suggest that 1/f noise is higher at low gate biases (during weak inversion) and reduces

at higher gate biases (at strong inversion) as shown in Figure Figure 5.34 and Figure 5.35. However, the data in Figure 5.36 show that NNSPD increases slightly with increasing bias in CR27, however the noise level is substantially lower than the noise level in both HV06 and CR25 across the measured range.

As with the n-channel devices, CR27 exhibits the lowest noise characteristics of the 3 p-channel samples. This is also in agreement with the findings of the CR27 MIS capacitors that were discussed in section 4.6.

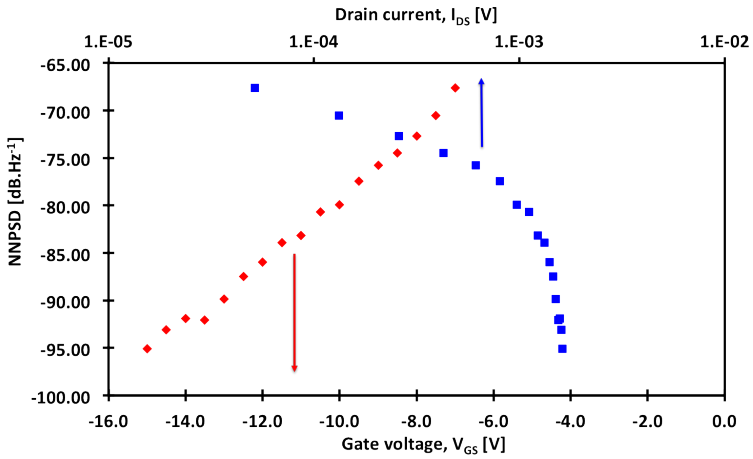

Figure 5.34: NNPSD - V_{GS} and I_{DS} characteristics of a 8000×1.5 μm HV06 p-channel MOSFET at 298 K and varying V_{GS}.

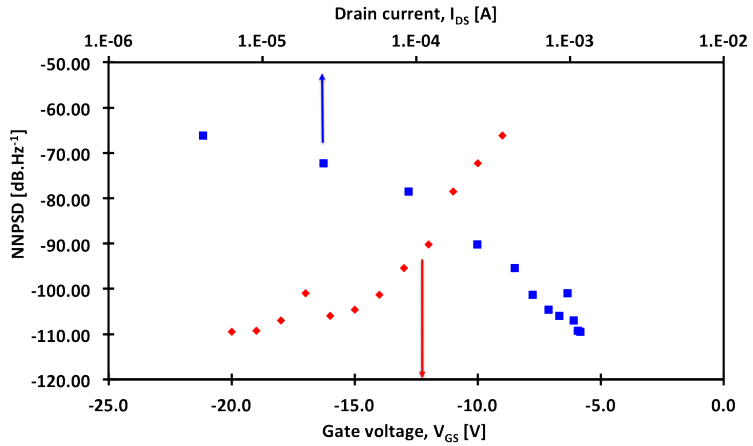

Figure 5.35: NNPSD - V_{GS} and I_{DS} characteristics of a 8000×1.5 μm HV06 p-channel MOSFET at 298 K and varying V_{GS}.

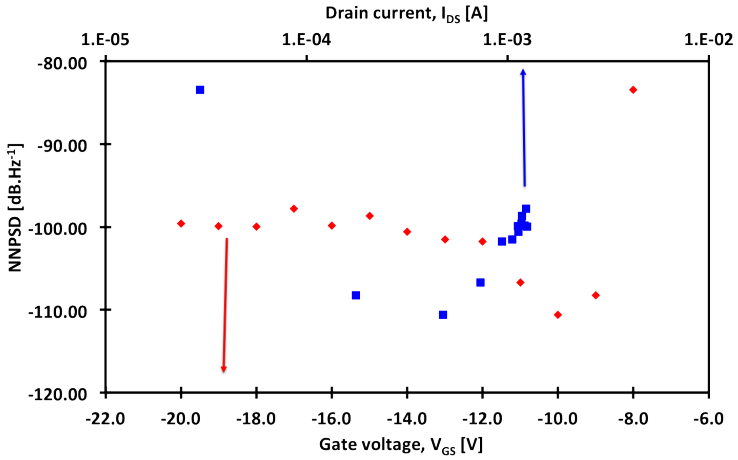

Figure 5.36: NNPSD - V_{GS} and I_{DS} characteristics of a 8000×1.5 μm HV06 p-channel MOSFET at 298 K and varying V_{GS}.

Figure 5.37 shows a plot of the frequency exponent against gate overdrive ($V_{GS} - V_{TH}$) for each of the p-channel MOSFETs, HV06, CR25 and CR27, respectively. The frequency exponent (α) is extracted from the fitted line of $\frac{1}{f^{\alpha}}$ that is applied to each of the extracted data sets in Figure Figure 5.34, Figure 5.35 and **??** for HV06, CR25 and CR27, respectively. As shown all 3 devices have consistently deviated from the common low frequency noise exponent ($\alpha = 1$) and α values of between 1 and 2 have been extracted across the measured voltage range. As all of the α values are >1, which is the opposite to the extracted value from the n-channel devices, this suggests that the trap density is lower at the SiO_2/SiC interface and increases further into the oxide [217][218]. Similar α values were extracted for nitrided gate oxides in SOI MOSFETs [218]. This variation between the α values for the n and p-channel devices could demonstrate information about the carrier-trap interaction and suggests that the electron interact with traps in the oxide close to the interface, whereas, holes interact with traps at deeper energy levels within the oxide.

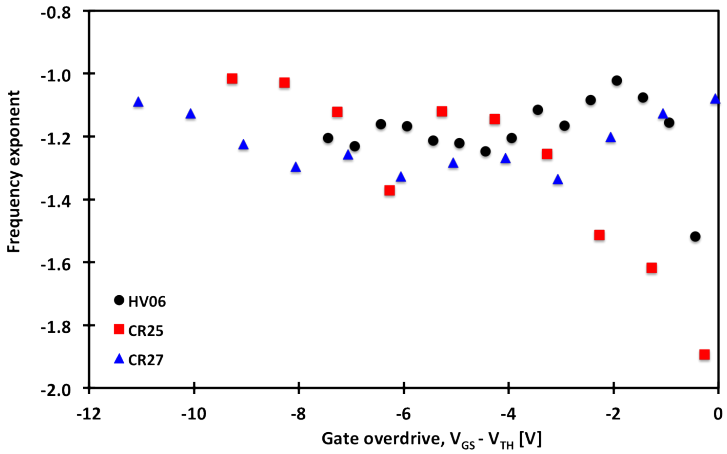

Figure 5.37: Frequency exponent (α) against gate overdrive (V_{GS}-V_{TH}) for the 8000×1.5 μm HV06, CR25 and CR27 p-channel MOSFETs measured at 298 K.

5.7 Impact of V_{TH} adjust implant on the MOSFET operation

In MOSFET technology a common method used to improve device performance through modifying the doping profile is ion implantation. In this investigation ion implantation was used to modify the MOSFET threshold voltage by controlling the doping profile near the semiconductor-dielectric interface.

As described in section 4.8, threshold voltage adjust implants were applied to the MOSFET channels to reduce the threshold voltage of the devices. In order to investigate the effect of the implantation on the n-channel MOSFET characteristics, 3 samples with the same gate dielectric treatment (sample CR27 as described in Table 4.1) but with varying threshold adjust implants referred to as NVT0, NVT1 and NVT2 were examined. An overview of the process steps for each of the implants is given in section 4.8, however, it is important to note that the basic premise is that NVT0, NVT1, and NVT2 represent increasing doses of nitrogen at the surface of the p-well.

A reduction in threshold voltage can be achieved using a low-high doping profile in the device channel, which is also known as a retrograde profile. Ion implantation is used to modify the implantation profile at the surface, which is then subtracted from the background doping, N_B to give ΔN. This has the same effect as changing the semiconductor-metal work-function (ϕ_{MS}) difference or changing the fixed oxide charge (Q_f) as it changes the bias point at which the channel becomes inverted by modifying the depletion layer charge, which is reflected in the third term of Equation 5.13 and becomes Equation 5.15.

The threshold voltage shift due to ion implantation can be derived using a simplified step profile as shown schematically in Figure 5.38 with a step depth of x_s, which is roughly equal

to the sum of the projected implant range and the standard deviation of the implant. If the maximum depletion width (W_{Dm}) is greater than x_s the threshold voltage can be calculated using Equation 5.15.

$$V_{TH} = V_{FB} + 2\phi_B + \frac{qN_B W_{Dm} - q\Delta N x_s}{C_i} \tag{5.15}$$

The maximum depletion width can be calculated using Equation 5.16.

$$W_{Dm} = \sqrt{\frac{2\varepsilon_s \varepsilon_0}{qN_B}\left(2\phi_B + \frac{q\Delta N x_s^2}{2\varepsilon_s \varepsilon_0}\right)} \tag{5.16}$$

V_{TH} is therefore decreased and W_{Dm} is increased by the added doping at the semiconductor surface. For the case of a dose localised at the semiconductor-dielectric interface (x_s=0) with a delta function, Equation 5.15 can be simplified to Equation 5.17 where D_i is the total dose ($\Delta N x_s$).

$$\Delta V_{TH} = \frac{qD_i}{C_i} \tag{5.17}$$

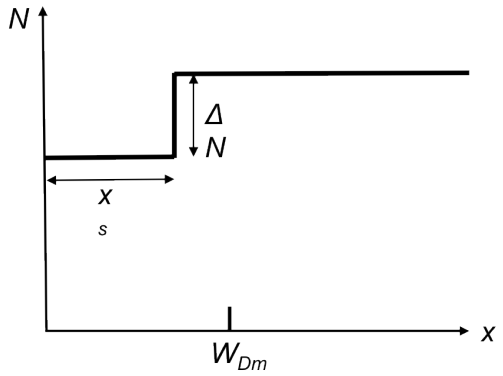

Figure 5.38: Step approximation of the channel doping profile after a threshold voltage adjust ion implantation process to reduce the doping concentration at the semiconductor surface.

The threshold voltage was extracted from the V_{GS}-I_{DS} characteristics from each of the samples using the linear extrapolation method, which consists of finding the V_{GS} axis intercept of the linear extrapolation of the V_{GS}-I_{DS} curve at its maximum first derivative point (i.e. the point of maximum transconductance) and then adding V_{DS}/2 to the extracted value to gain the threshold voltage [168]. The data in Figure 5.39, 5.40 and 5.41 show the $V_{GS} - I_{DS}$ characteristics from 298 K to 498 K for NVT0, NVT1 and NVT2, respectively. The drain bias in each of the measurements was 500 mV. The extracted V_{TH} is plotted against temperature for each of the devices as shown in Figure 5.42 and the room temperature V_{TH} was extracted

as 4.61 V, 3.60 V and 2.57 V for NVT0, NVT1 and NVT2, respectively. This shows that the change in V_{TH} (ΔV_{TH}) is 1.01 V between NVT0 and NVT1 and 1.03 V between NVT1 and NVT2. In this investigation, NVT0 received a 1.7×10^{12} cm^{-2} dose of nitrogen, NVT1 received a 2.35×10^{12} cm^{-2} dose of nitrogen and NVT2 received a 3.00×10^{12} cm^{-2} dose of nitrogen. If it is assumed that all of the implanted nitrogen is ionised at 298 K and x_s is assumed to be 0, then ΔV_{TH} can be calculated using Equation 5.17. This would predict a ΔV_{TH} of 1.34 V would be expected between NVT0 and NVT1 and NVT1 and NVT2. This suggests that at room temperature the implant is only partially ionised and the effective implant dose is smaller than the implanted dose. At increased temperatures ΔV_{TH} between the 3 samples reduces further as shown in Figure 5.42, which suggests that the degree of ionisation also varies across the temperature range. However, the change in V_{TH} with temperature is also affected by charges in the oxide, the reduction in n_i and E_g and therefore, a reduction in the band bending required to reach inversion and the carrier concentration in the bulk of the material, therefore, the observed change with temperature may not be solely due to the threshold adjust implant [1]. It has also previously been reported that counter doping in the channel can occur due to the post-deposition anneals that are implemented on the dielectric, which can act to alter the device threshold voltage[207]. This would also suggest that the dielectric growth, deposition and anneal conditions can act to counter dope the channel region. In this context, counter doping is when P atoms not only act as pasivating species for the SiO_2/SiC interfacial defects but are also incorporated in the SiC substrate, where a fraction of them can increase the MOSFET channel conductivity by the introduction of shallow donors. It has previously been reported that n-type donors (P) are incorporated in a very thin layer (2-3 nm) at the SiC interface [207]. The deposition of the phosphosilicate glass in the CR27 samples could have resulted in a similar phenomenon in the 3 devices under investigation in this section.

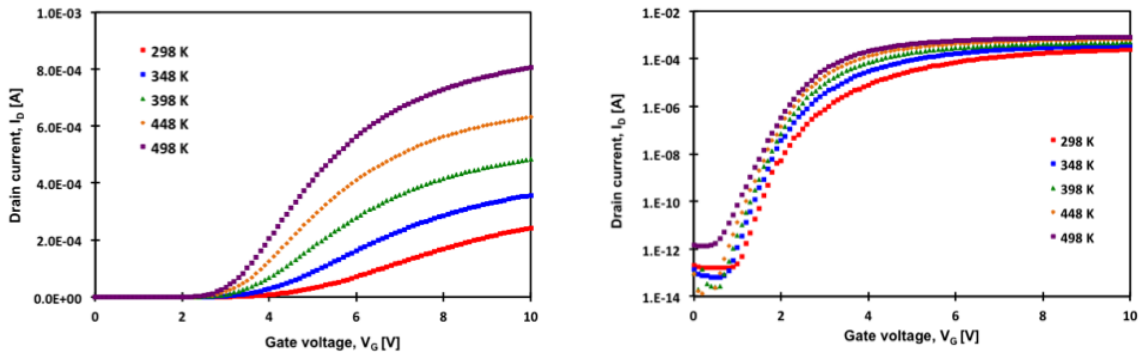

Figure 5.39: V_G-I_D characteristics of a 2000×1.5 μm CR27 n-channel MOSFET from 298 K to 498 K with NVT0 threshold voltage adjust implant.

The data in Figure 5.44, 5.45 and 5.46 show the E -μ_{FE} and the E-μ_C characteristics from 298 K to 498 K for each of the samples NVT0, NVT1 and NVT2, respectively. The value for μ_{FE} was extracted from the $V_{GS} - I_{DS}$ characteristics in Figure 5.39, 5.40 and 5.41

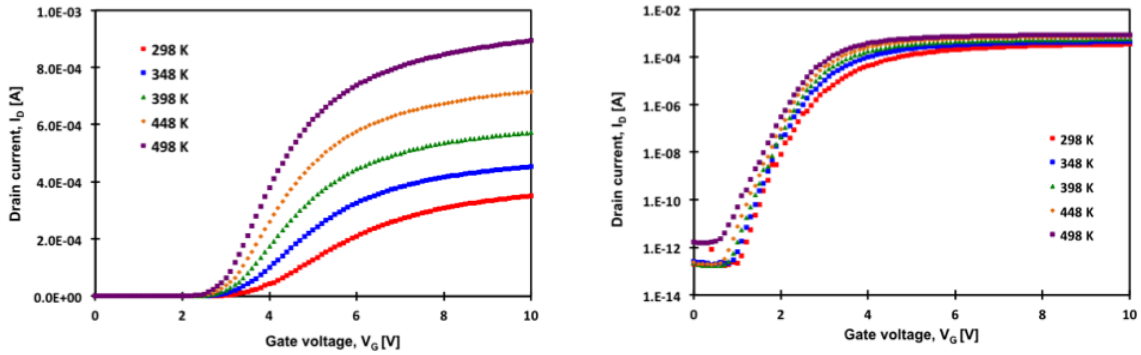

Figure 5.40: V_G-I_D characteristics of a 2000×1.5 μm CR27 n-channel MOSFET from 298 K to 498 K with NVT1 threshold voltage adjust implant.

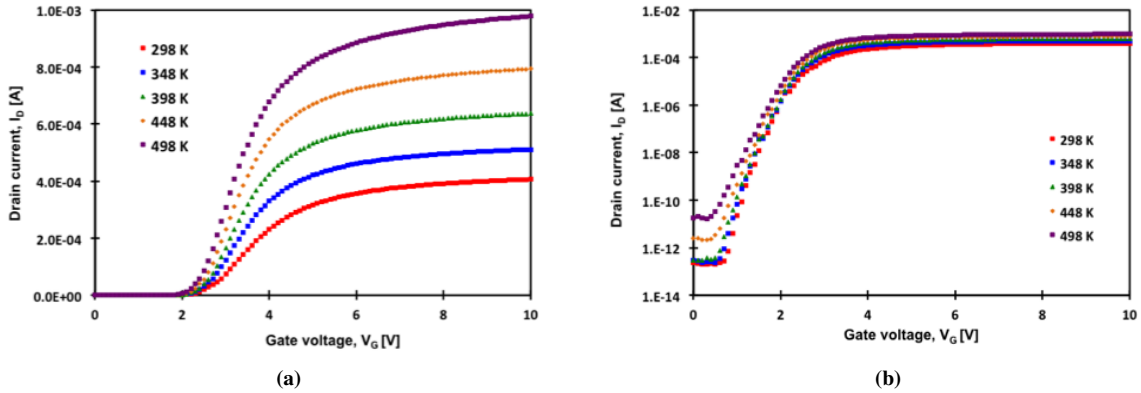

Figure 5.41: V_G-I_D characteristics of a 2000×1.5 μm CR27 n-channel MOSFET from 298 K to 498 K with NVT2 threshold voltage adjust implant.

using Equation 5.2. The theoretical mobility has also been fitted to each of the experimental data sets, as indicated by each of the solid lines in Figure 5.44a, 5.45a and 5.46a using Equation 5.6. As shown, each of the devices show an increase in field effect mobility with an increase in temperature. The NVT2 data shown in Figure 5.46a show the highest field effect mobility across the temperature range out of the 3 samples as supported by the data in Figure 5.47, which show the peak field effect mobility of each device as a function of temperature. Figure 5.44b, 5.45b and 5.46b show the modelled Coulomb scattering mechanism that was fitted to the measured characteristics using Equation 5.11. As shown, the mobility characteristics at low electric fields are dominated by the Coulomb scattering and all of the devices show an increase in mobility with increasing temperature. At high temperatures carriers have higher energy and so scatter less from trapped charges. Due to the lower probability of trap occupation at elevated temperatures, the scattering charge density also reduces, thereby giving higher mobility. This results in a higher current at higher temperatures due to a reduction in the effect of Coulomb scattering. This finding supports previous work carried out in the field [186] [208].

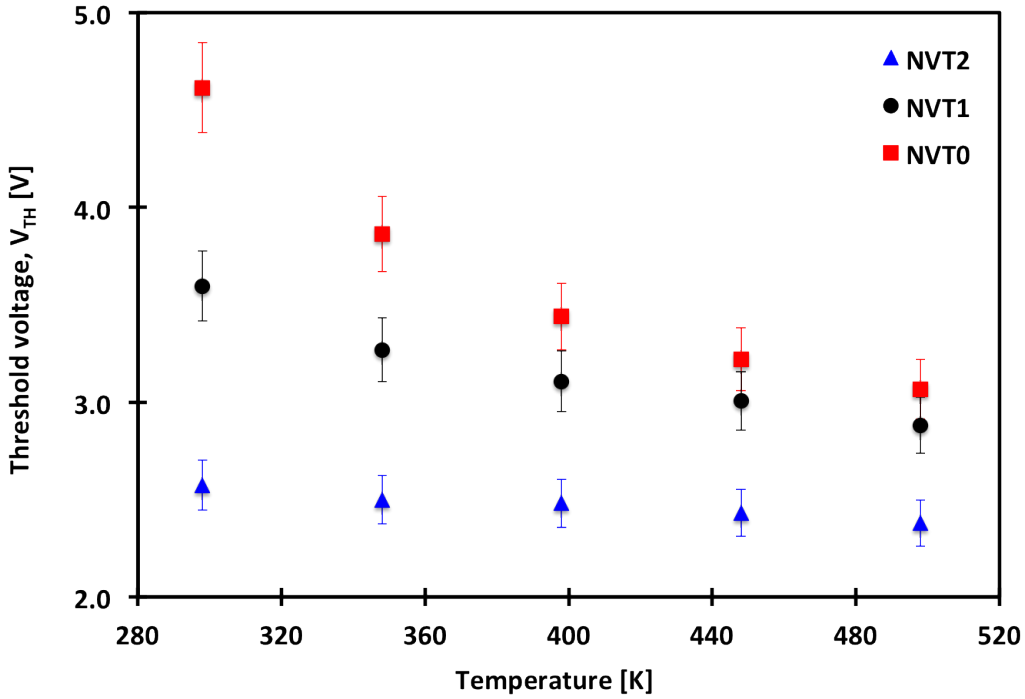

Figure 5.42: Threshold voltage (V_{TH}) against temperature for 2000×1.5 μm CR27 n-channel MOSFETs with NVT0, NVT1 and NVT2 threshold adjust implants.

The other important point to note is that the effects of Coulomb scattering are reduced with an increasing nitrogen implantation dose as shown in Figure 5.44b, 5.45b and 5.46b for NVT0, NVT1 and NVT2, respectively. The Coulomb mobility for NVT2 is significantly higher across the scanned temperature range than the other 2 samples and hence the peak field effect mobility is consistently higher as shown in Figure 5.47. This suggests that the increasing nitrogen implant dose has a beneficial impact on the semiconductor-dielectric interface. However, the interface trap profile across the scanned energy range within Figure 4.39 showed that D_{it} was relatively constant between all 3 samples (NVT0, NVT1 and NVT2), therefore, the increase in Coulomb mobility that is witnessed for the increase in nitrogen implant doses in the MOSFETs suggests that the reduction in Coulomb scattering must be due to the impact of the implant on the other oxide charges such as oxide trapped (Q_{ot}) or fixed oxide (Q_f) charge. The implant dose could also have an impact on the thickness of the transition layer at the dielectric-semiconductor interface as it has previously been demonstrated that there is a strong correlation between the transition layer thickness and the channel mobility in 4H-SiC MOSFETs. A thinner transition layer leads to higher mobility in 4H-SiC MOSFETs [219]. Scanning transmission electron microscopy (STEM) could be used to further investigate this principle in the samples under test in this investigation through providing an image of the transition layer that is present at the interface of each of the devices.

The results gained in Figure 4.39 that showed that there is very little difference in the D_{it} profile of each of the samples is further validated by the fact that there is very little

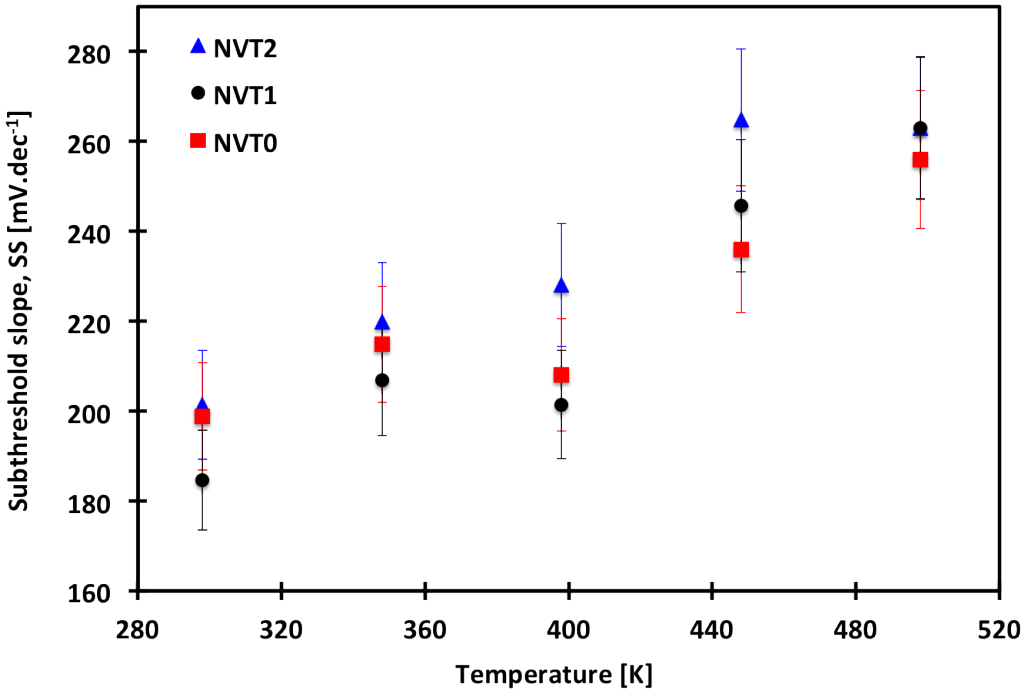

Figure 5.43: Subthreshold slope (SS) against temperature for 2000×1.5 μm CR27 n-channel MOSFETs with NVT0, NVT1 and NVT2 threshold adjust implants.

difference in the shift in subthreshold slope with temperature between each of the samples in Figure 5.43. As subthreshold slope is directly related to D_{it} as shown in Equation 5.14. This confirms that the increase in Coulomb mobility with an increase in nitrogen dose is not due to an decrease in the density of interface states at the SiO_2/4H-SiC interface.

At high electric fields the field effect mobility of each of the samples is severely limited by surface roughness scattering as shown in Figure 5.48. All of samples show a comparable and constant surface roughness scattering mechanism across the entire scanned temperature range as shown in Figure 5.48. This suggests that surface roughness scattering is not temperature dependent in the 4H-SiC n-channel MOSFETs and supports the theoretical investigations that have previously been performed [198] [200]. However, it also highlights that there is a slight variation in surface roughness across the samples that were tested, which suggests that this could be due to the variation in implants doses/treatments for the 3 samples, NVT0, NVT1 and NVT2. This could be further investigated by exploring the physical surface roughness of each of the samples after ion implantation and prior the formation of the gate oxide using atomic force microscopy. The physical topography could then be correlated to the mobility characteristics.

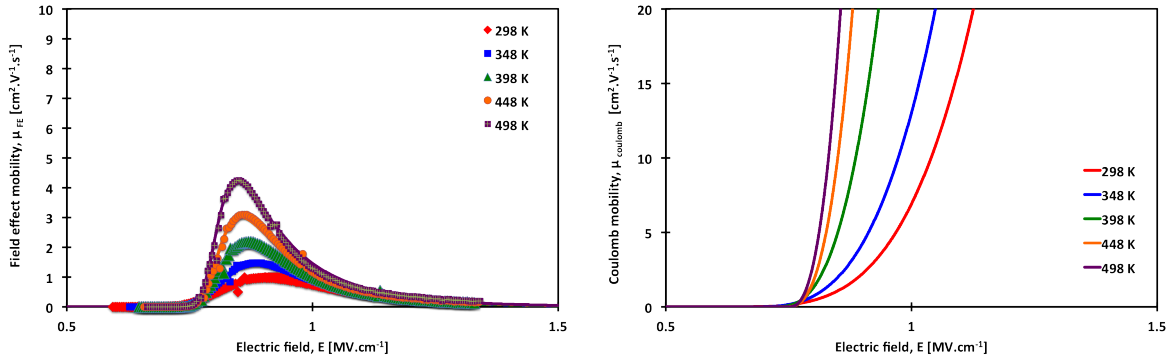

Figure 5.44: (a)μ_{FE}-E and (b) μ_{Coulomb}-E characteristics of a 2000×1.5 μm CR27 n-channel MOSFET from 298 K to 498 K with NVT0 threshold voltage adjust implant.

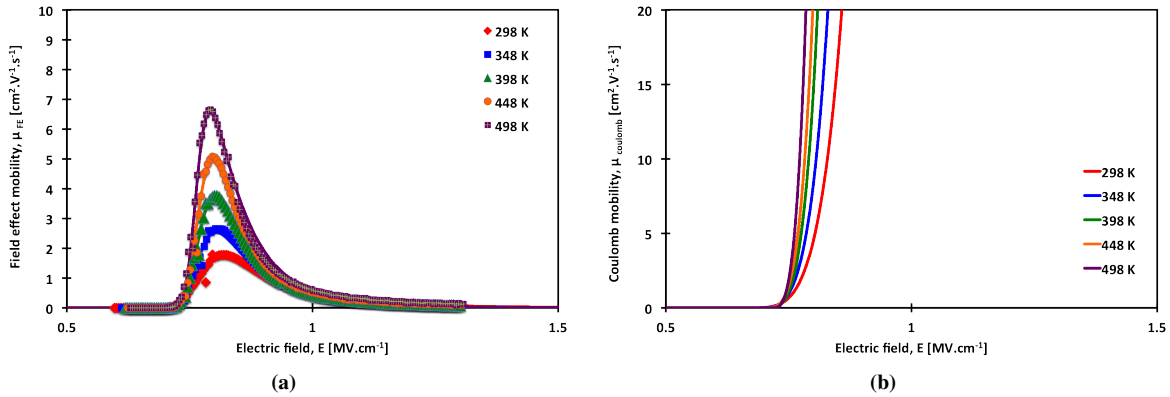

Figure 5.45: (a)μ_{FE}-E and (b) μ_{Coulomb}-E characteristics of a 2000×1.5 μm CR27 n-channel MOSFET from 298 K to 498 K with NVT1 threshold voltage adjust implant.

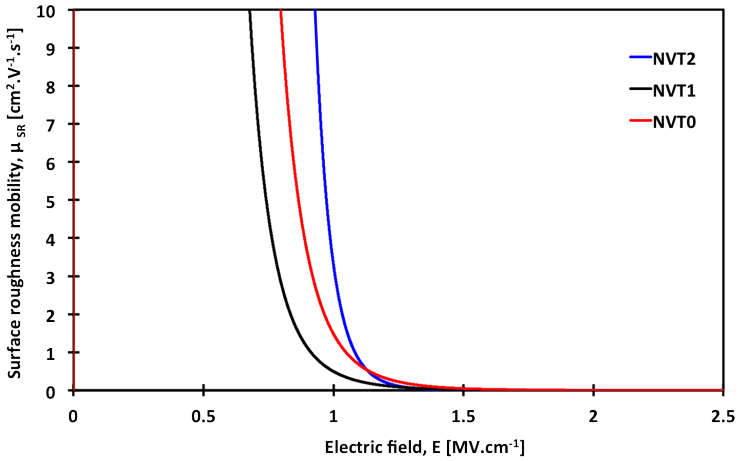

Figure 5.48: Surface roughness scattering (μ_{SR}) against electric field (E) for 2000×1.5 μm CR27 n-channel MOSFETs with NVT0, NVT1 and NVT2 threshold adjust implants.

The findings show that the nitrogen implant within the p-well acts to improve the low

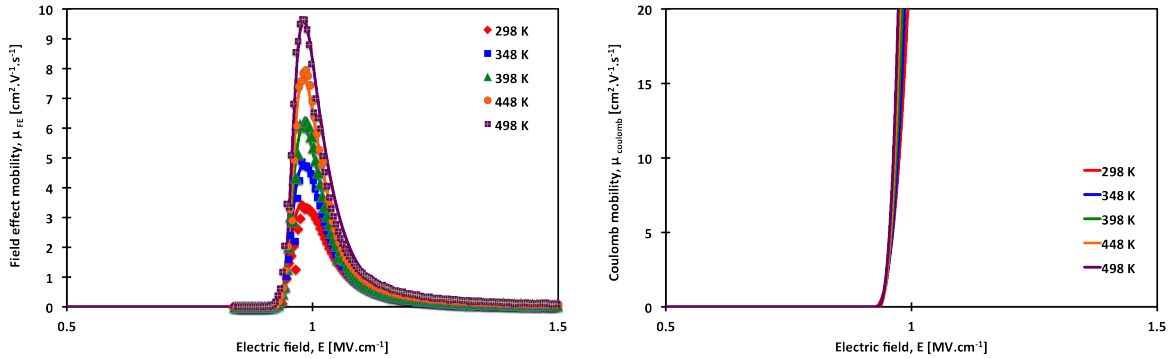

Figure 5.46: (a)μ_{FE}-E and (b) μ_{Coulomb}-E characteristics of a 2000×1.5 μm CR27 n-channel MOSFET from 298 K to 498 K with NVT2 threshold voltage adjust implant.

electric field mobility characteristics of the n-channel 4H-SiC MOSFETs as an increased dose of nitrogen during the implant acts to reduce the effects of Coulomb scattering and, therefore increase Coulomb mobility. The results found in this study also support the results of Moscatelli *et al.* [220]. However, conversely the findings suggest that an increased dose acts to increase the degree of surface roughness scattering in the MOSFET channel, which acts to reduce the overall mobility. For the case of NVT2, which shows the least Coulomb scattering across the temperature range and, therefore, the highest peak field effect mobility, if the surface roughness mobility was increased to a value similar to other reported work, where D1 is quoted to equal 5.82×10^{14} cm.s^{-1} and $\gamma1$ is equal to 2 [200], the devices could potentially show field effect mobility values of over 50 cm^2.V^{-1}.s^{-1} from 1 to 3.5 MV.cm^{-1} and a peak μ_{FE} of 130 cm^2.V^{-1}.s^{-1}. A graphical representation of this is shown in Figure 5.49. Therefore, the main limiting mechanism that should be given attention is that of surface roughness scattering as this currently severely dominates the characteristics from 0.5 MV.cm^{-1} onwards. The behaviour of mobility with temperature could also be related to the Schottky barriers in the metal contacts that were discussed in Chapter 3, therefore, further investigations to establish the contribution of the contact behaviour to the MOSFET mobility behaviour would be very useful to help improve the mobility characteristics.

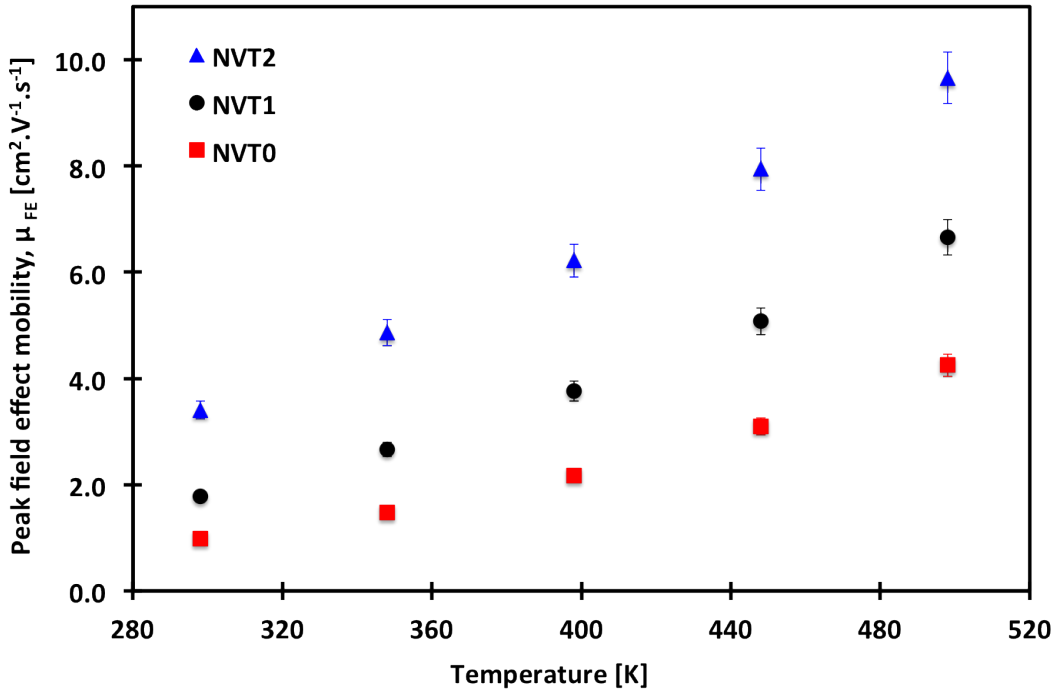

Figure 5.47: Peak field effect mobility (μ_{FE}) against temperature for 2000×1.5 μm CR27 n-channel MOSFETs with NVT0, NVT1 and NVT2 threshold adjust implants.

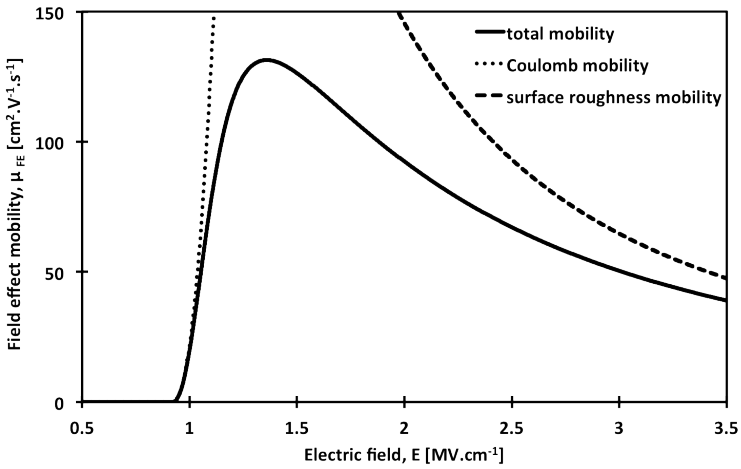

Figure 5.49: Modelled μ_{FE}-E characteristics of a 2000×1.5 μm CR27 n-channel MOSFET at 298 K with an NVT2 threshold voltage adjust implant.

5.8 Summary

The focus of this chapter was on the investigation of the electrical characteristics and device performance parameters of the 4H-SiC n and p-channel MOSFETs that had undergone different dielectric process treatments (sample HV06, CR25 and CR27) to establish which technique provides the most suitable characteristics for a complementary CMOS process.

The investigation into the temperature dependent electrical characteristics of the devices demonstrated that all of the devices showed similar characteristics across the measured temperature range including an increase in I_{DS}, a reduction in V_{TH}, a reduction in D_{it} and, therefore, an increase in μ_{FE} with increasing temperature. This demonstrated as temperature increases there is a reduction of interface trapping effects, and therefore, Coulomb scattering reduces causing the device mobility and current to increase.

The CR27 samples for both n and p-channel MOSFETs exhibit the highest field effect mobility characteristics suggesting that a thin thermally grown oxide provides improved interfacial characteristics. This was further validated by the 1/f noise characteristics of the CR27 MOSFETs, which exhibited the lowest 1/f noise characteristics out of the 3 dielectrics at 298 K.

All 3 dielectrics in both the n and p-channel devices showed severely high mobility limiting surface roughness scattering during strong inversion and high electric fields, which suggests that a process parameter, which is consistent amongst all 3 dielectrics and both the n and p-channel devices is causing high surface roughness in the channel, which is acting to degrade the channel mobility. In order to improve the device characteristics a major focus should be given to increasing the surface roughness mobility of the samples. There is a strong trend across all of the examined samples of extremely low surface roughness mobility from applied electric fields of 1 MV.cm^{-1} onwards, which is consistent across all of the processed samples and much lower than other reported devices. This is also consistent between the n and p-channel devices, which suggests that it is inherent in the process technique used in both devices. This suggests that process contributions that are acting to degrade the surface roughness mobility of the devices is a major factor which is consistent across all of the samples. This suggests that the severely low μ_{SR} is not a contribution of the dielectric processing steps but could be a product of the ion implantation or the post-implantation anneal process. The behaviour of mobility with temperature could also be related to the Schottky barriers in the metal contacts that were discussed in Chapter 3, therefore, further investigations to establish the contribution of the contact behaviour to the MOSFET mobility behaviour would be very useful to help improve the mobility characteristics.

An investigation into the 1/f noise characteristics of each of the MOSFET samples between 1 Hz and 100 kHz showed that in the n-channel MOSFETs the oxide trap density was higher close to the interface, whereas, in the p-channel MOSFETs the trap density was consistently higher further away from the SiO_2-SiC interface consistently across all 3 dielectrics. The investigation also highlighted that in weak inversion the 1/f noise characteristic of all of the devices is dominated by mobility fluctuations due to charge trapping at the interface as a consequence of Coulomb scattering, which can be described by the McWhorter low frequency noise model [216].

Finally, an investigation into the impact of the threshold voltage adjust ion implantation procedure on the device characteristics was investigated for the CR27 n-channel MOSFETs. The findings showed that the increasing nitrogen dose was successful in acting to reduce the device threshold voltage, however, the nitrogen implant within the p-well also acts to improve the low electric field mobility characteristics of the n-channel 4H-SiC MOSFETs as an increased dose of nitrogen during the implant acts to reduce the effects of Coulomb scattering and, therefore increase Coulomb mobility.

Chapter 6

Conclusions and future work

6.1 Summary

The main objective of this study was to gain an in depth understanding of the impact of process variations in both 4H-SiC Ohmic contacts and dielectrics that are employed in 4H-SiC CMOS devices in order to facilitate performance and stability improvements in devices such as the MOSFET used in integrated circuits.

As presented in chapter 2 there are a number of key issues and challenges in the technology including oxide growth and Ohmic contact formation as well as device operating concerns such as oxide reliability, reduced channel mobility and threshold voltage instability and one of the aims of this thesis was to understand the performance of the 4H-SiC MIS samples in the investigation in order to inform process improvement steps to overcome some of the issues.

Chapter 3 involved a study into the performance of the Ohmic contacts that have been employed on both the n and p-type 4H-SiC structures that are analysed throughout this thesis. This investigation involved both electrical and physical characterisation across a large temperature range of the contacts including current-voltage measurements on two-terminal resistor structures, four-terminal cross-bridge Kelvin resistor structures and four-terminal van der Pauw structures as well as atomic force microscopy (AFM) in order to extract the resistance, specific contact resistance, sheet resistance and surface morphology of the contact metallisation samples. The results showed that both contacts performed reliably up to 650 K with ρ_c values of $10^{-3}\,\Omega.\text{cm}^2$ which are comparable to other Ni based contacts reported in the literature. A key issue, however, is that the n-type contact showed rectifying behaviour across the measured temperature range, which could be a product of the fabrication procedure, which acts to modify the chemical structure or composition of the structure. Further investigation is required to fully validate this hypothesis.

The impact of dielectric formation and processing on the operation of both 4H-SiC MIS structures and MOSFETs was then investigated for 3 dielectrics with varying process condi-

tions (HV06, CR25 and CR27) on both n and p-type 4H-SiC in chapter 4 and 5. This included measurement of the electrical characteristics between 298 K and 448 K.

The 3 dielectrics exhibited very similar properties on both n and p-type 4H-SiC. However, several issues with the CR25 MIS capacitor samples were observed including the highest mobile and oxide trapped charges out of the 3 dielectrics on both n and p-type, a very large variation of interface trap density with temperature and both showed an increase in D_{it} at the conduction and valence band edge, respectively with increasing temperature, there was a large variation in the conduction mechanisms which were observed for n and p-type CR25 MIS samples dielectric. The n-type sample exhibited a trap assisted tunnelling conduction mechanism, whereas, the equivalent p-type sample demonstrated an extremely low leakage current and showed no electric field or temperature dependence. All of the above points demonstrate that the CR25 dielectric processing technique produces the lowest quality dielectric out of the 3 methods investigated, which could also be a product of the deposited oxide and the removal of the original thermally grown SiO_2 layer.

HV06 has a very low equivalent oxide thickness in both the n-type and p-type sample, which could be due to a modification of the relative permittivity of the dielectric (ε_r) or due to a reduction in the physical oxide thickness due to the post oxidation anneal treatments that were carried out on this sample as described in Table 4.1.

The investigation into the temperature dependent electrical characteristics of the MOSFET devices demonstrated that all of the devices showed similar characteristics across the measured temperature range including an increase in I_{DS}, a reduction in V_{TH}, a reduction in D_{it} and, therefore, an increase in μ_{FE} with increasing temperature. This demonstrated that as temperature increases there is a reduction of interface trapping effects, and therefore, Coulomb scattering reduces causing the device mobility and current to increase.

The investigation into the impact of the threshold voltage adjust implantation on the MIS capacitor characteristics identified that a decrease in N_A with temperature was witnessed for all of the samples, NVT0, NVT1 and NVT2. This could be due to an increase ionisation of the implanted nitrogen dopants with temperature. It was observed that a higher implant dose leads to a a large shift in V_{FB}, therefore, suggesting the nitrogen implant acts to modify the oxide charge of each of the samples (Q_m+Q_F+Q_{ot}). However, the variation in implant dose has no impact on D_{it} as all 3 samples showed equal D_{it} for E_{TH}-E_V values of 0.2 to 1.6 eV. The effect of the threshold voltage adjust implantation on the MOSFET characteristics showed that the increasing nitrogen dose was successful in acting to reduce the device threshold voltage, however, the nitrogen implant within the p-well also acts to improve the low electric field mobility characteristics of the n-channel 4H-SiC MOSFETs as an increased dose of nitrogen during the implant acts to reduce the effects of Coulomb scattering and, therefore increase Coulomb mobility.

As a solution for a complementary process for both n-type and p-type 4H-SiC MIS technology the most viable process technique of those examined is CR27. CR27 on both n-type and p-type 4H-SiC showed extremely promising characteristics with acceptable equivalent oxide thicknesses and oxide capacitances that were representative of SiO_2, the sample had the lowest oxide charge for the n-type MIS capacitor and the second lowest oxide charge for the p-type MIS sample. This supports the theory that a thin thermally grown oxide layer at the semiconductor-dielectric interface is beneficial for an enhanced interface and reduced gate leakage in a 4H-SiC MIS structure [195]. All 3 dielectrics showed comparable D_{it} values at room temperature, however, CR27 showed the largest decrease of D_{it} with temperature out of the 3 samples on both n-type and p-type 4H-SiC, which would make it the most suitable dielectric for high temperature applications. The CR27 samples for both n and p-channel MOSFETs exhibit the highest field effect mobility characteristics suggesting that a thin thermally grown oxide provides improved interfacial characteristics. This was further validated by the 1/f noise characteristics of the CR27 MOSFETs, which exhibited the lowest 1/f noise characteristics out of the 3 dielectrics at 298 K.

All 3 dielectrics in both the n and p-channel MOSFET devices showed severely high mobility limiting surface roughness scattering during strong inversion and high electric fields, which suggests that a process parameter, which is consistent amongst all 3 dielectrics and both the n and p-channel devices is causing high surface roughness in the channel, which is acting to degrade the channel mobility. In order to improve the device characteristics a major focus should be given to increasing the surface roughness mobility of the samples. There is a strong trend across all of the examined samples of extremely low surface roughness mobility from applied electric fields of 1 $MV.cm^{-1}$ onwards, which is consistent across all of the processed samples and much lower than other reported devices. This is also consistent between the n and p-channel devices, which suggests that it is inherent in the process technique used in both devices. This suggests that process contributions that are acting to degrade the surface roughness mobility of the devices is a major factor which is consistent across all of the samples. This suggests that the severely low μ_{SR} is not a contribution of the dielectric processing steps but could be a product of the ion implantation or the post-implantation anneal process.

An investigation into the 1/f noise characteristics of each of the MOSFET samples between 1 Hz and 100 kHz showed that in the n-channel MOSFETs the oxide trap density was higher closer to the interface, whereas, in the p-channel MOSFETs the trap density was consistently higher further away from the SiO_2-SiC interface consistently across all 3 dielectrics. The investigation also highlighted that in weak inversion the 1/f noise characteristic of all of the devices is dominated by mobility fluctuation due to charge trapping at the interface due to Coulomb scattering, which can be described by the McWhorter low frequency noise model [216].

6.2 Future work

The future work, which can build upon the findings of this thesis, is made up of 2 main components. Firstly a monolithic Ohmic contact process for both n and p-type 4H-SiC could be investigated. This could involve investigations into the cause of the rectifying behaviour of the n-type contact, ways in which the specific contact resistance can be improved and also an investigation into the impact of the ion implantation doping procedure and post implantation anneal on the contact characteristics. An investigation into the long term stability of the contacts whilst operating at elevated temperatures in air is also required in order to validate as to whether the metallisation provide a viable solution for long term high temperature applications.

Secondly, further investigation is required to improve the device performance of the MIS system for CMOS applications. This would involve examination of the surface roughness scattering mechanism that is severely limiting the MOSFET device performance of all of the examined dielectrics. It would also be extremely beneficial to explore the use of a thin thermal oxide layer followed by varying deposited oxides in different annealing conditions to optimise the device performance and potentially provide a MIS solution for long term high temperature applications.

There is also a significant opportunity for further investigation of the 1/f noise characteristics of the devices. The temperature dependence of the 1/f noise characteristics could be investigated to further validate the findings that interfacial charge trapping decreases with increasing temperature and the technique could also be used to investigate the variation in threshold voltage with temperature.

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