Newcastle University
School of Electrical and Electronic Engineering

Design, Analysis and Implementation of Voltage Sensor for Power-Constrained Systems

By

Reza Ramezani

A thesis submitted for the degree of

Doctor of Philosophy

January 2014

Abstract

Thanks to an extensive effort by the global research community, the electronic technology has significantly matured over the last decade. This technology has enabled certain operations which humans could not otherwise easily perform. For instance, electronic systems can be used to perform sensing, monitoring and even control operations in environments such as outer space, underground, under the sea or even inside the human body. The main difficulty for electronics operating in these environments is access to a reliable and permanent source of energy. Using batteries as the immediate solution for this problem has helped to provide energy for limited periods of time; however, regular maintenance and replacement are required. Consequently, battery solutions fail wherever replacing them is not possible or operation for long periods is needed. For such cases, researchers have proposed harvesting ambient energy and converting it into an electrical form. An important issue with energy harvesters is that their operation and output power depend critically on the amount of energy they receive and because ambient energy often tends to be sporadic in nature, energy harvesters cannot produce stable or fixed levels of power all of the time. Therefore, electronic devices powered in this way must be capable of adapting their operation to the energy status of the harvester. To achieve this, information on the energy available for use is needed. This can be provided by a sensor capable of measuring voltage. However, stable and fixed voltage and time references are a prerequisite of most traditional voltage measurement devices, but these generally do not exist in energy harvesting environments. A further challenge is that such a sensor also needs to be powered by the energy harvester's unstable voltage. In this thesis, the design of a reference-free voltage sensor, which can operate with a varying voltage source, is provided based on the capture of a portion of the total energy which is directly related to

the energy being sensed. This energy is then used to power a computation which quantifies captured energy over time, with the information directly generated as digital code. The sensor was fabricated in the 180 nm technology node and successfully tested by performing voltage measurements over the range 1.8 V to 0.8 V.

Acknowledgments

I would like to express the deepest appreciation to my supervisor Prof. Alex Yakovlev, who has the attitude and the substance of a genius: he continually and convincingly conveyed a spirit of adventure in regard to research. Without his guidance and persistent help this thesis would not have been possible.

I am also grateful to Dr. Fei Xia and Dr. Delong Shang for their fruitful discussions on various related topics. I would like to thank my friends and colleagues, Dr. Mohammed Alamin, Dr. Reza Rafiee, Dr. Maxim Rykunov, Dr. Ra'ed Al-Dujaily and Dr. Danil Sokolov for their inspiring discussions.

I would also like to thank my fiancé, Golnaz whose remarkable support helped me significantly throughout this research. The last but not the least; I would like to thank my parents; Ali Ramezani and Hamideh Baimani, my nanny Kefaiat, my sisters Leila and Sanaz and my brother Borzo, for supporting me spiritually throughout my life.

This work was supported by the Engineering and Physical Sciences Research Council (EPSRC) under Grant No. EP/G066728/1, "Next Generation Energy-Harvesting Electronics: Holistic Approach,".

Contents

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List of Abbreviations

Ack	Acknowledgement
ADC	Analog to digital converter
big-D	Big digital
CMC	Current mode control
CMOS	Complementary metal–oxide–semiconductor
DAC	Digital to analogue converter
DC	Direct current
DFS	Dynamic frequency scaling
DRC	Design rule checking
DVFS	Dynamic voltage frequency scaling
DVS	Dynamic voltage scaling
EDA	Electronic design automation
FET	Field effect transistor
FF	Fast-fast
FFT	Fast fourier transform
gds	Graphic database system
Hex	Hexadecimal
LC	Inductor-capacitor
LDO	Low-dropout
lef	Library exchange format
LSB	Least significant bit
LVS	Layout versus schematic
MEMS	Microelectromechanical systems
MEP	Minimum energy point
MPPT	Maximum power point tracking
MS	Mode selector
MSB	Most significant bit
NAND	Negated AND
NMOS	N-channel metal-oxide semiconductor
NT	Number of transitions
ODE	Ordinary differential equation
P&R	Place and route
PFM	Pulse frequency modulation

PMOS	P-channel metal-oxide semiconductor
PMU	Power management unit
POR	Power-on reset
PWM	Pulse width modulation
QoS	Quality of service
RC	Resistor–capacitor
Req	Request
RFID	Radio-frequency identification
RTL	Register transfer language
SAR	Successive approximation register
small-A	Small analogue
SS	Slow-slow
STG	Signal transition graph
TG	Transmission gate
UMC	United microelectronics corporation
VCO	Voltage controlled oscillator
VTC	Voltage to time converter
ZCS	Zero current switching
ZVS	Zero voltage switching

List of symbols

C	Capacitor
d_i	Deadline to execute the task
E_c	Energy available
e_i	Energy consumption of the task
E_s	Energy scavenged
GNC	Ground
Gsps	Giga sample per second
Hz	Hertz
I_c	Collector current
I_s	Reverse saturation current
I_t	Technology-dependent scaling parameter
K	Coefficient of decaying voltage at each switching action
K_b	Boltzmann constant
L	Transistor length
l_{eff}	Effective channel length
m	Sub-threshold slope factor
mA	Milliampere
MHz	Megahertz
mJ	Millijoules
mm	Millimetre
mV	Millivolts
n	Switching Index
nF	Nanofarads
nm	Nanometer
pF	Picofarads
P_{max}	Maximum power
q	Electrical charge
R	Resistor
s_i	The time which each task should start being executed
t	Time
t_p	Propagation delay of an inverter
uH	Microhenry
uW	Microwatt

V_{BE}	Base-emitter voltage
V_{dd}	Power supply
V_{ds}	Drain-source voltage
V_{gs}	Gate-source voltage
V_T	Thermal voltage
V_{th}	Threshold voltage
W	Transistor width
α	Activity factor
β	Gain factor
γ	Velocity saturation index
μeff	Effective mobility
Ω	Ohm

List of publications

Patent

1. A. Yakovlev, R. Ramezani, and T. Mak, "APPARATUS AND METHOD FOR VOLTAGE SENSING," UK Patent Application no.1 005 372.6 Newcastle University, March 2010.

Journal publication

1. R. Ramezani, A. Yakovlev, F. Xia, J. Murphy and D. Shang, Voltage Sensing Using an Asynchronous Charge-to-Digital Converter for Energy-Autonomous Environments, IEEE Journal of Emerging and Selected Topics in Circuits and Systems (JETCAS), vol.3, No. 1, pp. 35-44, 2013.

Conference publications

1. R. Ramezani, D. Sokolov, F. Xia, and A. Yakovlev, "Energy-modulated quality of service: New scheduling approach," in *Faible Tension Faible Consommation (FTFC), IEEE*, 2012, pp. 1-4.
2. R. Ramezani and A. Yakovlev, "Capacitor Discharging Through Asynchronous Circuit Switching," in *Asynchronous Circuits and Systems (ASYNC), 2013 IEEE 19th International Symposium on*, pp. 16-22.
3. R. Ramezani and A. Yakovlev, "Reference Free Voltage Sensing Using an Asynchronous Charge-to-Digital Converter" IDTechEx Energy Harvesting Europe, 15-16 May 2012, Berlin, Germany.

Technical reports

1. R. Ramezani, A. Yakovlev, T. Mak, and D. Shang, "Voltage sensing using an asynchronous charge-to-digital converter for energy harvesting circuits," *NCL-EECE-MSD-TR-2010-161, Microelectronic System Design Group, School of EECE, Newcastle University*, December 2010.
2. D. Shang, R. Ramezani, F. Xia, A. Yakovlev, "Wide-Range, Reference-Free, On-Chip Voltage Sensor for Variable Vdd Operations", *NCL-EECE-MSD-TR-2010-159, Microelectronic System Design Group, School of EECE, Newcastle University*, October 2010.

Chapter 1. Introduction

1.1 Motivation

Continuous growth in demand for portable electronic devices has led to a great deal of attention being paid to circuit power consumption. Traditionally, portable electronics system are designed as battery-powered devices with efficient power control techniques applied to prolong battery life. Power or clock gating, dynamic voltage scaling (DVS) [1] and dynamic frequency scaling (DFS) [2] are the most conventional examples of techniques used to achieve maximum energy savings. While battery-operated devices are extremely common and incredibly popular, there are classes of applications where dependence on a battery is impractical. In such applications, when a continuous source of energy is required, replacing the battery may be either costly or highly inconvenient. For example, battery replacement in implanted medical devices [3-5] is significantly expensive or extremely risky. The limiting factor for these devices is the longevity of the battery sources. Using the current technology, battery powered devices can perform continuous operation between 5 to 10 years. After this time, the device should either be removed or the battery is replaced [6-8]. According to these researches, the patients who were using lithium battery powered pacemakers need reoperation every eight years.

RFID tags [9] and Micro-sensor networks [10-12] are another example of applications where due to the size and the weight of batteries they are rendered impractical. In RFID tags, the mean time for replacing battery, due to the energy density, shelf-life trends and the communication method, is only a year or two [13]. In micro/nano-sensor networks, containing large number of nodes, replacing batteries is next to impossible [14]. For these sensors the needed power is in the range of milli or even microwatt. However, the output power for a conventional rechargeable lithium-ion battery is in the range of hundreds of Watt [15].

The most promising alternative to power these applications is to harvest energy from the environment and to convert it into electrical energy. Advances in MEMS processing and materials technology have made it possible to produce electrical energy from mechanical [16], thermal [17, 18], light [19], kinetic [20] and electromagnetic [21] energy sources. These are mostly considered to be sporadic in nature but permanently available. In any system which uses these sources, energy can no longer be freely used if functionality is to be optimised in order to achieve the levels of performance demanded. In fact, the functionality should be tuned to match the energy status rather than being used to tune performance. Put simply, the amount of energy which flows into the system shapes or merely modulates the functionality, and therefore the performance, of the system. This is known as energy-modulated quality of service (QoS) [22].

1.2 Energy-modulated quality of service

In electronic design nowadays, energy-aware systems have attracted huge interest among the designers of systems that have to operate in an energy-deficient environment. Within this environment, despite conventional assumptions which consider that data are the only unknown factor, energy is now an unknown parameter as well. However, the range of variation of energy is smaller, measurable and more predictable. This draws attention to the fact that systems can be equipped with means to measure energy (by simply measuring the voltage). This energy information then can be used to optimize system performance. Regardless of how this is achieved, a system which links energy information to system performance (which I simply call quality of service) can deliver an energy-modulated quality of service [23]. In this context, quality of service is simply the speed and the data precision of the operation (e.g. operation at 1MHz speed and 16-bit data precision delivers higher QoS compared to operation running at 500KHz and 8-bit data precision).

In real system implementation, in order to achieve energy-modulated quality of service, certain algorithms are employed. These algorithms regulate the operation of the system according to the energy information in a scenario of interest. For example, in a very conservative scenario, low-power operation (e.g. the power consumption of a particular operation becomes less than its nominal power consumption) is the main concern. Therefore, the system is always configured to operate at the minimum possible level of performance which is defined according to the energy information. Another interesting scenario is to configure the system for a specific level of performance at all times. In this scenario, the quality of system operation, for instance, the precision of computation is adjusted according to the energy information. As far as system operation is concerned, the most reliable algorithm would be the one which guarantees the survivability of the system. Such an algorithm should be able to arrange and prioritize tasks in a queue in order to produce meaningful results without wasting energy on possibly interminable task. Two slightly different classes of such algorithms are described below.

There are various different online or off-line scheduling algorithms [24-26] which optimize the functionality of a system according to the amount of energy available (E_c), predictions of energy scavenged (E_s), energy consumption of the task (e_i), maximum possible performance (achieved at P_{max}), and a deadline to execute the task (d_i). These algorithms arrange queues of tasks according to the time which each task should start being executed (s_i). To calculate the start time s_i, the above stated information (E_c, E_s, e_i, P_{max} and d_i) is employed.

Another class of algorithms [23] considers tasks as continuous actions. Therefore, any amount of progress towards completing a task can be meaningful and valuable. From this point of view, if the amount of energy available is not sufficient to finish the task,

the load can still use the energy and produce results which are less precise or otherwise deliver a lower quality of service. For instance, after spending insufficient energy, only part of the result is useless. The remainder of the result may be of a somewhat lower quality but is still meaningful and useful. It can be argued that such imprecision in terms of data is tolerable for a system operating in an energy-scarce environment.

Regardless of the mechanisms employed by any of these algorithms, information on the energy available for use is essential. Consequently, a circuit should be designed in order to measure the amount of available energy. The main challenge here is that the circuit is operating in the same environment as the rest of the system, and therefore it measures the energy which is also used as its own power supply. The next challenge is that, in an energy harvesting environment, stable or fixed references such as for voltage or time are not guaranteed. Therefore, a circuit is required which can robustly operate under conditions of energy variation but with no need for any such reference.

1.3 Thesis main aim

The main aim for this research is to design a voltage sensor circuit which can reliably operate in energy harvesting systems. However, stable and fixed voltage references, a prerequisite of most traditional voltage measurement devices [27, 28] generally do not exist in energy harvesting environments [29]. Therefore, the main requirement for this sensor is to operate without the need for any references.

1.4 Contributions of the thesis

In line with the requirements described in the previous sections the main contribution of this thesis is:

- **Reference-free voltage sensing:**

This is based on the idea of capturing a portion of the total energy that is directly related to the voltage being measured or sensed. This energy is then used to power a computation which quantifies over time the energy captured and therefore the voltage sensed.

Following contributions are also been achieved throughout this research:

1) **The relationship between voltage drop and circuit switching:**

   The relationship is explored between the switching behaviour of a self-timed digital circuit and the dynamic characteristic of voltage on the capacitor while the circuit is powered by it.

2) **Sensor circuit design and silicon fabrication:**

   Following up on the specifications considered for this sensor, necessary circuits are carefully designed and tested over the range of voltage from super-threshold region down to subthreshold. The sensor was, then, fabricated on-chip using 180nm UMC technology.

3) **Energy harvesting power platform:**

   The sensor designed in this work can be simply employed to develop a power platform for any energy-aware systems. An example of such system is designed and successfully tested.

1.5 Organisation of the thesis

The remainder of the thesis is organised as follows:

a) **Chapter 2:**

   This chapter creates an in-depth insight into energy harvesting systems, different voltage measurement techniques and various techniques of low-energy circuit design.

b) **Chapter 3:**

The importance of the relationship between the switching behaviour of the self-timed counter and the dynamic characteristics of the voltage on the capacitor was explained before. This chapter contains research on exploring a closed-form expression of relationship between capacitor discharging and digital circuit switching. In this chapter a self-timed counter is also designed which will be used as the computational unit of the sensor.

c) **Chapter 4:**

This chapter describes the circuit details of an autonomous reference-free voltage sensor designed according to the principles of proposed charge-to-digital sensing method. The sensor, fabricated in the 180nm technology node, was tested successfully through performing measurements over the voltage range from 1.8V down to 0.8V.

d) **Chapter 5:**

The main aim for this chapter is to employ my designed sensor in an energy harvesting system. Using this sensor, a power platform designed in two main parts. The first part supplies less regulated voltage to the load with the assumption that the load is capable of working robustly under the voltage variation. The load is capable of modulating its functionality according to the energy information captured by the sensor. The second part of the power platform provides fixed and tuneable voltage for those parts of the load which require stable and controllable voltage for short period of times.

e) **Chapter 6:**

This chapter summarizes the results achieved in this research. It also discusses the main areas for future works based on the results of this study.

Chapter 2. Background

In this chapter, background information is provided on energy harvesting systems, voltage measurement and techniques for low-energy circuit design. The development of energy harvesting systems has started to attract the attention of industry, and several well-known companies have formed teams of experts to develop electronic solutions for problems in energy harvesting systems. One prominent example is the power platform, MAX17710, designed by the Maxim Company, which is described at the end of this chapter.

2.1 Energy harvesting system design

Figure 2-1 depicts a general overview of an energy harvesting system. In this system, the harvester extracts energy from a source of energy in the environment and converts it into electrical form.

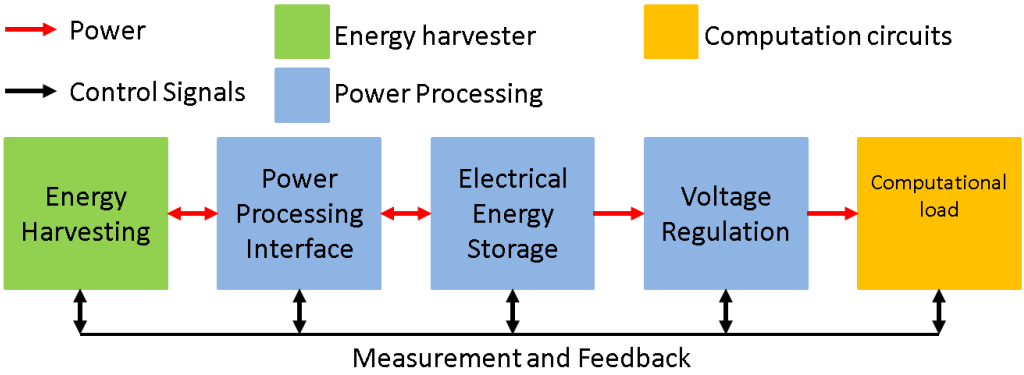


Figure 2-1 General block diagram of energy harvesting system [30].

The first stage, which is called the power processing interface, ensures that the efficiency of the harvester in terms of both harvesting and generating energy is maximized. For this purpose, techniques such as transducer frequency tuning, adaptive damping and maximum power point tracking (MPPT) are employed.

Part of the power processing is dedicated to solving the problem of the intermittent nature of the energy generating at the harvester and the energy consumption at the load. For that, once the energy accumulated in storage in a super-capacitor or a battery reaches sufficient level, the load can be triggered to start functioning.

The final stage of power processing is the voltage regulator. In this stage, the voltage on the storage component is converted into the voltage required by the load. Employing an appropriate tuneable voltage regulator is crucial to implementing techniques such as dynamic voltage scaling (DVS) and power gating. The main requirement in implementing these techniques is that the load has to have the intelligence to define a strategy by which the voltage regulator can be tuned. Depending on the efficiency and effectiveness of that strategy, the energy savings can be improved.

For energy-deficient environments, a more flexible strategy is that the intelligence of the load is used to tune not only the voltage regulator but also the functionality of the load according to the amount of energy available. This is a so-called energy-aware system [31]. Figure 2-2 depicts a simple system paradigm in which the load functionality can be tuned according to a measurement of the available energy. As stated in the previous chapter, different task scheduling algorithms can be used for this purpose.

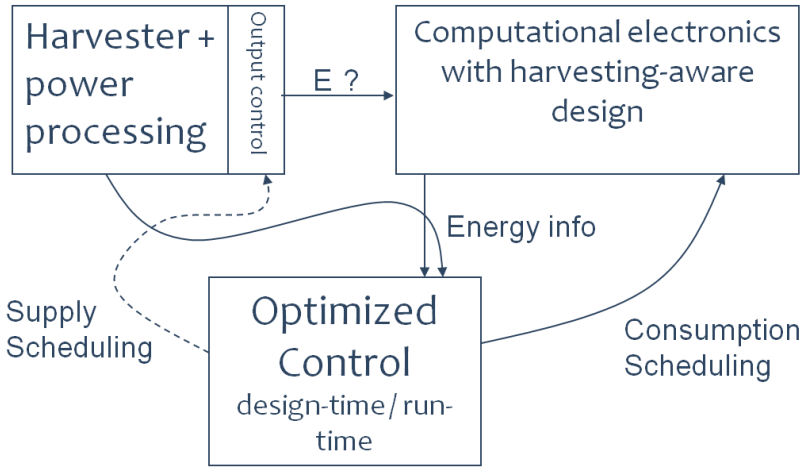


Figure 2-2 Energy-aware paradigm for an energy harvesting system [31].

In this system, regardless of the strategy employed by the load, measuring energy resources is required. In the system shown in Figure 2-1, this information can be safely collected from the energy storage element. Considering the fact that the energy storage is in the form of a fixed capacitor (C), the energy (E) is obtained by simply measuring the voltage (V) on the capacitor ($E = CV^2$).

It should be noted, however, that the energy harvesting systems provide a fundamentally different operating environment for electronics compared to conventional systems. For example, in terms of voltage measurement, the conventional assumption of having access to a reliable reference (in the form of voltage or time) is no longer valid. Of course, given that it is the supply voltage which varies; this is the unknown voltage which should be measured.

2.2 Voltage measurement techniques

The importance of voltage measurement in the design of energy-aware systems to operate in energy harvesting environment has been discussed in the previous section. In this section, different techniques of voltage measurement are detailed.

2.2.1 Mode selector or POR

Mode selectors (MS) [27, 28, 32] or power on-reset (POR) [33] circuits are designed mainly to control the mode of circuit or system operation by detecting certain voltage levels. In these circuits, the output voltage is held low while the input voltage is below a certain threshold. This can be used to guarantee that, at low voltage, the circuit does not enter into an unknown state. At a sufficiently high input voltage to guarantee robust circuit operation, the output voltage is set high. Examples of MS and POR circuits are described below.

As can be seen in Figure 2-3, for a value of V_{in} higher than a certain threshold, the voltage on the gates of *M1* and *M2* is fixed. This configures the state of the cross-coupled latch (*M3* and *M4*) so that V_{out} is set high. If V_{in} drops below that threshold, the state of the cross-coupled latch is inverted and V_{out} declines to zero.

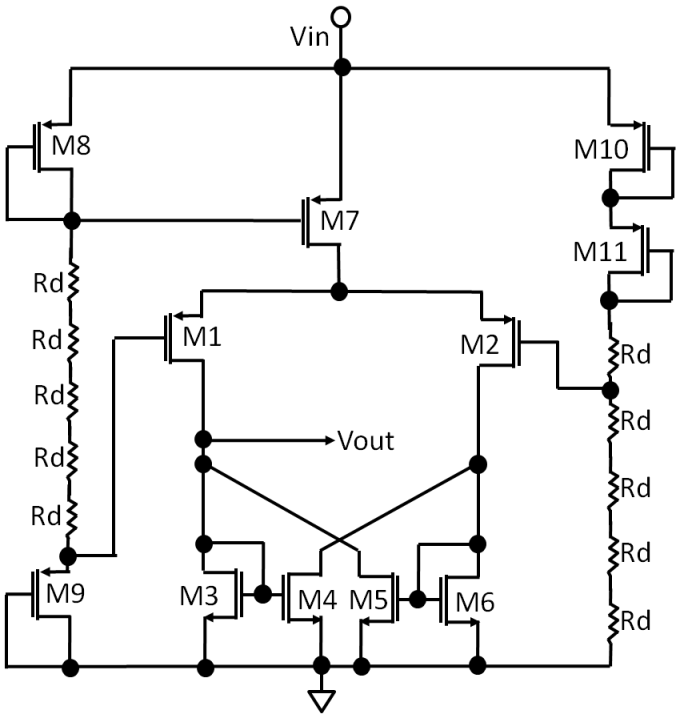


Figure 2-3 Mode selector circuit [32].

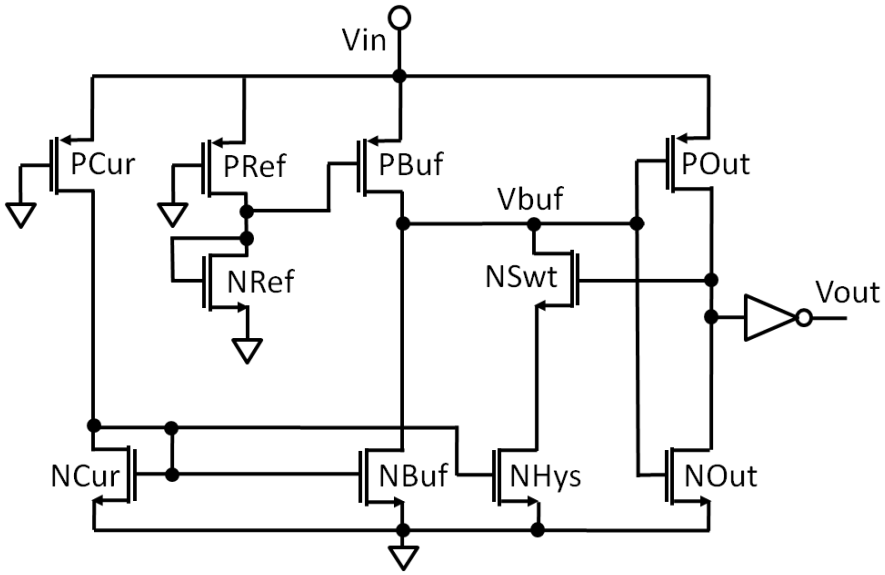


Figure 2-4 Power on-reset signal [33].

Figure 2-4 shows a simple implementation of a power on-reset circuit. In this circuit, the V_{ref} voltage generated as result of the voltage divider (P_{Ref} and N_{Ref}) controls the current mirror (P_{Buf}). For low V_{in}, the V_{Ref} is not sufficiently low to switch on the P_{Buf} transistor, and therefore V_{buf} is very small so that the output voltage consequently drops to zero. At sufficiently high V_{in}, the V_{ref} is low enough with respect to V_{in} to turn on the P_{Buf} transistor and therefore the current between P_{Buf} and N_{Buf} is copied from the P_{Cur} and N_{Cur} branch. As a result, a fairly high value of V_{buf}, ideally close to V_{in}, is generated and that sets the output voltage to be high. In principle, the circuit output voltage jumps from high to low and from low to high at the same value of input voltage. However, using N_{Swt} and N_{Hys} transistors, a hysteresis window is created. While the output voltage is high, N_{Swt} is in the off state, and while it is low N_{Swt} is on. This makes the low to high threshold voltage slightly bigger than the high to low threshold.

2.2.2 Voltage sensing using comparators and reference generators

Another widely used method of voltage sensing, or even of measurement when it is called a Flash ADC, is based on the simple idea of comparing the unknown voltage with a known voltage reference [34]. In this method, the state of the output voltage is shown if the unknown voltage is higher or lower than the reference voltage. Figure 2-5 shows a general overview of such sensing techniques.

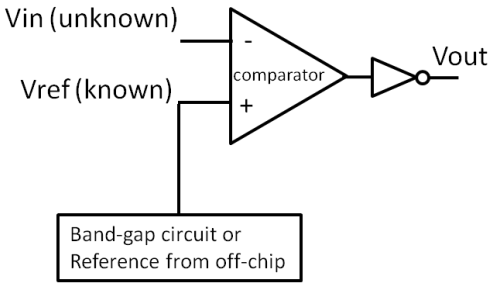


Figure 2-5 Voltage sensing based on comparison to a reference.

2.2.2.1 Band-gap circuit

Band-gap circuits are probably the most commonly used circuits in the chip industry used to generate an on-chip fixed and stable reference voltage whenever it is needed [35, 36]. Their operation relies on the characteristics of bipolar transistors, and specifically the effect of temperature on the base-emitter junction. For this junction the relevant equations are:

$$V_{BE} = \ln\left(\frac{I_c}{I_s}\right) V_T \quad , \quad V_T = \frac{K_b T}{q} \approx 26mv \; at \; 25° \qquad (2-1)$$

Where I_c is the collector current, I_s is the reverse saturation current, V_T is thermal voltage, K_b is the Boltzmann constant and q is the electrical charge. Thermal voltage has a positive temperature coefficient and I_s is directly related to temperature. The

combination of these two effects establishes an inverse relationship between V_{BE} and temperature. On the other hand, ΔV_{BE} is directly related to temperature:

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = \ln\left(\frac{I_{c2}}{I_{c1}}\right) V_{th} \qquad (2-2)$$

In a band-gap circuit, V_{BE} and ΔV_{BE} are combined in a way that temperature variation effect on circuit operation is hugely eliminated.

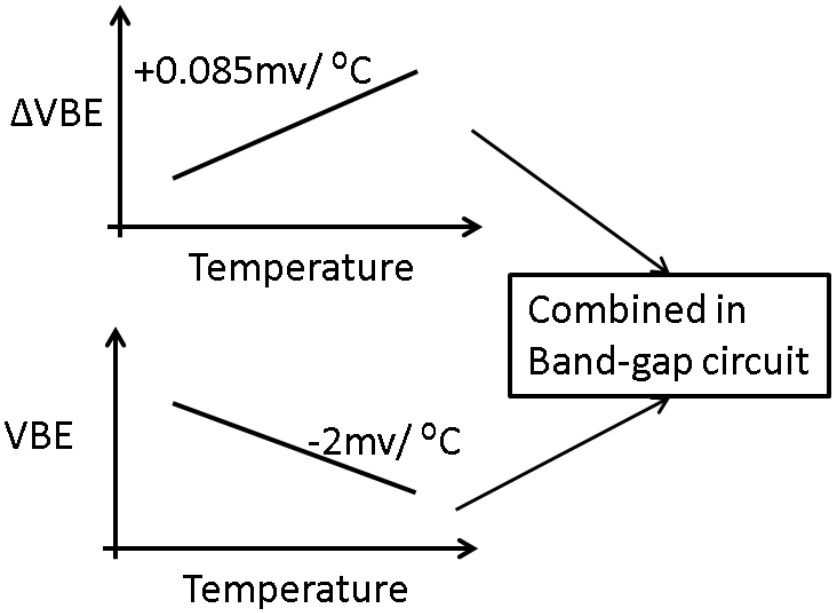


Figure 2-6 Relationship between the V_{BE} and ΔV_{BE} [37, 38].

Figure 2-7 shows a simple band-gap circuit whose output voltage is relatively independent of temperature variation.

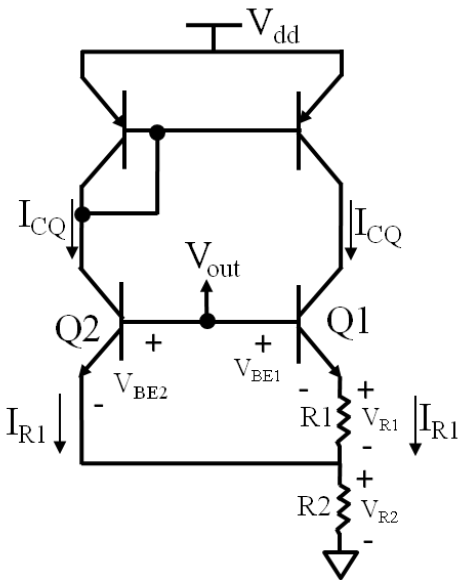


Figure 2-7 A simple band-gap circuit.

$$V_{R1} = V_{BE1} - V_{BE2} = \Delta V_{BE} \quad , \quad I_{R1} = \frac{\Delta V_{BE}}{R1} \qquad (2-3)$$

$$V_{R2} = R_2 2 I_{R1} \Rightarrow V_{R2} = R_2 2 \frac{\Delta V_{BE}}{R1} \qquad (2-4)$$

$$V_{out} = V_{BE2} + V_{R2} \qquad (2-5)$$

As can be seen, since V_{out} is a combination of V_{BE} and ΔV_{BE}, it stays constant over a range of temperature variations.

2.2.3 ADC

Converting analogue voltage into a digital value using the ADC is perhaps the most popular method of measuring on-chip voltage in the microelectronics industry. Several examples of widely used ADCs are detailed below.

2.2.3.1 Voltage-to-time converter (VTC)

Reshaping an unknown voltage into a form of signal which is countable is the crux of this technique. For example, in a voltage-to-time converter, the voltage is applied to a voltage-controlled-oscillator (VCO) [39, 40] to generate a signal with a unique

frequency. In VCO, the output frequency is a function of the input voltage, so that the higher the voltage, the higher the frequency and vice-versa. In later stages, this frequency is counted within a fixed interval of time using a simple counter.

Figure 2-8 shows a simple implementation of the voltage to time and time to digital converter. The main issue with this method is that the output is not only a function of voltage but also of variations in process and temperature. This technique also requires a fixed time reference to enable and disable the counter.

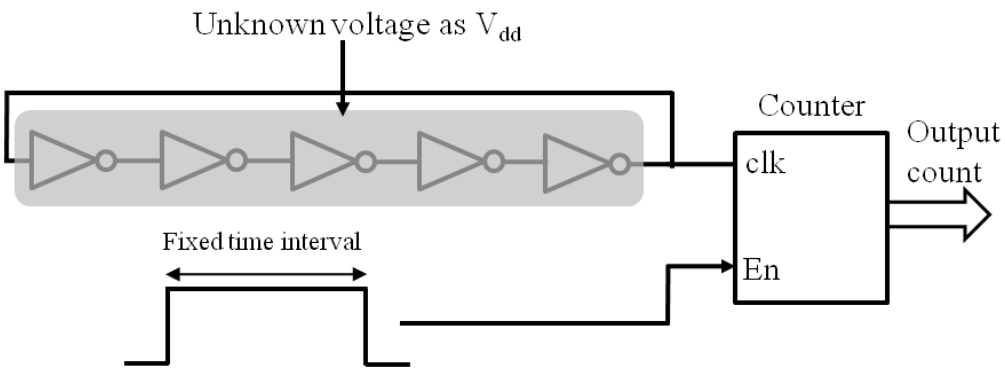


Figure 2-8 Voltage to time and time to digital converters.

Figure 2-9 shows a block diagram of another implementation of the voltage-to-time-to-digital technique which uses a digital delay line to generate the thermometer code which is then converted into binary. In this implementation, the start signal is simply a rising edge and is fed into the delay line. A signal transition from “0” to “1” occurs at the output of each delay element which receives the start signal. After a fixed time interval, the stop signal is applied which samples the output of all of the delay elements. This output will be in the form of a thermometer code (for example, 11…100…0) which will be converted into binary code using combinational logics.

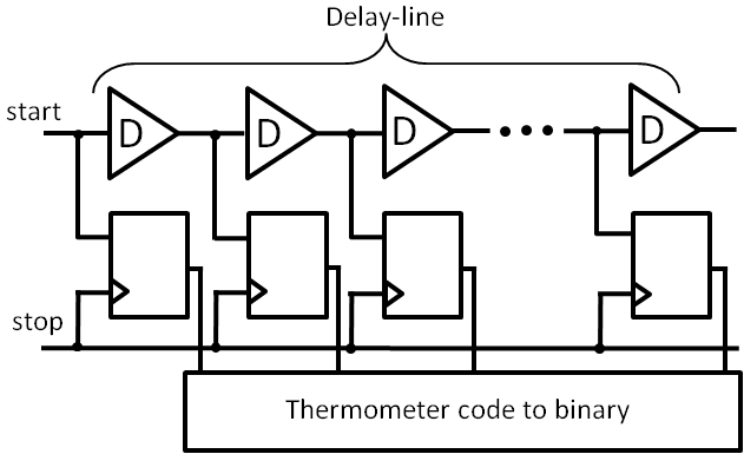


Figure 2-9 Voltage to time to digital using delay line.

In this technique, the delay line is powered by the voltage which is unknown. Therefore, the delay property of each delay element will be a function of the voltage under measurement. Thus, each value of the unknown voltage produces a unique thermometer code (unary code) at the output of the delay line [41]. As with the previous implementation, the delay line's operation is not only sensitive to the supply voltage but also to process and temperature variations. Therefore, additional logistics are required to make the design robust against unwanted variations. The following table shows the 4-bit thermometer code representation [42]:

Table 2-1 Four-bit thermometer code.

N	Thermometer code
0	0000
1	1000
2	1100
3	1110
4	1111

2.2.3.2 Charge run down ADC

Figure 2-10 shows a simple block diagram of the run-down ADC [43]. In this ADC, the unknown analogue voltage is sampled into a capacitor. At the time of conversion, the capacitor is discharged through a constant current source (*I*). The voltage on the capacitor is constantly observed using a comparator for a certain threshold (in this case *GND*). While the capacitor is discharged, the output voltage of the comparator is high, and therefore the counter is enabled and counts a fixed clock frequency. At the point at which the voltage on the capacitor reaches the threshold voltage (capacitor is fully discharged), the comparator output drops to zero and this disables the counter. The count value of the counter is then the digital value of the input analogue voltage.

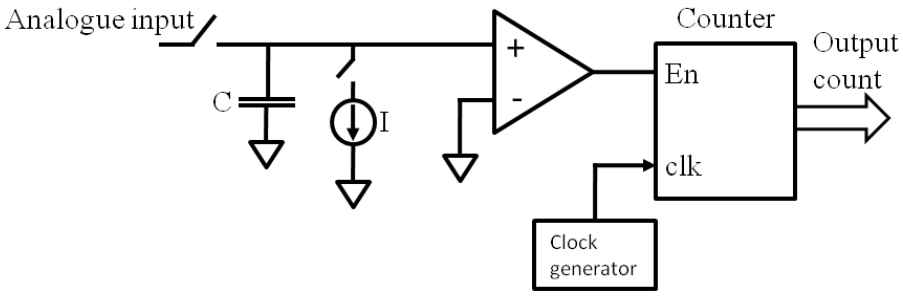


Figure 2-10 Charge run down ADC.

2.2.3.3 Successive-approximation register (SAR)

Successive approximation technique converts the analogue voltage into a digital value using a method called binary search [44, 45]. The conversion in this technique can be simply explained in two phases. In the first phase, using a binary search algorithm, a binary combination is applied to a DAC. The DAC generates an analogue voltage which, in the second phase, is compared to my unknown input voltage using a simple comparator. The binary code which generates the closest value to my unknown voltage

is the digital output of the ADC. Figure 2-11 depicts the block diagram of a simple SAR ADC [46].

At the beginning of the conversion phase, the digital code generated by SAR logic is *MSB*='1' and the other bits are zero. This generates $V_{ref}/2$ at the output of the DAC. This voltage is compared to the unknown input voltage. If it is greater, *MSB* is set to zero and if it is less, *MSB* is held high. Then SAR moves to the next bit down and performs the same procedure. At the end of the conversion phase, a digital combination is achieved which represents the value of the unknown input voltage. Since in the binary search method all possible quantization levels are generated and tested, this ADC is very slow in high resolution applications.

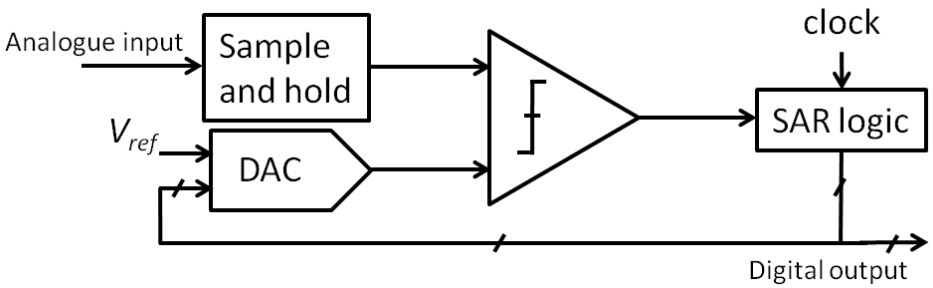


Figure 2-11 Simple block diagram of SAR ADC.

There exists another implementation for SAR ADCs called charge redistribution, which uses a charge scaling DAC architecture [47]. A simplified circuit of a charge redistribution implementation of these types of ADCs can be seen in Figure 2-12. The circuit operates in three modes; sample, hold and redistribution modes. In the sample mode, the switch S_A is connected to the input voltage (V_{in}) and the switch S_B is closed. As a result, V_{in} is sampled on each capacitor in the network. In the hold mode, S_B is opened and $S_0 \ldots S'_{N-1}$ are connected to the ground, therefore V_C becomes $-V_{in}$ which means that the V_{in} has been sampled at the input of the comparator. In the redistribution

mode, the S_B is opened and the S_A switch is connected to the reference voltage (V_{ref}). In this mode the actual conversion is started by connecting the *MSB* switch (S_0) from the ground to the V_{ref}. The equivalent capacitor in the network is *2C*, and therefore connecting *C* to the V_{ref} creates a 1:1 capacitor divider between *C* and the remaining capacitors in the network, which is also *C*. This produces a value of V_C equal to $-V_{in}$, which was charged to the network before, plus $V_{ref}/2$ which is obtained as a result of the 1:1 capacitor divider. The value of the bit is determined by the operation of the comparator at this stage. For values of V_C lower than zero, which means that V_{in} is greater than $V_{ref}/2$, the comparator output jumps to high. This indicates that the *MSB* should be set to logic "1". Conversely, for values of V_C greater than zero, the comparator output stays low which indicates that the *MSB* should be set to logic "0". The conversion is carried out for all the bits in the same way until the value of *LSB* is produced. V_C for the *LSB* is $-V_{in} + (MSB)V_{ref}/2 + (MSB\text{-}1)V_{ref}/4 + \ldots + (LSB)V_{ref}/2^N$. According to the operation of this ADC, at the end of the conversion cycles, V_C should converge to zero.

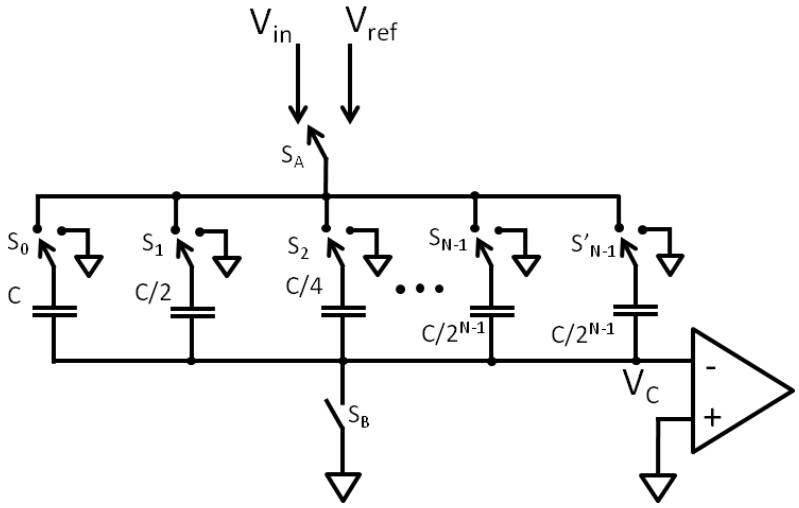


Figure 2-12 N-bit SAR-ADC based on charge redistribution.

The major energy consumption involved in the charge redistribution implementation of SAR ADCs is due to the generation of a fixed voltage reference. There exist a number of clever SAR ADC designs in which the designer removes the requirement for a reference voltage [48, 49] by using differential configurations for the capacitor network. Furthermore, an extra capacitor is used to shift the input voltage to high and to create $2V_{in}$ voltage. Then, the ADC will compensate for $2V_{in}$ so that at the end of the conversion cycles V_C converges to V_{in}, as opposed to the conventional design in which V_C would converge to zero. However, although the requirement of a voltage reference is removed, the fixed clock frequency and accurate switching timing are still required [50].

2.2.3.4 Delta-sigma ADC

In this section, the operation of the delta-sigma ADC is studied largely from an experimental point of view [51]. A simple block diagram of such ADC is depicted in Figure 2-13. In this ADC, the unknown input voltage is differentiated from the output of the DAC (in the feedback loop) to provide the input to the integrator.

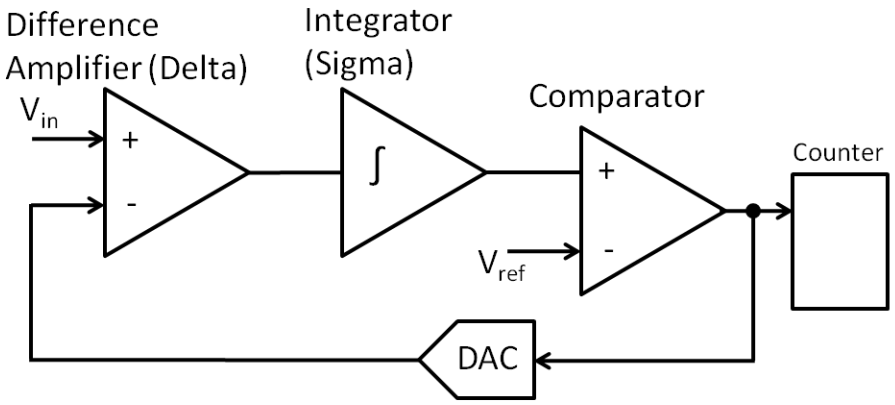


Figure 2-13 Delta-sigma ADC.

The integrator generates a ramp signal in response to the edges of the input pulses. The ramp signal is compared to the reference voltage at the comparator, generating a bitstream at its output. As shown in Figure 2-14, this bitstream is oversampled using a counter with a clock frequency of at least double the frequency of the bitstream (Nyquist rate). Usually, the output of the counter is applied to a low-pass filter to remove the effects of quantization error and oversampling noise.

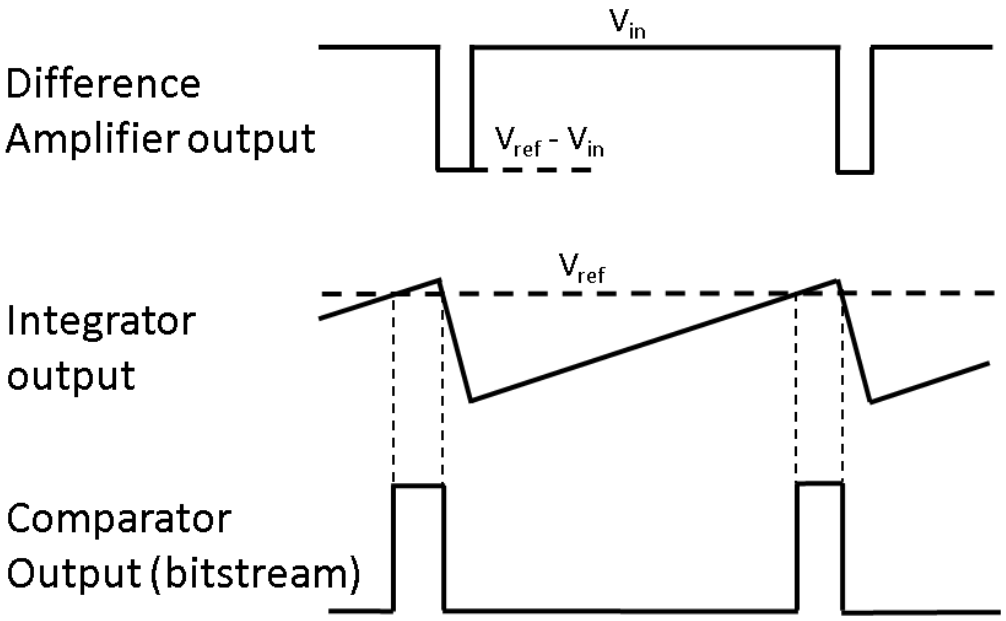


Figure 2-14 Delta-sigma operation waveforms.

The delta-sigma ADC is capable of producing high resolution output; however, due to oversampling, it is fairly slow compared to other types of ADCs.

2.2.3.5 Flash ADC

In the flash ADC, the input voltage is simply compared to several pre-set values using a number of analogue comparators. For each voltage interval that the input analogue voltage is realized in, a binary code is generated using simple combinational logics. Flash ADCs are well known for their speed of conversion compared to other types of ADCs. However, a significant number of comparators, even for low levels of precision, is required. In order to mitigate this, a design has been reported which uses simple sense amplifier flip-flops instead of an analogue comparator [52].

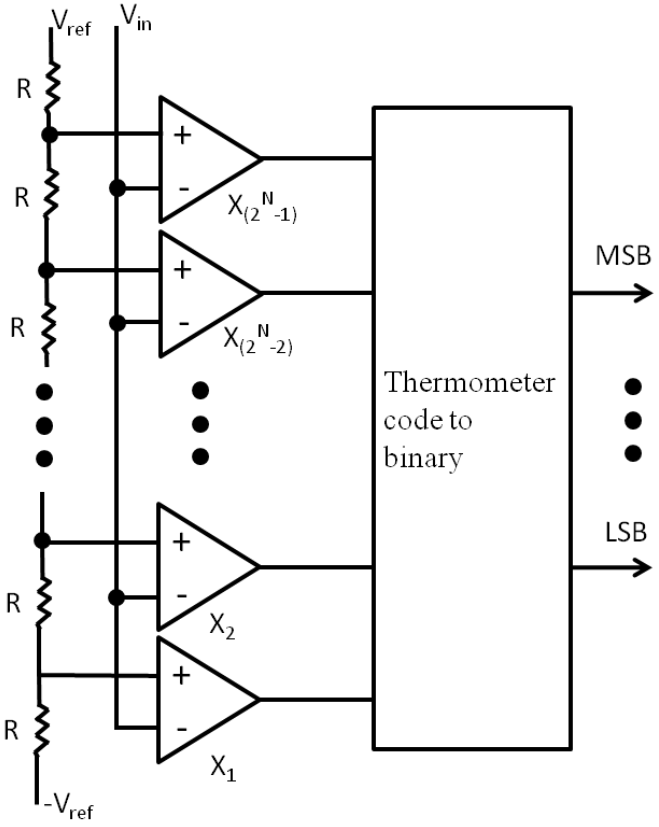


Figure 2-15 Block diagram of Flash ADC.

Following table provides an overview of different analogue to digital converters in terms of speed, precision, power consumption and types of reference requirements:

Table 2-2 an overview of different ADC techniques.

Type of ADC	Advantageous	Disadvantageous	Reference required
SAR	Medium to high resolution (8-18 bits) [46]	Medium speed (up to 5Msps)	Voltage and time reference
Delta-Sigma	High resolution (16-24 bit), low power consumption [53]	Low speed due to oversampling (typical range of 100Ksps up to 4Msps for ADS1271 and ADS1675 from Texas Instruments)	Voltage reference and fixed clock pulse
Flash	Very fast (Gsps) [53]	Low resolutions (8-bit), large power consumption and area	Voltage reference

Table 2-2 shows that providing reference (voltage and time) for above ADC designs is essential. However, the above table contains only ADCs which are discussed in this thesis, there are no reference-free ADCs in the literature. Consequently, they will fail to operate in the energy harvesting environment.

It is intuitively obvious that, for any electronic circuit operating in an energy harvesting system, energy consumption is crucial. Note that, in these systems, designing low-energy consumption circuits is not the goal but a prerequisite. In the following section, the circuit energy consumption is analysed however, low-energy consumption techniques are described in Appendix A.

2.3 Circuit energy consumption

Energy in a circuit is consumed through dynamic (or switching), static (or leakage) and short circuit energy dissipation [54].

$$E_{Total} = E_{Dynamic} + E_{static} + E_{short-circuit} \qquad (2-6)$$

The energy consumption of a switching action is called dynamic energy consumption, which is quadratically related to V_{dd} [55]:

$$E_{Dynamic} = \alpha C {V_{dd}}^2 \qquad (2-7)$$

Where α is the activity factor (the number of active nodes in the circuit per cycle), C is the switch capacitance and V_{dd} is the supply voltage. For supply voltages above threshold level, switching or dynamic energy consumption is dominant.

The next type of energy consumption in a circuit is static or leakage energy consumption. This type of energy consumption exists due to the current leakage in transistors which are not switching. Static energy consumption is given by [55]:

$$E_{static} = V_{dd} I_t e^{\frac{V_{gs}-V_{th}}{nV_T}} \left(1 - e^{-\frac{V_{ds}}{V_T}}\right) T \qquad (2-8)$$

$$I_t = \mu_{eff}\, C_{ox} \frac{w}{l_{eff}} (m-1) {V_T}^2 \qquad (2-9)$$

Where I_t is a technology-dependent scaling parameter, V_{gs} is the gate-to-source voltage, V_{ds} is drain-to-source voltage, V_{th} threshold voltage, V_T thermal voltage, n is related to the subthreshold slope, T is the latency of computation, μ_{eff} is the effective mobility, W is the transistor width and l_{eff} is the effective channel length.

When the input signal is applied to a circuit, there is a moment at which the NMOS and PMOS transistors are simultaneously on. At that moment a path is established from V_{dd} to *GND*. The current flowing through that path creates the short-circuit energy dissipation [56]:

$$E_{short-circuit} = \frac{\beta}{12} (V_{dd} - 2V_T)^3 \tau \qquad (2-10)$$

Where β is the gain factor, τ is the rise or fall time of the inputs of the inverter. Since the amount of short circuit energy dissipation is very small compared to the dynamic and static energy consumption, it is usually neglected in calculating total energy consumption [56].

Asynchronous circuits are mostly described as low-power circuits. The following section details the asynchronous design technique in terms of power consumption.

2.3.1 Asynchronous design

Most digital circuits are designed using a global clock signal. This signal allows events in the circuit to be accurately timed. For example, the clock signal can be used to synchronize the necessary communication, and also to sequence the operations within

the circuit. From a design point of view, circuits which employ clock signals in their operations are called synchronous circuits, whereas asynchronous circuits are designed to be clockless. For the latter circuits, operations are timed relative to each other rather than to a global clock signal. For instance, a handshaking protocol can be used to configure the communication or sequence between operations in the circuit. Several of the most common such protocols are described below.

2.3.2 Bundled data

In this protocol, the data in normal Boolean format traverses between components using *Req* and *Ack* signals. This is typically implemented either in a 4-phase or 2-phase handshaking protocol. In 4-phase, when the *data* is ready the sender sets the *Req* high, where at this stage *Ack* is low. The receiver detects the high *Req*, samples the data and sets the *Ack* high. The sender notices the positive edge of the *Ack* signal and sets *Req* low. At the end, the receiver senses the low *Req* and so in response it sets the *Ack* low. This protocol is presented in Figure 2-16 using *data*, *Req* and *Ack* waveforms.

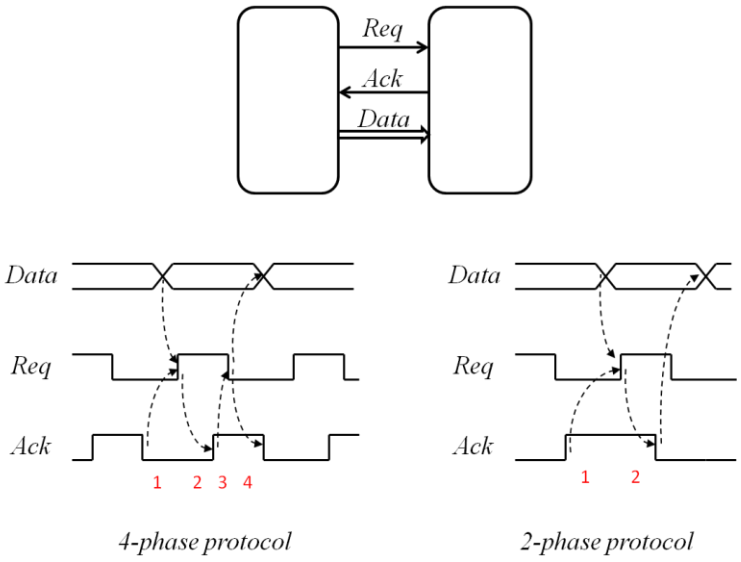


Figure 2-16 Bundled data protocol

The unnecessary transition to zero in 4-phase handshaking costs energy and reduces speed. In comparison, the 2-phase handshaking protocol does not create any transition to zero. Using simple waveforms, this protocol is shown in Figure 2-16. Note that here the signal events (or edges) on *Req* and *Ack* are used to complete the communication. In this protocol, once the receiver is ready to receive the data and the data is ready, the sender issues a signal event on the *Req* wire. The receiver detects this, absorbs the data and generates an event on the *Ack* wire which signals that the handshake is finished.

2.3.2.1 Request signal

In the bundled-data protocol, one of the critical assumptions is that the sender issues the *Req* signal after producing the data. As a result, different techniques and design methods have been explored to guarantee the appearance of the *Req* signal after the *data*. Some of these techniques are listed below:

a) The circuit is designed in such a way that it generates a completion signal at the end of its operation.

b) The circuit is bundled to a delay line. The assumption is that the delay line is longer than the longest delay path in the circuit.

c) In using a dual rail protocol, each logic bit is encoded into true and false signals as presented in Figure 2-17. A spacer stage which acts as completion signal is accommodated between two successive valid data items.

	t f
spacer	0 0
Logic 0	1 0
Logic 1	0 1
Not used	1 1

Figure 2-17 Dual rail encoding

Due to the removal of the clock signal in asynchronous circuits, they are classified into three different classes according to the quality of their operation with respect to the delay assumptions made:

a) Self-timed or bundled delay circuits, which require extra effort and consideration in order to satisfy all timing assumptions so as to operate robustly.

b) Speed-independent circuits, where the circuit operation is robust irrespective of gate delays and assuming that wire delays are negligible.

c) Delay-insensitive circuit operation is robust assuming any arbitrary values for gate or wire delay.

In synchronous circuits, using the clock signal makes the design process easier, but the energy consumption of the circuit increases. Since the clock frequency is set for the longest delay path in the circuit, with perhaps an extra safety margin, an idle state is created at each clock cycle for the shorter delay paths in the circuit. This increases the

leakage energy consumption of the circuit. Generating and maintaining the clock signal is another source of energy overhead in synchronous circuits. Avoid clocking the circuit by using asynchronous circuits is one of the approaches used to decrease the energy consumption of the system [54, 57, 58].

Typically, asynchronous circuits consume less energy compared to their synchronous counterparts. One of the reasons for this is that the asynchronous operation does not allow for an idle state in the circuit, and therefore the leakage energy consumption decreases dramatically. In asynchronous designs, a completion detection signal is generated at the end of circuit operation. Once the completion detection is issued, the circuit realizes the outputs and starts a new task and thus no idle state is created. A circuit with no idle mode has less time to leak.

Despite the advantages mentioned above, employing asynchronous circuits can create a number of challenges. For instance, designing a circuit which can produce a completion signal is not an easy task. Therefore, techniques such as bundled delay lines or dual-rail implementation are used which require extra logic. The extra logic added to these circuits usually increases the energy consumption overhead. Another challenge is that the asynchronous designs are not fully supported by commercial Electronic Design Automation (EDA) tools [57]. Therefore, asynchronous circuits are often implemented using custom-built tools.

2.3.3 Dynamic voltage scaling (DVS)

It is well-known that the supply voltage (V_{dd}) has a direct effect on the circuit energy consumption and operating speed [59]. An example of voltage scaling to achieve low-energy consumption is to operate at the subthreshold region below the transistor threshold [55, 60, 61]. In this region, which is also called weak inversion, the ratio of

(I_{on} /I_{off}) decreases exponentially (in subthreshold) [60]. I_{on} is defined as the drain-to-source current when the transistor is on and I_{off} is the current when the transistor is in the idle mode.

It is known that, if circuit supply voltage (V_{dd}) is decreased, the gate propagation delay (T) will increase exponentially, [55] and therefore leakage (static) energy consumption (E_s) increases exponentially. For values of V_{dd} greater than the threshold voltage, the dynamic energy consumption is dominant, and hence total energy consumption decreases while V_{dd} decreases. In the subthreshold region, the leakage grows exponentially when V_{dd} decreases. At a certain level of V_{dd}, the amount of leakage energy consumption will exceed the amount of dynamic energy consumption, and consequently the total energy consumption starts to increase with decreasing V_{dd}. At that level of V_{dd}, the circuit energy consumption per switching activity is at a minimum, and this is called the minimum energy point (MEP) [29]. As an example, the energy consumption of a simple asynchronous counter is plotted in Figure 2-18. This figure shows that the counter energy per count is at its minimum at 280mV. Research has shown that, by operating at the minimum energy point, more than 50% energy savings can be achieved [29].

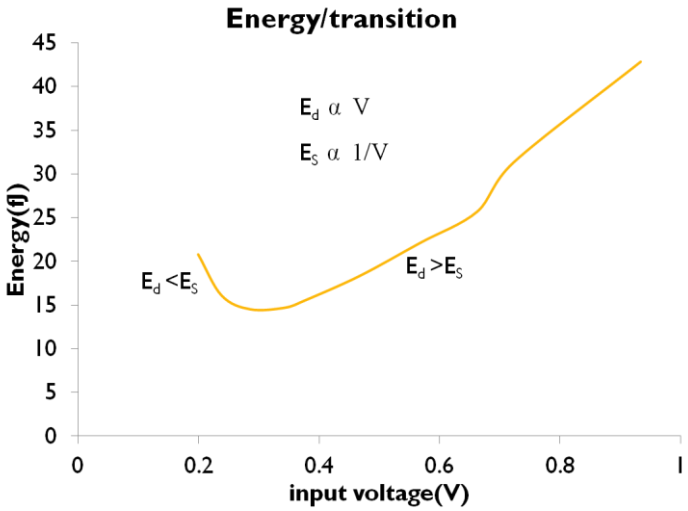


Figure 2-18 Energy per transition for an 8-bit asynchronous counter.

For this simulation, energy consumption of the counter was measured under different fixed level of supply voltages.

2.3.4 Dynamic frequency scaling (DFS)

The frequency of the clock signal in a circuit is determined by the speed of operation in the circuit. On the other hand, the speed of operation in the circuit is determined by the supply voltage of the circuit. Therefore, the level of supply voltage is determined by the frequency of the clock signal of the circuit. In dynamic frequency scaling technique the frequency of clock signal is decreased, consequently, the required supply voltage can be decreased. Therefore, by decreasing the supply voltage the overall energy consumption of the circuit is decreased. This technique is often referred to as dynamic voltage/frequency scaling (DVFS) as the true energy saving comes from decreasing the supply voltage [62].

2.3.5 Voltage converters

The key requirement of DVS is to design an efficient DC to DC converter which can scale the level of voltage according to the demand from the load circuit. A considerable

amount of research has led to numerous novel designs of DC to DC converters with high efficiency. For instance, a traditional buck converter has been modified in order to operate not only in the pulse-width-modulation (PWM) mode but also in the pulse-frequency-modulation (PFM) mode [63]. In this design, a novel technique of analogue-to-digital conversion using a ring oscillator and counters is proposed. In this paper, the experimental results show the highest efficiency for a low current load at PFM mode, while for higher load currents PWM is the most efficient mode. It has been shown that at high current load situation, the conduction loss is the main source of the power loss, therefore, varying the frequency of switching at power transistors, similar to operation at PFM mode, will decrease the efficiency [64]. In this situation PWM offers higher efficiency. Conversely, at light current load, the quiescent power loss is dominant, therefore, operating at PFM mode which offers lower quiescent current, gives higher conversion efficiency compared to PWM mode [64]. Another DC to DC converter design [65] uses current-mode-control (CMC) feedback. Studies have shown that CMC approach outperforms voltage-based control in terms of simplicity and also over-current protection [66, 67]. It is argued in one study [65] that the peak inductor current is relatively high at discontinuous-conduction mode. Therefore, the power transistor, and thus the chip area required for this mode of operation, must be large. On the other hand, continuous-conduction mode gives higher efficiency when the operation frequency is of the order of a few megahertz, and a fast current sensing circuitry is proposed in order to achieve a switching frequency of a couple of megahertz. In a further study [68] the authors show that driving transistors in the power train with different voltages increases efficiency and also the load current for the same transistor sizes. An additional interesting DC to DC converter has also been proposed in [69]. In this design, the input voltage to the chip is greater than the nominal voltage of the technology. Therefore, it is proposed to stack transistors in the power train. The control circuitry in this design is

powered by a separate on-chip switched capacitor converter. In order to apply control to the transistors in the power train, a set of voltage shifters are designed.

As stated before, more techniques of energy saving in a circuit at transistor-level and system-level are described in Appendix A.

2.4 Power platform designed by Maxim

Figure 2-19 shows a block diagram of the power platform designed by MAXIM for energy harvesting applications. This platform can operate using both high voltage and low voltage energy harvester sources. According to its specifications, this device has two main functionalities. The first is to charge a battery cell and the second is to provide the consumer with regulated voltage.

As seen in Figure 2-19, the high voltage energy harvester is connected to the pin called CHG and the battery cell is connected to the BATT pin. While the V_{CHG} is greater than V_{BATT}, the battery cell is charged. This path is protected by a 5.3V shunt protection circuit so as not to overcharge the cell. An external protection circuit is also employed at the CHG pin if the V_{CHG} exceeds 5.3V.

The low voltage energy harvester charges an external 47uF capacitor. Once the voltage on this capacitor (FB) exceeds the FB_{on} threshold, the boost converter starts operating. This generates a PWM signal on the LX pin with a 90% duty cycle. The external inductor forces a voltage greater than the V_{CHG} on the LX pin. This creates a path from LX to the CHG pin which charges the 0.1uF capacitor. After a while, the voltage on the 47uF capacitor will drop below the FB_{on} threshold and the boost converter stops operating.

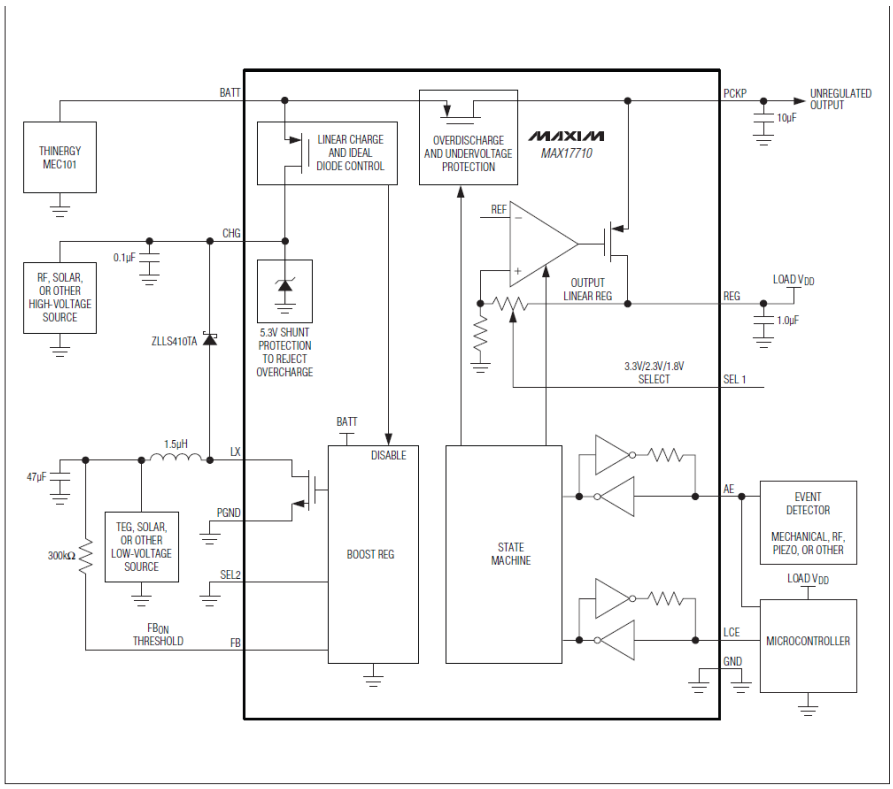


Figure 2-19 Block diagram of MAX17710 designed by *MAXIM*.

To generate a regulated output voltage, a reference voltage is generated from V_{BATT} which is stable at any time. This voltage is applied to a conventional LDO which consists of a comparator and a FET, as seen in Figure 2-19. Once the voltage at the output drops due to load consumption, the V_G of the FET is lowered through the negative feedback loop and therefore more current is injected to the output which will compensate for the voltage drop. The same mechanism forces the output voltage to be low if it rises to too high a value. In this design, the gain of the feedback loop is designed to be adjustable. Therefore, the load can select the output voltage from three options: 3.3V, 2.3V and 1.8V.

A number of important functionalities required for energy harvesting systems are provided by this power platform. However, the main functionality required for energy-aware system, which is energy measurement, is not covered. In this power platform no

mechanism is available for the load to receive any information about the amount of energy available. Consequently, due to the absence of such a measurement, the load fails to follow energy-aware strategies.

MAX17710 is just discussed as an example of energy harvesting power platform in industry. In the same category, many companies have developed similar systems with different designs. For instance STMicroelectronics has announced SPV1050 with an already built-in MPPT circuit to tune the harvester and also Buck-Boost converter to adjust the output voltage [70]. Another example of such design is BQ25504 announced by Texas Instruments. The design provides nano-power management platforms from extremely low power energy harvesters (input voltage from harvester >= 80mV). DC-DC converter with high efficiency (90%) is yet another feature provided by this design [71].

2.5 Conclusion

It was previously discussed that the main aim of these thesis is to design a voltage sensor which can operate in energy harvesting environment. The conditions imposed by energy harvesting environments, require the measurement technique to operate without any reference voltage or time or a stable supply voltage [29, 72, 73]. From an extensive literature research it is clear that the existing methods of measurement do not have the capacity to operate in such environments, and it is clear that a new voltage measurement technique is required. This technique must be able to operate free of references with respect to voltage, current and time, under conditions of variations in supply voltage.

Chapter 3. Principle of capacitor charge to digital switching

3.1 Introduction

My proposed sensing method is based on the following two steps: (i) sampling the energy related to the sensed voltage into a storage, and (ii) mapping this energy into a digital code. The simplest solution to sample the energy is to employ a capacitor which pinches an amount of incoming energy and saves it in the form of electrical charge. Once the energy is sampled a measurement tool is required to measure it. This sensing method proposes to use the same energy stored in the storage as the energy source which runs the measurement tool. In other words, I discharge the capacitor through the switching actions of the circuit that implements the measurement tool. How to select a circuit for such a measurement tool? The main requirement for the circuit to do the job of converting the charge to code is that this circuit should maintain maximum proportionality (even if it's not linear), i.e. each portion of charge must turn it to a distinctive contribution towards the code value. There are various options to build such a circuit, but the important aspect is that it should not spend energy on switching actions that do not contribute to the code. This is where I need a sequential and hazard-free circuit.

The remainder of this chapter is as follows: Section 3.2 contains a comprehensive mathematical exploration of the relationship between switching behaviour of the circuit and the voltage drop while the circuit is powered by a capacitor. Section 3.3 describes the design of an asynchronous binary counter. This counter serves as the ruler in this scenario.

3.2 Capacitor discharging through dynamic digital switching

Let us consider the case where a self-timed circuit such as a ring oscillator, is powered by a capacitor C_s which is initially charged to produce a certain initial level of supply voltage. From the system point of view, a confined source of energy connected to a self-timed circuit creates an autonomous system which operates as long as energy is available in the source [74].

In a simple RC circuit the object of energy consumption is *R*, which is a resistive physical component. In my circuit, shown in Figure 3-1, switching activity is the main object of energy consumption. In the beginning, the capacitor is fully charged so the voltage on the capacitor is high. Thus, the oscillation frequency is high and in the same way, the rate of energy consumption is high. Every switching action draws some amount of energy from the capacitor. In consequence, the energy of the capacitor is decaying. This decreases the voltage on the capacitor and consequently, the frequency of the output oscillation is decreased. The output oscillation of this circuit is shown in Figure 3-2.

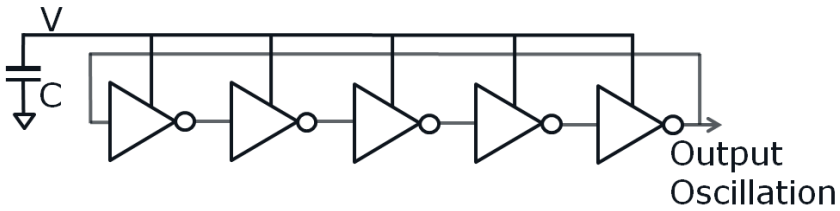


Figure 3-1 Ring of inverters being powered by a capacitor.

3.2.1 Circuit model

Switching activity in any digital circuit connected to an energy source is in fact a process of charging and discharging its parasitic capacitors through PMOS and NMOS transistors respectively.

In a simple ring oscillator, consisting of L (odd number) of inverters, each inverter receives the result of the previous inverter being flipped. Accordingly, the current inverter makes a transition from low to high or from high to low as it is shown in Figure 3-3. Let us define the sum of the capacitance of the drain diffusion of PMOS and NMOS and the capacitance of the wires and the fan-out gates as an equivalent small capacitor (C_l) attached at the output of each inverter [75]. During the transition from low to high the PMOS is on and NMOS is off, so C_l is charged from the main supply. This constitutes the major part of energy consumption of the inverter. In the opposite way, a high to low transition discharges C_l. At this state the energy which was taken from the main supply before, is discharged through NMOS.

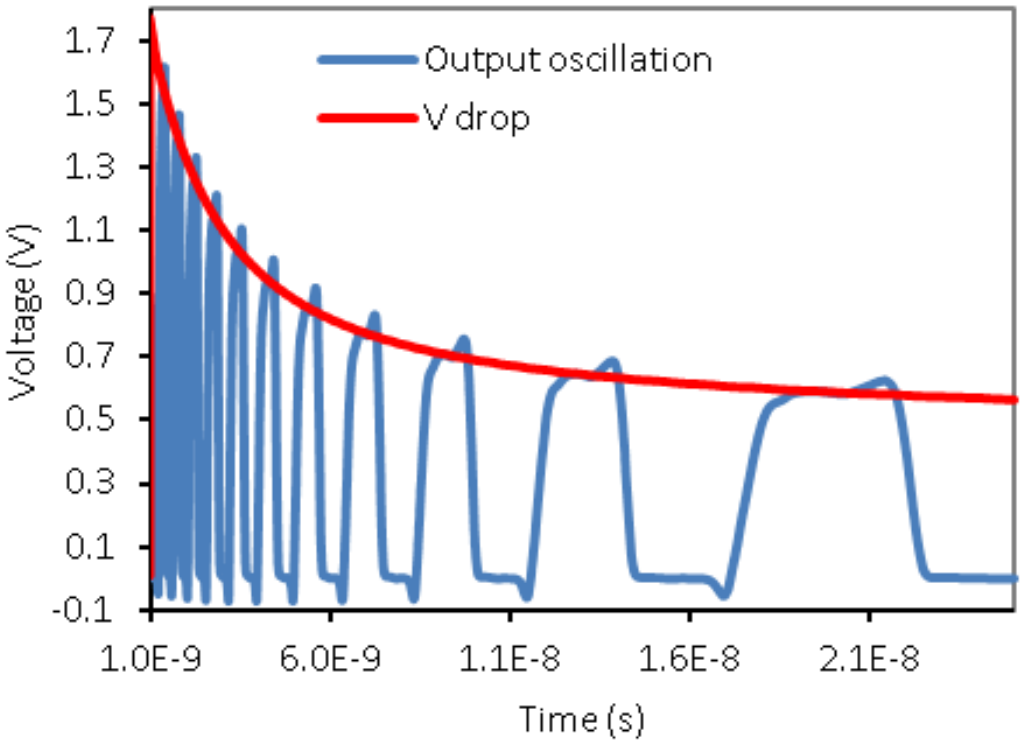


Figure 3-2 Output oscillation and voltage drop of the ring oscillator.

180nm UMC technology library was used for this simulation.

The operation of the ring oscillator can be explained in three states, shown in Figure 3-4. State 1 represents the circuit status when no charging or discharging action

takes place. Thus it is the situation when C_s is connected to the ring oscillator but no switching has been fired. Every other (say odd-numbered) inverter output is at logical 1, i.e. the corresponding parasitic capacitor C_l is charged to the level of voltage equal to that of C_s. The remaining inverter outputs are at logical 0 and their capacitors C_l are empty. This state also describes the circuit status between two successive switching actions. The system is in State 2 when a switching action occurs. One of the charged capacitors C_l (of the inverter which is supposed to switch from 1 to 0) is gradually discharged. There is no energy consumption from the source capacitor during this state (ignoring leakage). In State 3 the discharged capacitor associated with the next inverter in the ring (which is supposed to switch from 0 to 1) starts receiving charge from the source capacitor. This is the only state which draws energy from the main supply. Note that, in real operation an overlap exists between State 2 and 3, however, to simplify the analysis I consider them as distinct states.

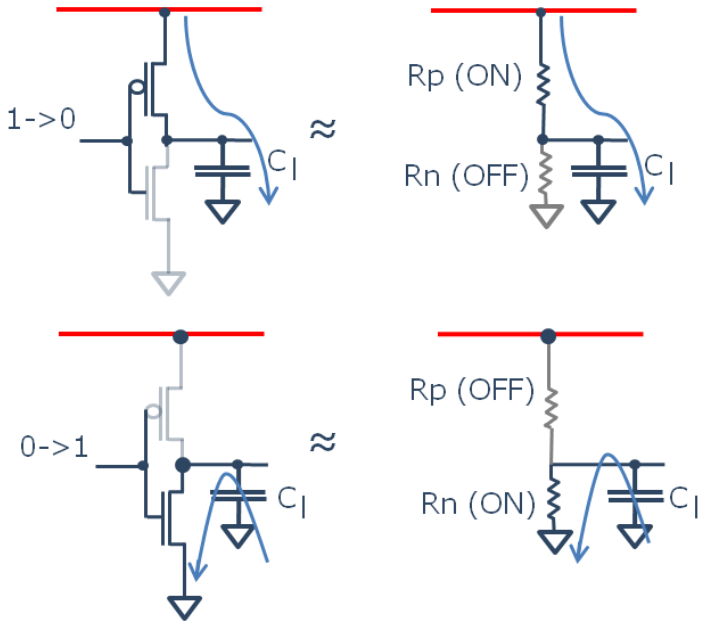


Figure 3-3 Transistor switching in an inverter

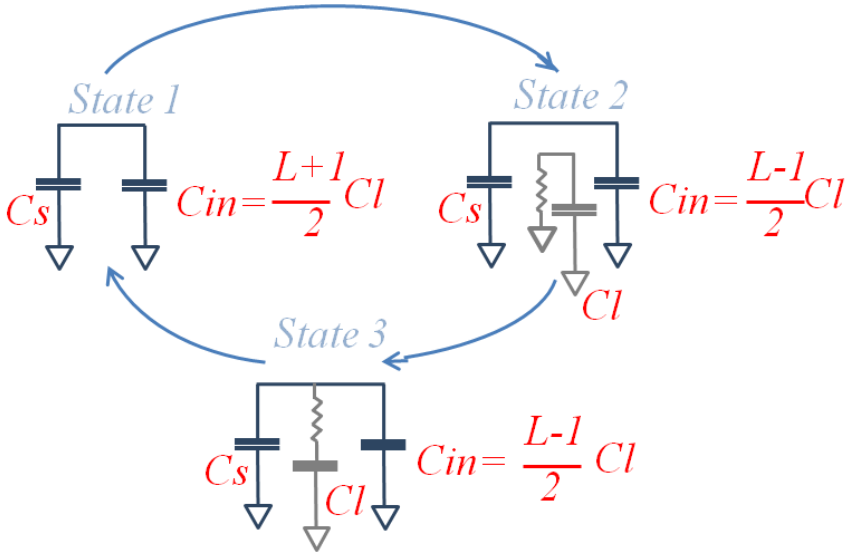


Figure 3-4 Circuit state at dynamic switching, L is the number of inverters.

Figure 3-5 depicts a simple RC structure which models the ring oscillator in the third state. R_s is the resistance of a PMOS transistor while it conducts, R_l stands for the leakage resistance, C_s is the sampling capacitor and C_l is the output parasitic capacitance of each inverter. I use ordinary differential equations (ODE) to explore the voltage dropping function over time. For this circuit I can write:

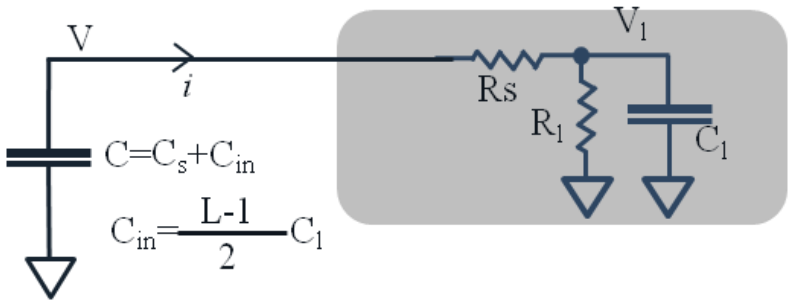


Figure 3-5 RC model for ring oscillator in terms of power consumption.

$$i = \frac{V - V_l}{R_s} = C_l \frac{dV_l}{dt} + \frac{V_l}{R_l} \qquad (3-1)$$

$$V_l = V - R_s i, \;\; i = -C \frac{dV}{dt} \qquad (3-2)$$

Using (3-1) and (3-2) and considering $C >> C_l$, the ODE for the circuit is:

$$\frac{d^2V}{dt^2} + \left(\frac{R_s + R_l}{R_s R_l C_l}\right)\frac{dV}{dt} + \frac{V}{R_l R_s C_l C} = 0 \qquad (3-3)$$

In this equation I define:

$$\alpha = \frac{R_s + R_l}{2R_s R_l C_l} = \frac{1}{2C_l(R_l || R_s)}, \qquad \omega^2 = \frac{1}{R_l R_s C_l C} \qquad (3-4)$$

The solution of (3-4) is:

$$V(t) = k_1 e^{s_1 t} + k_2 e^{s_2 t} \qquad (3-5)$$

$$S_{1,2} = \frac{1}{\tau_{1,2}} = -\alpha \pm \sqrt{\alpha^2 - \omega^2} \qquad (3-6)$$

Note that, I am not interested in solving (3-5), however the characteristic of the voltage drop is of interest. C_l is of the order of Femtofarad (10^{-15}) and (R_s+R_l) is of the order of Megaohm (10^{+6}). Therefore, $\alpha^2 >> \omega^2$, so I have:

$$\sqrt{\alpha^2 - \omega^2} \cong \alpha - \delta, \quad \alpha \gg \delta \qquad (3-7)$$

$$S_1 \cong -2\alpha, \qquad S_2 \cong -\delta \qquad (3-8)$$

Interestingly, the time constant of the voltage drop at the beginning ($1/S_1$) is due to charging the parasitic capacitor (C_l) through a parallel equivalent of the switching and leakage resistors (R_l and R_s). The voltage drop with this time constant persists so

electrical charge among capacitors (C and C_l) becomes apportioned according to their sizes. Charge equilibrium occurs at:

$$V_1 = V_0 \frac{C}{C + C_l}, \quad K = \frac{C}{C + C_l} \qquad (3-9)$$

K is the coefficient of decaying voltage at each switching action. Since $C>>C_l$, K is only slightly less than one.

3.2.2 Switching Index

The previous section presented a circuit model that approximates my target system as an *RC* circuit with charge sharing between a set of capacitors, which dynamically switch from one configuration to another. For one particular stage of charging and discharging the above equations give an approximate solution to the charge distribution condition. This section will move one level of abstraction up and will consider the overall dynamic switching process in the system. This process will consist of the previously described stages or cycles as elementary switching steps that can be characterized by their voltage drops with the rate of K and delays whose value will be determined by the current voltage level. My goal here is to derive an equation that will characterize the value of voltage V as a function of time, bearing in mind that I am now talking about the time which it takes to perform an entire sequence of cycles (I will call it "global physical time") rather than time during a single cycle exponential curve in previous section. Will this also be an exponential curve in global time?

To perform such a derivation as a brute force, i.e. trying to express V as a function of time directly, would require solving many iterations of the ODE with changing *RC* parameters. Instead, I will follow a different approach which will be based on selecting some form of a generator function that will act as an intermediate parameter between

voltage V and global time t. This generator will be the index of a switching cycle as the following analysis shows.

Suppose that operation starts at $t=0$ and $V=V_0$ and the circuit is in state 1 (Figure 3-4). Switching is started by a fast transition to either state 2 or 3. Let's assume that switching begins by a fast transition to state 2. I have mentioned earlier that the only important state in terms of discharge of C is state 3. According to Figure 3-6, in state 3, voltage drops exponentially from initial voltage to where the charge equilibrium occurs. After this point, the circuit cycles around states 1 and 2 and starts state 3 again. The new initial voltage at the start of each switching action is a factor of K than the initial voltage of the previous switching action. Therefore, the voltage step magnitude decreases K times after each switching of two adjacent inverters. Suppose n number of switchings occurs (n in Figure 3-6 is a switching index) and the voltage magnitude reaches:

$$V = K^n V_0 \qquad (3-10)$$

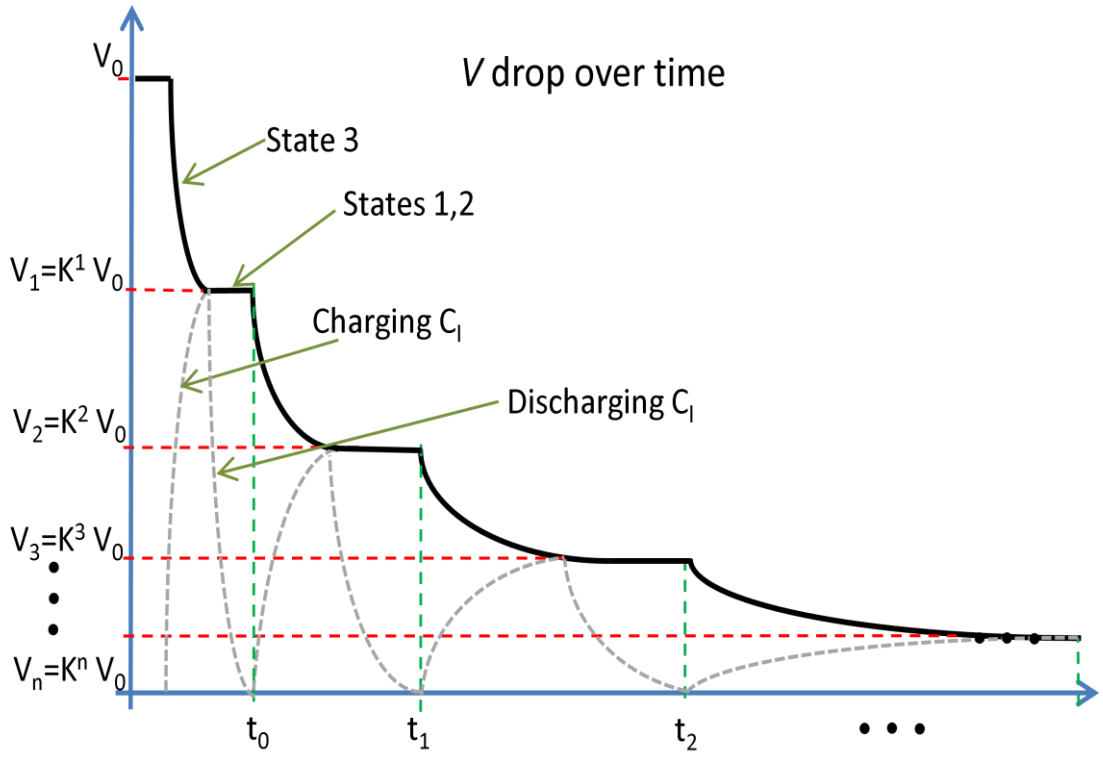


Figure 3-6 Voltage drop over time

Since K is less than one, V becomes a descending exponential function of the switching index. And, if I normalize the voltage to its initial value (V_0), I have:

$$V_N = K^n \qquad (3-11)$$

The time which takes the circuit to cycle around states 1, 2 and 3 is:

$$t_s = t_{p2} + t_{p3}, \quad t_{p1} \cong 0 \qquad (3-12)$$

In this equation, t_p is the time of a single switching action, which is in fact the *propagation delay of an inverter* (t_p). Note that, since K is only slightly less than one, I assume that t_s is almost constant during each cycle. As it is shown in Figure 3-6, the time of charging and discharging C_l within t_s is considered approximately the same

(there is a small difference between the resistances of NMOS and PMOS which I neglect), so I have:

$$t_{p2} = t_{p3} = t_p \;\; => \;\; t_{cycle} = 2t_p \qquad (3-13)$$

The propagation delay of an inverter, which is a function of the transistor behavior, however stretches over (global) physical time *t* with every increment of the switching index. For operation above transistor threshold (super-threshold region), the time of switching (propagation delay) is approximately inversely proportional to *V*. However, below threshold (subthreshold region), the propagation delay becomes a complex function of *V*. The following is a model for the propagation delay of a single inverter proposed by [76]:

$$t_p = \begin{cases} t_{super-V_{th}} = \dfrac{pC_lV}{(V-V_{th})^{\gamma}}, & V_{dd} > V_{th} \\ t_{sub-V_{th}} = \dfrac{pC_lV}{I_0 e^{\frac{V-V_{th}}{N_s}}}, & 0 < V_{dd} \le V_{th} \end{cases} \qquad (3-14)$$

I_0 is the drain current when the V_{gs} is V_{th}, γ is the velocity saturation index between 1.3 and 2 (for α =2 I have pure inverse proportionality), N_s is mkT/q (*m* is the sub-threshold slope factor, $1/N_s \approx 28$) [77], C_l is the parasitic capacitor and *p* is the fitting parameter.

3.2.3 Solution for super-threshold

Consider the case where *V* is greater than V_{th} so, the propagation delay (t_p) becomes inversely proportional to *V* (assuming γ=2). In order to simplify the analysis, I tabulate t_s and V_N (normalised of V_n) as a function of the switching index in Table 3-1. In this table, *physical time (t)* is the cumulative (global) time which takes to discharge C_s to a certain level corresponding to the current switching index value, and $2 \cdot p \cdot C_l$ is simply called *A*. This time is in fact the accumulation of the propagation delay at each switching. So, for the index equal to *n* I can write:

$$t = \sum_{i=0}^{n-1} \frac{A}{K^i} = \frac{A}{K^0} + \frac{A}{K^1} + \frac{A}{K^2} + \cdots + \frac{A}{K^{n-1}} =$$

$$A\left(\frac{K^{n-1}}{K^{n-1}} + \frac{K^{n-2}}{K^{n-1}} + \cdots + \frac{K^0}{K^{n-1}}\right)$$

$$= \frac{A}{K^{n-1}} \sum_{i=0}^{n-1} K^i \qquad (3-15)$$

This adds up all the time intervals t_s that precede n and represents the total time spent on the first n switching events.

I know that $K<1$, so I have finally the sum of geometric progression:

$$t = \frac{A}{K^{n-1}} \frac{1-K^n}{1-K} = \frac{AK}{K^n} \frac{1-K^n}{1-K} \qquad (3-16)$$

And if consider that after the n-th switching event $V_N=K^n$ I can substitute it into (3-16) and obtain:

$$t = \frac{AK(1-V_N)}{V_N(1-K)}$$

Hence:

$$V_N = \frac{AK}{t(1-K)+AK} = \frac{1}{at+1} \qquad (3-17)$$

Here, I denoted $a = \frac{(1-K)}{AK}$.

This equation, which is a convenient approximation obtained by a simple analytical derivation, shows that the voltage drop in the super-threshold region is a *hyperbolic function with respect to time*. As it is seen in Figure 3-7, if a super capacitor is used as C_s, K becomes practically near one and as a result, V_N becomes near one ($V\sim=V_0$). The

general and more accurate form of V_N can be obtained by employing the t_p model from (3-14):

$$t_p = \frac{AV_N}{(V_N - V_{THN})^\gamma} => t$$

$$= A\sum_{i=0}^{n} \frac{K^i}{(K^i - V_{THN})^\gamma} \qquad (3-18)$$

Note that V_{THN} stands for V_{th} normalized by V_0. Simple solution to (3-18) is to convert series into integral ($i=0,n$):

$$\int \frac{AK^i}{(K^i - V_{THN})^\gamma} di$$

$$= \frac{A(K^i - V_{THN})^{1-\gamma}}{ln\, K - \gamma\, ln\, K} \Big|_{i=0}^{i=n} \qquad (3-19)$$

Assume I have $\gamma=1.3$ (as a more realistic case for CMOS logic), so I have:

$$V_N = V_{THN} + (\frac{-{}^{10}/_{3}\, A}{ln\, K\, (t - BA)})^{3.333}, B$$

$$= \frac{{}^{10}/_{3}}{ln\, K(1 - V_{THN})^{0.3}} \qquad (3-20)$$

This equation has been plotted in Figure 3-8 against the simulation result. Regardless of the physical parameters, the trend of the voltage drop over time from (3-20) matches the curve from the simulation results. Considering meaningful values for physical parameters in order to plot (3-20), I assume $V_{th}=0.7V$, $K=0.99$ and A, which is related to the size of the parasitic capacitor and saturated current [77], at the order of 10^{-11}. Comparison shows that the maximum error between the simulation result and my analytical solution is around 4.6%.

Table 3-1 Analysis for super-threshold region

$switching\ index$	$V_N = K^n$	$t_s = \frac{A}{V}, (A = 2pC_l)$	$Physical\ time\ (t)$
0	K^0	$\frac{A}{K^0}$	$\frac{A}{K^0}$
1	K^1	$\frac{A}{K^1}$	$\frac{A}{K^0} + \frac{A}{K^1}$
2	K^2	$\frac{A}{K^2}$	$\frac{A}{K^0} + \frac{A}{K^1} + \frac{A}{K^2}$
⋮	⋮	⋮	⋮
n	K^n	$\frac{A}{K^n}$	$\sum_{i=0}^{n} \frac{A}{K^i}$

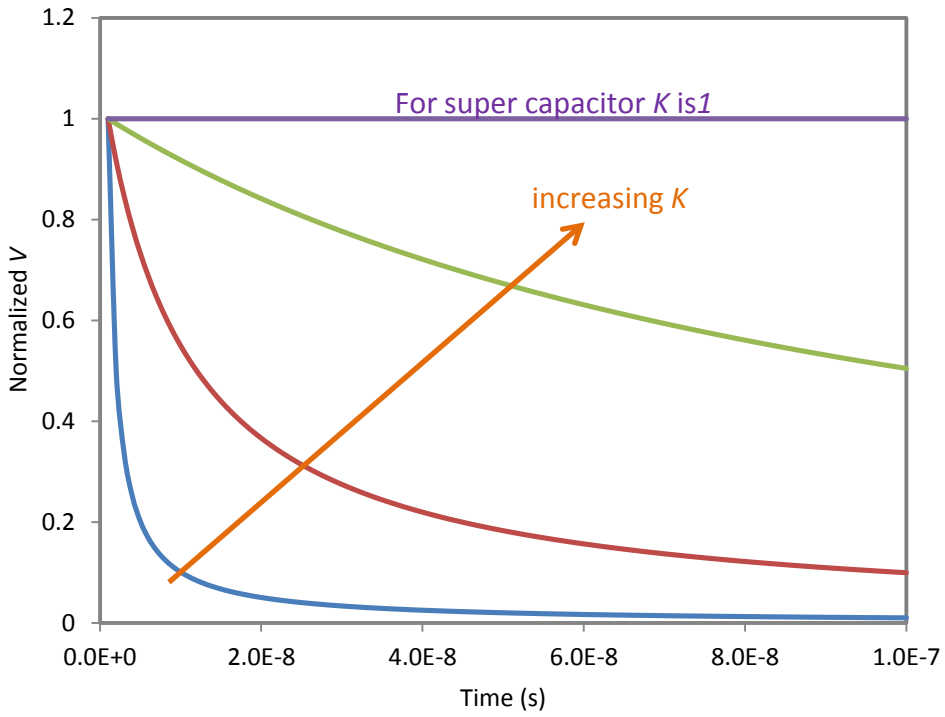


Figure 3-7 Simulation of voltage drop from equation (3-15) with respect to K. For Cs as supercapacitor K is the one. Suppercapacitors offer high value of capacitance compare to the conventional capacitors.

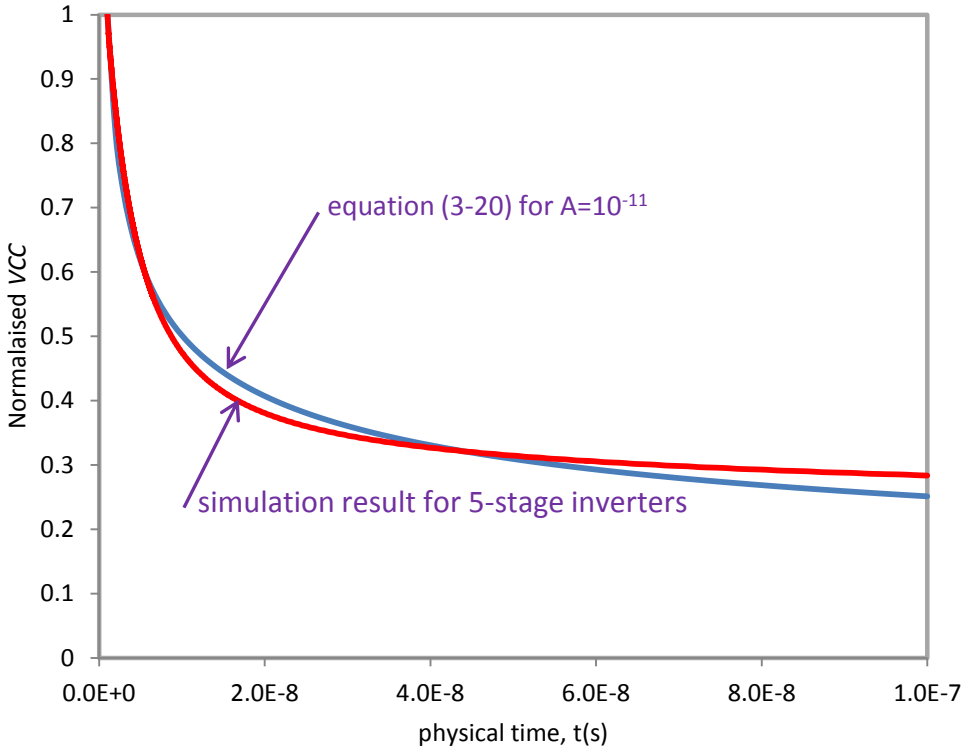


Figure 3-8 Voltage drop at super-threshold region, general form. The equation (3-20) was plotted using Matlab and the simulation results was captured using 180nm UMC library running Cadence tool.

3.2.4 Solution for sub-threshold

In the subthreshold region, due to exponential relationship between the drain current and *V*, the propagation delay becomes a complex function of voltage. In this region I have (from 3-14):

$$t_p = \frac{C_l V}{I_0 e^{\frac{V-V_{TH}}{N_s}}} = A\frac{V}{e^{D(V-V_{th})}} \quad , \quad D = \frac{1}{N_s} \qquad (3-21)$$

Note that, *A* in this equation is a parasitic capacitance (in order of 10^{-15}) over the saturated current (in order of 10^{-6}). In the same way as super-threshold, *V* is normalized

to its initial value which is V_{TH} for this region. Table 3-2 contains V_N and t_p as functions of n for sub-threshold. Using this table, the physical time is given by (i=0,n):

$$t = A \int K^i e^{D(1-K^i)} di$$

$$= -A \frac{e^{D(1-K^i)}}{D \ln K} \Big|_{i=0}^{i=n} \qquad (3-22)$$

After solving this integral and applying the limits, I have:

$$V_N = 1 - \frac{ln(1 - \frac{Dt \ln K}{A})}{D} \qquad (3-23)$$

This equation is plotted against the simulation result in Figure 3-9. The result shows that the maximal deviation of my analytical solution from simulation is around 5.4%.

In this analysis, an intermediate factor, called a switching index, was introduced to simplify the process of deriving the important relationship between the voltage on the capacitor V and time. Notably, both time and voltage of the power supply of the circuit are thus quantized according to the switching index, rather than using a fixed time discretization step as often happens in numerical analyses of circuits. Voltage is dropping exponentially and time is stretched as a complex function of energy. In consequence, the overall time is obtained by accumulating the intervals of switching in the form of generating functions. Solving these functions provides analytical solutions which express voltage as a function of time.

Table 3-2 Analysis for sub-threshold region

$switching\ index$	V_N	$t_s\ ,(A = 2C_l/I_0)$	$Physical\ time\ (t)$
0	K^0	A	A
1	K^1	$AKe^{D(1-K)}$	$A + AKe^{D(1-K)}$
2	K^2	$AK^2e^{D(1-K^2)}$	$A + AKe^{D(1-K)} + AK^2e^{D(1-K^2)}$
⋮	⋮	⋮	⋮
n	K^n	$AK^ne^{D(1-K^n)}$	$A\sum_{i=0}^{n} K^ie^{D(1-K^i)}$

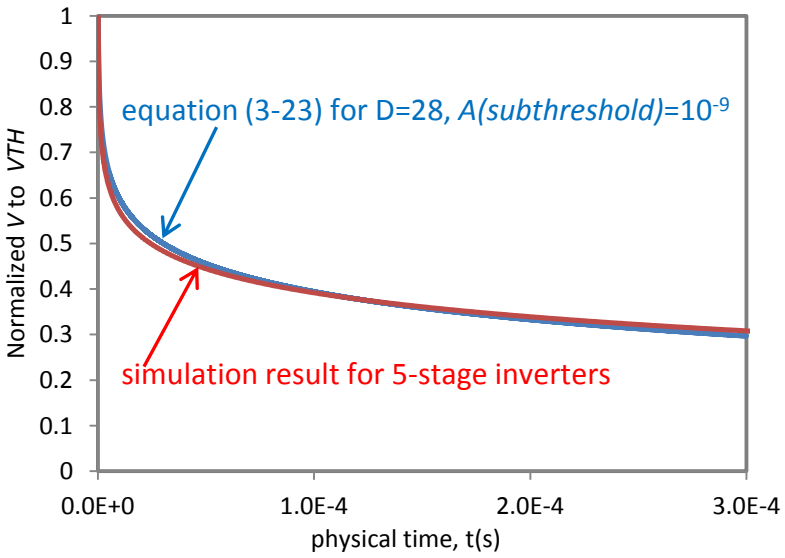


Figure 3-9 Voltage drop at sub-threshold region

3.3 Asynchronous binary counter as the measurement tool

One candidate for a charge measuring device, or ruler, could be a self-timed linear shift register, in which I could shift a value 1 bit as a slider during the discharging process. While this might be a plausible approach the size of the shifter may be a problem for a sufficiently large capture range of the sensed values. Hence my preference falls on a self-timed (asynchronous) counter, in which the accumulated code could be standard

binary-weighted. This way the frequency of switching activity in the bits of the counter, from the least significant to most significant one, will be divided by two between each pair of bits, and I will be able to accommodate a large amount of switching activity in a compact form. It should be emphasized, however, that the requirement for switching actions to form a totally sequential series of logic gate transitions, in which there are NO transitions that are ineffective (such as those done in parallel or as glitches), is absolutely fundamental for the proportionality between the charge and the code. Needless to add, another reason for having the counter built as a self-timed circuit is that it should operate correctly and smoothly from the voltage supply that varies in time (as the capacitor is being discharged). These requirements have led us to the idea of using a speed-independent sequential counter.

3.3.1 Asynchronous counter using Toggle Logic

The binary counter is built from toggle logic blocks, each toggle working as a data bit. An *n*-bit counter needs *n* toggle blocks. In such a binary counter each bit should toggle twice as much as the bit in the next stage. Signals among the logic blocks are connected in such a way as to provide the binary code in the bits with progressively increasing weights (as powers of *2*). As it is shown in Figure 3-12 one approach is to apply the Acknowledgement (*Ack*) signal from next stage to the feedback (*Fee*) path instead of $\overline{Y}$ and use the inverted version of $\overline{Y}$ to reset the bit in the next stage.

In line with [78] the toggle logic uses flip-flops to generate Y and Q as shown in Figure 3-10. This figure pertains to a multi-bit structure in the form of Figure 3-12, with cross-bit $Ack - Fee$ and $\overline{Y}$ - Req connections. In a single-bit setup, Ack and Fee signals are connected to the local *Req* and $\overline{Y}$. Changes in the internal state ($X, \bar{X}$) make transitions on the request signal, *Req*, to reset Y and $\bar{Y}$. Feedback paths send Y and $\bar{Y}$ to

the back-end flip-flop, which modifies the state of the internal stage to trigger another count (toggle). The toggling continues when there is enough V_{dd} to drive the circuit.

The signal transition graph (STG) [78] which describes the cyclic behaviour of the toggle circuit is shown in Figure 3-11. It illustrates the transitions of signals at each individual cycle for the asynchronous toggle circuit described in Figure 3-10 under single-bit connection assumptions. Suppose the initial state of the graph is when $Q = 0$, $\bar{Q} = 1, Req = 0, Y = 1$ and $\bar{Y} = 1$. The outputs $[Y, \bar{Y}]$ are toggling when traversing the *STG*.

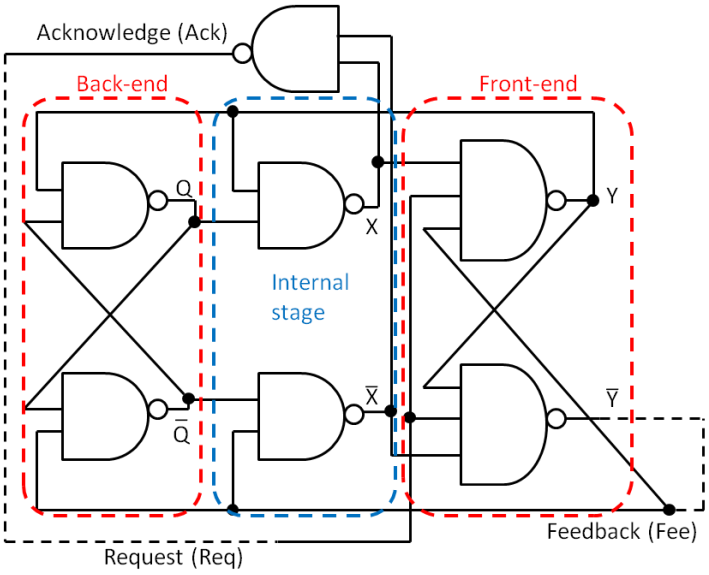


Figure 3-10 Schematic of an asynchronous toggle circuit which is the basic building block for the charge-to-digital converter.

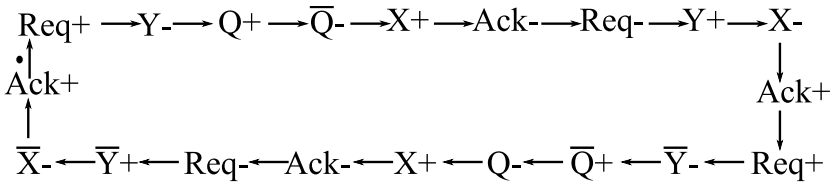


Figure 3-11 Signal Transition Graph (STG) describing the toggle circuit.

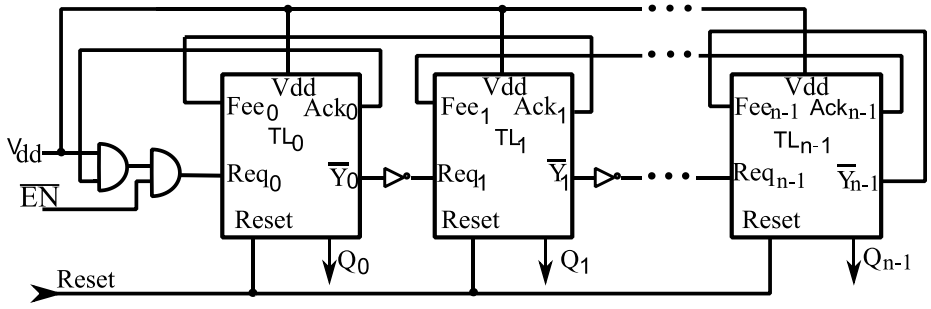


Figure 3-12 A general n-bit asynchronous counter based on toggle logic. This counter serves the charge-to-digital purpose in a sensor application, if the input is connected to a sampling capacitor.

This asynchronous counter acts as both an oscillator and an encoder, thereby combining the two main functionalities in one circuit: converting power (i.e. the V_{dd} value) to frequency and integrating frequency to code. It is crucial that every signal transition of every logic gate in this asynchronous counter (as can be seen from the above STG) contributes to the formation of the output code from the sensor, and each such transition consumes a certain portion of energy taken from the capacitor. As the entire counter is a speed-independent circuit (hazard-free), its logical behavior as specified by the STG in Figure 3-11 remains invariant to the changing of V_{dd}. The voltage dropping over time is shown in Figure 3-13. In this work, I have implemented all my circuits in a 180nm technology and all quantitative results are from analogue simulations using Spectre in the Cadence toolset.

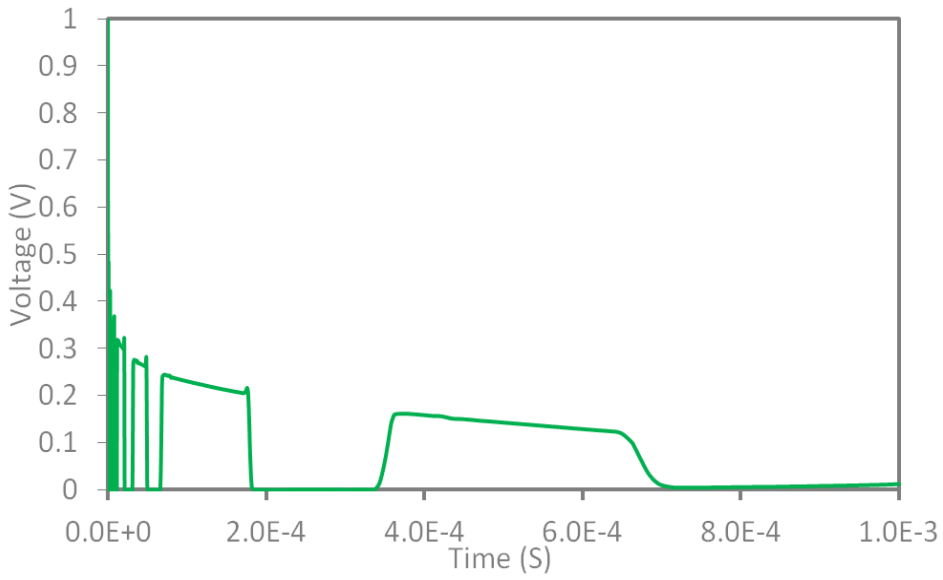


Figure 3-13 LSB bit of the counter while the capacitor charge is decreasing and the voltage on the counter is degrading.

3.3.2 Switching activity vs. count (code)

In this section the proportionality between the switching activity (number of gate transitions) and output count is analyzed. First I study a full counter cycle or counting to 2^n in an *n*-bit counter. The number of transitions for counting to 2^n is:

$$NT(2^n) = \sum_{i=0}^{n-1} [NT(C_i{}^+) + NT(C_i{}^-)] \qquad (3-24)$$

$NT(C_i{}^+)$ is the total number of logic gate transitions pertaining to bit *i* flipping from 0 to 1. Similarly $NT(C_i{}^-)$ is the total number of gate transitions when bit *i* flips from 1 to 0.

Table 3-3 Conversion from binary code to cumulative code

Count	Cumulative code (C_i^+, C_i^-)			Binary Code		
0	0(0,0)	0(0,0)	0(0,0)	0	0	0
1	1(1,0)	0(0,0)	0(0,0)	1	0	0
2	2(1,1)	1(1,0)	0(0,0)	0	1	0
3	3(2,1)	1(1,0)	0(0,0)	1	1	0
4	4(2,2)	2(1,1)	1(1,0)	0	0	1
5	5(3,2)	2(1,1)	1(1,0)	1	0	1

Table 3-3 shows the value of the count in the form of binary and cumulative code for values from 0 to 5. The cumulative code shows the number of transitions quantitatively and which can be directly related to energy consumption.

In this section, the aim is to derive the relationship between the count and the number of transitions in the counter. By exploring the switching behavior of my *n*-bit toggle counter, this relationship can be obtained for each value of count. For example for counting to 2 (fully cycling an *n=1* counter) I have: $2 = 2^1 : 6T_3 + 18T_2 + 2T_1 = 26$, where T_3 denotes the transition in a 3-input NAND gate, T_2 the transition in a 2-input NAND gate and T_1 the transition in an inverter. This equation shows that for counting to 2, 26 transitions occur in the counter (all bit flippings from 1 to 0 and vice-versa contribute to this number of transitions). Based on these results, for the number of transitions (*NT*) I can write (for counting to 2^n):

$$NT(2^n) = 2^n(6T_2 + 2T_3) + \sum_{i=0}^{n-1} 2^i(6T_2 + 2T_3 + 2T_1) \quad (3-25)$$

Equation (3-25) can be simplified by normalizing to transitions in inverters. A realistic assumption is $T_3 = 3T_1,\ T_2 = 2T_1$ in terms of energy consumption. Based on this I rewrite (3-26) as:

$$NT(2^n) = 2^n 18 + \sum_{i=0}^{n-1} (2^i)20 = 38\,2^n - 20 \qquad (3-26)$$

Any arbitrary non-negative integer value of count (not necessarily powers of 2) can be expressed in binary form:

$$Count = \sum_{i=0}^{n-1} b_i 2^i\ , \forall\ b_i\ \epsilon\{0,1\} \qquad (3-27)$$

Where b_i=0 or 1 corresponds to the i^{th} bit of the binary value of *Count*. The number of transitions for each value of count (*NT* (*Count*)) is an aggregation of the number of transitions for each term in (3-24). In other words, each b_i=1 contributes a counting up to 2^i to the overall counting up to *Count* and each b_i=0 contributes nothing.

The total number of transitions for any value of count is:

$$NT(Count) = \sum_{i=0}^{n-1} b_i NT(2^i) \qquad (3-28)$$

By substituting (3-26) into (3-28), I have:

$$NT(Count) = 38\sum_{i=0}^{n-1} b_i 2^i - 20\sum_{i=0}^{n-1} b_i \qquad (3-29)$$

Figure 3-14 shows an almost proportional relationship between the value of count generated by the counter and the number of gate transitions (switching activity) required to complete the corresponding counts according to (3-29).

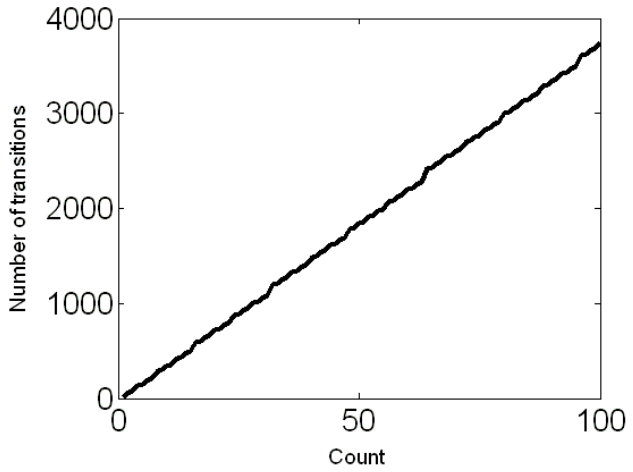


Figure 3-14 The relationship between the output count of the counter and the number of gate transitions according to (3-29).

3.3.3 Switching activity vs. input energy

According to the configuration of my proposed sensing method, V is sampled into C_s. (I remind that the energy stored in C_s is a squared function of the input voltage.) In this analysis I model C_s and its load, which is the counter, as an RC circuit. However, it should be noted that due to the properties of the load, being a switching circuit with varying voltage supply, its impedance R is not constant but a non-trivial function of V. For C it is reasonable to consider C_s. In (3-20) and (3-23) I have shown that voltage drop is a complex function of time (t), so:

$$V_{dd} = F_1(t) \qquad (3-30)$$

Figure 3-15 shows the simulation result of how the voltage (V) on the C_s drops when the counter is operating. In the counter, due to its fully sequential operation, the frequency of switching activity (gate transitions) is inversely proportional to the gate delay and it is known [76] that the propagation delay is a non-trivial function of V , therefore the rate or frequency of the gate transitions becomes a function of V:

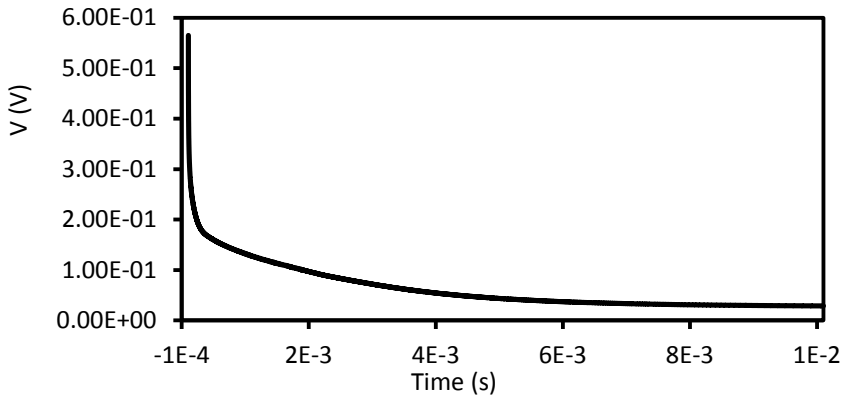


Figure 3-15 Voltage drop as a function of time for counter as load.

$$\begin{cases} f = {}^{1}/_{t_p} \\ t_p = G(V) \end{cases} => f = F_2(V) \qquad (3-31)$$

From (3-30) and (3-31), I find that the gate transition frequency is a complex superposition with respect to time, which is also shown in Figure 3-16. Thus, to find the number of gate transitions over the range of voltage (V) drop at each sensing round (t_f is the required time that the counter finishes counting):

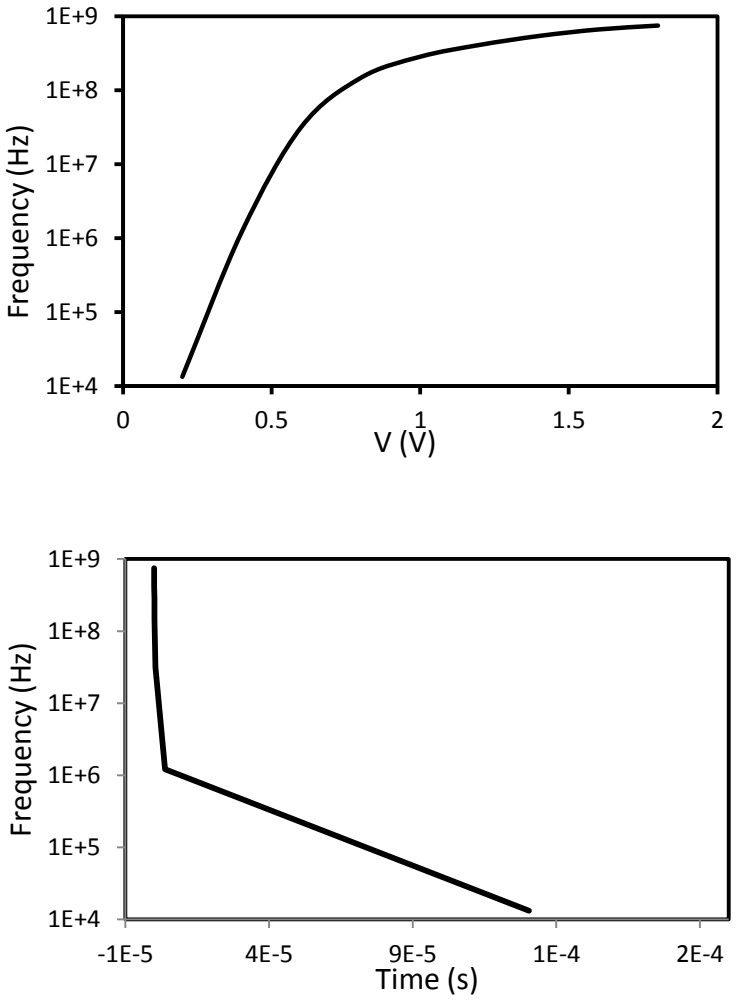


Figure 3-16 Frequency as function of voltage and time of discharging.

$$Number\ of\ transitions = \int_0^{t_f} f dt$$

$$= \int_0^{t_f} f\left(F_2\left(F_1(t)\right)\right) dt \qquad (3-32)$$

From (3-32) I come to the point that the number of gate transitions is related to the frequency at which the counter operates and, on the other hand, that the frequency is a function of *V* (or, in other words, the energy sampled into the capacitor). Besides that, the previous sub-section showed a proportional relationship between the output count (code) and the switching activity in the counter. It is crucial that every signal transition in the asynchronous counter contributes to the formation of the output code from the

sensor, and each such transition consumes a certain quantum of energy taken from the capacitor. Thus, the switching activity and output of the counter virtually becomes nonlinearly proportional to the input energy 'invested' into this computation.

3.4 Summery

The main aims in this chapter are to: 1) Investigate the operation of a digital switching circuit upon procurement of power by a pre-charged capacitor, and 2) a switching circuit with minimal complexity which can quantify in the form of a digital code the charge stored in a capacitor. In addressing these objectives, the first section of the chapter embarks into exploring the relationship between the switching behaviour of a ring oscillator and voltage dropping while the power procurement of the circuit is attained by a capacitor. The analysis was contacted over two operational regions characterized as super and sub-threshold. The maximum discrepancy between analytical and experimental results was 4.6% for the super-threshold case and 5.4% for sub-threshold region of operation. In a subsequent section, an asynchronous counter was designed and its functional efficacy was assessed as a candidate to be used in sensing. Conceptually in the design of a sensor to materialize the charge-to-digital conversion, the task for the counter is to convert the charge of a capacitor to a digital code. My proposed asynchronous counter can be utilized as both an oscillator and an encoder, thereby encompassing the two main functions in a single circuit: Its operation is comprised of conversion of power (i.e. the V_{dd} value) to frequency and integration of frequency to encoded information. Detailed exploration of the functional characteristics of the counter reveals that every signal transition in the counter contributes to the formation of its output code. A possible obstacle in incorporating this counter is the existing nonlinearity in its power relation, attributable to the fact that the operation occurs in the deep sub-threshold region. Such nonlinearity is yet acceptable within the

context of designing a sensor to operate within the energy harvesting environment. Therefore, this counter exhibits the required properties that are desirable in a switching circuit to be utilized as a converter of charge to digital code.

Chapter 4. Design and implementation of the Reference-free voltage sensor

4.1 Voltage sensor implementation

This chapter describes the implementation of the voltage sensor according to the sensing technique detailed in the previous chapter. First I detail the implementation of the sensor with timing reference. Then the reference free implementation of the proposed sensor is delivered.

4.1.1 Voltage sensor with timing reference

Figure 4-1 shows a general architecture of the proposed voltage sensor circuit. A sensing round starts with the charging of the sampling capacitor from the V_{dd} being sensed. The resulting amount of charge on this capacitor is uniformly related to the V_{dd}. The capacitor is then discharged for some time by using the energy in its charge to perform some quantifiable work. The amount of work completed reflects the sampled charge (and thus the V_{dd} value at the time of sampling). In this design, my asynchronous counter, designed in the previous chapter, counts the pulses generated by itself to record its amount of work.

The sampling circuit in Figure 4-1 works in two states. In the first or charging state S_1 is on and S_2 is off. C_{sample} is charged to V_{dd}-V_{s1}, where V_{s1} is the voltage drop across S_1. This state should be long enough to fully charge the sampling capacitor ($t_{charging}$). In the second or conversion state ($t_{conversion}$) S_1 is off and S_2 is on. In this state V_{in}, which is V_{dd}-V_{s1}-V_{s2} where V_{s2} is the voltage drop across S_2, is applied to the counter. In this design S_3 is used to bypass the sampling circuit at the end of the conversion time. At

this time, the counter stops counting and latches the output. Not shown in the figure, the end of conversion should also fully discharge C_{sample} readying it for the next sensing round.

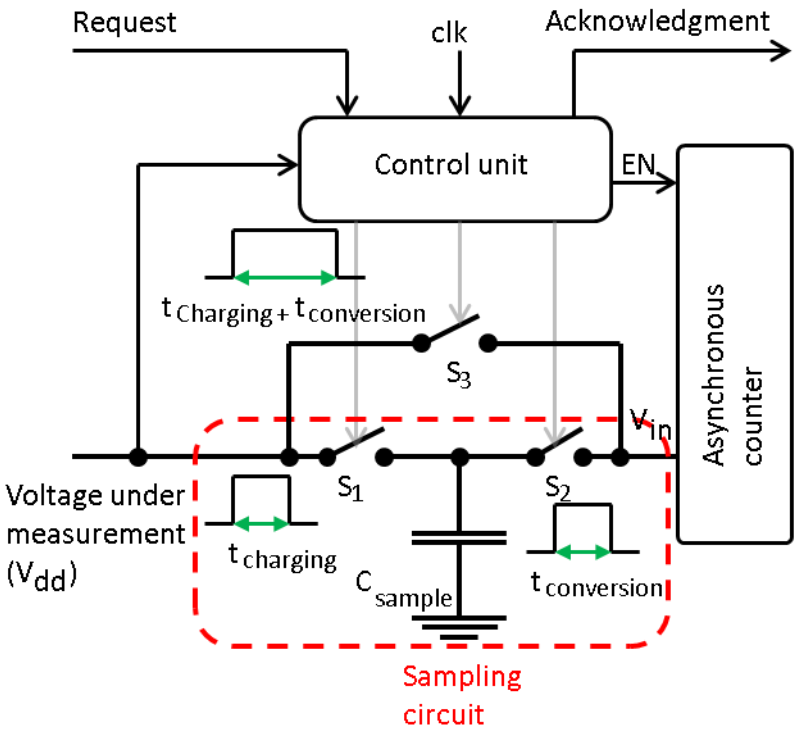


Figure 4-1 General architecture of the proposed sensor with timing reference.

4.1.2 Sensor operation

From Figure 4-1 it can be seen that the sensor operation consists of three separate sub-operations: (*i*) charge the sampling capacitor (charging), (*ii*) run the counter using the charge stored in the sampling capacitor to generate the digital output code (conversion) and (*iii*) bypass the sampling circuit, stop the counter and latch the outputs (output). Figure 4-2 shows the outputs of the counter during these sub-operations when the stop signal is arbitrarily issued 4µs after charging stage by the controller just to show the operation of the sensor. The flip-flop structure of the counter makes it straightforward to

latch the outputs when the counter is stopped. With the capacitor used (12pf) the charging stage is very short, almost invisible in the Figure 4-2.

Figure 4-3 depicts the value of the output count for three different sampling capacitor values with three different output time choices ($T = t_{charging} + t_{conversion}$) over a range of voltages ($V_{dd} = [0, 1]$). This figure shows two slightly different slopes on each individual curve. The reason is that dramatic decrease in on to off currents (I_{on}/I_{off}) in subthreshold region changes the delay property of the circuit [60].

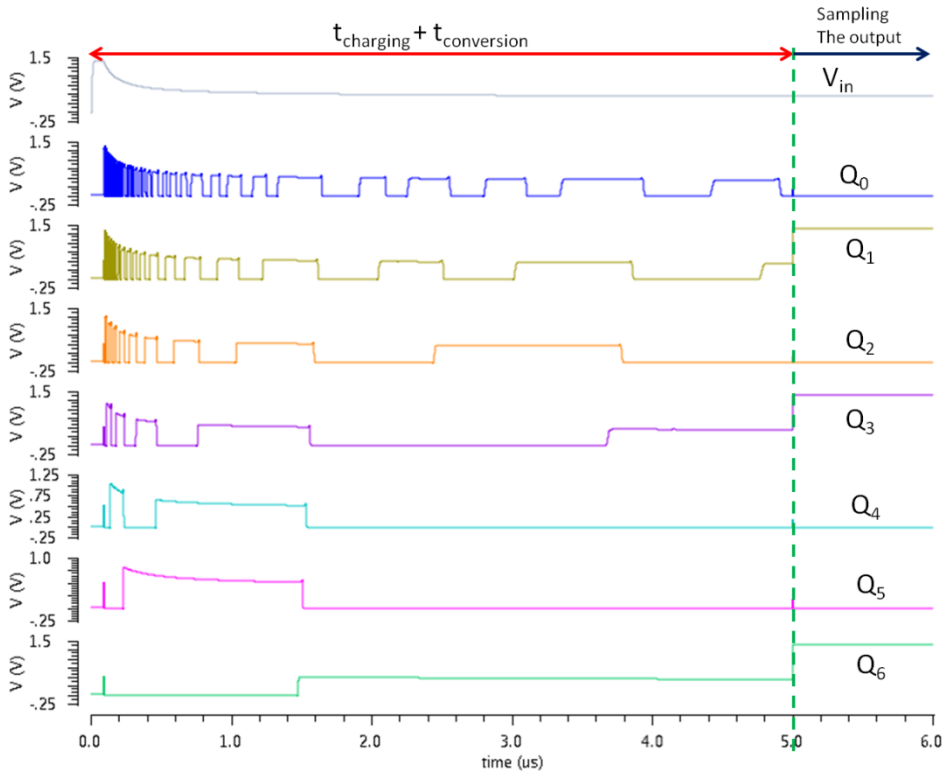


Figure 4-2 The general architecture of the proposed sensor (with reference) was simulated using 180nm UMC library. In this figure the counter output during one complete cycle of conversion is shown.

The range of output code (and thus measuring resolution) depends on the value of the sampling capacitor. Using bigger capacitors provides more energy at each V_{dd} and higher measuring resolution. There is a trade-off between sensor resolution and energy

consumption as larger sampling capacitor means higher energy used in the sensing. The latency of capacitor charging is minor, and there is little latency-resolution trade-off in the charging process.

Conversion time plays an important role on measuring resolution. Early stopping of the counter can lead to small output range and, if combined with low V_{dd}, lower resolution outputs. The latency-resolution trade-off is the main factor for conversion time selection.

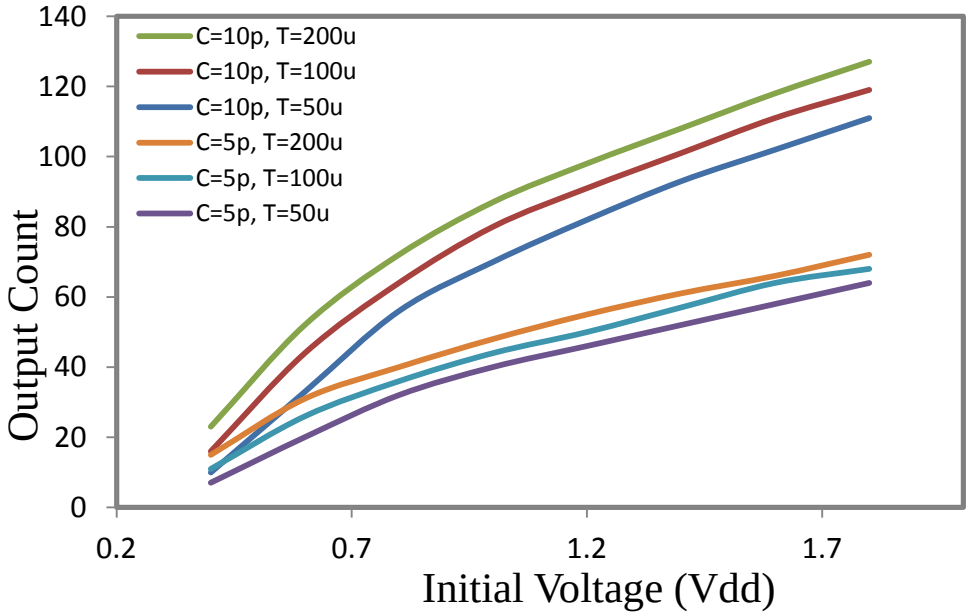


Figure 4-3 The output count versus input voltage for two different values of capacitor and three different time lengths of sampling and conversion.

The value of resolution can be captured by dividing the range of measured voltage over the range of code [79]. Therefore, taking the data from Figure 4-3, the resolution of measurement for C=10p and C=5p are 11 mV per LSB and 19 mV per LSB respectively. The smaller the V/LSB the higher the resolution therefore, the measurement using

C=10p gives higher resolution than C=5p. In normal ADC operation, the high resolution conversion is usually considered to deliver higher precision results [79].

It is clear that the value of count increases uniformly with the sensed V_{dd}. For voltage sensors, the requirement for linearity in this relationship is not as strong as for conventional ADC solutions. Voltage sensors are envisaged to be used by on-chip control whose actions are relatively coarse grain (fine-grain, high precision control tends to be power consuming and not suitable for this context) and the voltage sensor needs only be able to provide information on the trend of variance and reasonable estimates of voltage. In addition, voltage sensors may be thoroughly characterized at design time or even calibrated after chip implementation, which would provide sufficient data for control algorithm design without needing to be truly linear.

4.2 Reference-free voltage sensor implementation

Figure 4-4 shows the general architecture of the proposed voltage sensor [80]. In this architecture a capacitor C_{sample} is used as the energy storage unit. Its operation is organized by the control unit using switches S_1 and S_2. My previously designed asynchronous counter is used as the computational unit which implements the measurement tool as described above. The sensing round starts by receiving the request signal from a power management unit or any other entity which requires information from the sensor. An example of such a unit can be seen in the next chapter. The control unit disconnects C_{sample} from the V_{dd0} being sensed (S_1 open) and connects it to the asynchronous counter (S_2 closed). It enables the counter to start counting for some time. In due course, it stops the counter and flips the switches (S_1 closed and S_2 open). The sensing round is finished by issuing the acknowledgment signal to the environment. The counter's eventual progress is the output code describing V_{dd0}.

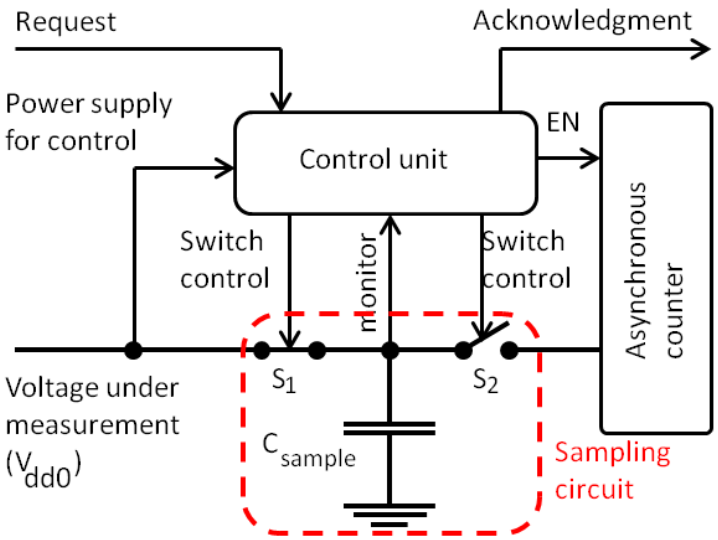


Figure 4-4 Voltage sensor that samples a charge from the main energy supply and stores it in a small capacitor. This capacitor's voltage will be used as V_{dd} input to the asynchronous counter circuit.

4.2.1 Control unit

It is assumed that between consecutive sensing operations C_{sample} is fully charged. Based on simulation, considering a 10pF sampling capacitor, the charging time is less than a microsecond. That means between two successive sensing operations at least 1 microsecond delay is required.

Figure 4-5 shows that in the absence of a controlling strategy the counter consumes all the energy stored in the capacitor and the counter dies with no code at the outputs. Consequently, a sophisticated controlling strategy is necessary to monitor the voltage drop on the capacitor and preserve the output code before the energy is used up. This part which is shown in Figure 4-6 consists of two units controlling and monitoring units. The monitoring unit is formed by a reference generator (RG) and an asynchronous dynamic comparator. The controlling unit governs the sampling circuit and the counter using the results of the monitoring unit.

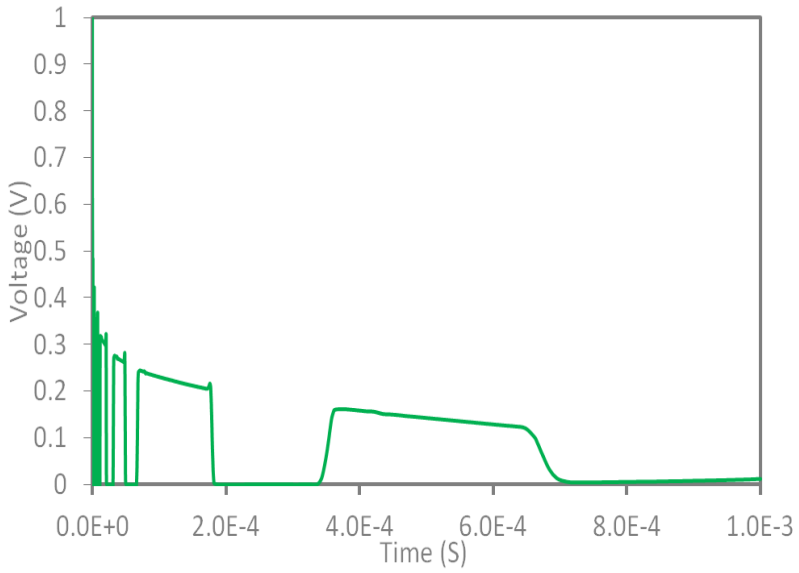


Figure 4-5 LSB bit of the counter while the capacitor charge is decreasing and the voltage on the counter is degrading. As it can be seen, the output of the counter degrade to zero.

Considering the voltage drop in Figure 4-5, it is necessary to generate an indicating pulse when the voltage (V_{dd}) reaches a designated level. This indicating voltage may be chosen to trade-off sensing resolution with sensing latency. The higher the indicating voltage is, the shorter the sensing delay will be, but the sensing precision will suffer. On the other hand, this pulse must be generated before the counter stops operating. Without stable external references, internal voltage references must somehow be generated. This could be based on such V_{dd}-independent characteristics as transistor thresholds but ideally should be tunable. A circuit which I call reference generator (RG) is designed to serve as such an indicator. Simulation results show that the minimum operating voltage for the counter is 140mV where it can still maintain its code. Although the monitoring and the controlling parts are fast, in order to avoid any trouble (e.g. incorrect measurement) from process variation especially at the *SS* corner I considered a safety margin and designed the RG circuit to generate the indication pulse around 170mV in my sample implementation. The counter operation is stopped at 170mV but for the

sensor to work, the original sensed V_{dd0} must be greater than this as Figure 4-8 shows a need for voltage to "fall down" to the 170mV threshold. I found that the starting point of this fall for reliable operation is from at least 250mV. Thus, the operating voltage for this sensor runs from 250mV to 1.8V.

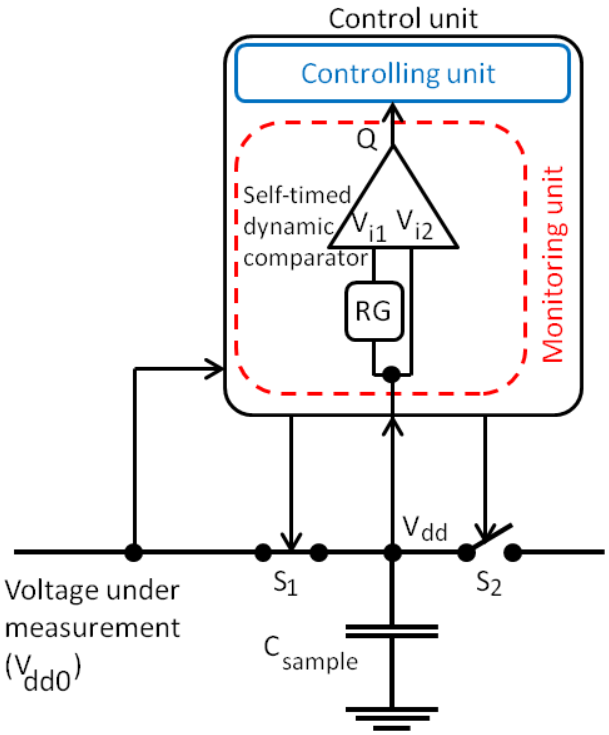


Figure 4-6 Monitoring and controlling units block diagram.

Figure 4-6 depicts the block diagram of the control unit in more detail. While the V_{dd} drops due to the counting action of the counter a comparator compares V_{dd} with the voltage at the output of the RG circuit. This comparator is supplied by the V_{dd0} shown in this figure. Prior to the indication pulse being generated by the RG circuit, *Vi2* is greater than *Vi1* at the input of the comparator. The comparator detects that and pushes *Q* to zero. This state is preserved till the indication pulse is generated. After that *Vi1* becomes greater than *Vi2* hence, the comparator sets the *Q* high. This rising edge on the *Q* signal is sensed by the controlling unit. This unit terminates the sensing process, stops the

counter and issues the acknowledgment signal. The circuits used in the control unit are detailed next.

4.2.2 Reference generator (RG)

As mentioned above, the lack of external references motivates an internal RG. The RG circuit used in this sensor is similar to the POR design proposed in [33]. It is shown in Figure 4-7. In this design input voltage (V_{dd}) is scaled down by a voltage divider (*P_Ref* and *N_Ref*) to form V_{ref}. The difference between V_{dd} and V_{ref} forms the source-gate (V_{sg}) voltage for *P_Buf*. Figure 4-8 shows the operation of the RG circuit in one single sensing round. At the start V_{dd} is V_{dd0}. When the sensing round is started V_{dd} begins to drop. Before the point called first threshold voltage in Figure 4-8, the current mirror and *P_Buf* are on. The resistance of *P_Buf* is sized to be smaller than that of *N_Buf* therefore V_{buf} is pulled up to V_{dd} and as a result, output voltage follows the V_{dd}. When V_{dd} drops further, V_{ref} goes down. V_{dd} - V_{ref}, which is V_{sg} for *P_Buf*, also becomes smaller. That makes *P_Buf* more off (the driving capability of *P_Buf* is reduced). Therefore, it doesn't pull up V_{buf} anymore. Instead, *N_Buf*, which is still on, pulls V_{buf} down to ground. With still more reductions of V_{dd}, *N_Buf* will be turned off. At this point (second threshold) *N_Buf* and *P_Buf* are both off but due to smaller size of *P_Buf* compared to *N_Buf*, V_{buf} is pulled up to V_{dd} again. This serves as the indication pulse which changes the state of the comparator.

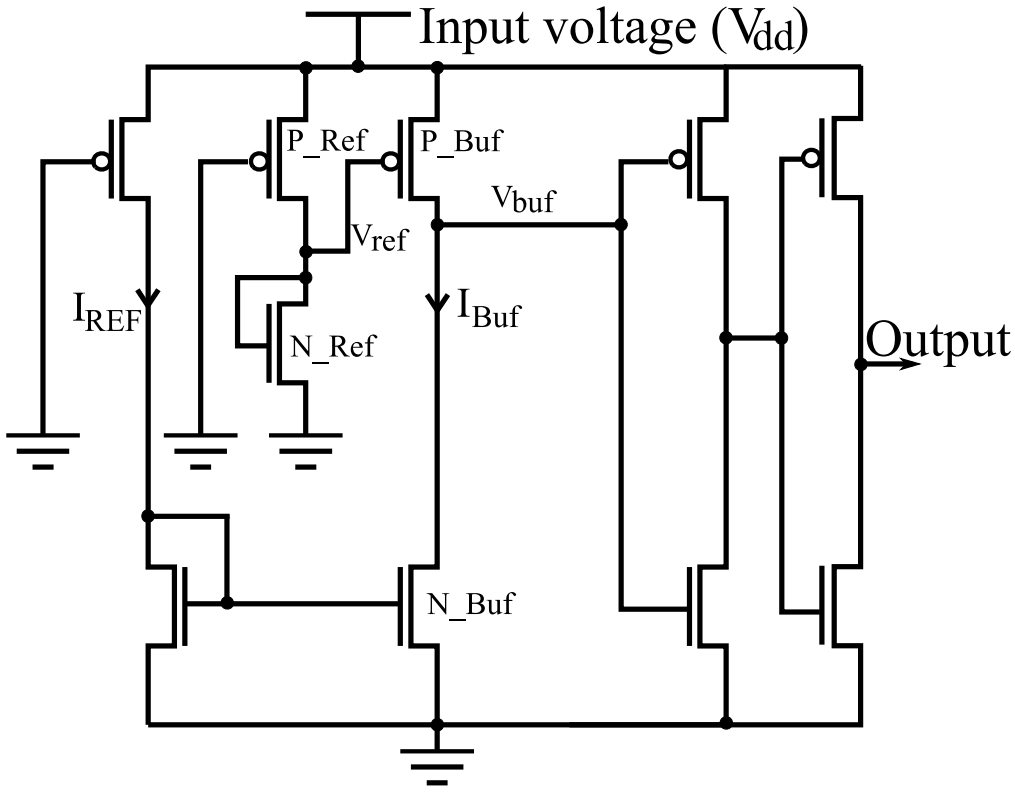


Figure 4-7 Schematic of reference generator.

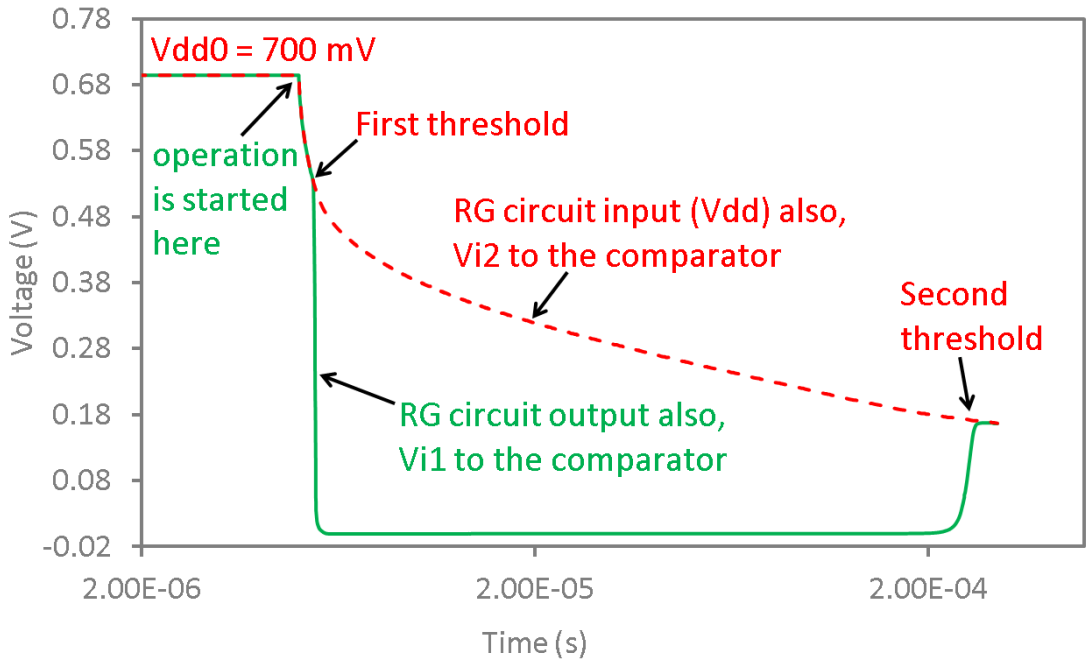


Figure 4-8 Simulation results on reference generator circuit using Cadence tools at 180nm technology process. At low Vdd0 operation is started after the first threshold.

The operation of this circuit is highly affected by the size of the transistors used in the design. For instance, varying the size of *P_Ref* and *N_Ref* can be used to change the time difference between the first and the second thresholds. That affects the response time of the sensor. Close thresholds decreases the response time. However, an early second threshold degrades the precision of the sensor.

4.2.3 Comparator

My design needs a comparator circuit to serve the control unit. The comparator used in this design is adapted from [63] and shown in Figure 4-9. In the absence of the *Clock* signal both outputs are held high. The comparator starts evaluation mode when *Clock* is pulsed high. Then, the difference between the input voltages resolves the competition between the cross-coupled latches. For instance, *Vi1* > *Vi2* then *Vo2* high and *Vo1* low, and vice versa.

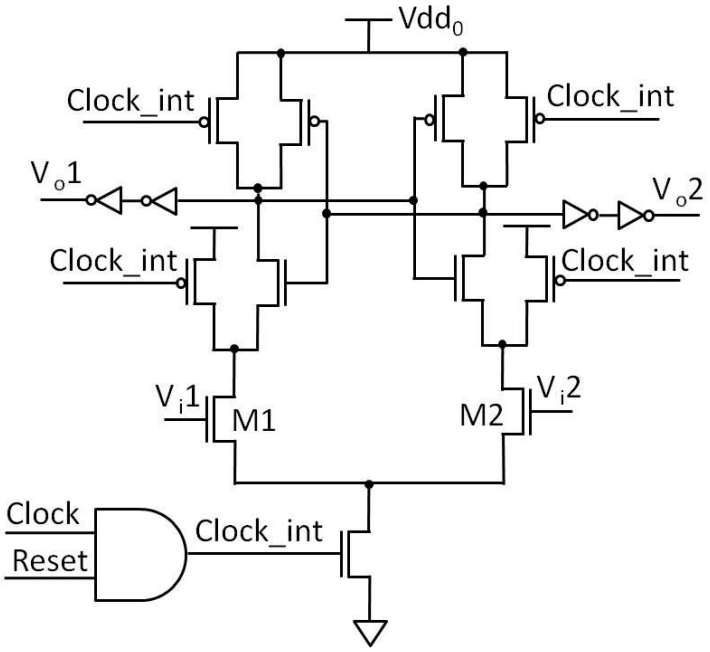


Figure 4-9 The comparator design used in the self-timed dynamic comparator.

In my particular case, the comparison situation is different. It is preferred to have *Vi1* to drive the output in case of equilibrium between the inputs. This situation happens before the first threshold and after the second threshold shown in Figure 4-8. For this purpose, *M1* is chosen to be bigger than *M2* in Figure 4-9. Through simulations, I realized that normally $W_{M1}=1.5\times W_{M2}$ (W_{M1} and W_{M2} are the widths of *M1* and *M2* respectively) can guarantee the robust operation at all process corners and temperature variation within the range of 0º up to 100º. At lower temperatures (e.g. -20º), $W_{M1}=3\times W_{M2}$ is required. A digital comparator, such as the one used in this design, needs a clock to trigger repeated rounds of comparison. My design requirements do not allow external clocks and this problem must be solved internally.

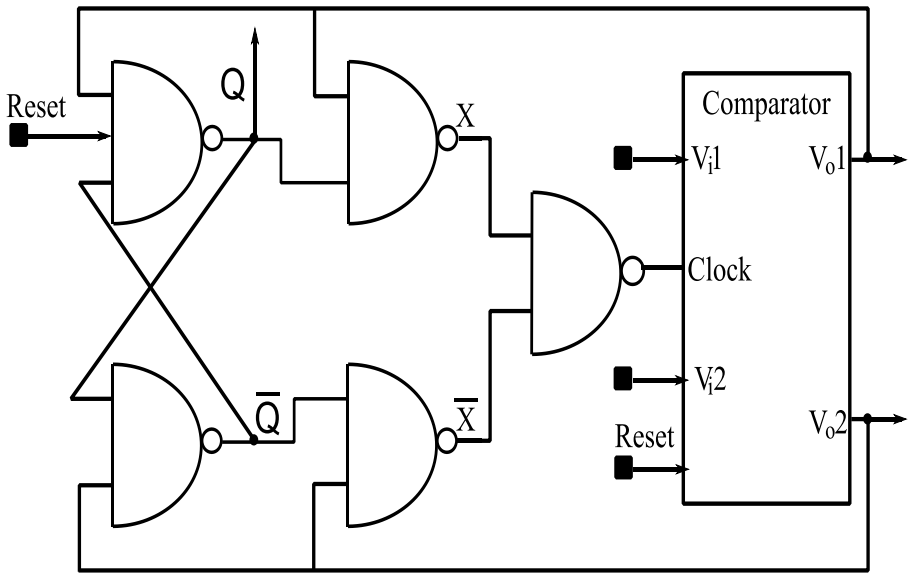


Figure 4-10 Self-timed dynamic comparator.

4.2.3.1 Self-timed dynamic comparator

This section introduces an approach which helps to employ any digital comparator for repeated comparison without external clocks. The design is based on combining the digital comparator with the toggle-logic described in the previous chapter. In the toggle-logic, conceptually, toggling is started by a change forced from the outside. Then it operates cyclically between its front and back ends. I used the comparator shown in Figure 4-9 as a new front-end for the toggle logic. In this circuit, shown in Figure 4-10, the *Reset* input is where the operation is enabled from the outside. The outputs of the comparator serve as the input to the back-end and internal stage. The results of each comparison round generate the clock for the next comparison round.

In this circuit while the *Reset* signal is held low it forces *Q, Clock, Vo1* and *Vo2* high. The comparator starts evaluation mode as soon as *Reset* is set high. The comparison is done between *Vi1* and *Vi2*. If *Vi1> Vi2* then *Vo1=0*. Falling edge on *Vo1* (*Vo2*) sets *Q* ($\bar{Q}$) high, $\bar{Q}$ (Q) and *Clock* low. Low level on the *Clock* signal terminates the evaluation mode so, *Vo1* and *Vo2* are forced back high. Recursively, the high level on these signals

push *Clock* high again. So, evaluation mode is started again and the loop is repeated in the same way.

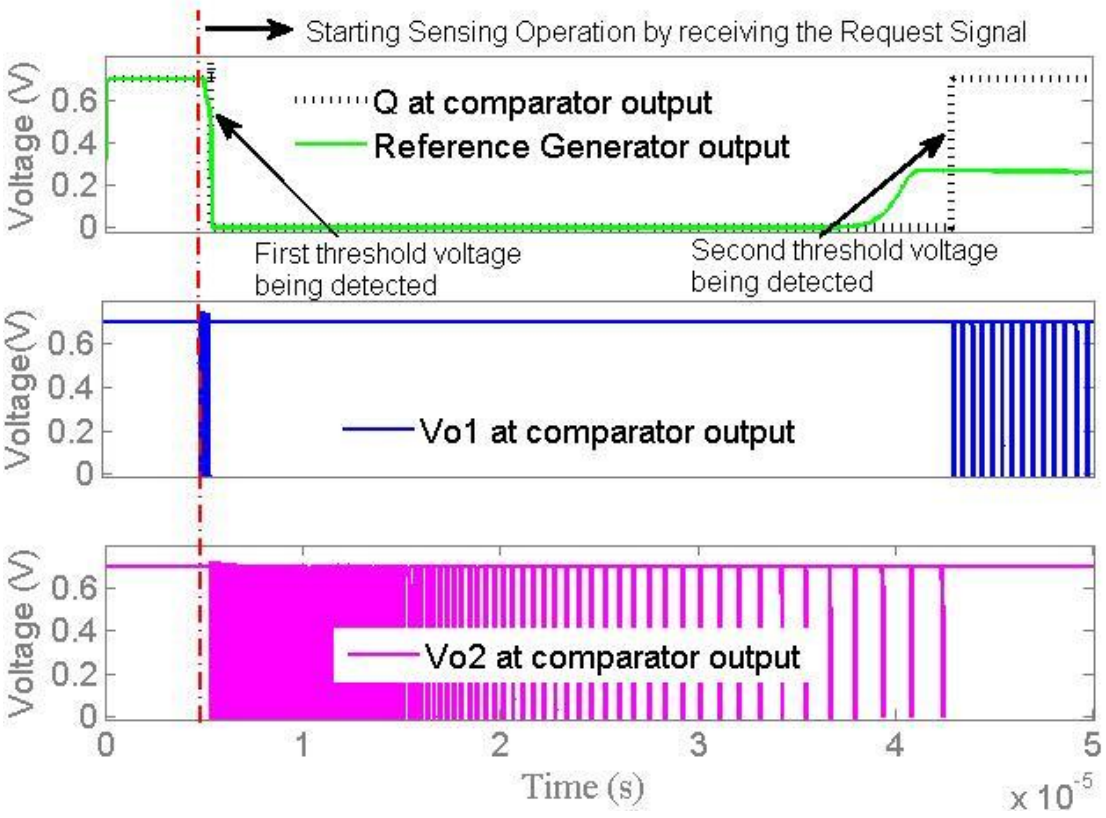


Figure 4-11 This figure is the simulation result of self-timed dynamic comparator. For this simulation, 180nm UMC technology librarye was used. This figure shows how the output voltage of the RG circuit changes the state of the comparator.

The operation of this comparator is shown in Figure 4-11. Before the first threshold and after the second threshold being detected, *Vi1>Vi2* then $Vo2, Q = '1'$ and *Vo1* oscillates. Between these two points, *Vi1<Vi2* then $Vo1 = '1', Q = '0'$ and *Vo2* oscillates.

The operating frequency of the dynamic comparator, seen at its outputs (*Vo1* and *Vo2*) is related to the time of decision making in the comparator. This time is a function of both the difference between the inputs and the magnitude of the input voltages. In the previous section, choosing *M1* bigger than *M2* creates higher weight for *Vi1* compared

to *Vi2* in comparing evaluation. This weight contributes to the true difference between *Vi1* and *Vi2*. For instance, the true difference between *Vi1* and *Vi2* after the second threshold is greater than this difference before that point. That justifies the increase of frequency after the second threshold is detected. If the two thresholds are close together, the comparator uses less energy but may be less robust.

4.2.4 Controlling unit

The main challenge in this section is to design a simple operational digital circuit which is fully supplied by the voltage being measured (V_{dd0} in Figure 4-4). This control aims to, firstly, have S_1 open and S_2 closed during the nonoperational time. Secondly, keep S_1 closed and S_2 open for the period of sensing operation (operational time). And finally, stop the counter and issue an acknowledgment (*Ack*) signal. Figure 4-12 depicts the control circuit designed. Before the request arrives the comparator is reset thus the Q output of the comparator is high. Therefore the input clock signal to the flip-flop FF1 is high. That keeps the Q of FF1 low and $\bar{Q}$ high. So, S_1 is closed and S_2 is open. Receiving the request signal toggles the state of the flip-flop. Consequently, S_1 and S_2 become open and closed respectively. That also enables the comparator and the counter to start operating.

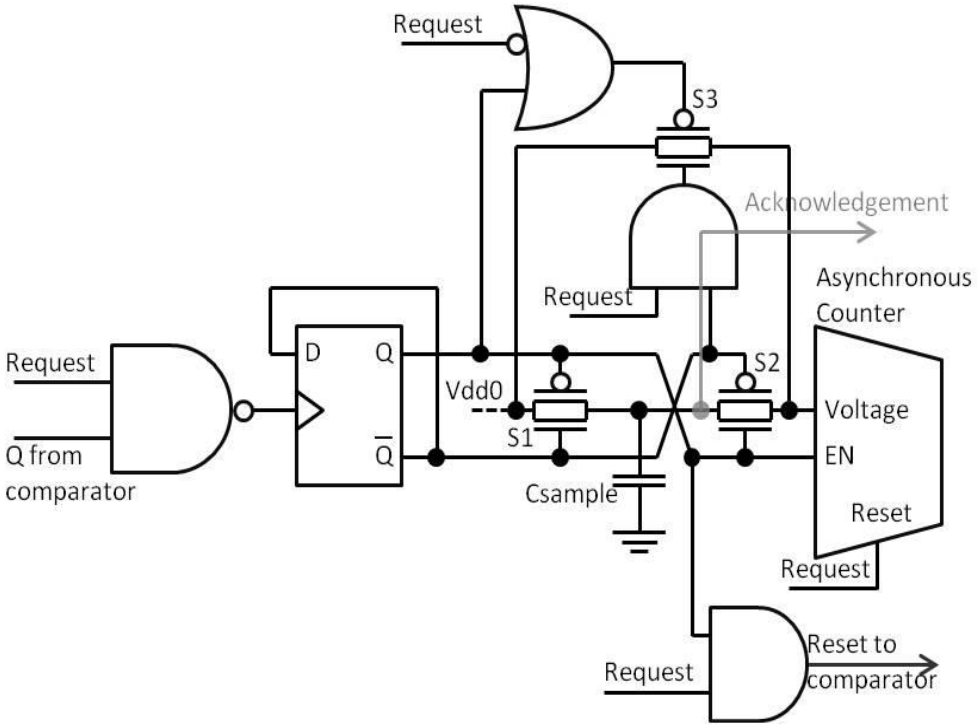


Figure 4-12 Controlling unit in details.

During the counting process, the output Q of the comparator is dropped to 0 but that doesn't change the state of the flip-flop. By reaching the second threshold, the RG circuit sets the Q of the comparator high again. That changes the state of the flip-flop back to its initial state (S_1 open and S_2 close), stops the counter making it latch the last value of count. At this moment the third switch (S_3) becomes closed. It connects the counter to V_{dd0} which charges the magnitude of the outputs of the counter up to V_{dd0} as shown in Figure 4-13. On finishing the sensing operation C_{sample} is charged again. That creates a rising edge on *Ack* to inform the environment about the validity of output code. S_3 is switched off when the request signal is pulsed low. This means that the 1 microsecond of waiting is added into the critical path of sensing.

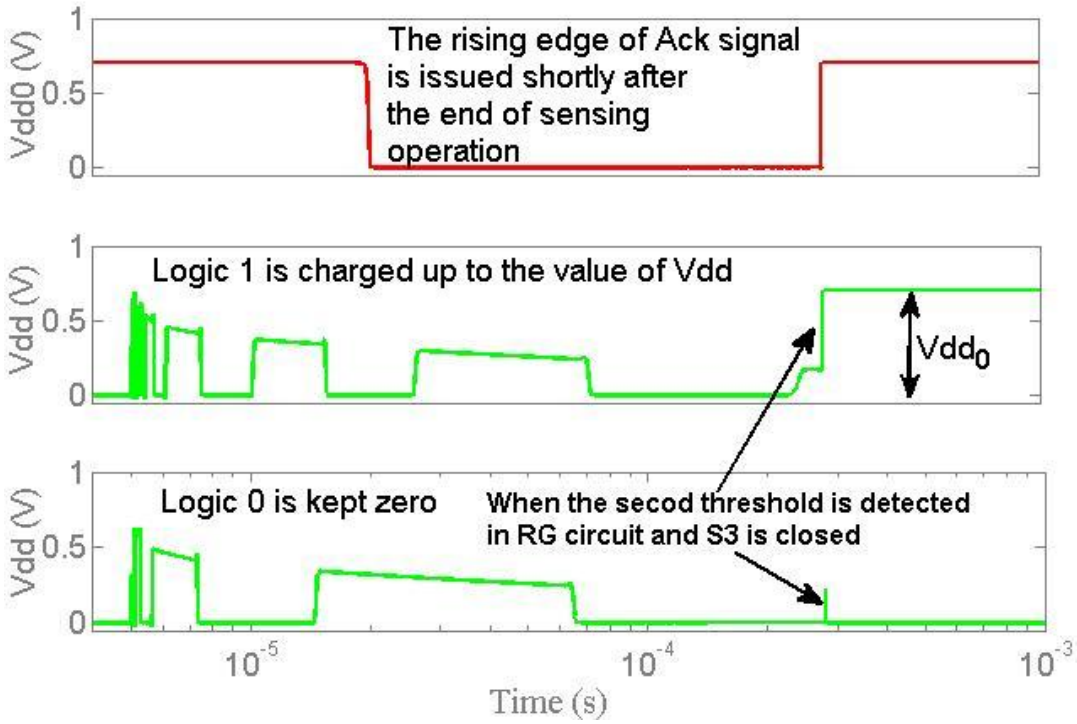


Figure 4-13 The termination of sensing operation.

4.2.5 Sensor operation analysis

Figure 4-14 depicts the values of the output count for four values of sampling capacitor, 5pF, 10pF, 12pF and 20pF, over the range 0.25V<V_{dd}<1.8V in simulation. The range of output code (and thus measuring precision) depends on the value of the sampling capacitor. Using bigger capacitors provides more energy at each V_{dd} and higher measuring precision. There is a trade-off between sensor precision and energy consumption and delay as a larger sampling capacitor means higher energy and longer time used in the sensing. As I mentioned before, for voltage sensors, the requirement for linearity in this relationship is not as strong as for conventional ADC solutions. The V_{dd0} to code characteristics shown in Figure 4-14 are therefore of very good quality.

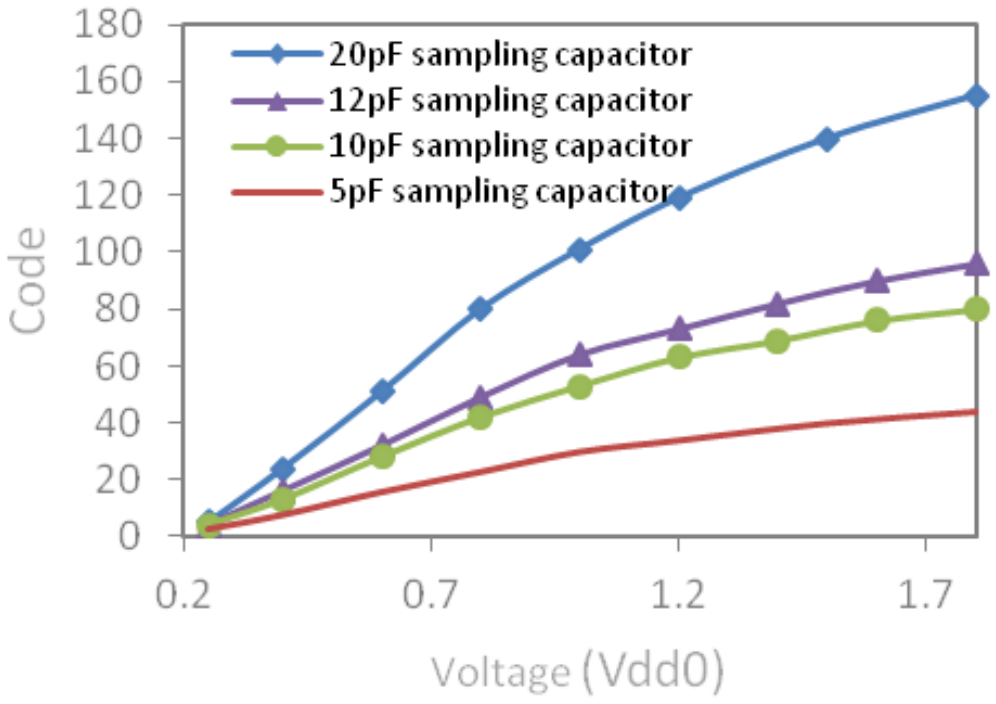


Figure 4-14 The output code of sensor over a range of voltages (V_{dd0}) from 0.25V to 1.8V.

I also examined the sensor circuit against process and temperature variations. The variation of output code versus voltage over various corners of analysis and temperature variation has been plotted in Figure 4-15. The design works robustly (no measurement failure) at all process corners over the range $0^{o}<T<100^{o}$. The effect of process variations on the RG circuit varies the first and second threshold shown in Figure 4-8. Therefore, the sensor generates different codes at different process corners. The analysis showed the maximum variation at *FF* and *SS* corners. The proper on-line solution to overcome process variations highly depends on the power management strategy being hired. The design can also be properly calibrated off-line to achieve highest accuracy [52]. Monte Carlo simulations are also conducted to examine the design over a wide range of variations (3-sigma in this case). The result of output code variation per randomly generated sample has been plotted in Figure 4-16. The result showed a single operation

error, where an out of range code of 63 was generated (expected range was between 25 and 35), among 200 randomly generated samples (0.5% error rate).

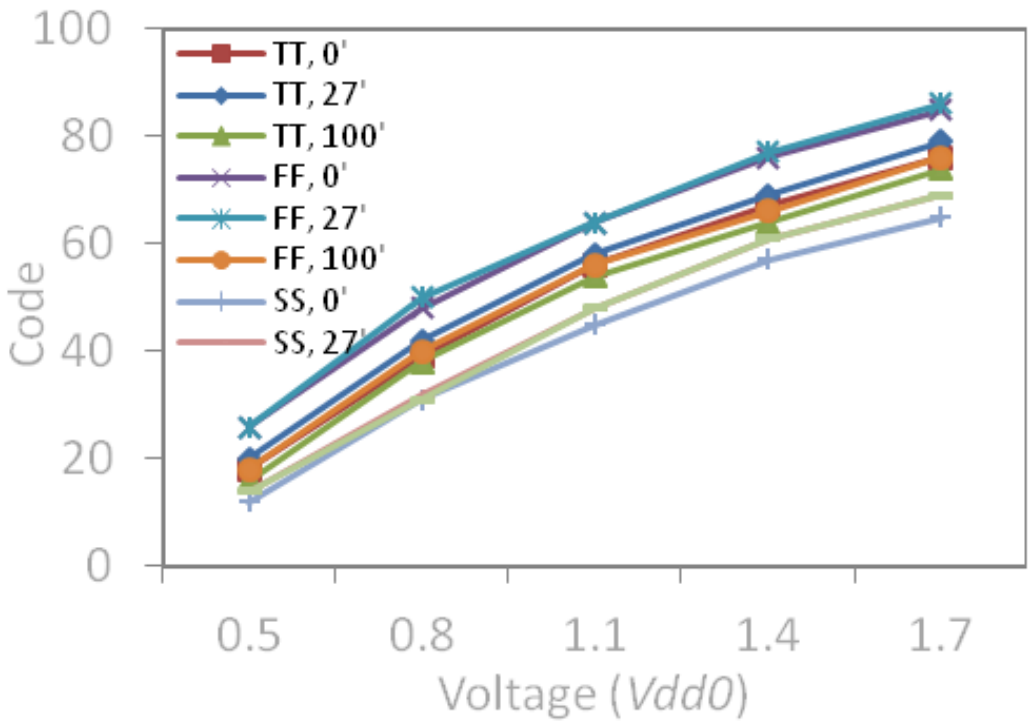


Figure 4-15 Variation of the output code over process and temperature variations.

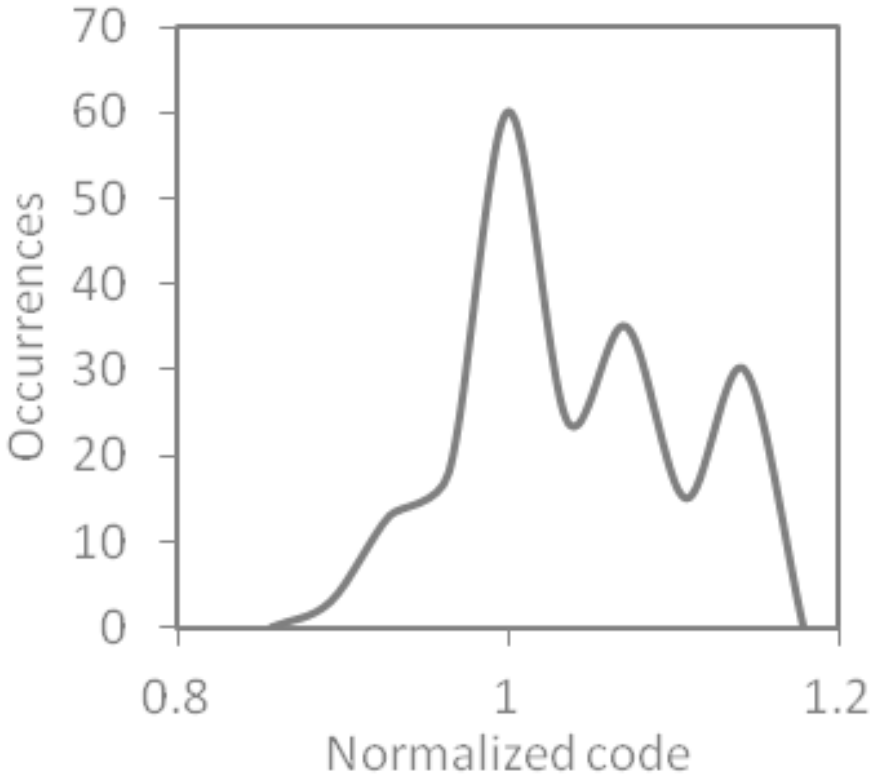


Figure 4-16 Monte Carlo simulation for 200 samples with $V_{dd0}=1.5V$ and $C_{sample}=5p$.

It was thoroughly discussed that due to the application of this sensor linear operation is not essential, however, it is important to explore the error margin of such nonlinearity. In Figure 4-17 the output code of the sensor is plotted against a) the real measured voltage, b) the predicted voltage as if the operation of the sensor is linear. According to this results the maximum error of 32% is accrued at the very beginning of the curve (output code=5). This point is in the deep subthreshold region and therefore the sensor operation is suffering from significant nonlinearity.

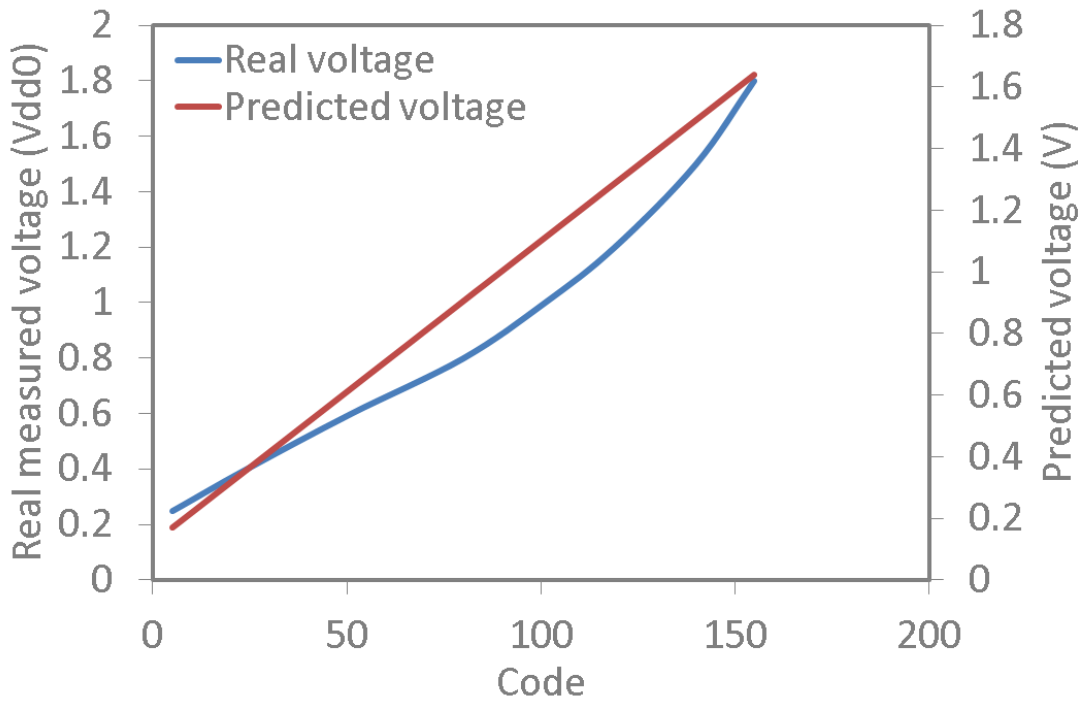


Figure 4-17 The output code of the sensor against a) the real measured voltage, b) the predicted voltage as if the operation of the sensor is linear for C=20pf.

4.2.6 Energy consumption of the sensor

In this sensor, two different energy consumer elements contribute to the overall energy consumption. The first part which consists of asynchronous counter and RG circuit is entirely powered by the energy stored in the sampling capacitor. For this part, operation continues as long as the energy is available on the capacitor. For less energy consumption a smaller capacitor can be used at the cost of lower precision of the output code. The second part is the control unit and the dynamic comparator which are supplied by the power supply (V_{dd0}). As it is shown earlier, the control unit is formed by several gates, one flip-flop and three transmission gates. The energy consumption of this part of the design due to small activity at each sensing round is considerably small. In the dynamic comparator the energy consumption depends on the number of comparisons being done in each sensing round. In this circuit, the number of

comparisons can be reduced by bringing the second threshold closer to the first threshold shown in Figure 4-8. This "polling" style of comparison, although theoretically straightforward and allowing the use of existing circuits, is not entirely satisfactory from the energy point of view. I believe that by substituting this approach with a solution not requiring repeated switching can reduce the energy consumption of the sensor. Part of my future work will be looking for solutions to eliminate polling in the comparator. However, this will not be a trivial task as existing non-polling techniques such as that used in [52] cannot be readily adapted to work in my environment. In [52] an analogue technique was used to design an asynchronous delay element. In this design voltage on a capacitor which is slowly charged by input signal, flips the state of the output inverter. One may want to use the same technique to detect the second threshold generated by the RG instead of using the active comparator in my design. The weakness of this technique is that the voltage on the capacitor should reach to at least 50% of output inverter's supply voltage. But in my design, depending on the supply voltage, output of the RG (170mV) might be less than 10% of the supply voltage ($V_{dd0}=1.8V$) which makes it undetectable by using the technique from [81].

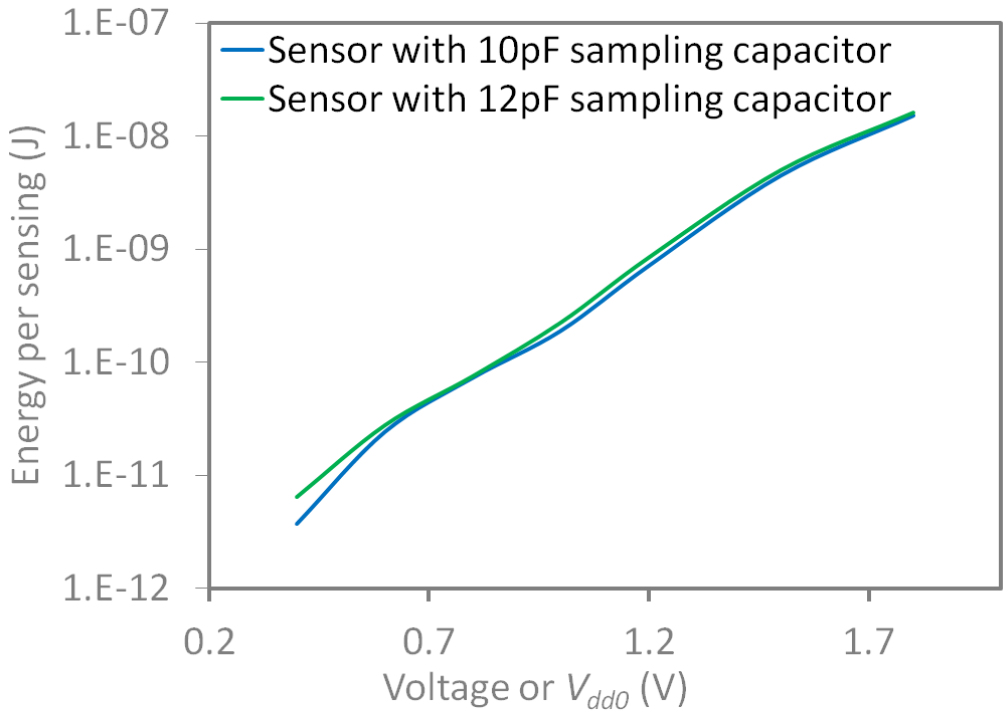


Figure 4-18 Energy consumption of the sensor.

Figure 4-18 depicts the overall energy consumption of the sensor per sensing round. This graph shows the relationship between the energy consumption of the sensor and the value of V_{dd} it measures. This monotonically increasing relationship conveys that the sensor's energy consumption only increases when the energy supplied to the system increases.

4.3 Physical implementation of the proposed sensor

The reference-free voltage sensor designed in this chapter was fabricated at a 180nm UMC technology. For this tape out, the chip design flow is started by verifying each single part of the design through exhaustive set of simulation runs. At this stage, circuits are exercised against all different possible scenarios so design's bugs are captured and fixed. The next stage is to layout the circuits.

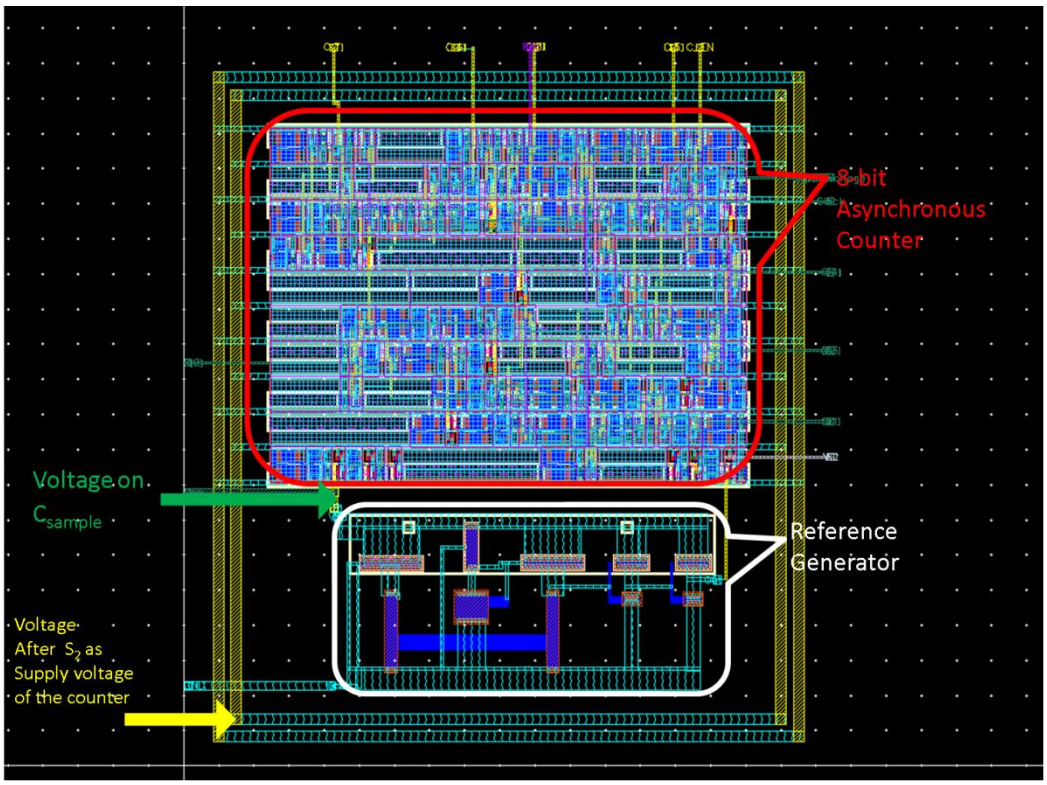


Figure 4-19 The layout of asynchronous counter and reference generator

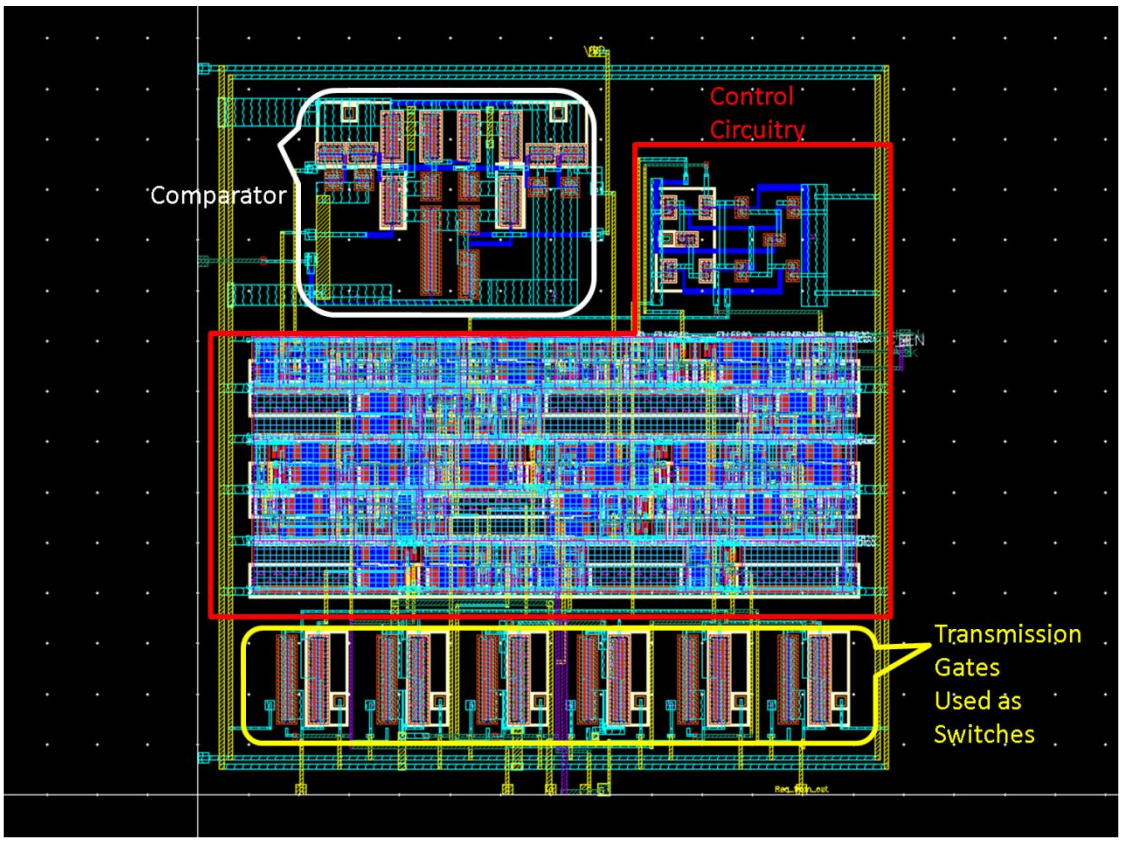


Figure 4-20 The layout of the comparator, control circuitry and switches

The design is laid out in three power domains. The first domain is the reference generator (RG) circuit which is supplied by the voltage on the sampling capacitor. The layout of the RG is depicted in Figure 4-19. In the second power domain, also shown in Figure 4-19, the asynchronous counter uses the voltage on the sampling capacitor after S_2 switch. The third power domain, shown in Figure 4-20, contains control circuitry, comparator and switches of the design.

The sensor is entirely designed and simulated using analogue tool called Virtuoso from Cadence package however for chip design, big digital (big-D) small analogue (small-A) protocol is followed. In this protocol which is shown in Figure 4-21, the design is assumed to be digital with a number of embedded analogue circuits called analogue macros. According to this protocol, the design is described in RTL abstraction

and then translated into acceptable form of netlist. Note that in this protocol, all analogue macros are also instantiated in the netlist however their abstract view must be generated. The final netlist is imported into the place and route tool (P&R) called Encounter for floorplanning, power planning, cell placements and routings.

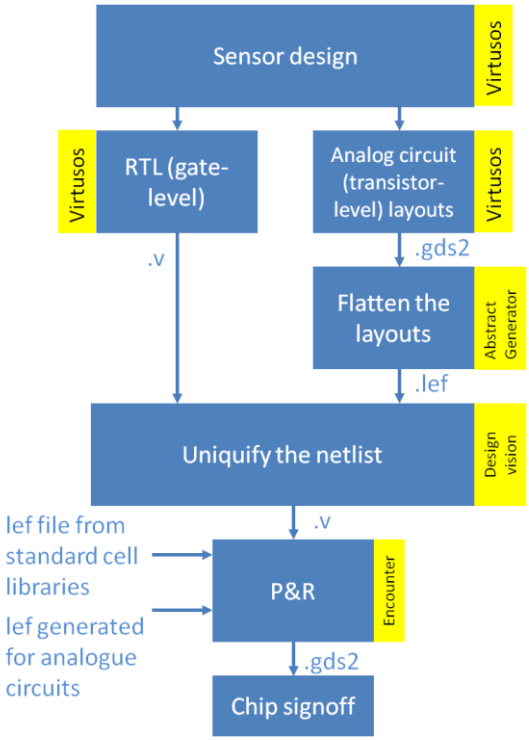


Figure 4-21 Chip design flow

Analogue circuits are manually laid out and individually investigated against DRC (design rule checking) and LVS (layout versus schematic) checks in order to generate analogue macros. Usually, Virtuoso generates the .gds2 file for the layouts and these files are applied to the abstract generator tool to generate the abstract view of the analogue macros in the form of .lef file. Figure 4-22 shows the content of the .lef file generated by the abstract generator for transmission gate which is used as analogue switch. In the .lef file, the dimension of the each metal layer in the layout is described and also the coordinate of each pins are extracted.

```
VERSION 5.6 ;
BUSBITCHARS "[]" ;
DIVIDERCHAR "/" ;

MACRO TG
  CLASS BLOCK ;
  ORIGIN -0.02 -0.66 ;
  FOREIGN TG 0.02 0.66 ;
  SIZE 9.95 BY 7.27 ;
  SYMMETRY X Y R90 ;
  PIN Ctr
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER metal1 ;
        RECT 0.02 5.95 0.26 6.19 ;

    END
  END Ctr
  PIN Ctr_bar
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER metal1 ;
        RECT 9.73 2.85 9.97 3.09 ;

    END
  END Ctr_bar
  PIN GND
    DIRECTION INOUT ;
    USE GROUND ;
    PORT
      LAYER metal1 ;
        RECT 0.06 7.63 0.3 7.87 ;

    END
  END GND
  PIN In
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER metal1 ;
        RECT 0.05 4.48 0.29 4.72 ;

    END
  END In
  PIN Out
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER metal1 ;

        RECT 9.7 4.43 9.94 4.67 ;

    END
  END Out
  PIN VCC
    DIRECTION INOUT ;
    USE POWER ;
    PORT
      LAYER metal1 ;
        RECT 0.05 0.73 0.29 0.97 ;

    END
  END VCC
  OBS
    LAYER metal6 ;
      RECT 0.02 0.66 9.97 7.93 ;
    LAYER metal5 ;
      RECT 0.02 0.66 9.97 7.93 ;
    LAYER metal4 ;
      RECT 0.02 0.66 9.97 7.93 ;
    LAYER metal3 ;
      RECT 0.02 0.66 9.97 7.93 ;
    LAYER metal2 ;
      RECT 0.02 0.66 9.97 7.93 ;
    LAYER metal1 ;
      RECT 0.02 0.66 9.97 7.93 ;
  END
END TG

END LIBRARY
```

Figure 4-22 The generated .lef file for transmission gate (TG) as analogue switch. The file is generated by abstract generator tool.

As it is seen in Figure 4-21, the generated .lef file from abstract generator for analogue circuits, the .lef file for standard cells provided by the foundry and the final netlist are imported into P&R tool for chip signoff. In this tool, the size of the core, floorplanning of the design, power planning for multiple power domains designs and *I/O* cell arrangement is performed.

4.3.1 Measurement results

The voltage sensor described in this chapter has been fabricated in the UMC 180nm CMOS process. Figure 4-23 shows the microphotograph of the die. The area occupied by the voltage sensor is only 0.013 mm^2. The chip contains my proposed asynchronous counter, the RG circuit, the comparator and the control unit. The sampling capacitor has

been placed off the chip. The fabrication shows that the voltage drop on S_2 is more than what the simulations showed. Consequently, the voltage level at the output of the counter is always slightly less than the voltage on the sampling capacitor. Therefore, at voltage level below 0.8V the sensor fails to latch the output of the counter. Therefore, below 0.8V the output of the sensor is incorrectly zero. It is also notable that due to parasitic capacitances of the *IO* pins and metal tracks the size of sampling capacitor has been increased. My experimental results have been measured for 1nF sampling capacitor.

Figure 4-24 shows the output of the counter while it is powered by the sampling capacitor. This figure shows four successive bits starting operation at 1.8V and counting as the capacitor is discharged. Figure 4-25 depicts the logic 1 voltage generated at the output of the sensor when V_{dd0} is 0.8V. This figure shows that the RG circuit detects the second threshold voltage around 240mV where the output of the counter is latched and *Ack* signal is generated. As it is seen in this figure although the counter stops counting at the very end, the logic holds the state down to 50mV. Figure 4-26 shows the operation of the sensor under variable voltage. A sinusoidal signal with 1V offset, 0.8V peak to peak amplitude and 5Hz frequency is used as input V_{dd}. Figure 4-27 shows the output code of the counter over the range of voltage from 1.8V down to 0.8V. The overall energy consumption of the design per sensing action is shown in Figure 4-28. This figure shows that the energy consumption of the design is dominated by the energy drawn by the sampling capacitor.

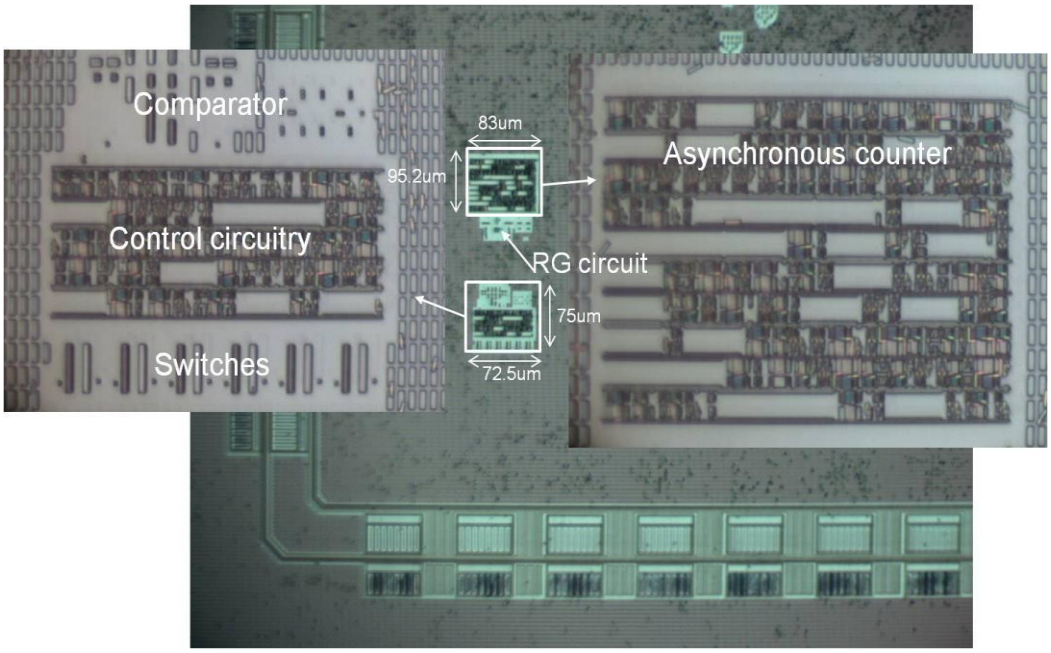


Figure 4-23 Die micrograph of the voltage sensor in 180nm technology node.

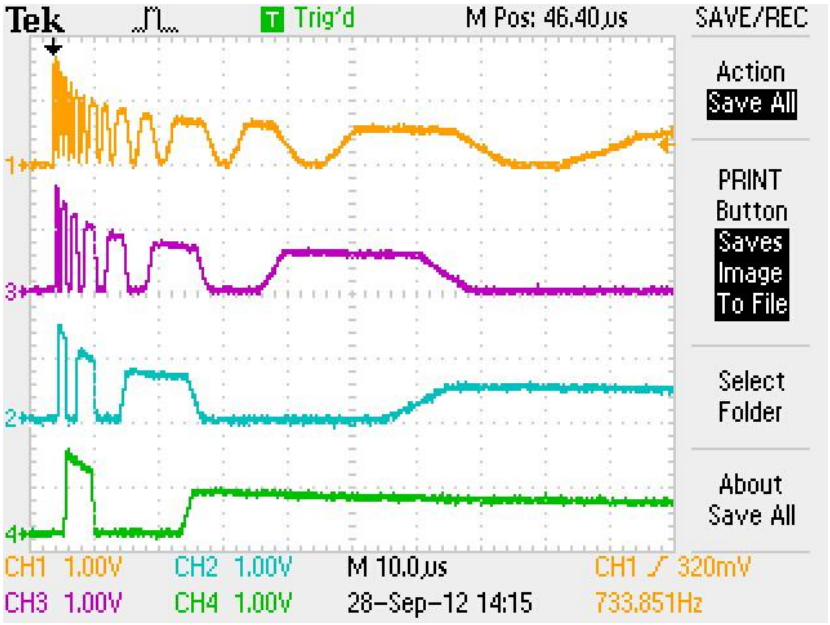


Figure 4-24 Counting action of my proposed asynchronous counter while it is powered by the sampling capacitor = 1nF.

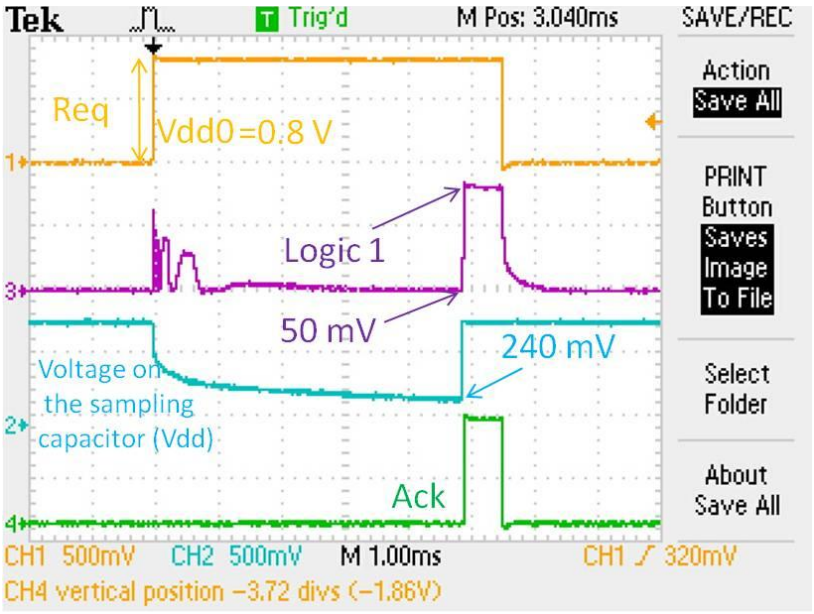


Figure 4-25 Logic one at the output of the sensor.

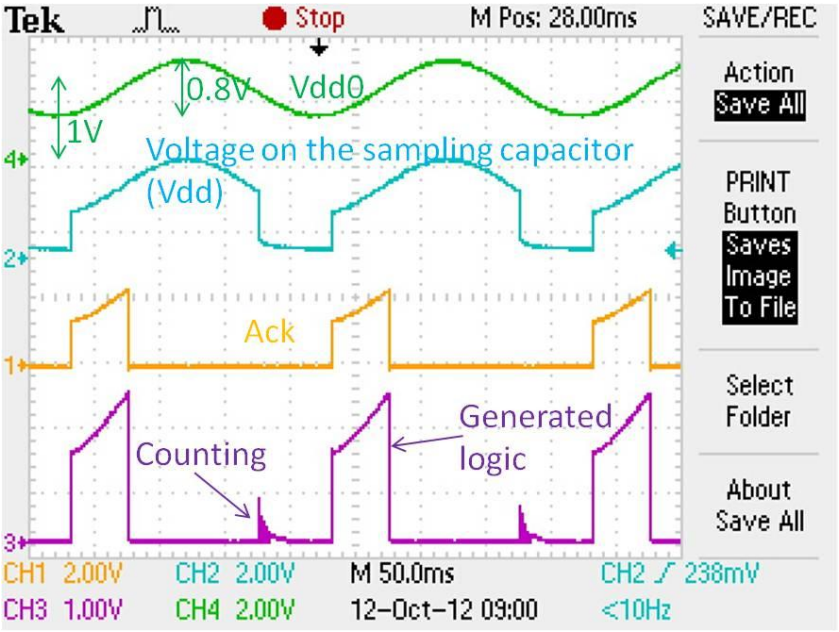


Figure 4-26 Sensor operation under variable voltage.

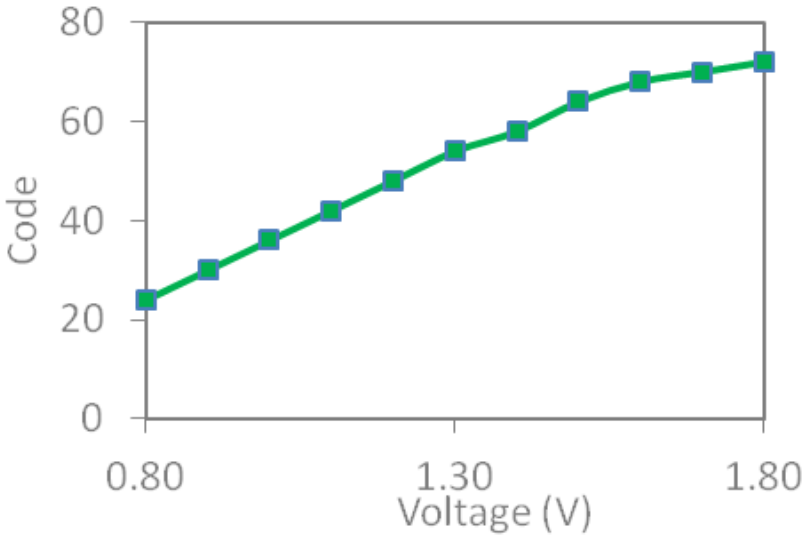


Figure 4-27 Output code of the counter over a range of voltage from 0.8V to 1.8V.

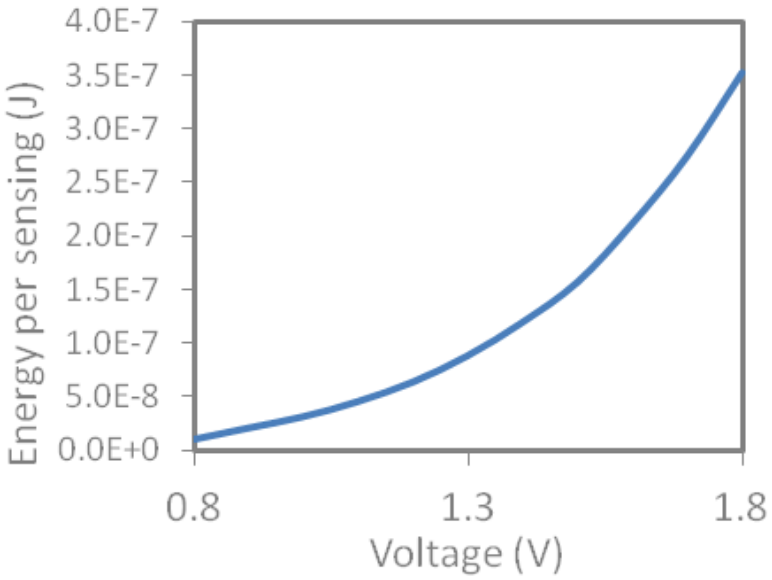


Figure 4-28 Energy consumption of the sensor measured per each sensing.

4.4 Conclusion

This chapter presents a voltage sensor for energy harvesting circuits based on a charge-to-digital converter. Reference-free implementation of the proposed voltage sensor frees it up from the requirement for a reference voltage or any external stable power supply.

This makes it suitable for the voltage variable environment. This voltage sensor consists of a capacitor-based sampling circuit, control unit and an asynchronous toggle counter circuit taken from previous chapter. The counter works using the charge stored in the sampling capacitor to count. This counter does not require a separate clock, as it relies on the asynchronous handshaking protocol under the principle of semi-modular circuits [78]. The key feature of this method is that the counter is entirely powered by the energy of the charge obtained from the voltage it measures, and the speed at which it works reflects this voltage. The sensor, fabricated in the *180nm* technology node, was tested successfully through performing measurements over the voltage range from *1.8V* down to *0.8V*

Chapter 5. Case study of reference-free voltage sensor

5.1 Introduction

As a case study, this chapter presents a power management platform specially adapted for energy harvesting systems by employing the reference-free voltage sensor which was designed in the previous chapter. This platform consists of two main parts. The first part supplies incompletely regulated voltage to the load, with the assumption that it is capable of working robustly in conditions of voltage variation. For example, consider a simple architecture of a sensor node as proposed by [12]. Usually the main computational unit, here the FFT processor, can be supplied by variable voltage within an acceptable range. The second part of the power platform provides tuneable voltage for short period of times, for instance, as is the case, for oscillators, transmitters and receivers. The challenge now is that such voltage controllability should be provided even though no stable references are available.

5.1.1 Proposed power unit for computational load

This section describes a simple power unit which employs the proposed voltage sensor designed in the previous chapter to provide the computational load with information about unregulated voltage. The main assumption for the computational load in this system is that it should operate robustly when the voltage varies. Due to this assumption, one of the best candidates for that would be a computational load which is based on self-timed logic.

In the system shown in Figure 5-1, the energy from the harvester is stored on a supercapacitor. A protection unit limits the voltage of the load (V_{dc}) within a safe range

and the sensor's operating voltage range is from 0.25V to 1.8V. Considering a small safety margin the safe range is set from 0.5V to 1.8V. This range of voltage supports the necessary operational voltage for most digital circuits designed in a 180nm technology node. Since in this system the operation of the load is irrespective of the operation of the sensor, once the protection circuit conducts ($V_{dd0} = 0.5V$) the load starts working at a preset state set by the power management unit.

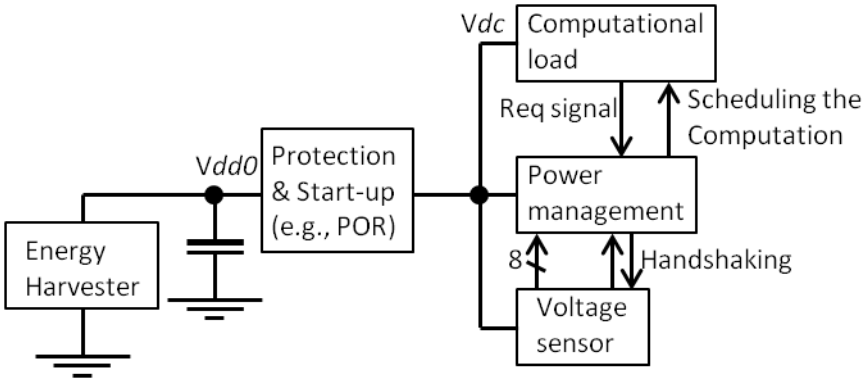


Figure 5-1 Block diagram of the system using voltage sensor.

Once the load's working mode is started, the load issues a request signal at the beginning of every one or more operations to the power management unit. This unit communicates to the voltage sensor using a handshaking protocol. The request signal from the load traverses the power management unit, reaches the voltage sensor and starts a new sensing round. Once the voltage sensor finishes its operation, it issues an acknowledgement signal to the power management unit. This unit receives the value of the voltage on the supercapacitor in the form of a digital code. The strategy of the power management unit may be to employ this data to optimize the energy effectiveness of the system.

In this mechanism, energy effectiveness of the system greatly depends on the design of the power management unit. To design this unit several parameters have to be considered such as the rate of energy scavenged by the harvester, the size of the

supercapacitor and the load. The first two parameters describe the source of energy, and the load needs to be tuned according to them. The load in this system is assumed to be functionally tunable in many scenarios. The task of the power management unit is to tune the functionality of the load to optimize its energy effectiveness according to a scenario of interest. Such a tuning is possible if several run-time reconfigurable parameters are controlled. For instance, for the FFT (Fast Fourier Transform) [22], energy consumption is a function of precision and transformation size. Memory size has also been introduced as a parameter which can be used to control the overall energy consumption [12].

5.1.1.1 Power management strategy

The strategy adopted here is merely to demonstrate the feasibility of such a system by optimizing its energy effectiveness. In this system, efficiency in terms of energy per unit of computation or activity is not the goal. The present strategy for the power management unit is to compare the readings from the voltage sensor with several preset values. This way, the quantity of energy coming from the source is reflected in several ranges. Each of these ranges is linked to a certain computational configuration in the load. Having determined the range of energy, the power management unit configures the load for the corresponding computation.

This strategy draws attention to the robustness of sensor operation. In the previous chapter, variation in the fabrication process was introduced as a parameter which affects the measurement taken by the sensor. Therefore, a certain amount of error is introduced into the system. Maximal deviations from the typical-typical (*TT*) corner of as low as 80mV at 0.5V and as high as 300mV at 1.8V were observed in the simulations. These represent less than 18% of the sensor error and are tolerable in most applications where very precise tuning of the V_{dd} is not needed. If this amount of error is not tolerable, the

sensor can easily be calibrated off-line using various techniques [52], since the output is a digital code.

5.1.1.2 System operation case study and discussion

This system is simulated using data from the vibration-based electromagnetic energy harvester [82]. Harvesters such as the unit chosen here are essentially current sources, so they can in theory charge energy storages up to any voltage value. Figure 5-2 shows the observed voltage behaviour of this harvester under a 6KΩ load. Figure 5-3 shows the voltage on the supercapacitor increases as the harvester is operating. If the charging continues without energy being drawn from the supercapacitor, the voltage would rise until either protection is activated or the capacitor breaks down.

In this system, the voltage on the load has the freedom to vary between 0.5V and 1.8V. Note that the rate of voltage variation in this system is very slow (4.5e-4 V/s) due to the presence of a supercapacitor. Therefore, in a short period of time the voltage seems to become almost stable. Figure 5-3 shows that the voltage increases from 0.5V to 2V in 3332 seconds, which represents 0.45mV per second. Thus, such a voltage can be considered as flat in the scale of one second. This time is long enough for the system to run the sensor and tune the load and for the load to complete a number of computations. However, over a long period of time, the system is strictly speaking similar to a DVS (dynamic voltage scaling) system which supports several different levels of voltage. Hence, the load in this system should be able to robustly operate under the voltage scaling. In the present simulations, the asynchronous FFT [22] is used as the load. The same considerations are applied in the case of using any synchronous load; however, extra control is needed to adapt its clock frequency to the voltage (DVFS) according to the required functionality.

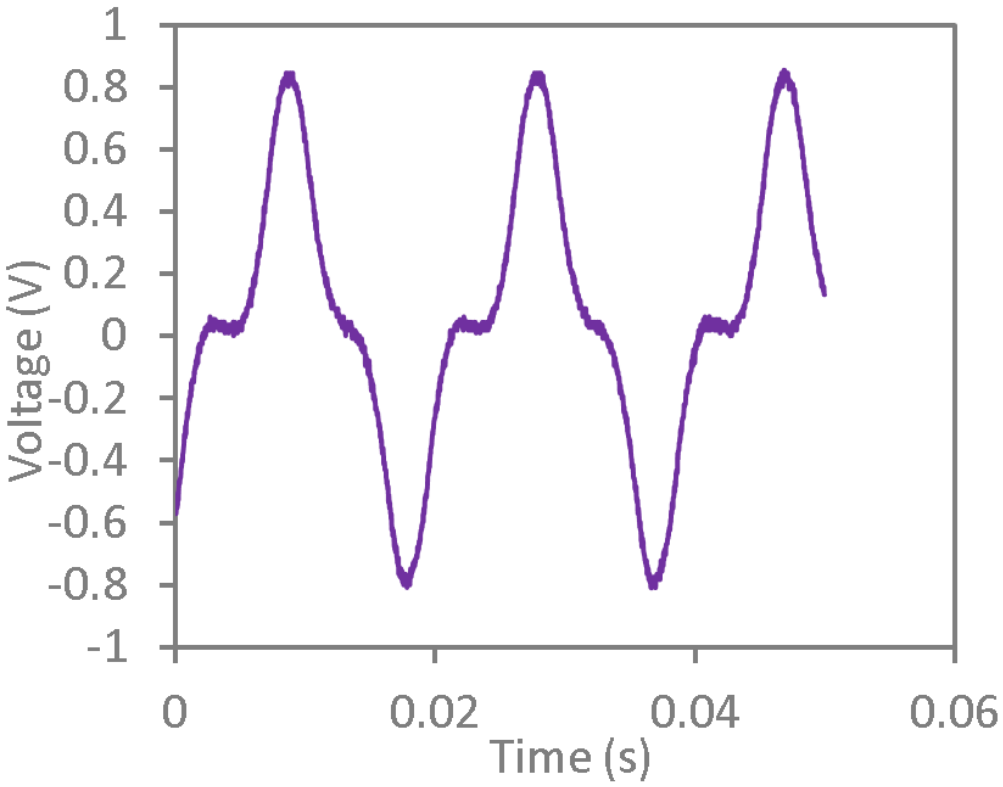


Figure 5-2 Output of the harvester when the vibration frequency is 52.4Hz, 6kΩ load and 60mg acceleration.

Tuning the FFT based on this strategy works as follows. The range of energy lower than 20mJ is assigned to the FFT configuration with a 512-point transformation and 12-bit precision. For this configuration, this amount of energy is enough for the load to complete approximately 24K operations. The next range is the amount of energy between 20mJ and 30mJ, which is assigned to the configuration with the same size of transformation but 16-bit precision. The FFT consumes almost 30mJ energy to complete 20K operations in this configuration. In general, as long as the energy available increases, the constraints regarding the number of computations per energy can be relaxed and the precision and transformation size increased. This simply increases energy effectiveness. Figure 5-3 shows that employing the FFT in a higher energy consumption mode regulates the voltage on the load to some degree. In this example, due to the amount of energy provided by this particular harvester, the number

of computations which can be specified here is huge. This particular example demonstrates that energy effective systems may schedule computations of higher quality and quantity when energy is plentiful; and reduced, but still acceptable, quality and quantity when energy becomes scarce. It is worth noting that, even though the polling comparator increases the energy consumption of the voltage sensor, especially under high V_{dd0}, the maximum energy used by the sensor in one sensing round is of the order of 10^{-8} Joules. This is negligible compared with the consumption by the system load in this example, which is in the order of 10^{-2} Joules.

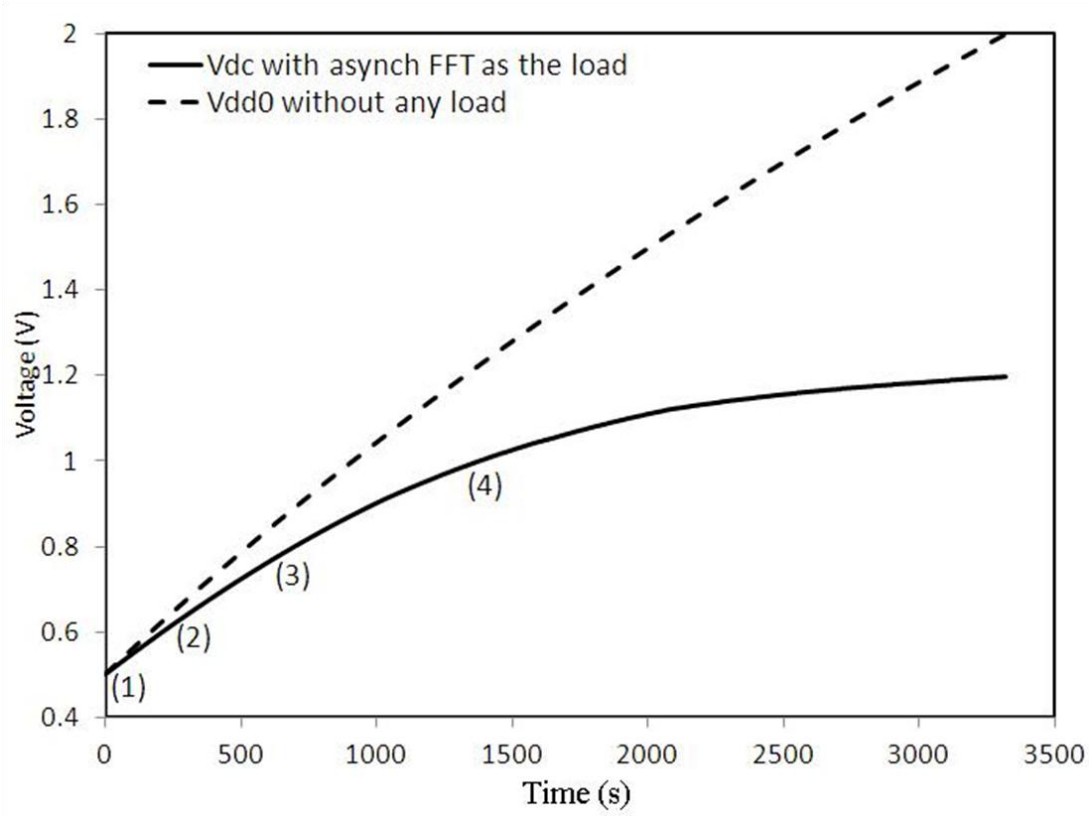


Figure 5-3 The voltage of the source with and without the FFT, the performance of the FFT is controlled depend on the available energy. (1) Transformation size 512, precision 12 bits, (2) transformation size 512, precision 16 bits, (3) transformation size 1024, 8-bit precision and (4) transformation size 1024 and *12*-bit precision.

5.1.2 Proposed power unit to provide controllable supply voltage

The second part of the proposed power platform is specially designed in the form of a buck converter to provide voltage for the parts of the load which require a controllable supply voltage. Principally, the output voltage in buck converters is controlled by switching the current of an inductor. For this purpose, two switches are employed to connect and disconnect the inductor to and from the power supply. The inductor receives energy during the time intervals within which it is connected to the power supply and discharges the energy into the load circuit during the time intervals within which it is disconnected from the power supply. The timing of the switches is controlled

by a pulse width modulated (PWM) signal generated by the control unit. The control unit uses the output voltage of the converter to generate the PWM signal. Figure 5-4 depicts the general architecture of the proposed buck converter. The design contains two separate power domains. The power train, PWM generator and power management unit (PMU) operate at the main power supply, while the voltage sensor uses the output voltage of the converter to operate. The voltage sensor in this design is the reference-free voltage sensor designed in the previous chapter. The interaction between the circuits of the two power domains is established by placing a stage of voltage level shifters in between them.

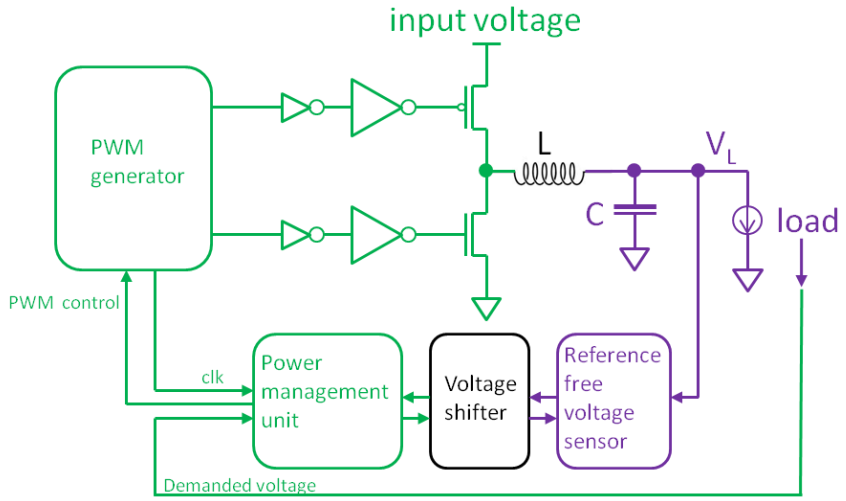


Figure 5-4 General architecture of the proposed power platform

5.1.2.1 General architecture

I assume that the input voltage shown in Figure 5-4 is the voltage on the supercapacitor in Figure 5-1 which is captured from the energy harvester. This voltage gradually increases as the harvester scavenges more energy. Once this voltage reaches a sufficient level, the PWM generator starts generating a clock (*clk*) signal and power management unit (PMU) exits its reset state and starts operating. The important task of PMU is to sense the level of the output voltage (V_l) and adjust the duty cycle of the PWM signal

accordingly. At the beginning of operation, PMU sets the duty cycle of the PWM signal to the maximum (≈ 97%) so V_l is increased quickly. PMU constantly monitors the level of V_l by means of a voltage level shifter (which operates in the form of a voltage level detector). Once a certain level of voltage is detected, the PMU sends a request signal to the voltage sensor through a delay line. The sensor measures the value of V_l and reports it back to the PMU. PMU utilizes the value of the measured voltage and the value of the requested voltage set by the load to adjust the duty cycle of the PWM signal. The value of V_l will rapidly respond to the alteration of the duty cycle of the PWM signal. Therefore, the next round of sensing must be delayed so V_l has enough time to be properly stabilized (this time is a function of the LC filter). This is the reason why an adjustable delay line is employed right before the start of the new sensing round. The similar procedure is repeated as long as the value of V_l reaches to the requested voltage by the load.

I believe that this platform is only enabled when the load needs a certain value of voltage. Furthermore, my voltage sensor operation is significantly low power. Therefore, requesting consecutive round of sensing as long as the power platform is enabled is acceptable.

5.1.2.2 Circuit operation

The PMU and PWM generator operations are started when a start up circuit such as a simple power-on reset (POR) circuit finds the input voltage sufficiently high for robust operation. The detailed architecture of interconnects between the PMU and peripherals is shown in Figure 5-5 and the operation waveforms are shown in Figure 5-6. The clock signal is an internal signal generated by the PWM generator and its frequency is modulated by the level of supply voltage. At first, the mode of operation recognized by the PMU is cold-start; therefore, it sets the duty cycle of the PWM generator (*PWM_DC*)

to the maximum. An 8-bit input to the PWM generator determines the duty cycle of the output pulse. In the example used to plot signals in Figure 5-6, the maximum duty cycle was set at 250 (*0xFA* in *Hex*). It is shown in Figure 5-7 that a high duty cycle of the PWM signal forces the output voltage of the converter to increase rapidly. This voltage (*Output_Voltage*) is continuously monitored through a simple voltage level shifter in the form of a comparator by the PMU for a minimum voltage level. The monitoring is done in three stages which occur at three successive rising edges of the clock. First, the PMU issues a reading signal (*Output_Voltage_reading*) to enable the voltage shifter. Second, it reads the output of the voltage shifter; and, third, the voltage shifter is disabled. The same operation is repeated continuously so logic "1" is received from the voltage shifter which means that the output voltage of the converter is sufficiently high for the reliable operation of the load circuit. From this point, the PMU enters the normal mode of operation. In this mode, it issues an enable signal (*counter_en*) to a loadable counter to count. The counter generates a request signal (*Req*) to the voltage sensor when its counting is finished. This counter acts as an adjustable delay line in order to make sure that the output voltage of the converter has been stabilized before the sensor operation starts. This delay-line is effectively tuned according to the off-chip LC filter. After receiving the *Req* signal, the sensor starts and finishes its operation followed by sending an acknowledgement signal (*Ack*) to the PMU through a voltage shifter. The *Ack* signal of the sensor should be monitored constantly; therefore, this particular level shifter is enabled by each raising edge of the clock signal. Once the *Ack* signal is detected, the PMU reads the sensor outputs in the 3-stage monitoring process described above. Note that the demanded voltage set by the load, which is also applied to a set of voltage shifters, is monitored in the same way as the *Ack* signal. It is assumed that the demanded voltage from the load is in fact set by the computational part of the load which is operating under variable voltage.

Once the readings are completed the PMU computes *PWM_DC* based on the current duty cycle value, the voltage measured by the sensor and the voltage demanded by the load. A different approach can be adopted to compute the duty cycle. In this particular implementation, (5-1) has been used to generate the results. This equation gives:

$$PWM_{DC(next)} = \frac{PWM_{DC(current)} demanded\ voltage}{measured\ voltage} \qquad (5-1)$$

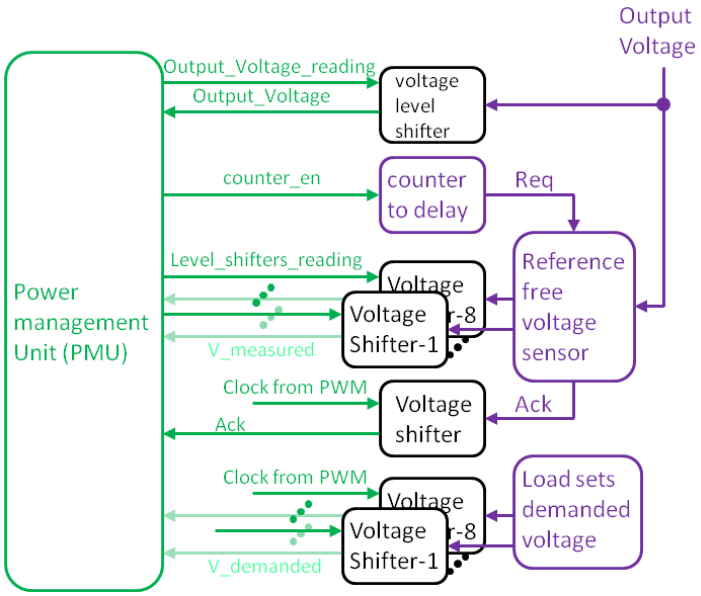


Figure 5-5 PMU signalling

As a case study, it can be assumed that the voltage demanded is 1V (code *0x35* in *Hex*), and during the cold-start state detected by PMU the output voltage is pushed from 0V to 1.6V. The sensor detects this voltage and sends the code to PMU. Using equation (5-1), *PWM_DC* is set to *0xAE*. As seen in Figure 5-7, this duty cycle pushes the output voltage down to 1.15V (≈1.2V). In the next round of measurement, the sensor detects this level of voltage and returns *0x3F* to PMU. For this, the *PWM_DC* computed by PMU is *0x92*, which brings the output voltage down to 1V as requested.

The converter is also examined in situation in which the input voltage is changing as well. As shown in Figure 5-7, if the input voltage drops from 1.8V down to 1.4V, the

output voltage which has previously been set to 1V will drop to 0.8V. Through the sensing process, the PMU recognizes the drop and re-computes the *PWM_DC*, taking the new measurement from the sensor on board.

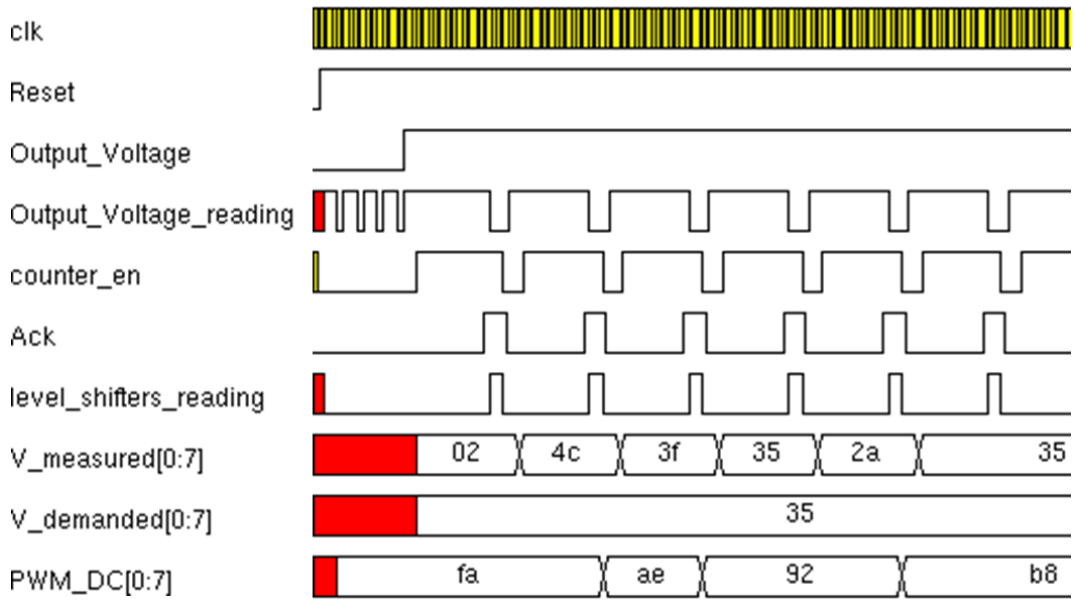


Figure 5-6 Waveforms for PMU

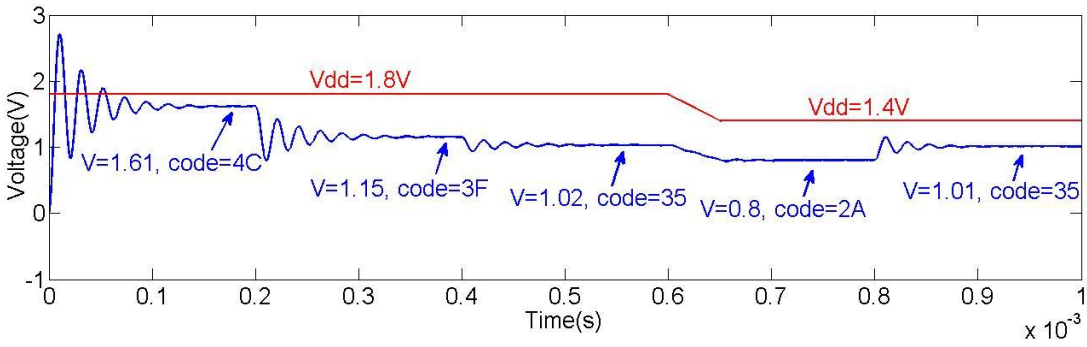


Figure 5-7 Output voltage of the converter over time, (codes are in Hex) for L=500uH and C=22nF.

5.1.2.3 Power management unit (*PMU*)

In the previous section the operation of the converter was presented in detail. It has been clarified that the operation is designated by the power management unit (PMU). Figure 5-8 depicts the algorithm for the operation of the PMU designed for this converter. According to this algorithm, the operation of the PMU can be viewed in three states: 1) monitoring, 2) reading and 3) computing.

In the monitoring state, the PMU waits for the output voltage to reach the sufficient level for robust operation of the load. The PMU reads the value of output voltage from the sensor and the voltage demanded from the load in the reading state. Finally, the PMU computes the proper PWM duty cycle according to the information provided. The PMU with this specification has been designed and simulated at RTL level.

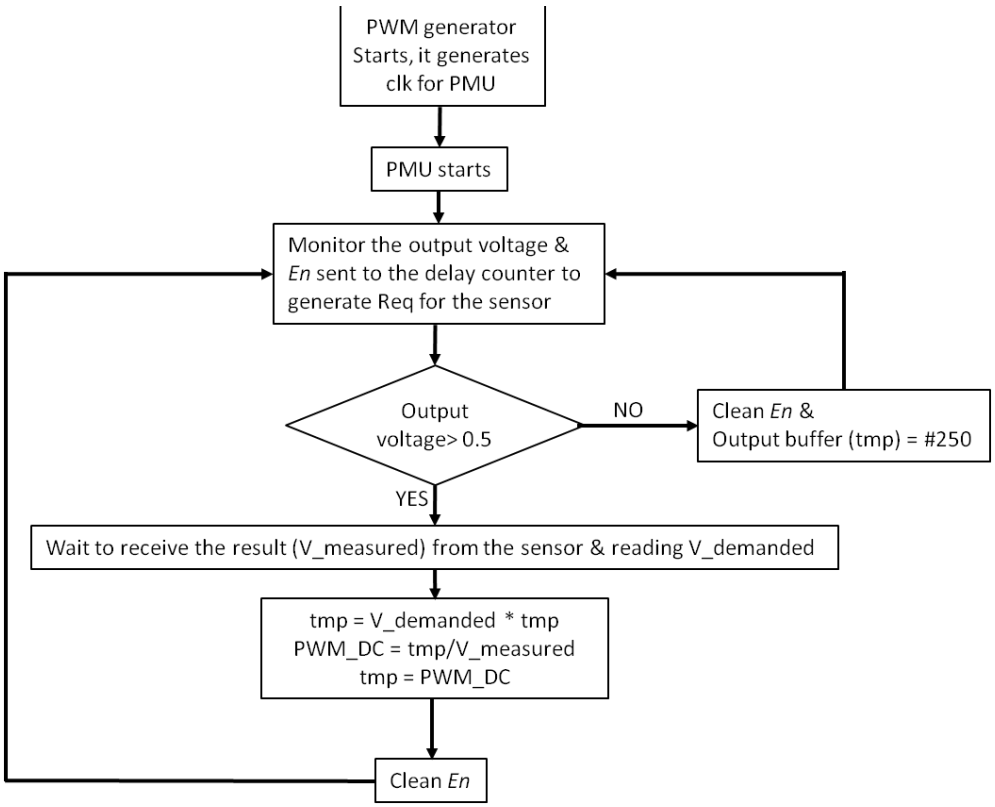


Figure 5-8 Flowchart showing the operation of the PMU

In order to prepare the PMU for fabrication, the RTL design should be synthesized using 180nm technology node Faraday libraries. Figure 5-9 shows the circuit generated for PMU by the Design Vision tool from the Synopsys package tools. Using PrimeTime from the same package tools, the power consumption of the design for the test-bench in Appendix C was found to be around 67uW.

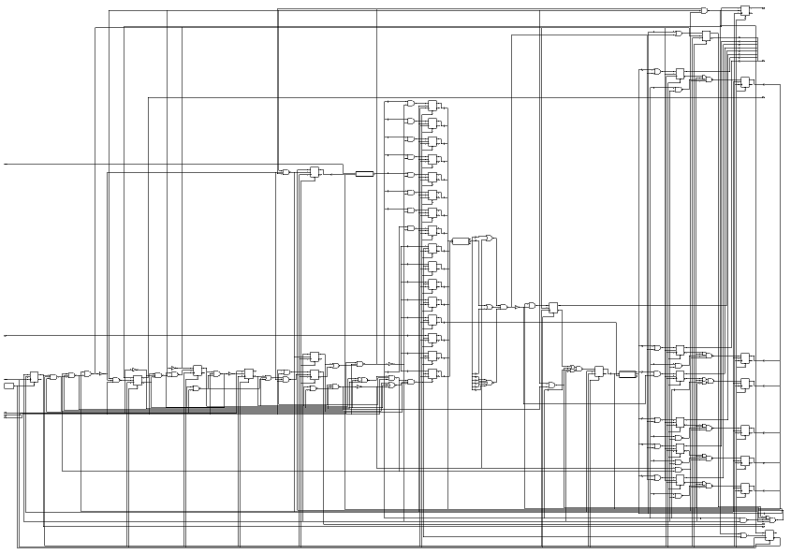


Figure 5-9 The schematic of the PMU generated by the synthesis tool.

In this design, the PMU is the only part which needs to be timed; however, accurate timing is not required. Thus, it is crucial to guarantee the robust operation of the PMU within the range of input supply voltages. However the operation of such a circuit breaks down due to violations of the timing assumptions. PrimeTime was employed to examine the design for the most critical path at the worst case process corner. It was found that, at the *SS* corner, the longest path takes 51.86ns. As a result, reliable operation requires a clock frequency smaller than 9.64MHz.

The PWM generator also serves as the clock generator in this design. It is discussed later how the PWM generator provides clock signals with different frequencies. Thus, reliable operation can be guaranteed by selecting the clock frequency which does not violate the timing assumptions of the PMU within the operating voltage range. It is believed that frequency selection can be conducted at the calibration stage after fabrication.

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : pmu
Version: C-2009.06-SP3
Date   : Fri Nov 23 11:49:42 2012
****************************************


  Startpoint: In_Data_reg[3]
              (rising edge-triggered flip-flop clocked by clock)
  Endpoint: PWM_DC_reg[7]
              (rising edge-triggered flip-flop clocked by clock)
  Path Group: clock
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clock (rise edge)                  0.00       0.00
  clock network delay (ideal)              0.00       0.00
  In_Data_reg[3]/CK (DFCLRBN)              0.00       0.00 r
  In_Data_reg[3]/Q (DFCLRBN)               0.39       0.39 f
  div_70/U12/O (INV1S)                     1.03       1.42 r
                    .
                    .
                    .
  div_70/u_div/u_add_PartRem_0_0/U21/O (AO222)      0.47     48.84 f
  div_70/u_div/u_add_PartRem_0_0/U20/O (AO222)      0.46     49.29 f
  div_70/u_div/u_add_PartRem_0_0/U19/O (AO222)      0.46     49.75 f
  div_70/u_div/u_add_PartRem_0_0/U18/O (AO222)      0.46     50.21 f
  div_70/u_div/u_add_PartRem_0_0/U17/O (AO222)      0.46     50.66 f
  div_70/u_div/u_add_PartRem_0_0/U16/O (AO222)      0.45     51.12 f
  div_70/u_div/u_add_PartRem_0_0/U15/O (AO22)       0.25     51.37 f
  div_70/u_div/u_add_PartRem_0_0/U14/O (AO112)      0.28     51.65 f
  div_70/u_div/u_add_PartRem_0_0/CO (pmu_DW01_add_10)  0.00  51.65 f
  div_70/quotient[0] (pmu_DW_div_uns_0)             0.00     51.65 f
  U123/O (AN2)                             0.21      51.86 f
  PWM_DC_reg[7]/D (DFCLRBN)                0.00      51.86 f
  data arrival time                                  51.86

  clock clock (rise edge)                  60.00     60.00
  clock network delay (ideal)               0.00     60.00
  PWM_DC_reg[7]/CK (DFCLRBN)                         60.00 r
  library setup time                       -0.18     59.82
  data required time                                 59.82
  -----------------------------------------------------------
  data required time                                 59.82
  data arrival time                                 -51.86
  -----------------------------------------------------------
  slack (MET)                                        7.96
```

Figure 5-10 Part of the report generated by the PrimeTime for worst case process corner timing analysis

5.1.2.4 Voltage level shifter

As stated above, due to multiple power domains in the design, the use of voltage shifters is indispensible. For this purpose, the design of a zero-bias current comparator [83] is optimized to be used as voltage level shifter. Figure 5-11 shows the adapted circuit to be used as the voltage level shifter.

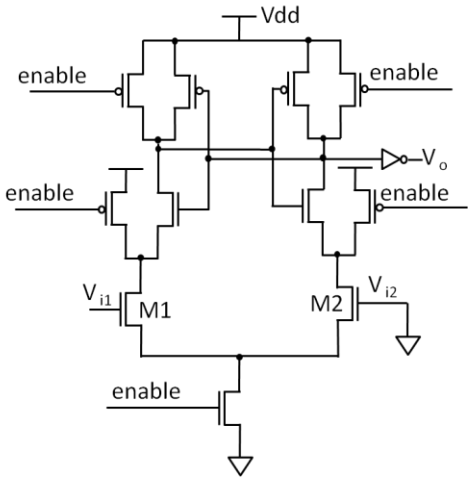
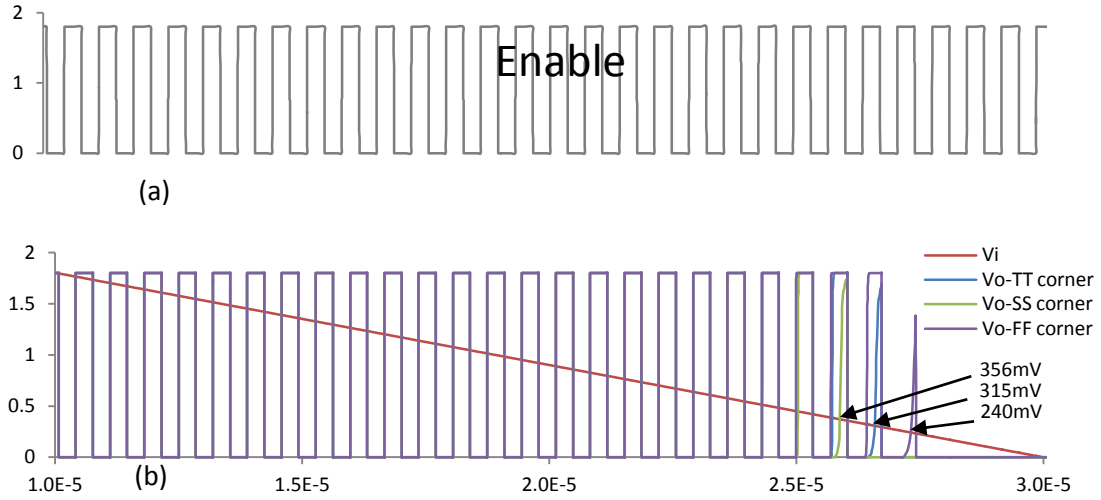


Figure 5-11 Zero-bias current comparator to be used as voltage shifter

The operation of this circuit as a comparator has been discussed in the previous chapter; however, in this chapter this circuit is used as a voltage level shifter. In principle, one simple solution to convert a comparator into a simple voltage shifter is to connect one of the inputs to the maximum voltage of the logic zero. In the present design, however, providing such a fixed voltage permanently is almost impossible. The solution to this problem is to constantly apply a ground (GND) to one of the inputs (for instance V_{i2} in Figure 5-11) which uses the transistor with the larger channel width. That way, the required voltage margin (ξ) between V_{i1} and V_{i2} is created. For V_{i1} to win the comparison, the following must be satisfied:

$$V_{i1} > V_{i2} + \xi \qquad (5-2)$$

Analysing the simulation results for this design, a setting of $W_{M2}= 1.5\times W_{M1}$ was applied, and W_{M2} and W_{M1} are the widths of *M2* and *M1* respectively. Figure 5-12 shows that the variation of ξ across different corners of analysis is slightly bigger than 100mV; however, it is sufficiently above zero.



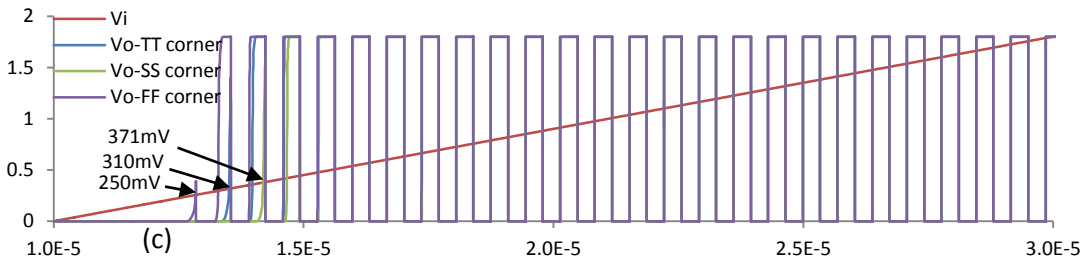


Figure 5-12 Voltage shifter operation in different process corners, (a) enable signal, (b) operation with falling input, (c) operation with raising input.

5.1.2.5 PWM generator

One of the crucial parts of any DC-DC buck converter is the design of the PWM generator. Various designs have been proposed in the literature for low power PWM generators [69, 84, 85]. Analog solutions [69] usually rely on a comparison between a ramp signal and a fixed voltage reference. A solution of this kind cannot be adopted in the present design since obtaining a fixed voltage reference cannot be guaranteed. In digital solutions, PWM pulses can in principle be generated by pushing an adjustable delay into a fixed clock frequency. For example, the design in [84] uses a simple delay line with a multiplexer to achieve an adjustable delay line. It was concluded in this study, however, that low frequency pulses require longer delay lines and consequently bigger multiplexers, which will increase the area overhead of the design.

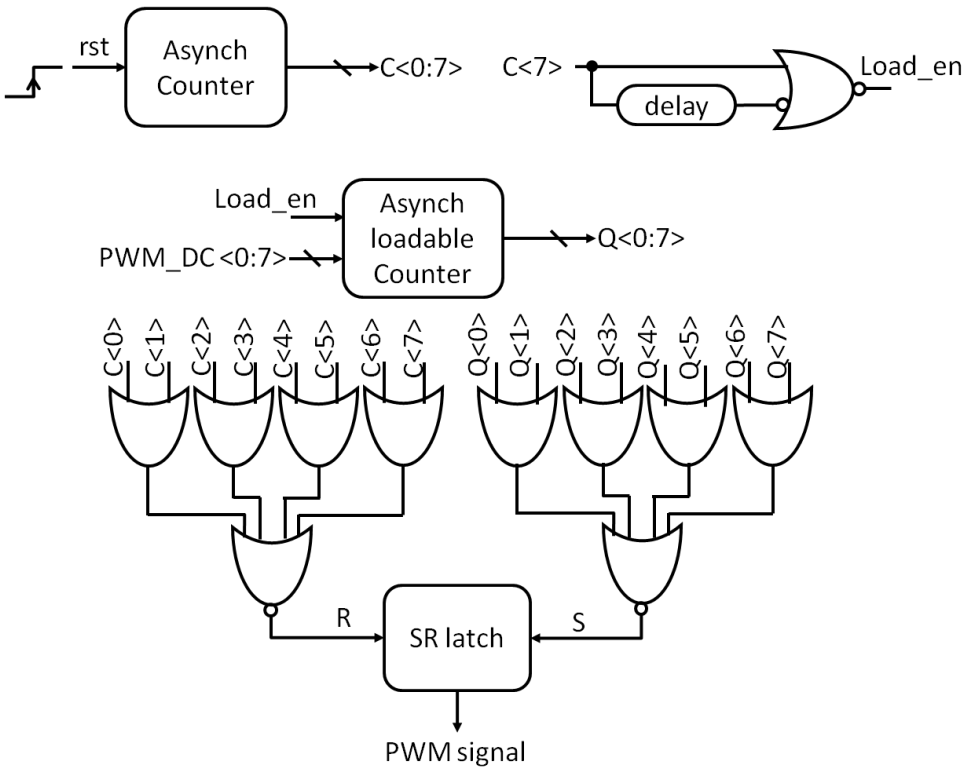


Figure 5-13 Block diagram of the ascynchronous *PWM* generator.

The schematic of the proposed PWM generator is depicted in Figure 5-13. The asynchronous counter designed in chapter 3 is also used here. Once the *Load_en* is generated, the loadable counter counts 256-*PWM_DC* clock cycles. During this time the output *PWM* signal is reset. When the output of the loadable counter (Q[7:0]) reaches "00000000", the *S* becomes 1 and as a result the PWM signal is set as high. This signal remains high for the *PWM_DC* number of clock cycles. At the end, the output of the asynchronous counter (C[7:0]) becomes "00000000", which resets the *R* and that will reset the PWM signal. This operation is shown in Figure 5-14. Note that the signals generated at the outputs of the asynchronous counter are used as the clock frequency of the PMU. It was stated above that a frequency which does not violate the timing assumptions of the PMU should be selected for reliable operation in the post-fabrication calibration stage. The lowest frequency generated by the asynchronous counter at its MSB is around 1.22MHz, which is sufficiently lower than the acceptable clock

frequency of PMU (9.64MHz) in its worst case operation. In order to achieve maximum system performance and minimum power consumption, the highest clock frequency which is smaller than 9.64MHz generated by the counter must be used. For this purpose the sixth output bit (C<5>) with a frequency around 4.88MHz gives the best results.

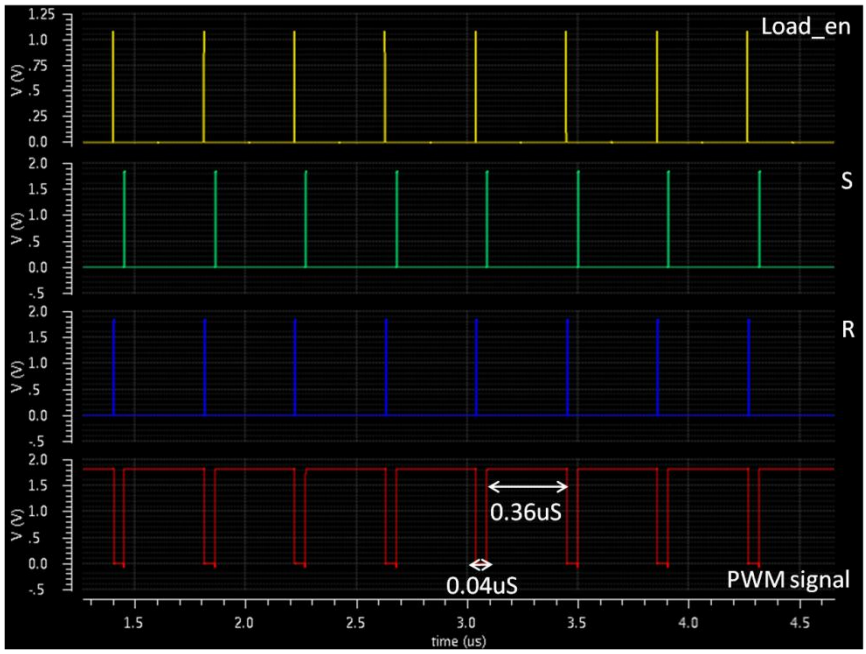


Figure 5-14 PWM generator operation at *V=1.8V*, frequency of output PWM signal is 2.44MHz, *duty cycle = 0.88* (*PWM_DC = #240*).

5.1.2.6 System efficiency

This section studies the proposed design in terms of efficiency and power losses, although achieving high efficiency is not the ultimate goal of this design. Conventionally, the types of loss in a buck converter are recognized to be 1) conduction loss, 2) timing error, 3) switching loss, and 4) quiescent loss [86].

The on-resistance of the power switches dissipates power as the current flows through the power train. This is what is called conduction loss. For an on transistor I have:

$$r_{ds} = \frac{1}{g_{ds}} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_T - V_{DS})} \qquad (5-3)$$

In order to minimize the conduction loss, r_{ds} must be minimized. For this purpose, the length (L) must be minimized and the width (W) must be increased. Increasing the width of the transistor will increase the size of the gate capacitance. Therefore, increasing the width of the transistor to reduce power loss is only effective if the power loss due to the gate capacitance is small. Figure 5-15 shows the relationship between the width of the NMOS and PMOS and their power loss while the length has been kept at 180nm.

Short circuit power dissipation due to timing error is also another source of power loss. A short circuit path is temporarily established in the power train during switching. The conventional approach to reduce this loss is to create dead-time while neither switch is on.

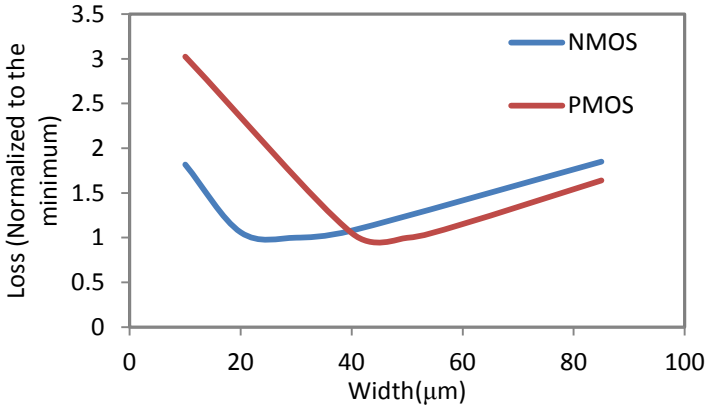


Figure 5-15 Optimizing the size of the width of the transistors for the minimum loss, $W_N=30\mu$ and $W_P=50\mu$.

In order to overcome the problem of timing error, a simple circuit is designed to create a fixed dead-time within the switching cycle.

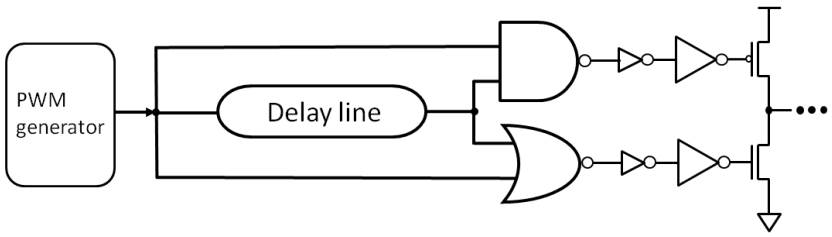


Figure 5-16 Circuit solution to create a fixed dead-time.

The pulses generated at the PWM generator are delayed through a fixed delay line. Negative OR (NOR gate) and negative AND (NAND gate) operations are used between the delayed pulse and the original PWM pulse, and the results are applied to the PMOS and NMOS power switches respectively. Using this circuit, as seen in Figure 5-17, guarantees that NMOS is switched ON when the PMOS is properly OFF and vice-versa. That removes the possibility of forming a short-circuit path during switching.

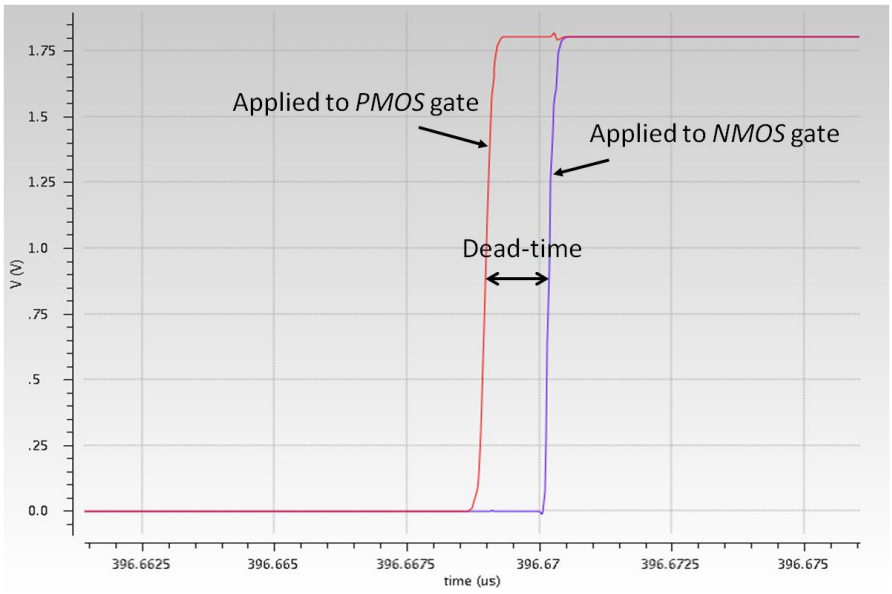


Figure 5-17 The dead-time created to overcome timing error

The third type of loss is switching loss. This comes in to the picture when the voltage on the switch and the current through the switch are not zero at transient time. The product of the voltage and current gives the amount of switching loss. Conventionally,

zero-current switching (*ZCS*) or zero-voltage switching (*ZVS*) are used to decrease switching loss. These circuits operate to control the dead-time periods within transient time to guarantee that either the voltage on the switch or the current through the switch is zero. The fixed dead-time created by the circuit in Figure 5-16 not only reduces the loss due to timing error, but also partially recovers the switching loss. Due to the fact that the main design objective here is not efficiency, the design of *ZCS* or *ZVS* has not been considered for this system.

Quiescent loss is the power consumption of the control circuitry. It usually comes in to the picture when the converter powers a light load.

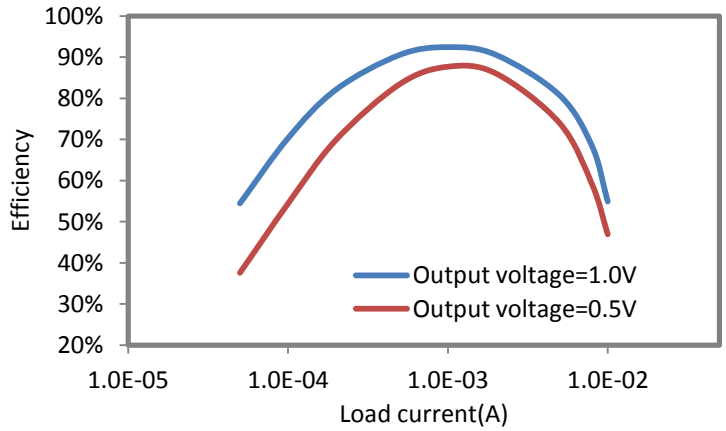


Figure 5-18 Simulation result of the efficiency of the proposed converter for 2 different output voltages without considering the PWM.

Figure 5-18 depicts the efficiency of the converter for two different output voltages over the range of load current without considering the power consumption of the PWM generator. A comparison of different sources of loss shows that, at high current load, the conduction loss of the switches in the power train is the main source of power loss. As the current load levels decrease, the other sources of power loss such as switching and timing error become dominant. The power consumed by the control circuitry, or

quiescent power loss, is usually only important with light loads. That is why lower efficiency is achieved for lighter loads as shown in Figure 5-18.

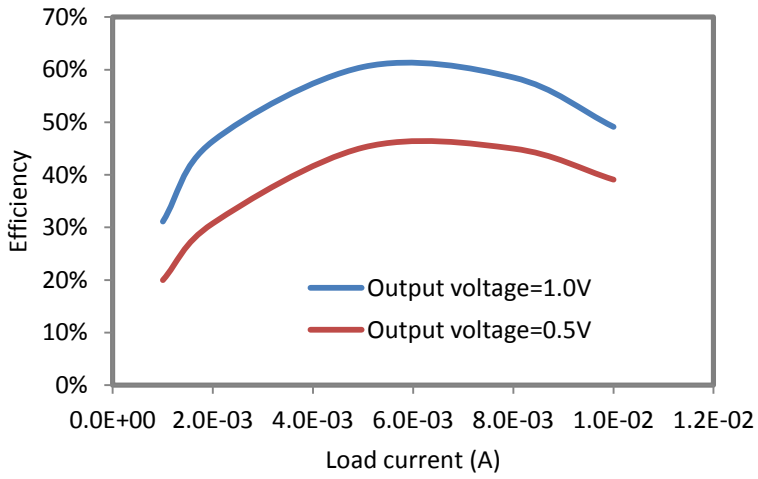


Figure 5-19 Simulation result of the efficiency of the proposed converter for 2 different output voltages with PWM.

In Figure 5-19, the power consumption of the PWM generator has also been taken into consideration in measuring the efficiency of the converter. As expected, the overhead due to the power consumption of the PWM generator massively degrades efficiency with light loads. As seen in this figure, the maximum efficiency reaches 60% when the converter supplies a 5mA load at 1V.

The normal range of efficiency for converters is usually reported to be above 80%; however, in this design the maximum efficiency does not exceed 60%. The reason for this is that the power required to generate the clock frequency is spent from the total power budget of the converter. In the design of conventional converter, efficiency is measured without considering the power consumption of the reference clock and voltage generators.

5.2 Conclusion

The ultimate goal in this chapter is to design a power platform using the proposed reference-free voltage sensor. This platform is designed in two parts. The first part supplies that part of the load which can tolerate variations in voltage with incompletely regulated voltage. In this part, the main effort is not spent on power processing, but on tuning the load according to the level of measured voltage to improve the energy effectiveness of the system. The second part of the design contains the circuitry which provides the controllable supply voltage for the load. The essential requirement for this part is flexible operation since the supply voltage fluctuates. This is achieved in the present design by removing those parts which are dependent on the fixed timing. In this design, the only part which needs to be timed is the PMU; however, accurate timing requiring a fixed frequency reference is not needed. It has been explained that the PWM generator provides the internal clock with the frequency modulated by the level of input voltage. Generating the internal clock adds more overhead to the overall power consumption of the design. As a result, the efficiency of the system degrades as seen in Figure 5-19. It is believed that, in the context of system performance, the efficiency achieved is tolerable for a system operating in an energy-scarce environment. In fact, the objectives for a system operating in such conditions change from energy efficiency to robust operation and consequently load computation survivability.

Chapter 6. Conclusions

In this work, the importance of the measurement of energy to develop an energy-aware system within energy harvesting environment has been described. It has been shown that, in energy harvesting environment, providing a fixed and stable power supply as well as a voltage or time reference is next to impossible.

This thesis has presented a unique design of a reference-free voltage sensor which provides the energy information required for the system. The simple design of this sensor allows robust operation under supply voltage variations.

6.1 Summary

The proposed solution for the design of such a sensor is to use the very simple idea of charge-to-digital conversion. For this purpose it is assumed that the energy of the harvester can be sampled into a capacitor. This energy is used to generate switching activity in a circuit. The amount of switching generated is related to the level of energy sampled into the capacitor. In the third chapter of this thesis, the concept of charge to circuit switching was discussed in detail. A ring oscillator was used as the simplest circuit to generate switching activity. Through detailed analysis and circuit modelling, a closed-form mathematical solution was achieved which shows a hyperbolic relationship between capacitor discharging voltage and digital circuit switching for both super- and sub-threshold regions (3-20 and 3-23). The design of an asynchronous counter was also proposed which can be used instead of a ring oscillator in real sensor implementation. The reason for this is that the counter is capable of generating the switching activity in the more compact binary code form as opposed to the ring oscillator which generates unfolded results as thermometer code.

The detailed circuit design of the reference-free voltage sensor was discussed in the fourth chapter. This sensor contains an energy storage unit whose stored energy is related to the voltage being sensed; the asynchronous counter is used as a computation unit to convert this energy to a binary code, and a control unit manages the sensing process including its start and finish. For this sensor, the sensing round starts by receiving a request signal from a power management unit or any other entity which requires information from the sensor. The control unit disconnects the capacitor from the power supply and connects it to the asynchronous counter. Then, it enables the counter to start counting for a certain time and, in due course, it stops the counter. The sensing round is finished by issuing an acknowledgment signal to the environment. The counter's eventual progress is the output code describing the level of power supply.

A control unit was then designed to conduct the code recovery process. The task of this unit is to monitor the voltage drop on the capacitor and preserve the output code before the energy is used up. This is achieved through the design of a dynamic comparator, a controlling circuit and a reference generator. The reference generator uses the intrinsic property of CMOS technology to create a soft reference which indicates a threshold voltage. This circuit has been configured in such a way that an induction pulse is generated towards the very end of the voltage drop when the capacitor discharges. The indication pulse is detected by the comparator circuit and that triggers the control unit. The control unit stops the counter and saves the last of its output results and then sends out an acknowledgment signal.

The voltage sensor has been fabricated in the UMC 180nm CMOS process. The area occupied by the sensor circuitry is 0.013 mm^2. The chip contains the proposed asynchronous counter, the internal reference generator circuit, the self-timed dynamic comparator and the control unit. Through this fabrication run, the feasibility of voltage

sensing through the proposed charge-to-digital technique was successfully tested. The experimental results from the chip demonstrate (shown in Figure 4-27) successful operation over the voltage range from 1.8V down to 0.8V. The detailed analysis of the chip showed that the voltage drop on the charging switch (S_2 in Figure 4-4) at subthreshold region was more severe than what the simulation results had shown. This unexpected voltage drop was the reason why the sensor failed to operate at voltages below 0.8V. One possible improvement to this design is to use bigger transistors for this switch in order to minimize its voltage drop.

In the fifth chapter, a simple example of a power architecture was designed, which contains two parts. The first part uses the voltage sensor, a simple management unit and the computational load. In this part, it was assumed that the computational load can work robustly in conditions of voltage variation. The voltage sensor detects the level of incoming voltage and sends this information to the management unit. The management unit employs this information to tune the configuration of the computational unit so that it fits the energy status. In simple terms, while the amount of energy is sufficiently high, computation at high resolution is configured, and at poor energy status lower resolution is chosen. The second part of the proposed power architecture contains a design of a simple DC-DC buck converter. In this design, the voltage sensor is used to reference freely measure the output of the converter. A simple management unit was also designed for this part, which uses the results from the voltage sensor to adjust the PWM generator. This part of the power architecture is specially designed to provide controllable supply voltage for very short periods of time. This can be used to power components such as phase locked-loops or transmitters.

6.2 Future work

The first part of this research delivers insights into the relationship between capacitor discharging through circuit switching employing a simple ring oscillator circuit. This analysis can then be generalized to more complex circuits, even those with random switching, by, for example, applying approximations. For instance, a more complex self-timed circuit, such as a micro-pipeline, can be approximated by a parallel-sequential oscillator where the cycles of charging and discharging of the parasitic caps alternate with some discretisation in time. The most important point is that this discretisation should be accomplished not with a constant time step, but with a logic switching step; where, again, the switching index is the basis for the generating function. The time interval between adjacent steps is then modulated by the voltage on the power line, which clearly declines. So, the approximate characteristics of the whole process would still be as a complex hyperbola, similar to the one derived in the simple circuit analysis. This is an interesting conjecture which needs to be investigated in future research.

This thesis has also addressed the concept of energy-aware systems as the main candidate for energy harvesting environment. Two main characteristics of this system are: 1) high resolution techniques used to control power, including power gating, clock gating and DVS, and switching activity, such as pipelining, parallelizing, or task scheduling; 2) an effective system management regime which configures the mode of operation in the system via controlling the power and switching activity. A prerequisite to the latter is a highly refined online voltage measurement method which can operate reliably in energy harvesting environments. It is believed that the sensing technique proposed in this work is, in fact, the necessary foundation upon which to implement any energy-intelligent system. One of the most interesting areas for future work is thus to

implement the energy-aware system designed in the fifth chapter. For this system, apart from changing the precision of the computation, prioritizing the task queue, or even powering down some part of the memory according to the energy information can be used to optimize system performance.

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Appendix A

The following describes the techniques of energy saving in a circuit at transistor-level and system-level:

Transistor-level energy saving techniques

Using different size of transistors for different gates is another circuit-level technique used to minimize energy consumption [75, 87]. In a real circuit operation, not all of the gates need to operate at the same speed. Therefore, the sizes of transistors can be adjusted so that the delay constraints are satisfied. This will reduce the total energy consumption of the circuit.

Threshold voltage is also one of the parameters which can be used to control circuit speed and energy consumption. Using low-threshold transistors will increase the circuit's operating speed and also the leakage current. Conversely, high-threshold transistors result in low circuit speed and leakage current [75, 87].

Voltage between the bulk (body) and source (S) of the transistor can also be used to save energy. In normal operation, V_{bs} is kept zero, with no body bias or NBB; however, it can be inversely biased. Reverse body-bias or RBB, which is used when the transistor is in off-mode, increases the threshold voltage of the transistor. Increasing V_{th} means lower leakage and lower speed of operation [88]. Conversely, forward body bias (FBB) used in the on-mode increases speed and decreases the sensitivity to variation in V_{th}. It also decreases the sensitivity to gate length, oxide thickness and doping of the channel [88].

System-level energy saving techniques

The effect of V_{dd} on energy consumption has been fully detailed in previous sections. The DVS technique has also been studied in which energy savings are achieved by scaling the supply voltage. At the system level, the same concept can be used, albeit with more flexible strategies. For instance, a system with many components can be supplied with different V_{dd} levels according to the speed required by each component. Here, lower V_{dd} supplies slow down components and higher V_{dd} supplies speed them up [75]. Using this approach, energy can be saved wherever high speed is not required.

Using variable V_{dd} for each individual circuit is another approach used to achieve the same goal. In this technique V_{dd} is increased when the circuit needs to operate at high speed and vice-versa. An adjustable voltage regulator with high efficiency over a wide range of output voltages is required in this approach.

Power and clock gating are perhaps the most widely used methods of saving energy in the microelectronics industry. In these techniques, the power and clock are disconnected from parts of the circuit not currently in use. The circuit will be powered and clocked whenever its operation is started, and extra circuitry is required to detect inactive zones in the system. A retention mechanism is also required to save the state of the circuit before powering down and to restore it after powering up.

1. Pass transistor

Studies have shown that pass transistors instead of standard logic gates can also be used to achieve low energy consumption [89, 90]. Energy savings, in this technique, are achieved due to the fact that the pass transistors do not need a continual power supply, as opposed to the traditional circuit topology.

2. Adiabatic switching

In simple inverters, while the header transistors are conducting the footer transistors are off, therefore, the C_l receives charge from the main power supply. At this phase the energy extracted from the main power supply is $C_l V_{dd}^2$. Half of this energy is dissipated on the header transistors and the other half is stored in the C_l. By changing the combination of the input signals, the footer transistors start conducting and header ones are switched off. At this phase, all the energy which was previously stored in the C_l, is dissipated. Consequently, the dynamic energy dissipated of a single gate contains one charging and one discharging phase, is $C_l V_{dd}^2$. Half of this energy is dissipated at the resistance of the channel of the header transistors and the other half is dissipated at the footer ones [91].

Let's assume that the power supply is a current source which can deliver constant current at the switching time (T). Therefore, the energy dissipation on the header and the footer transistors due to the resistance (R) of their channel is [91]:

$$E_{diss} = PT = I^2 RT = \left(\frac{C_l V_{dd}}{T}\right)^2 RT = \left(\frac{RC_l}{T}\right) C_l {V_{dd}}^2 \qquad (A-1)$$

This equation shows that the energy dissipation on the channel resistance during the charge or discharge periods can be reduced by increasing the switching time (T). This is called adiabatic charging and the circuits are using adiabatic switching if the charging and discharging phases are arranged to be adiabatic. The word adiabatic refers to the fact that the charge is transferred while the heat generating is removed (due to the lower energy dissipation at each transistor) [91].

3. Charge recycling

The charge recycling scheme is one of the newest methods used to save power at the circuit level. In this technique a capacitor is placed between the footer transistor and the

ground. The current which passes through this capacitor towards the ground charges the capacitor. This charge is used as a virtual V_{dd} for the next logic block [92].

Through the switching activity in source block, the charge collected by the virtual ground is increased. The source block has the option to use the real ground instead of the virtual one if the voltage on the virtual ground becomes too high. The voltage on the virtual ground is then pushed to a higher voltage using a simple analogue charge pump so it can be used as the virtual V_{dd} for target blocks. Target blocks are not required to stay active all the time. Therefore, the charge collected in the past can be used to power them. If the virtual V_{dd} is not sufficiently high, the target block chooses the real V_{dd} maintaining robust operation. Reported results show that recycling the charge can save energy up to 10% on average [92].

Appendix B

The IO file to designed for the chip tape out:

```
# IO file for UMC180 mini@sic, including bond pads
#
# Filling order:
# Top: left --> right
# Left: bottom --> top
# Bottom: left --> right
# Right: bottom --> top
#
# IO pads snap to 0.62 grid with offset of 0.02
#
# ------------------------------------------------
(globals
    version = 3
    total_edge = 4
    io_order = default
)
# 3 IO rings:
# 1: Bond pads, 5.53um from die edge
# 2: IO pads, 84.53um from die edge
# 3: Corner cells, overlaps ring 2
(row_margin
          (top
          (io_row ring_number = 1 margin = 5.53 )
          (io_row ring_number = 2 margin = 84.53 )
          (io_row ring_number = 3 margin = 84.53 )
          )
          (left
          (io_row ring_number = 1 margin = 5.53 )
          (io_row ring_number = 2 margin = 84.53 )
          (io_row ring_number = 3 margin = 84.53 )
          )
          (bottom
          (io_row ring_number = 1 margin = 5.53 )
          (io_row ring_number = 2 margin = 84.53 )
          (io_row ring_number = 3 margin = 84.53 )
          )
          (right
          (io_row ring_number = 1 margin = 5.53 )
          (io_row ring_number = 2 margin = 84.53 )
          (io_row ring_number = 3 margin = 84.53 )
          )
)
(iopad
    (top
    (locals ring_number=1 )
    (keepclear begin = 5.53 end = 219.12)

          (inst  name="1_pad"           cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
          (inst  name="2_pad"           cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
          (inst  name="3_pad"           cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
          (inst  name="4_pad"           cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
          (inst  name="gnd_ana1_pad"    cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
          (inst  name="vcc_ana1_pad"    cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
          (inst  name="5_pad"           cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
          (inst  name="6_pad"           cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
          (inst  name="7_pad"           cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
          (inst  name="8_pad"           cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
          (inst  name="9_pad"           cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
          (inst  name="10_pad"          cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
```

```
(keepclear begin = 1294.82 end = 1519.47)
(locals ring_number=2 )
(keepclear begin = 84.53 end = 140.12)

    (inst  name="I44"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I46"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I16"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I27"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="gnd_ana1"       cell = XSCI0CUTDSG place_status=placed indent=0 )
    (inst  name="vcc_ana1"       cell = XSCI0CUTDS place_status=placed indent=0 )
    (inst  name="I12"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I9"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I13"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I10"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I14"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I69"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )

    (keepclear begin = 1215.82 end = 1440.47)
)
(left
(locals ring_number=1 )
(keepclear begin = 5.53 end = 219.12)


    (inst  name="12_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="13_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="14_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="15_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="16_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="17_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="18_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="19_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="20_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="21_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="22_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="47_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )


(keepclear begin = 1294.82 end = 1519.47)
(locals ring_number=2 )
(keepclear begin = 84.53 end = 140.12)

    (inst  name="I63"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I65"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I43"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I42"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I41"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I40"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I39"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I38"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I37"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="I36"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="vcc_io"         cell = VCC3ACUTD place_status=placed indent=0 )
    (inst  name="I17"            cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )

    (keepclear begin = 1215.82 end = 1440.47)
)
(bottom
(locals ring_number=1 )
(keepclear begin = 5.53 end = 219.12)

    (inst  name="23_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="24_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="25_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="26_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="27_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="gnd_ana2_pad"   cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="vcc_ana2_pad"   cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
    (inst  name="29_pad"         cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
```

```
      (inst  name="30_pad"          cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="31_pad"          cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="32_pad"          cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="33_pad"          cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )

(keepclear begin = 1294.82 end = 1519.47)
(locals ring_number=2 )
(keepclear begin = 84.53 end = 140.12)


      (inst  name="I64"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I19"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I20"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I22"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I21"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="gnd_ana2"        cell = XSCI0CUTDSG place_status=placed indent=0 )
      (inst  name="I45"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I5"              cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I23"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I24"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I26"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I25"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )


      (keepclear begin = 1215.82 end = 1440.47)
)
(right
(locals ring_number=1 )
(keepclear begin = 5.53 end = 219.12)

      (inst  name="35_pad"  cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="36_pad"  cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="37_pad"  cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="38_pad"  cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="39_pad"  cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="40_pad"  cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="41_pad"  cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="42_pad"  cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="43_pad"  cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="44_pad"  cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="45_pad"  cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="46_pad"  cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )

(keepclear begin = 1294.82 end = 1519.47)
(locals ring_number=2 )
(keepclear begin = 84.53 end = 140.12)


      (inst  name="I66"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I35"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I34"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I33"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I32"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I31"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I30"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I29"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I28"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="gnd_io"          cell = GNDACUTD place_status=placed indent=0 )
      (inst  name="I15"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )
      (inst  name="I18"             cell = UMC18_IMEC_PAD_65x65_F_V1x0 place_status=placed indent=0 )


      (keepclear begin = 1215.82 end = 1440.47)
)
(topright
(locals ring_number=3 )
      (inst name = corner_1 orientation = r0 cell = CORNERD )
```

```
    )
    (topleft
    (locals ring_number=3 )
        (inst name = corner_2 orientation = r90 cell = CORNERD )
    )
    (bottomleft
    (locals ring_number=3 )
        (inst name = corner_3 orientation = r180 cell = CORNERD )
    )
    (bottomright
    (locals ring_number=3 )
        (inst name = corner_4 orientation = r270  cell = CORNERD )
    )
)
```

Appendix C

The following is the RTL implementation of the PMU design. The RTL has been synthesized using the standard library of 180nm UMC technology node.

```
Module
pmu(clk,V_measured,V_demanded,Ack,Output_Voltage,Reset,counter_en,Req,level_sh
ifters_reading,Output_Voltage_reading,PWM_DC);

input clk;
input [0:7] V_measured;
input [0:7] V_demanded;
input Ack;
input Output_Voltage;
input Reset;
output reg counter_en;
output reg Req;
output reg level_shifters_reading;
output reg Output_Voltage_reading;
output reg [0:7] PWM_DC;
reg tmp_0;
reg tmp_1;
reg tmp_2;
reg [0:7] In_Data;
reg [0:15] tmp;
reg Voltage_tmp;

always@(posedge clk)
  begin
       if (Reset == 0)
              begin
              Req <=0;
              counter_en <= 0;
              end
       else if (Ack == 1 && tmp_0 == 0 && counter_en == 1)
          begin
            tmp <= (V_demanded * tmp);
            level_shifters_reading <= 1;
            tmp_0 = 1;
            tmp_1 = 1;
            Output_Voltage_reading <= 0;
          end
       else if (Ack == 0 && Req == 0)
          begin
            tmp_0 = 0;
            Req <= 1;
            level_shifters_reading <= 0;
            Output_Voltage_reading <= 1; // to read the Voltage
            tmp_1 = 1;
            tmp_2 = 1;
            tmp <= PWM_DC;
           end
       else if (Ack == 0 && Req == 1 && tmp_2 == 1)
          begin
            Voltage_tmp <= Output_Voltage;
            tmp_2 = 0;
          end
       else if (Ack == 0 && Req == 1 && tmp_2 == 0 && Voltage_tmp == 1)
          begin
            counter_en <= 1;
          end

       else if (Ack == 0 && Req == 1 && Voltage_tmp == 0 && tmp_2 == 0)
```

```
          begin
            tmp_0 = 0;
            Req <= 0;
            counter_en <= 0;
            tmp <= 16'b0000000011111010;
            level_shifters_reading <= 0;
            Output_Voltage_reading <= 0;
            tmp_1 = 1;
            PWM_DC <= 250;
           end
       else if (level_shifters_reading == 1 && tmp_0 == 1 && tmp_1 == 0)
          begin
            if ((tmp / In_Data) > 255) PWM_DC <= 250;
            else PWM_DC <= (tmp / In_Data);
            Req <= 0;
            counter_en <= 0;
            tmp_0 = 0;
            level_shifters_reading <= 0;
            tmp <= PWM_DC;

           end

       else if (Ack == 1 && tmp_0 == 1 && Req == 1)
              begin
              In_Data = V_measured;
              tmp_1 = 0;
              end


  end
endmodule
```

The validation of the RTL implementation is fulfilled through the following test-bench:

```
module testbench();

reg clk;
reg [0:7] V_measured;
reg [0:7] V_demanded;
reg Ack;
reg Output_Voltage;
reg Reset;
wire Req;
wire level_shifters_reading;
wire Output_Voltage_reading;
wire [0:7] PWM_DC;
wire counter_en;

pmu inst_pmu
(.clk(clk),.V_measured(V_measured),.V_demanded(V_demanded),.Ack(Ack),.Output_V
oltage(Output_Voltage),.Reset(Reset),.counter_en(counter_en),.Req(Req),.level_
shifters_reading(level_shifters_reading),.Output_Voltage_reading(Output_Voltag
e_reading),.PWM_DC(PWM_DC));

initial
       begin
          $dumpfile("testbench.vcd");
          $dumpvars(0, pmu);
       end
initial
    begin
        clk = 0;
       forever #40 clk = ~clk;
    end
initial
   begin
```

```
       #0      Output_Voltage <= 0;
       #0      Ack <= 0;
       #0      Reset <= 0;
       #80    Reset <=1;
       #1000   Output_Voltage <= 1;
       #160   V_measured <= 8'b00000010;
       #0      V_demanded <= 8'b00110101;
       #800   Ack <= 1;
       #280    Ack <= 0;
       #160   V_measured <= 8'b01001100;
       #0      V_demanded <= 8'b00110101;
        #780  Ack <= 1;
       #260    Ack <= 0;
       #160   V_measured <= 8'b00111111;
       #0      V_demanded <= 8'b00110101;
      #780    Ack <= 1;
       #260    Ack <= 0;
       #160   V_measured <= 8'b00110101;
       #0      V_demanded <= 8'b00110101;
      #780    Ack <= 1;
       #260    Ack <= 0;
       #160   V_measured <= 8'b00101010;
       #0      V_demanded <= 8'b00110101;
      #780    Ack <= 1;
       #260    Ack <= 0;
       #160   V_measured <= 8'b00110101;
       #0      V_demanded <= 8'b00110101;
      #780    Ack <= 1;
       #260    Ack <= 0;

   end

always @(negedge clk)
 begin

       $monitor($time , " V_measured %d V_demanded %d clk %d Ack %d
Output_Voltage %d Reset %d Req %d level_shifters_reading %d
Output_Voltage_reading %d PWM_DC %b", V_measured, V_demanded, clk, Ack,
Output_Voltage, Reset, Req, level_shifters_reading,counter_en,
Output_Voltage_reading, PWM_DC);

 end

 initial
    begin
        #15000
        $finish;
    end
  endmodule
```