Reduction of Variable Speed Drive IGBT Switching Loss, Utilising the IGBT Gate Drive, Without Increasing Radio Frequency Radiated Emissions

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Abstract

Radio frequency radiated emission from a variable speed drive must be limited below defined limits to avoid interference with electronic equipment. It is possible to comply with the international standards however, the current state of the art methods such as large gate drive resistance and output filters significantly reduce the efficiency or increase the cost of the products. It is known that the main source of emissions emanate from the switching transients associated with the output power semiconductors, however the exact mechanisms and specific sources are unknown. This thesis examines the interaction of power devices during the switching transient identifying features which can be controlled by a sophisticated gate drive design. Analysis of the frequency content of the signals is presented together with methods to minimise power losses while maintaining compliance with radiated emission standards. A research program has been undertaken to identify the sources responsible for radiated emissions and predict a figure of merit as an indication of compliance. Measuring radio frequency content on high voltage and current signals is difficult and several techniques to accurately achieve this are presented. Simple passive gate drive solutions which can be easily implemented are examined along with a discussion on more complicated optimised solutions.

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List of Symbols

Symbol	Description
C_{ox}	Oxide capacitance per unit area
C_{ge}	Gate emitter capacitance
C_{gc}	Gate collector capacitance
D	Diffusion constant
E_C	Conduction band minimum energy
E_F	Fermi level energy
E_{on}	IGBT Turn on energy loss
E_m	Maximum electric field strength
E_{rr}	Reverse Recovery Energy
E_V	Valence band maximum energy
g_{fs}	Forward transconductance
I_c	Collector Current
I_F	Diode forward current
I_g	Gate current
I_{pk}	Peak current
I_{rr}	Reverse recovery current
k	Boltzmann's constant
L_{ch}	Length of channel
N_D	Donor ion concentration
Q	Electron charge
Q_{rf}	Diode depletion charge
Q_{rr}	Reverse recovery charge
Q_{rs}	Diode stored Charge
R_g	Gate resistor
T	Temperature
$T_{d.on}$	Turn on delay time
V_a	Avalanche breakdown voltage
V_{bi}	Built in voltage (pn junction)
V_{ce}	Collector emitter voltage
$V_{ce,sat}$	Collector emitter saturation voltage (when the device is turned on).
$V_{contact}$	Voltage drop due to semiconductor / metal contact resistance
V_{DC}	DC bus voltage
V_F	Diode forward voltage
V_{FRM}	Repetitive peak forward voltage
V_{ge}	Gate emitter voltage
$V_{gatePSU}$	Power supply voltage for gate drive
V_{GP}	Gate plateau voltage
V_t	Threshold Voltage
W	Depletion width

Symbol	Description
W_{n-}	Width of diode intrinsic region
W_{ch}	Width of channel
X	Electron affinity
Φ_m	Metal work function
α_{pnp}	Gain of pnp transistor
ε_s	Permittivity of semiconductor
μ_n	Electron mobility
τ	Carrier lifetime

List of Abbreviations

Abbreviations	Description
ac	Alternating current
AGD	Active Gate Drive
ARB	Arbitrary Waveform Generator
BJT	Bipolar Junction Transistor
CE	Conformité Européenne
CGD	Conventional Gate Drive
CISPR	Comité International Spécial des Perturbations Radioélectriques
CSTBT	Carrier Stored Trench Gate Bipolar Transistor
DAC	Digital to Analogue Converter
dc	Direct current
DCCT	Direct Current Current Transformer
DFT	Discrete Fourier Transform
DIGBT	Doubly Diffused Insulated Gate Bipolar Transistor
DVM	Digital Volt Meter
EM	Electromagnetic
EMC	Electromagnetic Compatibility
e.m.f	Electromotive Force
EMI	Electromagnetic Interference
EUT	Equipment Under Test
FPGA	Field Programmable Gate Array
FRED	Fast Recovery Epitaxial Diodes
FS	Field Stop
FWD	Free Wheel Diode
HF	High Frequency
HV PSU	High Voltage Power Supply
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
IPM	Intelligent Power Module
JFET	Junction Field Effect Transistor
LF	Low Frequency
MF	Medium Frequency
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOV	Metal Oxide Varistor
NPT	Non Punch Through
OATS	Open Area Test Site
PSU	Power Supply Unit
PT	Punch Through
QP	Quasi Peak
RE	Radiated Emissions
REFOM	Radiated Emissions Figure of Merit
RF	Radio Frequency
R.M.S	Root mean square
SMPS	Switched Mode Power Supply
SOA	Safe Operating Area
SOI	Silicon on Insulator
SVM	Space Vector Modulation
UHF	Ultra High Frequency
VHF	Very High Frequency
VSD	Variable Speed Drive

Chapter 1: Introduction

1.1 Power Losses and Radiated Emissions in a Variable Speed Drive

Variable speed drives (VSD) in industrial applications are used to convert energy from a fixed frequency ac mains supply to a variable output frequency for speed control of an electrical machine. Over the last few decades, the increase in the performance of the power transistors used to control the flow of power have led to smaller, more efficient devices. Increases in microprocessor technology have allowed faster data processing improving the ability to execute complex control algorithms and improve the dynamic performance and precision of machine control. With increasing acceptance of human induced climate change, users of VSDs demand more efficient products to reduce their carbon footprint while maintaining an acceptable cost of equipment. While advances in individual components have contributed to the improvement in efficiency, the entire VSD system must be considered as a whole to leverage commercial and environmental benefits to the customer [1].

Control Techniques Unidrive SP™ is a range of ac VSDs used for high performance industrial applications. The functional blocks within the VSD and system can be considered representative of a typical industrial VSD design and are illustrated in Figure 1-1. A three phase diode rectifier converts the sinusoidal mains voltages into a unipolar voltage which is then smoothed via the low pass LC filter to provide a smooth dc voltage. A switch mode power supply (SMPS) converts the rectified and smoothed dc voltage to appropriate voltage levels suitable for a microprocessor and digital control electronics. The control electronics provide the interface to the outside world receiving motion control demand signals and relaying confirmation of these operations. The full bridge output stage is also connected to the dc bus where switching signals, provided from the control circuitry and software, create switching patterns to shape the output voltages and currents to the motor. A cable containing three output phases, a safety earth and enclosed in a wire mesh shield connect the output of the VSD to a motor located at some application specific distance.

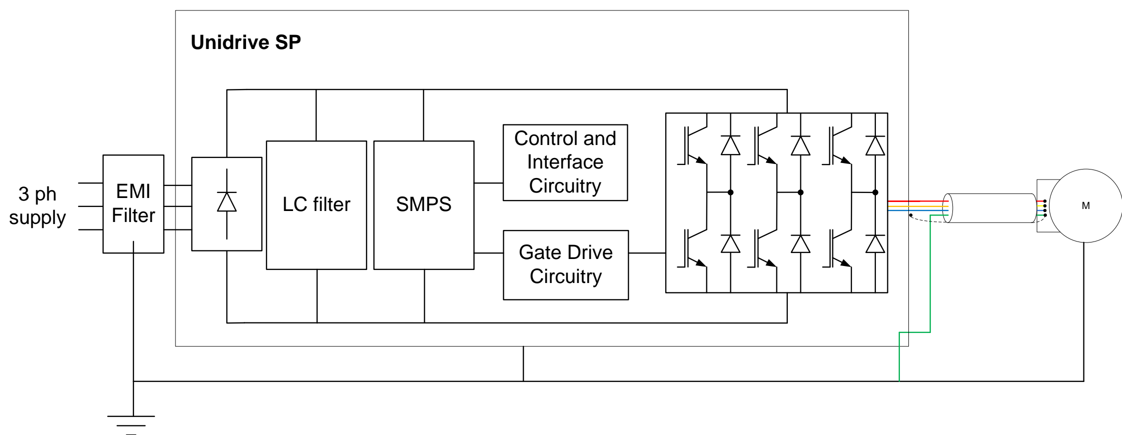


Figure 1-1: Block diagram representation of an ac-dc-ac VSD

There are several modulation techniques used to control the switches in the output bridge to achieve sinusoidal outputs with minimal distortion and the maximum possible root mean square (r.m.s.) voltage. For each case, when the required combination of insulated gate bipolar transistors (IGBTs) are switched on, the full dc bus voltage is applied to the terminals of the motor. The inductance of the motor windings causes the current to change at a relatively slow rate. When the desired current level has been achieved, the switches can be turned off. To achieve a high fidelity sinusoidal current waveform, the switching frequency of the IGBTs must be several multiples of the fundamental frequency of the output current. For the Unidrive SP™, the switching frequency can be selected from either: 3 kHz, 4 kHz, 6 kHz, 8 kHz or 12 kHz. During the transient switching action (for both on to off and off to on), the IGBTs momentarily support both the full output phase current and simultaneously the full dc bus voltage. Under these conditions, the power loss is very high and the resulting energy is dissipated as heat. When operating at the maximum switching frequency, there are 24000 pulses of energy loss per second for each IGBT and diode in the output bridge contributing up to 60% of the total energy loss of the VSD depending on operating conditions[1]. If the duration of each pulse can be minimised the total energy loss can be greatly reduced.

The switching action of these devices establishes electric and magnetic fields with spectrum extending into radio frequencies. These radio frequencies can interfere with

[1] Based on SPMD1404 operating at 6 kHz switching frequency.

components and circuits within the product itself or can be transmitted from the product into the environment causing non-intentional interference with other products. With the increasing use of electronics in an industrial environment for control and monitoring purposes, it is important that products do not interfere with the performance of neighbouring equipment in an unexpected manner. International technical standards have been introduced to define the acceptable level of power supply disturbance and radio frequency emissions which a product can emit, to which other products must be immune [2, 3].

The radio frequency spectrum has been classified into bands for use with communication equipment. The allowable level of unintentional signals are protected by national laws based on technical standards [4] which may be interpreted for specific products and environments. At low frequencies (30 kHz to 300 kHz), medium frequencies (300 kHz to 3 MHz) and high frequency (3 MHz to 30 MHz), the national grid system of power cables can operate as efficient antennas transmitting noise in these frequency ranges into the atmosphere [5]. It is not practical to take measurement of an individual product's emissions broadcast in this manner, however standards provide a test method to determine the voltage disturbance applied to the cables from an individual product. These are referred to as conducted emissions and the limits are defined over a frequency range of 150 kHz to 30 MHz. EMI filters can be designed to contain the common and differential mode currents, in this frequency range, within the VSD system and prevent conduction onto the mains supply. While the filter design is complex requiring a detailed knowledge of material properties of ferrites and capacitors over wide operating ranges, there are known procedures to design such systems at an acceptable cost. Above 30 MHz, (very high frequency (VHF), 30 - 300 MHz, ultra high frequency (UHF) (300 MHz to 3 GHz)) structures within VSD system including cables become efficient antennas and can radiate signals directly into the surrounding environment. Generic standards applicable to a commercial VSD define an acceptable limit to these radiated emissions [4, 6].

As part of a VSD development process, the product is tested for compliance with the standards to ensure suitability for CE (Conformité Européenne) marking allowing it to be placed for sale on the market in Europe. The VSD is installed in an open area test

site (OATS) in a manner representative of a customer installation with an electromagnetic interference (EMI) filter designed to suppress conducted emissions, communication cables and connections to a motor as described in the VSD installation manual. An antenna is located at a distance of 3 m from the equipment under test (EUT) and connected to a receiver. When the EUT is in its operating mode, the receiver software scans through the required frequency spectrum recording the measured electromagnetic field strength. When the VSD rotates a motor, a significant increase in broadband emissions above background noise can be measured over the range of 30 MHz to 100 MHz.

The current state of art method for reducing the measured emissions is to increase the switching time for the IGBTs by increasing the gate resistance or to add additional filters [7-9]. However, as described above, increasing the switching time results in an increase of power loss, reducing the system efficiency and the addition of filters adds cost and increases the physical size of the system.

It has been identified from work carried out at Control Techniques that different power semiconductor manufacturer's devices can have different levels of radio frequency (RF) emissions for the same switching period. From this observation, it can be deduced that the switching time may not be critical to the production of RF emissions but some less understood phenomenon.

1.2 Objectives of the Work

The main objective of this work is to provide an understanding of the linkages between the operation of power switching devices and the measured radiated emissions. From this understanding, the sources of the radio frequency emissions should be identified in time. The role and influence of the gate drive in generating the radio frequency content should be examined together with research into published gate drive control methods. A method to quantify measured radiated emissions across a wide frequency range is required and a comparison of measured electrical signals to radiated emissions limits defined in international standards is needed. A possible solution to improve the trade off between switching loss and radiated emissions is required which can be extended to

include a method to assess the physical construction of a VSD for its ability to suppress radiated emissions.

1.3 Overview of the Thesis

This thesis consists of seven chapters, the first, giving an introduction to the objectives of the research task and a brief outline of the contributions to knowledge and commercial benefits.

The research presented in chapter two gives background information to enable the reader to understand the problem in depth from several disciplines: power semiconductor physics; radio frequency engineering applied to a VSD system; and frequency analysis techniques for use at radio frequencies. The limitation to the control of radiated emissions in IGBT switching transients is presented.

In chapter three, a review of relevant published literature for gate driving techniques for IGBTs is researched. The merits of these solutions when applied to radiated emissions and variable speed drives is discussed and identifies a lack of specific material in this area.

Chapter four presents the practical application of the theory and determines the limits of common laboratory equipment for both measurement of radio frequency components within relatively high voltage and current switching signals. The impact of VSD construction with regards to its influence on the switching transients and hence radiated emissions is discussed.

Chapter five describes the evaluation of a simplified VSD system to determine the electrical sources responsible for the radio interference. Sophisticated hardware is developed to accurately control features in the switching transient at realistic operational speeds. The features of the switching signal responsible for the radiated emissions are identified and can be used to determine key parameters which can be controlled in a commercial product.

Chapter six describes how methods to measure and control radiated emissions in a simplified system can be applied to a more complex commercial VSD operating in an

industrial environment with the expected fluctuation in supply voltage, load current and temperature. The measurement techniques discussed in preceding chapters are implemented and evaluated to reduce the switch on energy loss while complying with international standards for radiated emissions.

Chapter seven summarises the work presented in this thesis giving conclusions. Further work is discussed regarding application of the techniques presented here to future semiconductor technologies such as wideband gap materials.

1.4 The Contribution to Knowledge

Throughout the research programme undertaken for the degree of Engineering Doctorate, several techniques have been used and discoveries identified which have not been published previously.

In this thesis:

- the dominant source of radiated emissions is found to be the RF content within the collector emitter voltage during the IGBT switching transient. In a commercial VSD system, this finding is expanded to include the voltage transient measured between the output phase and ground connection.
- the peak broadband emissions have been identified to occur at four specific points on the voltage waveform. The location of the peak emission changes with load current and VSD construction.
- it is found that the RF content in the IGBT collector current does not contribute to the measured radiated emissions.
- the influence of the bus bar impedance on the IGBT switching trajectory has been identified and the potential opportunities to reduce the switching loss are discussed.

A patent for design of gate drive circuitry has been filed (September 2012):

- “Selectable impedance gate drive.”

1.5 Commercial Benefits to Industry

This research project carried out offers commercial benefits to industry by:

- Improving VSD gate drive design which can offer an increase in product efficiency, (a valuable benchmark versus competitors).
- The increase in efficiency will offer a reduction in product size, which will reduce component costs and environmental impact through reduction in transported mass.
- An improved dynamic performance offered by operation of a VSD at a higher switching frequency can improve process control offering further efficiencies in the manufacturing industries.
- A reduction in switching losses can offer a reduction in thermal cycling of IGBTs giving a reduction in thermal fatigue increasing the useful lifetime of VSDs.
- A radiated emissions figure of merit (REFOM) has been found which can be used in a laboratory to understand the radiated emissions sources from a product reducing product development time.

Chapter 2: Key Principles

2.1 Introduction

This chapter describes the key principles which must be understood when considering the design of a gate drive circuit for low switching loss while considering the requirements for compliance to radiated emissions limits. The three main topics include:

1. Power Semiconductor Physics
2. Radiated Emission Sources
3. Frequency Analysis

The switching operation of an IGBT is far from ideal. The operation of the IGBT is highly dependent on the impedance of the gate drive circuitry, impedance of the power circuit, dc bus voltage, load current and temperature [1, 10-12]. To understand how these parameters effect the device operation, an understanding of the semiconductor physics for both the IGBT and diode is required. Developments in semiconductor technology have resulted in many competing technologies, each of which has benefits within a niche voltage or current rating. Section 2.2 will discuss the characteristics of IGBTs and diodes which are used in state of the art inverters. The theoretical design of the devices is discussed where they effect the electrical characteristics. The characteristics which can be influenced by gate drive circuit design, power circuit design and thermal performance where it relates to electrical characteristics and electromagnetic compatibility (EMC) are presented.

Research into electromagnetic (EM) field radiation has been extensive for many years since first described by Maxwell [13-15]. The majority of the research has focused on the use of EM waves for intentional transmission at specific frequencies where the impedance of cables, power supplies, antennas and the physical dimensions of antennas can be carefully designed to maximise their radiation efficiency [15-17]. The type of radio signals which radiate from a VSD are broadband in content and emanate from multiple sources, voltages and currents, and radiate in all directions [9]. Important information describing the potential radiated emission sources is presented in this chapter.

Radiated emissions are known to arise from the transient switching voltages and currents of the IGBTs [18]. The radio frequency content within these signals occurs for a short duration relative to the switching periods. Many published papers imply that an increase in switching time reduces the EMI emanating from a VSD [19, 20]. Analysis identifying the precise location in time of the radio frequency content and analytical methods to reduce the magnitude over the frequency range of interest is presented. The shape of a switching transient is considered for its radio frequency content.

2.2 Power Semiconductor Physics

The majority of power semiconductor components are constructed from high quality silicon dies. Research has been carried out into the use of alternative materials which offer superior characteristics such as silicon carbide and gallium nitride however at premium prices [21, 22]. This section of the thesis will only consider devices which are currently available and used for mass market industrial VSDs. The devices considered operate over a voltage range 600V to 2kV with a current rating up to 1000A.

2.2.1 Diodes

Diodes used in power electronics can be divided into two categories in terms of their semiconductor physics: the PIN diode and the Schottky diode. The PIN diode uses a pn junction to block reverse bias voltages. When conducting in the forwards direction, the current is carried across the pn junction by minority carriers (holes in the n-type material, electrons in the p-type material). The significance of this for power losses and for fast switching operation will be discussed in section 2.2.1.1. The Schottky diode losses increase with blocking voltage and is not normally used above 600 V when constructed from silicon. Power devices constructed from materials with higher avalanche voltages can utilise the Schottky diode construction up to higher voltages before the conduction losses prohibit this. These will not be discussed in detail in this thesis [21].

2.2.1.1 PIN Diode Structure

The silicon PIN diode is constructed with three distinct regions of doping. To enable electrical connections to the device, a layer of metal must be deposited on each end to form contacts (see Figure 2-1). The anode is heavily doped with acceptor ions to create

a p region which can create a low ohmic contact with the metal. This is important to reduce power loss when current flows through the device (the high doping concentration is denoted with "+"). For n-type material, the doping needs to be above 10^{19} cm^{-3} to achieve a low ohmic contact to the metallisation hence the inclusion of the n^+ region at the cathode [23]. Doping in the middle region of the diode is low (between 10^{15} to 10^{17} cm^{-3}) to support a high electric field and is denoted with "-".

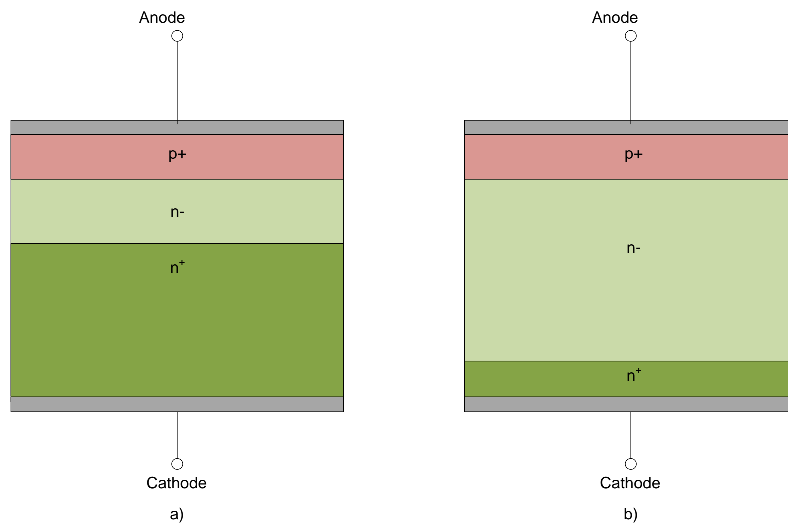


Figure 2-1: Structure of PIN diode a) Epitaxial diode; b) Diffused diode

The p^+n^- junction is responsible for supporting the reverse blocking voltage. The breakdown voltage can be increased by reducing the doping level in the n^- region (or drift layer). The avalanche breakdown voltage (V_a) indicates the point where static avalanche initialises and can be determined from equation (**2-1**) [24].

$$V_a = 5.34 \times 10^{13} \cdot N_D \qquad (2\text{-}1)$$

Where N_D is the doping concentration of donor ions in the n^- region.

At avalanche, the electrons are accelerated by the electric field with sufficient energy to excite an electron from the valence band into the conduction band generating an electron / hole pair. The new electrons and holes are also accelerated by the electric field causing the process to repeat. The electrons and holes contribute to the leakage current, increasing power dissipation in the diode which can lead to thermal destruction of the device [25].

When the p^+n junction is in high injection (discussed in section 2.2.1.4), the doping in the low doped n^- region does not contribute significantly to the charge balance i.e. the processes are the same as if this region is undoped. For this reason it is referred to as intrinsic hence the "i" in PIN.

The PIN diode can be constructed by two different methods depending on the blocking voltage required [26]. For low blocking voltages, the n^- region only needs to be a few μm thick and so can be grown epitaxially on n^+ substrate followed by a diffusion of acceptor ions to create the p^+ region. As the voltage requirements increase, it becomes more cost effective to begin with a n^- substrate then diffuse both the p^+ and n^+ region at each end.

2.2.1.2 Static Operation

2.2.1.2.1 Reverse Blocking

The PIN diode operates under reverse bias using the depletion region set up by the pn junction to support high blocking voltages [24]. As the reverse voltage is increased, the depletion width increases. The maximum electric field E_m in an abrupt pn junction is given by equation (2-2).

$$E_m = \sqrt{\frac{2qN_D V_a}{\varepsilon_s}} \qquad (2\text{-}2)$$

where:

- q is the electron charge;
- ε_s is the permittivity of the semiconductor.

As the applied reverse voltage is increased, the depletion region expands and hence the region supporting the electric field also expands with a triangular characteristic. This is referred to as a Non-Punch Through (NPT) diode and the maximum depletion width (W) for the device occurs at the avalanche voltage which is given by equation (2-3).

$$W = \sqrt{\frac{2\varepsilon_s V_a}{qN_D}} \quad (2\text{-}3)$$

If the electric field reaches the n^+ region before falling to zero, it reduces rapidly due to the high doping concentration giving an approximately trapezoidal electric field (see Figure 2-2). This is referred to as a Punch Through diode (PT). This is not strictly the correct terminology as the field does not reach another doping type however the title has generally been accepted [26].

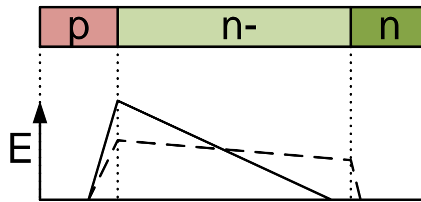


Figure 2-2: Electric field profile for NPT (solid) and PT (dashed)

In a PT device, the electric field strength can be reduced across the n^- drift region to a level which will not cause avalanche in the n^+ region. The electric field strength can then reduce over a short distance in the n^+ region allowing PT devices to be thinner for a given blocking voltage hence giving a lower forward voltage. However, that can lead to unwanted characteristics such as a snappy behaviour when switching (see section 2.2.1.4.3) [27]. This n^+ layer is often referred to as the buffer layer or field stop layer.

In practice the breakdown voltage at the edge of the component is lower than deep within the silicon. There are various physical methods used to raise this voltage to the one dimensional (1D) theoretical condition. Details of these will not be discussed further however they should be considered when modelling the device behaviour [24].

Datasheet values for reverse blocking capability are often quoted at 25°C. It is important to note that the breakdown voltage reduces by 1.5 V/K as less additional energy is required to excite the electron to the conduction band [24].

2.2.1.2.2 Forward Conduction

The PIN diode consists of two junctions (J1 and J2) that can be represented in an energy band diagram (Figure 2-3). Under forward bias conditions, holes are injected into the intrinsic region from the p^+ region and electrons are injected into the intrinsic region from the n^+ region. Assuming the junctions are ideal emitters (i.e. only holes cross J1 and only electrons cross J2) the holes and the electrons must recombine in the intrinsic region for current to flow.

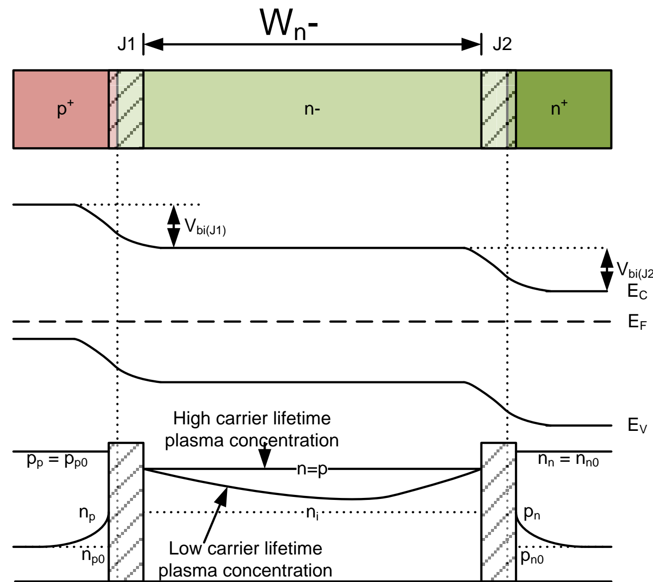


Figure 2-3: PIN diode band diagram and plasma concentration

The concentration of the charge carriers (holes and electrons) will exceed the low doping concentration of the drift region giving a quasi neutral mix of charged particles which is referred to as plasma. The voltage drop across the device when forward bias is given by equation (2-4). It can be seen that the voltage drop across the n- region adds to the total forward voltage hence the requirement for a thin drift region, particularly at high voltages.

$$V_F = V_{contact} + V_{J1} + V_{J2} + V_{n-} \qquad (2\text{-}4)$$

The forward voltage drop across the drift region (V_{n-}) is given in equation (2-5) which shows the dependence on the carrier lifetime (τ) and the width of the intrinsic region (W_{n-}) as determined for the required blocking voltage, where τ should be large to reduce

V_{n-}. For a short carrier lifetime, the holes and electrons recombine after a short distance giving a catenary distribution.

$$V_{n-} = \frac{3\pi kT}{8q} e^{\frac{W_{n-}}{\sqrt{D\tau}}} \quad (2\text{-}5)$$

where:

- k is Boltzmann's constant
- T is the Temperature
- D is the diffusion constant for silicon

2.2.1.3 PIN Diode Applications

For a VSD output bridge and SMPS applications, the conduction loss is an important factor and hence a high plasma concentration is required to reduce the resistance. However as the switching frequency increases, the switching losses both in the diode and IGBT or metal oxide semiconductor field effect transistor (MOSFET) tend to dominate. For these applications, the designed plasma concentration is a compromise between conduction loss and switching loss [11, 28, 29]. These diodes are often referred to as fast recovery epitaxial diodes (FRED). When switching these devices rapidly, there are other interesting characteristics which must be considered.

In an effort to reduce the plasma concentration, the carrier lifetime can be altered by irradiating a diode with high energy particles, proton and helium implantation or heavy metal diffusion such as platinum or gold [27, 30]. The plasma concentration can be shaped along the length of the diode by controlling the implantation energy to achieve the required depth of diffusion.

2.2.1.4 PIN Diode Switching Characteristics

2.2.1.4.1 Switch On

When the diode begins to switch on, the voltage across it must first increase to the repetitive peak forward voltage (V_{FRM}) before falling to V_F (see Figure 2-4). V_{FRM} is a function of the rate of change of current (di/dt) and can be greater than 100 times V_F [26]. This voltage overshoot also adds to the voltage stress on the switching device

(IGBT) which is conducting the full load current during this instant. This voltage stress is in addition to the parasitic inductance voltage drops and can be difficult to measure from a module unless direct probing of the diode contacts can be achieved.

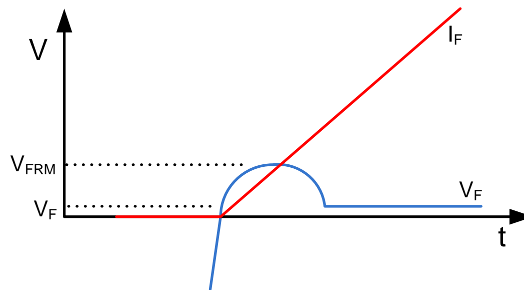


Figure 2-4: Diode switch on waveform.

When the diode becomes forward biased, the forward voltage has to overcome the resistance of the n^- region while the plasma is forming. This voltage peak becomes more significant on high voltage components as the volume of plasma is larger [26].

2.2.1.4.2 Switch Off

During switch off of the diode, the holes and electrons in the plasma recombine or are swept from both ends by a reverse recovery current (I_{rr}). The diode can only begin to support the voltage when the plasma concentration reaches zero at one end of the n^- region allowing a depletion layer to form. The stored charge in the diode can be considered in two distinct regions which can be observed as the diode switches off. The total charge swept out by the reverse current is commonly referred to as reverse recovery charge (Q_{rr}). The diode stored charge (Q_{rs}) or excess plasma must be removed to the point where the depletion layer just forms. The charge that continues to be swept out of the diode to allow the depletion layer to expand is referred to as the diode depletion charge (Q_{rf}) [11]. The rate of change of voltage (dV/dt) of the diode is determined by the concentration profile of Q_{rf} throughout the n^- region, the rate of recombination, and the rate at which the charge carriers are swept out by load current.

In Semikron publications [26, 27], reference is made to a softness factor to characterise the reverse recovery current of a diode (see Figure 2-5 and equation (**2-6**)), however values for this softness factor are not published in their data sheets. This could be a

useful figure however, it would have to include a plot of softness factor versus di/dt and given for a range of temperatures and load currents for a circuit designer to be able to apply to new designs.

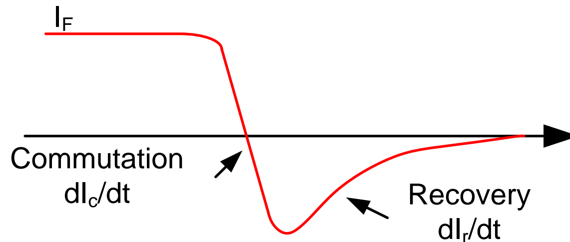


Figure 2-5: Soft Recovery PIN diode (softness factor S)

$$S = \left| \frac{-\frac{dI_c}{dt}|I = 0|}{\left(\frac{dI_r}{dt}\right)\max} \right| \quad (2\text{-}6)$$

A diode is considered to be a hard recovery diode if the rate of change of commutation current (dI_c/dt) is less than half of the rate of change in recovery current (dI_r/dt) otherwise it is referred to as a soft recovery diode. For a given stored charge the peak reverse recovery current (I_{rr}) is proportional to di/dt.

2.2.1.4.3 Snap-Off

During switch off, it is possible to have very fast current transients during the reverse recovery period. This will depend on operating conditions and diode characteristics. The high current transients have been blamed for increasing electromagnetic emissions and so diodes should be designed to avoid operating in this area [31, 32]. This very fast recovery is referred to as snap-off and can result from three different conditions within the diode. The plasma and associated waveforms are illustrated in Figure 2-6.

There are three different positions in the recovery tail where snap-off can occur leading to a different characteristic waveform [11, 27]:

- **Type 1:** A shallow plasma in the middle of the n^- region can give a snap-off soon after the peak reverse recovery current.

- **Type 2:** An insufficient thickness of the diode n$^-$ region may result in snap-off towards the end of the switch off period.
- **Type 3:** An excessively strong anode emitter and/or weak cathode emitter may lead to snap-off in the middle phase of the switch off process.

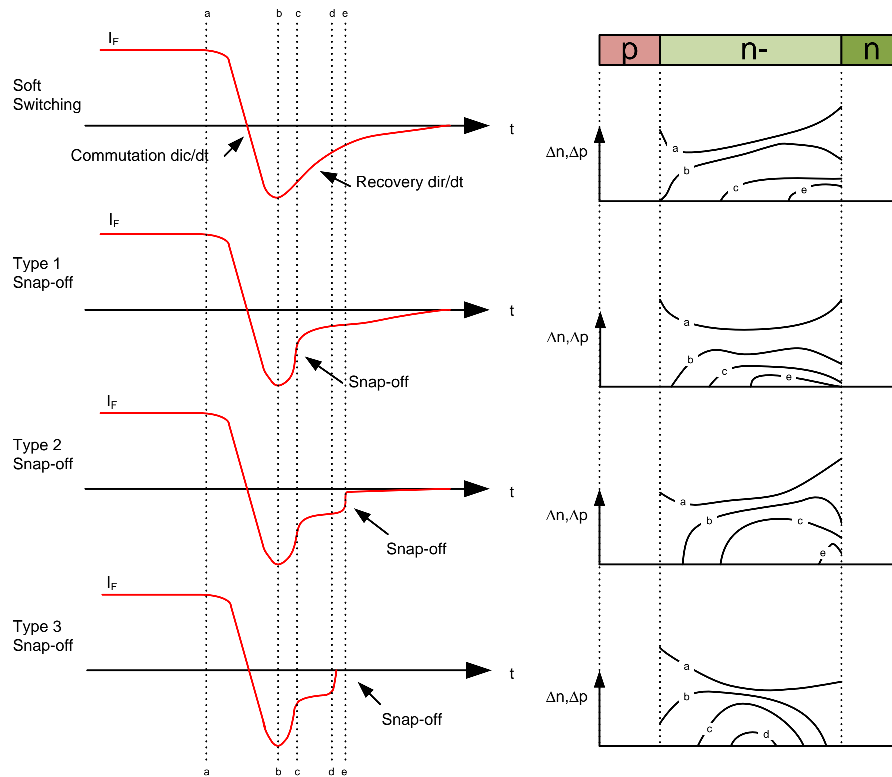


Figure 2-6: PIN diode plasma concentration during snap-off for different types of diodes

There are various operating condition which can increase the chance of snap-off [11]:

- The carrier lifetime hence plasma concentration is a function of temperature. At low temperature, the carrier lifetime is shorter hence the diode can become more snappy. This condition would typically be observed as type 1.
- At a low forward current, the plasma concentration is low resulting in snappy behaviour (type 2).
- At high dc bus voltage, the diode appears thinner because the depletion layer expands much faster increasing the risk of snap-off in the tail (type 3).

- High di/dt extracts the excess charge rapidly. An initially low plasma concentration in the middle region will result in a snap off after the current peak (type 1).

2.2.2 IGBT

The IGBT combines the high current and voltage capability of the bipolar junction transistor (BJT) with the high input impedance of the MOSFET in a single device. It has been assumed that a PIN diode has been used in the switching waveforms presented in this chapter unless otherwise stated.

2.2.2.1 Device Structure

The structure of an IGBT can be split into two different regions, the gate region and the high power region. For the following description of the device structure and operation, the planar gate structure, Non-Punch Through technology is used. This is extended in section 2.2.2.2 to include specific features which are used to customise the device depending on the application.

The structure of the IGBT is shown in Figure 2-7. Areas which have characteristics similar to simpler devices have been indicated as these will aid the description of device operation. The n-channel MOSFET has been identified as the small area under the emitter contact and the polysilicon / oxide gate. The n region under the emitter is highly doped to give a good ohmic contact to the emitter terminal. This forms the source of the MOSFET. The surrounding p region, referred to as the p-base, is usually the substrate or body in a MOSFET device. The p-base region is also connected to the emitter terminal allowing the gate voltage to be referenced to the emitter creating a MOS junction. The application of a positive voltage to the polysilicon gate, relative to the p-base attracts electrons towards the gate which collect below the insulating oxide layer. When the concentration of free electrons in a very thin layer under the gate, is greater than the p-base doping concentration, this is called an inversion layer or channel.

The n^- drift region forms the drain of the MOSFET. When the drain is positively biased relative to the source and the inversion layer has formed, a current of majority carriers (electrons) will flow along the channel into the drain.

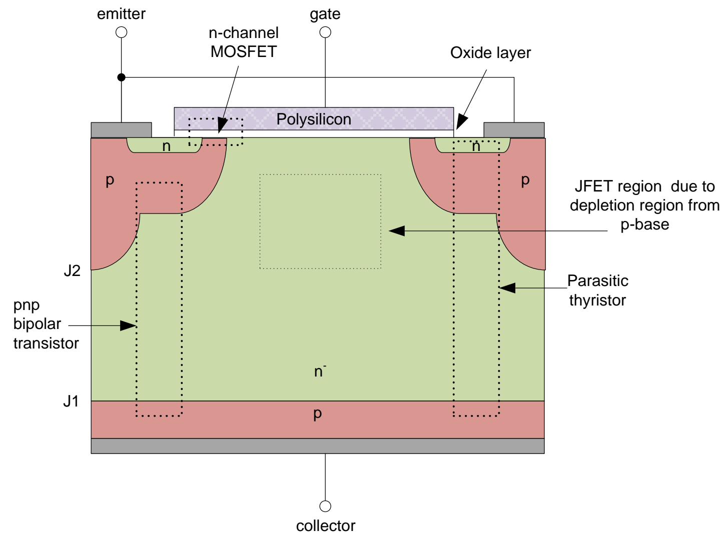


Figure 2-7: Planar gate, Non-Punch Through IGBT structure

The pnp transistor consists of the p layer at the IGBT collector, n^-drift layer and p-base layer connected to the IGBT emitter. From the semiconductor point of view, the terminals of this device have been labelled incorrectly. The emitter of the pnp transistor is actually the labelled as the collector of the IGBT and likewise for the pnp collector [11].

The JFET (junction field effect transistor) region is formed by adjacent cells in the drift region. The depletion layer around the p-base acts to pinch off the current flowing from the channel and increases the IGBT resistance. This effect increases as the cell density increases [11].

The npnp structure is often referred to as a parasitic thyristor. The thyristor is normally in its blocking condition and hence does not influence the device performance. The p-base region of the IGBT forms part of the gate which is shorted to its cathode via the IGBT emitter terminal and remains off. Under conditions with high current densities or fast transients, a voltage drop across the p region can occur causing the thyristor to latch on. The thyristor will remain in the conducting state until the voltage across the IGBT is reversed. In most hard switched IGBT applications, this voltage across the device will not be reversed hence the latched IGBT leads to thermal runaway and device destruction.

Unlike a MOSFET, there is no reverse conducting path through an IGBT due to the p layer at the collector. A separate freewheeling diode is always used in parallel to the IGBT for this purpose.

The IGBT structure as shown in Figure 2-7 is a single unit cell. This pattern is repeated many times throughout a single chip. The number of unit cells hence area of the chip is determined by the required current. The thickness of the device determines the blocking voltage in a similar manner to the PIN diode.

The planar gate structure is often referred to as a DIGBT. This is in reference to the construction techniques of double diffusing first the p-base followed by the n+ region to form the gate structure [33].

2.2.2.2 Evolution of Device Structure

As IGBT technology and manufacturing capabilities have progressed, there have been several distinct changes to the device structures. This section will discuss these improvements, associated electrical characteristics and applications.

Competition between manufacturers has led to a proliferation of marketing terms to describe variants of IGBT structure [34]. The various names will be mentioned throughout this section.

Non-Punch-Through

The structure of the Non-Punch-Through IGBT has been described previously. As manufacturing processes improve, the capability to manufacture thinner chips has led to a reduction in forward voltage drop for a given blocking voltage as illustrated in Figure 2-8. Enhancing the emitter efficiency (ratio of minority carrier current to total diffusion current crossing pn junction) of the p-emitter, has also reduced the on state voltage however this can lead to increase the switch off losses [35].

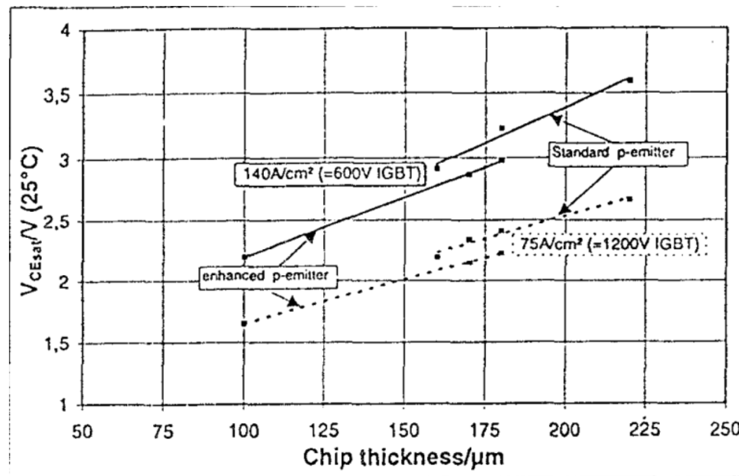


Figure 2-8: Reduction in V_{ce} with chip thickness [35]

2.2.2.2.1 Punch Through (Field Stop)

The Punch Through IGBTs have an additional n^+ layer included in the device structure between the n^- drift and the p collector (see Figure 2-9). This layer can be called a buffer layer or field stop layer. Depending on the IGBT manufacturer, the device technology may be promoted as either Punch Through (PT) or Field Stop (FS) [36].

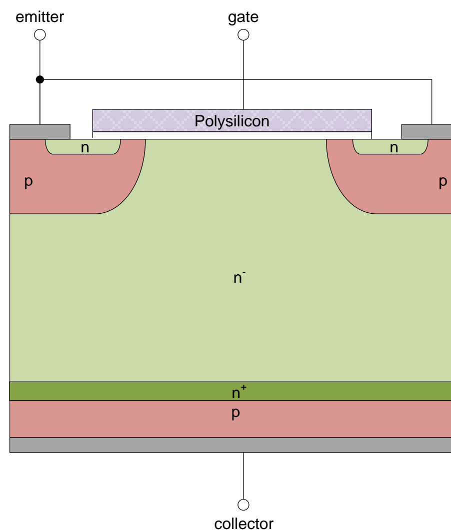


Figure 2-9: Planar Gate, Punch Through IGBT structure

The Non-Punch Through device is symmetrical i.e. the device can block both forward and reverse voltage. With the addition of the n^+ buffer layer, the PT devices have reduced capability to block reverse voltages (reverse blocking of tens of volts for a

1200V device) [37]. Many circuit applications do not require the IGBT to block reverse voltages so this has not proven to be a commercial obstacle.

The benefits for the n^+ buffer layer are exposed when considering the forward blocking voltage. In the same manner as the PIN diode, the electric field is dropped across the n^- drift region to a level where the n^+ buffer layer can safely reduce the field in a shorter distance [38]. Using Punch Through technology allows the use of thinner devices for a given voltage rating compared to Non-Punch Through. The thinner device reduces the forward voltage drop hence reduces the conduction losses.

One of the advantages of the Punch Through device is the reduction in tail current if the electric field reaches the n^+ buffer layer during switch off. At high operating voltages, the tail current can become insignificant [36]. Depending on the resistivity of the drift region, the collector-emitter voltage at which the electric field reaches the Field Stop layer can be chosen by the device manufacturer for optimum performance. When using these devices, it may be advantageous to have a gate driver circuit and PIN diode which causes an intentional voltage overshoot up to the device rating during switch-off to minimise power loss. No work has been published in this area.

With the reduction of device thickness for a given voltage, the total plasma is lower in the PT device compared to the NPT. For high voltages devices, this gives a reduction in switching losses for similar operating conditions.

Switch off losses in a PT device increase with temperature and are more sensitive to junction temperature than NPT. PT have a small positive temperature coefficient [39] but this is less than the NPT. Care should be taken if short circuit conditions are likely to occur as thermal runaway occurs at a lower temperature in PT devices compared to NPT devices.

2.2.2.2.2 Trench Gate Devices

The use of a trench gate eliminates the problems associated with the restricted JFET region in the IGBT. A deep channel is etched into the device substrate which is then passivated with an oxide layer and filled with the polysilicon which will form the gate. The processing involved to construct the deep trench can be time consuming and hence

expensive. A typical trench gate structure is shown in Figure 2-10. When a positive bias is applied to the gate, a vertical inversion layer (channel) forms through the p-base allowing conduction.

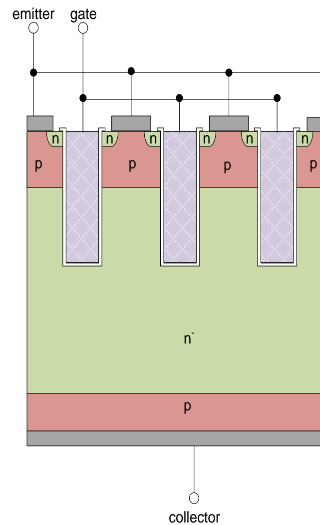


Figure 2-10: Trench Gate, Non-Punch Through IGBT structure

The trench gate structure can be constructed with a tighter cell pitch compared to the planar structure. This allows a higher current density and gives a lower $V_{ce(sat)}$ voltage drop for a given area reducing the conduction losses compared to the planar device.

During early development of the trench gate, there were three disadvantages of this structure [40]:

- Excessive over-current under short circuit conditions;
- Low yield due to complex processing (1998);
- Poor oxide reliability especially at high voltages [39].

Due to the lower $V_{ce(sat)}$ and higher cell density in the planar structure, the transconductance of the device is higher. The short circuit ruggedness is inversely proportional to the peak short circuit current [41]. The trench IGBT has more channel width due to smaller cell pitch resulting in higher peak current therefore lower short circuit withstand time.

2.2.2.2.3 CSTBT

In an effort to reduce conduction loss, a new concept structure was published in 1996 which is now available as a commercial product. The carrier stored trench gate bipolar transistor (CSTBT) is similar to a PT trench gate however it includes an n^+ layer between the p base and drift region (see Figure 2-11). This n^+ layer restricts the hole current through the device causing it to accumulate in the drift region. The accumulation of holes adds to the plasma and lowers the resistance. Forward voltage has been claimed to be reduced by 25% for the same switching loss as a trench gate device [42].

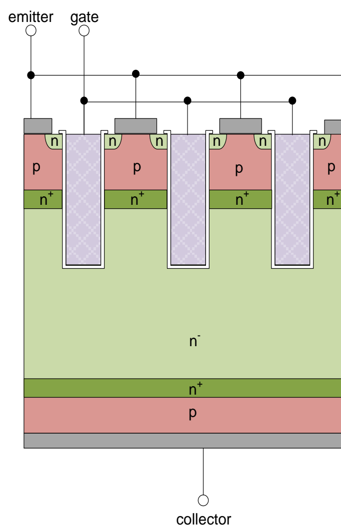


Figure 2-11: Structure of CSTBT

2.2.2.3 Operation

2.2.2.3.1 Forward Blocking

When the gate emitter voltage (V_{ge}) is held below the threshold voltage (V_t) the channel inversion layer cannot form. A forward bias applied to the IGBT is blocked by the pn junction between the p-base and n^- drift layer (J2) (see Figure 2-7) and is determined by the open base breakdown voltage of the internal pnp BJT [43]. To achieve high blocking voltage IGBTs, the n^- drift layer can be increased in thickness and the doping reduced to support the electric field.

2.2.2.3.2 Forward Conduction

If a positive bias is applied across the gate emitter exceeding V_t, an inversion layer forms allowing the flow of current. The collector emitter forward voltage has to be increased to exceed the built-in voltage of the pn junction at J1 before current will flow through the device [28]. This is illustrated in Figure 2-12.

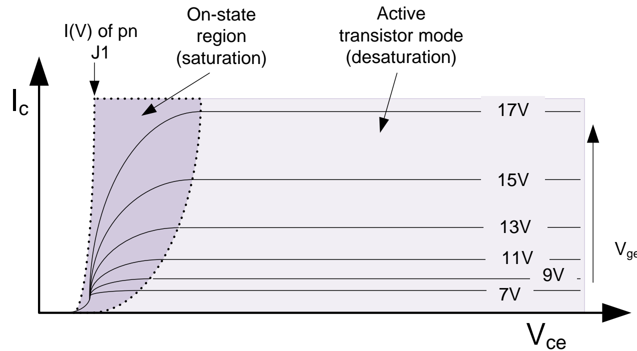


Figure 2-12: IGBT forward characteristics

When the IGBT is forward conducting, an electron current flows from the IGBT emitter, through the MOS channel into the drift region. This electron current supplies the base current to the internal pnp structure. By applying a higher gate voltage, more electron current can flow allowing a lower V_{ce} for a given collector current. The electrons in the drift region cause the base emitter (J1) of the pnp to be forward biased allowing holes to be injected into the drift region from the IGBT collector (pnp emitter). These holes are then swept into the collector of the pnp transistor allowing current conduction to take place. The mixture of holes and electrons in the drift region is referred to as plasma and functions in a similar way to a PIN diode.

As for the PIN diode, the need for low conduction loss has to be balanced with the need to both supply and extract the plasma quickly during switching (see Figure 2-13) [34]. The carrier lifetime profile can be adjusted throughout the IGBT drift region to achieve the optimum operating point for the application. The operating point for the device will depend on the switching frequency, operating voltage and load current of the application.

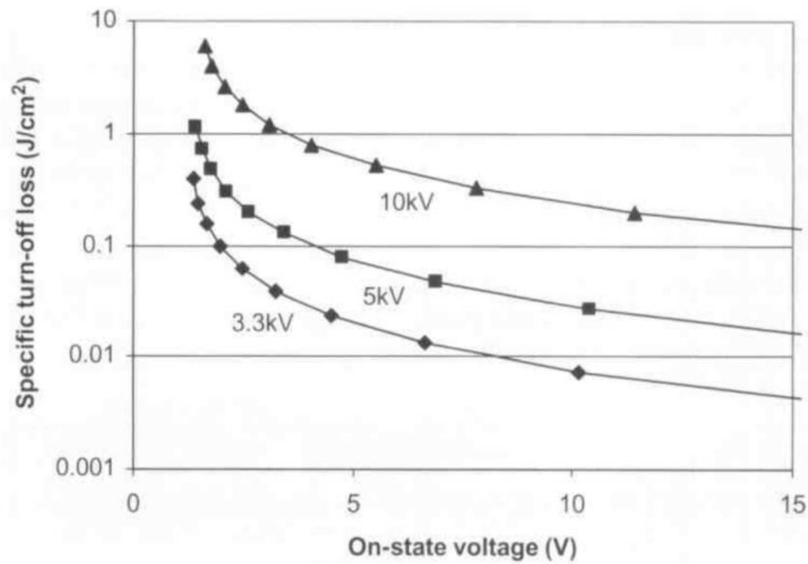


Figure 2-13: Example curve illustrating trade off between switching and conduction loss [34]

2.2.3 Device Switching Characteristics

2.2.3.1 Switch On

The switching characteristics of the IGBT depend on the circuit in which they are used. To gain an initial understanding of the mechanisms, a typical test circuit is presented (see Figure 2-14). The load is purely inductive and is in parallel with a freewheeling PIN diode. Several authors have given a description of the switching mechanism and the most complete is found in [27].

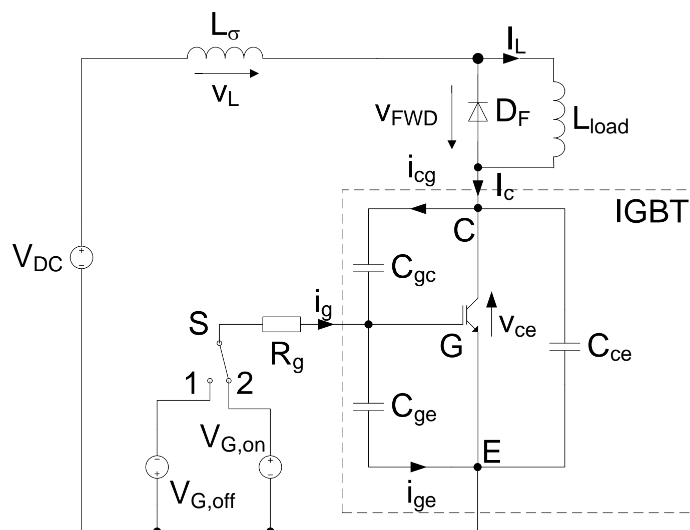


Figure 2-14: IGBT pulse test circuit

For the following switching patterns, a quasi-stationary model is used [27]. This assumes that the plasma and the space charge regions react quickly enough to assume their steady state at any instant during the switching transients. The voltage and current waveforms for switch on are shown in Figure 2-15.

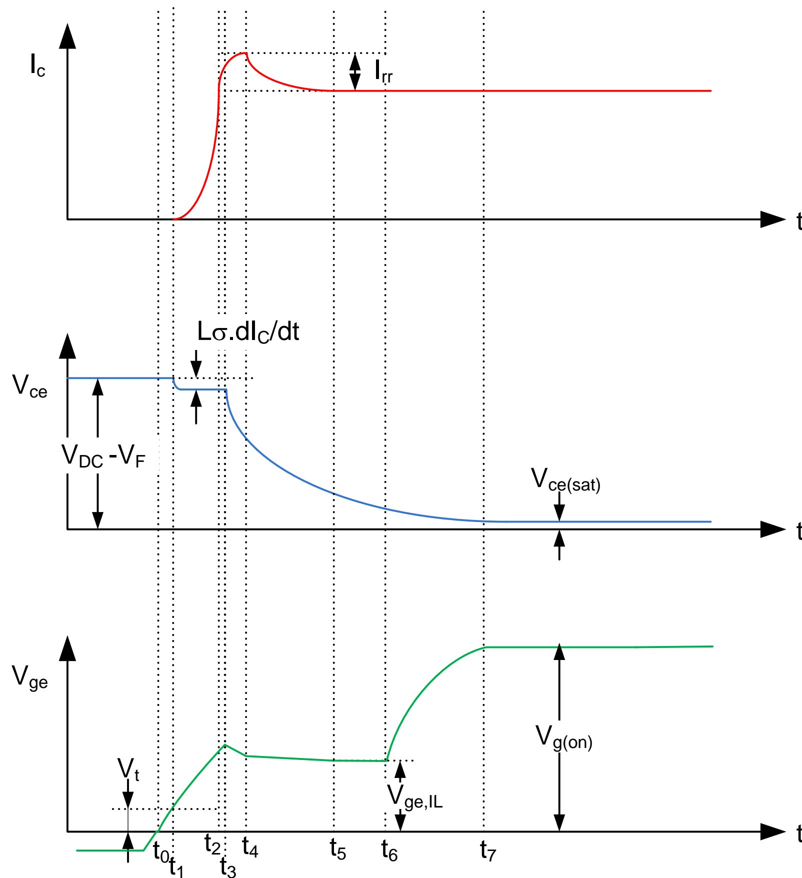


Figure 2-15: IGBT switch-on waveforms with a bipolar diode

Phase 1 (t_0 to t_1): At time t_0, the demanded gate voltage is increased from a negative value (usually -6V) to a positive value (+15V) and in represented in the diagram by the ideal switch S which is thrown to position 2 to begin to charge the gate capacitance (C_{ge}) via the gate resistor R_g. As V_{ge} increases, the MOS junction creates and expands a depletion layer in the p-base region under the oxide, which, with further voltage increase forms an inversion layer. Electrons can only pass through the inversion layer once established hence the pnp transistor cannot switch on until after this threshold voltage is reached.

The gate current I_g flowing through the gate resistor charges the input capacitance C_{ge} and begins to discharge C_{gc}. The rate of charge is determined by the series combination of the capacitance and the gate resistor. This gate voltage at any point up to t_1 can be calculated using equation (2-7).

$$V_{ge}(t) = V_{G.on}\left(1 - \exp\left(-\frac{t}{\tau_1}\right)\right) \qquad (2\text{-}7)$$

where:

$$\tau_1 = R_g.(C_{ge} + C_{gc}) \qquad (2\text{-}8)$$

By rearranging equation (2-7), the time between the operation of switch S and the inception of the collector current is known as the switch-on delay time $t_{d.on}$ and is given by equation (2-9).

$$t_{d.on} = -\tau_1.\ln\left[1 - \frac{V_t}{V_{g_on}}\right] \qquad (2\text{-}9)$$

Phase 2 (t_1 to t_2): At t_1, V_{ge} exceeds the threshold voltage, V_t, electrons begin to flow through the MOS channel into the n^- region. As this is the base of the pnp transistor, the emitter of the pnp (collector of IGBT) injects holes into the n^- region causing current (I_c) to flow through the IGBT.

The gain (α_{pnp}) of the transistor in power IGBTs is very low, and as a result, the rise in collector current after t_1 is closely related to the rise of the current in the MOS transistor. Using the assumption that the IGBT's collector current is approximately equal to the MOS current, the power MOSFET's equations for the current rise related to the gate voltage can be applied [27].

The freewheeling diode D_F remains forward biased until I_c reaches the value of the load current in the inductor (since $I_F = I_L - I_c$) hence the voltage across the diode remains positive holding the load voltage to the positive dc bus. The rapid change in current due to commutation causes voltage drops in the parasitic inductances in the circuit such as the device bond wires and bus bar as seen in Figure 2-15. The voltage across the IGBT

can be calculated from equation (2-10). For the circuit setup as shown in Figure 2-14, the voltage drop across the diode would increase the voltage across the IGBT.

$$V_{ce} = V_{DC} + V_F - L\frac{dI_c}{dt} \tag{2-10}$$

It is important at this stage to understand how the drop in the voltage due to the parasitic inductance can reduce the ability to control the switch-on dI_c/dt. This can be examined by looking at the current through the gate collector capacitor as shown in equation (2-11).

$$i_g = \left(C_{gc} + V_{cg} \frac{dC_{gc}}{dV_{cg}} \right) \cdot \frac{dV_{cg}}{dt} \tag{2-11}$$

C_{gc} is related to the depletion layer within the IGBT, where the capacitance will increase with decreasing voltage [44]. As a result, the required discharge current I_g will change as a function of the change of V_{gc}. The gate current I_g is determined by the voltage drop across the gate resistor (2-12), hence a reduction in I_g will lead to an increase in current flow into the C_{ge} which would increase dV_{ge}/dt increasing the dI_c/dt acting as a positive feedback loop [45]. The parameters of this feedback loop are dependent on the IGBT construction including the relative size of parasitic capacitors C_{gc} and C_{ge} [46]. This effect can result in a loss of control of dI_c/dt from the gate drive. One method to reduce the impact of this is to add additional capacitance across the gate emitter [27]. This larger capacitance would absorb I_g minimising the increase in V_{ge}.

$$i_g = \frac{\left(V_{g,on} - V_{ge}\right)}{R_g} \tag{2-12}$$

Phase 3 and 4 (t_2 to t_4): At t_2, the collector current I_c equals I_L, and the current through the freewheeling diode, D_F, has reduced to zero. The PIN diode cannot support the reverse voltage until the plasma has recombined or been swept out. The current in the diode continues to fall with the same di/dt, flowing in a negative direction. At t_3, when Q_{rs} has been swept from the PIN diode the depletion layer begins to form at the pn

junction, the diode can then begin to block the voltage while Q_{rf} continues to be removed.

The voltage across the IGBT decreases at the same rate as the diode blocks the voltage. In the IGBT, C_{gc} is further discharged by the falling voltage, however, the reduction in collector emitter voltage reduces the depletion width. The depletion can be thought of as a parallel plate capacitor, and as the depletion width reduces, the capacitance increases. The current which flows from C_{gc} is drawn from both the gate supply and also from C_{ge} (see Figure 2-16). The result of pulling current from C_{ge} is a reduced V_{ge}, leaving a small peak in the V_{ge} waveform and holding the IGBT in the active region. The reduction in V_{ge} reduces the maximum collector current restricting and delaying the removal of the reverse recovery charge.

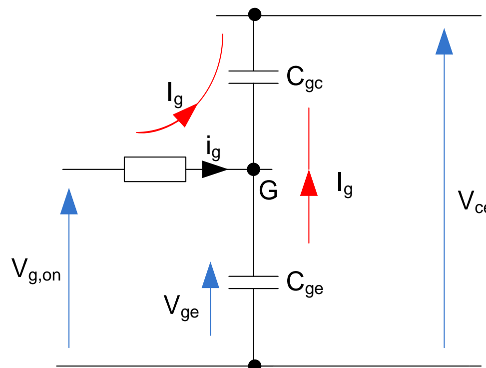


Figure 2-16: Current flow in IGBT internal capacitance when V_{ce} falls

Phase 5 and 6 (t_4 to t_6): After t_4, the gate emitter voltage will continuously re-adjust to the falling reverse-recovery current of D_F. This change is not always easy to see as V_{ge} is proportional to the square root of collector current. The rate of change of V_{ce} is limited by the slowest of either the charging of C_{gc} with the gate current or the discharging of the diode by the reverse recovery current.

At t_5, the diode tail current has fallen to zero and hence the gate voltage remains at a stable voltage which allows the IGBT to deliver the load current I_L. The gate-emitter voltage can be calculated based on the load current using equation (2-13) [27]. This has been simplified in equation (2-14) to emphasise the relationship between the collector current and the gate emitter voltage.

$$V_{ge,IL} \cong V_t + \sqrt{\frac{I_c \cdot L_{ch}}{W_{ch}} \cdot \frac{2}{C_{ox}} \cdot \frac{1-\alpha_{pnp}}{\mu_n}} \quad (2\text{-}13)$$

$$I_c = \frac{K}{(1-\alpha_{pnp})} .(V_{ge} - V_t)^2 \quad (2\text{-}14)$$

Where:

- μ_n is electron mobility;
- C_{ox} is the gate oxide capacitance;
- L_{ch} is the channel length;
- V_t is the gate threshold voltage;
- V_{ge} is the gate emitter voltage;
- K is a constant;
- α_{pnp} is the gain of the IGBT pnp transistor.

Since V_{ge} remains almost constant during the time interval t_4-t_6, we can conclude that virtually all of the gate current I_g flows into the gate collector capacitance C_{ge}. In considering this, it is possible to see how the gate current I_g can be used to control the V_{ce} transient. The maximum limit to the dV_{ce}/dt will be set by the diode reaching dynamic avalanche. It is important to remember that C_{gc} continuously changes with voltage. With conventional gate drives, this leads to a parabolic reduction in V_{ce}.

Phase 7 (t_6 to t_7): at t_6, V_{ce} has dropped to the level where the IGBT changes from the active transistor mode (desaturation) to the saturation region. In this mode, V_{ge} is no longer related to the load current however, V_{ce} is strongly dependant on V_{ge} as more base current can flow into the pnp transistor. In an effort to minimise the conduction losses, the level of $V_{ge,on}$, should be chosen to be as high as possible while considering the short circuit protection. The time taken to reach the $V_{ge,on}$ is determined by the time constant τ_2 as shown in equation (2-15). It should be noted that the capacitances C_{gc} and C_{ge} have now increased compared to those used for time constant τ_1 due to the change in V_{ce}. The switching process is finished when V_{ce} has reached $V_{ce,sat}$.

$$\tau_2 = R_g \cdot (C_{ge} + C_{gc}) \qquad (2\text{-}15)$$

Figure 2-17 shows the switching trajectory taken on a $I_c(V_{ce})$ characteristic curve. This indicates how the load current changes with V_{ge} (quadratic relationship as expected from equation (2-13)). It is obvious that the highest current achieved during switch on is related to the reverse recovery current. It is important that the entire trajectory is within the IGBT safe operating area (SOA).

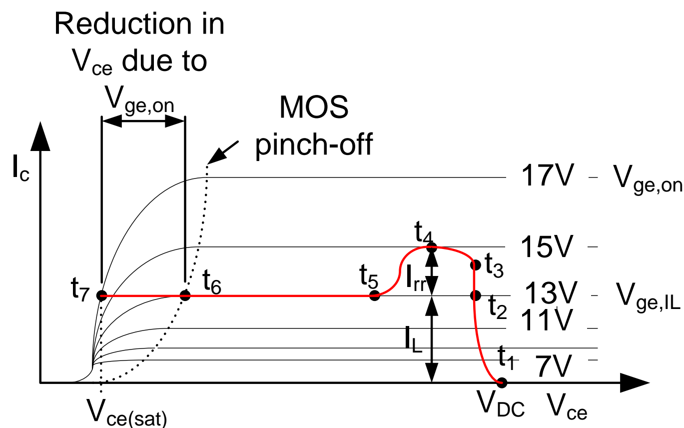


Figure 2-17: $I_c(V_{ce})$ characteristic curve for switch on.

2.2.3.2 Switch off

To analyse the switch off waveforms, the same test circuit as shown in Figure 2-14 is used. Initially, it is assumed that the load current is flowing through the inductor and the IGBT. At time t_0, the demand voltage is reduced to a low value (usually -6V) represent here by switch S thrown to the off position where it is assumed that $V_{ge,off}$ is negative. The waveforms are shown in Figure 2-18.

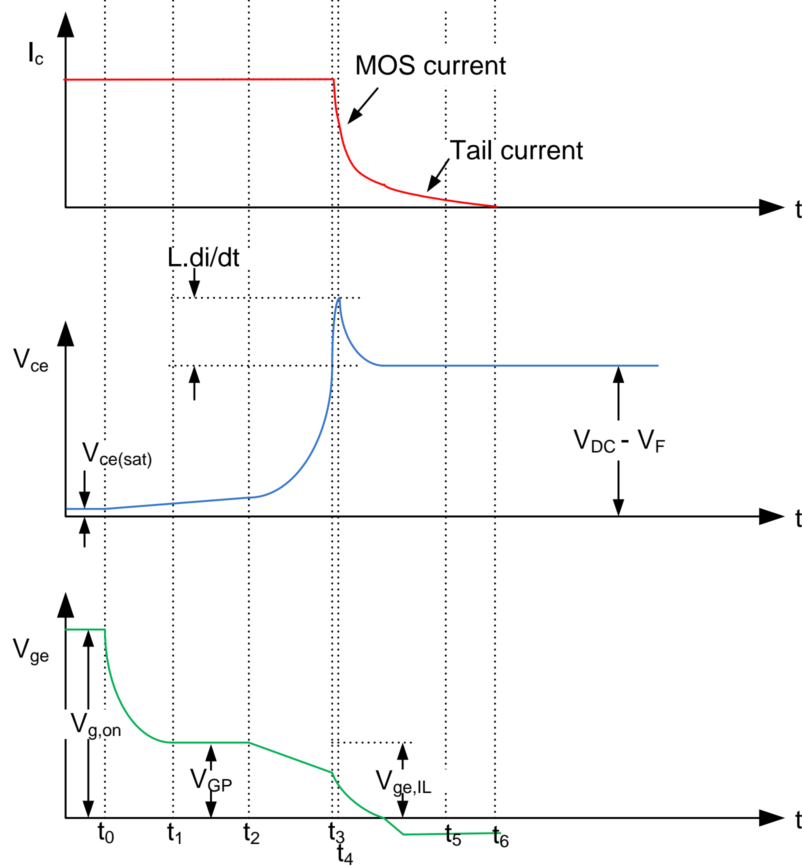


Figure 2-18: IGBT switch-off waveforms with bipolar diode

Phase 1 (t_0 to t_1): Throwing the switch to the off position, allows the gate capacitor C_{ge} to discharge and gate collector capacitor C_{gc} to charge. The time constant during switch off is the same as that in phase 6 during switch on (2-15). The gate voltage during this phase can be determined from equation (2-16).

$$V_{ge}(t) = V_{g,on} \cdot \exp\left(-\frac{t}{\tau_2}\right) \tag{2-16}$$

During this stage, the IGBT remains in the saturation region and hence the gate voltage does not affect the collector current. The charge carrier concentration in the channel reduces as V_{ge} is reduced. This reduces the base current for the pnp transistor resulting in a small increase in V_{ce}. As the V_{ge} is reduced further, the flow of electrons into the n^- region ceases.

Phase 2 and 3 (t_1 to t_3): At time t_1, the electron concentration at the p-base / n^- region reduces. Due to the wide base of the BJT, the hole current is influenced by the electric field which is established by the electron current. Consequently the hole current also reduces giving an increase in V_{ce}. After all the electrons have been swept from the drift region or recombined, the hole current rises rapidly to allow the load current to continue at a constant level [47]. The depletion region which forms, causes V_{ce} to increase rapidly. The maximum dV_{ce}/dt depends on the plasma concentration profile. As in a PIN diode, there are several factors which may cause a lower dV_{ce}/dt:

- When low current is flowing, the charge can only be swept out with a maximum rate $dQ/dt = I_L$. The expansion velocity of the depletion layer hence dV_{ce}/dt is related to the load current.
- If dynamic avalanche occurs during voltage build-up, generation of new charge carriers takes place which must be swept from the device. This causes a reduction in dV_{ce}/dt.
- If the gate plateau voltage, (V_{GP}) is greater than V_t, the MOS channel will still allow electrons to flow into the drift region. This can cause the voltage to rise slowly until V_{ge} falls below V_t. This is related to the carrier lifetime and gate resistor value [27].

The voltage rise in a PT and NPT device can be very different. The voltage rise (phase 3) of a PT IGBT has an unusual shape which shows a decrease in dV_{ce}/dt followed by a fast increase. The decrease is caused by high carrier concentration near the n^- region and buffer junction. The fast increase is due to the electric field reaching the buffer layer [39].

Phase 4,5 and 6 (t_3 to t_6): at t_3, the collector-emitter voltage reaches the dc bus voltage ($V_{DC} + V_F + V_{FRM}$) and the free wheel diode can begin to conduct current. The negative dI_c/dt in the stray inductance L induces a voltage V_L, given by equation (2-17) which appears on the IGBT as a transient voltage overshoot.

$$V_L = L \cdot \frac{di_C}{dt} \qquad (2\text{-}17)$$

At t_4, the rate of change in collector current has reached it maximum and V_{ce} begins to reduce from the peak overshoot voltage. This increases the C_{gc} further increasing the time for the gate voltage to decay.

The few remaining holes in the drift region slowly get swept out allowing the IGBT current to drop to zero. This section of the current waveforms is referred to as a current tail. The tail current increases with junction temperature but the initial dI_c/dt reduces with temperature [47].

The switch off loss is related to the amount of stored charge in the space charge region. For high voltage devices, the charge space charge region is wide to facilitate forward blocking, however this increases the switch off loss [35]. The switch off trajectory of current versus voltage is shown in Figure 2-19.

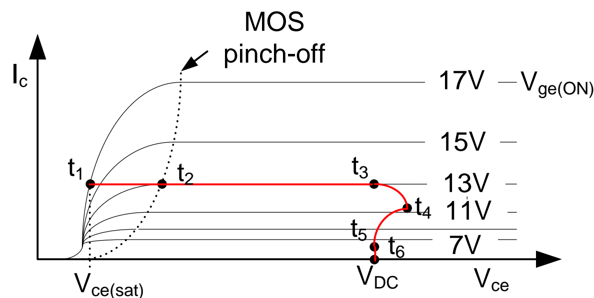


Figure 2-19: $I_c(V_{ce})$ characteristic curve for switch off

2.3 Radiated Emissions Sources from a VSD

A distinct increase in radiated emissions from a VSD system can be easily detected when the full bridge output is enabled to rotate a motor. The IGBT switching transients only exist in time for up to 200 ns for switch on and another 200 ns for switch off. With a switching frequency of 10 kHz, the period is 100 μs hence the emissions can be considered as a pulsed source. A source which has a short duration in the time domain will have a broadband spectrum in the frequency domain. In the case of a VSD the radiated emissions measurements are taken from 30 MHz to 1 GHz however, the increase in the emissions is often in the range of 30 MHz to 100 MHz [48].

When designing an antenna system for an intentional transmitter the geometry is carefully chosen to match the frequency of operation to ensure efficient radiation. However given the broadband nature of the source signal, it is not easy to identify a single antenna structure which radiates efficiently and in fact there are many possible antennas and emission paths which complicate the analysis.

This section considers some antenna theory and applies it to a simple model of a variable speed drive system consisting of the VSD module, motor cable and motor to evaluate the possible sources of emissions.

2.3.1 Emission Sources

Seven possible parasitic antennas have been identified from a VSD system and are shown in Figure 2-20. These consist of current loops which create magnetic fields and time varying voltages related to the IGBT switching of the high powered signals to the motor [49, 50]. The changing voltages can establish electric fields which can radiate. During the development of a VSD, a considerable effort is made to reduce the area of current loops within the VSD for both the performance benefit of reduced inductance and to minimise radiation. However, given the conflicting requirements of creepage and clearance for functional safety and layout for thermal requirements, it is impossible to avoid some loop area. Possible parasitic antennas within the system are identified as:

1. The large loop consisting of one leg in a power module and the dc bus filter capacitors. This is driven by differential mode currents creating H- fields.

2. H- fields generated by loops within the drive, can inductively couple onto other loops in the near field such as those formed by structural metal work, communications and sensor cables which themselves radiate giving a second potential source of emissions.
3. The switched voltage applied to each phase cable will change potential relative to the ground plane at each switching instance. Due to cost requirements and ease of installation, the braided cable used cannot provide a perfect shield. E-fields established between the three output phase conductors and the ground plane can give a third potential source of emissions.
4. A significant parasitic capacitance exists between the cable shield and the phase conductors due to their close proximity. The change in potential of the phase conductors due to IGBT switching causes a common mode current to return along the cable shield. This current is returned to the dc bus capacitors via the EMI filter for conducted emissions.
5. The second source of shield current arises from the imperfect cancellation of the magnetic field from the three phase currents. As the phase conductors are not coaxial within the cable, the magnetic fields as seen by the shield induce opposing currents in the shield. In a coaxial cable used for communications systems the continuous nature of the outer shield contains all the induced current on the inner layer of the conductor. However due to the complex weave in a braided cable, the individual conductors can force this current towards the exterior of the shield causing radiation. Given the imperfect shielding capability, magnetic fields established by the phase conductors can also directly radiate acting as a noise source.
6. In large VSDs, the layout of the cable terminals spreads the phase conductors further apart. The separation of the conductors can create a dipole antenna arrangement which can radiate electric fields. Shielding of this area by conductive mechanical structures may reduce the effectiveness of this antenna however this is very dependent on individual VSD design.
7. As the cables are unlikely to run in perfectly straight lines in a typical installation, several bends are required. Bending can lead to scattering of the RF signals which can provide a seventh source of radiated emissions [15] [52].

While the cable shield has been identified as a potential source of emissions, it is important to consider the benefits it offers. The power cables are often located in the vicinity of sensitive control cables. There is a considerable reduction in the magnetic field and electric field particularly in the low frequency. The behaviour as an antenna is difficult to predict due to unknown impedance, orientation, radiation resistance etc. [51].

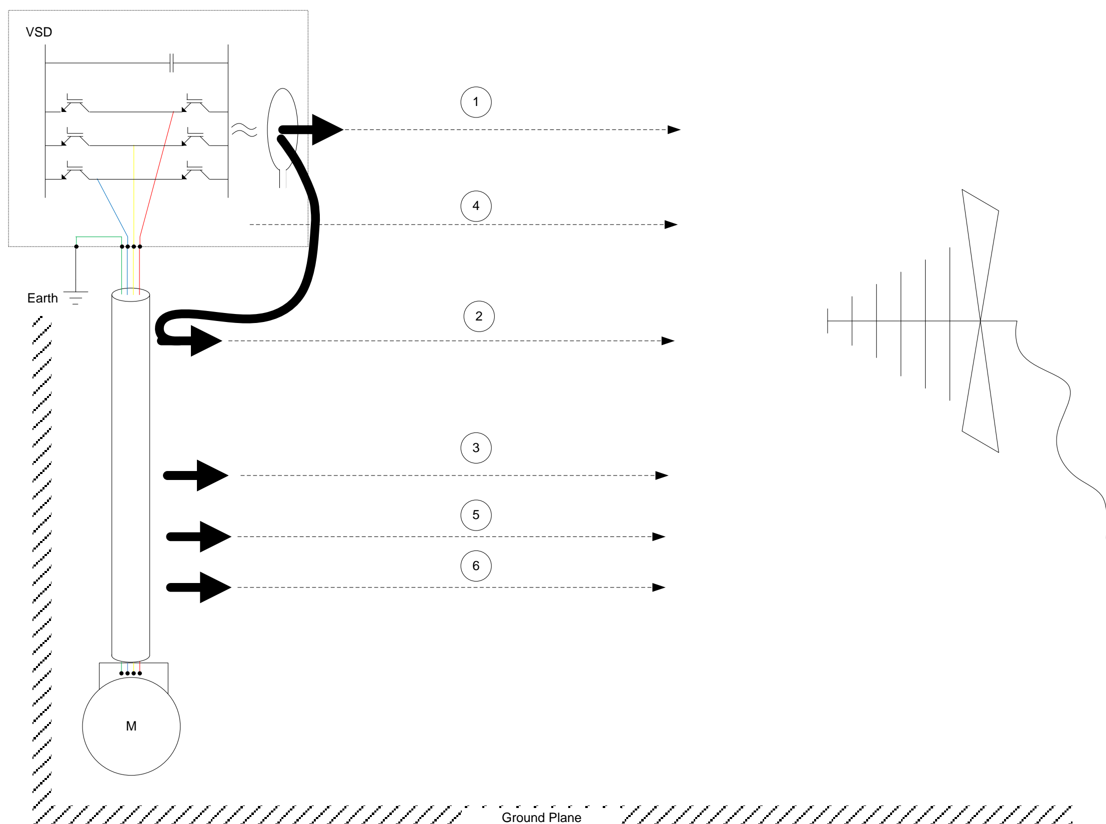


Figure 2-20: Illustration of Emissions sources from VSD system

2.3.2 Power Cables

Given the importance of the power cable with regards to radiated emissions, a closer look at its structure is required to understand the factors contributing to radiated emissions.

The recommended cable for use with VSDs consists of four cores surrounded by a braided shield or armour as shown in Figure 2-21. Three of the cores are used to supply power to the motor while the fourth provides a safety earth connection to restrict

dangerous voltages on parts which can be touched in the event of a motor fault. The shield can be positioned close to the conductor insulation or may be separated from the conductors by a further layer of insulation. The capacitance between the conductors and the shield reduces as the shield is moved further from the core.

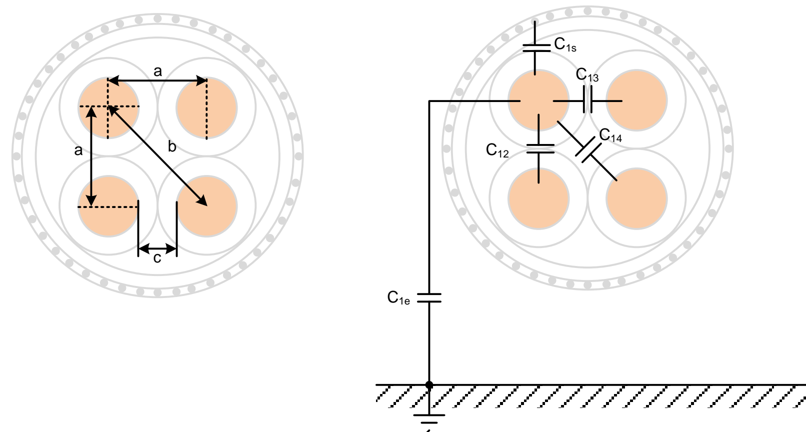


Figure 2-21: Cross section of power cable identifying internal capacitances for one conductor

It is very difficult to achieve an accurate model of a power cable at high frequencies due to the influence of manufacturing tolerances. Several cable models are discussed in the literature however these tests have been carried out in laboratory conditions where the cables have been held in fixed positions [53]. Along with the fundamental frequency required to rotate the motor, the power cables also carry the PWM switching frequencies and the higher frequency harmonics contained in the switching waveforms [54]. It is unclear how these models can be adapted to higher frequency ranges, different lengths of cables and different cable layouts due to the unpredictable change in geometry during installation arising from bending. The unsymmetrical layout of the cable will affect the mutual inductance hence the impedance as seen between phase and ground will depend on currents flowing in neighbouring conductors.

2.3.3 Cable Capacitance

The parasitic capacitances increase the common mode current flowing in the conductor. This section will look at the cable construction to identify the capacitance and analyse the impact of a shield.

For a radiated emissions test, the motor cable is connected between the VSD and the motor. The VSD is mounted in a cabinet representing a typical customer application

and the cabinet is isolated from the ground plane to represent worst cast conditions. The cabinet is connected to earth via the supply cable. A motor is positioned a few centimetres above the ground plane also on an isolating platform. The path taken by the cable will vary in the height above the ground plane. In an ideal situation, an assumption can be made that the cable height is constant and that the cable is sufficiently long, then the capacitance per unit length can be calculated using the Method of Images [55].

The capacitance per metre depends on the conductor radius (r) and the height above ground (h) as shown in equation (2-18). A plot of the capacitance is shown in Figure 2-22 for a single conductor with a radius of 1.02 mm (equivalent to 2.5 mm^2 cable) and for a radius of 2.025 mm (equivalent to 10 mm^2 cable). It can be seen how the capacitance reduces rapidly as the height is increased up to a distance of five times the radius and more gradually beyond this.

$$\frac{C}{l} = \frac{2\pi\varepsilon_0}{\ln\left(\frac{h+\sqrt{h^2-r^2}}{r}\right)} F/m \qquad (2\text{-}18)$$

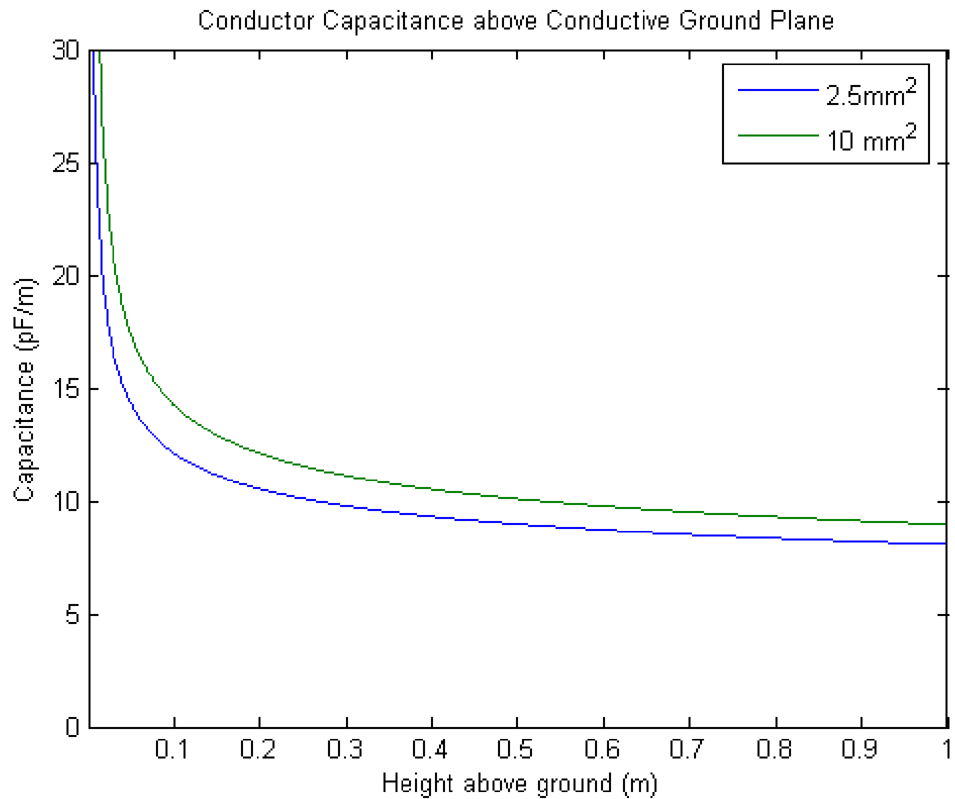


Figure 2-22: Cable capacitance to ground from a single conductor

Within a cable, there are capacitances between conductors and between the conductors and the shield. These capacitances have been identified in Figure 2-21 for one conductor and calculated for two sizes of typical cables (these cables include an additional layer of insulation between the shield and the conductor) in Table 2-1. The relative permittivity, ε_r, is taken to be 2.7 (for PVC) for these calculations.

Table 2-1: Calculated cable capacitance for a typical power cable

Conductor area (mm^2)	a (mm)	b (mm)	c (mm)	C_{12} pF/m	C_{13} pF/m	C_{14} pF/m	C_{1s} pF/m	C_{1e} pF/m
2.5	3.44	4.86	1.4	245.56	245.56	97.23	672.90	8.07
10.0	6.05	8.55	2.0	721.23	721.23	120.92	731.13	8.97

The typical range of shield coverage is from 40% to 98% [49, 56]. To simplify the conductor to shield capacitance calculation, the shield is assumed to be solid and perfectly conducting. To get a more accurate approximation, the capacitance should be multiplied by the shield optical coverage. The capacitance between the conductor and ground should also be reduced by the inverse of this factor. When considering this, and using the figures obtained in Table 2-1, it can be seen that the capacitance between the conductor and ground is insignificant when using a shielded cable.

The individual capacitances calculated in Table 2-1, do not all require charging at the same switching instant. The cable charging current can lead to significant heating of the power cable due to the cable resistance particularly at high switching frequencies.

2.3.3.1 Skin Effect

High frequency currents do not flow uniformly through a cross sectional area of conductor. The current density is at its highest value on the outer surface of the conductor and falls off exponentially with depth. This phenomenon is referred to as the skin effect and the skin depth is the distance at which the current density is reduced to a factor of e^{-1} [13].

The high frequency current flows in a reduced area resulting in an increased resistance. This "ac" resistance can be calculated using equation (2-19) and can be seen to be frequency dependent.

$$R_{AC} = \frac{\sqrt{f\pi\sigma\mu}}{2\pi a\sigma} \cdot l \text{ (if skin depth is much less than } a\text{)} \qquad (2\text{-}19)$$

where:

- f is the frequency;
- σ is the material conductivity;
- μ is the permeability;
- a is the radius of the conductor;
- *l is the length of the conductor.*

For power cables, the fundamental frequencies used to rotate a motor are of the order of a few Hertz up to several hundred Hertz. The skin depth at these frequencies is larger than the radius of the conductors and hence this phenomenon is not observed. When considering the radio frequency content of the signals, the skin depth at 30 MHz is 11.9 μm in copper which is less than the thickness of a braided shield. At these frequencies, the contact impedance between the braids becomes capacitive reducing the impedance along the shield. It is a combination of these effects which makes accurate predictions of the cable performance impractical for a user installed VSD application.

2.3.4 Cable Inductance

In a three phase, four core cable, the conductors are not balanced. At a particular operating point, the current flowing in one conductor will be equal to the current flowing in both the other lines at a first approximation. The distance between the shield and each conductor should ideally be constant. The problem with the typical power cables is the use of a safety earth conductor which removes the symmetry from the cable and will lead to an increase in common mode currents which depend on the 3 phase current vector [54]. As the IGBT switching events only occur for a short duration, coupling at radio frequencies is minimal and unlikely to influence the switching transients. Alternative cable structures as shown in Figure 2-23b can preserve this symmetry among the three conductors.

The mode conversion of differential mode currents to common mode currents due to the unsymmetrical cable structure can lead to radio frequency components of the phase currents contributing to radiated emissions. It is not possible to quantify the magnitude of these currents as the high frequency content in the phase currents would occur at the same instant as the cable charging currents related to the dV/dt.

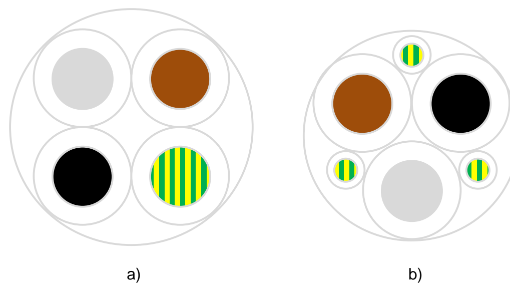


Figure 2-23: Cable cross section a) 3 phase , 1 ground non-symmetrical b) 3 phase, 3 ground, symmetrical.

2.3.5 Braid Structure

A typical braid structure is shown in Figure 2-24. The variables between various designs of braid are described in [56] and include: the number of carriers (belts of wires); picks (number of carrier crossings per unit length); the ends (number of wires in each carrier); wire diameter and radius of the shield. The pitch angle is the angle between two crossing carriers and is a major factor in determining the optical coverage. The optical coverage is usually given in percentage and is a ratio of the area covered by the wires to the area exposed by the small diamond spaces.

The transfer impedance of a perforated shield is the result of two phenomena [56]:

- diffusion through the metal (same as a solid shield the current has to diffuse through the shield due to skin depth)
- mutual coupling through the holes.

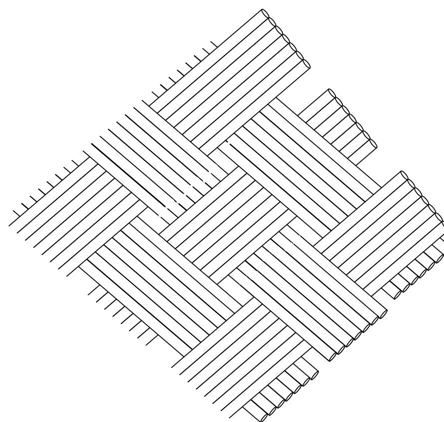


Figure 2-24: Structure of Braid

The transfer impedance can be calculated analytically for simple geometries. This may be useful when comparing one cable to another however it is not a useful figure when evaluating a system performance as the connection method will usually have a larger impedance.

Within a braided cable, the layers of the braid overlap. This overlap causes an individual strand of braid to be displaced with regard to the axis of the cable. This is referred to as porpoising. Porpoising affects the shielding impedance with the continued change from outer layer to inner layer. The braid will carry the external shield current over a short section however some of this will then be transferred to the inner structure as the strands swap position due to finite impedance at the cross over point [57]. The impedance at the cross over points is complex and will become more capacitive at radio frequencies however this impedance may vary strongly with cable bending.

The weave angle greatly affects the mutual inductance of the shield for a given optical coverage. This is related to the magnetic polarisation along the axis of the rhombus which is formed. The mutual capacitance is not affected to the same extent by weave angle.

The mutual inductance increases with the hole number and shape. In a similar manner, increasing the inductance of the shield by increasing the weave angle reduces the benefit of the shield at high frequency due to resonance.

There are a few general rules about shielding design which are useful to consider. A shield having a given optical coverage will be more leaky given few large holes compared to many small holes. This is shown in Figure 2-25 where the transfer impedance of a braid is compared to a solid copper tube. α is the weave angle; a is the radius of the shield, d is the tube wall thickness; K is the optical coverage; C is the number of carriers. It can be seen that as the optical coverage is reduced, the transfer impedance increases at high frequencies. It is assumed that the results shown in this graph continue up to higher frequencies.

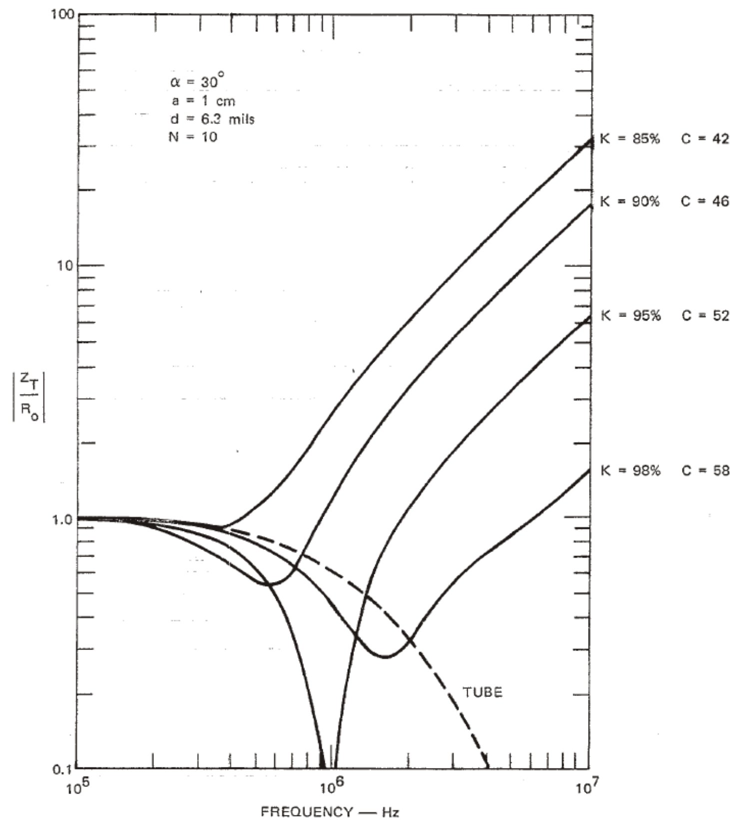


Figure 2-25: Transfer Impedance of a Braided- wire shield [56]

For coaxial cables, the shield transfer impedance is often published by the cable manufacturers. Similar data has not been found for three phase power cables.

2.3.5.1 Impedance Matching

It is common for the impedance of cables which carry radio frequency signals to be matched to the impedance of the source and load to avoid reflections. Given the complex impedance of the motor (load), the broadband nature of the switching signals and the emphasis on reducing energy loss, it is not possible to implement impedance matching. This can lead to line reflections and several cable resonance effects which can cause peaks in the radiated emissions spectrum [58].

2.3.6 Cable Summary

The various cable parameters discussed above are important to precisely model the cable performance and impact on radiated emissions. The most significant parameters are the capable capacitance as this can be seen to effect the switching transient of the IGBT and the inductance as this gives the transmission line properties associated with

reflected signals at higher frequencies. The addition of a braided shield complicates the analysis of the radiated fields and radio frequency current paths however the benefits of including and properly terminating the shield to reduce the radiated field strength far outweighs the additional modelling complexity.

2.4 Frequency Analysis

At a first approximation, the switching transients observed in the voltage and current are trapezoidal. The rise and fall times are determined by the gate resistor value, load current, voltage etc. while the switching frequency and hence the period are selected by the user. Many papers [59-61] cite the rate of change of this voltage (or current) to be the source of EMI and have attempted to implement strategies to control this rise time. This section will present an analysis of simple switching trajectories in the frequency domain using the Fourier Transform and the Wavelet Transform.

2.4.1 Frequency Content in Switched Signals

Several simple pulse waveforms are constructed in Matlab® with a period of 1 ms, a 50% duty with linear rise and fall trajectories as illustrated in Figure 2-26. The rectangular pulse represents the ideal switching profile with instantaneous rise and fall. Two trapezoids are shown with a rise time of 100 ns (typical for voltage rise time switched by an IGBT), and 1 μs. Two functions, one whose first derivative and one whose third derivative is continuous have been constructed and are referred to as s-ramps (similar to those found in motion control). It is known from testing of IGBTs that the switching loss is proportional to the switching time hence minimising the switching time is a key objective in VSD design.

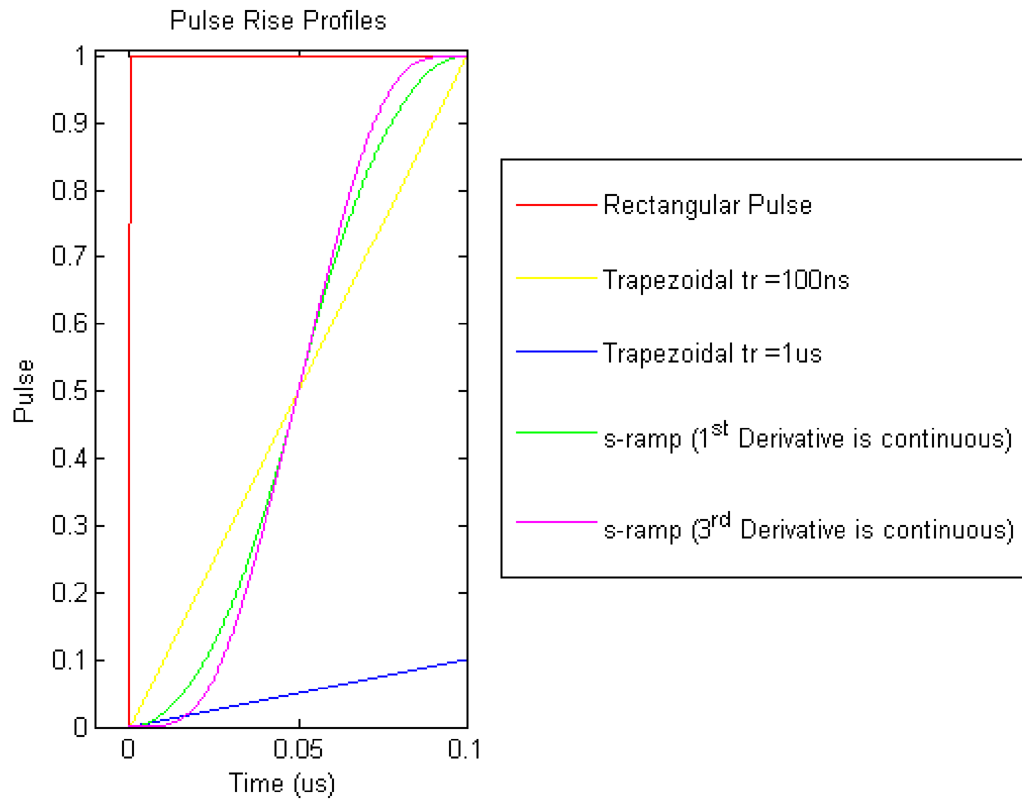


Figure 2-26: Sample pulse trajectories

Assuming these signals repeat indefinitely, a Fourier Transform can be calculated to evaluate the frequency content. An envelope is fitted over the resulting spectrum for each of the waveforms and the results are shown in Figure 2-27. It can be seen that the square wave has the largest magnitude across the frequency range, however at lower frequencies around 1 MHz the signal levels are similar for all signals with a 100 ns rise time. This is consistent with conducted emissions testing where the emissions can be related to the dV/dt of the switching transient. The magnitude can be seen to fall linearly (-40 dB/decade) with frequency for the trapezoidal pulses however for the s-ramp profiles, the rate of reduction in magnitude increases with frequency. In this example, the magnitude of the s-ramp with a continuous first derivative at 100 MHz is comparable to the 1 μs trapezoid. However in the time domain, the rise time is ten times shorter which would lead to a proportional reduction in switching loss from the IGBT. The broadband nature of the pulse in frequency domain illustrates that it is not necessary to detect a sinusoidal signal such as ringing in the switching transient to have

high frequency content. Ringing would display a narrowband feature in the frequency domain and is not considered in the general problem of radiated emissions from VSDs.

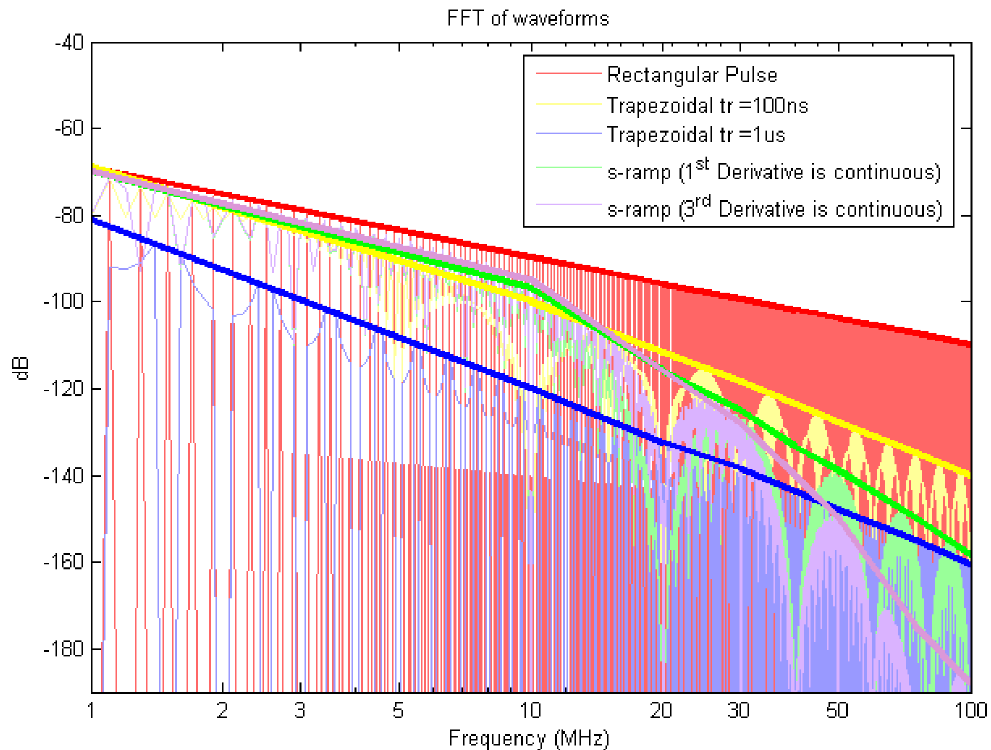


Figure 2-27: DFT of shaped pulse waveforms

2.4.2 Limit of Curve Shaping for Radiated Emissions

Shaping of the switching transients of an IGBT as illustrated in Figure 2-27 appears to offer potential to give a fast switching speed and a reduction of radio frequency components. However, further examination of the theory presents a limitation where curve shaping can no longer offer benefits.

An illustration in the frequency domain of a perfect trapezoidal waveform with a 100 ns rise time is shown in Figure 2-27. The envelope for the frequency content initially falls by 20 dB/decade however at a break point, this then falls by 40 dB/decade. The break point (f_{c1}) occurs at a frequency determined by (2-20). Utilising an s-ramp with the same rise time, a second break point can be observed where above this frequency, the magnitude decays at 60 dB/decade. It is this second break point which offers the possibility to reduce radiated emissions if it occurs significantly below 30 MHz.

$$f_{c1} = \frac{1}{\pi \times t_r} \tag{2-20}$$

For a given magnitude of trapezoid (dc bus voltage) in the time domain, an attenuation of the frequency content above 30 MHz is required to pass the radiated emissions test. To take advantage of the 60 dB/decade reduction at 30 MHz, it is assumed that the second breakpoint must occur at or below 20 MHz. The breakpoint utilising the s-ramp can be determined using equation (2-21) [62] which is dependent on the rise time of the first derivative of the switching signal ($t_{r(dV/dt)}$).

$$f_{c2} = \frac{1}{\pi \times t_{r(\frac{dV}{dt})}} \tag{2-21}$$

At the limit of the s-ramp curve, $t_{r(dV/dt)} = 0.5 \times t_r$ resulting in 50 ns for $t_r = 100$ ns. If we assume that f_{c2} must be at or below 20 MHz, this gives us a minimum $t_r = 31.8$ ns. The attenuation of the signal is relative to the magnitude of the trapezoid hence for a given limit in either voltage or current, the required attenuation will increase with voltage or current. The attenuation of the signal can be determined using (2-22) where further sinc functions can be added for higher orders of smooth derivatives, again each with its rise time equal to half of the previous rise time.

$$E = 20 \times log_{10}\left(sinc(\pi \times t_r \times f).sinc(\pi \times t_{r(\frac{dV}{dt})})\right) \tag{2-22}$$

As new semiconductor materials are developed which are capable of operating with shorter switching times, the benefits of curve shaping are likely to disappear and additional methods to contain the RF signals are required.

2.4.3 Wavelet Transform

A Fourier Transform decomposes a signal into a set of infinite sine waves with magnitude and relative phase. While the signal can be reconstructed in the time domain, it is not possible to obtain information regarding the position in time for pulsed or discontinuous signals. It is possible to apply windowing functions with the Fourier Transform assuming the signal repeats periodically however higher frequency components can be distorted by spectral leakage. The wavelet transform presents a

method of identifying the frequency content of a signal and also provides a representation of this in the time domain [63, 64]. This is achieved using a user defined wave shape with zero mean, finite energy and of finite duration in the time domain referred to as a *mother wavelet*.

This chosen mother wavelet can then be translated, dilated, and cross-correlated with the original signal. To illustrate this procedure, two trapezoidal wave shapes with a 100 μs rise and fall time and period of 1 ms, representing typical switching transients in a VSD are shown in Figure 2-28 and are evaluated using a Mexican Hat wavelet (2-24) (which is the first differential of the Gaussian Function (2-23)). The wavelet transform is shown in (2-24) where a is the scale used to assess different frequency content by dilation (and can be compared to ω in the Fourier Transform) and b is the translation parameter to assess different time segments. As the wavelets are not true sinusoids, the scale does not represent a true frequency [63]. Instead a pseudo-frequency can be related to the scale and the dominant frequency of the mother wavelet.

$$\Psi(t) = (1-t^2)e^{-\frac{t^2}{2}} \quad (2\text{-}23)$$

$$c(a,b) = \frac{1}{\sqrt{a}}\int a(t)\Psi(\frac{t}{a}-b)dt \quad (2\text{-}24)$$

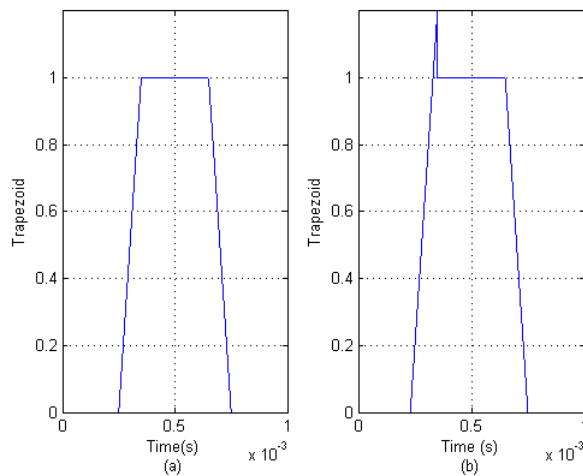


Figure 2-28: a) Trapezoidal pulse with 10us rise time. b) Trapezoidal pulse with overshoot.

The plotted Scale in Figure 2-29 is logarithmic and is inversely proportional to the centre frequency. In this case, scale values of 8.33 and 2500 correspond to 30 MHz and

1 kHz respectively. The trapezoid having a period of 1 ms has a fundamental frequency of 1 kHz if repeated periodically. In this example it can be seen that the maximum amplitude at 1 kHz is 0.75 across the time range. Reading the frequency content with time requires careful attention when using the illustrated diagrams. A sinusoidal waveform with a magnitude A will only achieve a magnitude A in the time domain when the phase corresponds to $\pi/2$, likewise in the wavelet representation, the peak of this frequency content will only occur momentarily in time.

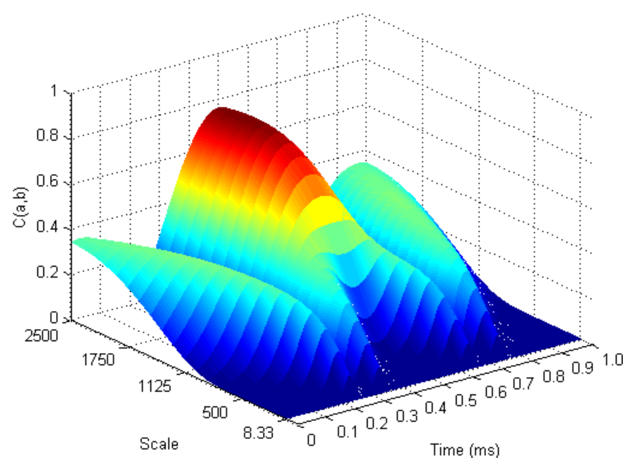


Figure 2-29: Wavelet Transform of Trapezoidal pulse 1 kHz to 30 MHz

The interesting application of the wavelet transform is to identify short time duration features which contain radio frequency content. To illustrate this, the two trapezoids shown in Figure 2-28 are evaluated in Figure 2-30 and Figure 2-31 over a frequency range of 30 MHz to 100 MHz using the Mexican Hat wavelet at the scales indicated. For the trapezoidal pulse, four distinct areas of radio frequency content have been identified as corresponding to a discontinuity in the first derivative of the signal. For the trapezoid signal with the overshoot five distinct regions of radio frequency can be identified. In this example the largest magnitude signal can be easily identified in time and focused corrective action taken to minimise the radio frequency content in this specific area.

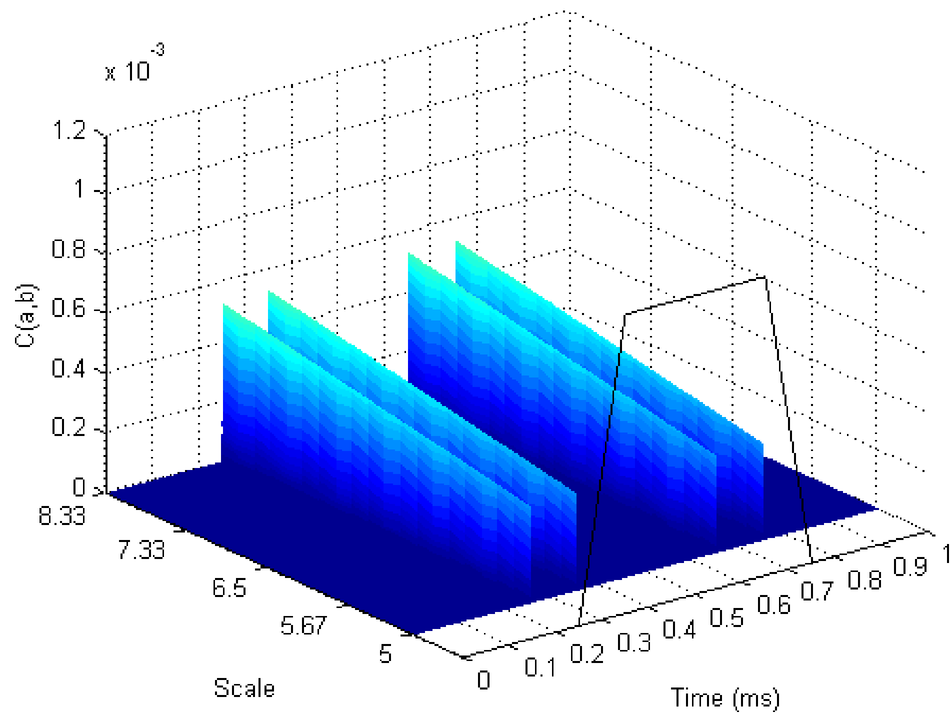


Figure 2-30: Wavelet Transform of Trapezoidal pulse 30 MHz to 100 MHz

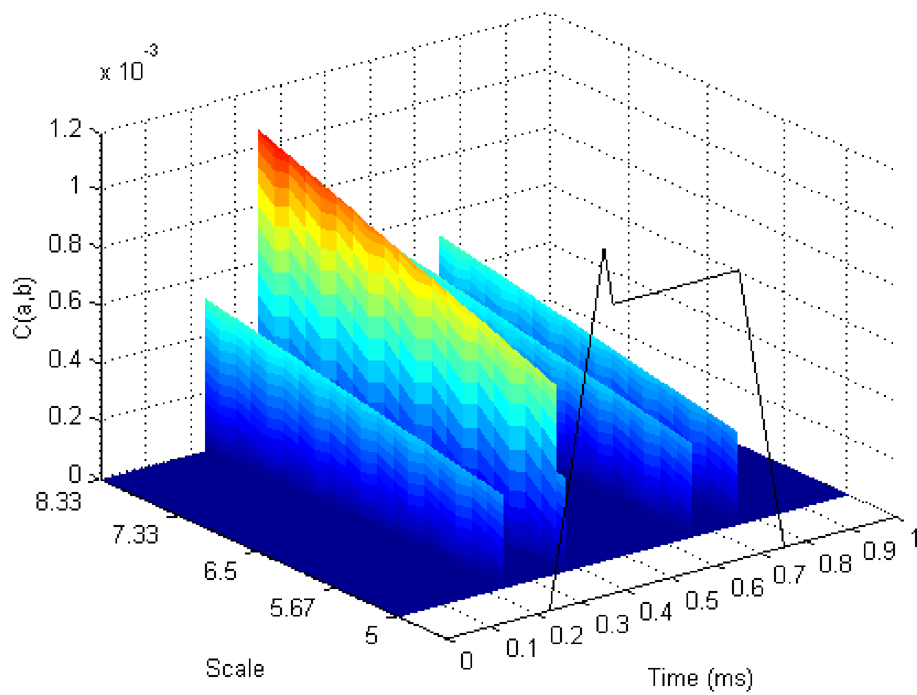


Figure 2-31: Wavelet Transform of Trapezoidal pulse with overshoot 30 MHz to 100 MHz

In signals measured from a VSD, it is unlikely that the rise time and fall time of the transient signals are equal. Where the use of the wavelet transform has been demonstrated to identify the radio frequency content in the overshoot of the signal, the same techniques can be applied to both switch on and off transients.

Considering the breakpoints described above, all frequencies up to the first breakpoint will appear to have a single pulse source of broadband emissions for the duration of the rise time. For the ideal trapezoid, at frequencies beyond the breakpoint, there will be a pulse source at both the beginning and end of the rise transient. As more breakpoints are added for the s-ramp, the number of pulsed sources further increases albeit at the higher frequencies and for shorter durations.

2.5 Summary of Chapter 2

This chapter has collected published information in three important disciplines which illustrate in detail how the power stage of a VSD is switched, how voltages and currents can travel along cables particularly at high frequencies and how the necessary physical structures such as cables and metal work can act as parasitic antennas. Frequency analysis has been carried out on some typical switching transients in an effort to identify the potential sources of radio frequency interference in the frequency range of 30 MHz to 100 MHz responsible for radiated emissions.

The switching transients of the IGBT are very dependent on the gate resistor selection influencing both the collector current and voltage trajectories. A study of the switching transients highlighted how the current and voltage transients are mostly independent of each other and with sophisticated control techniques could be modified to influence the high frequency currents.

The power cable used between the VSD and the motor is a very complex system when examined at radio frequencies. The change in impedance with cable length, bending and termination methods provide quantities which are capable of radiating radio frequency components present on either the conductors or shield.

In the frequency range associated with radiated emissions from a VSD, 30 - 100 MHz, the rise time of voltage and current transients are of secondary importance. Short rise

times are needed to minimise switching loss and the finer details and the discontinuous higher derivatives of the signals are responsible for the radio frequency content.

Chapter 3: Review of Gate Drive Circuits

3.1 Introduction

The gate drive circuit acts as the interface between the microcontroller and the IGBT. Its primary function is to respond to the logic level signal from the controller and shape the signal to a suitable form for the power device. In addition to the primary function, the gate drive must also protect the switching device in the event of a predictable fault condition.

In the description of IGBT switching transients, a simple fixed gate resistor is used to control the current flow into the gate of the IGBT. Sophisticated methods have been found in the literature which are designed to meet specific applications and constraints for improved protection and performance. These are achieved by controlling the timing and magnitude of the signals applied to the IGBT gate. As shown in chapter 2, the RF content responsible for radiated emissions is confined to specific features in the switching transients. Control of these features using a gate drive offers an opportunity to reduce radiated emissions without the need for expensive physical filters. This chapter discusses these gate drive designs and identifies parameters which could be useful in the control of radiated emissions.

3.1.1 Implementation of Gate Drive

IGBTs are used in many products from VSDs to induction cookers to washing machines. In many of these products, the cost effective solution for driving an IGBT is a commercially available modular gate drive. These tend to include the interface and protection circuitry, isolated power supplies and condition monitoring.

For very cost sensitive applications, the gate drive can be optimised to the user specification and constructed from discrete components. This has the advantage in some topologies, where, for example, the over current protection features can be executed in a central processor, multiple power supplies can be combined for space and cost savings.

IPMs (Intelligent Power Modules) or “SMART Modules” are modules which have the gate control inside constructed on an integrated circuit (IC). It has been suggested that

this is only suitable for small power rating IGBTs due to peak current requirements however in [65] a 16A peak gate drive on an IC has been realised. The combination of physically small features required for the logic control of the gate drive and the relatively large features required for the high voltage and current requirements needed to switch an IGBT can pose significant problems to device manufacturers leading to a poor yield [66]. While the IPMs carry a premium price, they have the advantage of reduced real estate and component count reducing the system costs.

Attempts have been made to implement the gate drive on the same silicon as the power device [65]. Several problems with this include isolation during fault conditions, additional manufacturing processes leading to higher device cost and reduced yield. As silicon on insulator (SOI) processes improve, the associated cost may make this technology more favourable [67].

3.2 Inverter Configuration

The majority of applications for IGBTs are in high powered circuits such as Switched Mode Power Supplies and Variable Speed Drives. The arrangement of the power switches are, in many cases, determined by the application and control method. E.g. a Matrix converter has nine bi-directional switches, a Full Bridge inverter has six switches, and the majority of typical dc-dc converters have one or two switches [68]. Each switch construction depends on the power rating of the application. There are economical and technical restrictions on the size of the silicon which can be used to manufacture an IGBT [69]. To achieve higher power ratings, the chips need to be connected in series, parallel or both. The gate drive requirements depend on the chosen configuration.

The gate drive circuitry is only one piece of the complex VSD circuitry and as such requires an interface to a microprocessor for control signals. The required interface can depend on the operation voltage, power topology, and number of IGBTs to be controlled. It is assumed that all the control or sensor signals can be transmitted into the gate drive without delays or interference and these aspects will not be considered further.

3.2.1 Single IGBT

For low power circuits, a single IGBT chip solution is the simplest and cheapest solution. The smallest IGBTs commercially available are rated at 1 A, 600 V. The largest single chip IGBTs are rated at 300 Amps, 1200 Volts and are limited by thermal performance [70].

IGBTs do not have a body diode and need to have an anti-parallel diode to allow reverse conduction for inductive loads [71]. The diode is usually contained within the same package to minimise the stray inductance. Small packages have low inductance and can have good thermal performance as they are not affected by the proximity of other devices [72].

3.2.2 Series IGBTs

To achieve a higher blocking voltage using IGBTs, it can be useful to connect several devices in series. This will give good results when the devices are static (i.e. either on or off). When the devices change state, (switch on or switch off), it is important that the transient voltage is shared across all devices evenly to avoid excess stress to single devices. Snubber networks are the traditional method for implementing the series connection of IGBTs by matching all the transients to the slowest device. Snubber networks are bulky, dissipate energy, have a high component count taking valuable real estate and often suffer from low reliability [73].

Active gate drive controls have been designed to achieve voltage sharing without snubber networks [74]. These will be discussed further in section 3.4.2.2. Minimisation of switching loss is usually a secondary requirement in comparison to voltage sharing. A small increase in IGBT loss can be tolerated in large systems where efficient cooling systems can be implemented, whereas incorrect voltage sharing will lead to device destruction.

Allowing a system to operate at a higher bus voltage for a given power rating may offer significant benefits which may include: a lower operating current, smaller and cheaper power connectors and external equipment [73]. This needs to be balanced against the additional cost of the high voltage system. While the dV_{ce}/dt of individual IGBTs can be controlled to a defined level, the dV/dt of the series connected system could be very large giving rise to EMI issues which may require additional filtering.

3.2.3 Parallel IGBTs

There are physical limits to IGBT cell current density and manufacturing limits to device chip area to meet satisfactory production yields [11]. To increase the current capability of a power switch, it can be useful to connect several IGBTs and diodes in parallel. This can be achieved by paralleling discrete components or Si (silicon) chips within a module. It is important that each device operates within its safe operating area at all times to avoid failure. This can be difficult to control due to temperature differences across a module and parasitic elements exaggerated by the parallel connections. Individual monitoring of IGBT chips is costly and often safety margins

are included in the system design especially in the switching characteristics to protect the worst case device.

3.3 Design Considerations

The design of a gate drive for a commercial product must satisfy the functional specification and must provide protection to the power devices in the event of a likely fault condition. While measurements of radiated emissions are not considered under fault conditions, several techniques implemented for protection highlight control parameters of the IGBT which can be influenced by the gate drive. Several circuits are considered here to illustrate methods of voltage and current control by shaping the gate transient.

3.3.1 Gate Drive Power Supply

The most common power supply for an IGBT gate drive is an isolated dc to dc converter. These devices are compact and offer galvanic isolation. Several gate supply rails can be induced from a single primary circuit to save space and component count.

The industry standard $V_{ge,on}$ for an IGBT control is 15 V. +20 V_{ge} is the maximum rating of the majority of devices, limited by the maximum electric field strength allowed in the oxide layer. Operating at a high gate voltage reduces the conduction losses but reduces the ability of the circuit to withstand short circuit conditions [66].

Negative bias (typically greater than -5V) is often applied to IGBTs to increase the immunity to dV/dt from the complementary power device switching. Negative bias is not always necessary if other protection is provided. The positive and negative gate supply voltages and impedance will affect the switching losses however this can be compensated for with the correct choice of gate resistor [75].

When choosing the gate drive power requirements, the gate charge data and not the gate capacitance should be used. This is due to the Miller effect where the gate capacitance changes with the applied collector emitter voltage [76]. The large peak power to charge the gate only flows during the device switch on and off transient. The average power may be several orders of magnitude less than this. All components in the gate drive must be suitably rated to survive the peak power dissipation and average dissipation for the designed switching frequency.

For some gate drive topologies, monitoring of the supply voltage is necessary to avoid IGBT failure in the event of a voltage dip, for example, a reduction in gate voltage during the on state could cause the IGBT to operate in the active region leading to high power loss and thermal failure. The supply impedance must be low to supply the large peak currents during switch on and off the IGBT. If there is active under-voltage detection, it is important that this does not become unstable when switching the large peak currents [66].

3.3.2 Dead-Time Interlock

IGBTs take a finite time to change state from low impedance to high impedance and vice versa. In most inverter output stages, two devices are connected across a high voltage dc bus with the midpoint connected to the output terminal. It is important that the devices are not allowed to conduct current at the same instant to avoid a shoot-though [68]. A delay must be incorporated into the system to ensure one device has completely switched off (including tail current) before the other switches on. This can be implemented in either software where a defined dead time or blanking period is included in the PWM signals, or in hardware.

3.3.3 Temperature Sensing

Temperature monitoring of the IGBT plays an important part in achieving the maximum IGBT performance. Although the characteristics of the IGBT change with temperature, a study using this feedback to control the switching characteristics of the gate drive has not been found. It is important when measuring the switching losses for online monitoring that it is carried out at the worst operating temperature [27]. While the characteristics of the device change with temperature, the additional expense to a gate drive of adapting to this may not be justified by the benefit of tracking the reduced losses.

3.3.4 Overvoltage Protection

During the switch off of an IGBT, the voltage across the device increases to the dc bus voltage. As the current through the device begins to fall, the rapid change in current (dI_c/dt) can produce a voltage across the parasitic inductances of the power loop consisting of the electrolytic capacitor, laminated bus bar and IGBT module bond wires.

A circuit designer must ensure that any voltage overshoot does not cause the IGBT to operate outside its SOA as this will lead to failure.

It is possible to use active clamping methods to restrict the overvoltage during switch off as described in [77, 78] where a metal oxide varistor (MOV) or Zener diode in series with a blocking diode are inserted between the collector and gate to provide feedback (see Figure 3-1). As the collector voltage increases beyond a designed limit, the feedback device conducts current into the gate terminal, charging the gate capacitance and increasing V_{ge}. This action allows the IGBT to continue to operate in the active region reducing the dI_c/dt hence limiting the voltage overshoot. This is a low cost circuit to implement however achieving a reliable and repeatable performance is difficult due to the temperature dependence of MOVs and Zener diodes. The value of the gate resistor must be chosen to ensure the gate plateau voltage is above the threshold voltage to avoid a delayed response [27].

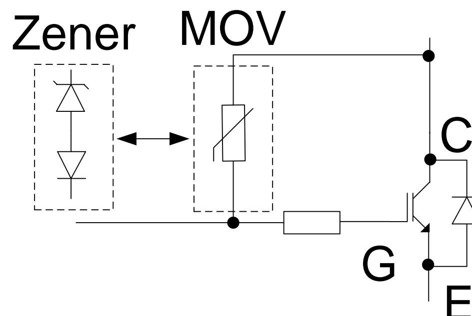


Figure 3-1: Illustration of MOV or Zener used for overvoltage control

3.3.5 Over-Current Protection

For most gate drives, knowledge of the current is not required during normal switching and it is usually left to the microcontroller to switch the IGBTs. However, many gate drives include protection features which detect fault currents.

Uncontrolled over-current in an IGBT can drive the device out of saturation. This causes the collector emitter voltage to increase leading to high power dissipation which can result in a thermal failure. The types of faults which cause high currents to flow can be split into two categories: hard short circuit and soft short circuit. The protection features for each case need to be considered separately.

Both hard and soft short circuits cause the IGBT to enter its active region. In this condition, the output current is related to the gate voltage by the transconductance. By monitoring the gate voltage, the short can be detected and the device switched off before damage is incurred [79]. In many gate drives, V_{ge} is clamped to a maximum voltage using a Zener diode, restricting the maximum fault current. By limiting the current, the gate controller may have more time to operate before the device is destroyed.

When a load is connected to an IGBT via a long cable, the cable has a significant capacitance which must be charged as discussed in section 2.3.3. This cable charging introduces large current spikes for a short duration at the beginning of each switching cycle. It is important that these spikes do not cause damage to the IGBT.

3.3.5.1 Hard Short Circuit

During a hard short circuit, for example, a cable short or incorrect installation, the output phase current rises to a high level causing the IGBT to saturate. V_{ce} rises as the trajectory moves along the operating curve determined by the applied gate voltage, towards the desaturation boundary further increasing the loss in the device. A protection circuit must act very quickly to limit the current by reducing the gate voltage and turn the device off. This is in the order of 10 μs to avoid thermal destruction of the device [66]. It is important that switching off an IGBT from the short circuit condition is carried out in a controlled manner to limit the dI_c/dt and hence a dangerous voltage overshoot arising from the parasitic inductance of the circuit.

3.3.5.2 Soft Short Circuit

During a soft short circuit, the current rises to a level above the continuous current rating of the device. This current can only be tolerated for a short period of time (up to a few ms depending on the current level) before damaging the device. Such a fault may be the result of insulation break down in a long cable or the electric machine.

In the protection method proposed by [80], V_{ce} is used in conjunction with an RC filter to curve fit the protection to the SOA of the device during switch on (see Figure 3-2). In the event of the current approaching the SOA limit, the voltage across the IGBT

would increase. This would reduce the current flowing from the gate circuit through D2 and direct it through the RC network switching on MOSFET M1. By using M1 in its active region, the IGBT gate capacitance would be discharged limiting the collector current but would not necessarily switch the IGBT off. Using the RC network allows the device to operate to the limits of the SOA before switching off and may avoid tripping the VSD in an emergency situation. As the capacitor is discharged slowly through R3, the cumulative effect of soft short circuits would be captured.

While this proposed gate drive does offer protection to soft shorts, there are several challenges with using this type of gate drive. The gate power supply must provide a continuous current source which reduces the advantage of the IGBT voltage control input. The current limit for a given IGBT's SOA has been determined from the thermal properties of the silicon chip. It is not possible to operate at all points within the SOA continuously without destroying the IGBT requiring some method to signal to the control system that a fault has occurred and followed by the switching off of the device.

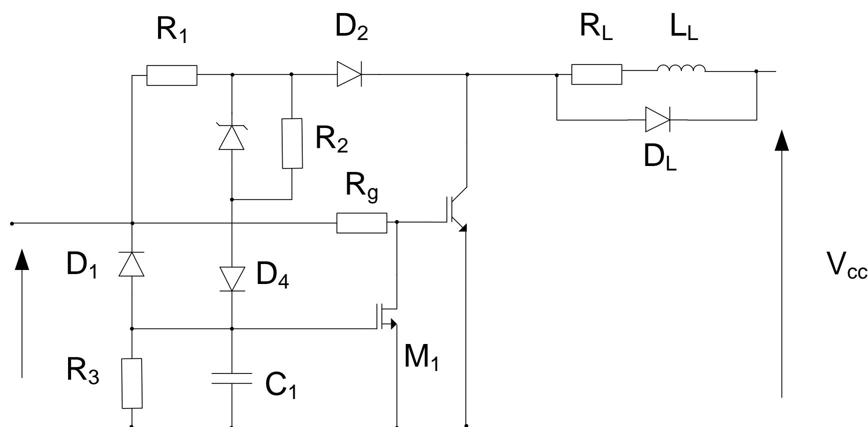


Figure 3-2: Gate Drive offering protection against soft shorts for limits of SOA.

As with the hard short circuit case, the voltage overshoot would need to be considered to avoid stressing the device (an additional resistor in series with the MOSFET would achieve this).

3.3.6 Switching Loss

Switching loss in an IGBT depends on many operating conditions. Losses given in a datasheet only represent the losses due to the collector voltages and currents and do not include the dissipation in the gate as they are small in comparison [26].

As the gate voltage increases beyond the threshold, the collector current begins to increase. This will increase to a peak value equal to the sum of the load current and the peak reverse recovery current in the free-wheeling diode. The collector emitter voltage across the device will reduce slightly due to the parasitic inductance in the power loop, however, it remains at approximately the dc bus voltage. When the collector current has reached its peak value, the current can then reduce to the load current. The voltage across the device reduces to a small value related to the output current. Integrating the product of the voltage and current during this period gives the switching energy dissipated as heat in the device. The reverse of this process is repeated for switch off.

Emitter inductance provides an unwanted feedback to the gate drive during switching transients with the effect of reducing the gate voltage as measured on the silicon during switch on and increasing the gate voltage during switch off. This has the result of increasing the switching time resulting in an increase in switching loss. This inductance becomes very important when switching parallel devices as it may lead to current sharing issues [81]. As the IGBT current rating increases, an additional emitter terminal (Kelvin Emitter) is added to the gate circuit to remove the influence of the load current.

A large part of the switching losses during switch off are due to the tail current. This is due to the charge stored in the base of the IGBTs BJT as discussed in chapter 2 and cannot be influenced by the gate voltage [71].

3.3.7 Conduction Loss

When an IGBT is held in the off state, a leakage current in the order of several μA can flow through the device. The power loss associated with this leakage current is insignificant compared to switching losses and on state losses. Conduction loss in an IGBT can be approximated by the sum of the voltage drop across the p-n junction and the voltage drop across the (on-state) MOSFET multiplied with the output current [71].

The voltage drop across the MOSFET appears as a resistive drop increasing with collector current. In the saturation region, the voltage across the MOS junction is directly related to the applied gate emitter voltage. Increasing the gate voltage reduces $V_{ce(sat)}$ hence reduces the conduction losses. When the gate voltage is increased, the available current under a short circuit condition also increases. To protect against this situation, a very fast protection circuit is required [81].

3.4 Control of Switching Transients

The switching transients under normal operation are conventionally controlled with the selection of the gate resistor. Several reasons for improved control for specific applications are discussed in this section with both passive gate drives and active gate drives controlling the entire switching cycle, specifically dV_{ce}/dt and dI_c/dt control.

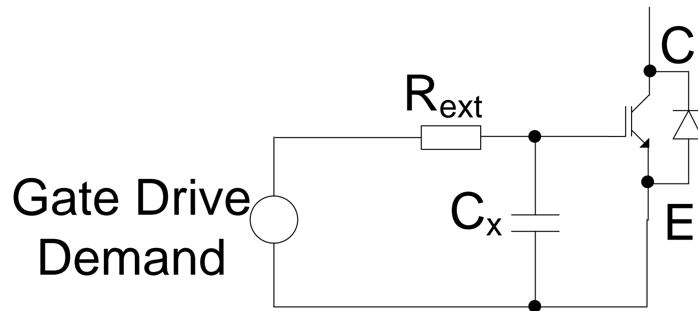
In the literature, many references are given to the influence of dV/dt and di/dt on EMI [59-61]. Special attention is given to circuits which apply special techniques to control these features.

3.4.1 Passive Gate Drive

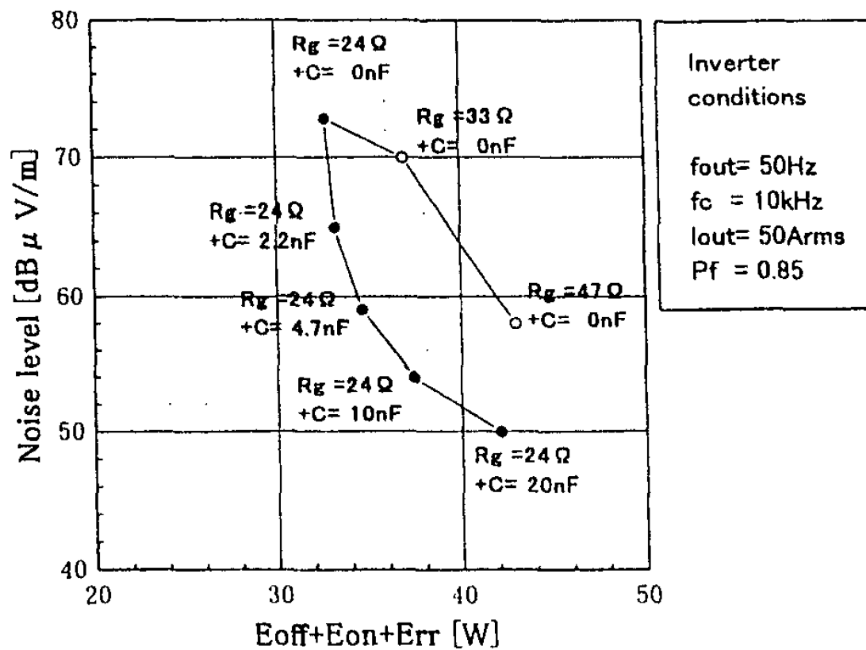
The Conventional Gate Drive (CGD) is passive consisting of just a resistor to control the switching characteristics. Designers of early IGBT gate drives adjusted the value of the gate resistor (R_g) to limit peak current during switch on and limit voltage overshoot during switch off [71, 82]. With improvements in the diode performance for fast switching applications, the stored charge in the diode has been reduced, reducing the peak reverse recover current and this is no longer the major concern when choosing the gate resistance. With advanced IGBT module and dc bus layout, the stray inductance has been reduced which in turn reduces the voltage overshoot at turn off. Different values of gate resistance can be used for switch on and switch off by utilising a diode to control the current flow [83]. In more recent application notes [84-86], reference has been made to use of these resistors to control EMI however the actual value to be used must be determined by trial and error.

A small modification to the CGD circuit has been proposed in [87] by using a capacitor (C_x) connected across the gate emitter terminal (See Figure 3-3). It was suspected that the EMI measured from the VSD resulted from the current ringing driven by the dI_c/dt. During switch on, the increased capacitance in series with the gate resistor slows the dV_{ge}/dt thus reducing the dI_c/dt (as linked via the transconductance). As the capacitance is increased, a smaller gate resistance can be utilised for the required dI_c/dt. During the Miller plateau, the gate voltage remains constant, the voltage across the capacitor has no effect on the gate voltage or dV_{ce}/dt profile. However, the reduced gate resistance allows a larger gate current to flow into the gate charging C_{gc}. The voltage fall time is

thus reduced resulting in a reduction in switching losses. An attempt at radiated emission comparison has been carried out [87] using a loop antenna which shows a small reduction in switching loss and a significant reduction in noise emissions with this gate drive as illustrated in Figure 3-3.



a.



b.

Figure 3-3: a) CGD with Cge added; b) Change in switching loss and emissions with modified gate drive [87].

In [88], the RC network used above was expanded to a T network formed by two resistors and a capacitor (see Figure 3-4). With the particular IGBT under test, it is found that the current flow needed to charge C_{gc} is not all supplied by the first gate resistor (R_{ext}), instead, the voltage at V_{ge} droops a little as charge is taken from the

IGBT parasitic C_{ge} causing current to flow from the external gate capacitor (C_x) via R_{int}. The values of R_{int} and C_x are used to control the dV_{ce}/dt where R_{ext} is used to control dI_c/dt. Correct sizing of the passive components is found to result in a reduction in time for V_{ce} to fall but more specifically, the paper indicates a reduction in tail voltage related to the size of the capacitor. The initial specification for this circuit is for a reduction in switching loss for a defined dI_c/dt limit for the purpose of EMI performance however the reason for this limit and the type of EMI is not discussed.

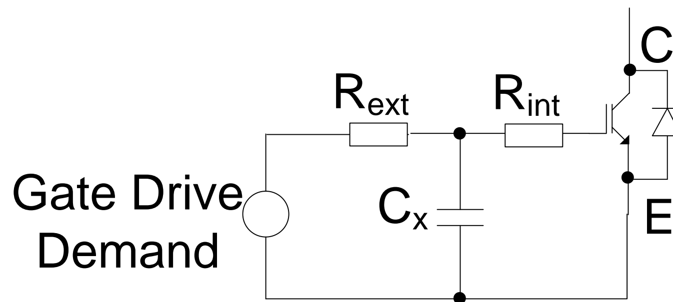


Figure 3-4: T – Network and gate current waveforms.

It has been shown in [89] (as discussed in chapter 2), that the collector current during switch on can be related to the input voltage V_{ge} during the phase from V_t to the beginning of the Miller plateau. During the Miller plateau, the gate voltage is determined by the load current. In the proposed gate drive, the reference voltage V_{ref} is increased to the maximum V_{cc} (see Figure 3-5). The gate voltage at the chip cannot be changed during the Miller plateau using a driver circuit. The gate current can still be controlled during the Miller plateau. Any additional voltage applied by the gate drive is dropped across the gate resistor.

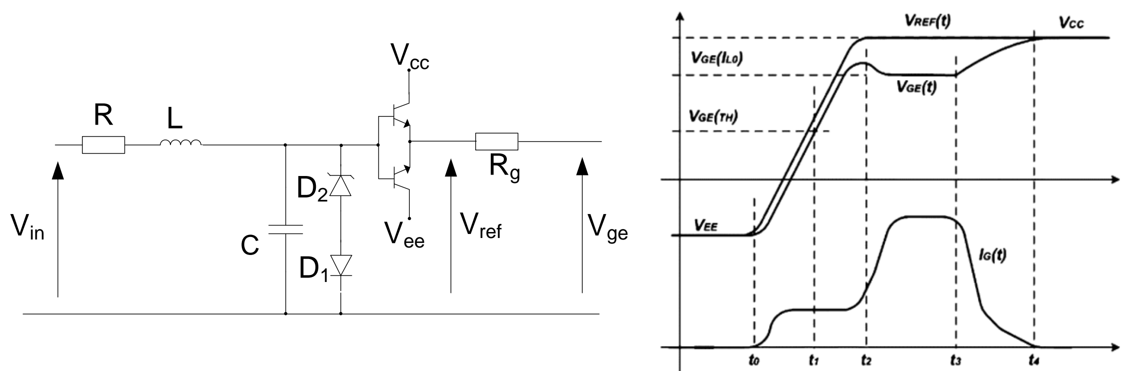


Figure 3-5: Gate profile shaping using an RLC network [89]

The gate voltage shaping circuit consists of a simple RLC circuit (see Figure 3-5) and a current buffer. While the values of the components have been calculated to control the rise time of V_{ge}, the circuit topology is not much different from the conventional gate drive. However, by placing these components before the current buffer circuit, high current can be applied to the gate terminal during the Miller plateau.

A gate resistor has been used by [84, 89] to damp the oscillating circuit consisting of the gate capacitance, and gate and emitter parasitic inductance. The resistance needed for damping is several times smaller than that recommended by the IGBT manufacturers. This circuit is simple to implement and gives good control over the switch on dI/dt. Switch off characteristics have not been discussed. The dI/dt can be calculated and predefined for any IGBT with only a change in buffer and damping resistor needed.

The gate drive shown in Figure 3-5 is evaluated in [90] for short circuit protection during a hard short circuit. This circuit relies on the IGBT saturating, and entering the active region. When operating in this mode, the dI_c/dt can be related to the dV_{ge}/dt with the transconductance. Using this relationship, the gate drive can switch off the IGBT with a limited dI/dt avoiding large overshoots.

During normal switch off operation, the proposed gate drive would continue to shape the gate voltage with the same gradient as switch on. Unfortunately, this would not give optimised control during switch off as the controlled gradient would take place as the voltage was falling and during the Miller plateau and would most likely be negatively biased during the current rise phase. The switch on delay associated with increasing the gate voltage to the threshold voltage has not been considered with this proposal.

For many applications, accurate control of the voltage transient is not required and the objective of the gate drive is to obtain the shortest possible switching time to minimise losses. The patent described in [91] uses a simple passive capacitor positioned from the +15 V supply to the IGBT gate terminal as shown in Figure 3-6. This can give an advantage by reducing the period of instability as V_{ce} begins to fall by minimising the dip in the gate voltage by providing a low impedance path to provide charge to C_{gc}. While this method can reduce the switching losses, care is required in the power up sequence of such a circuit. As the gate drive power supply voltage increases at power

up, a transient current pulse will flow increasing the gate voltage created by the potential divider of the internal C_{ge} and external capacitance C_x. This can momentarily turn on the IGBT causing shoot through and possible device failure if the dc supply is present on the IGBT collector.

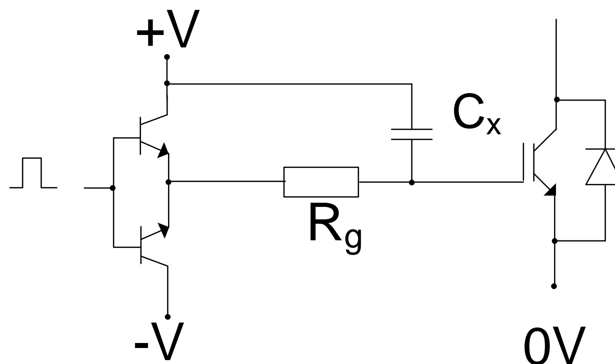


Figure 3-6: Insertion of capacitor to improve stability of voltage transient.

3.4.1.1 Sensing Using Gate Emitter Inductance

Igarashi et al have proposed the use of current feedback within the gate drive to control the gate resistance [92]. A pulse transformer has been included in series with the freewheeling diode to indicate the point where the current begins and ends its transition (see Figure 3-7). During the current ramp, the gate resistance is increased using a MOSFET to restrict the current rise time. While this circuit has slowed the switching transient, oscillations on the voltage transient have resulted from the additional inductance.

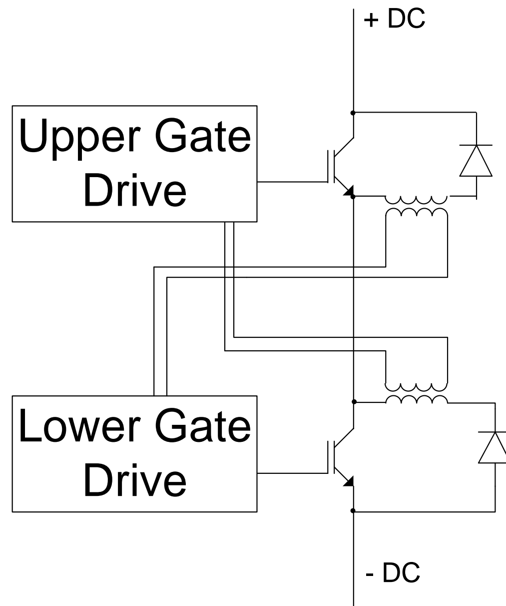


Figure 3-7: Pulse transformer in series with freewheeling diode for current measurement

This method for current control has been improved in [93, 94] where the voltage drop across the emitter stray inductance is used to measure dI/dt. A Zener diode is used to reduce the gate current if dI/dt exceeds a defined level removing the active components. The rated voltage of the Zener diode limits dI/dt where the value of resistor R_z determines the proportional gain for adjusting the gate current. A circuit diagram is shown in Figure 3-8.

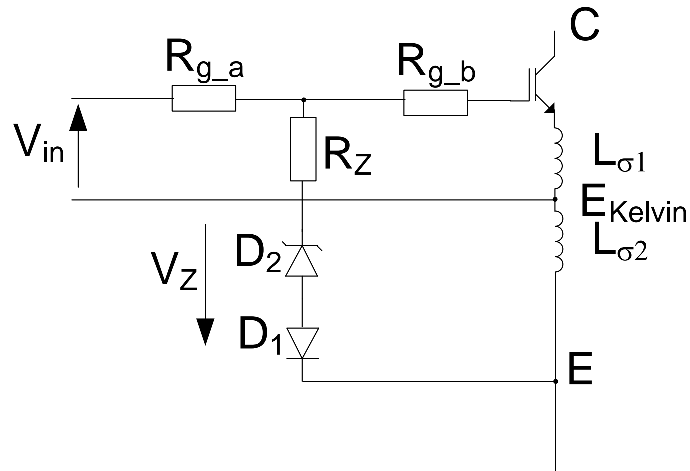


Figure 3-8: dI/dt control using a Zener diode

The problem with the proposed dI/dt control using a Zener diode as the feedback device, is that the maximum V_{ge} will be limited to the threshold voltage of the Zener diode during the IGBT on state (V_z = 12.5V in the example). Operating an IGBT at a low gate voltage will increase the conduction losses in the device significantly. While this circuit has been shown to provide dI/dt control, the current rise time is limited to 600 ns which further increases the dissipated loss compared to open loop control with the same gate resistance. The temperature dependence of the Zener diode threshold also needs to be considered for this design.

3.4.2 Active Gate Drive

Gate drives may contain many active components to realise features such as short circuit protection and are referred to as Active Gate Drives (AGD). This section will only analyse driver circuits where the switching characteristics are actively controlled during normal operation of the device. Initially the implementation of gate drive designs which control the entire switching profile will be presented.

3.4.2.1 Complete Profile Gate Drives

3.4.2.1.1 Three Stage Gate Drive

A 3 stage AGD for a single IGBT has been proposed and evaluated by Vinod [84]. The aim of this gate drive is to limit dI/dt and dV/dt to avoid current and voltage overshoots when switching in a hard switched half bridge circuit.

This design has three different modes of gate control which are selected by the microcontroller and output waveforms (see Figure 3-9):

- Stage I - Rapidly increasing V_{ge} from $-V_{ge}$ to V_t.
- Stage II - Limit dI/dt.

Stage III - Rapidly increasing V_{ge} to V_{gemax}.

The three stages are reversed for switch off with both dV/dt and dI/dt limited in stage II (see Figure 3-10).

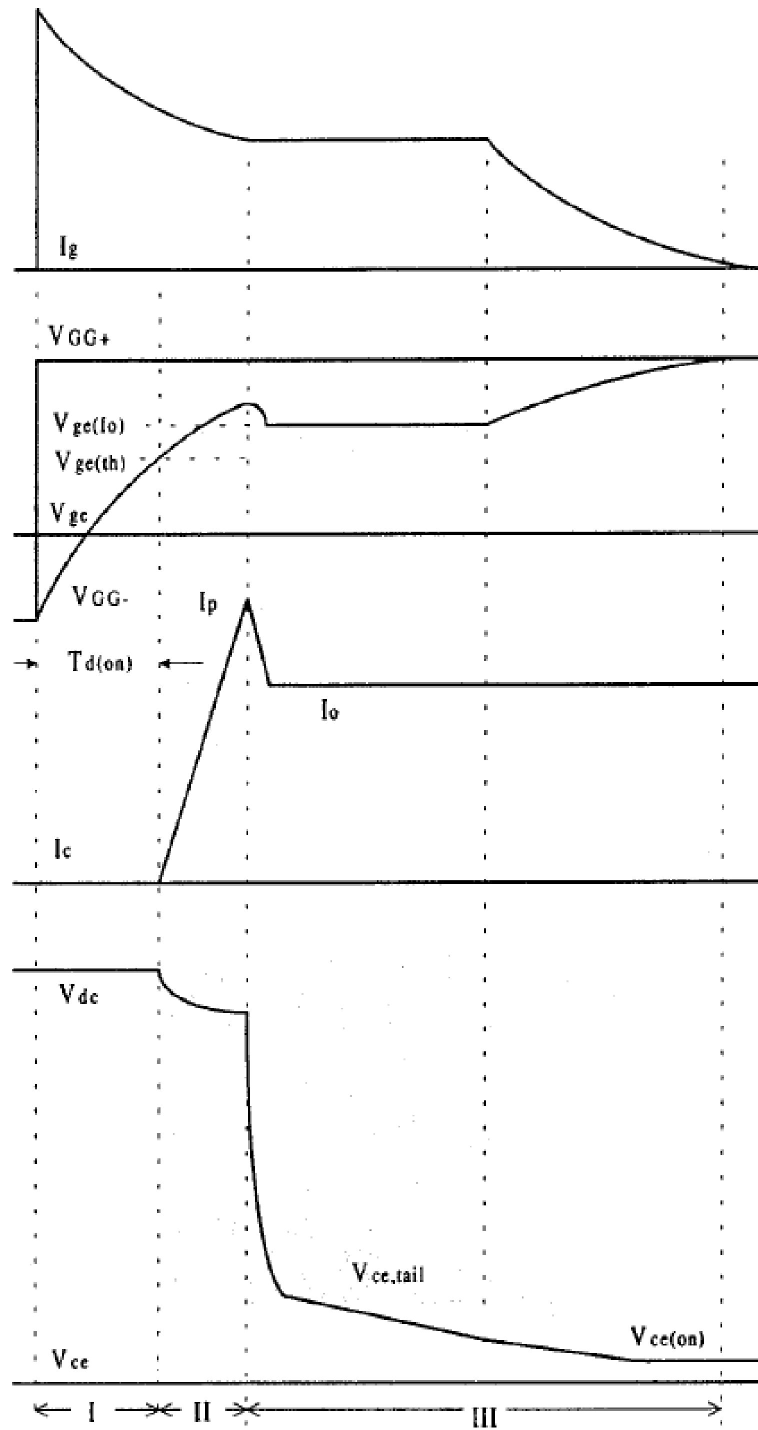


Figure 3-9: Switch on waveforms [84]

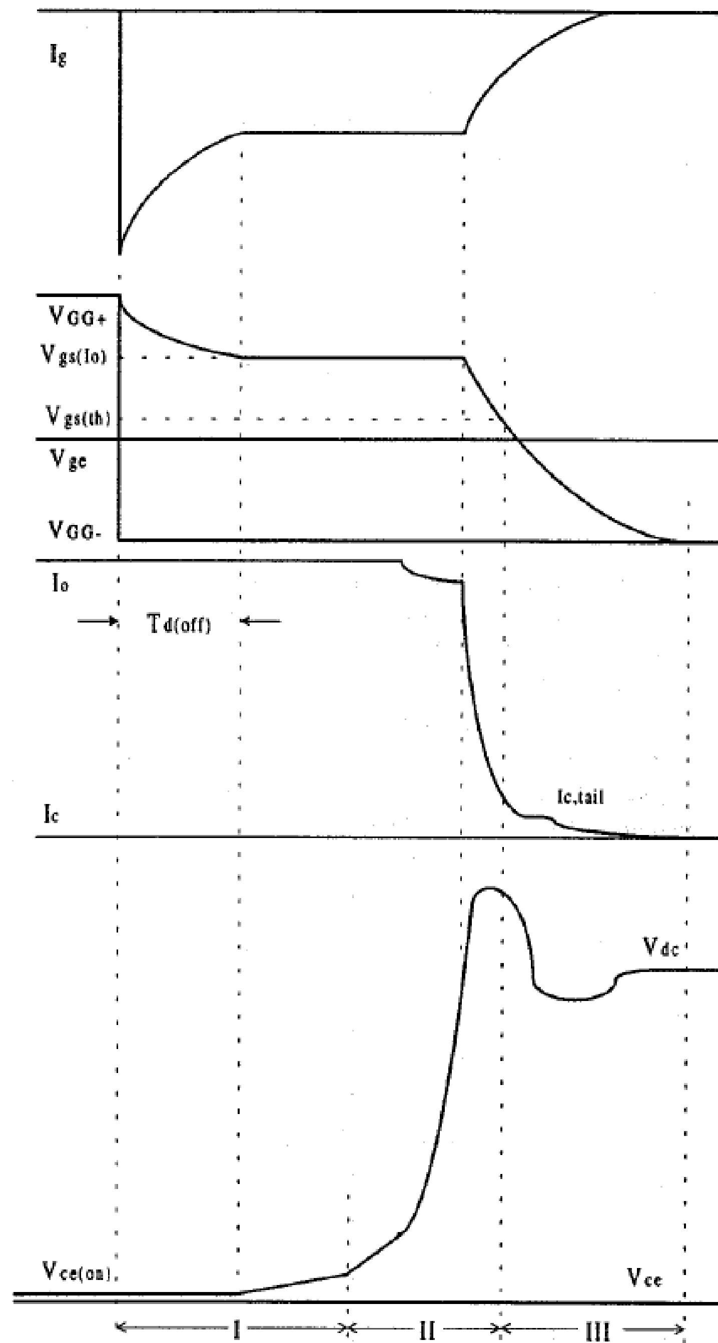


Figure 3-10 : Switch off waveforms [84]

To implement this circuit, two MOSFETS, six BJTs, ten resistors and a logic controller are required as shown in Figure 3-11 (a biased gate supply voltage has been assumed).

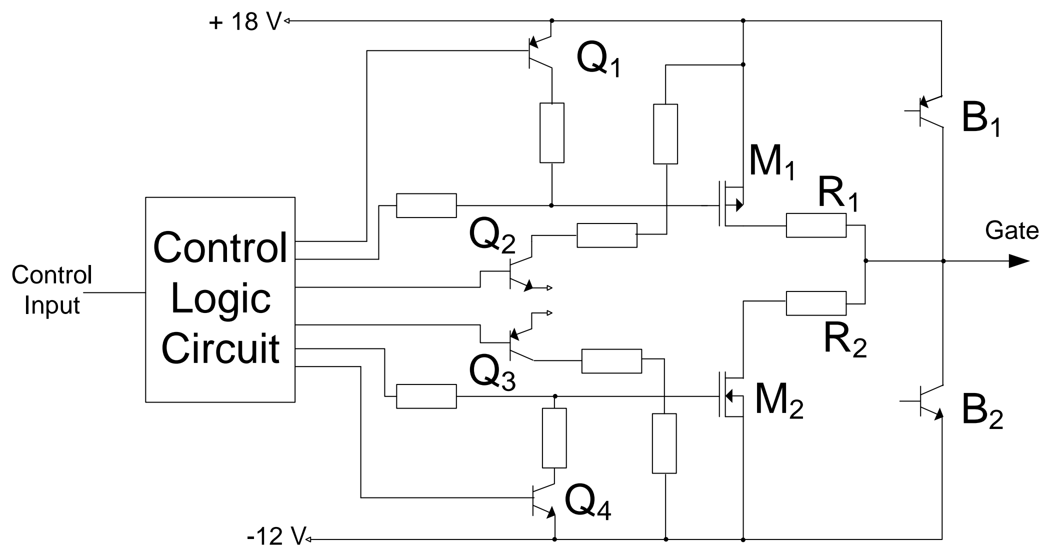


Figure 3-11: Three stage gate drive

For switch on Stage I in Figure 3-9, M_1 is switched on for a predefined time allowing a high current to charge the gate to the threshold voltage. R_1 is used to limit the peak current and provide damping in the gate drive. B_1 is used in the active region to control the current during Stage II. The end of Stage II is detected using the parasitic inductance between the Kelvin and power emitter. M_1 is switched on again to bring V_{ge} up to the 18 V supply voltage.

The proposed circuit has effectively reduced both switch on and off times which would result in better current loop performance. Stage II of this circuit has been designed to limit dI/dt to reduce the peak recovery current and associated ringing due to snap off by utilising a gate current control as opposed to the more commonly used voltage control. Emissions measurements have not been presented to confirm if this has reduced the EMI as claimed by Vinod. By reducing the maximum dI/dt, the waveform has changed significantly resulting in longer switching time for stage II. The increased gate current during the Miller plateau has increased dV/dt and the overall switching time is comparable to the CGD, however the switching losses have increased by approximately 20% for a gate resistance of twice the datasheet value.

The use of the voltage difference between the Kelvin emitter and power emitter to indicate the end of the current pulse is an interesting feature as it allows the gate drive circuit to adapt to different load currents. As identified in the transconductance

equation (2-14), the load current does not change linearly with V_{ge}, hence the imposed limit on the gate current will not give a constant di/dt over the entire rise time. The limit must be set for the highest collector current to be used resulting in a longer than necessary turn on delay for low current conditions.

During switch off, Stage II is initiated as the collector emitter voltage begins to rise. Reducing the gate current at this stage increases the switching time and unnecessarily increases device losses. It would have been beneficial to allow the high gate current to be extracted until the voltage had risen to the dc bus level and then only reduce the gate current to limit dI/dt. However the change-over times are relatively short. The proposed circuit has limited dI/dt and dV/dt but at the cost of increased switching losses when compared to the IGBT manufacturers recommended datasheet. However, if a CGD with Rg = 5.6 Ω is required to achieve the necessary dI/dt and dV/dt the losses in the AGD would be greatly reduced.

A similar two stage gate drive has been presented by Wang where the timing for each stage is determined using a fixed RC network [95]. High current MOSFETS allow the gate current to flow for each stage. The values of the resistance and capacitance in the timing circuit can be different for turn on and turn off and must be selected for each IGBT.

3.4.2.1.2 Feedback Loop

The function of the gate drive proposed by Schmitt [96] uses an EEPROM to define the switching signal for a defined 1 kV/µs voltage transient with reduced switching loss compared to a CGD. As previously seen, the switching profile has been split into various segments. The gate current is increased to its maximum value to reduce the delay time. As the collector current begins to rise, the gate current is reduced limiting dI/dt utilising feedback from the signal measured from the inductance in the emitter leg. Interestingly, the only limitation specified for dI/dt in this paper is the dynamic avalanche of the diode. V_{ce} is monitored using a capacitor and differential op amp. As the voltage begins to fall, the gate current is adjusted to maintain a constant gradient of V_{ce}. A similar closed loop gate drive has been implemented to limit current overshoots at switch on and voltage overshoots at switch off [97]. This circuit used a fast op amp

to control the rise time in 500 ns. Care is required to tune the circuit to avoid oscillations across the operating dc bus voltage range.

Schmitt has not described how the use of the EEPROM memory for the gate profiles is adjusted for the differing load conditions, however it is an interesting combination of digital profile shaping with analogue feedback.

3.4.2.1.3 Conducted Emissions from a MOSFET

A two stage resistance controlled gate drive for a MOSFET is presented in [98]. One large value of resistor is used to limit dI/dt during switch on and switch off (see Figure 3-12). A smaller resistor is used during the Miller plateau to increase the switching speed hence increase dV/dt for the falling voltage. The timing for the second resistor is controlled from an external processor although the details are not discussed. This paper shows that the conducted emissions reduce if the MOSFET is switched slowly and that the switch on of the device has a greater impact on emissions than switch off. It is not clear whether the dI/dt's are the same for the CGD and the 2 stage gate drive. Without this information, the results of this paper in terms of evaluating the gate drive for conducted emissions are inconclusive.

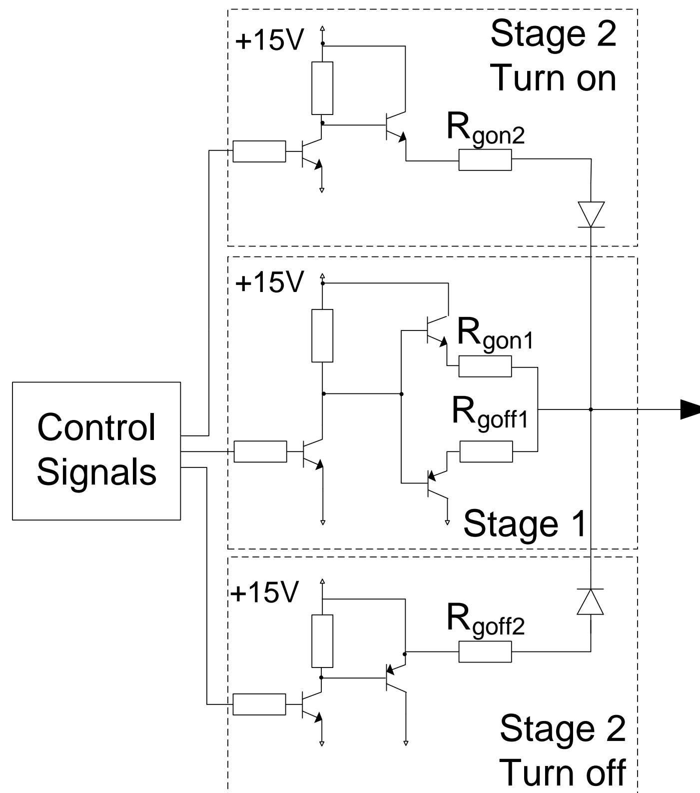


Figure 3-12: Switched resistance gate drive

3.4.2.2 Methods to Control dV_{ce}/dt

3.4.2.2.1 dV/dt Control for Series Devices

Several papers have been published by Palmer for active voltage control whereby the IGBT collector emitter voltage is actively controlled within a feedback loop for series connected IGBTs [73, 74]. A predefined input signal wave shape is created using an integrator circuit (see Figure 3-13). The output voltage ramp is measured using a voltage sense capacitor for each IGBT. The difference between the feedback signal and the demand ramp, results in a control signal used to drive a high current buffer for the IGBT gate. A gate resistance is used to maintain stability of the control loop. The small signal performance is limited by the input capacitance in the presence of the gate resistor.

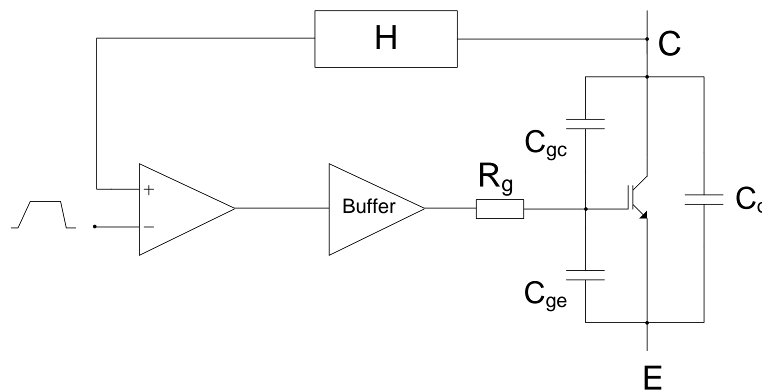


Figure 3-13: Feedback gate drive circuit for dV/dt control

When several IGBTs are connected in series, it is important that all the devices switch together. When the devices are on (low V_{ce}), C_{gc} is greatest hence the lowest bandwidth.

In [74], an initial bias step has been added to the control signal to ensure all IGBTs are in the high bandwidth controllable region before the dV/dt control is implemented (see Figure 3-14).

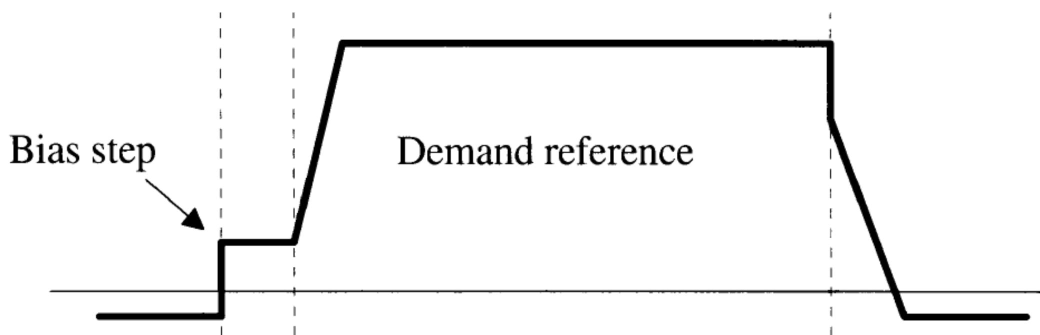


Figure 3-14: Bias Step added to Voltage demand

The limit of the bandwidth is determined by the IGBT and gate resistor, however details are not given of how this translates to a maximum dV/dt. A limitation imposed by the bandwidth may restrict the control of radio frequency components responsible for radiated emissions.

Very high bandwidth op amps are required to give adequate voltage control. A 180 MHz controller has been used in [99]. The amplifier gain and feedback gain are adjusted and an additional active snubber is placed between the collector and gate. This resulted in a controlled dV/dt of 2.7 kV/us. The addition of the active snubber allowed

the control loop to be stable with a smaller value for the R_g, resulting in lower switching losses. Exact details of the active snubber circuit have not been provided.

Park has used a feedback capacitor from the IGBT collector to sense the change in V_{ce} [100]. This has been utilised with a current mirror to alter the current injected into the gate terminal. The required dV/dt for both switch on and off can be determined by adjusting the parameters of the current mirror. While it has been shown that this control works well over a range of dc bus voltages, the fastest controlled rise time when operating at 600 V is 2.3 kV/μs giving a rise time of 260 ns which is not particularly quick.

3.4.2.2.2 dV/dt Limiting

In [93] dV/dt is sensed and differentiated using a capacitor connected to the collector. In this setup, dV/dt is not controlled, just limited by reducing the gate current if the dV/dt exceeds the required limit. The details of the opamp have not been included. The ramp is limited to 1 kV/μs. This is not a particular fast rate and as such has increased the losses in the device, however losses are not the most important control item in this case. A similar dV/dt control is used in [94].

3.4.2.2.3 dV/dt Control for Conducted Emissions

A dV/dt control strategy presented in [101] uses a four stage resistor control to get a good compromise between conducted emission and IGBT performance. Only one resistance value is used during a switching cycle the value of which is chosen depending on the output current. In this case compliance to the standards required the average conducted emissions to be below a defined limit. The dV/dt and magnitude of emissions for a given gate resistor value is measured. By using a small resistor at high output currents, the switching loss could be reduced at the sacrifice of higher conducted emissions. At lower output currents, the switching loss increase is less significant compared to the reduction in conducted emissions.

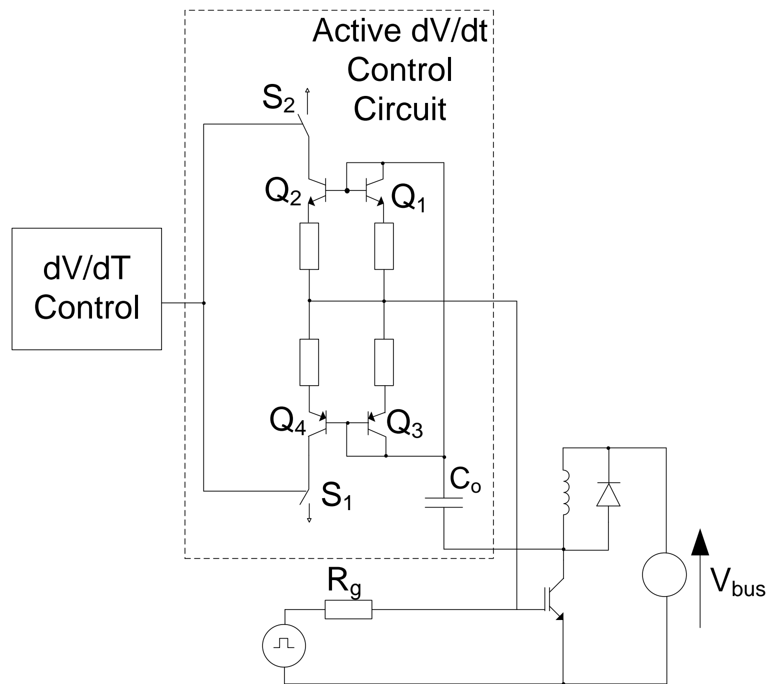


Figure 3-15: Gate drive schematic for control of conducted emissions.

Figure 3-16 illustrates the choice of resistance value. The optimisation function indicates the ratio between switching loss and conducted emissions. A lower optimisation function gives the best solution. This diagram indicated a different resistor value in 4 different current regions.

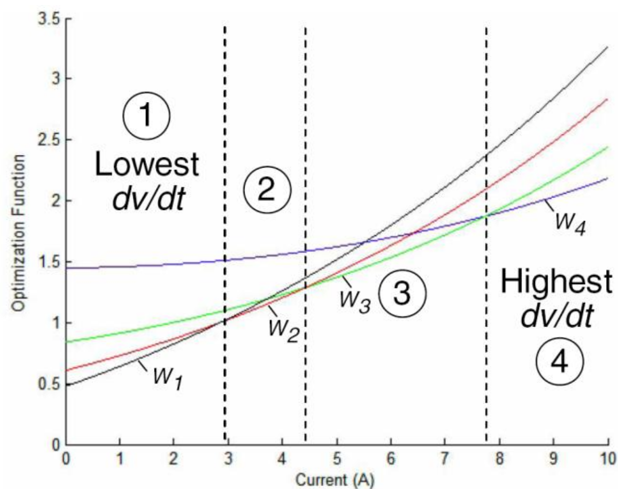


Figure 3-16: Optimisation of four stage dV/dt control [101]

In an application with a fixed frequency output, four different values of gate resistors are used giving, on average, a reduction in loss and also passing the conducted emissions standards. This circuit would not be effective for variable frequency products

as the benefit of the averaging of conducted emissions could not be used for stationary vectors or low output frequencies. However, such a circuit may find a use in a fixed frequency application such as a dc to ac converter supplying power to a mains network. In this case, the noise is measured using an average detector in which high levels of noise can be tolerated for a short period of time. Most radiated emissions standards for a VSD require measurements to be made using a peak or quasi peak (QP) detector with a 120 kHz bandwidth. In these cases it is not possible to take advantage of averaging the noise.

3.4.2.2.4 Parallel Gate Current Source / Sink

In [86], the author is only concerned with limiting conducted EMI (150 kHz – 30 MHz). To achieve this, a conventional gate resistor is used to limit dI/dt during switch on and switch off to a value where conducted emissions would pass the test. To minimise the switching loss, high gate current is applied to the gate in parallel to the gate resistor during the Miller region to increase the dV/dt. By reducing the time for the voltage to fall, the switching losses have been reduced. The point where the high current is enabled is determined by sensing the gate voltage. This solution would work for all values of output current. The dynamic performance of the current source is not discussed however, it is suspected that without some damping resistance the gate voltage of the IGBT may oscillate causing unwanted EMI. Radiated emissions and the snap off performance of the diode are not considered.

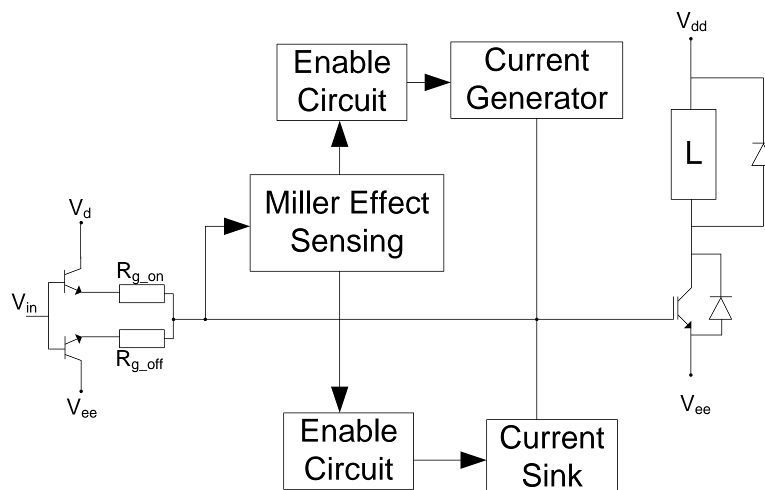


Figure 3-17: Block diagram of high current gate drive.

3.4.2.3 Methods to Control dI_C/dt

3.4.2.3.1 Feed Forward Gate Drive

In [100] a small external inductance has been added in series with the emitter of the IGBT. The change in current through the inductor is detected as a voltage and used to actively control the gate voltage via the device transconductance to control the gradient of the current. This method has been shown to work well and the rate of change of current can be programmed by the correct selection of components in the current mirror. This circuit is also evaluated with the dV/dt control discussed earlier without any detrimental interaction. However adding additional inductance in series with the emitter is not usually desirable due to the resulting voltage overshoot at turn off. In the example given, the rate of change of both voltage and current have been restricted without consideration of switching loss.

3.4.2.4 2 Stage Switch Off

In [94], a 2 stage switch off has been implemented to limit the dI/dt and hence limit the voltage overshoot. A schematic for the gate drive can be seen in Figure 3-18. As V_{ce} begins to rise beyond 15 V, the low gate impedance path through the MOSFET T2 is disabled giving a higher gate resistance for switch off.

In an ideal driver circuit, the high impedance gate drive should not be used until the moment the collector current begins to fall. By sensing for a change of 15 V in V_{ce}, the high impedance may switch on too early unnecessarily increasing the device losses. The driver circuit would have to include the time delay between detecting the voltage rise and changing the impedance of the gate path. This would be different for every IGBT and would have to be calculated.

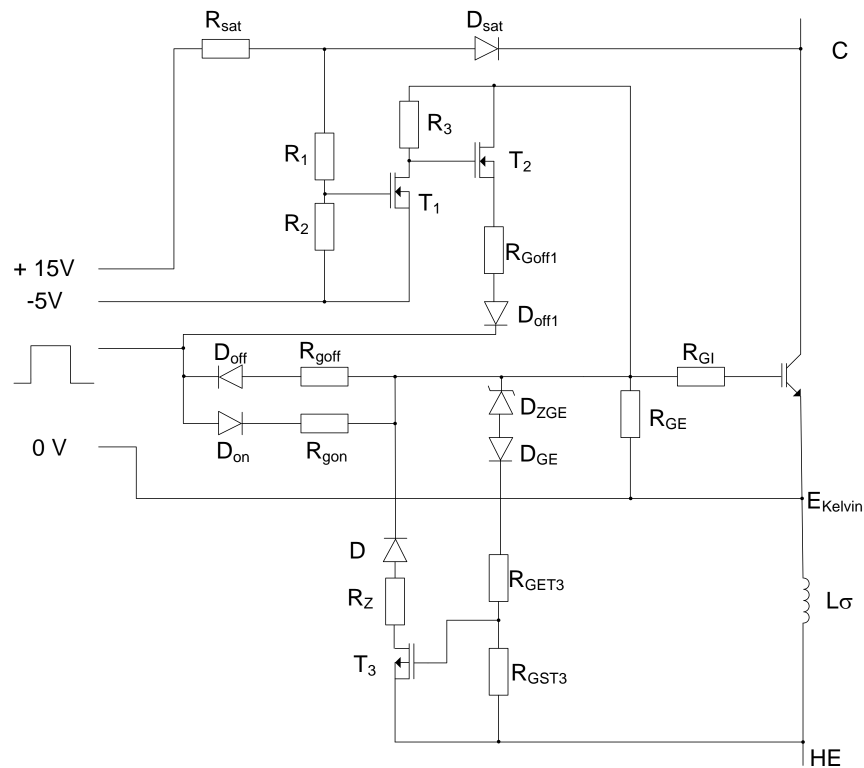


Figure 3-18:Two stage switch off gate drive

3.4.3 Reduction of EMI

Radio frequency electromagnetic interference (EMI) can be separated into four categories and the limits given in standards for VSDs [2]:

- Conducted Emissions
    - 150 kHz to 30 MHz signals imposed onto the power cables from the equipment under test (EUT) and transmitted to the mains supply network.
- Conducted Immunity
    - The EUT should function correctly when radio frequency signals from other equipment are coupled onto the supply and control cables.
- Radiated Emissions
    - Signals in the frequency range 30 MHz and above radiated from the EUT and associated cables.
- Radiated Immunity.

- o The EUT should function correctly when subjected to an electromagnetic (EM) field at a defined field strength and frequency range. Radiated immunity does not tend to be a problem for IGBTs due to the relatively large voltage thresholds and capacitances in the gate drive circuits.

These interference limits are concerned with protecting other products however care needs to be taken within a VSD to ensure immunity to its own switching signals. An example of this within the gate drive is the current which flows through parasitic capacitances in the IGBT due to the high dV/dt which can falsely trigger the complementary gate drive. This is often protected by a negative gate supply rail or additional external gate emitter capacitances.

Depending on the application of the product, each of the EMI categories will have permissible limits defined by product standards. For both conducted emissions and radiated emissions, detailed linkages between IGBT switching and EMI need to be evaluated, however, the papers researched above indicate a relationship between dI/dt and dV/dt and the measured emissions where in general, faster switching of IGBTs is related to increases in EMI however there does not appear to be an appreciation of the exact mechanisms involved. This lack of clarity is reflected in the presented solutions where some gate drives control dI/dt, while others control dV/dt and both claim to reduce EMI emissions. Given the references to both dI/dt and dV/dt control when considering EMI, it is important to understand whether the signals measured in a radiated emissions setup are related to the electric or magnetic field.

In many circuits output transients have been controlled using snubber components on the high power side of the device [93]. These components can be large, expensive, dissipate power and if not damped correctly can lead to resonance at radio frequencies.

In an effort to reduce emissions, the active gate drive proposed in [84] is evaluated in [85] by comparison to a conventional gate drive. It is interesting to note that during testing, both gate drives operated with the same dI/dt (100 A/us). Both conducted emissions and radiated emissions are measured. In both cases, the emissions were reduced using active control. This would imply that both emissions depend on dV/dt. In other papers [86], dI/dt are cited as responsible for the conducted emissions.

Several papers refer to oscillations between parasitic capacitance and inductance within the modules as a cause of the measured radiated emissions. Voltage and current waveforms have been captured but do not clearly indicate any oscillations. The resonant frequencies of the loops in a module and estimates of the circulating current have been used to identify the emission sources however, the influence of the cable has not been considered for these tests [102, 103]. It has been found from measurements, that a motor cable must be attached between the VSD and motor for any significant radiated emissions. The frequency analysis of a trapezoidal waveform presented in chapter 2 has shown that oscillating features do not need to be present for a signal to contain radio frequency components.

To illustrate how a pulsed signal can be translated into narrow band oscillations, an example of a plucked guitar string can be used. When a guitar string is plucked, (step input), the string will oscillate for some time at a defined frequency. If you pluck it harder, the frequencies remain the same but the amplitude increases. The same analogy can be applied to an antenna structure such as the cable where a step input EM wave is applied. Natural frequencies will resonate transmitting higher emission levels than other frequencies. The duration of the oscillation depends on the damping in the antenna at that frequency and the magnitude of the step input. The receiver averages the measurement over a time period defined by the bandwidth (discussed in chapter 4.6). Likewise, a step input to the receiver can give varying levels of narrowband measurements.

Attempts have been made by Rosales to create a three dimensional model of a drive and motor system connected via a cable and to evaluate this system for both radiated and conducted emissions utilising finite elements [104]. It is encouraging to find research into this area, however at present the models lack the necessary detail to accurately describe a practical system over the wide frequency range. The emissions sources have been modelled as time harmonic waves, the cables have solid shields and the motor model is simplified, neglecting the complex impedance of the parasitic capacitance between coils and the frame.

Several attempts have been successfully made to model the conducted emissions from a drive utilising measured or modelled dV/dt signals [105]. This can give reasonable accuracy at the lower frequencies associated with conducted emissions for a specific system layout however, the accuracy reduces at the frequencies increase. At present the most reliable method to determine the RF content is via measurement on an OATS.

3.5 Summary of Chapter 3

This chapter has presented a summary of the published literature on gate drive topologies including a description of the main features of the gate drive which are related to the switching performance. The commercial gate drive solutions tend are feature rich in terms of protection and cost effective if all features are required however, care needs to be taken to ensure the correct driver is chosen for each application.

Several novel gate drives have been presented where the switching pattern has been adjusted to achieve specific results such as voltage sharing in series connections, limited voltage overshoots and reduced conducted emissions. There is a common theme of minimising the switching loss in the devices and reducing switching times for improved control. The additional benefit of reducing switching delays using the gate drive hardware needs to be balanced against the increased cost and complexity of the circuits versus delay compensation algorithms in the control software. Several of the active gate drives have reduced the switching times of the IGBTs and improved control performance. In such cases, the switching time may vary with output load conditions and this should be considered when evaluating the benefits to control systems.

The novel gate drives have demonstrated that it is possible to control or limit dI/dt and dV/dt using the gate of the IGBT. This removes the need for large lossy snubber components. The gate drives performance can be adapted to the operating conditions providing optimum efficiency within the IGBT constraints such as voltage and current rating. There appears to be a difference in opinion between gate drive designers to the best method of timing the various stages of switching profiles. Several have opted for external, preconfigured times while others use feedback from the output signals. The use of the feedback signals could be subject to noise and must be designed with suitable

immunity. The predetermined time intervals do not adapt to operating conditions and may not give the optimum performance.

Many of the papers presented have attempted to design a gate drive with the intention of reducing electromagnetic emissions. There is disagreement in these papers to the source and mechanisms of both conducted and radiated emissions. This needs to be determined before a suitable gate drive can be designed.

It is clear that the control of the switching transient of an IGBT can be separated into stages, related to changes in the output waveforms. This has been achieved initially using open loop control where the shape of the gate emitter voltage transient is shaped either passively or with active components corresponding to predefined timing routines. These strategies have been further improved with a closed loop performance to determine timing between the different stages and then to control the slopes of the transient voltages and currents. While it has been demonstrated that control of these features is possible, it is not clear how the dV/dt and di/dt influence the radiated emissions measured from a VSD system.

Chapter 4: Practical Measurements of IGBT Switching and Radiated Emissions

4.1 Introduction

The staged control of an IGBT output voltage and current utilising the gate transient was discussed in chapter 3. Frequency analysis of a typical switching signal with different profile characteristics was presented in section 0 where it is shown, for example, that for a rise time of 100 ns, the frequencies associated with radiated emissions are contained in the fine details at the switching corners and not strictly related to the entire rise time. This chapter will illustrate the ability to control an IGBT to remove the features responsible for radiated emissions and define the specifications of a gate drive to test for radiated emissions.

The switching transients associated with IGBTs and diodes are of the order of hundreds of nanoseconds duration. To capture and analyse the transient trajectory of the voltages and currents requires equipment with a high bandwidth, high voltage and high current capability. The limits of this equipment will be discussed together with methods to improve the measurements. Several tests are carried out to determine the limits of control of the IGBT transient features and their correspondence to the semiconductor theory presented in chapter 2.

The switching transients are heavily dependent on the impedance of the dc link bus bar. An analytical study of the impact of switching loss is presented as a guide to future design and influence on radiated emissions.

Repeatable measurements of radiated emissions in an open area test site are not easy. It is important to establish the effect of the setup on the measured results. The requirements for compliance with international standards shall be discussed together with precautions taken.

4.2 Pulse Test Setup

For a given IGBT operating point i.e. fixed voltage, load current and temperature, the influence of the gate voltage is determined with the intention of controlling the radio frequency content in the switching signals. When operating at fixed load current, the

transient times for the voltages and currents are constant for each switching pulse. Under these conditions, as has been discussed in chapter 3, a feed-forward gate drive signal can be used with predetermined timings to control the current and voltage transients independently. A 100 MHz arbitrary waveform generator (ARB) was used to generate a programmable gate signal and evaluate the response of the IGBT.

When evaluating radio frequency content in the transient signals, it is important to avoid coupling signals from external sources such as the dc power supply. A test rig was constructed as illustrated in Figure 4-1 with the block diagram shown in Figure 4-2.

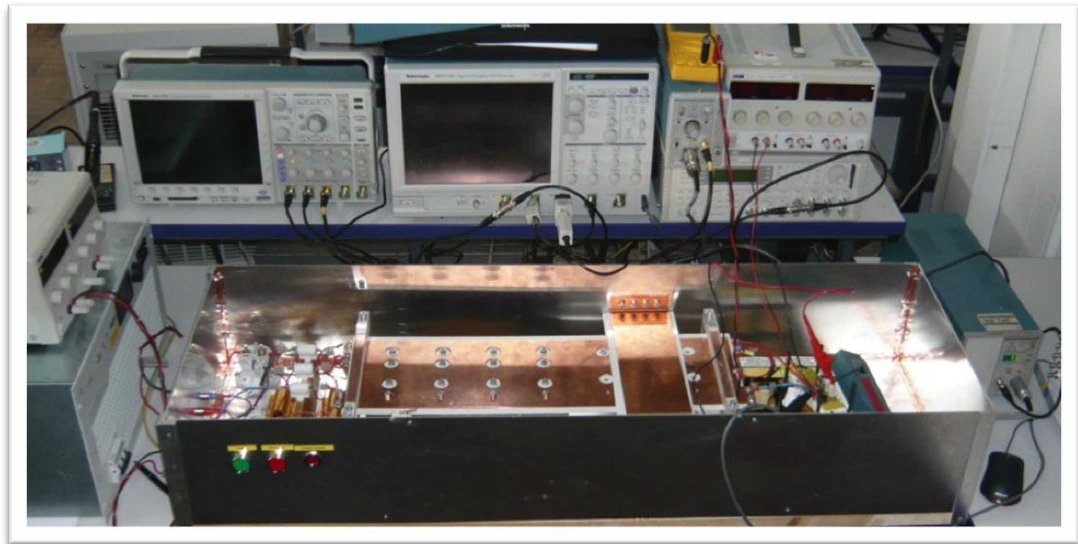


Figure 4-1: Photograph of Pulse Test Rig

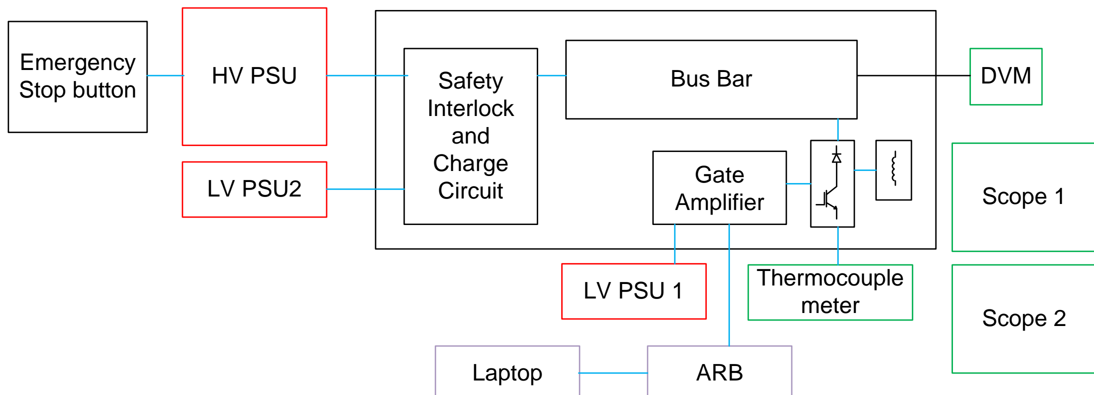


Figure 4-2: Block Diagram of Pulse Test Rig

The bus bar connects eight 2200 μF electrolytic capacitors capable of supporting a dc bus voltage of up to 800 V. The high voltage power supply unit (HV PSU) provides the

dc voltage to charge the capacitors when the charge circuit is enabled. When the dc bus is charged, it is isolated from the dc power supply using low capacitance reed relays to attenuate any coupled radio frequency signals from the HV PSU (see Figure 4-3).

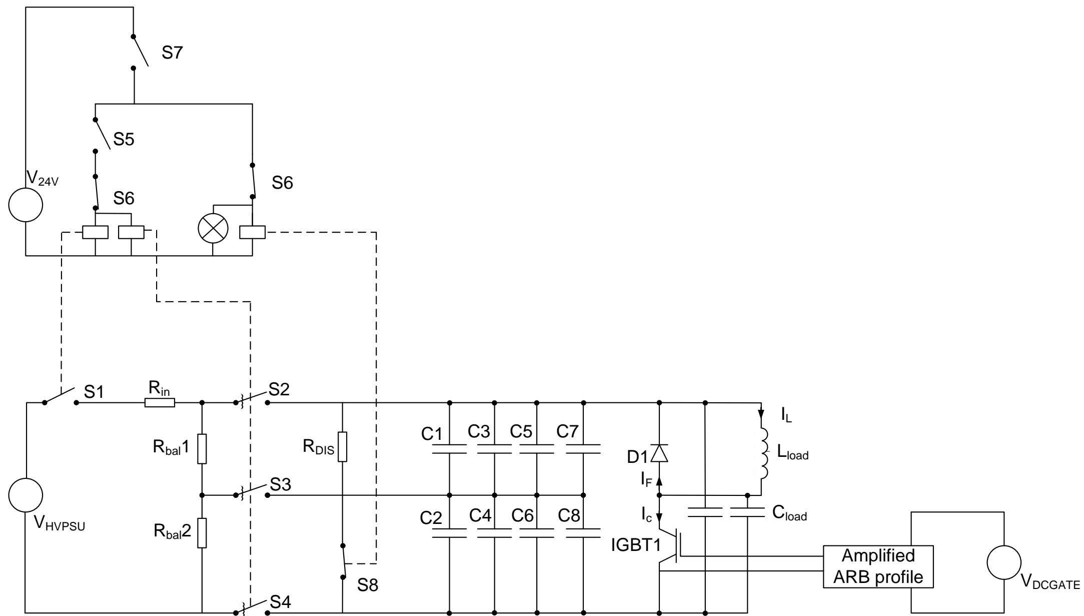


Figure 4-3: Pulse Test schematic

The pulse test profile can be programmed into the ARB where an initial pulse allows the IGBT collector current to ramp up via the load inductor, the switch off transient at this point can be captured on the oscilloscope and further analysed. After a short pause where the inductor current is carried in the freewheeling diode, the switch on IGBT transient is captured (see Figure 4-4). The control signals from a microprocessor in a VSD give a step change in switching demand at each transition from on to off and vice versa. By using the ARB to control this switching signal, the shape of the transient is controlled to evaluate specific features of the IGBT transients. The current from the ARB has been amplified using an emitter follower with a suitable bandwidth.

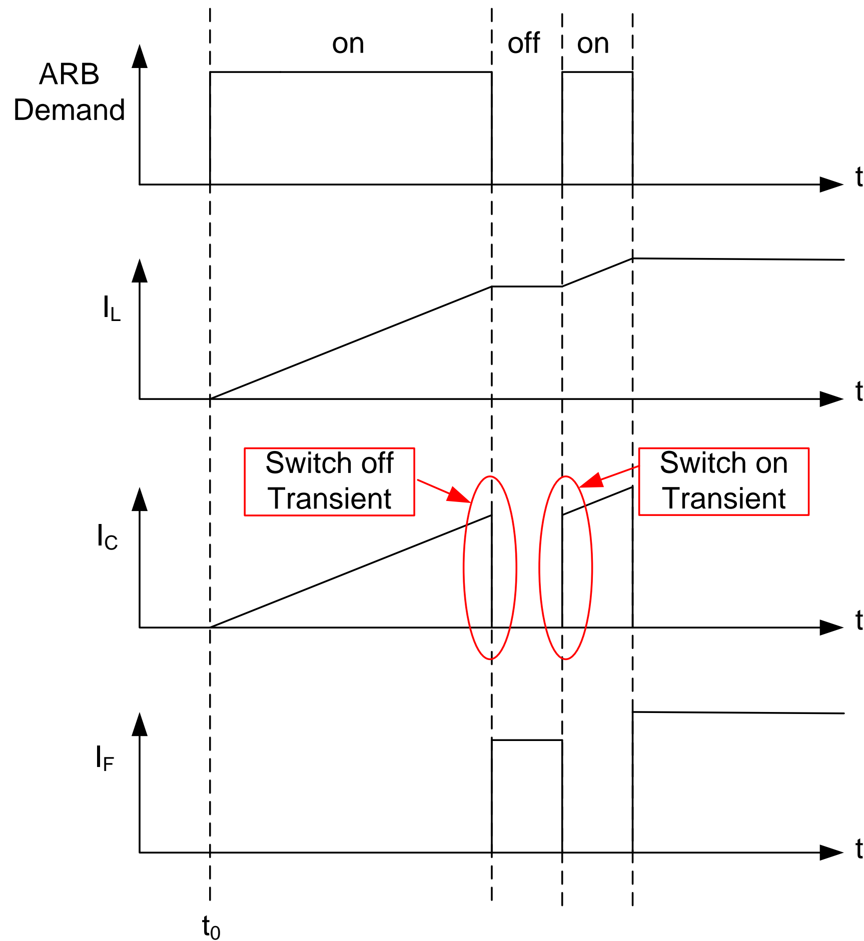


Figure 4-4: Timing diagram to achieve desired current level

4.3 Measuring Equipment

The transient collector emitter voltage, collector current, gate emitter voltage, gate current, demand signal and load current are captured using the oscilloscopes (DPO7453). The captured data is analysed using Matlab® to determine the switching loss and radio frequency content. All signals are sampled every 200 ps for 10000 points (2 µs) to ensure the bandwidth would be adequate for analysis up to 100MHz. The voltage probes (PHV641-L) have a bandwidth of 380 MHz while the dc current probes (TCP0030) have a bandwidth of 120 MHz. A time delay of 14 ns is observed between the voltage and the active current probes however compensation for this delay is included in the Matlab® analysis by time shifting the signals. The influence of current probes and voltage probes on the measurements is discussed below. Parasitic inductance in the module bond wires may lead to the voltages at the chip being significantly different to those measured at the terminals [78], however in this

investigation, loss measurements are only made for comparison and not used for a thermal design.

A type K thermocouple is attached to the underside of the IGBT module in a channel (1.5 mm x 1.5 mm) milled into the copper base plate directly under the IGBT under test using Loctite™ Output 384 thermal adhesive. The IGBT is mounted on a power resistor (HS300) which is used to heat the device above ambient temperature by controlling the applied voltage. All measurements are taken after the temperatures have reached steady state where it is assumed that the IGBT junction temperature is equal to the measured case temperature. Assuming that the switching energy during each pulse test is dissipated throughout the entire IGBT silicon volume, a typical energy pulse of 20 mJ would cause temperature rise of 4.86°C (See Appendix E). The effects of temperature on the radiated emissions will be considered in chapter 5.

4.3.1 Measuring Radio Frequency Content from Transient Signals

The oscilloscope used to capture the switching transients has a bandwidth of 3 GHz and is more than adequate to capture signals in the time domain for analysis of frequencies of interest up to 100 MHz. Signals with high frequency content are often used for communication purposes or clocks in digital systems which operate at low voltages (less than 5 V), however, the voltages switched by the IGBT are several hundreds of volts. The vertical resolution of a typical laboratory oscilloscope is eight bits which can be extended to ten bits by averaging multiple data captures. With an IGBT operating with a 600 V dc bus, the vertical resolution must be set to at least 100 V per division to capture any voltage overshoot which may occur. The minimum voltage increment which can be recorded with this setting is 4 V. Typical time domain switching signals are analysed below in the frequency domain using Fourier analysis to determine the frequency content.

As only the transient is captured, there will be a large discontinuity at either the beginning or end of the data depending on whether the it is a turn on or a turn off transient. This discontinuity will mask the high frequency content of the transient and is usually minimised using windowing. With a transient signal between two constant dc levels, it is possible to completely remove the spectral leakage from the discontinuity

while perfectly preserving the radio frequency content. To implement this, a mirror image of the signal about the discontinuity can be created. The newly combined signal (original and mirror image) will remove one of the discontinuities. The dc component of the switching signals are not of interest for the evaluation of radio frequency content hence the entire mirrored signal can be offset so the beginning and end values have zero amplitude.

While the actual voltage measurements are necessary to capture time domain information, a high pass filter will remove the large magnitude, low frequency components while preserving the essential radio frequency content bringing it within the dynamic range of the oscilloscope. Active filters operating with a high voltage and high bandwidth are not available so a passive filter, designed to attenuate frequencies at 1 MHz and below by 100 dB was constructed. A 6th order filter is required to obtain the required attenuation as shown in Figure 4-5. The frequency response shown in Figure 4-6 was simulated using SIMetrix® SPICE programme, where 100 dB attenuation has been achieved at 1 MHz (blue line). A measurement of the constructed filter frequency response is also shown giving good correlation to the simulation between 5 to 80 MHz with some resonance features around 90 MHz due to the parasitic capacitances from the layout of the discrete components (green). The measured results are used in further calculations.

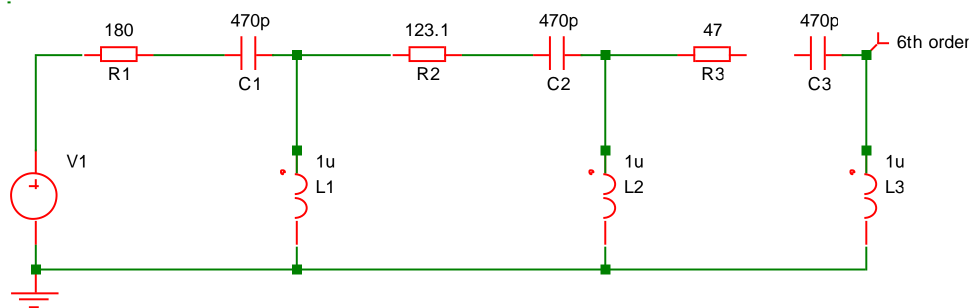


Figure 4-5: Passive filter schematic

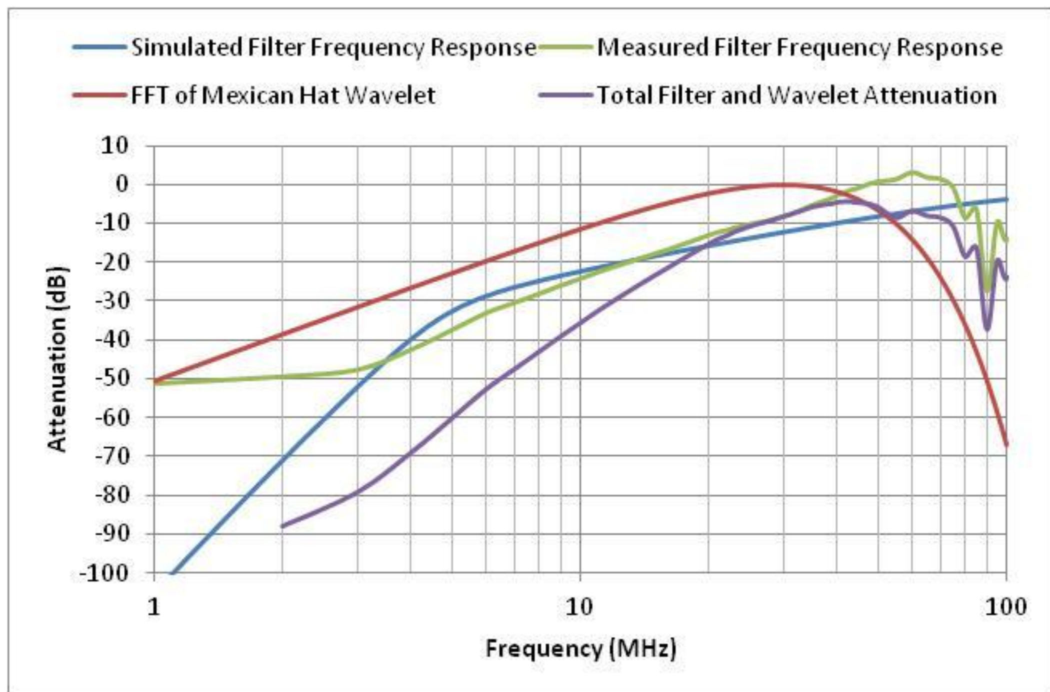


Figure 4-6: Frequency Domain Filter and Wavelet Attenuation

A measured V_{ce} signal and a V_{ce} signal filtered through the 6th order filter can be seen in Figure 4-7a. A Discrete Fourier Transform (DFT) of these signals is given in Figure 4-7b. The Fourier analysis of the V_{ce} trace can be seen to have a significant high frequency content which rolls off at approximately 20 dB/decade. This is due to spectral leakage from the discontinuity at the beginning of the signal as discussed earlier. Fourier analysis of the mirrored signal illustrates how significant this spectral leakage can be and uncovers the actual radio frequency content in the signal.

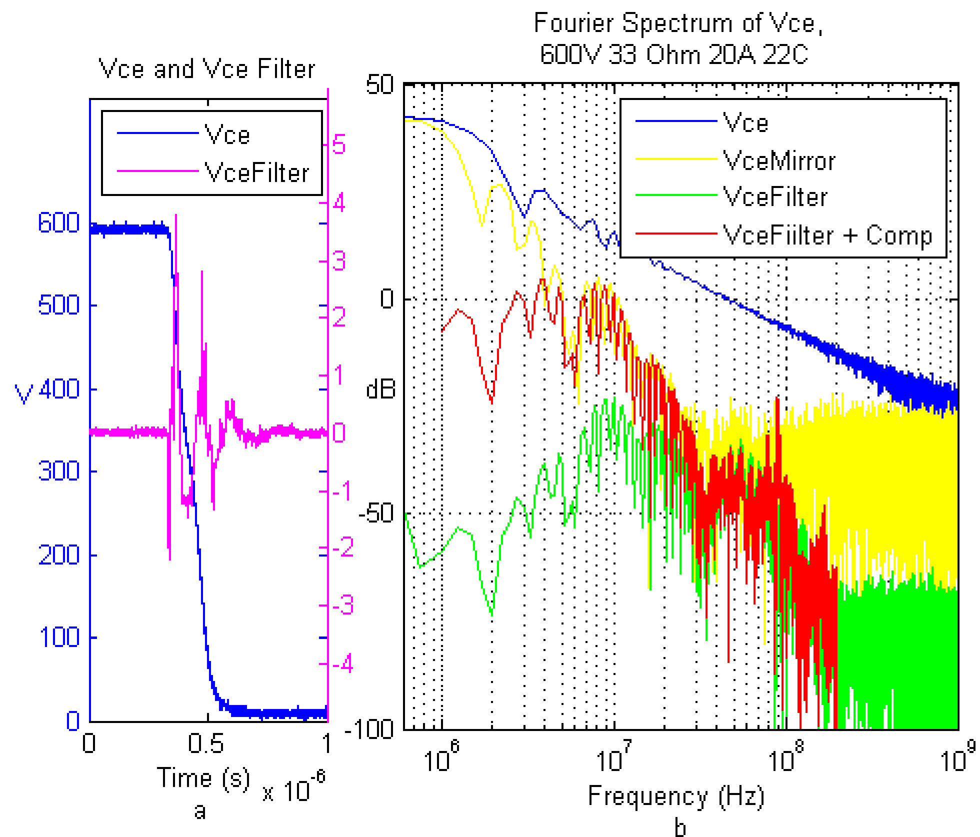


Figure 4-7: a) Captured V_{ce} and V_{ce} filtered signals; b) Fourier analysis of voltage signals.

Due to the limitations in the oscilloscope vertical resolution, the noise floor is reached due to quantisation error from the analogue to digital converter when the amplitude has fallen by 49.92 dB using the standard equation given in [106]. The analysis presented in section 0 has illustrated that a fixed attenuation gives different bandwidths depending on the wave shape. For example, consider two trapezoids with different rise times. The amplitude of the envelope in the frequency of a trapezoid with a rise time of 200 ns has decayed by 49.92 dB at 55 MHz. However for a rise time of 100 ns, a 49.92 dB attenuation does not occur until 77 MHz.

From the observed V_{ce} measurement in Figure 4-7, the rise time is 155 ns however the noise floor restricts the measurement of frequency beyond 30 MHz. This implies that the measured signal is not an ideal trapezoid but includes further break points which attenuate the higher frequency content. To accurately measure the frequency content of the signal, the lower frequency components must be attenuated before measurement by the oscilloscope as illustrated with the high pass filter. By utilising the passive filter,

the frequency where the noise floor begins can be extended towards 200 MHz as the vertical resolution on the oscilloscope can be increased. As the attenuation response of the filter is not ideal, the amplitude of the filtered signal can be compensated across the known frequency range. This is shown in the red trace in Figure 4-7b which shows good agreement to the unfiltered signal between 5 MHz and the noise floor.

The Mexican Hat wavelet has a finite duration in the time domain and hence is useful to locate the position of frequency components in time with a known accuracy and linear phase. The frequency response of the wavelet with a 30 MHz pseudo frequency is shown in Figure 4-6.

Applying the wavelet analysis to a measured turn on voltage waveform (wV_{ce}), features with radio frequency components can be identified in Figure 4-8. A corresponding signal measured using the physical high pass filter (V_{ce} filter) is shown in magenta. The collector current is shown for reference where it can be seen that the diode recovery does not display excess snappiness. The wavelet analysis of V_{ce} has identified four peaks of radio frequency emissions which can be correlated to features in the switching transient:

- Point 1: V_{ce} drops due to I_c beginning to rise (wV_{ce_1});
- Point 2: dI_c/dt reaches maximum rate of change(wV_{ce_2});
- Point 3:V_{ce} begins to fall as diode supports voltage(wV_{ce_3});
- Point 4: V_{ce} reaches IGBT saturation (wV_{ce_4}).

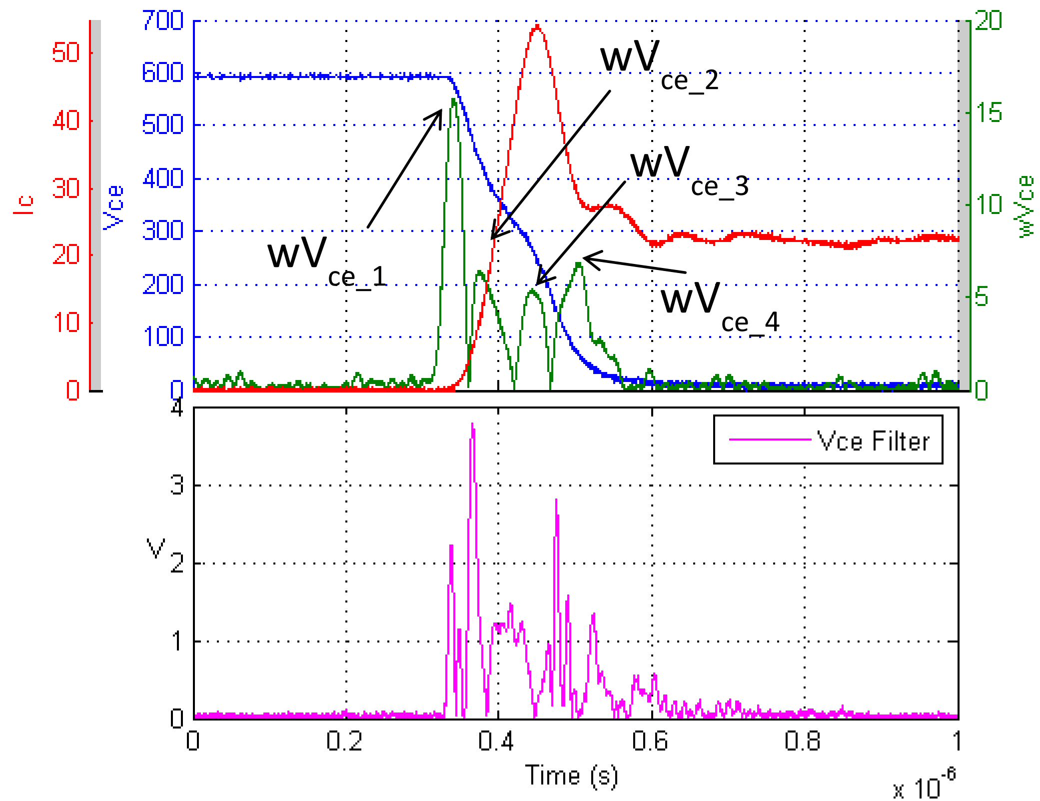


Figure 4-8: Mexican Hat Wavelet Analysis (with pseudo frequency of 30 MHz) of V_{ce} and V_{ce} Filter

The impulse response for the passive filter is unknown however in comparison to the wavelet transform, it would appear to have a longer duration given the series of small peaks when the IGBT voltage has fallen to the saturation level. This gives some uncertainty in the time domain location. While the high pass filter gives more attenuation at low frequencies, it requires an additional channel in the oscilloscope limiting the choice of signals which can be measured.

4.4 Dc Bus Bar Configuration

The dc bus bar in a VSD is used to carry energy from the input rectifier to the dc link capacitors and onto the IGBT module where it is chopped by the IGBT switching action to give a variable frequency output. The impedance of this bus bar will influence the switching characteristic of the IGBT and needs to be carefully considered in the design. This section looks at several simplified equations to determine the impact of the bus bar impedance on the switching transient. While the bus bar may be a physically large

structure, it is only the impedance as observed from the IGBT module connections which will influence the switching process.

As described in section 2.2.3.1, before the IGBT switches on, the load current is entirely supported by the diode and the current path as shown in Figure 4-9a. As the current transfers to the IGBT, the current loop changes as shown in Figure 4-9b and Figure 4-9c during reverse recovery of the diode. When the device is fully on the current loop is shown in Figure 4-9d. The current transients versus time are shown in Figure 4-10 along with the voltage induced across the stray inductance. The stray inductance (L_{module}) in the IGBT module is shown as a lumped parameter in series with the IGBT emitter. When the current rises through the IGBT, any inductance in the bus bar (L_{σ}) is in series with the module inductance and referred to as (L_{stray}). The voltage drop shown is resultant from the combination of these inductances.

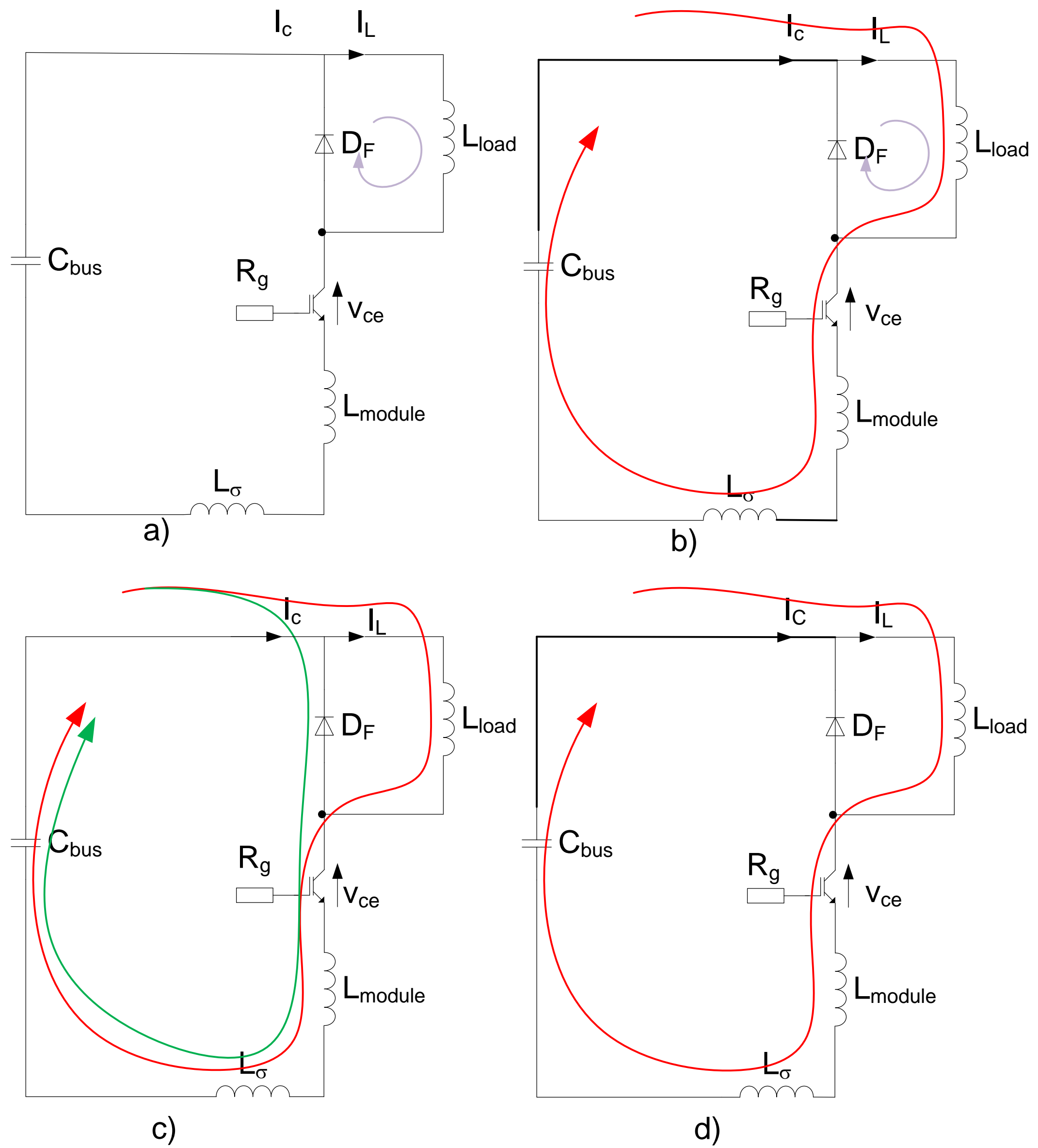


Figure 4-9: Illustration of transient current path at switch on

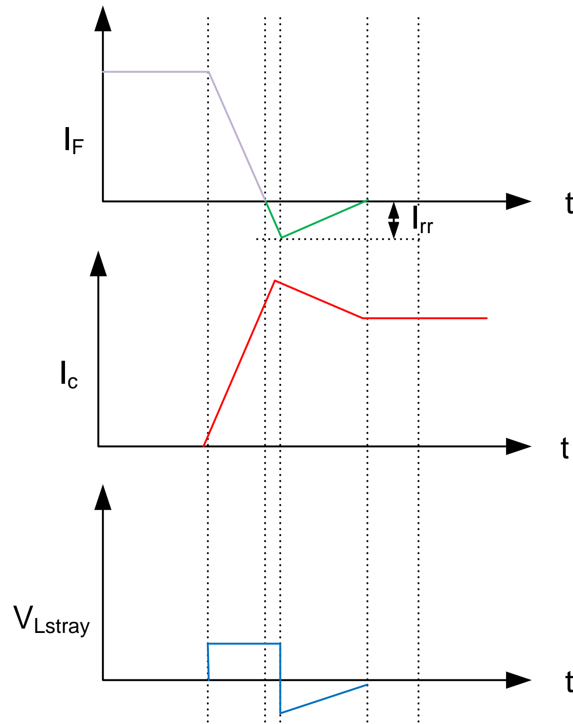


Figure 4-10: Illustration of transient currents and induced voltage

When the IGBT is not saturated, the rate of change in current is determined by the application of the gate voltage via the transconductance. If the bus bar impedance is inductive, then the change in bus bar current gives a voltage drop across the inductance. This voltage drop does not affect the current transient provided the V_{ce} is larger than $V_{ce\,(sat)}$ for the applied gate voltage at that instant. During this transition, the load inductance acts as a current source.

The power dissipated in the IGBT can be calculated from the product of the instantaneous voltage across the IGBT (V_{ce}) and the current through the IGBT (I_c) as discussed later. Increasing the bus bar stray inductance reduces V_{ce} during the switching transient reducing the power losses in the first region. There is minimal change to the diode reverse recovery process as the diode must block the full dc bus voltage at the end of the transient.

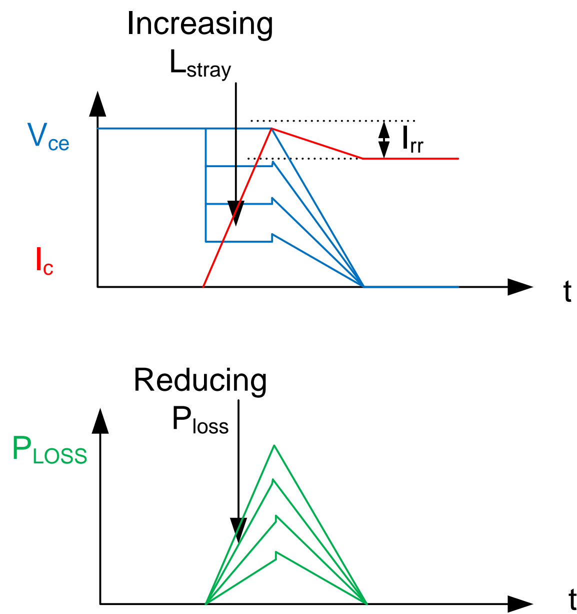


Figure 4-11: Effect of switch on power loss with bus bar inductance

The energy dissipated during turn on can be approximated by finding the area of the two triangular segments. During the rise of the collector current (t_{ri}), peak power loss is given by (4-1) and during the fall of the voltage by (4-2).

$$E_{tri}=\frac{1}{2}\times t_{ri}\times(I_L+I_{rr})\times\left(V_{DC}-L\frac{I_L}{t_{ri}}\right) \qquad (4\text{-}1)$$

$$E_{tfv}=\frac{1}{2}\times t_{fv}\times(I_L+I_{rr})\times\left(V_{DC}-L\frac{I_L}{t_{ri}}+L\frac{I_{rr}}{t_{fv}}\right) \qquad (4\text{-}2)$$

During switch off, the current transfers from the IGBT to the diode and the current flow is a little simpler as there are no reverse currents through the devices. This follows reverse sequence of Figure 4-9d, b then a. The transients are illustrated versus time in Figure 4-12 with the different power losses depending on the stray inductance in Figure 4-13.

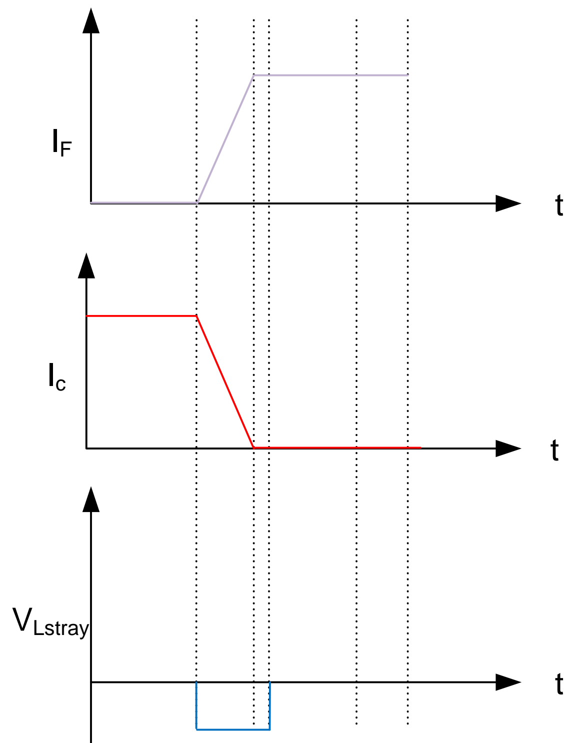


Figure 4-12: Current transient during switch off

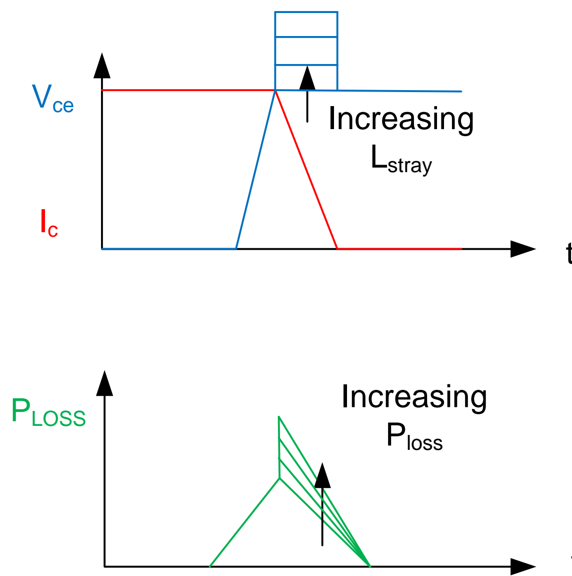


Figure 4-13: Change in switch off loss with increasing bus bar inductance

The power loss during the rise of the voltage is not affected by the stray inductance (4-3).It can be seen that the energy losses increase with the stray inductance for the same di/dt and can be described by equation expanded in (4-4).

$$E_{trv} = \frac{1}{2} \times t_{rv} \times I_L \times V_{DC} \quad (4\text{-}3)$$

$$E_{tfi} = \frac{1}{2} \times t_{fi} \times I_L \times \left(V_{DC} + L \frac{I_L}{t_{fi}} \right) \quad (4\text{-}4)$$

Combining equations (4-1), (4-2), (4-3) and (4-4) to give the total switching loss, (4-5), the energy loss dependant on the stray inductance (E_L) can be separated and is presented in (4-6).

$$E_{total} = \frac{1}{2} \times \left[L \left(I_{rr}^2 - \frac{t_{fv}}{t_{ri}} \left(I_L^2 + I_{rr} I_L \right) \right) + V_{DC} I_L \left(t_{fi} + t_{rv} + t_{fv} + t_{ri} \right) + V_{DC} I_{rr} \left(t_{fv} + t_{ri} \right) \right] \quad (4\text{-}5)$$

$$E_L = \frac{1}{2} \times L \left(I_{rr}^2 - \frac{t_{fv}}{t_{ri}} \left(I_L^2 + I_{rr} I_L \right) \right) \quad (4\text{-}6)$$

From (4-6), it can be seen that the contribution to the total loss due to the stray inductance can be either positive or negative depending on the current levels and switching times. The voltage fall time (t_{fv}) is usually larger than the current rise time (t_{ri}) and apart from very low load currents, I_{rr} is smaller than I_L. The combination of these factors leads to a reduction in total switching loss with an increase in stray inductance particularly at high currents. Table 4-1 illustrates a case with fixed transient times for a range of load currents and two inductance values using equation (4-6). With these transient parameters, increasing the inductance by an order of 10 gives a corresponding reduction in switching loss.

Table 4-1: Example of Loss Reduction due to Bus Bar Inductance

	t_{ri} (ns)	50		t_{ri} (ns)	50
	t_{fv} (ns)	100		t_{fv} (ns)	100
	I_{rr} (A)	5		I_{rr} (A)	5
	L (nH)	5		L (nH)	50
I_L (A)	E_L (uJ)	V_{ce} drop		E_L (uJ)	V_{ce} drop
1	0.0325	0.1		0.325	1
2	-0.0075	0.2		-0.075	2
3	-0.0575	0.3		-0.575	3
4	-0.1175	0.4		-1.175	4
5	-0.1875	0.5		-1.875	5
10	-0.6875	1		-6.875	10
20	-2.4375	2		-24.375	20
30	-5.1875	3		-51.875	30
40	-8.9375	4		-89.375	40
50	-13.6875	5		-136.875	50
100	-52.4375	10		-524.375	100

At turn on, the limitation to the maximum inductance which can be used is determined by the induced voltage drop is equal to the dc bus voltage minus the IGBT saturation voltage. At this point, the turn on losses have been minimised. If we assume an equal rate of change of current at turn on and off, the same induced voltage is imposed onto the dc bus voltage at turn off which can stress the device. This is particularly important during short circuit where the load current can rise very rapidly. To take advantage of the reduction in loss requires careful transient control during switching off of the IGBT.

In the analysis above, it is assumed that the impedance of the bus bar is inductive. As the voltage overshoots during turn off are often a limiting factor of the switching speed, it is common practise to add additional capacitance close to the module to reduce the dynamic impedance. It has been found that this can alter the measured radiated emissions [107]. Considering the piecewise transient trajectory, the impact on the radiated emissions can be considered using the frequency analysis presented in chapter 2. At turn on, the beginning and end of the voltage drop due to the stray inductance is related to dI_c^2/dt^2. Therefore an increase in the inductance would also increase radio

frequency content in the voltage transient unless improved current transient control is implemented.

At turn off, the dI_c/dt must be reduced if the inductance is increased to maintain the IGBT within its SOA. As a result the voltage overshoot may occur for longer with the same amplitude. This would smooth the switching transient reducing the radio frequency content.

4.5 Switching Loss Measurements

IGBT switching loss must be determined by measurement from the final VSD system to ensure accurate results. This is due to both the influence on the losses of the dc bus bar impedance and the capacitance of the load cable. There is agreement among IGBT manufacturers on the procedure for calculating the switching energy from the measured voltage and current waveforms, however, the time span over which this measurement is taken varies. IR measure loss from the point where I_c has risen to 5% of the load current until V_{ce} falls to 5% of the dc voltage, Toshiba use 10% while others use 10% rise in I_c until V_{ce} has fallen to 2% [12, 78, 81]. A European standard has been published in 2007 [108] which specifies that the switch on energy should be measured from the instant when V_{ge} has risen to 10% of the gate supply voltage to the instant when the gate collector voltage has fallen to 2% of the of the dc bus voltage. Energy is defined as the area under the power curve obtained from the product of the voltage and current transients, the beginning of the energy of the loss measurement is insignificant as losses due to leakage currents are insignificant. However it is important to have a clearly defined boundary between the switching loss and conduction loss.

Transient waveforms captured on the oscilloscope often contain many oscillations due to cable capacitance and inductance which occur at the point of switching. To determine a nominal current level for each test, a straight line is plotted on the current waveform with a gradient to match the current rise due to the load inductor. This is extended towards the point where the current first rose during turn on as illustrated in Figure 4-14.

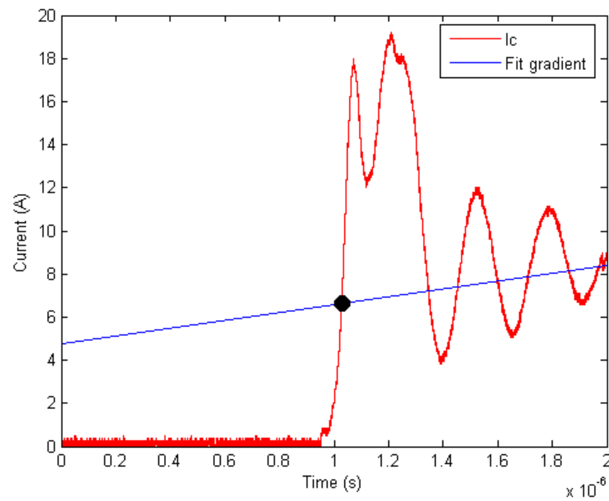


Figure 4-14: Illustration of Ic at switch on

The switch off energy span similarly has multiple definitions in the literature where the IEC60747-9 definition begins as V_{ge} to has fallen to 90% of the turn on applied V_{ge} until I_c has fallen to 2% of the device rated value [IEC60747]. It is important to capture the energy loss as V_{ge} begins to fall as this will correspond to a small but significant increase in the V_{ce} saturation voltage. All the energy measurements given in the standard assume a simple gate resistor is used to control the switching transients. This is not the case for AGD and hence throughout this work, switching energy has been calculated from the point when a change in switching power can be detected due to switching as illustrated in Figure 4-15.

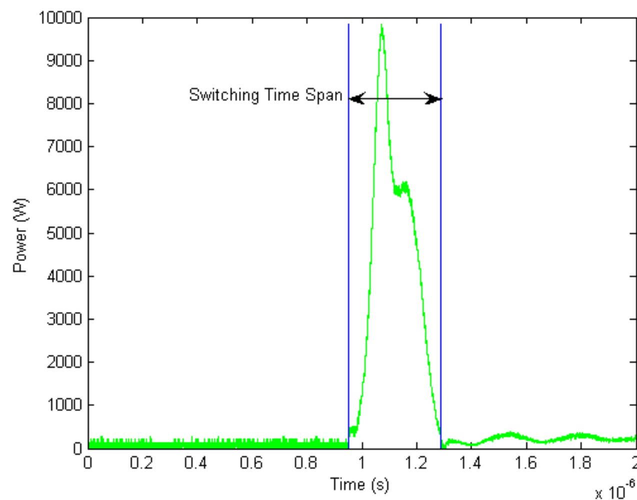


Figure 4-15: Power loss calculation for a switch on event.

4.5.1 IGBT Parasitic Elements

The importance of the IGBT internal gate capacitances have been described in section 2.2.3 in relation to the switching performance. Figure 4-16 shows how the gate capacitance of an Infineon™ FP25R12KT4 IGBT changes with the applied gate emitter voltage when the collector terminal is floating. This is measured using an LCR bridge where an applied 75 mV, 10 kHz signal is superimposed on a dc bias. When V_{ge} is below -1 V, the oxide capacitance can be measured to 6 nF. As the voltage increases from -1 V to +6 V, a depletion layer forms and expands. This shows a similar effect to increasing the gap between a parallel plate capacitor hence reducing the capacitance [44]. At 7 V, the capacitance increases significantly due to the formation of the inversion layer. It should be noted that the threshold voltage changes significantly (up to 2.5 V) over the rated temperature range.

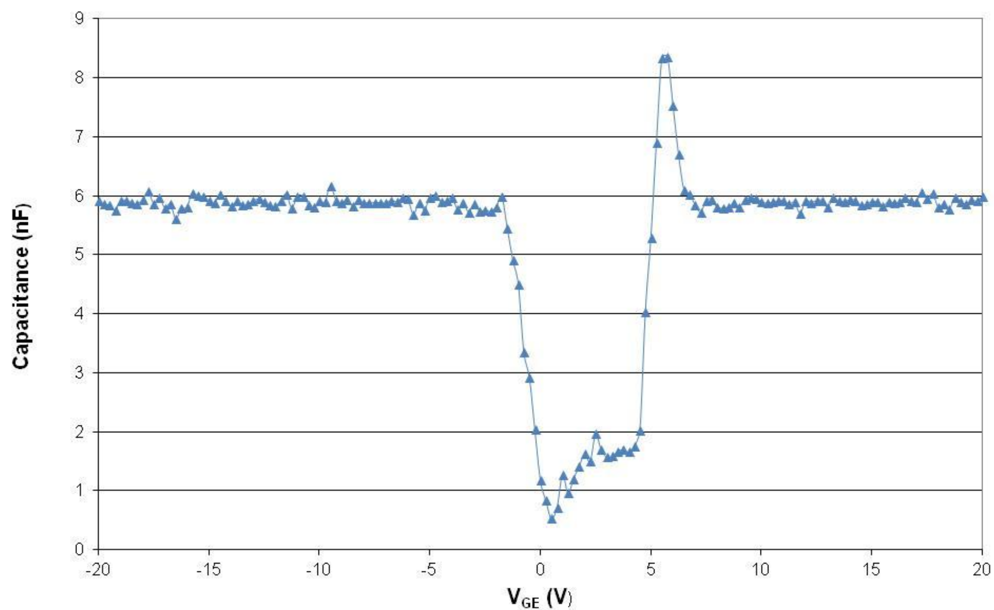


Figure 4-16: IGBT gate capacitance versus gate voltage

Due to fluctuations in the mains voltage, the voltage level on the dc bus can change during operation of the VSD. As several of the internal capacitances within the IGBT are voltage dependent, the applied dc bus voltage can influence the gate trajectory as illustrated in Figure 4-17. A step input voltage is applied via a large (33 Ω) gate resistance to bring the gate voltage up to the threshold voltage. The capacitance is seen

to reduce with the applied collector emitter voltage due to the depletion layer allowing the gate voltage to increase rapidly. This change in capacitance is due to the parasitic capacitance between the n-base and the gate which provides more charge to the gate at high collector emitter voltages [45]. This important characteristic adjusts the charge needed to bring the IGBT up to the threshold voltage and will have a significant impact on the gate drive requirements.

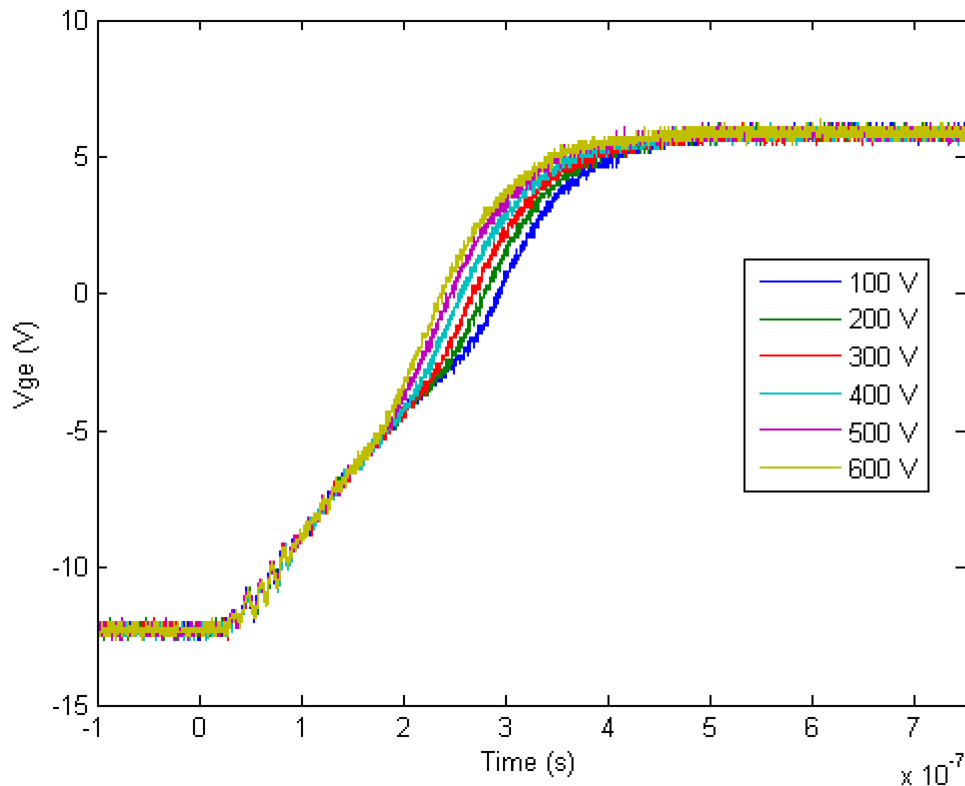


Figure 4-17: Change in V_{ge} with V_{ce}

4.5.2 IGBT transconductance

Section 2.2.3 discussed how the transconductance based on the physical geometry of the IGBT can be used to relate the unsaturated load current to the gate emitter voltage. To investigate the accuracy of this, a step input voltage is applied to the gate terminal via a 33 Ω resistor. The collector currents are measured for different bus voltages at turn on and are presented in Figure 4-18. Using equation (2-14) and the measured V_{ge}, the collector current is reconstructed from the square of V_{ge} above the threshold and then

multiplying by a K factor. This process gives reasonable results however, the required K factor changes depending on V_{ce}.

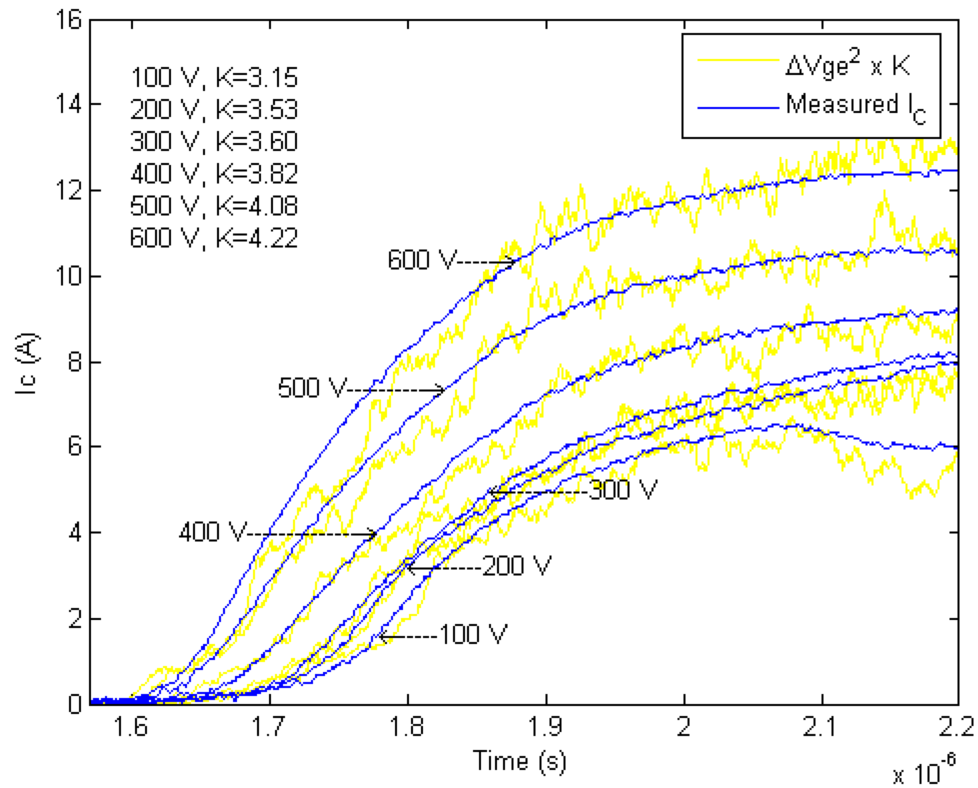


Figure 4-18: Change in transconductance in practice

The pnp transistor gain (α_{pnp}) is dependent on the collector emitter voltage due to the change in width of the depletion layer within the IGBT. The transistor gain increases (non-linearly) with collector voltage up to the reach through voltage for the Punch Through IGBT (point where the electric field reaches the n^+ buffer).

4.5.3 Intrinsic Time Delay in an IGBT

With slow transients, the collector current can be related to the gate voltage (quasi-static condition), however there is an intrinsic delay between a change in the input gate voltage before a corresponding change in the output conditions can be detected. Figure 4-19 illustrates the delay between features in the gate signal and corresponding features in the collector current. The threshold voltage (6.8 V) is subtracted from the measured V_{ge} voltage, the result squared and multiplied by K (4.22). Oscillations in the gate

voltage are also seen in the collector current where the delay (when compensated for probe delays) is approximately 25 ns. The delay results from the time taken for the inversion layer to expand due to the velocity of the carriers.

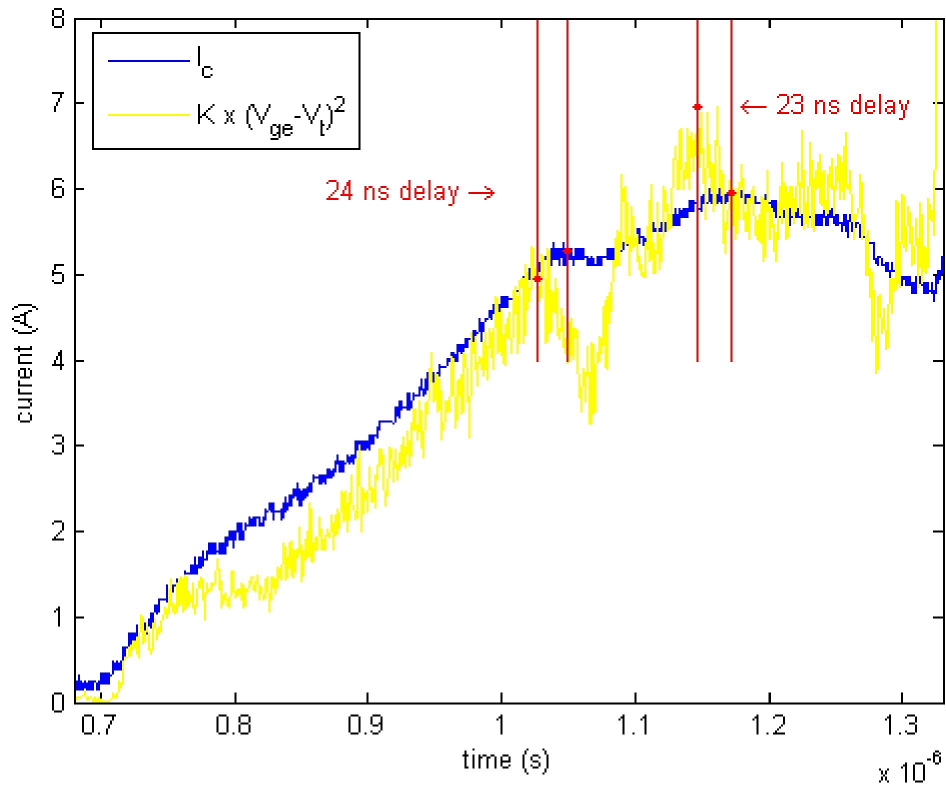


Figure 4-19: Intrinsic IGBT Loop Delay for Collector Current

When the IGBT voltage begins to fall, the dV/dt is related to the gate current. Where the gate voltage is held constant by the Miller effect, the gate current can be controlled by the voltage applied across the gate resistor. In Figure 4-20 there is a small increase in gate current as V_{ce} begins to fall. After 252 ns, the applied gate voltage is increased, increasing the gate current and causing a corresponding increase in dV/dt. In this section, a delay of approximately 10 ns is measured. In both cases, these time delays are too long to implement a closed loop feedback controller as part of the gate drive to reduce the radiated emissions. This delay results from the time taken to charge the parasitic capacitances in both the IGBT and diode and expand the diode depletion layer.

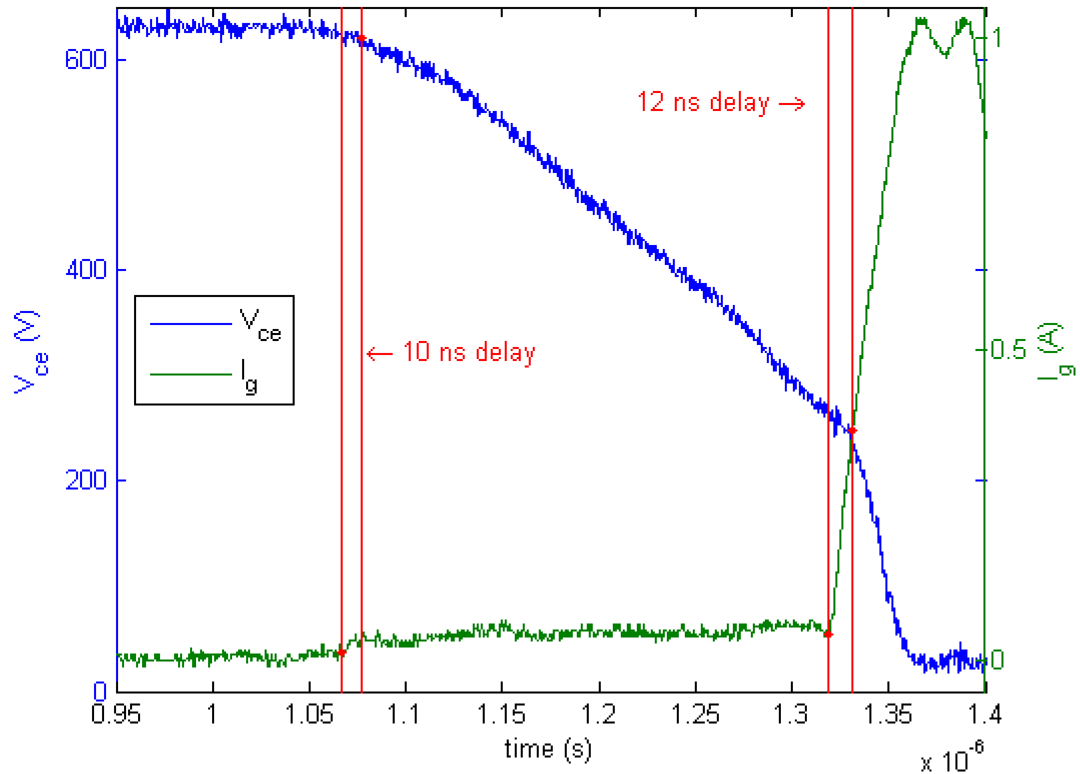


Figure 4-20: Intrinsic IGBT Loop Delay for Collector Emitter Voltage

While the measurements presented above display the delay between input and output response of the IGBT, it is important to observe the control of the switching transients by the gate signals. The current transient can be controlled by the gate voltage via the transconductance of the IGBT while the voltage transient can be controlled by the gate current.

4.5.4 Minimum Gate Resistance

The area of the gate current loop depends on the layout of the track and any connecting wires to the IGBT terminals. As a result, this loop will contain a significant inductance which can resonate with the IGBT capacitance. To minimise the gate oscillations, a minimum value of gate resistance is used. This is determined by measuring the impedance of the loop over a range of frequencies to determine a value for the lumped capacitance and inductance (biased above the threshold voltage). Assuming a second order system, a resistor value can be chosen to give critical damping giving improved control over the gate currents and voltage (see Appendix B for calculations).

4.6 Radiated Emissions Measurements

4.6.1 Open Area Test Site

The standard for radiated emissions to which Control Techniques™ products comply is IEC61800-3 [6]. This specifies electric field strength limits which depend on the customer installation environment, power rating of the VSD and the frequency of the emissions (Table 4-2). The Control Techniques VSDs are sold to customers with a class C2 environment however there are commercial benefits to expand the markets if the domestic limits can be met cost effectively.

Table 4-2: Radiated Emission Limits at 10 m.

<table>
<tr><th>Frequency (MHz)</th><th>C1* (class B)

Quasi-Peak dB(µV/m)</th><th>C2** (class A)

Quasi-Peak dB (µV/m)</th><th>C3***

Quasi-Peak dB (µV/m)</th></tr>
<tr><td>30-230</td><td>30</td><td>40</td><td>50</td></tr>
<tr><td>230 - 1000</td><td>37</td><td>47</td><td>60</td></tr>
<tr><td colspan="4">*C1: Domestic Environment, $V_{rated} < 1000$ V, (class B refers to CISPR nomenclature)

**C2: Any other environment $V_{rated} < 1000$V, professional installation required (class A refers to CISPR nomenclature)

***C3 Any other environment $V_{rated} > 1000$V, or $I_{rated} > 400$A, professional installation required.</td></tr>
</table>

The layout of the apparatus is described in IEC55022 and consists of a large conductive ground plane with an antenna located above the ground plane and directed towards the EUT at a distance of 3 m (see Figure 4-21) [109]. The equipment under test is placed on a table 1 m above the ground plane inside a non conductive shelter (no conductive parts including screws which could reflect the RF signals). The antenna cable is located under the ground plane and is connected to a receiver in the control shelter (with

windows as shown in the photograph) which, under software control, scans through the frequency range of interest and records the measured field strength.

Figure 4-21: Photograph of the OATS used

The shape of the ground plane can have an effect on the measured radiated emissions due to interference patterns from edge reflections [110]. For physically large EUTs, the proximity to the edge of the ground plane can change even though the distance to the antenna remains constant. This can make comparisons between measurements of an EUT taken at different test sites difficult and requires the inclusion of uncertainty measurements. By using a programmable gate drive, to evaluate different switching patterns for radiated emissions, the physical structure can remain static allowing accurate comparisons between different test patterns to assess potential sources or emissions.

Table 4-2 gives the field strength limits when measured at 10 m, however it is allowable to introduce a 10 dB correction factor across the frequency range for measurements at 3 m using the inverse distance fall off theory which assumes a simple hemispherical field pattern. Measurements at 3 m give a better signal to noise ratio. Studies by Mass and Kang have shown this parameter assumes a small radiating source with the antenna in the far field [111, 112]. Towards the lower frequencies, there is uncertainty that the antenna is in the far field at 3 m. In a VSD, the radiating structures are potentially large due to the long cable length, different types of source antenna and their orientation have been shown to affect measurements due to the proximity to the ground plane. Again, as

comparative measurements are taken this will work for the same physical setup, the attenuation across frequencies will remain constant for all tests.

The specification for the receiver is given in CISPR16-1-1 and includes a bandwidth of 120 kHz at -6 dB (see Figure 4-22 for acceptable pass band), a charge time of 1 ms and a discharge time of 550 ms for the quasi peak time constants [113]. The charge and discharge times have been determined from subjective annoyance levels by a listener of AM radio and are used to give a weighting to repetitive signal strength.

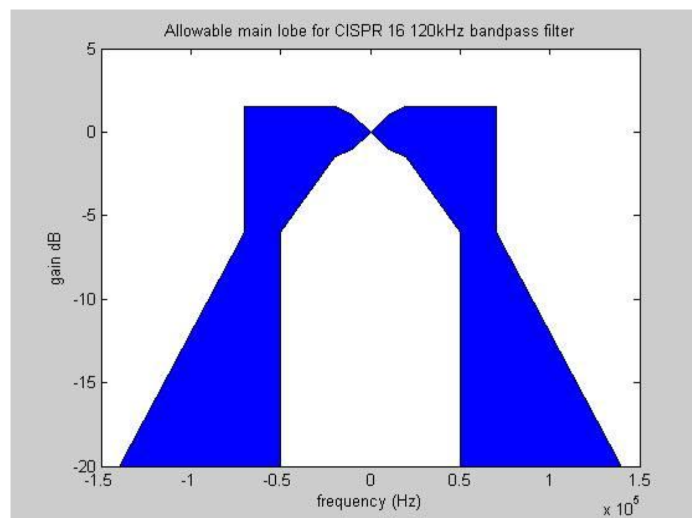


Figure 4-22: CISPR16 pass band

In a VSD, with a minimum switching frequency of 1 kHz, the transient duration is of the order of hundreds of nanoseconds hence a single pulse is unlikely to give large emissions with the charging time constant in the quasi peak detector. However, the discharge time encompasses many switching transients so the overall measured result is close to but a little lower than the peak. The effect of space vector modulation, and sinusoidal output current are captured by the quasi peak detector over the measurement time (at least 100 ms per measurement frequency to ensure that a steady state has been reached in the detector). A sweep of the frequency range of interest can take up to 15 minutes to complete.

The 120 kHz bandwidth has a correspondingly long envelope in the time domain (in the order of 30 μs). Any pulsed signals which occur within this period are averaged to determine the peak emissions. The period increases continuously in time only recording

either the peak or quasi peak value in the receiver. Using a similar filter on the electrical signals may give an indication of the frequency content however it is not possible to locate the features of the transient signals responsible for emissions at the centre frequency.

4.6.2 Gate Resistor Values

To illustrate the frequency range of interest, a simplified pulse test rig (described in section 5.3) is used with a CGD, where a step voltage is applied to the gate of the IGBT via the gate resistor. IGBT manufacturers often state a recommended gate resistor for this purpose, however the impedance of this test circuit (either gate loop or power loop) is not stated. The three different gate resistance values used for a comparison of radiated emissions in the following illustration are:

1) the minimum value used in a commercial product which complies with radiated emissions limits when used in a VSD (43.7 Ω);
2) the manufacturers recommended data sheet resistance, (20 Ω);
3) the minimum resistance calculated from measurements to give critical damping (5.6 Ω) as discussed in Appendix B.

The pulse test setup is operating with a steady state load current to evaluate the transient performance for the switching waveforms. The measured radiated emissions for the three different gate resistors for step demand (both turn on and off) are shown in Figure 4-23. Given the differences in the physical layout between a commercial VSD and the pulse test circuit, a direct comparison of radiated emission levels cannot be made, however the relative measurements from one test can be useful for an indication of the performance benefits of the gate drive. It can be seen in Figure 4-23 that the emissions are highest with the smallest gate resistor and lowest with the largest gate resistor.

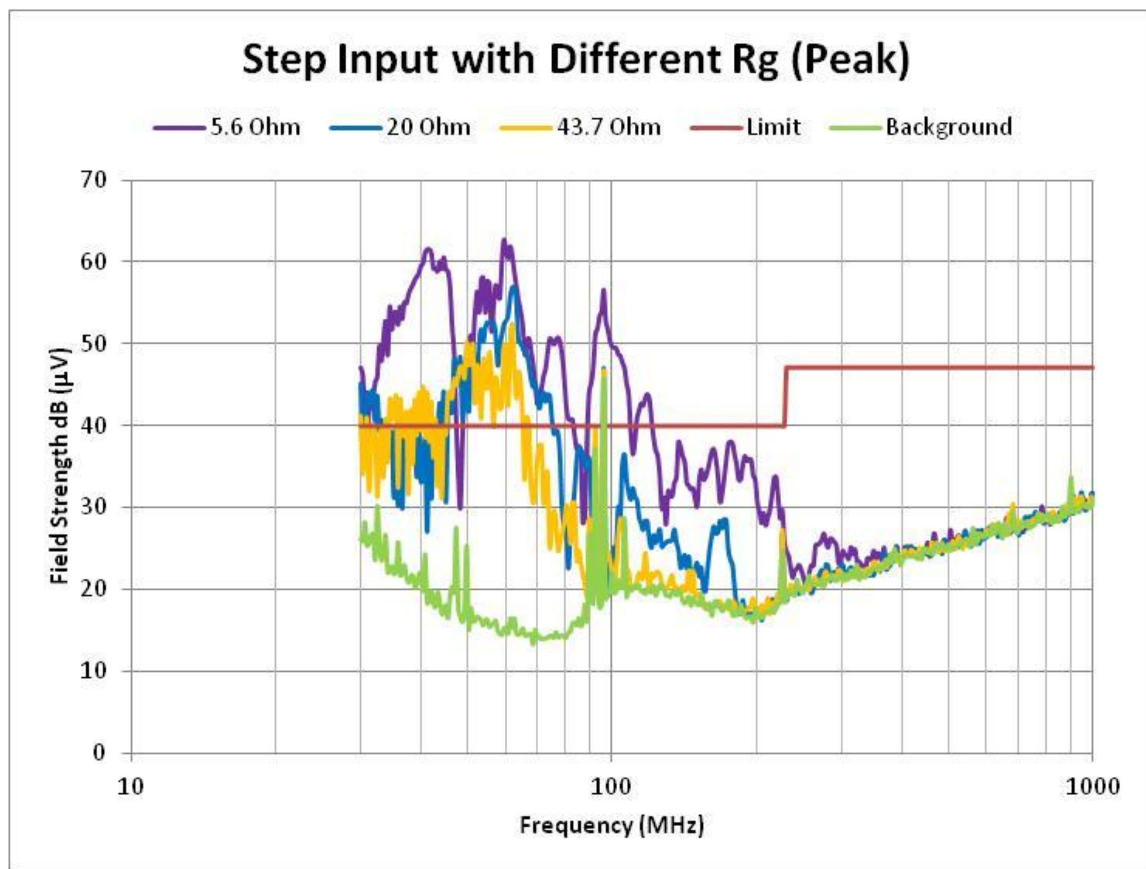


Figure 4-23: Measured Radiated Emissions from step input.

From observing the frequency spectrum, it is clear that the broadband emissions from the IGBT can only be detected above the background measurements up to a maximum of 400 MHz in this case (for a commercial drive, emissions typically only measurable up to 100 MHz). The emissions can be seen to decay with frequency at approximately 40 dB / decade as is the case with a trapezoidal waveform in the time domain. From previous experience, the radiated emissions resulting from the turn off transient are lower in magnitude than at turn on. It can be seen over the frequency range 30-33 MHz that the largest resistor has the lowest emissions, however, between 33-42 MHz the emissions from the 43.7 Ω resistor are higher than 20 Ω resistor. A method is required which looks at all the emissions across a wide frequency range to determine a figure of merit for a comparative analysis. This is presented in section 5.5.1.

4.7 Summary of Chapter 4

The testing carried out and presented in this chapter has highlighted several important features of IGBT switching. As a starting point, one important design consideration is

the bus bar inductance. The stray inductance in the bus bar as seen by the IGBT module will significantly reduce the switch on losses by adjusting the switching trajectories. The resulting voltage overshoot at turn off must be controlled particularly during short circuit conditions to prevent damage to the device. As the inductance influences the "corners" or second derivative of the switching transients, this will have an impact on radiated emissions. Analysis of the influence will be discussed in chapter 5.

The semiconductor theory presented in chapter 2 presents equations describing the operation of the IGBT, however measurement presented in this chapter demonstrate how the IGBT transient performance is dependent on many variables such as dc bus voltage, current, temperature and from internal feedback loops within the IGBT which can cause the switching mechanism to become unstable at high switching speeds. Control over both I_c and V_{ce} transients is demonstrated at low speeds using V_{ge} and I_g however, the intrinsic feedback delay due to parasitics within the device will not allow control, utilising feedback, over the fine details associated with the radio frequency content.

A high pass filter is required to give a good resolution on the radio frequency components associated with radiated emissions when measured using a standard laboratory oscilloscope. This is particularly important when operating at high dc bus voltages where the noise floor due to the vertical resolution restricts the highest frequencies which can be observed.

Chapter 5: Determination of Key Linkages of Radiated Emissions to Measured Voltages and Currents

5.1 Introduction

The control of the IGBT switching trajectory utilising both the gate drive voltage, gate current and the bus bar inductance has been presented in earlier chapters. Analysis methods to identify the location in the time domain of radio frequency content within a voltage or current signal have been discussed in section 2.4.3, however, the RF source signals and radiating structure in a VSD responsible for radiated emissions have not been identified.

This chapter presents measurements of radiated emissions taken from a simplified setup which represent a VSD system. Individual features in the voltage and current waveforms are adjusted using a custom, high frequency gate drive generator to assess their linkages to the measured radiated emissions.

As discussed in section 4.4, the mechanical construction of the product and the electrical layout can influence the measured radiated emissions. It has been shown that the gate emitter voltage can be used to control the collector emitter voltage and collector current transients which in turn adjust the RF content. However, the linkage between the RF content in the electrical signals and the measured radiated emissions are unknown hence it is not possible to define a suitable limit for compliance to the standards. In an effort to gain this knowledge, separate control of current and voltage transient features is required, so the designed waveform (constructed in section 5.2) is therefore modified to control the maximum voltage peak (hence, RF content) independently from the current peak. However, any change in the current profile, even in the saturated mode, will have an effect on the collector voltage profile due to stray inductance effects.

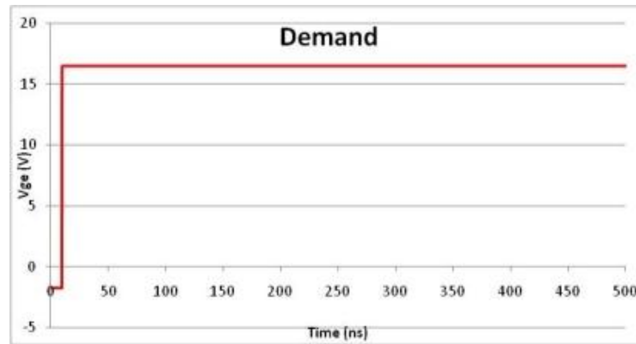
5.2 Control of Wavelet Magnitude to Influence Radiated Emissions

From measurements of radiated emissions from a VSD using a CGD fitted with different gate resistors, it is clear that a larger gate resistor, hence slower switching resulted in lower radiated emissions. Measurements of the wavelet peaks in both voltage and current waveforms also reduce with increasing gate resistance. To further analyze the linkage, a method to control the wavelet magnitudes while taking radiated emission measurements is required. The duration of the wavelet peaks is of the order of a few nanoseconds. It has been demonstrated in Chapter 4 that it is not possible to use closed loop feedback control to influence the gate signals over this time frame due to the intrinsic IGBT loop time delay. Instead, a custom gate drive generator utilising a high speed Field Programmable Gate Array (FPGA) programmed with the required gate voltage profile is used. The signals from the FPGA are converted using a digital to analogue converter (DAC) to produce a gate voltage with a 14 bit vertical resolution updated every 250 ps (4 GHz). The design of this gate drive circuit is shown in Appendix A.

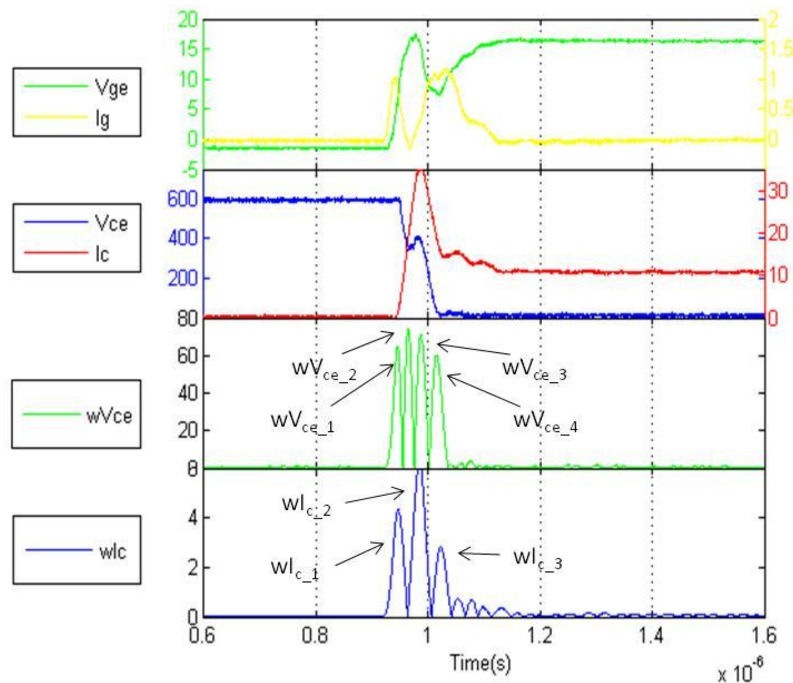
While control of the current and voltage transients with the gate drive can be separated into different phases as described earlier, the first three out of four locations where the voltage wavelet magnitudes reach their peak occur when the current is strongly coupled due to the stray and parasitic components. Under steady state operating conditions with a fixed dc bus voltage, temperature, and load current with constant ripple, a gate profile can be defined to minimise each wavelet magnitude in V_{ce} and I_c in turn. When a profile has been defined with minimal wavelet content, features can then be added which will increase the wavelet amplitude of the voltage and current independently.

As a starting point, using the FPGA gate drive, a step voltage input is applied to the gate resistor representing the action of a CGD (Figure 5-1a). A minimum resistance of 5.6 Ω is used to damp oscillations in the gate current loop circuit. A switch on load current of 10 A is used in each case and the associated switching transients are displayed in Figure 5-1b. A short cable connection to the inductor is used to reduce reflections giving clarity to the waveforms below, however a long cable is used for emissions

measurements. To describe the operation, reference is made to the theoretical switching profile presented in Figure 2-15. During switch on phase 1, (t_0 to t_1), the gate voltage (V_{ge}) rises rapidly from a negative potential, through the threshold at which point the collector current begins to rise. We can observe the first peak wavelet (wV_{ce_1}) in the voltage and current which occur simultaneously. The current wavelet peak (wI_{c_1}) is high as the current begins to increase rapidly and the voltage peak corresponds to the change in V_{ce} due to the stray inductance. As the collector current trajectory reaches its maximum rate of change, a second peak wV_{ce_2} occurs. The gate emitter voltage reaches its peak value as the collector current reaches its peak giving wI_{c_2}. At this time, the diode can begin to block voltage and hence V_{ce} begins to drop giving wV_{ce_3}. As the diode finishes its recovery process, wI_{c_3} peak can be observed. As V_{ce} reaches the saturation voltage, wV_{ce_4} occurs.



a.

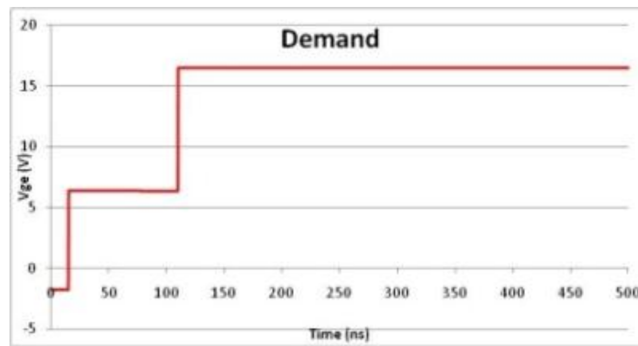


b.

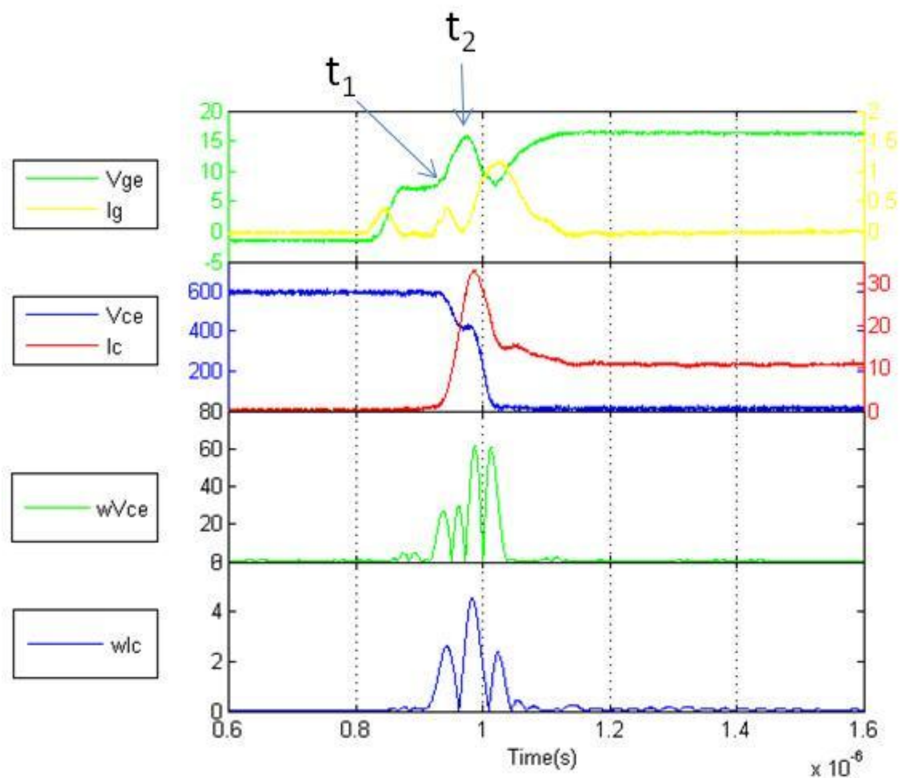
Figure 5-1: a) V_{ge} Demand; b) Voltage and current wavelet transform for step input.

As the collector current is related to V_{ge} via the transconductance, it follows that the rate of change of the V_{ge} during turn on dictates the rate of change of collector current. Using a CGD, the step voltage input causes the gate voltage to rise rapidly reaching its maximum rate of change as it crosses the threshold voltage. This instigates an equally rapid rise in the collector current immediately the threshold has been crossed. In an effort to gain control over the initial current rate of rise, the gate voltage is increased to

just below the threshold voltage and held for 85 ns to ensure the gate current has returned to zero separating switch on phase 1 and 2 (see Figure 5-2). V_{ge} is then increased with a step demand up to the maximum supply rail. However, due to the gate loop inductance, the gate current hence gate terminal voltage, cannot rise instantly. This reduces the rate of increase in collector current from previously observed. It is clear to see that this simple change in wave shape has the positive effect of reducing both wV_{ce_1}, wV_{ce_2} and wI_{c_1}. This shows that it is the third derivative of the current (d^3i/dt^3) at this point is responsible for wV_{ce_1} and wV_{ce_2}.



a.



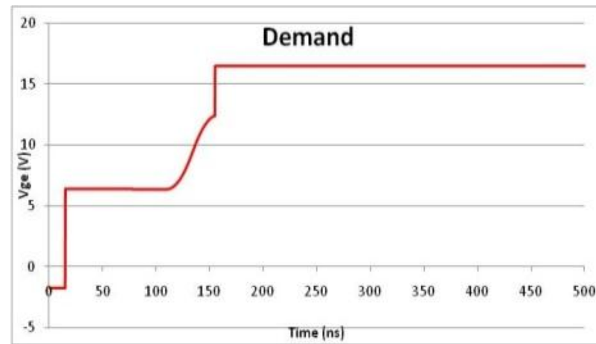
b.

Figure 5-2: a) V_{ge} Demand; b) Voltage and current wavelet transform, held at V_t for 85ns.

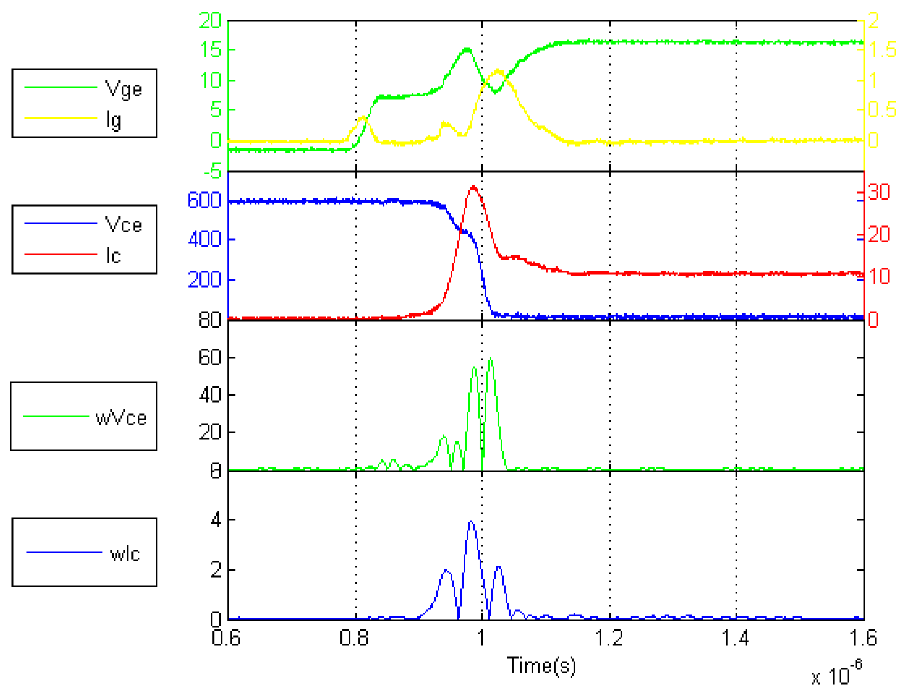
For phase 2, (t_1 to t_2), when the gate voltage rises above the threshold, the load current transfers from the diode to the IGBT. The rate at which this happens is related to the transconductance of the IGBT as has been demonstrated previously. It is difficult to use the transconductance equations to accurately predict the behaviour of the load current

from V_{ge} over the entire time for the current to rise due to the feedback voltage from the drop across the stray inductance and the carrier transit time in the IGBT when switching at high speeds. To further reduce wI_{c_1}, V_{ge} demand is shaped to slow down the rate of current rise as illustrated in Figure 5-3. The gate demand profile, derived using trial and error methods, is based on an s-ramp where the timing is adjusted until the wI_{c_1} and wI_{c_2} are seen to decay. This has the added benefit of further reducing wV_{ce_1} and wV_{ce_2}.

The rate of increase in the load current is controlled giving a gradual rise until it reaches a maximum value. While the current rises slowly, the voltage drop across the parasitic inductance is still visible, but reduced. When the load current is at its maximum rate of increase, V_{ce} levels out creating a plateau in the wave shape.



a.



b.

Figure 5-3: a) V_{ge} Demand; b) Voltage and current wavelet transform, controlled slope of V_{ge} to influence I_c.

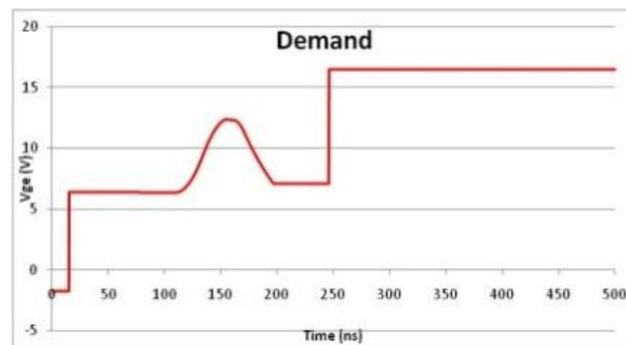
When using a conventional gate drive, the diode reverse recovery current carried by the IGBT increases to its peak value then decays to the load current. When the diode stored charge (Q_{rs}) has been swept out, the depletion layer begins to form as the diode depletion charge (Q_{rf}) is then removed. This results in the falling of V_{ce} as charge is swept out by the expanding depletion layer. The depletion layer can be thought of as a parallel plate capacitor whose capacitance reduces as the depletion layer grows. This

capacitance is discharged by the reverse recovery current while at the same time, the gate current charges the increasing capacitance (C_{gc}) within the IGBT. The rate of change in voltage is limited by the slowest of these mechanisms hence at low load currents, dV/dt is restricted by the diode while at higher current V_{ce} is restricted by the gate current. At the peak of the reverse recovery current, the depletion capacitance is discharged at the fastest possible rate causing the V_{ce} to fall very quickly as the diode begins to support the voltage. This change in voltage is the source of the third peak voltage wavelet (wV_{ce_3}).

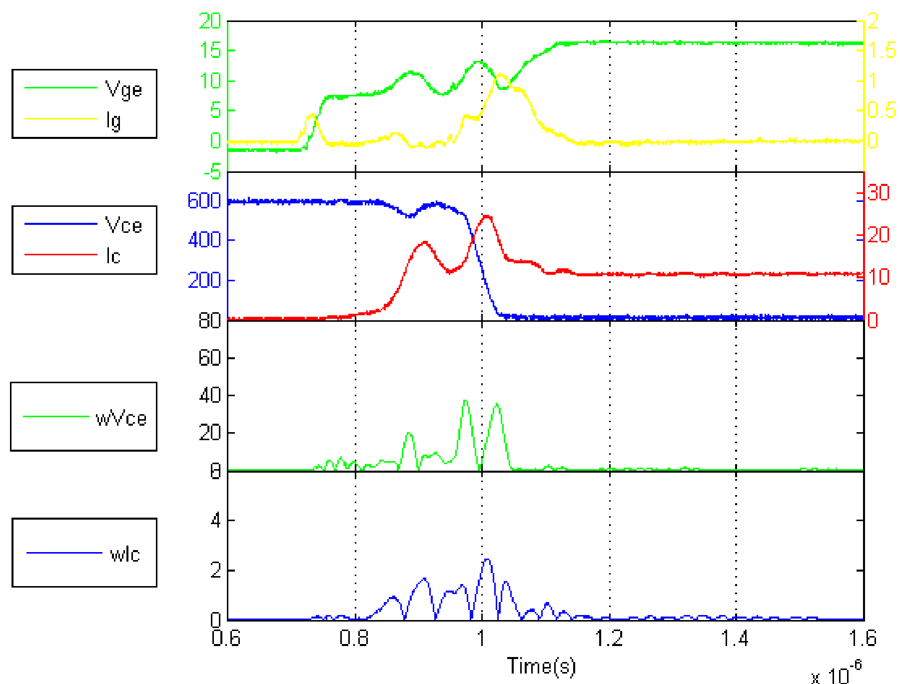
In an effort to gain control over the rate of change in the depletion layer, the gate voltage is used to split the stored charge (Q_{rs}) and the depletion charge (Q_{rf}) into two separate regions as shown in Figure 5-4. As the IGBT collector current is controlled by V_{ge}, the collector current is reduced to match the load current at the point where all the diode stored charge is removed. At this point, the depletion layer could not expand as there is no current flow through the diode and the entire bus voltage is dropped across the IGBT. The IGBT is momentarily held at the limit of IGBT saturation equivalent to the load current. At this point where Q_{rs} has been removed, V_{ce} does not drop but recovers to the dc bus voltage as there is no change in current to induce voltage drops in the stray inductance. After a short pause where the gate current falls to zero, the remaining step demand is applied to the gate allowing completion of the switch on transient.

This control method gives an unusual looking current transient with two peaks (see Figure 5-4). The first collector current peak is associated with wavelet peak, wI_{c_2}, and is significantly reduced. As the voltage does not fall after the first wavelet current peak, wV_{ce_2} has been further reduced. The remaining voltage wavelet peaks wV_{ce_3} and wV_{ce_4}, have been delayed in time until the voltage begins to fall as Q_{rf} is discharged. Additional peaks have appeared in the current wavelet transform which correspond to the second current pulse as the demand is stepped up to the maximum V_{ge}. It can be seen that the gate voltage does not follow the demand signal precisely. The IGBT's internal positive feedback causes a region of instability. As C_{gc} discharges with the falling collector voltage, the capacitance increases as the depletion width reduces. This

is a nonlinear process which begins by adding additional charge to the C_{ge} causing the V_{ge} to increase followed by a period of extracting charge from C_{ge} reducing V_{ge}. Precise control of the transient shapes through this region using the feed forward of the gate voltage is very difficult.



a.



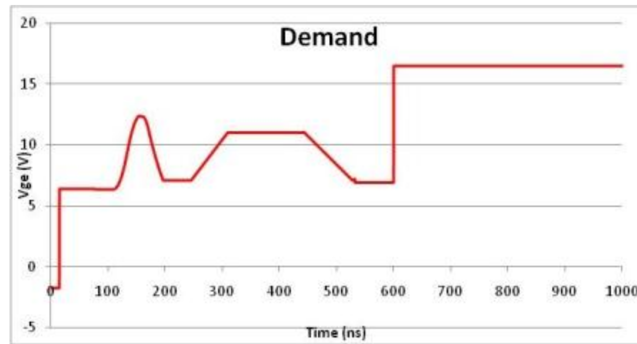
b.

Figure 5-4: a) V_{ge} Demand; b) Voltage and current wavelet transform, controlled slope of V_{ge} to remove Q_{rs}.

Towards the limit of saturation, a small increase in V_{ge} moves the IGBT into the active region where the load current is related to gate voltage, allowing an increase in the

collector current which in turn allows the diode depletion region to expand. The reduction in V_{ce} causes C_{gc} to discharge taking current from the gate terminal or from C_{ge}. The gate current is determined by the voltage drop across the gate resistor however the voltage at the gate terminal does not change much during the Miller region hence the current flow can be controlled by the voltage applied to the gate resistor.

A gate emitter voltage waveform is further adjusted causing V_{ce} to begin to decrease at a rate which reduced wV_{ce_3} as can be seen in Figure 5-5. V_{ge} is ramped up slowly to ensure the second derivative of V_{ce} remains low, reducing the wavelet peak. The actual voltage transient depends on the doping concentrations in the diode intrinsic region. PT diodes may show a sharp change in dV/dt as the depletion region reaches the buffer layer depending on the voltage level. As the voltage falls and approaches the on voltage, $V_{ce(sat)}$, the fourth wavelet voltage peak (wV_{ce_4}) occurs. The V_{ge} demand voltage is reduced just before this point to reduce the gate current hence limiting wV_{ce_4}. After this point, the diode tail current sweeps out the remaining charge with little change in voltage. The third current peak in the wavelet magnitude occurred at the same time as wV_{ce_4}. With the smooth transition of the diode tail current, wI_{c_3} is also reduced.



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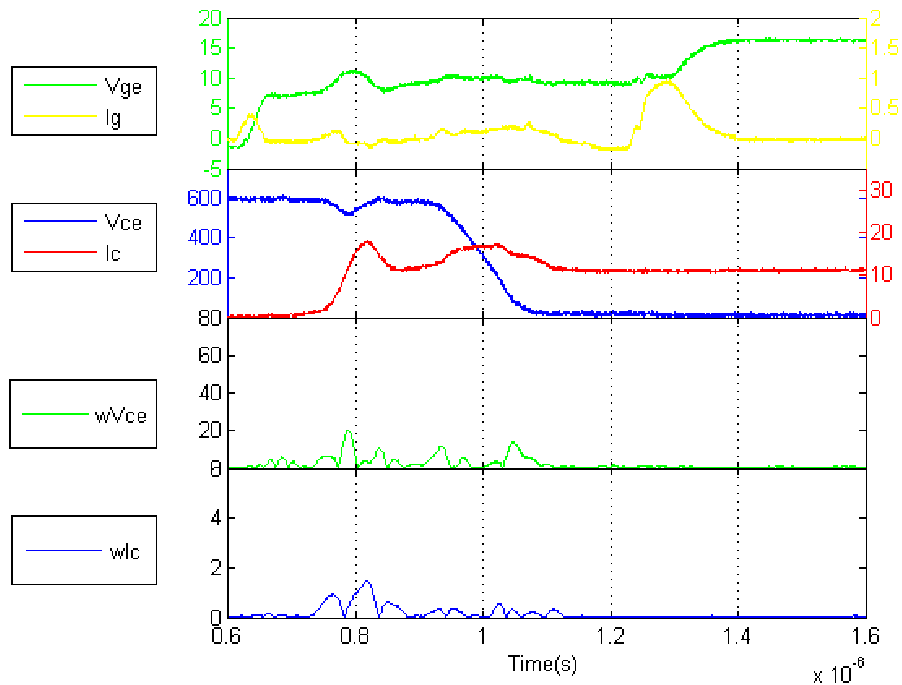


b.

Figure 5-5: a)V_{ge} Demand; b) Voltage and current wavelet transform, controlled slope of V_{ge} to remove Q_{rf}.

5.2.1 Switching Loss

One of the problems with the constructed V_{ge} waveform is an increase in switching time. The conventional gate drive fitted with the 43.7 Ω resistor has been taken as a benchmark for comparison of switching loss as this represents what is currently possible in a commercial product. The switching loss using the minimum gate resistor value has been reduced to approximately half of that used in the commercial product, however as discussed, this condition fails the radiated emissions test. Each stage of the reduction of

the wavelet magnitudes described above has resulted in an increase in switching energy (see Table 5-1).

Table 5-1: Switch on Loss

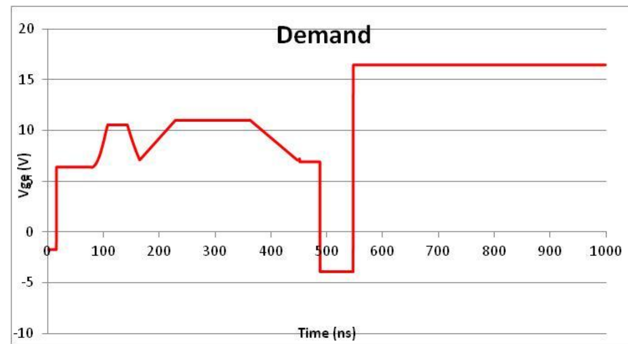
Test conditions	E_{on} (mJ)
R_g = 43.7 Ω, step input	1.300
R_g = 5.6 Ω, step input (Figure 5-1)	0.7368
Threshold hold (Figure 5-2)	0.8152
I_c control (Figure 5-3)	0.8632
Separate diode charge (Figure 5-4)	1.4338
Low wavelet switching (Figure 5-5)	2.1064

5.2.2 Isolated Peak Voltage Wavelet

The gate profile shown in Figure 5-5 has achieved a reduction in all the wavelet peaks throughout the switch on process. To assess the contribution to radiated emissions from either the voltage or current wavelets, the peak wavelets are reintroduced at a point in the switching transient where they could be controlled independently.

To induce a voltage disturbance, the gate signal is pulled low for a short period at the end of the Miller region then returned to the gate supply voltage (see Figure 5-6). This initiates the IGBT turn off procedure causing the collector emitter voltage to rise however, the voltage falls when the gate voltage is restored without disturbing the collector current. The magnitude of this voltage spike is controlled by the duration and depth to which the V_{ge} demand signal is reduced. The waveforms captured in Figure 5-6 shows a significant ripple in the collector current. This can be attributed to the capacitance of the long cable added to the test setup representing the motor cable. Sample waveforms for different demand signals and their corresponding radiated

emission measurement are shown in Appendix D. The load current continued to flow through the IGBT and did not transfer to the diode hence there is no change in the current wavelet.



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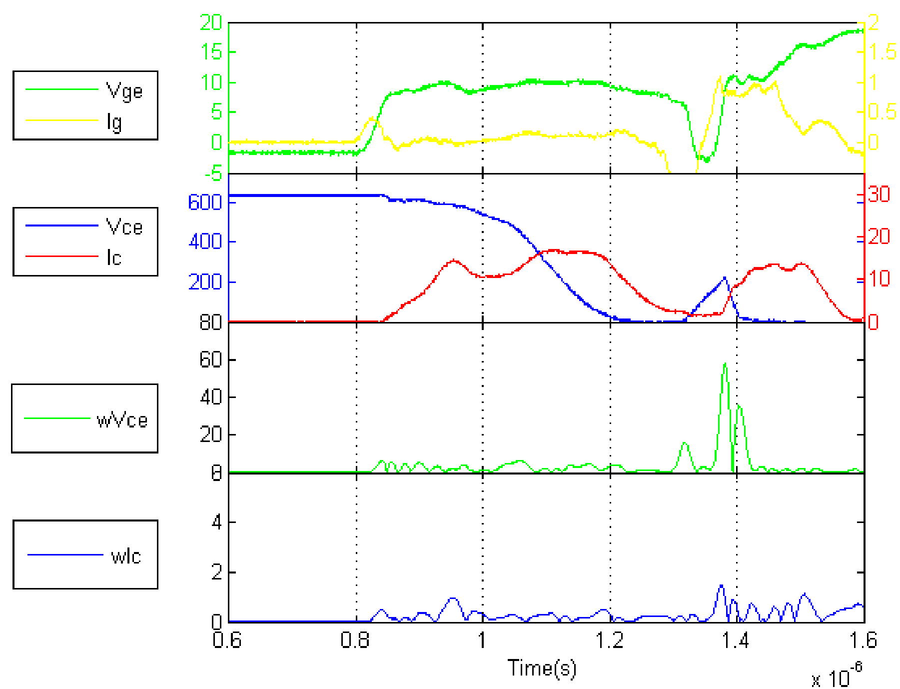
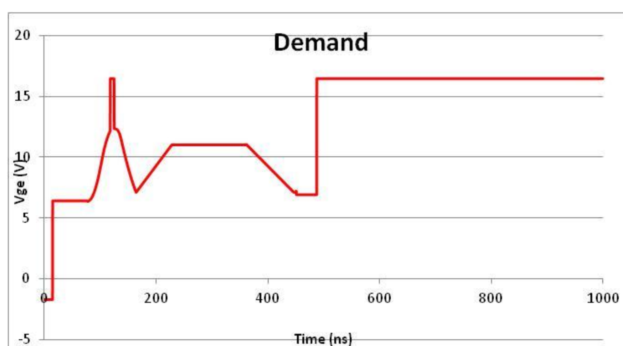


b.

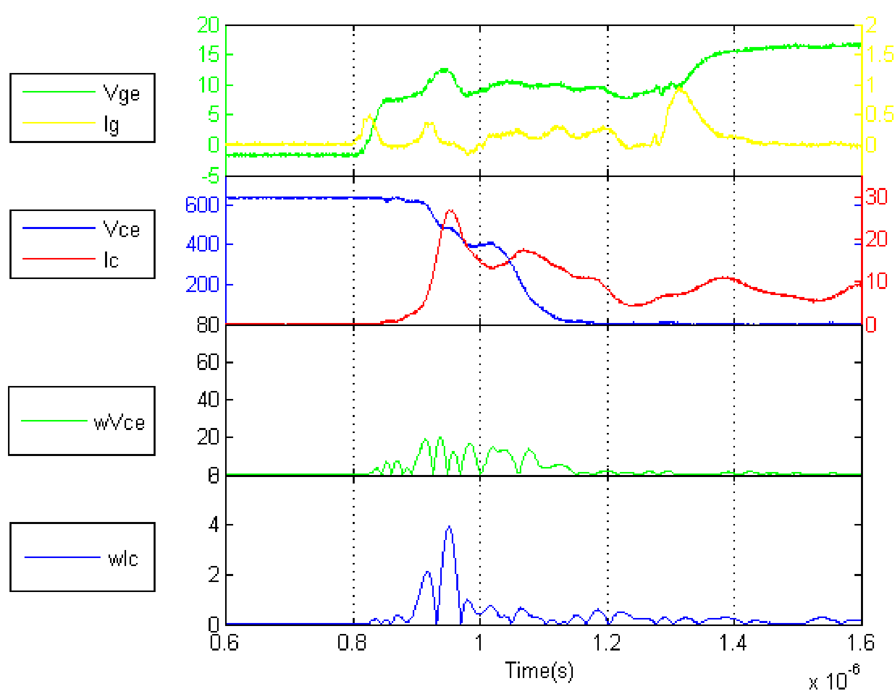
Figure 5-6: Illustration of wV_{ce} control

5.2.3 Isolated Peak Current Wavelet

A similar method is used to isolate the peak current wavelet by introducing a step in the gate signal as the diode stored charge is removed. This disturbance also causes a small change in the voltage wavelet due to linkage by the stray inductance.



a.



b.

Figure 5-7: Illustration of wI_c control

5.2.4 Switch Off Transient

When switching the IGBT, it is necessary to evaluate the switch off transient for radio frequency content. Control of the switch off transient via the gate drive signal is complex. As discussed in chapter 2, the IGBT must first be brought into the active region by reducing the gate voltage. However, when the collector emitter voltage has risen to the dc bus level, the collector current begins to reduce. The rate of change in current is related to the rate of change in gate voltage however, the gate voltage may already be pulled below the threshold at the gate terminal of the IGBT. To gain control, the gate signal would have to be increased to the limit of saturation at the point when V_{ce} has risen to the dc bus level then reduced in a controlled manner during saturation as described in [84].

To ensure the switch off transient has minimal influence on the radiated emissions, it is possible to mimic the operation of a large gate resistor using a profile programmed into the FPGA (see Figure 5-8). The turn off transients times have been increased with a slow linear ramp from positive to negative gate supply voltage. This increases the switching losses, however this is not important for this evaluation.

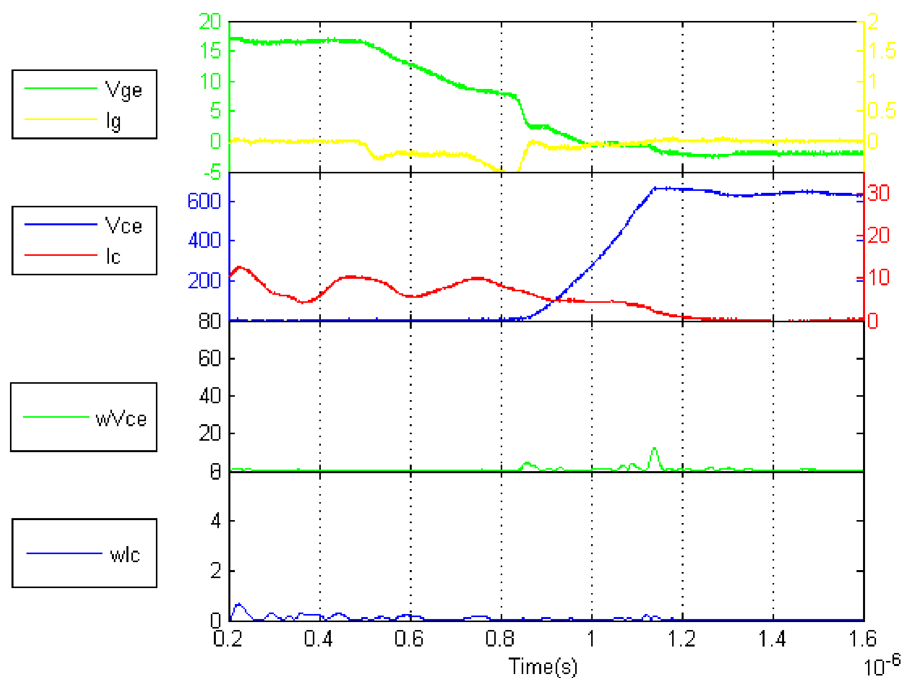


Figure 5-8: wV_{ce} and wI_c for switch off

5.3 Radiated Emissions Apparatus

Radio frequency emissions radiate from the physical components in a VSD system. The physical system is very complex as discussed in chapter 2 where the paths taken by the radio frequency currents are undefined. This section examines the measuring apparatus setup, the VSD setup and simplifies the test system to gain an understanding of the influence of an IGBT transient on radiated emissions.

5.3.1 Typical VSD Test Arrangement

The schematic for a typical VSD radiated emissions test is shown in Figure 5-9 where the mains supply to the VSD is filtered by an external EMI filter. The EMI filter is a custom design for the VSD to comply with conducted emissions limits defined in relevant standards [2, 3] and is installed during the testing as this is known to influence the radiated emissions by influencing current paths through stray capacitances.

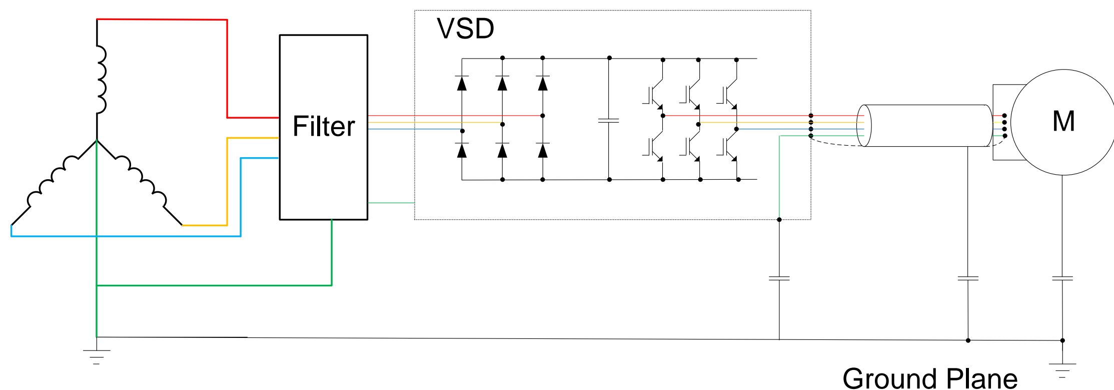


Figure 5-9: Typical setup schematic for testing VSD for radiated emissions on an OATS

To replicate a worst case typical customer installation, while complying with all the safety requirements and advice in the instruction manual, the filter and VSD are installed in an electrical cabinet on a metal ground reference plane. The cabinet and motor are isolated from the OATS ground plane using a wooden pallet. The safety earth conductors are attached to the filter, the VSD and motor in a daisy chain and the cable shields are connected at both ends of the motor cable as described in the VSD user manual.

The VSD power is supplied through this filter and rectified to give the dc bus voltage. The power for the control circuits is derived from the dc bus via a flyback converter. A speed demand signal is applied which causes the unloaded motor to rotate during testing. This is achieved by chopping the dc bus voltage across the inductance of the motor windings to create a current of the required frequency.

The approximately sinusoidal output current, presents different load current to the switching transient of the IGBT on each switching cycle. Depending on the load drawn by the motor, ripple voltages on the dc are also presented to the IGBT influencing the transient voltage. While the VSD can operate in steady state, the switching transients for all six IGBTs vary continuously. Radiated emissions measurements from this setup are useful to determine a pass or fail related to the defined limits but the source of the emissions cannot be determined.

5.3.2 Simplified Test Setup

To isolate the sources of the emissions, from the IGBT module, a single device is switched using the equipment previously used for pulse testing (Figure 4.3). A lower IGBT is switched on allowing the current to flow through an inductor and a 5 m cable which represents a typical motor cable. At 30 MHz, a wavelength of an EM wave in air is 10 m, and the half wavelength cable is an efficient antenna at the frequencies of interest. Two power conductors are shorted at the far end of the cable with the shield and the third phase conductor connected to the earth conductor. At the other end of the shield, the third power conductor and safety earth are connected to the metal frame of the test equipment which is connected to the earth of the power supply. All the test equipment is positioned on an 80 cm tall wooden table to isolate it from the OATS ground plane. The schematic for this setup is shown in Figure 5-10.

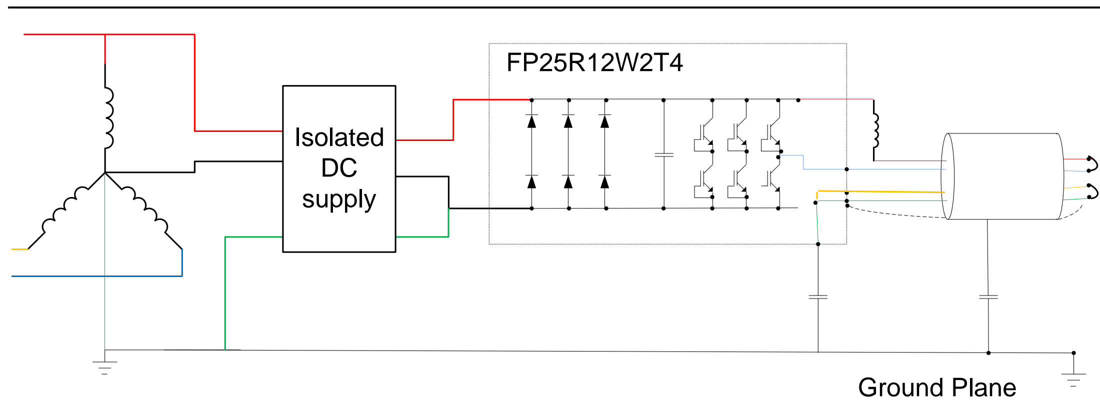


Figure 5-10: Setup of pulse testing equipment for radiated emissions on an OATS

The gate demand voltage for the switching IGBT is controlled using the high bandwidth DAC where the duty cycle and gate profile are defined in the FPGA firmware. A fixed frequency, fixed duty cycle signal is used to control the load current through the inductor. The on pulse is of a short duration (2 µs) allowing the current to ramp up to a peak level and the off time (364 µs) allows the current to decay in the inductor and freewheeling diode due to losses. With this setup, the load current at the point of switch on is consistent for each switching cycle giving a repeatable transient. Similarly, the switch off transient occurs at the same current level on each cycle (see Figure 5-11).

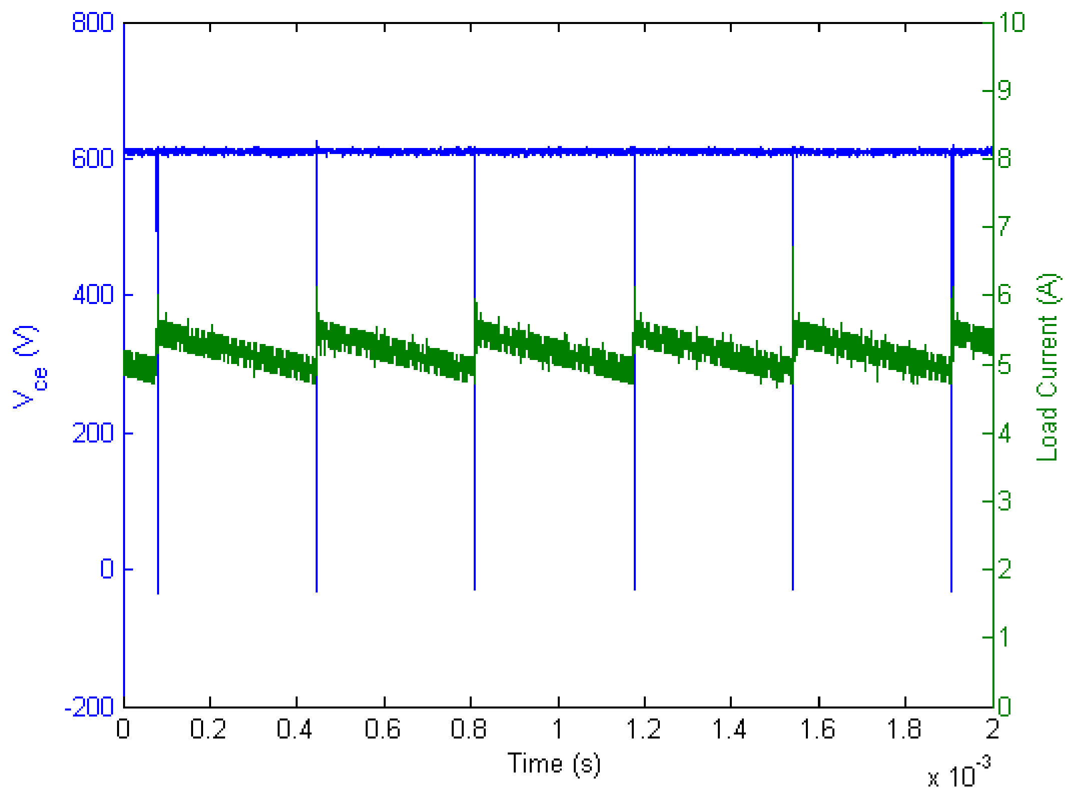


Figure 5-11: Continuous pulse train with fixed duty cycle to determine load current.

A photograph of the equipment located in the test shelter is shown in Figure 5-12a and the antenna position relative to the test shelter can be seen in Figure 5-12b. The metal mesh ground plane is continuous under the test shelter and antenna. The distance from the antenna to the closest edge of the equipment is 3 m. All power supplies are positioned close together with the cables held firmly in place.

a b

Figure 5-12: a) Pulse test setup for radiated emissions, b) OATS.

The 600 V power supply which is used to energise the dc bus, uses a variable transformer to give the required output voltage which is then rectified to dc. The two 24 V power supplies for the safety interlock and the FPGA board utilise switch mode power supplies and have a measurable frequency signature. A frequency scan taken with all power supplies and oscilloscope (DPO7304) operating but without the IGBT switching shows a small increase in emissions (see Figure 5-13). The change in load drawn from these power supplies will only have a minimal influence when the IGBT is switching hence the EMI signature does not alter. Large spikes are visible in the measurement close to 100 MHz and at 250 MHz. These are due to the broadcast radio stations which are weak at the measurement location in rural Wales. Background measurements taken in a city contain significantly higher levels of noise and intentional transmitters.

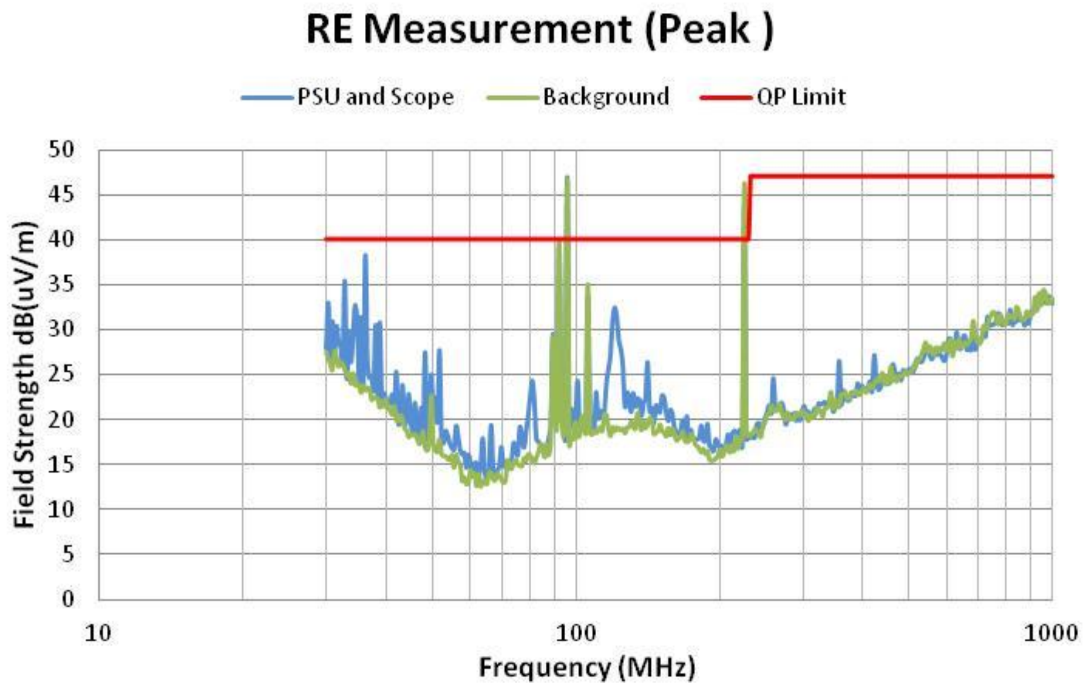


Figure 5-13: Radiated Emissions from power supply units without the IGBT switching.

5.4 Variables Influencing Radiated Emissions Measurements

5.4.1 Signal Interference

With a complex and unintentional transmitter such as a VSD system, there are many possible transmission sources as discussed in section 2.3. It is possible that these sources will interact with each other depending on the type, orientation and distance from the source. Figure 5-14 illustrates possible interference mechanisms. Currents circulating within loops in the VSD such as those created by the dc bus capacitors, bus bar and IGBT module give rise to magnetic fields. Other current loops such as those created by the gate current buffer and IGBT gate emitter capacitance can also create magnetic fields. Depending on the relative orientation of these fields, it is possible to observe reinforcement or cancellation due to near field superposition.

Electric fields are created around the VSD with the change in voltage relative to a reference ground. Examples would be the voltage on the load cable connected to the collector of the IGBT and the gate terminal. Again, superposition will occur in the near field. As the transmitted signals move further from the VSD system and transition into

electromagnetic waves, fields arising from magnetic sources and fields arising from electric sources can combine according to the principle of superposition [114]. An antenna positioned in the far field is only capable of a spot measurement of the combined signal.

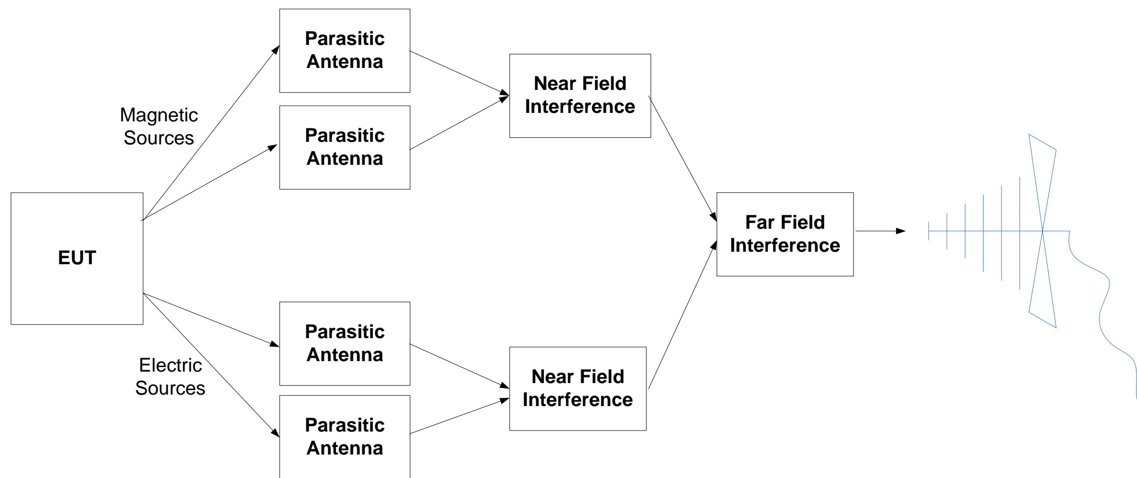


Figure 5-14: Signal path taken by radiated emission sources

While the antenna is a physically large object, it can be considered to measure the emissions at a single point on a sphere with a 3 m radius from the EUT. The conducting ground plane acts to reflect any signals with a negative elevation towards the antenna ensuring these are captured in the measurement. One phenomenon associated with the reflected signal is phase cancellation (far field superposition). If a continuous sinusoidal signal is transmitted from the EUT, the direct path from the EUT to the antenna is 3 m while the path of the reflected signal is longer and can be calculated by triangulation (see Appendix C for example calculations). The phase change due to the different transit times leads to interference from the reflected signal. This interference is consistent for tests with a continuous, fixed frequency, single emission source and fixed antenna height. However, the broadband noise from the IGBT switching transient is emitted in short bursts potentially from multiple sources. The time delay, and hence phase, of these bursts changes between gate voltage profiles. For a broadband emission source such as switching edges of an IGBT, it is unlikely that interference would occur due to its existence in time for a short period, however, the antenna would receive two distinct pulses where the relative delay is determined by the transit path which, due to

the averaging effect of the receiver bandwidth (as discussed in section 4.6), would have the effect of increasing the measured signal.

The antenna height is swept between 1 m and 4 m for a conformance measurement to allow for reflections by taking the highest value. As the antenna height is adjusted on the vertical mast, two uncertainties are introduced: (i) as the direct distance to the EUT increases with antenna height, this results in a reduction in the measured field strength; (ii), the antenna factors are not known from different angle of incidences other than the main lobe and hence this introduces further errors into the measurement [115].

With the use of the low RF content gate profile, potential emissions sources have been separated and controlled independently. Different profiles are implemented only in firmware hence no change to the physical radiating structure. In an effort to reduce the number of variables, all subsequent measurements are captured at an antenna height of one meter.

The use of time domain measurements are proposed in Krug [116] where an antenna is used to detect the EM field however the technique differs from the CISPR16-1-1 standard by using periodograms to analyse the signal in the time domain. This analysis shows many parallels to the method proposed in this thesis with regards to correlating a time domain measurement to the required frequency domain measurement. However, the proposed measurements in this thesis are of the voltage and current signals responsible for the EM fields before any interference due to the physical structure.

5.4.2 Azimuth

An ideal isotropic antenna radiates equally in all directions when positioned in free space. In practice real antennas will radiated more in one direction than any other and hence the azimuth pattern from the EUT must be considered. In an effort to identify the directivity of the parasitic antennas from the simplified test setup, measurements are taken for a step demand gate profile with a fixed resistor. The table supporting the apparatus is rotated 360° in 30° steps. Figure 5-15 illustrates the results at selected frequencies where an increase in emissions above background due to IGBT switching is observed (the radial axis is electric field strength in dB (μV/m)). From this diagram, it

is possible to see the peak directivity when the table is oriented at 90° and 270°. It is observed that as the EUT is not cylindrical, the shortest distance to the antenna changed with rotation about the table centre. When considering the physical structure and change in direct distance, it is determined that directivity of the EUT is negligible.

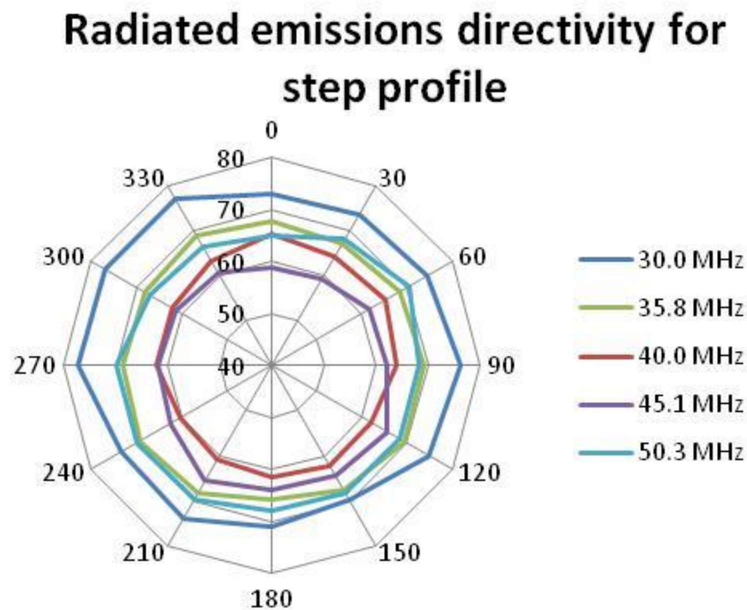


Figure 5-15: Azimuth pattern at select frequencies

While some degree of directivity is expected, there are several reasons why this has not been observed:

- The antenna used to measure the radio noise on the OATS is the Schaffner® CBL 6111C which has a half power beam width of 120° at 30 MHz which reduces with frequency to 80° at 1 GHz. The wide beam width illuminates the entire EUT structure and ensures that the majority of radiated signals are captured.
- The length of the cable attached to the test setup is 5 m long to give efficient radiation at 30 MHz however, the cable is held to the edges of the table where a portion is orientated in three normal directions. This positioning will cause it to radiate in all directions.

- The ground plane used on the OATS consists of several layers of wire mesh with the dimensions as described in the CISPR standards. This meshed surface as opposed to a plane surface may have the effect of scattering the reflected emissions in all directions.

As there appears to be little directivity from the EUT, all further measurements are taken at 0°.

5.4.3 Temperature

The measured emission spectrum is found to change with temperature as illustrated in Figure 5-16. The simplified VSD system is enabled and temperatures are allowed to reach steady state before the first measurement is taken early in the morning with a low ambient temperature. Further measurements are taken towards the afternoon as the ambient temperature rises. The IGBT case temperature is recorded using a thermocouple. The reason for the change in emissions is the change in the IGBT silicon characteristics with temperature such as reduction of threshold voltage. As the temperature increases from 33.5 °C to 38.4 °C, the peaks and troughs in the spectrum can be seen to shift towards the lower frequencies by 500 kHz as well as a change in magnitude. Over such a small temperature range, the physical properties of the parasitic antennas are not expected to change. While it is established that the temperature of the Si chip increases with each switch on pulse, the steady state operation of the pulse train removes any impact of this.

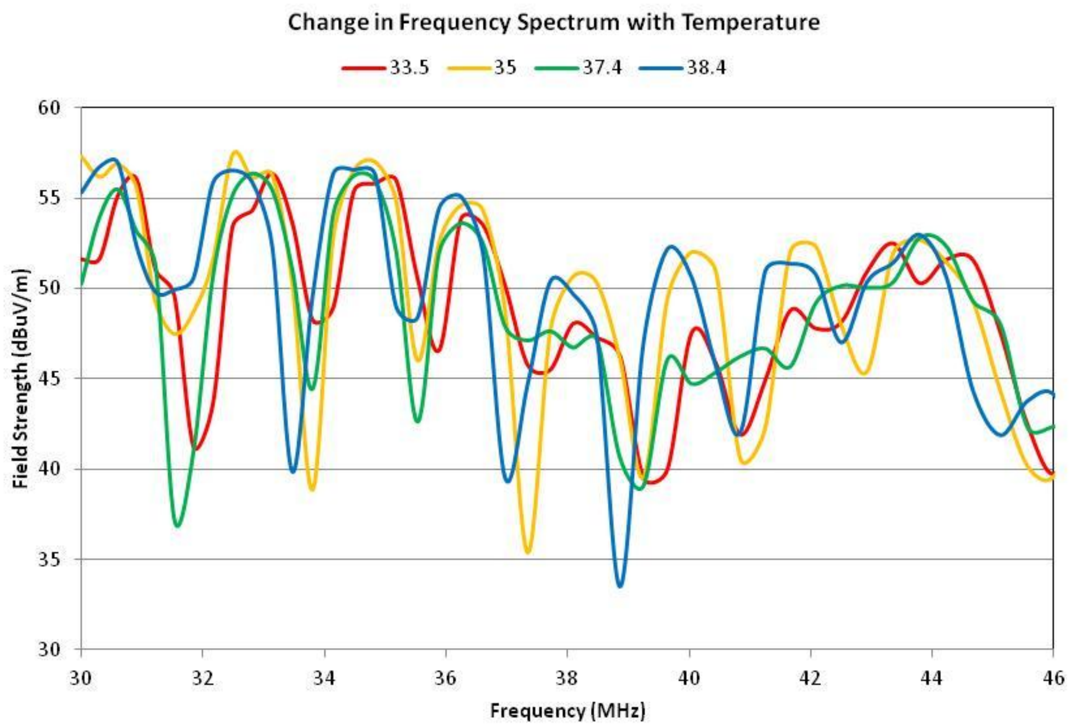


Figure 5-16 : Measured Radiated Emissions spectrum change with temperature

To view the frequency content, the V_{ce} and I_c transient signals are filtered in Matlab® using a band pass filter with a bandwidth of 120 kHz and adjusting the center frequency for each frequency of interest (see Figure 5-17 and Figure 5-18). Examination of the voltage waveforms also show spectrum changes with temperature however it has not been posible to correlate these to the peaks and troughs in the field strength as measured by the antenna. This is due to the radiation efficiency changing with frequency from the parasitic antennas.

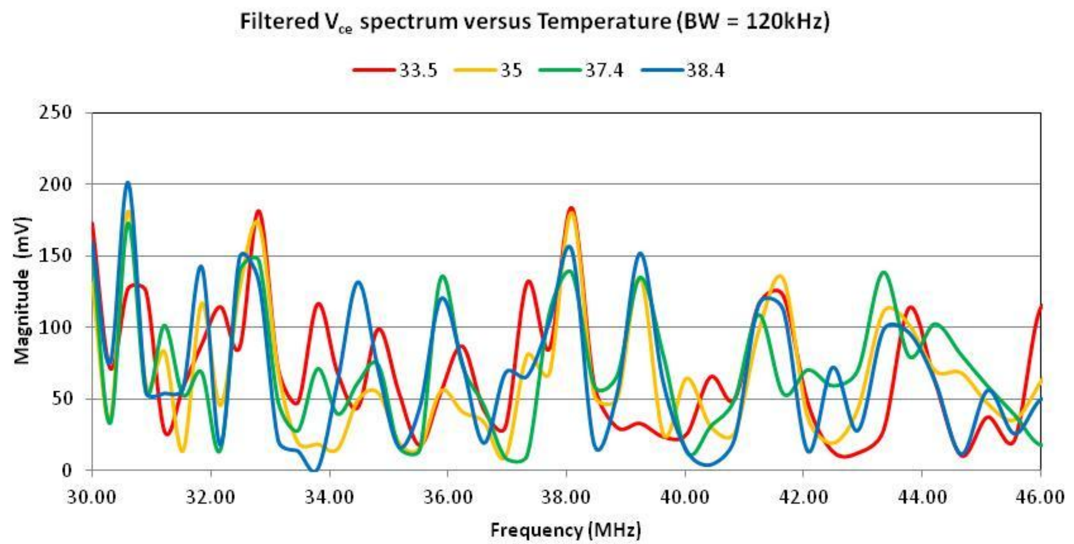


Figure 5-17: Frequency spectrum of V_{ce} change with temperature

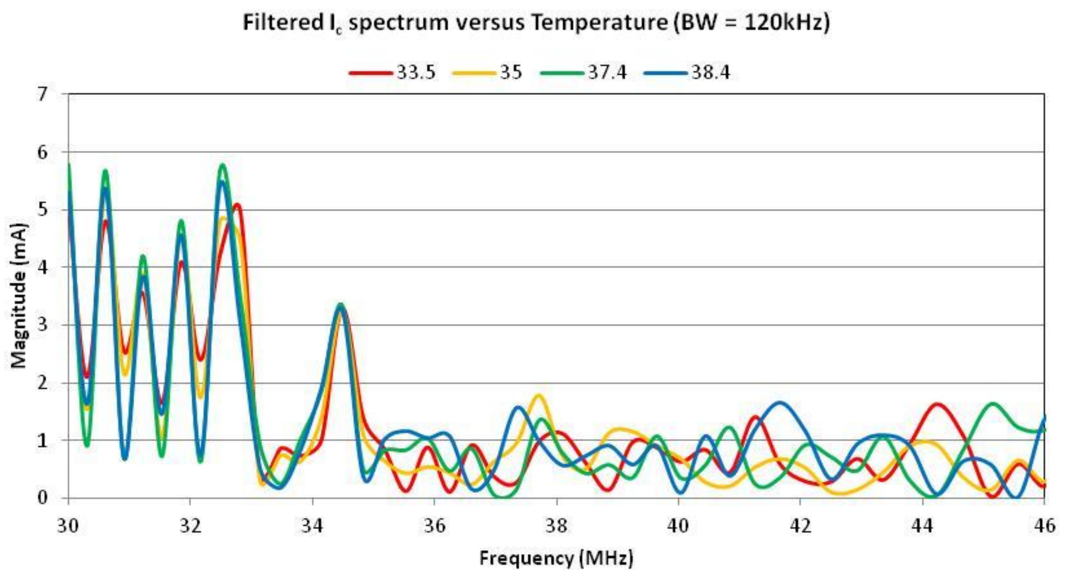


Figure 5-18: Frequency spectrum of I_c change with temperature

It is clear that the envelope of the spectrum does not change significantly over this temperature range. The temperaure of the EUT is not normally controlled during an OATS measurement due to the interference from heating and cooling equipment however, further research is required to determine the worst operating temperature for

the IGBT with regards to radiated emissions and potentially using the figure of merit described in section 5.5.1 and laboratory measurements.

5.5 Identification and Influence of Radiated Emissions Sources

It has been shown that the radiated emissions measured from a VSD are dependent on the gate profile as illustrated by the use of different gate resistor values. It has also been shown that the radio frequency content as identified using the wavelet transform can be controlled with a specifically shaped gate profile. However it is unclear how the magnitude of the features identified by the wavelet transform can be related to the measured radiated emissions. The following section describes how the key linkages are identified and can be used as a useful tool for the prediction of radiated emissions.

5.5.1 Radiated Emissions Figure of Merit

The radiated emissions measurements are made using a receiver with a bandwidth of 120 kHz. In the time domain, this translates to a 30 μs period (to capture 95 % of the energy). Analysis over such a long time relative to the IGBT switching transient cannot be used to locate the radio frequency content in time. As shown, the Mexican hat wavelet transform improves on this utilising its bandwidth of 34.54 MHz with a time window of 10 ns.

For radiated emissions measurements, the standards set a limit line across a range of frequencies. A measurement above this limit at a single frequency is sufficient to fail a test, however, this may arise from a resonance feature peculiar to equipment connections and layout. As the emissions from the IGBT are broadband in nature in this work, the r.m.s. value of the emissions between 30 to 50 MHz from the peak detector is calculated for each frequency spectrum sweep and used as the radiated emissions figure of merit (REFOM) to describe that measurement. This increases the weighting of the measured peak values while considering the frequency range covered by the wavelet transform. For each gate profile applied to the IGBT, a REFOM can be calculated.

5.5.2 Analysis of Electrical Signals

To capture the electrical voltage and current waveforms requires the use of probes connected to the circuits as previously discussed. The gate emitter voltage probe is

connected using small coils soldered to the IGBT terminals to reduce the inductance of the scope ground terminal. The collector and emitter terminals on the IGBT are separated too far to use the same connection method. The extra length of the ground lead is wrapped around the probe to minimise the stray inductance. The addition of voltage probes onto the nodes of the IGBT terminals adds additional capacitance however this is small compared to the IGBT internal capacitances. Inserting current probes around the wires adds additional impedance where datasheet values are 0.15 Ω at 10 MHz and 0.7 Ω at 100 MHz in series with the gate resistor and so, for consistency between electrical and radio measurements, and to allow correlation between the wavelet transform from the measured electrical signals and the EM waves, all probes remained connected in the circuit throughout testing. The oscilloscope is used to capture the V_{ge}, I_g, V_{ce} and I_c. There are no further channels available on the scope to capture the filtered V_{ce} or load current.

Where the wavelet transform gives a good insight to the time location of the RF content, the resulting measurement needs to be presented in a form which can be directly compared to the REFOM. As mentioned previously, the peak detector with 120 kHz bandwidth averages the amplitude of the signals in the time domain over 30 μs hence for an IGBT transition time of several hundred nanoseconds, the RE measurement using the peak detector includes a contribution from each of the peaks identified by the wavelet transform. As the radio frequency content only appears during the transient and not when fully switched on or off, the mean wavelet transform over the measurement time of (2 μs) is used to describe each test and are referred to as wV_{ce_mean}, wI_{c_mean}, wI_{g_mean} and wV_{ge_mean} for each of the measured signals.

5.5.3 Emissions Sources and Gate Profiles

It is shown in Figure 5-13 that the power supplies and measuring equipment has a small but measurable emission signature in the frequency domain. In a similar manner, when the FPGA programme controls the shaped pulse train to the IGBT but with the high voltage dc power supply discharged, a significant increase in emissions is measured. When the gate drive PCB is disconnected from the IGBT and operated in an identical manner, the increase in emissions can no longer be detected hence it is deduced the

emissions arise from either the magnetic field from the gate current loop (formed from the gate drive output, through the short wire through which the gate current is measured, through the C_{ge} and returning through the short emitter wire) or the electric field from the gate emitter voltage. This loop is larger than would be expected in a commercial VSD as a Tektronix™ TCP0030 current probe is inserted. In an effort to characterise this phenomenon, two sets of measurements are taken and analysed. For the first set, the gate wires are maintained as short as possible while allowing for the connection of the current probe. In the second set, the emitter wire in the gate loop is significantly increased to create a large loop antenna shown in Figure 5-19. The two test series are referred to as "No Loop" tests and "Loop" tests.

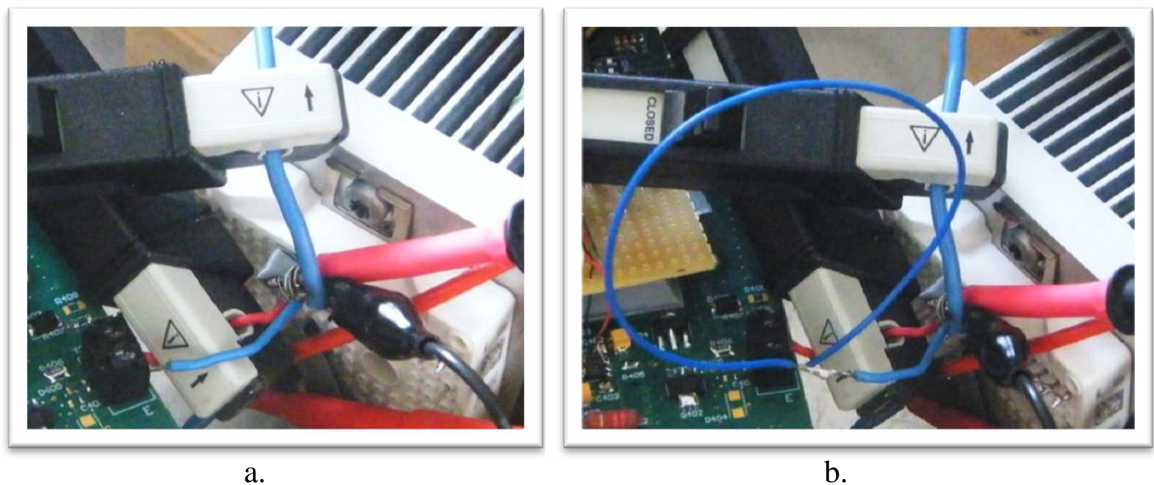


Figure 5-19: a) Connection of FPGA gate drive PCB to IGBT, No Loop; b) connection with Loop inserted in path

To assess the impact of the RF content in the gate current on the emissions, the REFOM is plotted against the measured wI_{g_mean} in Figure 5-20 on a linear scale. The radiated emissions have increased significantly with the addition of the gate loop which can be used to identify the loop as the emissions source. It is not possible to fully characterise the performance of this loop antenna from these limited test results and broadband frequency measurements. While these emissions are present and significant, field strength is low in comparison to those from the IGBT when switching high voltages and currents. While the applied gate profiles in each case are identical, the addition of the large loop in the gate circuit alters the impedance and resonance which strongly

influences the measured gate voltage at the terminals of the IGBT. Several measurements were repeated and checked to ensure consistent measurements however only one result for each setup is shown. This scenario illustrates how a change in the physical structure of the EUT can influence both the electrical signals within the circuit and also the radiated field strength.

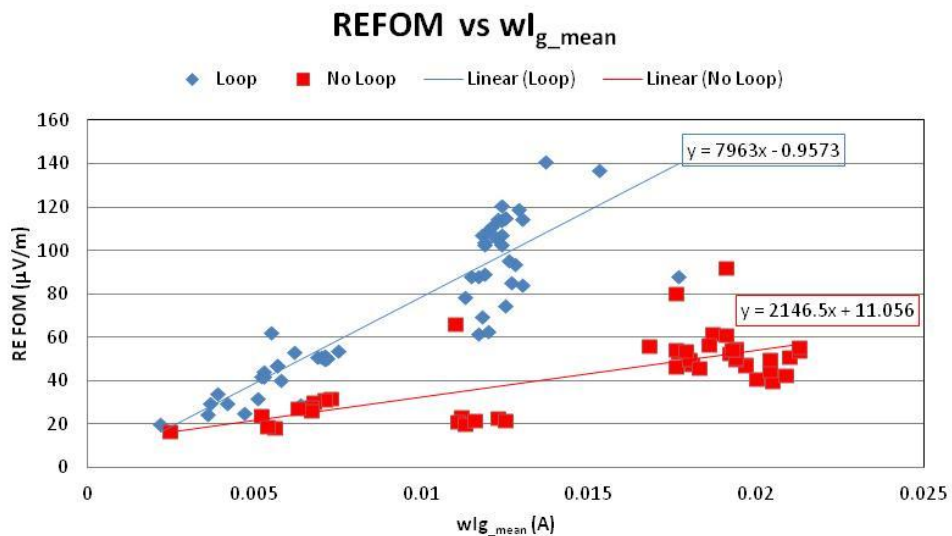


Figure 5-20: Change in REFOM versus wI_{g_mean}

The mean of the voltage wavelet transform (wV_{ge_mean}) is also plotted against REFOM in Figure 5-21. It can be observed that REFOM increases approximately linearly with the wV_{ge_mean} for both sets of tests but with a different gradient. This is unexpected as the change to the parasitic electric field antenna due to the loop is minimal hence the E-fields relative to the ground reference will not change.

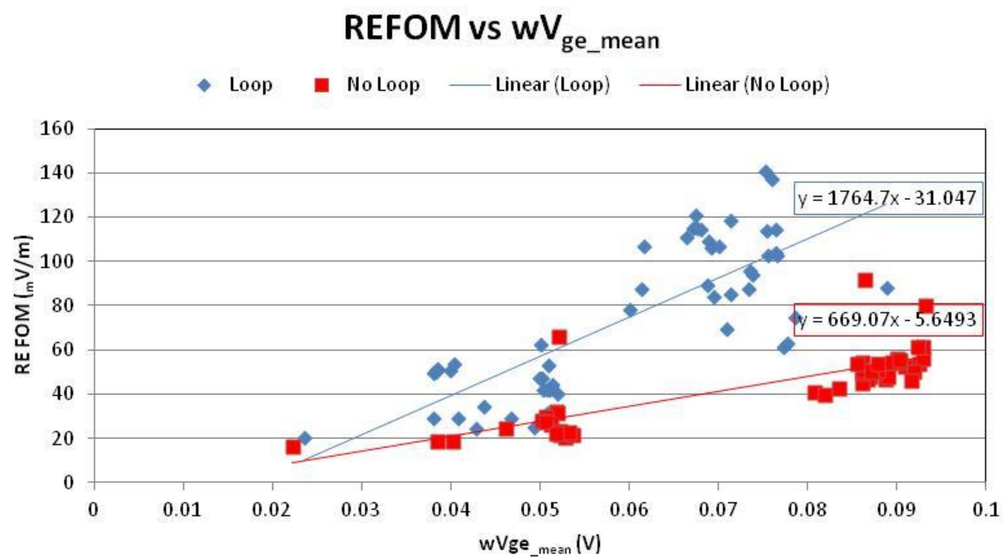


Figure 5-21: Change in REFOM versus wV_{ge_mean}

The increase in REFOM with gate voltage can be explained when considering the circuit impedance. The wavelet transform shows that the RF peaks in the voltage and current occur at the same location in time and hence are linked via the circuit impedance. This can be seen in Figure 5-22 where the peak wavelet magnitude for the gate voltage (wV_{ge_pk}) is plotted against the peak wavelet magnitude for the gate current (wI_{g_pk}). A trend line has been fitted which identifies the impedance over the frequency range evaluated by the wavelet transform.

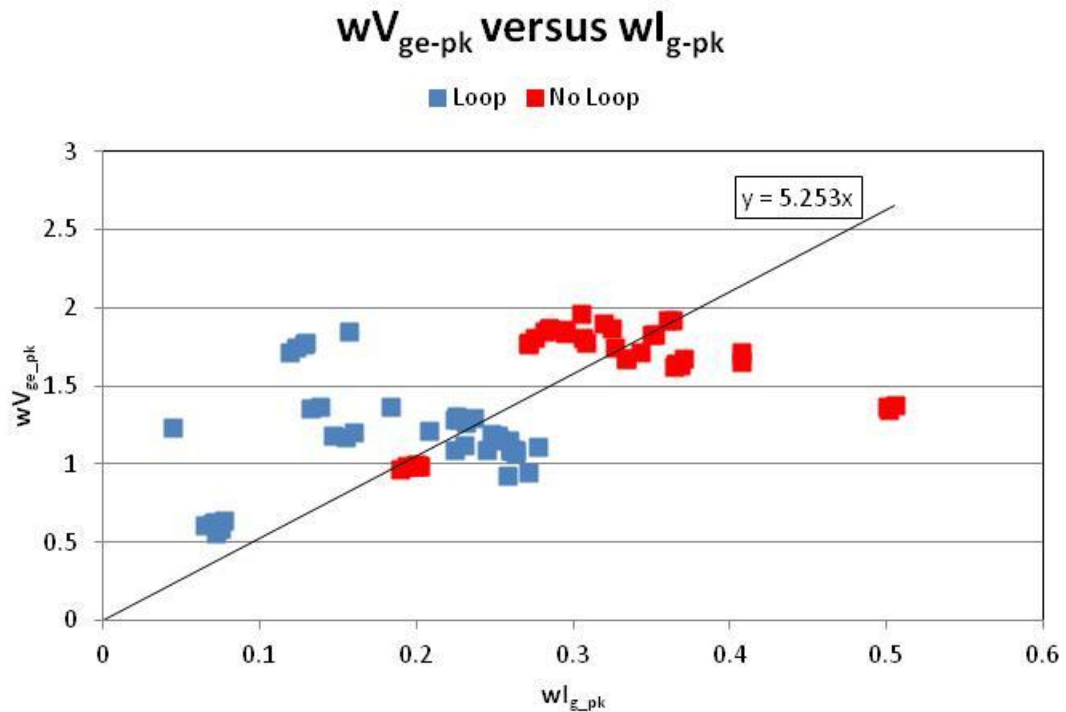


Figure 5-22: Change in gate circuit impedance Loop and No Loop

Enabling the dc bus voltage and repeating measurements with the range of gate demand profiles for both Loop and No Loop conditions, the REFOM is plotted versus the mean of the wavelet transform of V_{ce} (wV_{ce_mean}) in Figure 5-23 and wI_{c_mean} in Figure 5-24. It can clearly be seen that the emissions increase approximately linearly with voltage. The inclusion of the gate wire loop alters the magnitude of the RF components for each test however the relationship between the REFOM and wV_{ce_mean} is constant. This indicates that the small increase in emissions due to the gate circuit loop is insignificant to the measured RE when the IGBT is switching at a high bus voltage (however this may be responsible for some of the variance in the measurement).

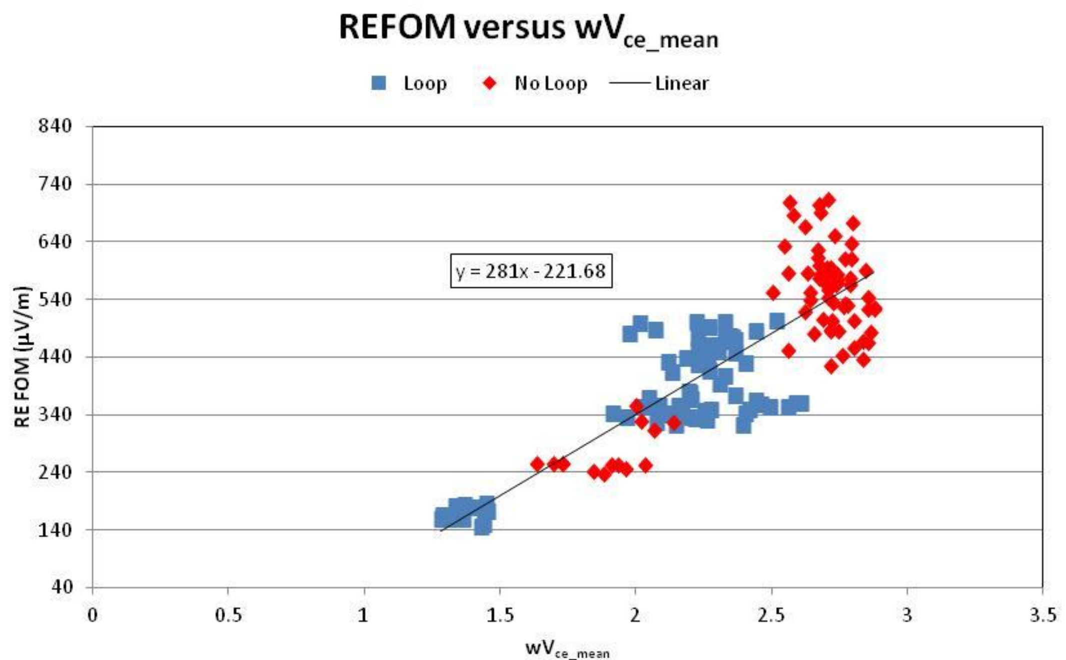


Figure 5-23: REFOM versus wV_{ce_mean}

As identified earlier, a rapid change in collector current induces a change in the collector emitter voltage due to the stray inductance and is unavoidable. However during the switching transients, a change in current as the diode begins to block voltage will correspond to a large change in V_{ce} due to the transitional changes within the devices. Care has been taken to only include the results where there is minimal change in V_{ce} due only to the stray inductance in Figure 5-24. No correlation could be found between the current and wavelet magnitudes and the emissions.

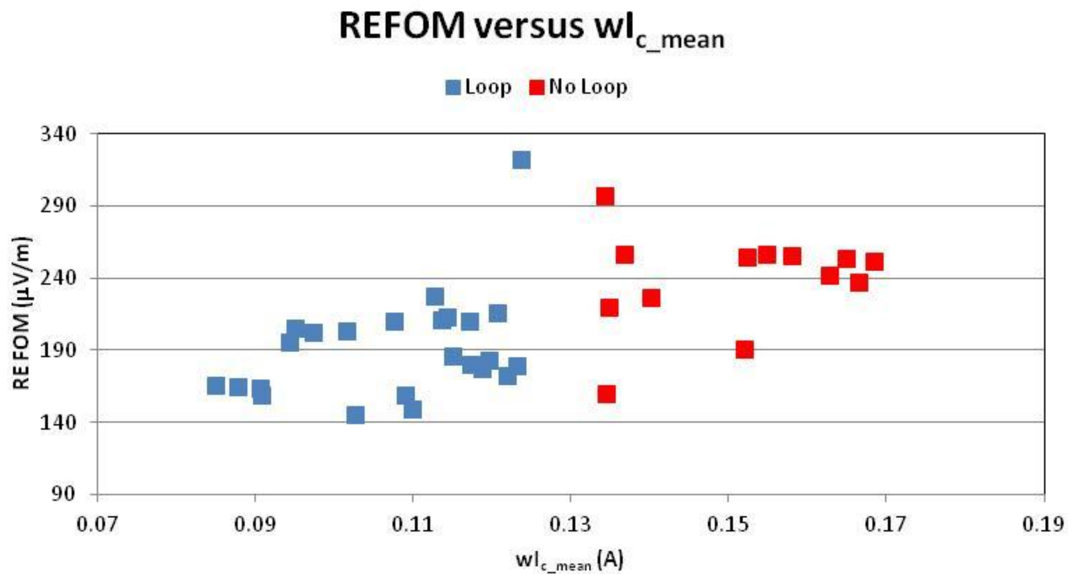


Figure 5-24: REFOM versus wIc_mean

To assess the use of the V_{ce} high pass filter, the I_c probe is disconnected from the oscilloscope (but remains connected in the circuit) and series gate profiles are re-evaluated. A DFT of the filtered signal is carried out and the mean of all components between 30-50 MHz calculated and referred to as V_{RF}. V_{RF} is plotted against REFOM in Figure 5-25.

As with the wV_{ce_mean}, a linear trend line can be fitted to the data using linear regression further confirming that the dominant source of the radiated emissions can be related to the RF content in V_{ce}. The goodness of fit in both cases has been evaluated using the coefficient of determination (R^2) where a value of 1 is a perfect match. When using the wavelet transform, R^2 = 0.74 compared to R^2 = 0.88 for the filtered signal. The radiated emissions can be approximately related to the mean of the filtered voltage be equation (5-1).

$$REFOM = 7840 \times V_{ce_{mean}}(Filter) + \ 96.198 \qquad (5\text{-}1)$$

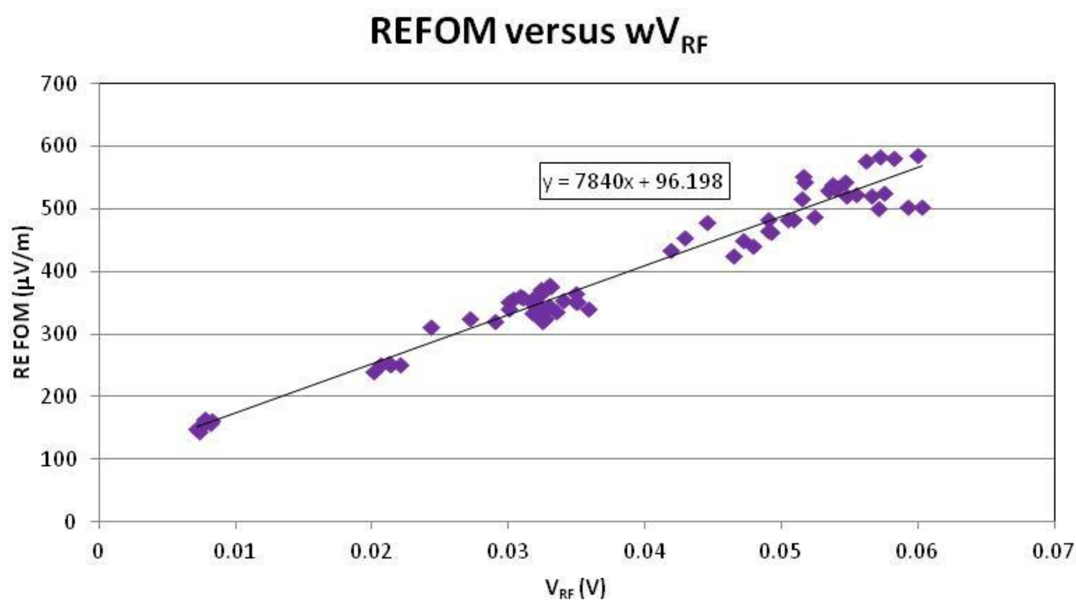


Figure 5-25: REFOM versus V_{RF}

As the radiated emissions limits are defined in dB, a comparison between REFOM and the V_{RF} shows a maximum error ± 1.0 dB µV/m for this setup (see Figure 5-26). Using wavelets alone, the maximum error is ± 3.2 dB µV/m. The variance can be attributed to fluctuations in temperature, contributions from other sources such as gate current, background disturbances, etc.

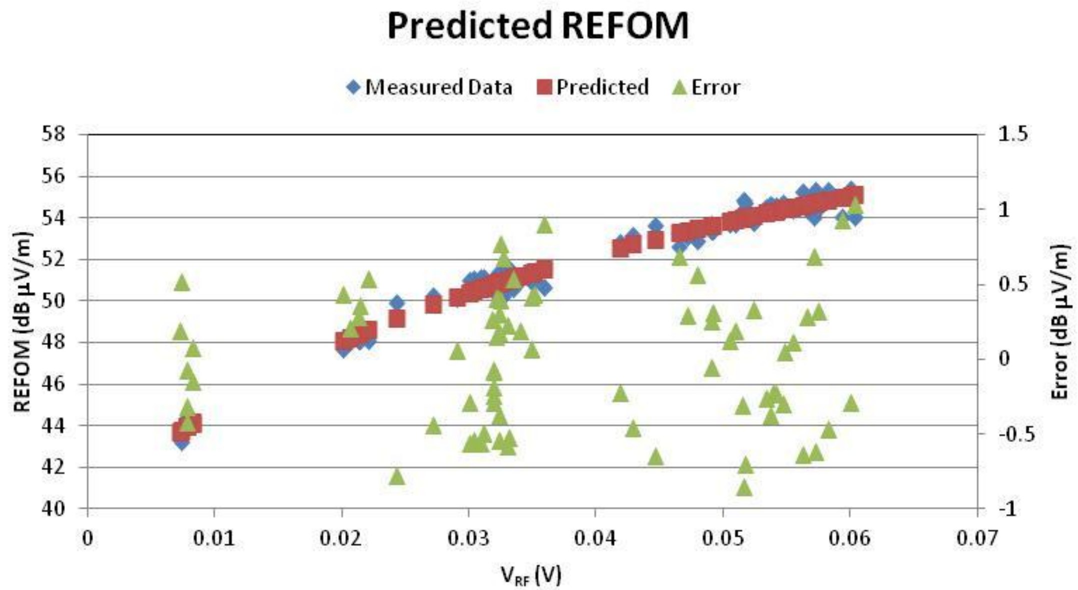


Figure 5-26: Predicted REFOM from V_{RF} measurements

There is a clear relationship between the measured radiated emissions from the simplified test setup and the measured collector emitter voltage wavelet magnitude which is further improved with the use of a high pass filter. There remains a significant uncertainty surrounding the exact sources. While no clear linkage can be determined between wI_c and REFOM, the testing of the gate loop indicates that the current loop can be an effective source of emissions and may be responsible for the variance. In a real VSD, the collector current loop and loop impedance would be further reduced with careful design consideration and is hence less likely to contribute to the emissions.

The potential sources of RE are considered in chapter 2 where the cable can act as an antenna for several sources. While the main electrical source for the measured radiated emissions has been determined above to be V_{ce}, it is not clear which of the identified antennas is responsible for the emissions. These details would be important factors in the cable selection however when using the IGBT gate drive to reduce radiated emissions, this is not important.

5.5.4 Minimum Rise/Fall Time

The location of the breakpoints in an ideal trapezoidal is discussed in chapter 2 where it is shown that the radio frequency components can only be influenced by waveform

shaping for a limited range of rise/fall times using a trapezoidal approximation. The rise time can be reduced further with the use of an s-ramp profile while having a lower amplitude above 30 MHz. For the simplified test setup used above, and using equation (5-1) to fit V_{RF} to REFOM, a value of 40 dB (μV/m) corresponds to 0.245 V (107.8 dB μV). While the limit lines given in Table 4-2 (and adjusted for measurements at 3 m) are for a quasi peak detector, it is found that an REFOM of 40 dB (μV/m) gives a pass for most tests when using a quasi peak detector.

The newly defined voltage limit can be used in conjunction with the analysis in section 0 where the envelope of the signal spectrum must be at or below the limit at 30 MHz. Evaluation of this limit for an ideal trapezoid and a 1st derivative s-ramp switching pattern is shown in Figure 5-27.

The envelope can be constructed for the waveforms by plotting the breakpoints and connecting them with straight lines with increasing gradient. The amplitude up to the first frequency break point (fc1) is given by (5-2) where T is the measurement period and t is the on time of the trapezoid. The second break point (fc2) (equation (5-4)) is given for a rise time (t_r) where a rise time of 134 ns and will just meet the limit for RE at 30 MHz with the trapezoidal waveform as shown in Figure 5-27. Using an ideal s-ramp where the time for the first derivative ($t_{r_dv/dt}$) is half of t_r introduces a third breakpoint (fc3) (equation (5-5)). The rise time can be reduced to 77 ns while still meeting the required limit at 30MHz for the s-ramp. Section 4.4 described how the switching losses are dependent on the voltage rise time hence by using a shaped voltage transient, the losses can be reduced in comparison to the ideal trapezoid. When using a 43.7 Ω resistor and a step gate voltage input which passed the radiated emissions test, the measured rise time is 121 ns which lies between the two ideal wave shapes presented here.

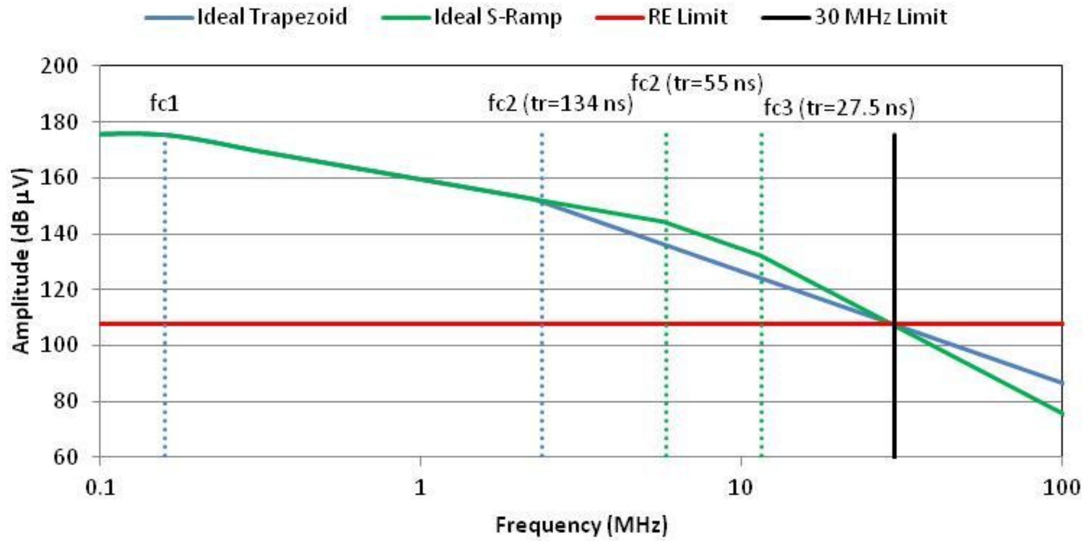


Figure 5-27: Rise Time Limits based on Ideal Trapezoid and Ideal S-ramp

$$A = 20 \times \log\left(\frac{\left(\frac{2 \times V \times t}{T}\right)}{1\mu V}\right) \tag{5-2}$$

$$fc1 = \frac{1}{\pi t} \tag{5-3}$$

$$fc2 = \frac{1}{\pi t_r} \tag{5-4}$$

$$fc3 = \frac{1}{\pi t_{r_dV/dt}} \tag{5-5}$$

The amplitude at fc1 is related to the dc bus voltage as given in (5-2) (600V in this example). Using this relationship, it becomes clear that as the bus voltage increases, t_r must have a corresponding increase to maintain compliance to the emission limits. Conversely, as the voltage is reduced, t_r can reduce.

5.6 Summary of Chapter 5

The control of the radio frequency content in the switch on transient of an IGBT via the gate emitter demand voltage has been demonstrated. By utilising this technique, it is possible to separate in time the features in the collector current waveform from those in the collector emitter voltage.

Although the relative magnitude of voltage in collector emitter voltage and gate emitter voltage is very different, the radiated emissions depend on the antenna efficiency hence signals cannot be compared to each other as the layout, separation and loop areas etc are different. A simplified radiated emissions apparatus setup has been described and investigated for a comparative evaluation for the dominant source of radiated emissions. Four potential sources have been measured and while it is possible to see that more than one source is responsible for the measured radiated emissions, a strong dependence on the radio frequency content measured from the collector emitter voltage has been found. No relationship could be found between the RF content in the collector current and the measured radiated emissions.

This voltage has been analysed mathematically using the wavelet transform to both identify the dominant sources of the emissions in time and also using a hardware high pass filter to improve the signal to noise ratio. In both cases, the emissions increased linearly with the mean of the calculated and measured signals. The variance and hence error in predicting the emissions is lower when using the hardware filter. Using this presented method of measurement, a very strong linkage between electrical measurements and radiated emissions has been established and has achieved a key objective of this research.

Using the relationship linking electrical measurements to radiated emissions, the allowable RF content in the collector emitter voltage can be predicted for each physical structure to comply with the radiated emissions limits in the standards. This has then been translated into an allowable rise time for the ideal trapezoidal waveform and the s-ramp. In reality, the switching pattern is likely to lie within these two ideal shapes hence these can be used as a guide to possible switching losses.

While the linkage has been established between the collector emitter voltage and radiated emissions, it is not possible to determine which mechanism or mode as described in section 2.3.1 is predominately responsible for the transmitting antenna, however several mechanisms can be discounted such as the current loops within the drive and current loops coupling in the near field. This is an area for further study to determine the exact radiating structures. The sacrifice of the switching losses using this gate driving process is not important for the research in this chapter. Now that the linkage of the collector emitter voltage to radiated emissions is confirmed, it is possible to investigate the operational modes of the VSD system and implement this new knowledge to reduce the switching losses.

Chapter 6: Radiated Emissions from a Variable Speed Drive

6.1 Introduction

This chapter examines how the linkages which have been determined in chapter 5 between radiated emissions and the RF content in the collector emitter voltage (V_{RF}) can be exploited to reduce the switching losses in a VSD system capable of rotating a motor. A commercially available VSD, Control Techniques™ DST1405, is studied in detail including all components which influence the impedance of the output phase connection and the physical connection of the shield. The wavelet transform is used to illustrate the sources of the peak of the RF content whereas the high pass filter discussed in chapter 4 is used to evaluate and predict the radiated emissions. The effect of the switching frequency and modulation strategy on radiated emissions are presented and discussed.

The relationship between the switching energy loss and the radiated emissions with both fixed resistor gate drive and shaped gate transient are presented together with a possible circuit solution to exploit the optimum solution.

6.2 The Commercial VSD for Evaluation

A Control Techniques™ DST1405 servo drive is chosen for evaluation of the radiated emissions performance. This VSD consists of a three phase rectifier, dc bus capacitors and 6 discrete IGBT and diode DuoPacks. The IGBTs are Infineon™ IKW40N120T2 trench gate and field stop technology IGBTs with soft, fast recovery PT anti-parallel diodes and do not contain an internal gate resistor. The gate drive consists of a fixed resistor for switch on with a parallel path to reduce the switch off resistance. The IGBT datasheet recommends the use of a 12 Ω resistor however for compliance with radiated emissions, a 24.2 Ω resistance is used leading to higher than desired switching losses.

6.2.1 Modulation Strategy

To create the sinusoidal output voltages and currents, the VSD must control the switching pattern of the six IGBTs. Modulation strategies differ in software complexity and performance, however space vector modulation (SVM) is used in the DST1405 [1, 117]. Output demand vectors can be represented by time averaging three different

switching combinations in a particular sextant for the hexagon as shown in Figure 6-1 where the rotational speed of the vector determines the fundamental electrical output frequency. Each leg in the IGBT bridge is represented with either a 1 or 0 indicating the output phase as either high or low.

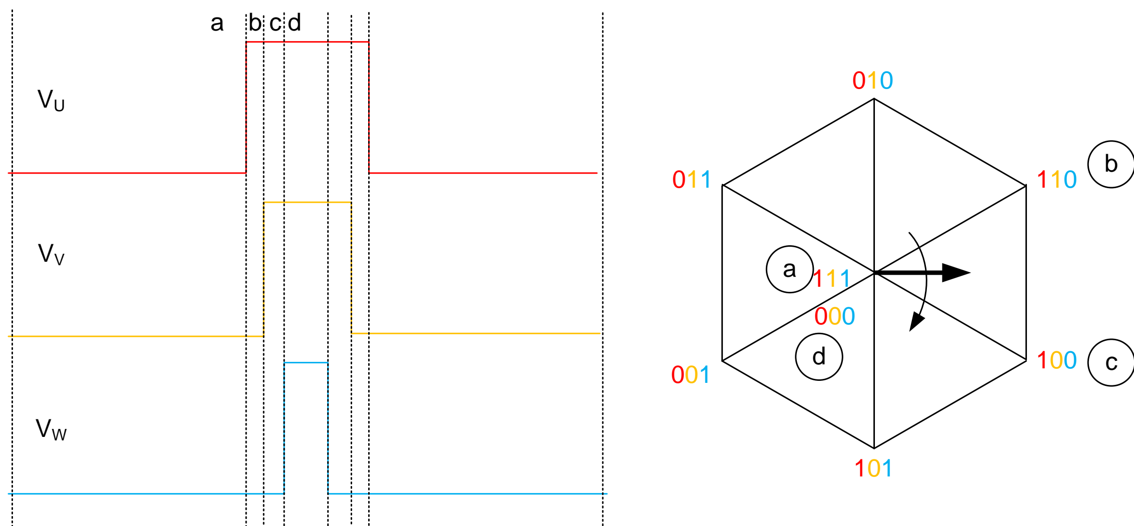


Figure 6-1: Illustration of SVM

During radiated emissions testing, a permanent magnet motor is rotated at no load and at a constant speed. The required torque, hence, current increases slightly with output speed to supply the increased motor losses. As discussed previously, the bandwidth of the receiving antenna during radiated emissions, is 30 µs. When operating at a low speed, the required output voltage is low hence time period d is short compared to period a ashown in Figure 6-1. At low current, the three rising edges and the three falling edges are close in time when using SVM. It is possible that all six pulses occur within the response time of the receiver even for low switching frequencies. At low currents, and when operating with a fixed gate resistor, the transient voltages contain higher levels of RF content as will be discussed in section 6.4. Under these conditions, the measured radiated emissions will be high. As the speed increases, the first three pulses separate in time from the latter three pulses due to the increasing back electromotive force (e.m.f.) and fall outside the measuring period reducing the measured

radiated emissions. Measurements (using a peak detector) with different motor rotational speed are shown in Figure 6-2.

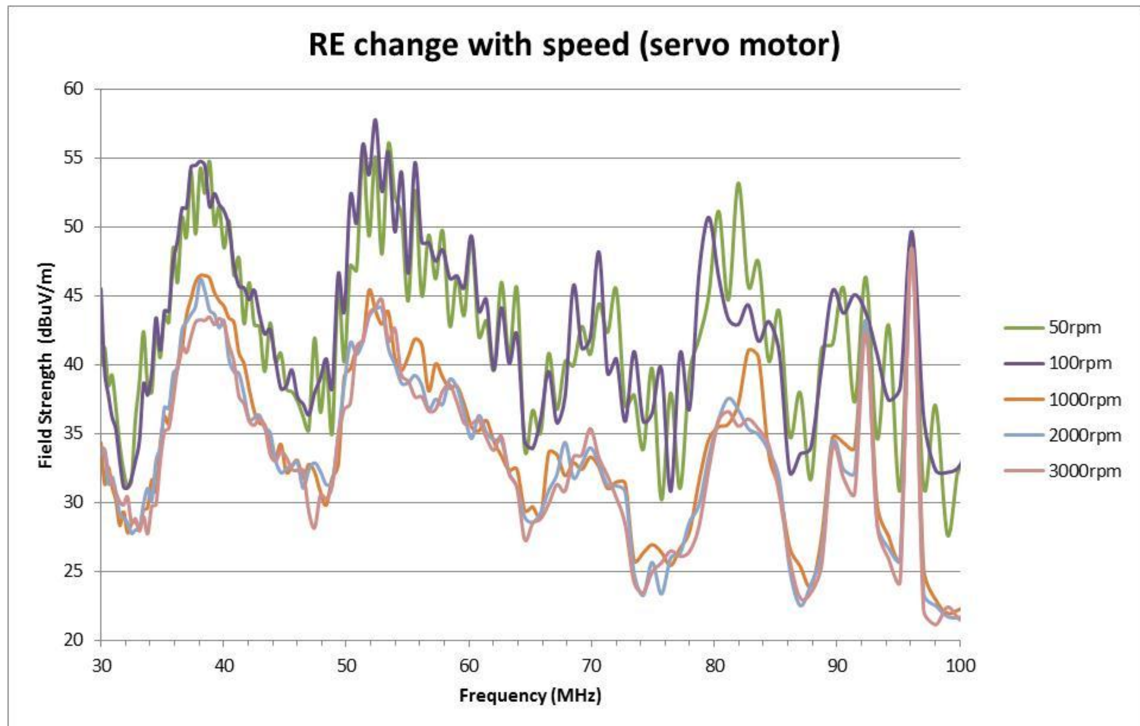


Figure 6-2: Change in radiated emissions levels with change in motor rotational speed.

The cable capacitance as seen by the VSD depends on the output vector position. To determine the impact of this on radiated emissions testing, the VSD is set to a stationary output vector and the emissions measured. The vector is rotated by 30° and the measurements repeated. The results can be seen in Figure 6-3. It is clear that the spectrum changes with the vector however, there are two distinct signatures shown. At 0°, and at intervals of 60°, only one phase in the cable is switched high to the dc bus voltage however at 30° and at intervals of 60°, two phases are switched to the dc bus voltage. During the compliance testing, the quasi peak receiver time constants smooth out the influence of the RE change with vector positions and hence give another explanation for the quasi peak value being lower than the peak.

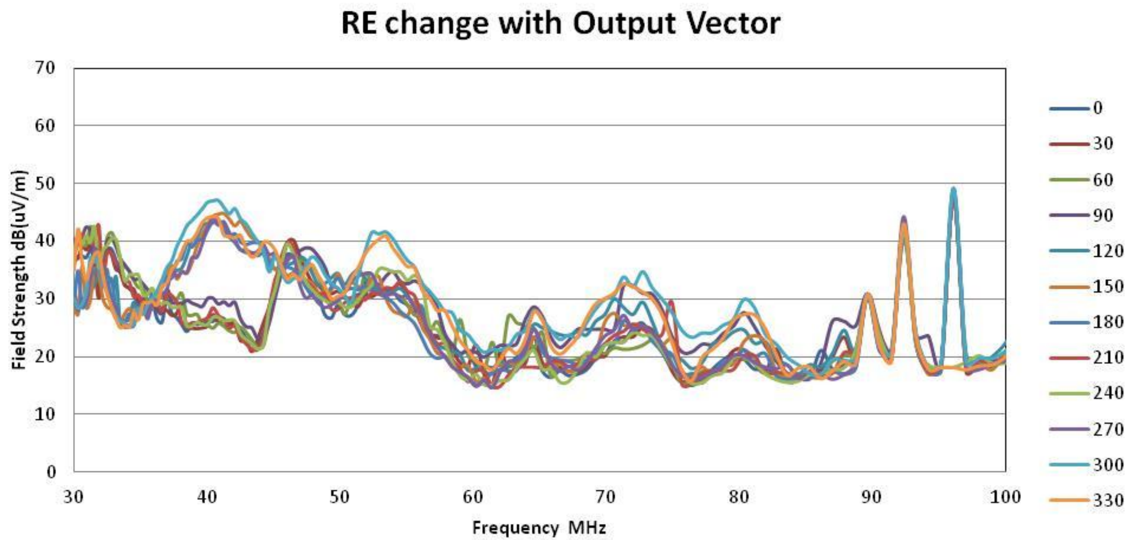


Figure 6-3: Change in radiated emission levels with output vector.

6.2.2 Switching Frequency

The DST1405 switching frequency is user selectable and can be used to optimise the system dynamic performance, reduce audible noise or increase VSD or motor efficiency. Radiated emissions measurements from operation at different switching frequencies, are shown in Figure 6-4. An increase in the peak emissions can be observed as the switching frequency increases but only at low rotational speeds. This phenomenon can also be related to the modulation strategy where the time between switching periods is reduced at higher switching frequencies causing more pulses to be captured within the receiver period.

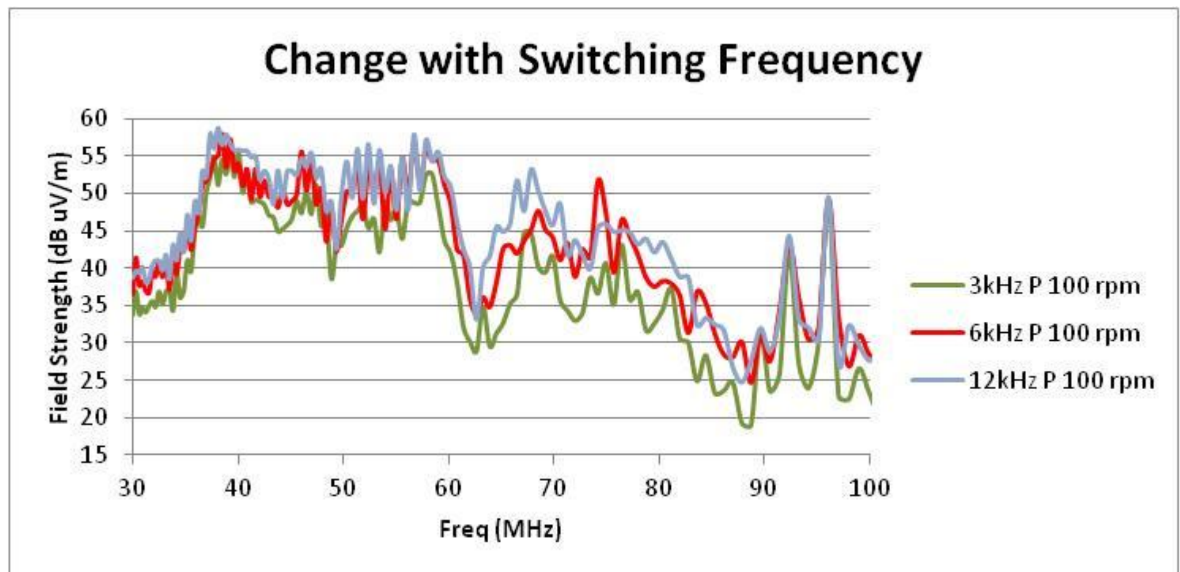


Figure 6-4: Change of radiated emissions with switching frequency

6.2.3 Gate Drive

The gate supply rails are powered using a flyback converter from the dc bus which gives four isolated 24 V gate supplies, one to power the three lower IGBTs and one for each of the upper devices. The schematic is shown in Figure 6-5 where the voltage from the transformer secondary windings is rectified and filtered. The voltage rails are split using a Zener diode to give +18 V and -6 V relative to the IGBT emitter. The switching signal is supplied from the microprocessor via an optocoupler which provides galvanic isolation. When switched on, current flows from the +18 V supply rail, through the series resistors (R_{on_a} and R_{on_b}) to the gate terminal of the IGBT and returns from the emitter to the negative rail via the capacitor (C_{ge_x}). For switch off, the optocoupler switches the output to the -6 V rail which discharges the IGBT gate capacitance via the parallel combination of the resistors (R_{on_b} and $R_{on_a}//R_{off}$). The values of three gate resistors are determined during product development to provide compliance to IEC61800-3 [6] for radiated emissions. The gate voltage is held negative when off to increase the noise margin for immunity to high dV/dt on the phase conductor particularly during short circuit conditions.

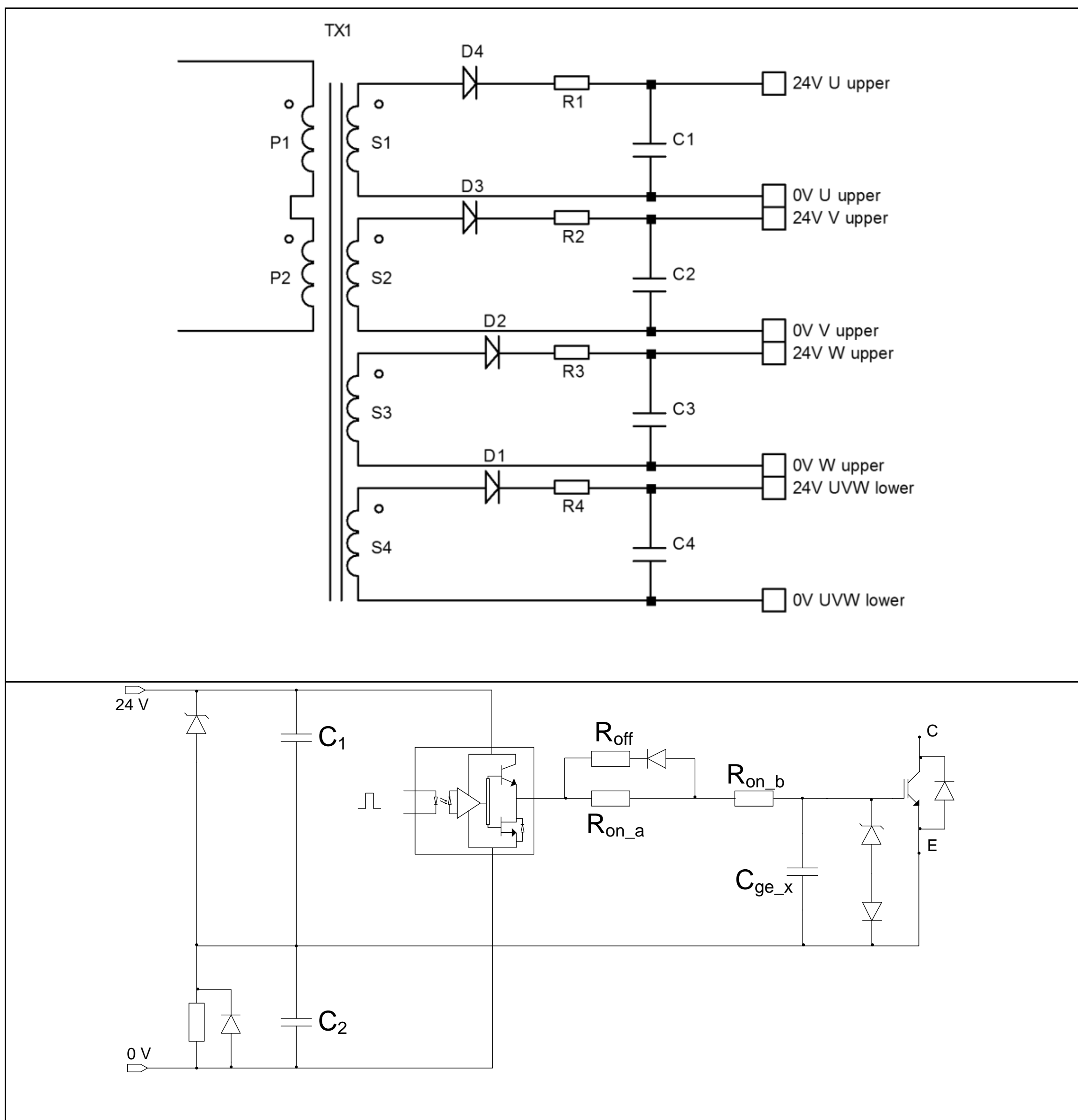


Figure 6-5: DST1405 gate drive circuit.

For accurate control purposes, the output current must be known for each switching cycle. The output phase is connected to a primary winding of a direct current current transformer (DCCT) where two output phases are combined on one DCCT reducing the number of required DCCTs to two. A current is applied to the secondary winding of the DCCT to maintain zero flux in the measuring device. The bandwidth of the DCCT circuit is 100 kHz which is suitable for measuring at the maximum output frequency but cannot measure any EMI related phenomenon.

A common mode filter (toroidal ferrite) surrounds the three output phase connectors (with two turns of each phase) which provides high impedance at high frequencies and

is intended to reduce radiated emissions. The three output phases terminate in a connector to which the motor cable is attached. The cable shield is connected to a specially provided bracket providing low impedance to the reference ground. In the simplified test setup, the emitter of the IGBT is connected to ground, the test chassis and cable shield, hence, measurements of V_{ce} are relevant for radiated emissions. The cable shield is no longer connected to the IGBT emitter when the VSD power is supplied through the rectifier however the VSD ground is connected to the negative dc bus via an X1 class capacitor providing low impedance between the shield and dc link at radio frequencies.

To facilitate compliance to conducted emissions a custom designed conducted EMI filter is connected between the mains supply and the rectifier. This prevents HF signals from propagating along the mains cables and provides a reduction in radiated emissions.

6.3 Measuring Probes and Ancillary Hardware

As noted during the RE measurements of the simplified VSD system, the impedance of the measuring probes has a strong influence on the IGBT transient switching trajectory. When carrying out pulse testing for energy loss measurements, a current probe is required to determine the collector current trajectory. The influence of this probe on the voltage transient can be seen in Figure 6-6 where the initial step in the voltage is due to the probe insertion impedance and the stray inductance of the wire loop required to physically locate the probe. The potential error in RF measurement due to the probes can be seen in Figure 6-7 where a significant difference can be observed in the wavelet magnitudes. When the VSD system is evaluated for RE, measuring probes are not attached and so it is important that the same circuit impedance is used for any laboratory measurements. The connection of the conducted EMI filter, all appropriate earthing structures and cable length as used for RE testing are included in laboratory measurements for RE as these also influence the switching trajectory and the dissipated switching loss.

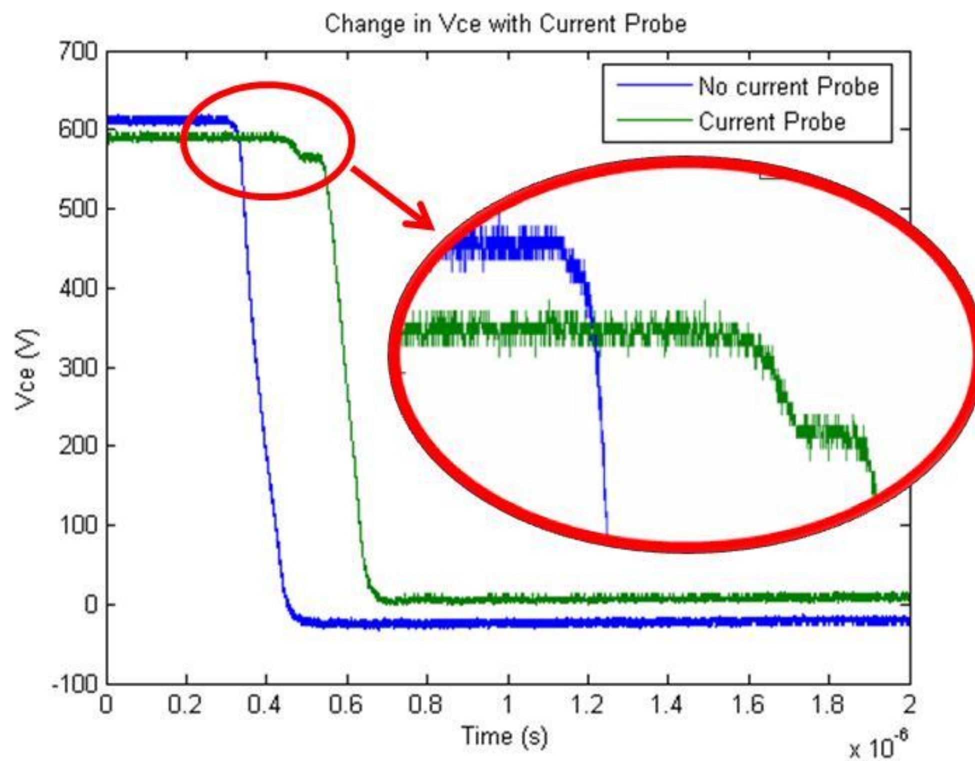


Figure 6-6: Impact of current probe on voltage switching trajectory

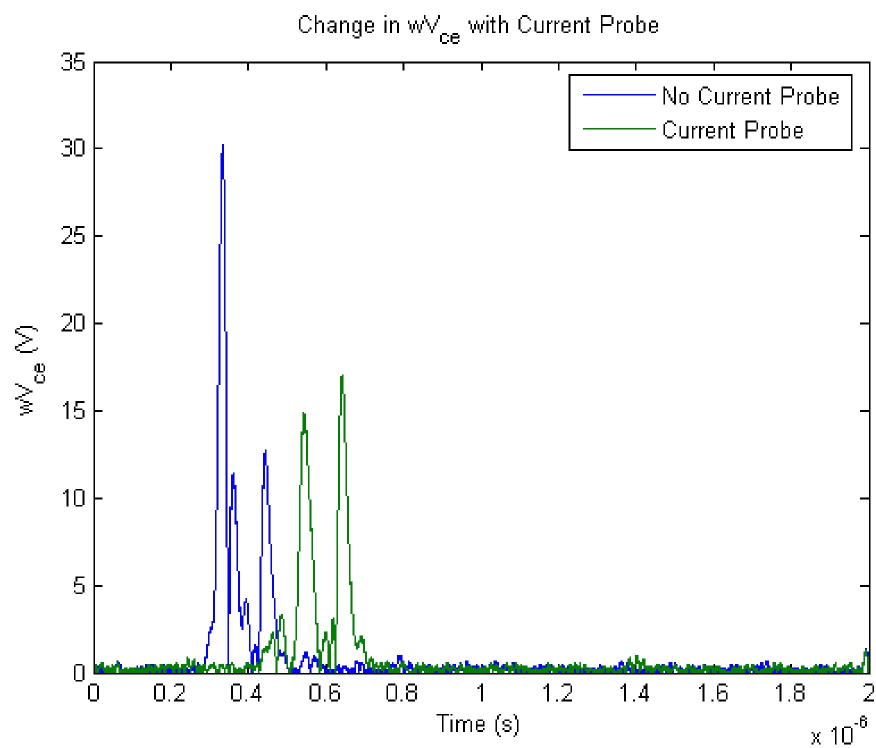


Figure 6-7: wV_{ce} for switch on transient with and without collector current probe.

To achieve the necessary high bandwidth for the radiated emissions, non-isolated voltage probes are used. The current measurement is made on the motor end of phase conductor where the probe impedance is small compared to the load and hence will have minimal influence on the switching trajectory. The cable capacitance (phase to all other phases and shield = 1.2 nF for the 5 m cable tested) is significantly greater than the probe capacitance (6 pF) and no influence of the voltage probes could be detected. The unused phase is connected to positive dc while capturing voltage measurements. Figure 6-8 illustrates the measurement setup.

Figure 6-8: VSD Pulse Test Setup.

6.4 Fixed Gate Resistor VSD Operation

As shown previously, it is possible to make a VSD to comply with the radiated emissions limits by increasing the gate resistance. To rotate an electrical machine, the output current varies sinusoidally at a frequency related to the motor rotational speed. The torque delivered to the load is determined by the magnitude of the output current from the VSD. Considering this, the load current, as chopped by the IGBT will vary between zero Amperes and the VSD maximum overload current.

As established from the semiconductor physics in chapter 2, the transient operation of the IGBT and diode will vary with the collector current. To determine the influence of this on the radiated emissions, pulse testing is carried out on the DST1405 servo VSD with the designed gate impedance (24.2 Ω) over the current range. The voltage transient is measured between the output phase terminal and the negative dc terminal for several load currents (Figure 6-9).

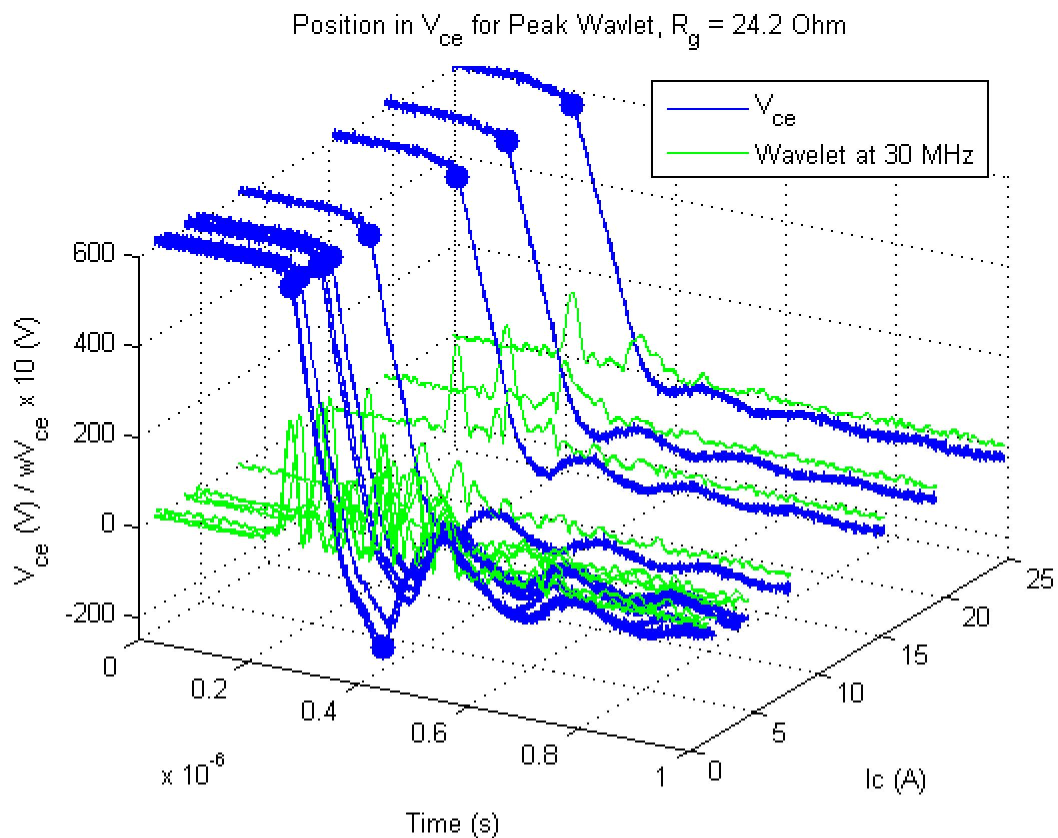


Figure 6-9: Switch on transient and peak emissions for R_g = 24.2 Ω

A 200 V undershoot can be seen in the voltage waveform when measured at the VSD's terminals which is not present in the simplified test setup. As the IGBT switches on, the change in voltage creates a travelling wave along the cable towards the motor. The terminal impedance of the motor is significantly higher than that of the cable hence current reflections occur [13, 16, 118]. The effect of cable reflections are observed previously in the collector current of the simplified pulse test setup, however they did not contribute to a significant disturbance in the voltage waveforms.

The change in the voltage waveform can be attributed to the use of the common mode toroidal ferrite which surrounds the three phase conductors as they leave the VSD and the DCCT. The inclusion of the ferrite presents three new effects with regards to radiated emissions:

1. a higher impedance is seen by the IGBT which reduces the transient time of the IGBT which, in turn, generates more RF content when measured at V_{ce}.

2. some of this RF content is blocked from reaching the cable by the ferrite which induces a series voltage to compensate. The current which still contains a significant RF content, travels along the cable and reflects from the motor terminals. This reflected current returns to the VSD and is observed flowing through the IGBT collector.
3. due to the high impedance of the ferrite, a voltage drop due to the reflected current flowing through the ferrite creates the 200 V undershoot is observed. The DCCT is connected in series with the ferrite and contributes to the impedances as shown in Figure 6-10 measured with zero curent bias.

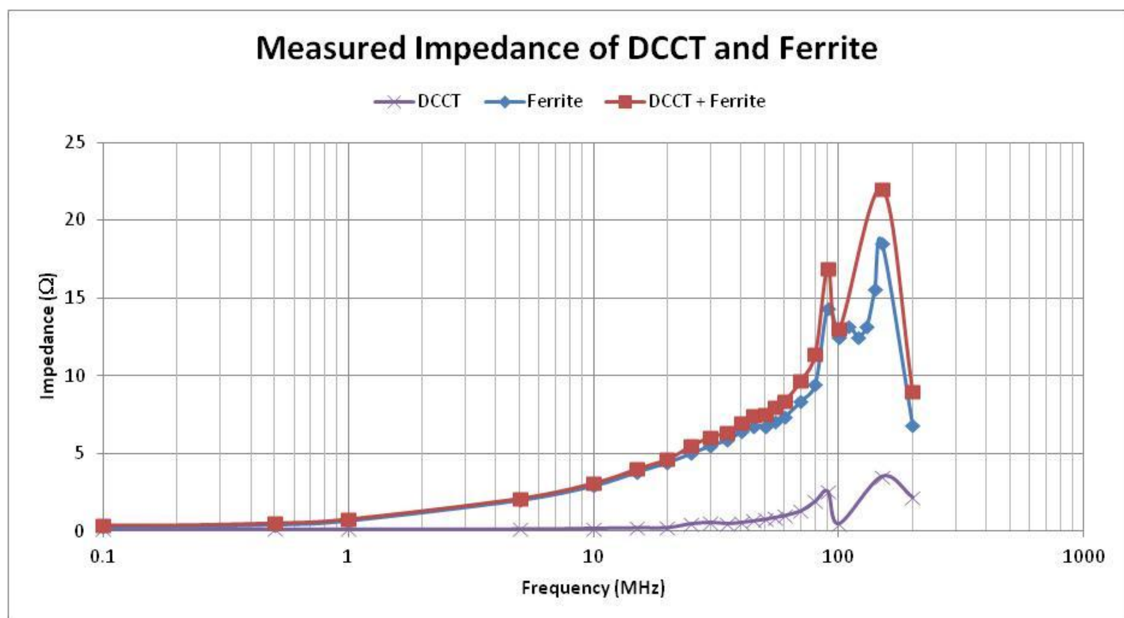


Figure 6-10: Measured Impedance of Ferrite and DCCT

This operation of the ferrite is an example of mode conversion where a differential current with RF content reflects along the phase conductor and creates a common mode voltage drop which contributes to radiated emissions. It also provides coupling between the output phases minimising the net common mode RF voltage.

When operating with a three phase output the sum of the three phase currents is approximately zero hence the ferrite does not saturate. During this pulse testing, only one phase is enabled hence the ferrite aims to restrict all the current. The ferrite does not approach saturation during this testing and its temperature remains below the curie point (112 °C) [119].

As the voltage on the cable is responsible for the radiated emissions, the series of testing is repeated with the output voltage measured relative to ground rather than the negative dc bus (see Figure 6-11). The transient voltage pattern is similar to V_{ce} measurements however the voltage has been offset by 300 V. This is due to the dc power supply reference to ground. The magnitude of the wavelet transform has altered a little due to the impedance between the ground and negative dc bus. At the lowest measured current, the reflected current returns to the VSD before the IGBT voltage has finished its transient. The voltage drop across the ferrite adds to the falling voltage drop across the IGBT giving a large peak in RF content at this point.

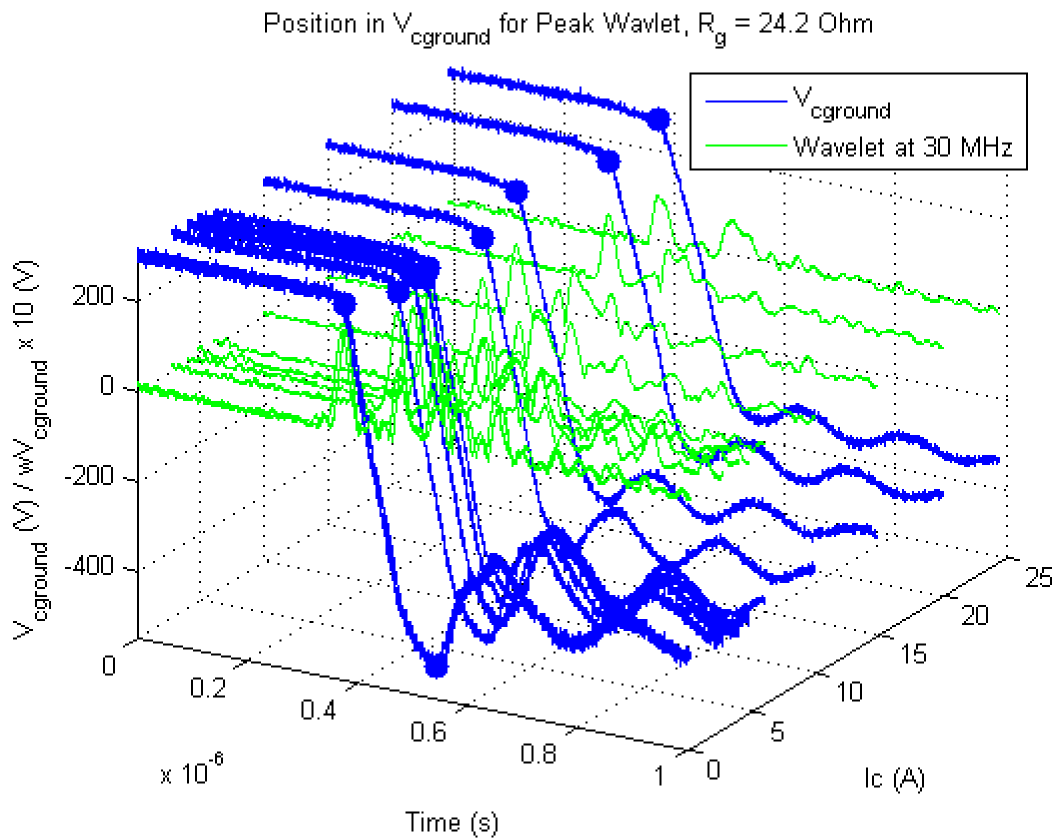


Figure 6-11: Switch on transient and peak emissions for R_g = 24.2 Ω measured to ground

At higher load currents, the voltage of the Miller plateau has increased hence the available gate current to complete the switching transient is reduced resulting in lower dV/dt. As the dV/dt reduces, likewise the reflected current magnitude hence voltage undershoot also reduces. The dV/dt versus current is shown in Figure 6-12 for different gate resistor values.

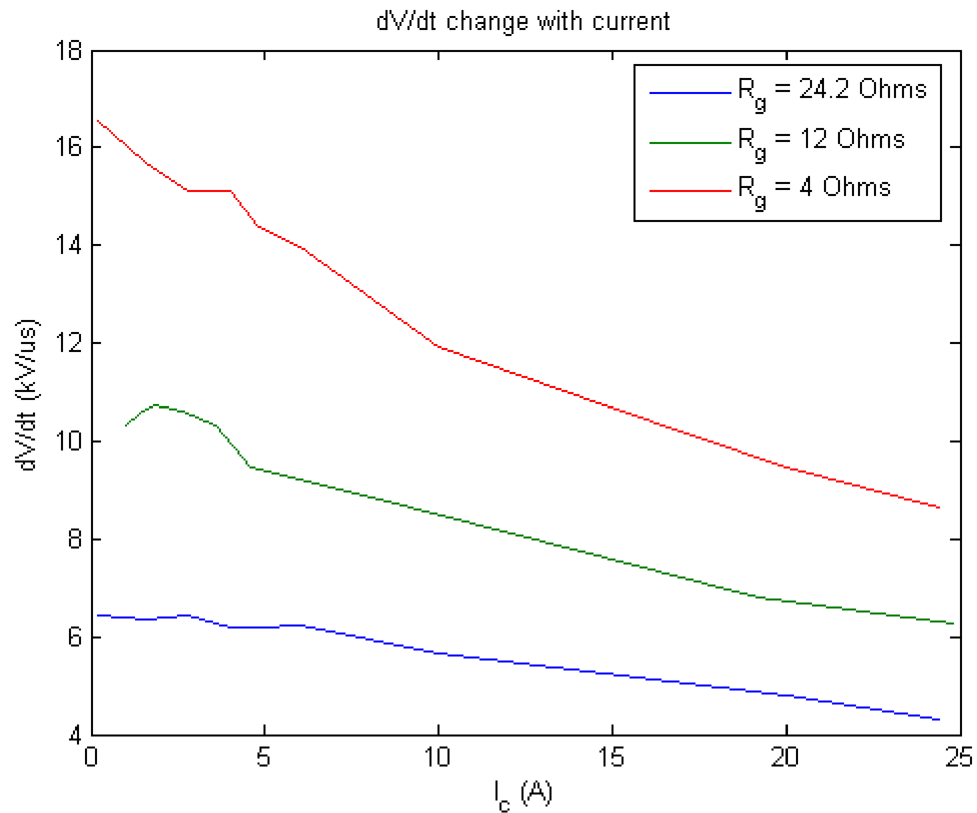


Figure 6-12: Change in dV/dt with current

This series of pulse tests is repeated using the manufacturers' datasheet R_g value of 12 Ω (Figure 6-13). In this case, we can see a slight voltage drop due to the stray inductance of the bus bar and the increased rate of change in current due to the smaller resistor. The bus bar inductance in this physically small VSD is low and includes a snubber capacitor located close to the IGBTs to limit voltage overshoots during the switch off of a short circuit condition. Therefore the large step in voltage as seen in the simplified setup cannot be observed. As the dV/dt has increased with this resistor value, it is possible to see a change in the shape of the voltage transient at low currents. The voltage transient can be seen to approach the IGBT saturation voltage just as the reflected current returns. In this case, the peak emissions remain at the point where the diode begins to support the voltage.

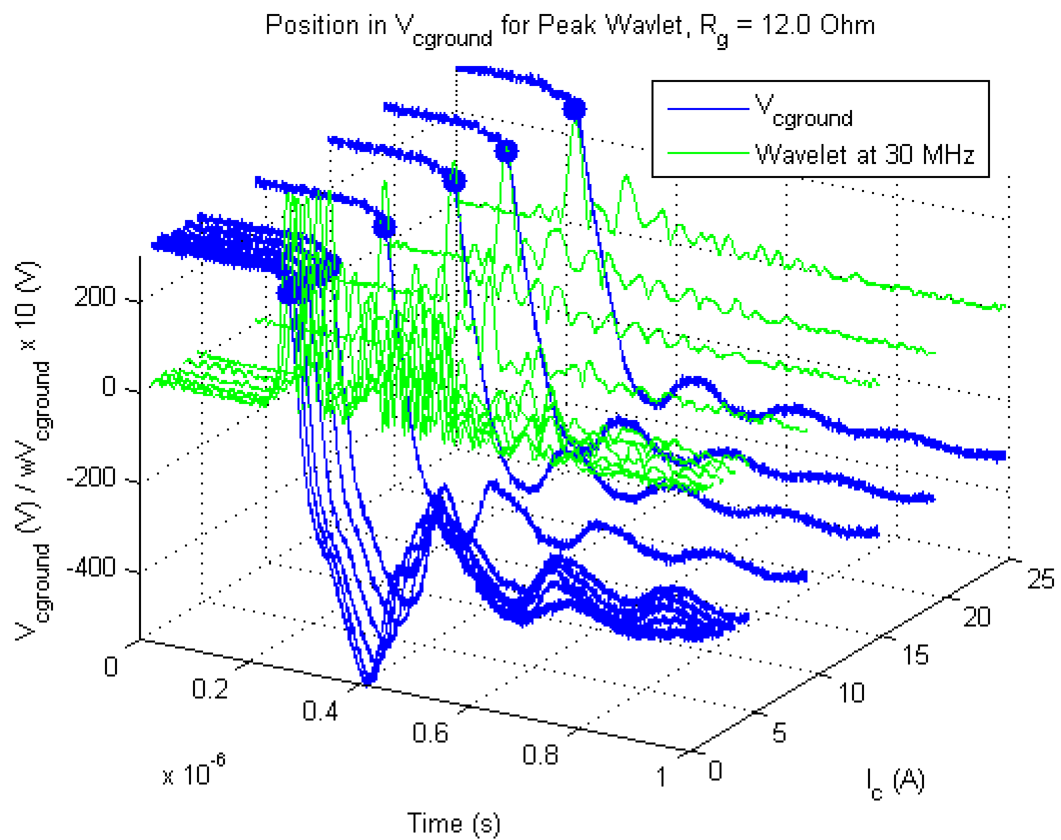


Figure 6-13: Switch on transient and peak emissions for R_g = 12 Ω

For testing with the 4.0 Ω gate resistor (shown in Figure 6-14), the further increase in dV/dt has led to a pronounced step in the voltage transient at the low currents. At this point, it can be seen that the peak wavelet magnitude occurs as the IGBT reaches the saturation voltage (point 4) just before the reflected current causes the voltage to undershoot.

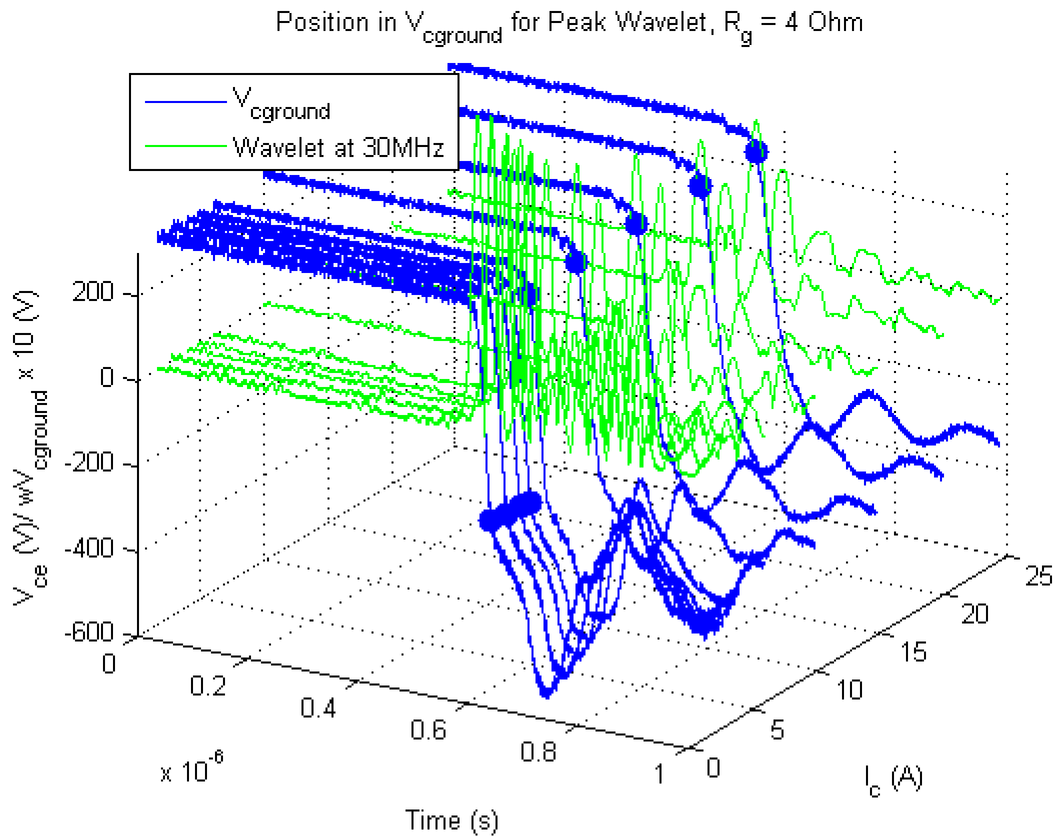


Figure 6-14: Switch on transient and peak emissions for R_g = 4 Ω

6.5 Switching Energy Loss

One of the important parameters which depends on the switching speed and hence the gate resistance is the switching loss. For each of the conditions shown above, the switch on energy loss is calculated from the voltage and current waveforms and is plotted in Figure 6-15. (Note the collector current transient is measured during a separate pulse test from that used to measure wV_{ce} to avoid distortion of the waveform). Although the exact switching energy cannot be accurately measured with this method, it does give a useful basis for a comparative evaluation.

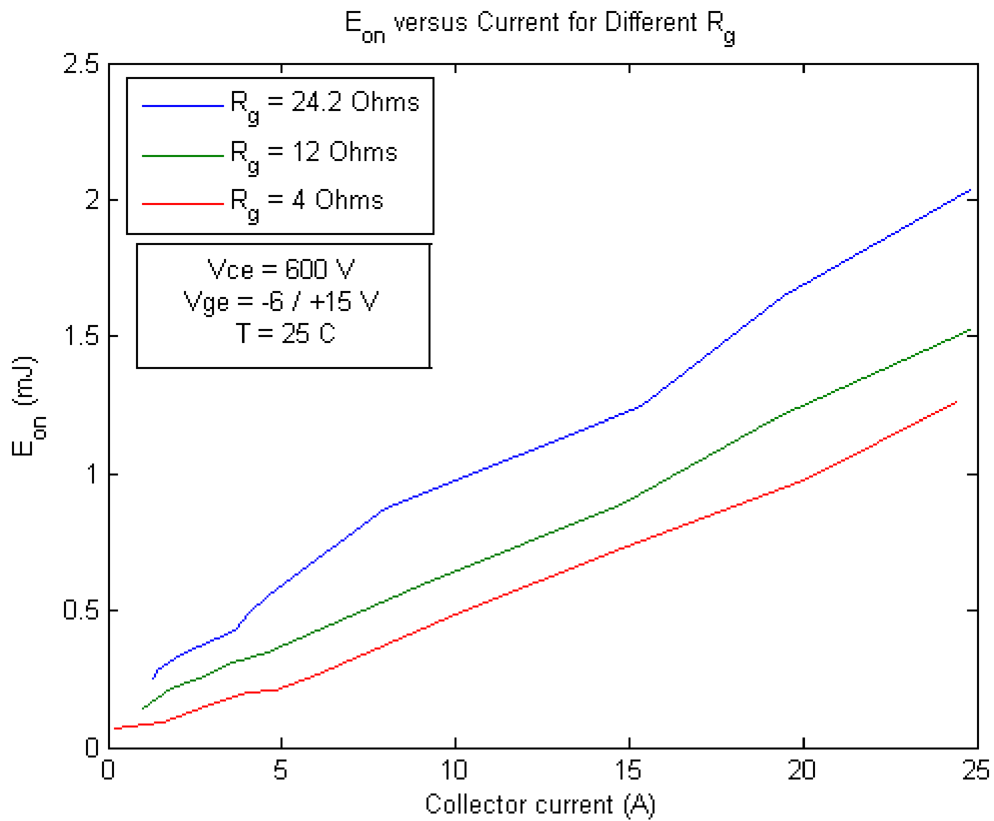


Figure 6-15: E_{on} for each of the above conditions

As expected, the switching time (hence switching loss) increases with the gate resistance. Under these conditions, the loss using the 24.2 Ω resistor has increased by 33 % compared to the datasheet resistance of 12 Ω.

6.6 Radiated Emissions Predictions

It was found in chapter 5 that the measured radiated emissions can be predicted from the measurement of the voltage transient using a physical high pass filter (V_{RF}). The results for each of the three gate resistances are shown in Figure 6-16 versus current. It is clear that for each case, the highest level of RF content is present at the lowest output current and as expected, the smallest gate resistor contains the largest voltage magnitude.

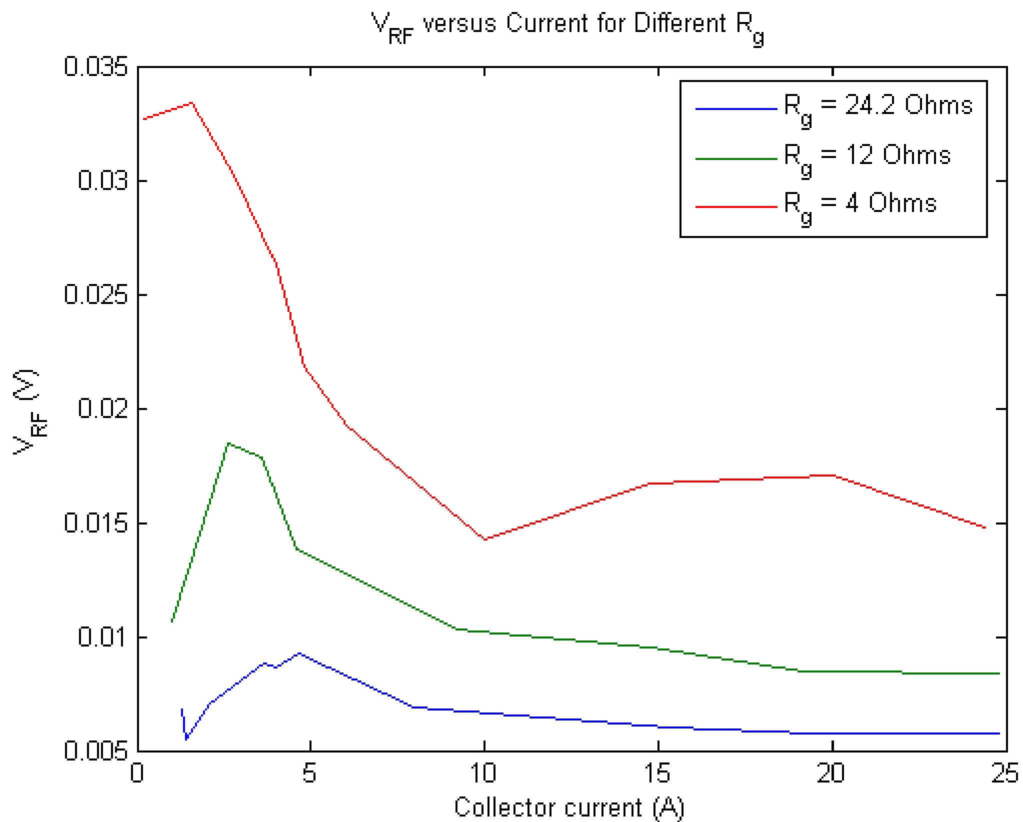


Figure 6-16: change in V_{RF} with current for different R_g.

As discussed in chapter 3, many publications in the literature have assumed that the radiated emissions are related to the dV/dt of the switching transient and while there is a relationship, this does not explain all the possible characteristics. Comparing Figure 6-16 to Figure 6-12 there is a general trend for emissions to reduce as the load current increases, However observing the dV/dt alone does not indicate the significant increase in emissions at low currents.

Radiated emissions measurements of the DST1405 (using the peak detector) from the three gate resistors are shown in Figure 6-17. It is clear to see how the reduction in gate resistance gives an increase in the radiate emissions, however it is important to note that the increase is not equal across the entire frequency range. For example between 30-33 MHz, there is no difference in the measured emissions from the 24.2 Ω resistor and the 12 Ω resistor however the peak value at approximately 40 MHz varies significantly for the three cases.

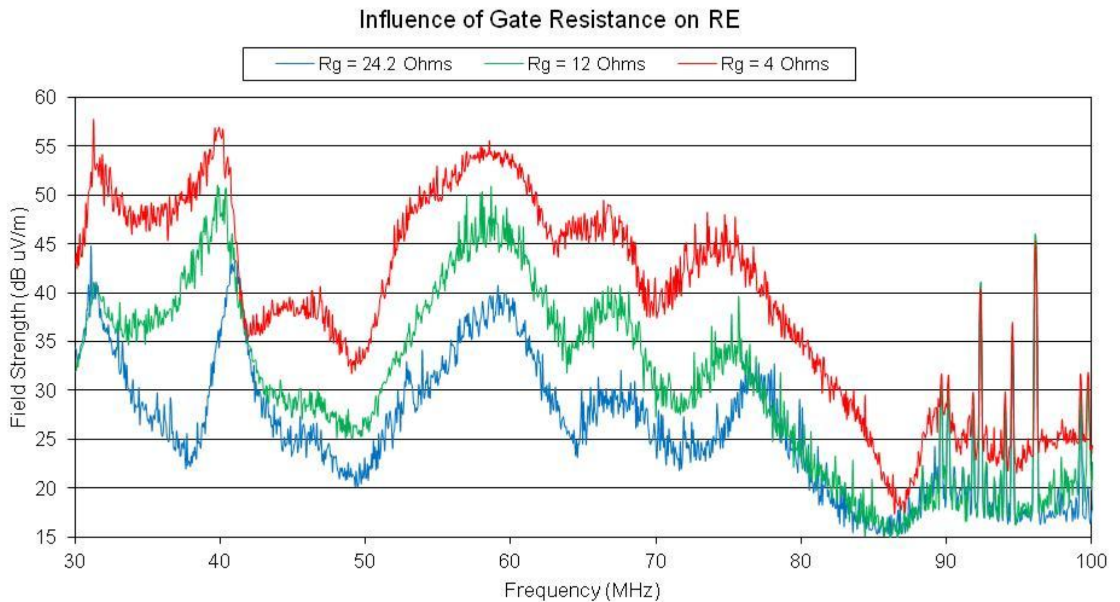


Figure 6-17: Measured Radiated Emissions for different R_g values

6.6.1 Switch Off

In the simplified testing, the switch off transient remained constant throughout all testing hence its impact on emissions is disregarded. With a fixed gate resistor value in the gate drive, it is not possible to ignore the contribution to RE. The different tests have been identified using the switch on resistance value shown in Figure 6-5 where Rg is the sum of R_{on_a} and R_{on_b}. For turn off, R_{on_a} is connected in parallel with R_{off} which in this case was a 6.8 Ω resistor resulting in a lower resistance during switch off. The peak emissions at switch off, as determined using the wavelet transform, for the DST1405 VSD always occurs at the peak of the voltage overshoot due to the diode forward recovery and stray inductance and hence increases with current as shown in Figure 6-18. At the higher load currents, the diode forward recovery voltage begins to decay before the peak voltage due to stray inductance has been reached smoothing the peak of the transient, reducing V_{RF}.

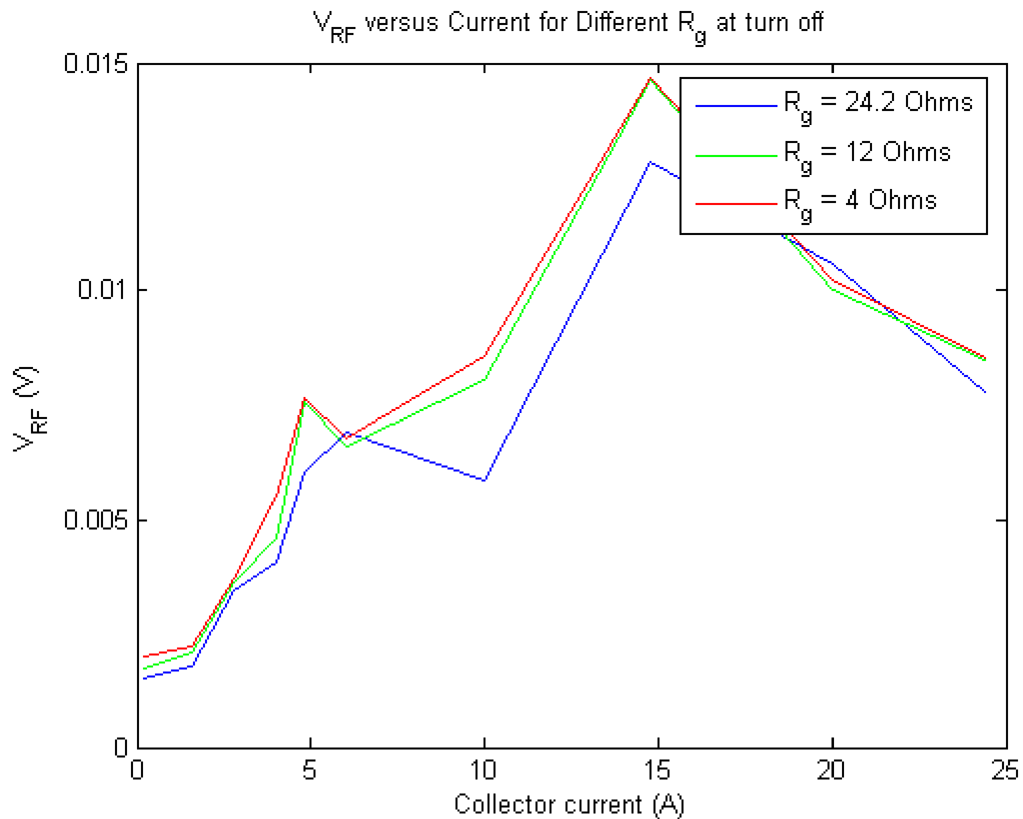


Figure 6-18: change in V_{RF} with current for different R_g at switch off.

The RF content in the switch off voltage is significantly lower than for switch on at low currents however this does increase to be a significant value at higher currents. The change in gate resistance has only a minimal influence on the measured emissions. As discussed in chapter 4, the receiver bandwidth of 120 kHz (which relates to a period of approximately 30 µs) will capture a contribution of the switch off transient at low currents. Where the mean of the filtered signal between 30-50 MHz is taken in for switch on, the sum of switch on and switch off is shown in Figure 6-19 and used to predict the radiated emissions.

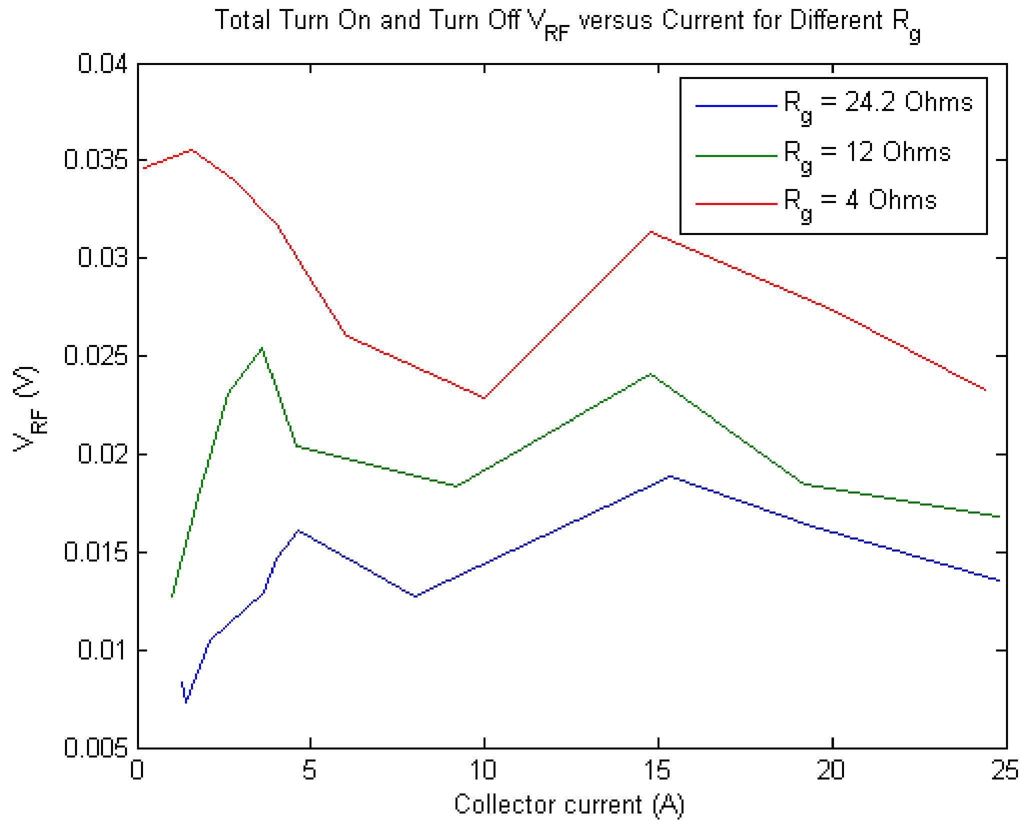


Figure 6-19: change in V_{RF} with current for different R_g (sum of switch off and switch on).

6.6.2 Filter Components

Two techniques have been used in the DST1405 to reduce the radiated emissions. The first is the inclusion of the EMC capacitor between ground and negative dc and secondly the ferrite ring surrounding the output phases. To assess the influence of these components, each is removed in turn from the VSD and the frequency content of the voltage transient measured at the VSD terminals with a gate resistance of 24.2 Ω. The results (for switch on), shown in Figure 6-20 are the RF content versus current.

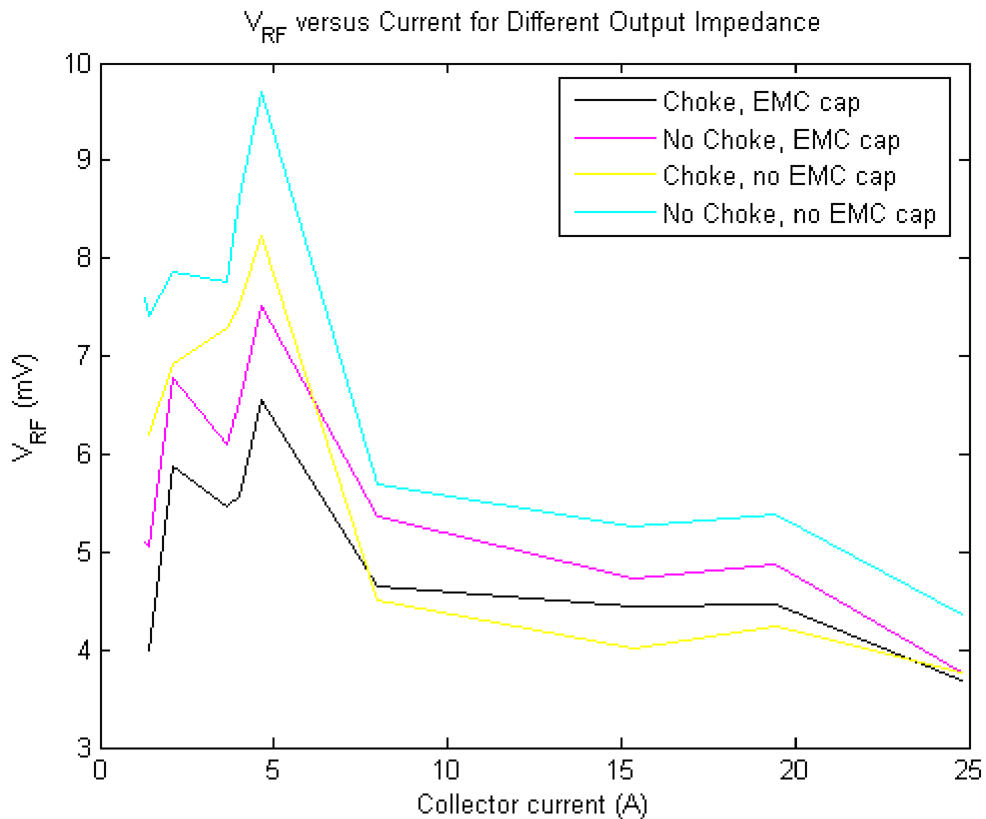


Figure 6-20: Measured V_{RF} with various combinations of filter components

It can be seen that the EMC cap offers a significant reduction of RF components across the range of currents. The addition of the ferrite has reduced the RF components significantly at low current outputs however the benefits are less clear as the output current increases.

Comparing the measured voltage results above to the measured radiated emissions for the four conditions (Figure 6-21 and Figure 6-22), the major problem with interpreting radiated emissions is highlighted. Where REFOM is calculated for each test configuration (and shown in the key) the order of these results can be correlated to the voltage measured with the high pass filter when the motor is rotated at 100 rpm (Figure 6-21). However, when the motor is rotated at 3000 rpm, the REFOMs for two of the conditions swap rank.

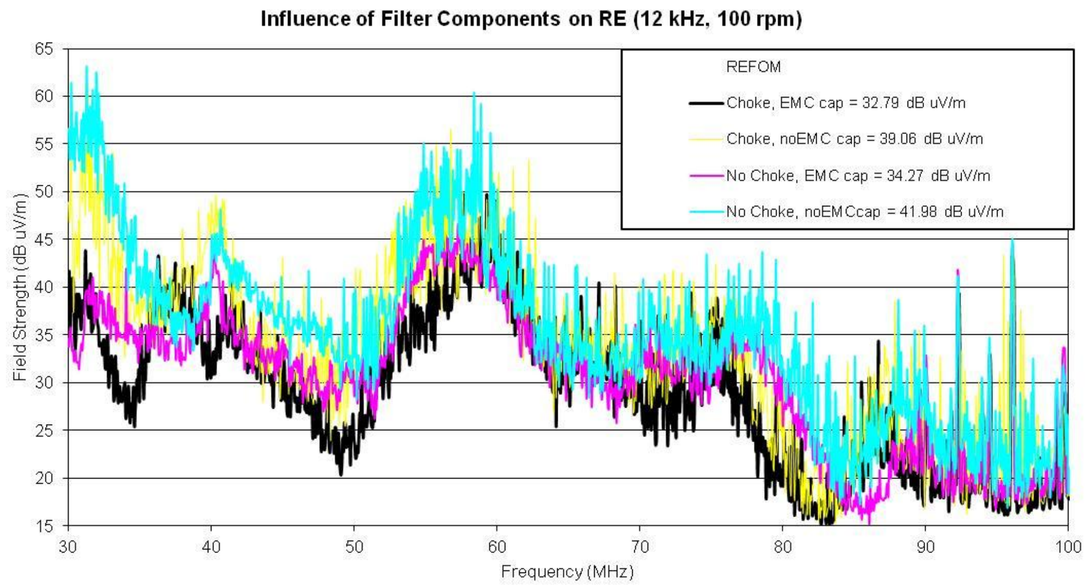


Figure 6-21: Measured Radiated Emissions for VSD internal filter components at 100 rpm

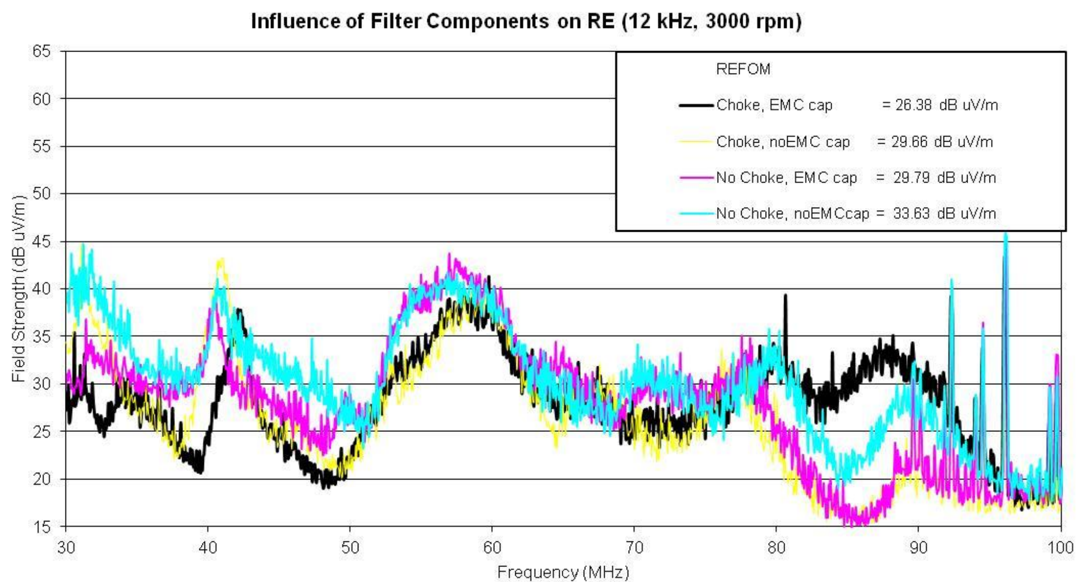


Figure 6-22: Measured Radiated Emissions for VSD internal filter components at 3000 rpm

In an effort to clarify this change of order, the REFOM for the two rotational speeds are plotted against the high pass filter output (sum for switch on and off) in Figure 6-23. By fitting a logarithmic curve to the datasets, it can be seen that the maximum deviation is ± 3dB. Hence the difference in emissions as predicted by the high pass filter is within an expected measurement error. This change of emissions with speed is an important

variable where the worst operating condition should be identified to determine a suitable pass / fail limit for V_{RF} for a range of drives.

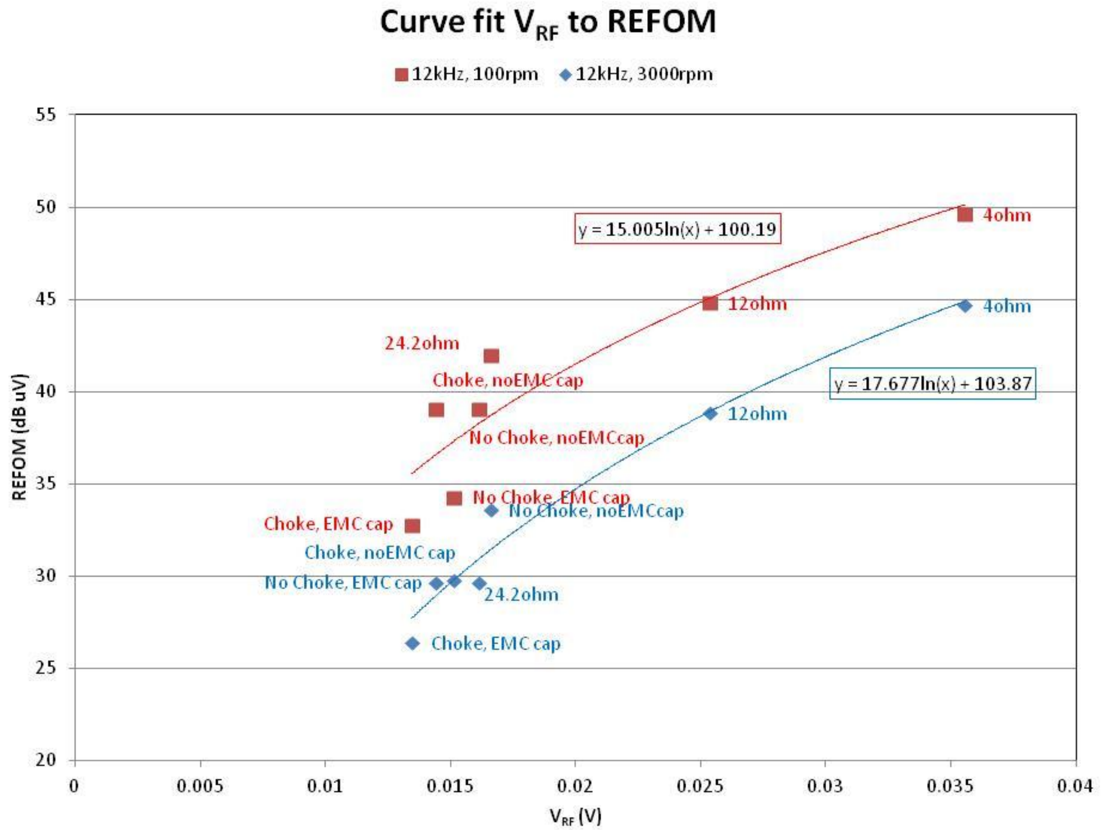


Figure 6-23: DST1405 REFOM versus measured RF content in voltage

6.7 Implementation of Passive Circuits to Increase Efficiency

From studying the voltage transient of the DST1405 VSD with the wavelet transform, it is clear that the low bus bar and module inductance does not create a source for radiated emissions hence there are no peaks at potential points 1 and 2 (wV_{ce_1} and wV_{ce_2}). Instead, at point 3 as the diode begins to block voltage and at point 4 as the voltage approaches saturation are the dominant sources of the emissions. Several passive gate drive solutions are implemented in an attempt to reduce the switching loss while maintaining compliance with radiated emissions limits.

6.7.1 Additional C_{ge}

Several gate drive solutions examined in chapter 3 utilised the addition of an external gate emitter capacitance (C_{ge}) in an attempt to reduce the IGBT switching losses. This

operates by shaping the switching transient separating the time constant associated with the collector current rise time from the gate impedance seen as V_{ce} begins to fall. To assess the benefit of this for the DST1405, pulse testing is carried out with various values of C_{ge} added and the results are shown in Figure 6-24.

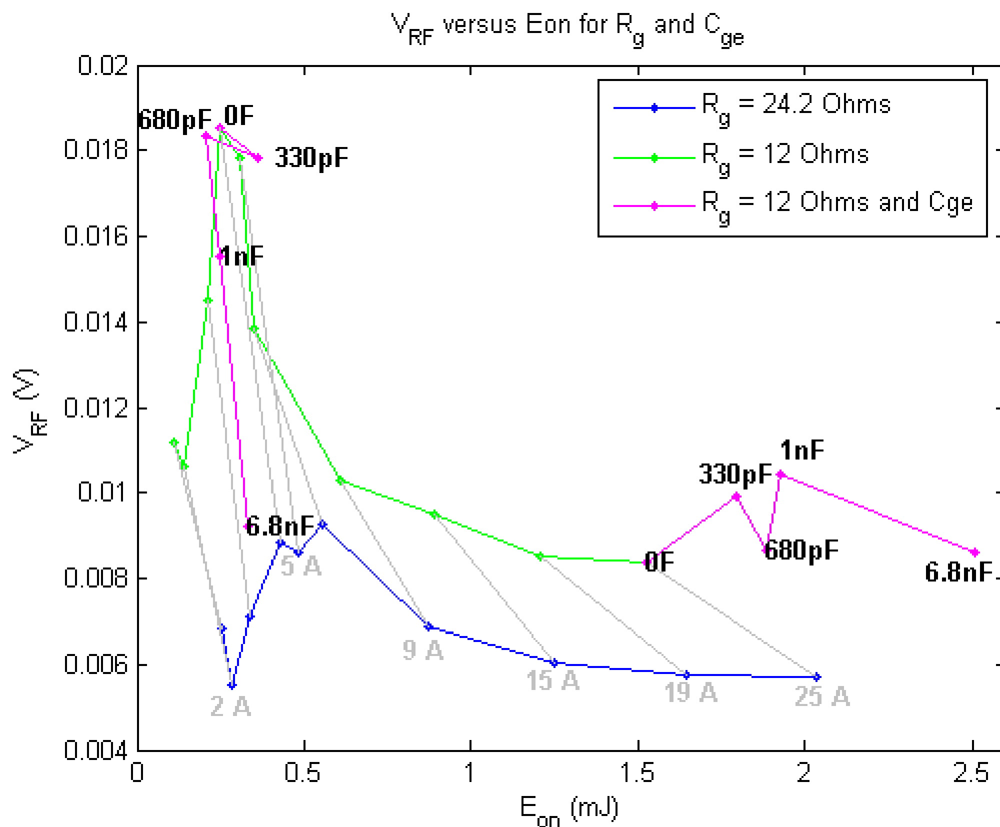


Figure 6-24: Switch on loss versus V_{RF} with external C_{ge}

The loss for a 24.2 Ω fixed resistor is measured at different output currents and is shown in blue. The loss is reduced by using the 12 Ω resistor, however V_{RF} increases as shown previously. The pale grey lines interpolate between the results indicating how the points may change for intermediated values of fixed resistance. Two load current points have been assessed for the addition of C_{ge}, 5 A and 25 A. At 5 A, small values of capacitance offer little benefit to either the loss or emissions, however as the capacitance is increased to 680 pF, there is a 19 % reduction in switching energy with no change in V_{RF}. As the capacitance is increased further to 6.8 nF, the losses have been reduced by 22 % compared to the 24.2 Ω measurement with a comparable V_{RF}. This is a very

desirable solution at reducing the radiated emissions as discussed in literature presented in chapter 3.

While the reduction in switching loss is desirable, it must be considered over the entire operating range of the IGBT. When operating with an output current of 25 A (highest loss in the diagram) the addition of a capacitance does not reduce V_{RF} however it has increased the switching loss by 23 % (Figure 6-24). The benefits in loss reduction at low currents are not sufficient to offset increases in losses at high currents.

Further attempts to shape the switching transient using passive devices resulted in a similar performance where each output current level could be optimised however changes due to temperature such as a shift in threshold voltage or load current reduced the performance. As an example of this, a capacitor is placed in parallel with the gate resistor to increase dI_c/dt as illustrated in Figure 6-25.

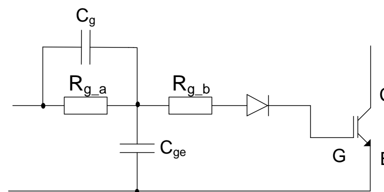


Figure 6-25: Passive gate drive, parallel capacitor

The series combination of the capacitors creates a potential divider which rapidly brings the gate voltage up to the Miller voltage for the designed output current. As the collector current is related to the gate voltage above the threshold by the transconductance, the collector current also rises rapidly reducing the switching losses in this period. The gate resistor then limited the gate current during the Miller region controlling the voltage transient. By careful adjustment of the ratio of capacitance values, the peak emissions located at point 4 (voltage approaching $V_{ce(sat)}$) can be independently reduced however this is very sensitive to load current due to the changing Miller voltage.

6.8 Switched Impedance

The method presented in this thesis to measure and quantify the RF content in voltage switching signals illustrates interesting properties and opportunities for reduction of

switching loss while maintaining compliance with radiated emissions. In Figure 6-16 the reduction in emissions with output current has been identified while also illustrating that lower loss, albeit with higher emissions can be achieved using a lower gate resistance. Figure 6-24 progresses this further showing how the gate impedance as a whole can be considered to control the balance of low switching loss with compliance with RE. To take advantage of this curve shape with an adaptable gate drive with selectable gate impedance could be used as illustrated in Figure 6-26.

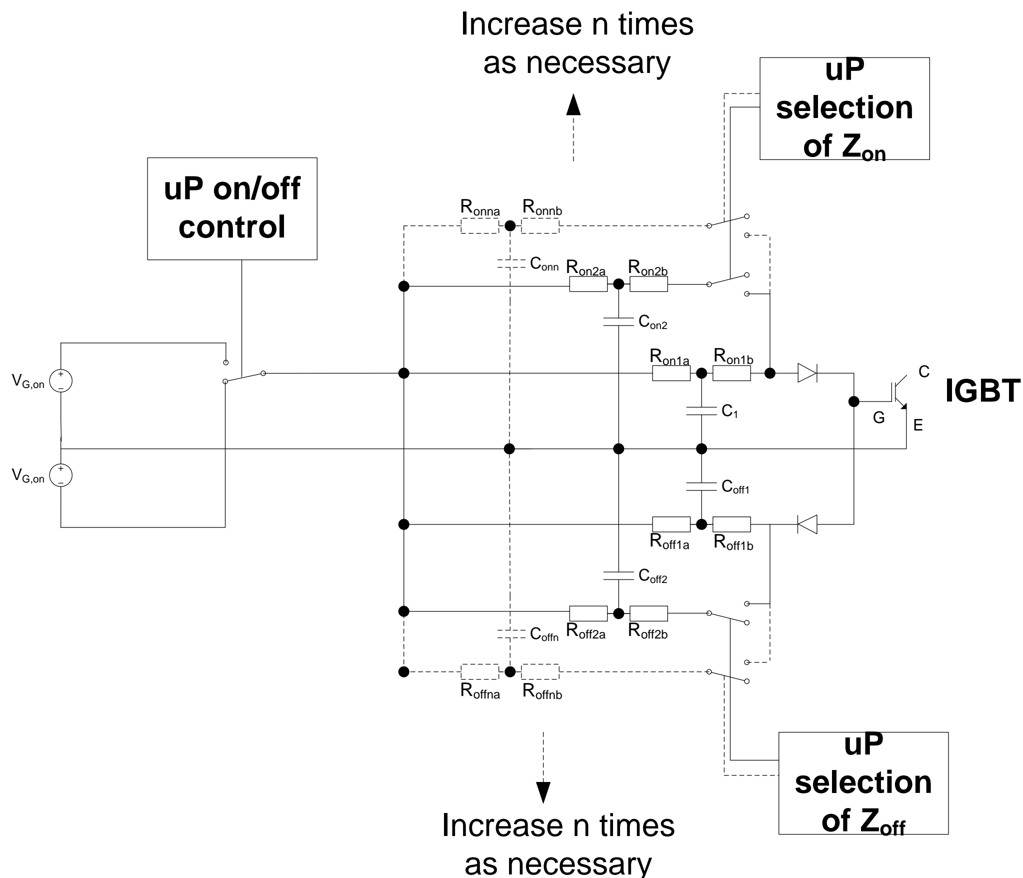


Figure 6-26: Selectable Gate impedance

During VSD operation, the decision of which impedance to select can be determined from the output current which can either be measured within the gate drive through various parameters of the IGBT such as $V_{ce(sat)}$ or Miller voltage or measured externally and fed through an opto-isolator to preserve galvanic isolation. The decisions can be made on a cycle by cycle basis hence operating at the output switching frequency. The

number of gate impedance choices is application specific where a high number can be used to optimise performance of the entire switching profile.

6.9 Simple control of wV_{ce_1} with threshold hold circuit

As presented in this thesis, the first peak source of radiated emissions (wV_{ce_1}) occurs as the load current begins to increase and is related to the stray inductance in the bus bar loop. In an effort to reduce the peak value of this, it is possible to utilise the stray inductance in the gate circuit loop.

When applying a step input demand to turn on an IGBT using a fixed gate resistor, the rate of change of V_{ge} is initially limited by the gate loop inductance. As the voltage trajectory increases towards the threshold voltage (V_T), the rate of change in voltage further increases. Under these conditions, the rapid change in V_{ge} beyond the threshold voltage demands a correspondingly rapid increase in I_c linked via the transconductance. However, if the gate voltage is initially held to a constant level just below the threshold, before increasing with the step demand, the inductance in the gate loop slows the V_{ge} trajectory causing a corresponding reduction in the initial collector current trajectory.

A simple threshold circuit is constructed as shown in Figure 6-27. A demand signal is applied to the gate drive from the microprocessor. The gate voltage is rapidly increased to a voltage just below the device threshold, held for a defined time, and then continues towards the on voltage.

Figure 6-27: Gate Threshold – Hold Circuit

Measurements of the voltage and current transients are shown in Figure 6-28 for three different plateau voltages. Figure 6-28a shows how V_{ge} is increased from the normally off -6 V up to either 3.12 V, 4.75 V or 7.12 V then held for approximately 100 ns. In the third case (red), 7.12 V is too close to the threshold voltage and collector current begins to flow. The small reduction in V_{ce} allows V_{ge} to continue to rise further due to the positive feedback loop. This condition is unstable and increases the time taken for turn on, increasing the switching losses. For the two cases with the lower voltages, a small change in the current transient is visible in Figure 6-28b with corresponding change in voltage trajectory shown in Figure 6-28c. The significant difference is visible in both wV_{ce_1} and wV_{ce_2} where the peak wavelet values have reduced by up to 15 %.

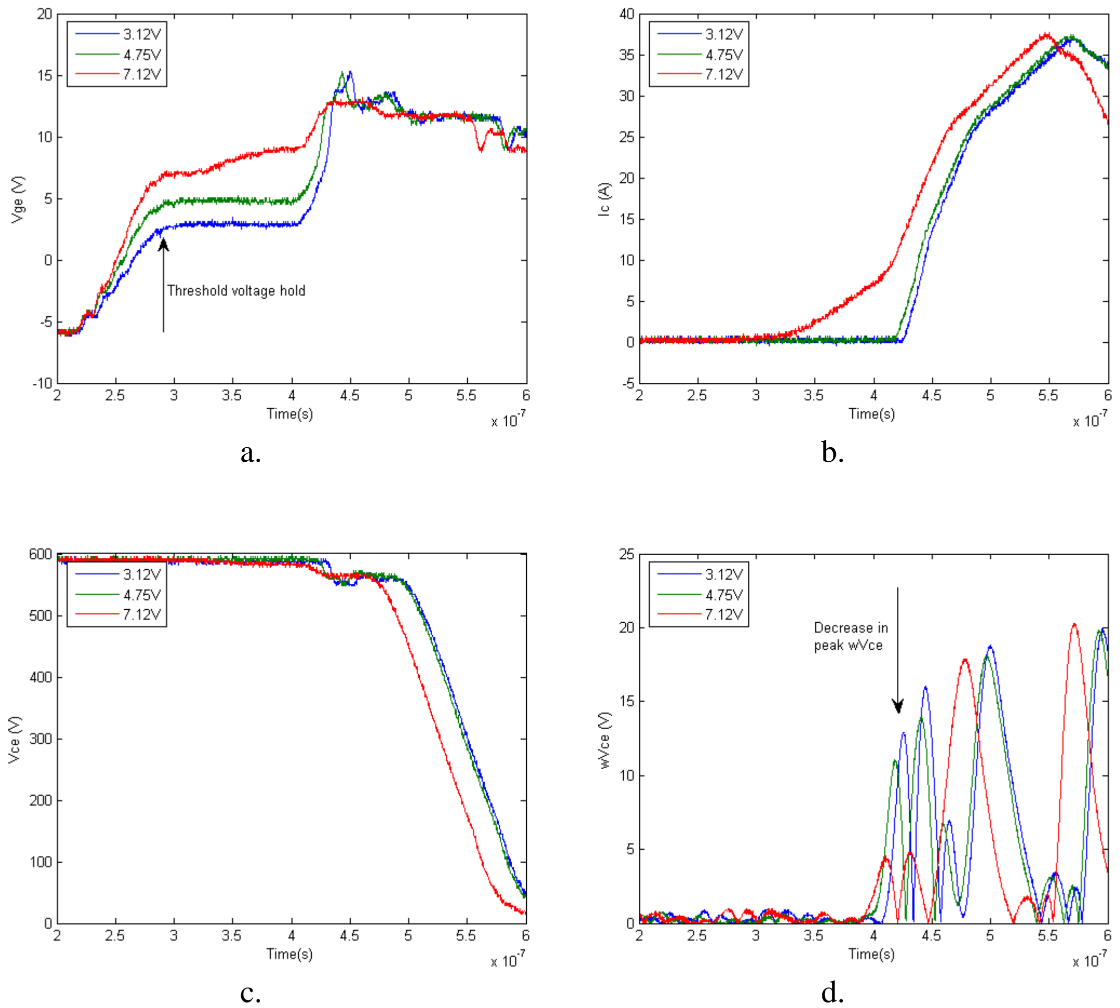


Figure 6-28: Threshold hold transient waveforms a) V_{ge}, b) I_c, c)V_{ce}, d)wV_{ce}.

This circuit works well at controlling the peak emissions at a specific operating point while preserving the low sensitivity to noise from the negative gate voltage. The IGBT threshold can change by up to 2.5 V with changing temperature so the defined operation level must take this into consideration to reduce the emissions across all operating conditions.

6.10 Summary of Chapter 6

The radiated emissions from a commercially available servo drive have been considered in this chapter. The VSD system including cable and motor are very complex when considered at radio frequencies. The unmatched impedances of the cable contribute to current reflections and changing impedance depending on modulation strategy and output vector add to the list of variables which contribute to the measured emissions.

The VSD must comply with the radiated emissions limits under all operating conditions so performance with motor rotation speed and switching frequency must be considered.

It is found that the radiated emissions change with the load current when operating with a fixed gate resistor value and the location in the switching transient of the peak emissions has been shown and related to the semiconductor device physics.

The method of measuring the RF content of the voltage signals, presented in chapter 5, has been used with the VSD and found to show good correlation over a range of gate resistors and filter components. The addition of a capacitor between negative dc bus and ground connection has given a reduction in broadband emissions which has further been improved with the use of a ferrite.

Passive methods of controlling the gate transient presented in literature in chapter 3 have been examined and found to offer improvements at specific operating points however these may have a detrimental effect as the voltage, output current and temperature change throughout operation. A method to select the optimum solution has been presented which can operate at two stage for low or high currents or can be expanded in complexity to increase the number of stages further optimising the gate drive. A patent has been applied for this gate drive solution for by Control Techniques.

Chapter 7: Conclusions

7.1 General Overview

The main objective of this work, to determine the source of radiated emissions from a VSD, is addressed in this thesis. The complex interaction between the IGBT and diode in the output leg has been described using semiconductor physics and methods to control the switching trajectory researched. It is possible to define a gate emitter voltage trajectory to optimise the dissipated switching energy while complying with the radiated emissions limits as defined in the standards, however this must be optimised for varying load current, voltage and temperature. Optimisation of the switching trajectory gives a significant reduction in switching loss in comparison to the state of the art method of a fixed gate impedance.

7.2 Frequency Analysis

It was previously known that the radiated emissions from a VSD can only be detected when the output is switching. This led to research into the switching transients as the source of the radio frequency noise considered in the time domain. A 120 kHz band pass filter as used by the receiver does not give adequate resolution in the time domain to identify features responsible for radio frequency content. Analysis of the pulsed signals using a Fourier Transform also masks the time location of the frequency content of the signals, however, the use of the wavelet transform offers a compromise between a narrow time window and narrow frequency bandwidth. With typical voltage and current rise times of 100 ns, the frequency content of interest (>30 MHz) is found to occur in the finer details of the switching transient and is not necessarily related to the rise time of the entire transient.

7.3 Transient waveform shape

Using this knowledge, shaping of the transient trajectory can be used to attenuate the radio frequencies while maintain similar loss values. However, there is a limitation to how far this concept can be taken as the transient rise times are reduced. It is confirmed by measurements of radiated emissions that the measured rise time of the transient voltage in a commercial VSD lies between the theoretical case of the ideal trapezoid and the optimised case for the s-ramp where the first derivative is continuous. From these

pulsed signals, it is clear that it is not necessary to observe ringing in the transient signals for radiated emissions to occur.

7.4 Gate Drive Solutions

Many papers have been published describing novel methods to control an IGBT gate drive switching transient to provide an optimised solution for a given application. No published solutions could be found specifically to control radiated emissions in the 30 to 1000 MHz range, however many claimed benefits for EMC without specific descriptions. A selection of the most promising for transient control is presented for di/dt and dv/dt. However, measurements presented here from pulse testing of an IGBT show that the intrinsic time delays within the IGBT are large, preventing the use of feedback for control of radiated emissions. A feed-forward solution is the most flexible control method for this research programme. A high bandwidth feed forward gate drive was designed and built as a research tool to give fine control over the IGBT switching transients by generating custom gate emitter voltage profiles.

Four transient signal sources were measured under control of the gate drive to assess their impact on radiated emissions. The RF content in the gate drive circuit can emit measurable radio frequency radiation particularly from poorly designed, large loop areas. From an understanding of the device physics, the collector current trajectory can be controlled independently from the voltage transient. By utilising this control method, it is possible to create a wide range of test profiles to determine the linkage to the measured radiated emissions. This gate drive is prohibitively large and expensive to be used in a commercial product, however the high specification is necessary for the research exercise presented in this thesis.

7.5 Measuring RF Content in Electrical Signals

Measuring the RF content in a high voltage signal is complicated by the limited vertical resolution of available oscilloscopes. The use of wavelet analysis on the measured transient identifies the position in time of the peak emissions sources, however there is a degree of uncertainty around the result due to insufficient attenuation of lower (<30 MHz) and higher (>100 MHz) frequencies. The use of a physical, sixth order, high pass

filter sufficiently attenuates the low frequency content to bring the higher frequency components within the dynamic range of the oscilloscope.

The connection of probes to the VSD system can lead to waveform distortion due to the insertion impedance which becomes critical at radio frequencies. The VSD construction and impedance to ground are critical to achieve suitable radiated emissions performance and as such, measurements taken of the voltage transient must include all physical components of the drive system which will be used for radiated emissions testing.

7.6 Dominant Source of Radiated Emissions

The broadband radiated emissions from a VSD are seen to occur up to 100 MHz. A method to capture this detail when measured using a 120 kHz bandwidth receiver has been presented and referred to as the radiated emissions figure of merit (REFOM). Measured resonance effects which cause crests and troughs in the spectrum caused by the physical structures such as the cables can be minimised by the REFOM while giving a good representation of the generated spectrum from the IGBT. A strong correlation is found between the frequency content in the collector emitter voltage and the REFOM. Using the average output from the filter for the physical setup used throughout this testing, an error of ± 1 dB was found when predicting the REFOM. While no correlation could be found for the RF content in the collector current, it has been shown from both semiconductor theory and measurements that the transient voltage depends heavily on the collector current transient therefore requiring careful control of the entire switching transient. The measured radiated emissions change with temperature due to changes in the switching trajectory resulting from the silicon characteristics. Measurements using the passive filter over a temperature range are required to determine the worst case operating condition.

7.7 Radiated Emissions from a Commercial VSD

A VSD is a complex system when considered at radio frequencies. The physical structures required to support the components, provide cooling and safety separation can contain many parasitic antennas. The linkages found between RF content in the output phase voltage to ground show a strong correlation to the measured REFOM. From

measurements of this voltage from a VSD which is compliant to international standards, a limit can be determined which can be used for product design purposes.

Control of radiated emission from a VSD is a difficult task given the wide range of operating conditions: ripple on the supply voltages; sinusoidal output currents; and fluctuating temperatures. By examining the features of the switching transient using the wavelet transform, the individual features responsible for radiated emission can be identified and corrective action taken by control of the gate drive. For a fixed resistor gate drive, operation at low currents (below ten percent) is found to give higher emissions than operation at higher load currents.

A possible solution to achieve an optimised performance is presented where the desired gate impedance can be selected depending on the operating conditions. Such a solution can provide minimal additional switching loss for the compliance with radiated emission limits.

7.8 Benefits of the reduction in RE

Radiated emissions standards have a pass / fail limit line which must be adhered to for compliance. There is no advantage gained by further reducing signals significantly below this limit. However, improvements in the trade off between dissipated switching loss versus radiated emissions potentially offer significant environmental and commercial advantages.

A large percentage of the volume and weight of a VSD consists of the cooling system – heat sink and fans. By improving the efficiency of the IGBT switching transient, the energy which must be dispersed by the cooling system to maintain components within their safe operating area is reduced leading to smaller, lighter and cheaper VSDs. The weight of the VSD is rarely a consideration for industrial installations however initial transportation costs can be significant for large, heavy systems.

An increase in operating switching frequency allows faster current control loops to operate before reaching the limits of the VSD cooling systems. This can result in better control performance of equipment and plant creating better products with less waste.

7.9 New Technology Devices

With customer demands for higher efficiency products, device manufacturers are engaged in considerable efforts to reduce both switching and conduction losses. New unipolar devices made from wide band gap materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN), can be operated at higher voltages with lower conduction losses [21, 22, 120, 121]. Using the unipolar devices removes the need to create electron/hole plasma during switching. As a result, these devices are capable of switching with lower losses and with higher transient speeds. As illustrated in chapter 2, the attenuation of high frequency components in a switching signal is possible by curve shaping, however, the benefits of this reduce as the rise time reduces. It also becomes increasingly difficult to implement any curve shaping techniques as the rise times are reduced to a few nanoseconds.

With the reduction in costs of wide band gap devices, the radiated emissions will again become a significant design issue due to voltage transition times approaching 5-10 ns. Operation in this area with 600V supply voltages will not allow control of radiated emissions by curve shaping. The slowing of the transients to comply with international standards removes the potential gain of the technology to save switching energy. Output filters will be required for such products to maintain compliance to radiated emissions standards however, operation with very high switching frequencies can lead to efficient output filter designs removing the PWM transients from the cables.

7.10 Recommendations for Further work

The research presented here has focused on the capability to balance radiated emissions with switching energy loss utilising the IGBT gate drive. This method has potential benefits for the current generation of Si devices however as discussed above, further techniques are required to fully utilise new material devices. Some areas where further work is required to implement this are:

1. Asymmetric bus bar inductance:
   The influence of the bus bar impedance on switching loss has been discussed in this thesis. Increasing the inductance at turn on helps to lower losses while increasing the inductance at turn off can increase losses and increase the

potentially damaging voltage overshoot. New materials are being researched which have a property of asymmetric magnetic hysteresis. If these can be adapted for use at high powers to control the inductance based on the current direction, there is a large potential for energy saving in all hard switched converters [122].

2. Combined Input / Output filter:
   It has been presented here that the impedance to ground is important for radiated emissions. This is due to the RF content in the phase conductors being capacitively coupled to ground in the cable and motor. These currents flowing in the ground must find a return path back to the DC bus. By using output filters designed to contain the RF content away from the ground, and within the VSD, the need for screened cable and associated radiated emission problems would be removed.

3. Better cable design:
   The capacitance of the motor cable has been shown to be significant for radiated emissions by the presence of two distinct signatures depending on the VSD output vector. Improved cable design with reduced capacitance to ground while maintaining good performance shield to avoid cross coupling could increase the allowable RF generation limit as discussed here.

APPENDIX A: 4 GHz Gate Drive Design

A.1 Scope

To achieve precision control over the IGBT gate voltage transient, suitable for measurements of radiated emissions, a feed forward gate drive was designed and constructed. This section presents the specification, schematics and PCB design required to implement the gate drive.

A.2 Specification and key components

Feature	Specification
Timing	The output voltage should be capable of changing every 250 ps (4 GHz)
Input Supply	Single 24 V supply
Gate Output Characteristics	Minimum positive output voltage:+15 V Minimum negative output voltage : -5 V Output resolution: 12 bit Peak current 5 A for 200 ns repeating every 50 µs
Dimensions	The outline dimension of a single drive board is not critical. However short connections to the IGBT are essential Board outline: 176 x 150 mm
I/O Specification	11 User programmable IO pins 8 DIP switches to assist with evaluation Bank of 8 LEDs to assist with evaluation LED indication for "FPGA Programmed" FPGA programming port Manual Reset button Two Push button inputs 16 bit ADC for current feedback (5 V operation) Isolated input for connection to drive. CMR = 3000 V\µs Isolation voltage = 600 VDC
DAC	To achieve the high speed output, a 4 GHz digital to analogue (DAC) is required. The most suitable part is the MAX5881 which giving 12-bit resolution, max of 4.3 GHz output clocking frequency. Four, 12 bit, parallel port inputs clocking at 1Gb/s (DDR).

FPGA	The FPGA needs to be suitable to store a large memory for a 10 μs output profile (1.92 Mb) and clock out the memory at 1 Gb/s on 4 parallel 12 bit ports. Low level timing controllers to define load current during pulse testing. Current loop control for continuous operation. Chosen part: VX6VLX75T-3ff484 from Xilinx
Opamp	Slew rate of the opamp must be a minimum of 200V/μs and operate from a 24 V supply. Chosen part: THS3091 from Texas Instruments
Internal Power Supplies	**5.0 V used for:** Current Feedback circuitry and ADC: Current requirements: 289 mA **3.3 V used for:** DAC Clock synthesizer Current requirements: 670 mA **2.5 V used for:** FPGA , I/O Current feedback ADC Current requirements: 355 mA **1.8 V used for:** DAC Flash memory Current requirements: 15 mA **1.0 V used for:** FPGA Current requirements: 1 A **24 V used for:** Output Voltage Amplifier Output Current Buffer All other Power supplies Current requirement: 420 mA

A.3 Schematic

The schematic was drawn using Altium Designer 6.0 and used to create the netlist for the PCB layout. The schematic version shown, is the latest version including all modifications required to the voltage amplifier found during testing (Figure A-1 to Figure A-10). The modifications required (which differ from the PCB layout) include: a biasing circuit to correct the output voltage; and a termination resistor on the input of the opamp. The bias circuit was constructed on vero board and is visible in the thermal

image (Figure A-15) while the termination resistor was mounted directly on the pins of the opamp.

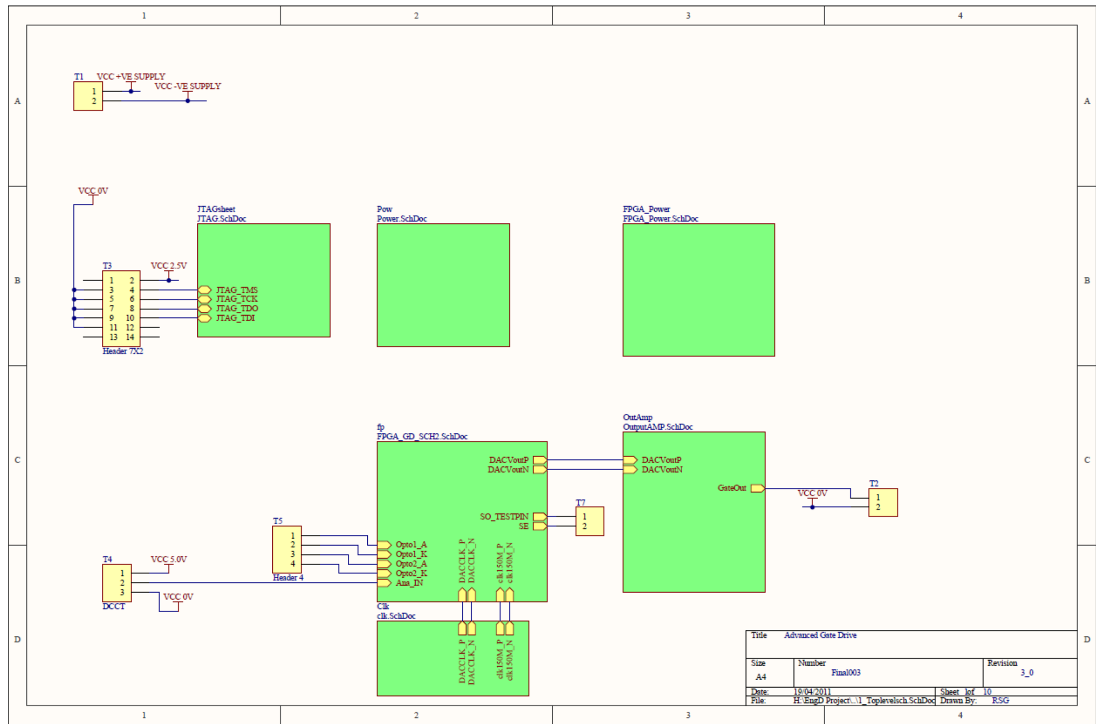


Figure A-1: Schematic Page 1

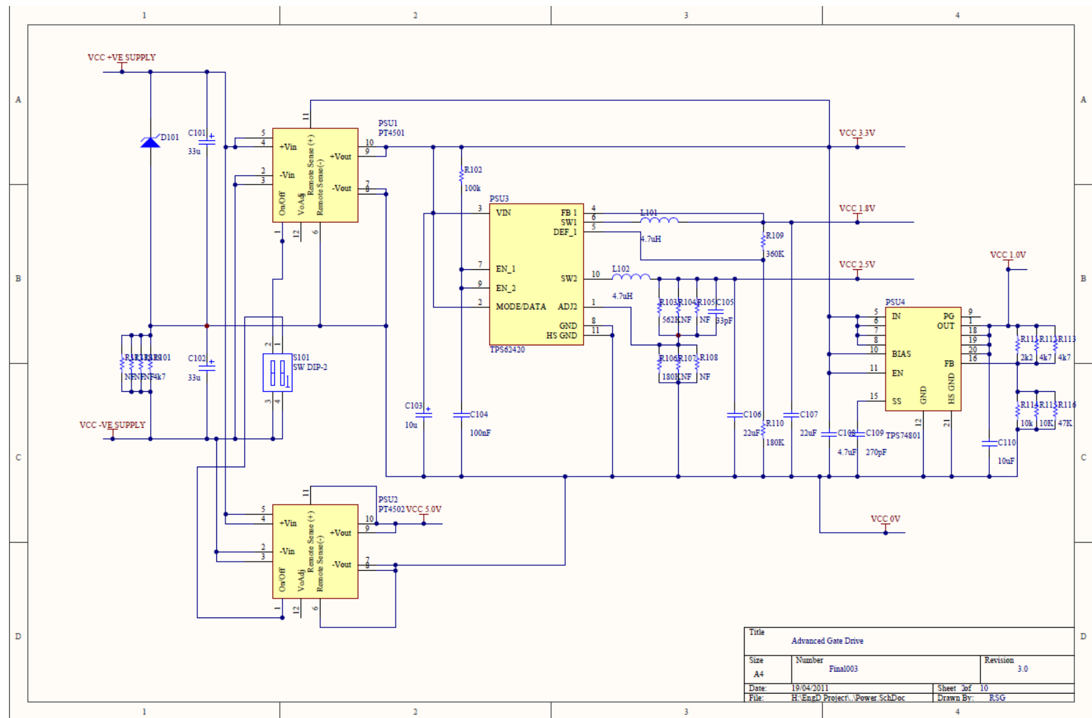


Figure A-2: Schematic Page 2

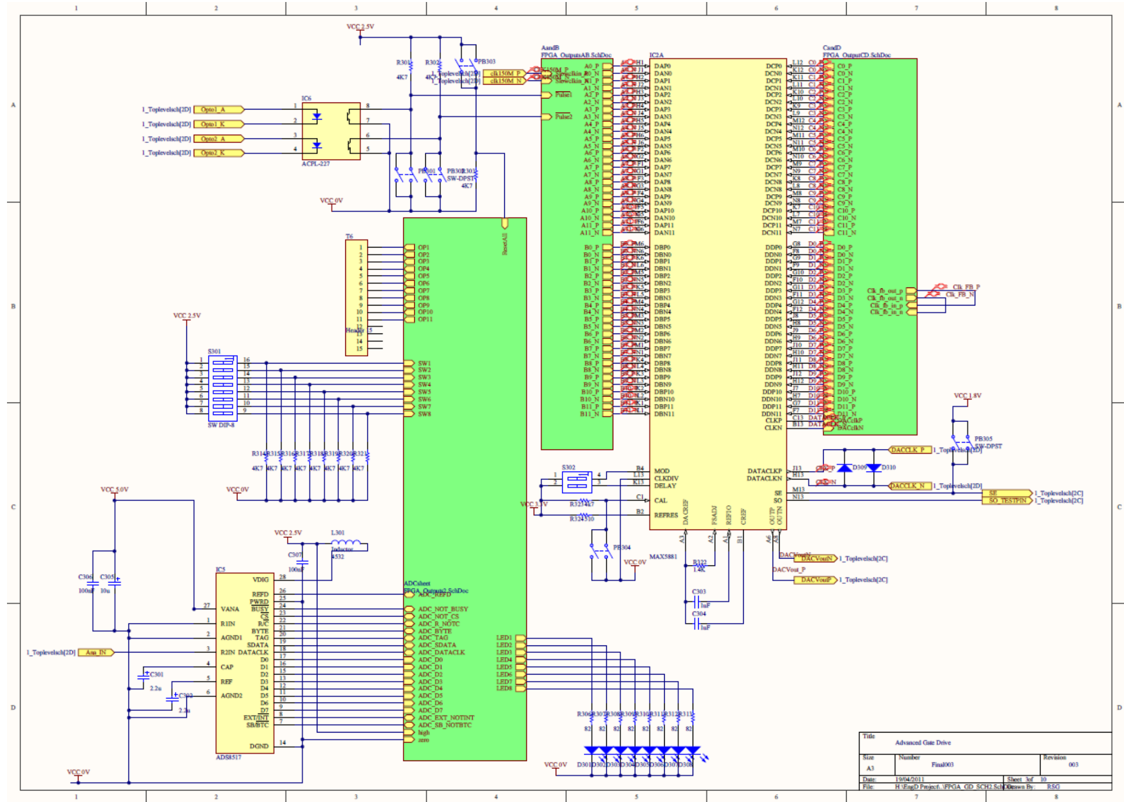


Figure A-3: Schematic Page 3

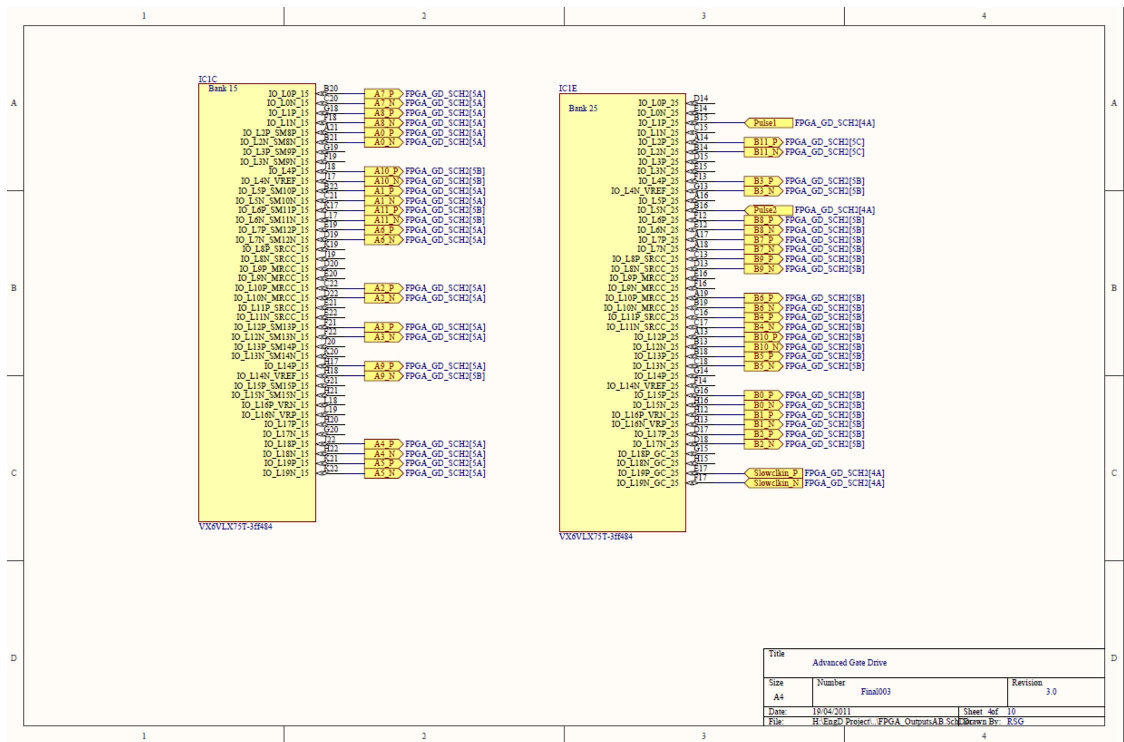


Figure A-4: Schematic Page 4

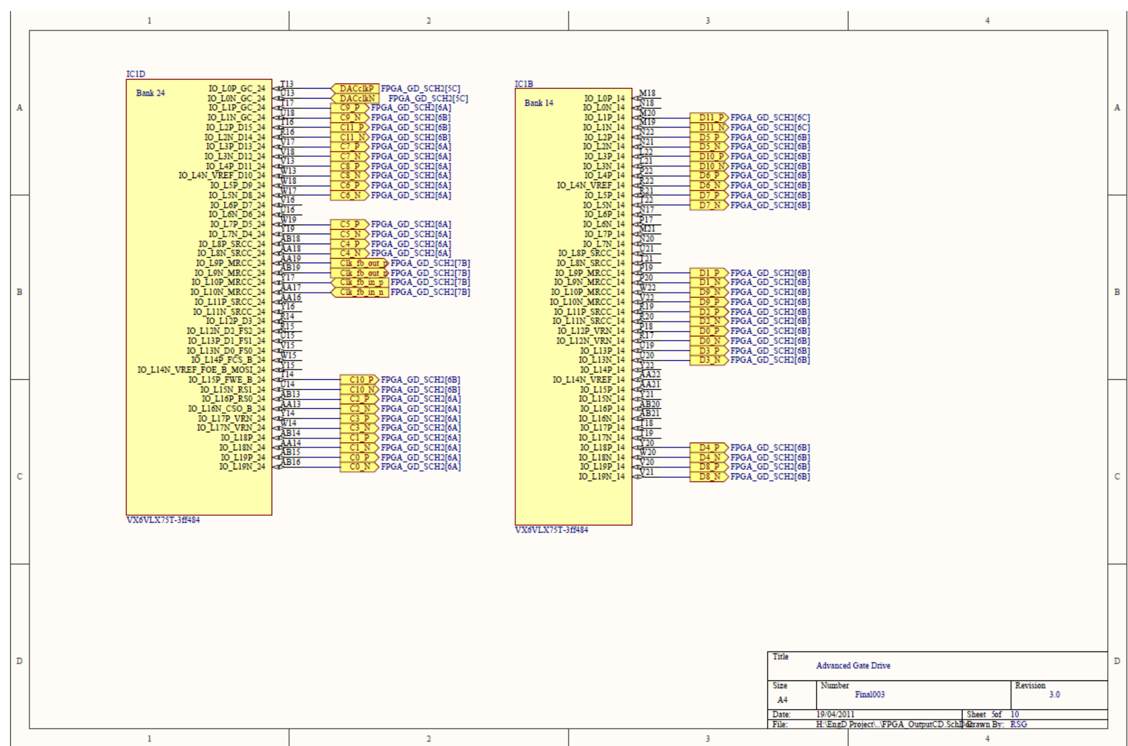


Figure A-5: Schematic Page 5

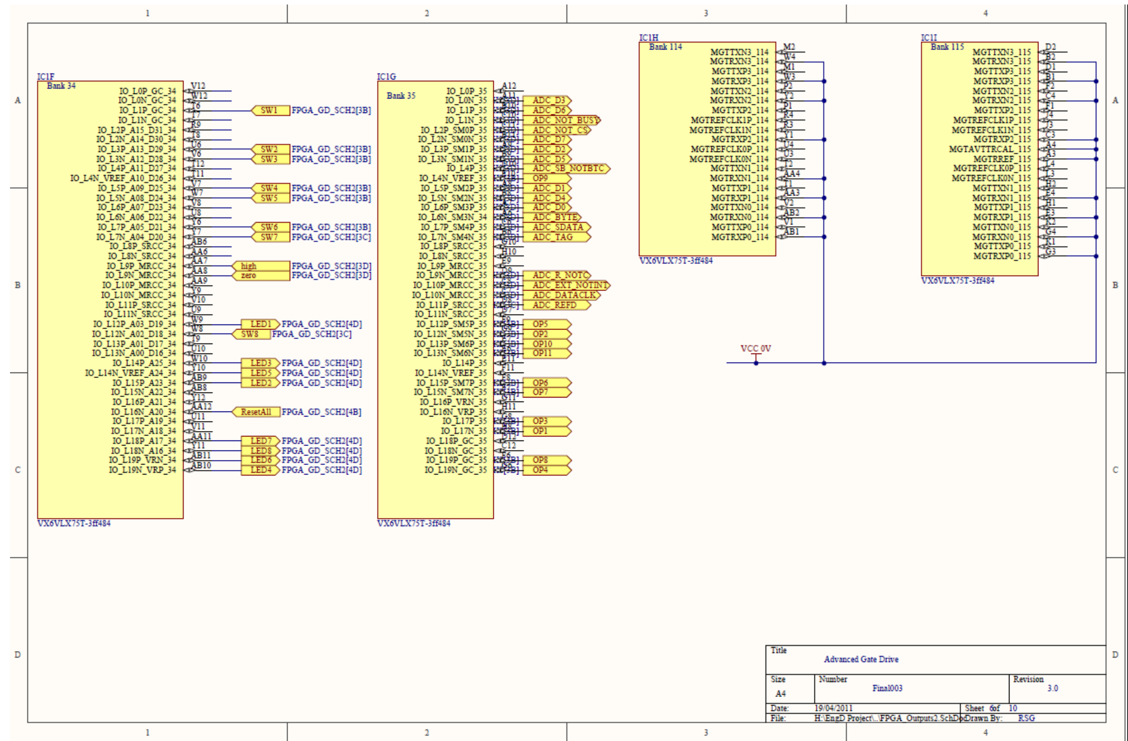


Figure A-6: Schematic Page 6

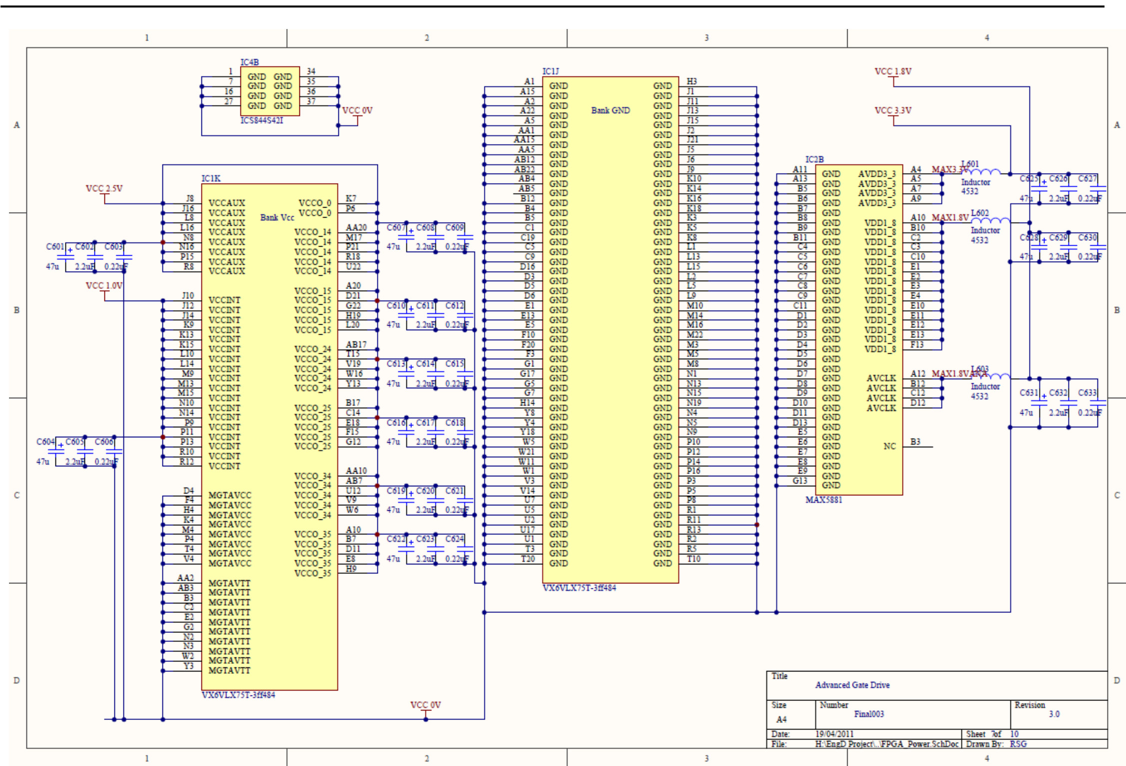


Figure A-7: Schematic Page 7

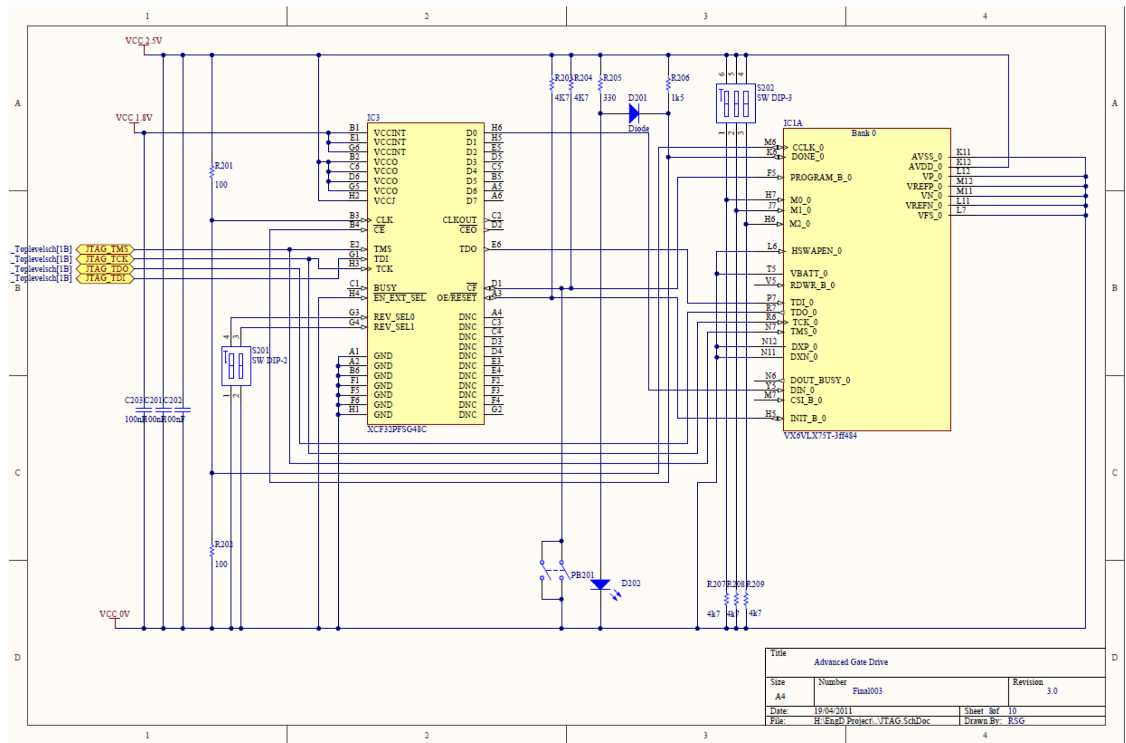


Figure A-8: Schematic Page 8

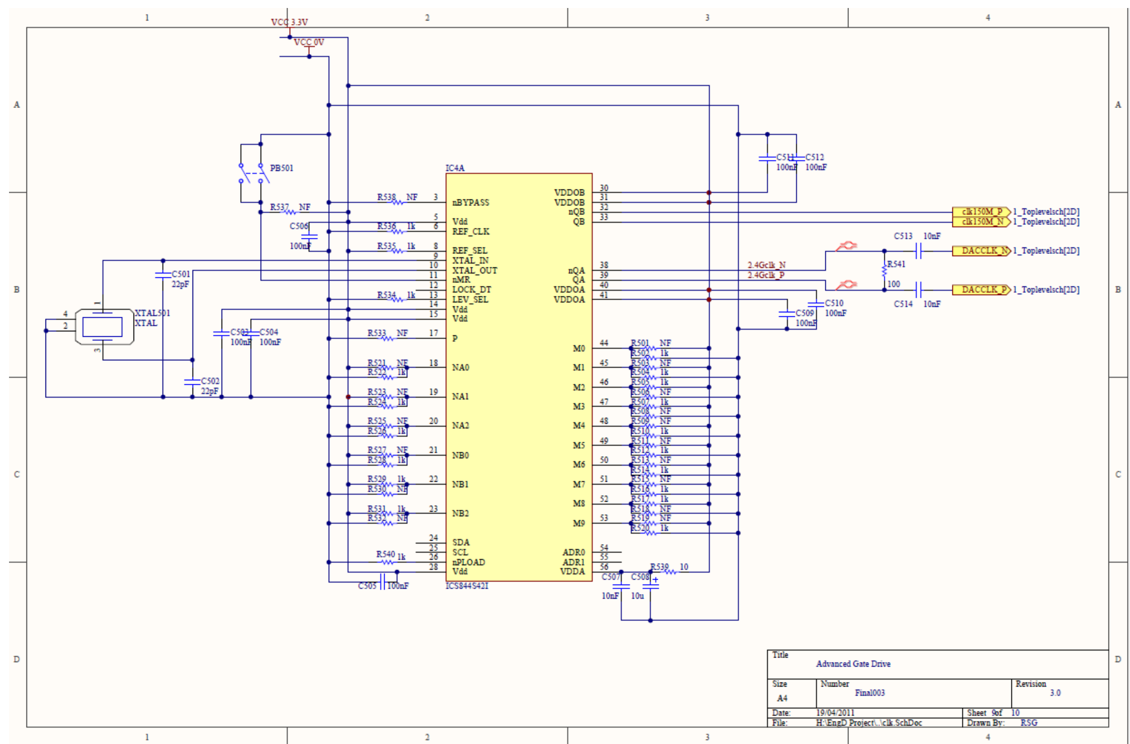


Figure A-9: Schematic Page 9

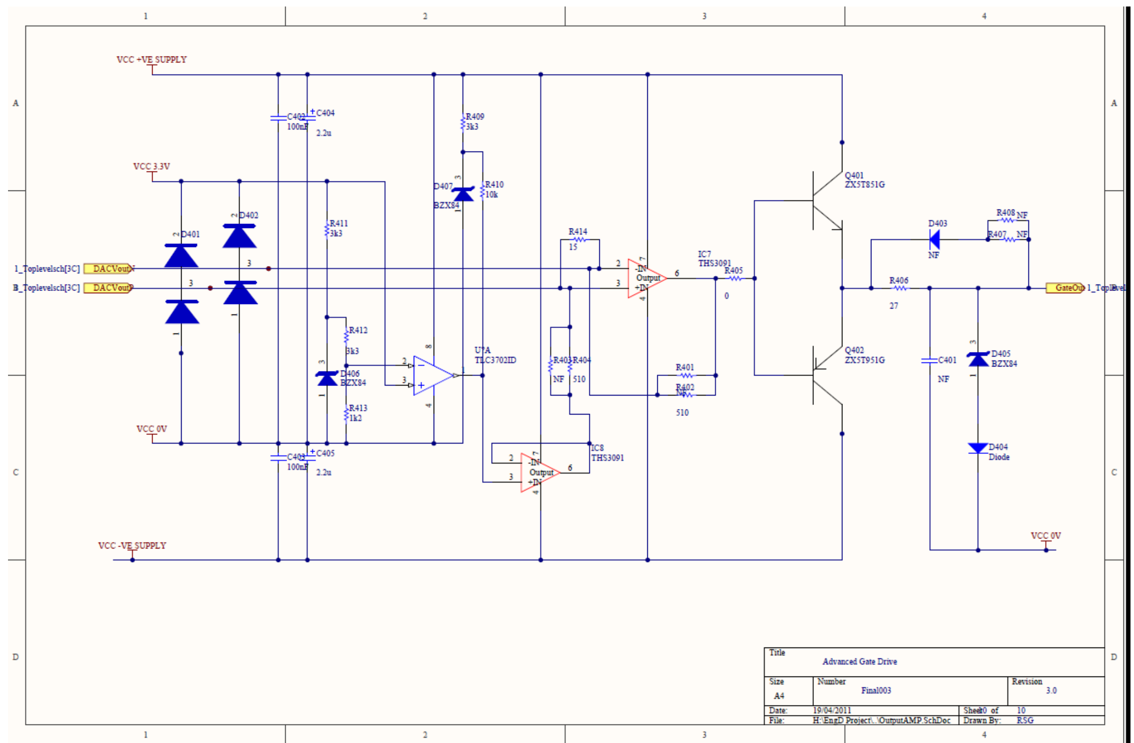


Figure A-10: Schematic Page 10

A.4 PCB

Due to the high signal speed, and compact pin out of the FPGA and DAC BGA packages, the PCB design requires careful consideration to ensure good signal integrity. In particular, routing the 48 differential, high speed signals from the FPGA to the DAC with the same impedance, transit time and with minimal cross talk is essential. Both the FPGA and DAC have 50 Ω internal termination resistors which reduces the complexity of the design. The signals were laid in two internal layers with a ground plane above and below each. The separation between the differential lines was maintained to give a 100 Ω differential impedance. The length of each pair of traces was controlled by twisting the signal lines around each other as shown in Figure A-11. (The lines which had to travel the shortest distance required the most manipulation to maintain the length without compromising the complex impedance).

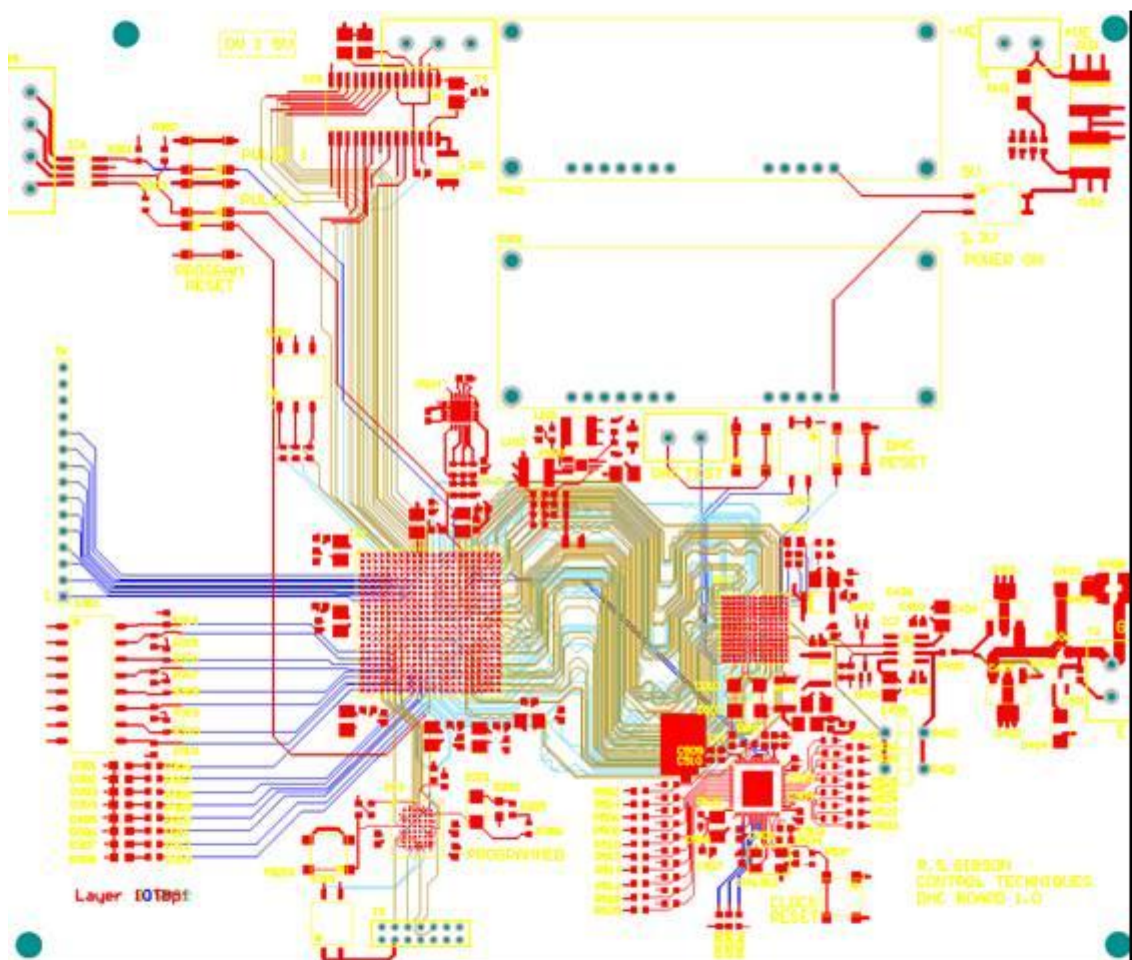


Figure A-11: High Speed signal tracks

Several components required multiple voltage rails, the most appropriate method to maintain signal integrity is to include two power planes. The shape of the power planes determined the overall component placement (see Figure A-12 and Figure A-13). All components are attached to the top of the board and the top and bottom of the board were used for low speed signalling. All vias were through hole which could also be used for functional the completed board. The top and bottom surfaces were finished with immersion gold.

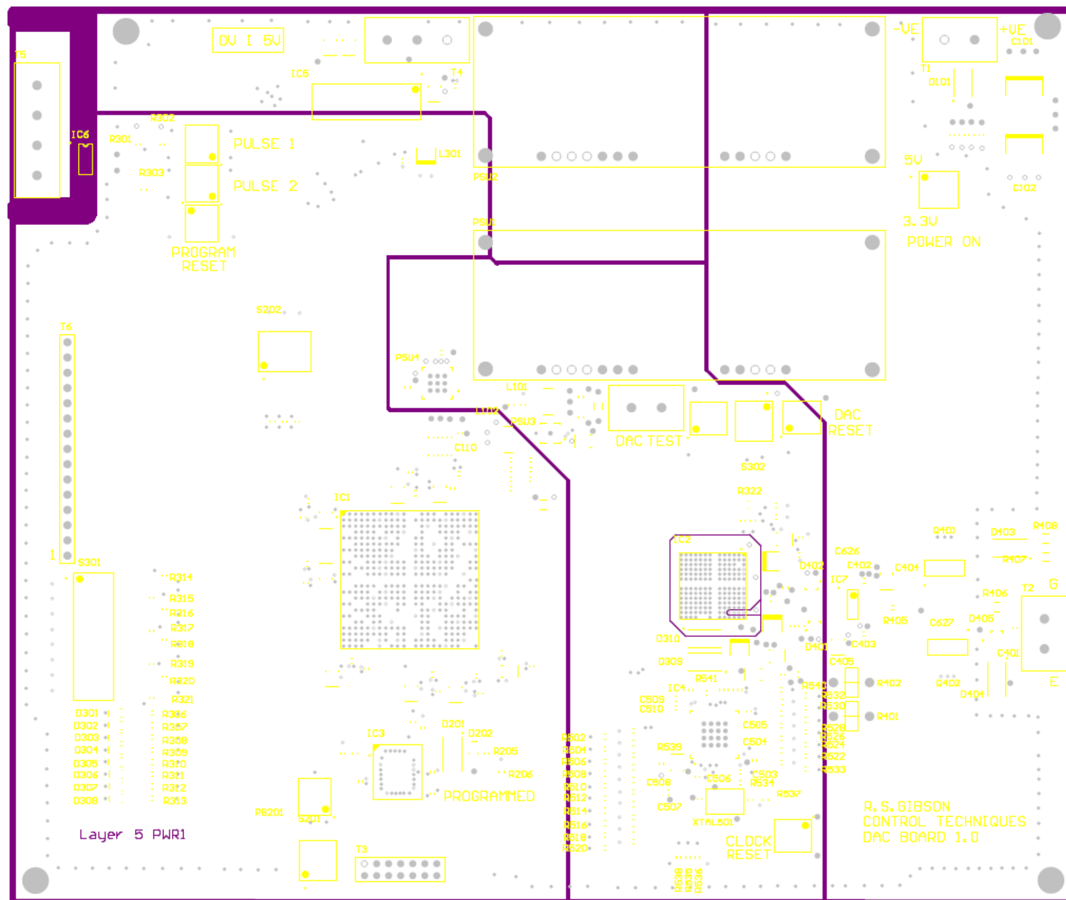


Figure A-12: PCB Power Layer 1

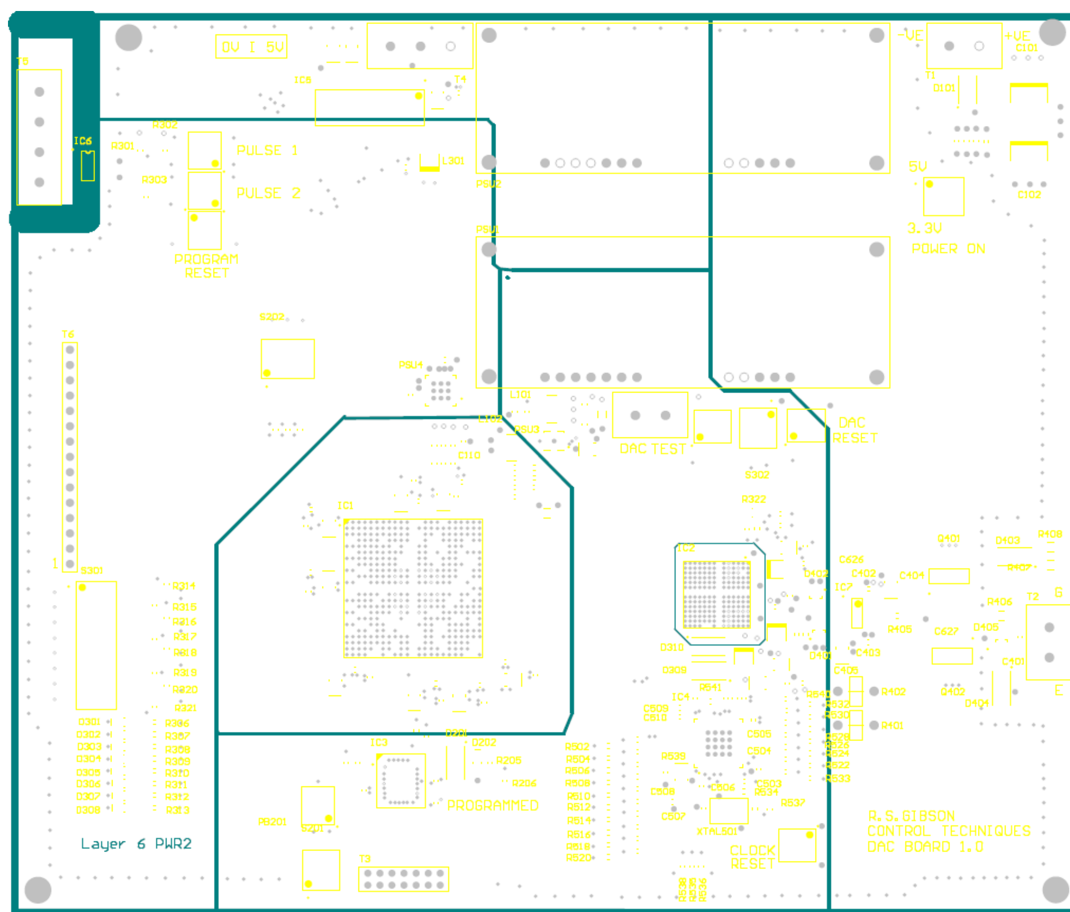


Figure A-13: PCB Power layer 2

A.5 Simulation

The critical design parameter for this PCB was the signal integrity of the high speed data lines. To ensure that the time delays between traces is acceptable, a simulation is carried out using ADS 2009. The PCB Gerber files for the signal layers are imported and converted to EDSarchive files suitable for the momentum EM solver. The mesh fitted is suitable to simulate up to 10 GHz which corresponded to the FPGA signal harmonic content, due to the short rise time. As all signals originate in the FPGA and terminate in the DAC, an IBIS model for the termination was not considered necessary. An ideal 100 Ω resistor was used to terminate the differential pairs.

Due to the complexity, computational memory requirements and time to solve, only three pairs of traces were simulated at a time. Each trace was evaluated for signal propagation time, voltage overshoot and crosstalk by applying a step voltage input to

each pair in turn. A typical result is shown in Figure A-14 where each trace was evaluated. The spacing between traces was designed to give at least -28 dB of cross talk (10 mil spacing). From the simulated result, -37.7 dB has been achieved. The maximum overshoot measured during switching was 7.0% which is within the acceptable range for the DAC of +/- 20%. The mean propagation time for all the traces was found to be 638 ps and difference between the fastest and slowest trace was found to be 24 ps which is suitable for the DAC operation.

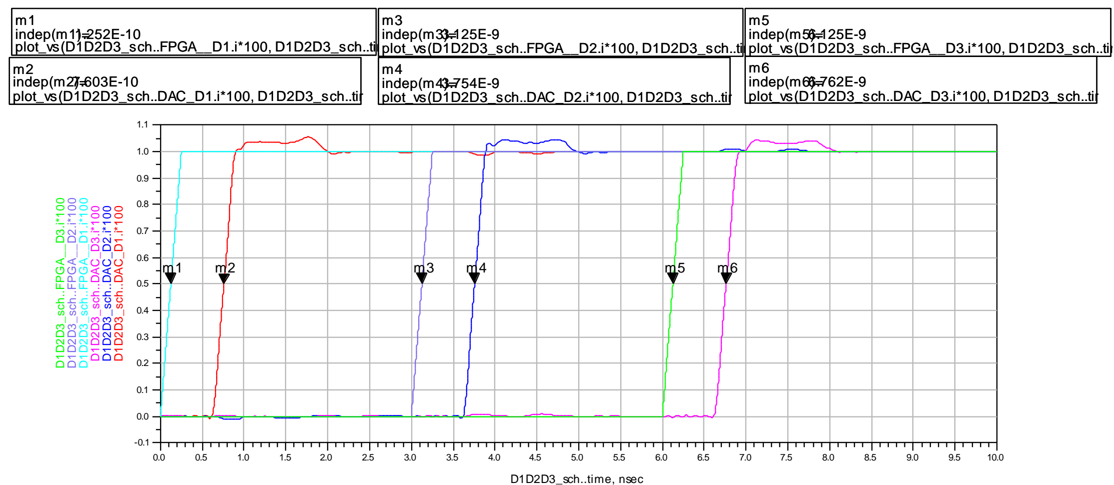


Figure A-14: Delay time and crosstalk for Data line D1, D2 and D3.

A.6 Measurement

After construction, the PCB was functionally tested. All parameters were found to meet or exceed the specification after the modifications described earlier were included. The most significant test to demonstrate the high speed capability of the output amplifiers was a step response measurement. The achieved rise time from the voltage amplifier from -5 V to +15 V is 6 ns corresponding to 3.3 kV/us.

The power drawn from the 24 V supply was measured as 10.25 W which is in line with expectations. To ensure that all components remained within their designed operating range, a thermal image was captured when operated from 24 V, clocking with a 4 GHz output. PSU3 is close to its maximum operating temperature under these conditions however an aluminium heat sink is added as a precaution which is visible in Figure A-15.

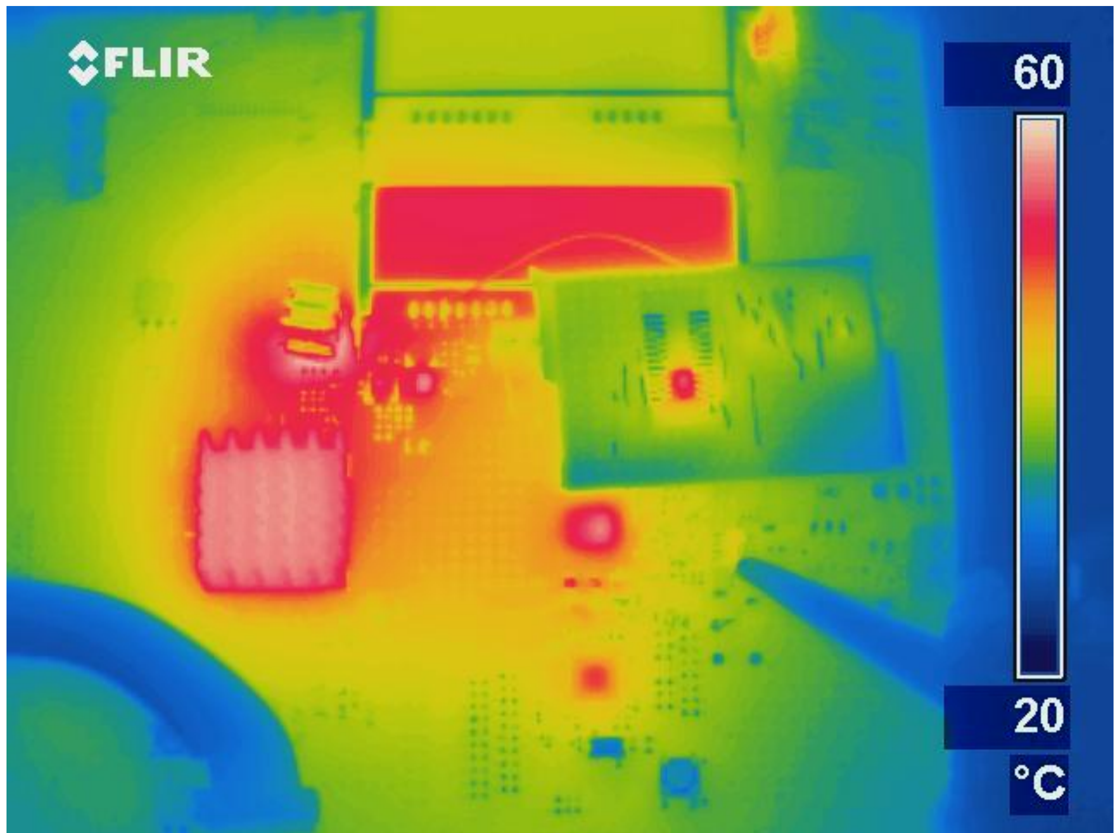


Figure A-15: Thermal image of operation PCB.

A.7 Assembled FPGA Gate Drive

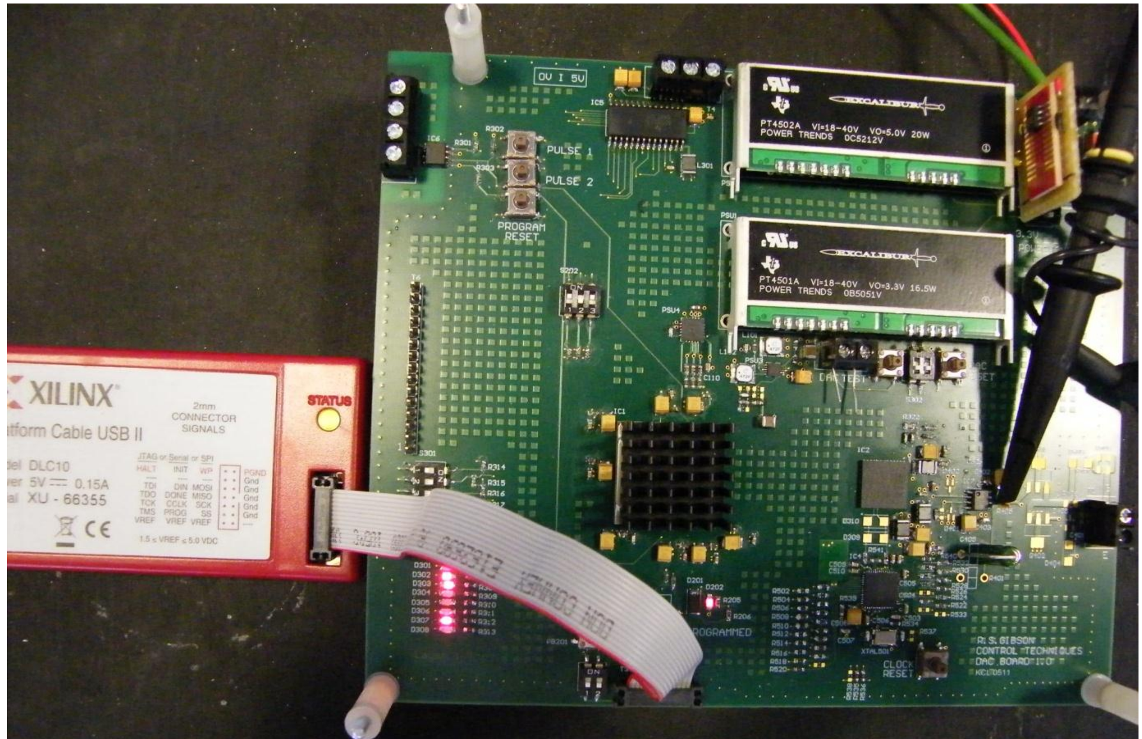


Figure A-16: Photograph of FPGA gate drive with programmer.

Appendix B: Derivation of Minimum Gate Resistor

The gate voltage and current transient is greatly influenced by the chosen gate resistor. A large resistor, increases V_{ge} rise time up to the Miller region due to the $R_g.(C_{ge} + C_{gc})$ time constant. During the Miller region, the gate current is limited by the gate supply voltage and the gate resistance. When using the designed feed-forward gate drive, the gate voltage demand can be rapidly adjusted. By using this control method, the large gate resistance value is no longer needed to control switching timings. However, due to the stray inductance in the gate loop, voltage oscillations can occur with the internal gate capacitance. To avoid this, a minimum value of gate resistance is required to provide damping. Assuming a second order system, a resistance can be calculated to give critically damped operation using equation (B-1). The inductance and capacitance in the loop are measured from a frequency sweep as shown in (see Figure B-1).

For the FP25R12KT4 connected to the FPGA gate drive, the IGBT is connected to the gate terminal using the same short wire links used during pulse testing and radiated emission testing. The gate resistor is replaced with a zero Ohm link. The current buffer transistors are removed and a sinusoidal voltage is swept with increasing frequency. The current is measured at each frequency and the impedance calculated (see Figure B-1). The values of capacitance and inductance are found to be 3.1 nF and 20 nH respectively which gives a minimum gate resistance of 5.08 Ω for critical damping.

$$\varsigma \geq \frac{Rg}{2}\sqrt{\frac{C}{L}} \qquad \text{(B-1)}$$

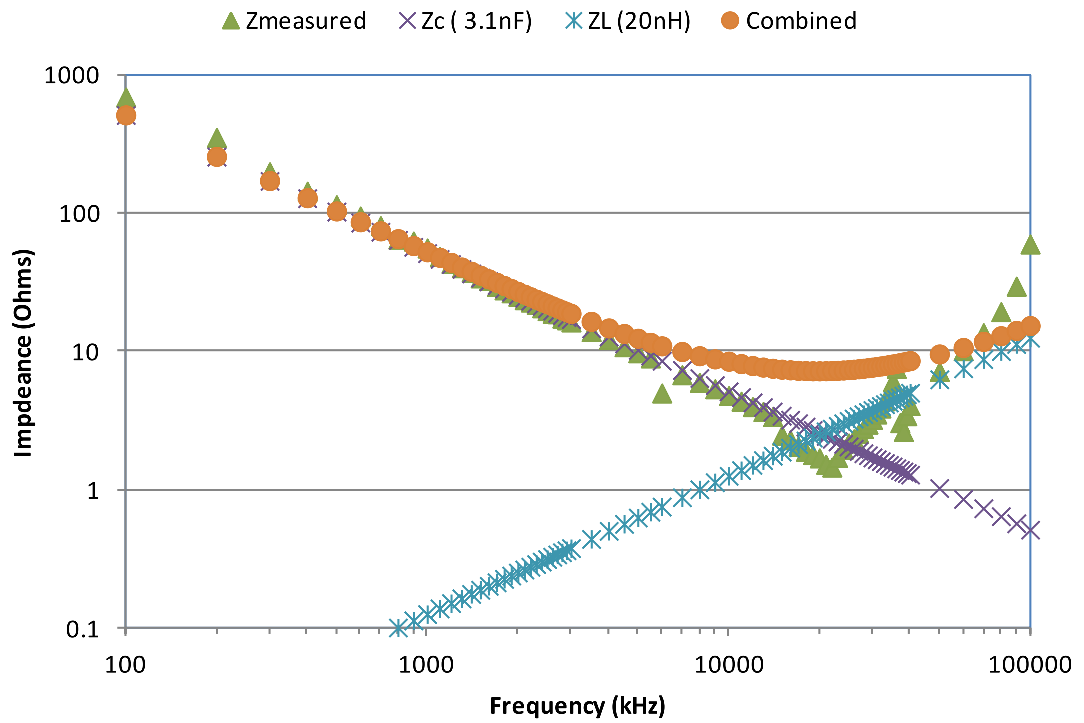


Figure B-1: Curve fitting to estimate gate capacitance and inductance

Appendix C: Reflected Signal Interference in Antenna Measurements

When using an open area test site with a conductive ground plane, there are two signal paths for the radiated signal to travel to the measuring antenna. These are the direct path and the reflected path. The distance of each of these paths differs depending on both the equipment height and the antenna height (see Figure C-1) [123]. The speed of the electromagnetic waves is assumed constant in air, correspondingly the change in path length of the two signals leads to different arrival at the antenna. Figures for the delay in time and phase for a typical OATS are given in Table C-1 and Table C-2.

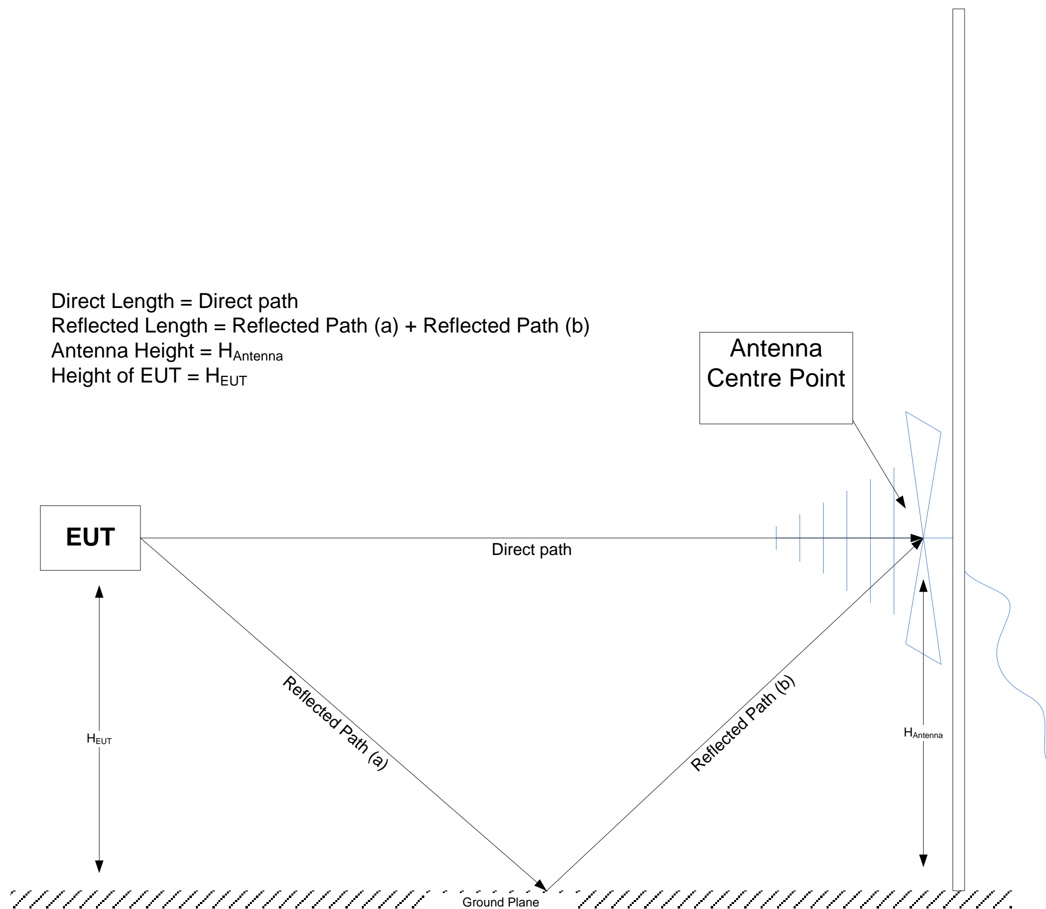


Figure C-1: Illustration of direct and reflected radiated emissions paths.

Table C-1: Signal transit time for various antenna heights.

Antenna Height (m)	Direct Length (m)	Reflected Length (m)	Difference in path length (m)	Transit Time difference (s)
1.00	3.00	3.61	0.61	2.02E-09
2.00	3.16	4.24	1.08	3.60E-09
3.00	3.61	5.00	1.39	4.65E-09
4.00	4.24	5.83	1.59	5.29E-09

Table C-2: Phase delay for different frequencies at different antenna heights.

Antenna Height (m)	Freq (MHz)	30	40	50	60	80	100
1.00	Phase delay (degrees)	21.80	29.07	36.33	43.60	58.13	72.67
2.00		38.89	51.86	64.82	77.79	103.71	129.64
3.00		50.20	66.93	83.67	100.40	133.87	167.33
4.00		57.18	76.24	95.30	114.36	152.48	190.60
	Period at Frequency (ns)	33.33	25.00	20.00	16.67	12.50	10.00

Table C-3: Constants used to calculate the above tables.

Constants		
Speed of light	3.00E+08	m\s
Distance to Antenna	3	m
Height of EUT	1	m

Appendix D: Shaped Gate Transients and Radiated Emissions Measurements

It is desirable to independently control the peak magnitude of the RF content in the collector emitter voltage and the collector current. This is achieved with a series of gate demand signals which achieved different a peak magnitude. The measured IGBT turn on transients are displayed in this appendix along with the measured radiated emissions sweep for several tests. All tests were carried out under the following conditions:

Rg = 5.6
Iload = 10 A
T = 25 °C
Vdc = 600 V

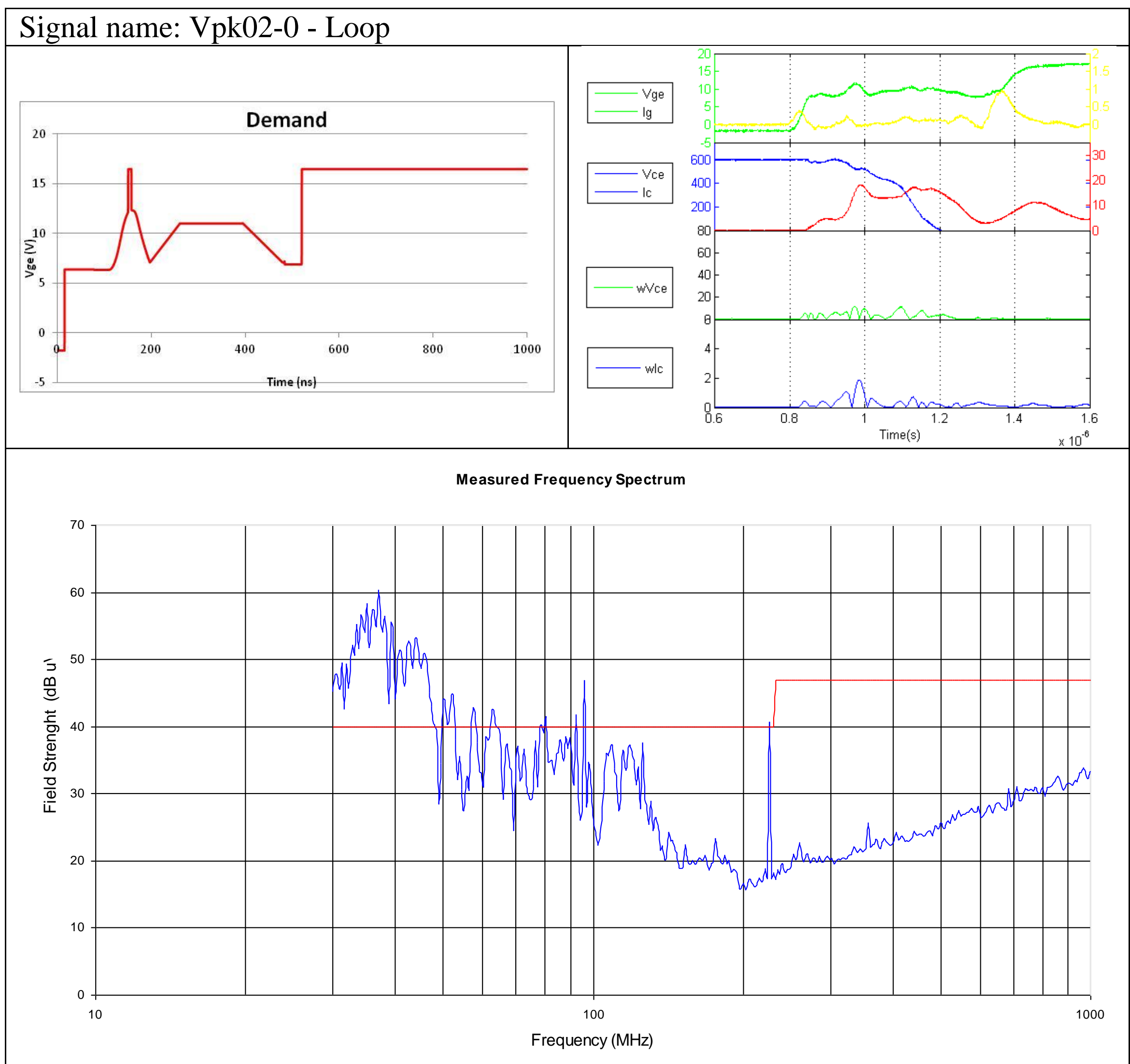


Figure D-1: RE from signal Vpk02_0

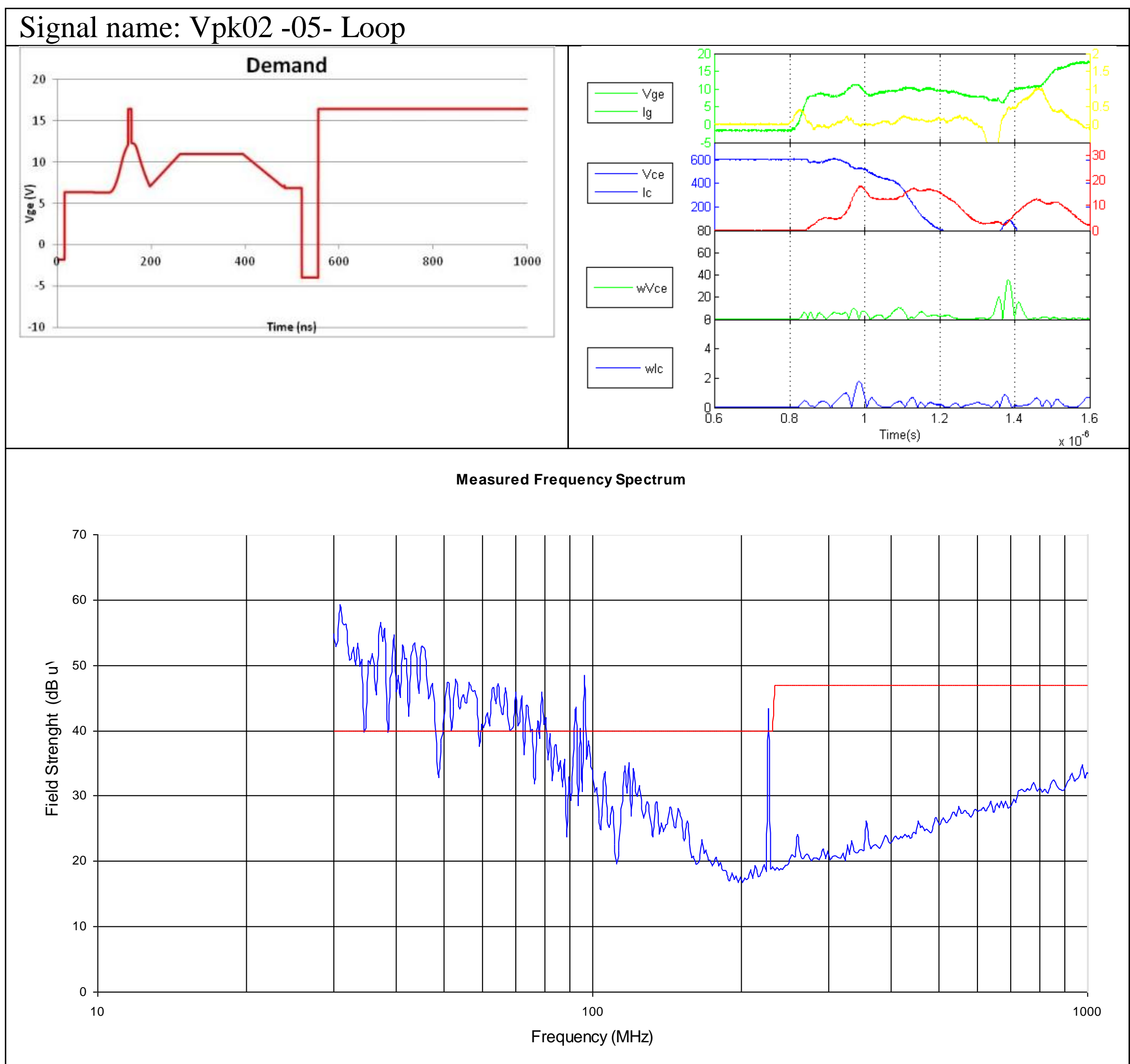


Figure D-2: RE from signal Vpk02_05

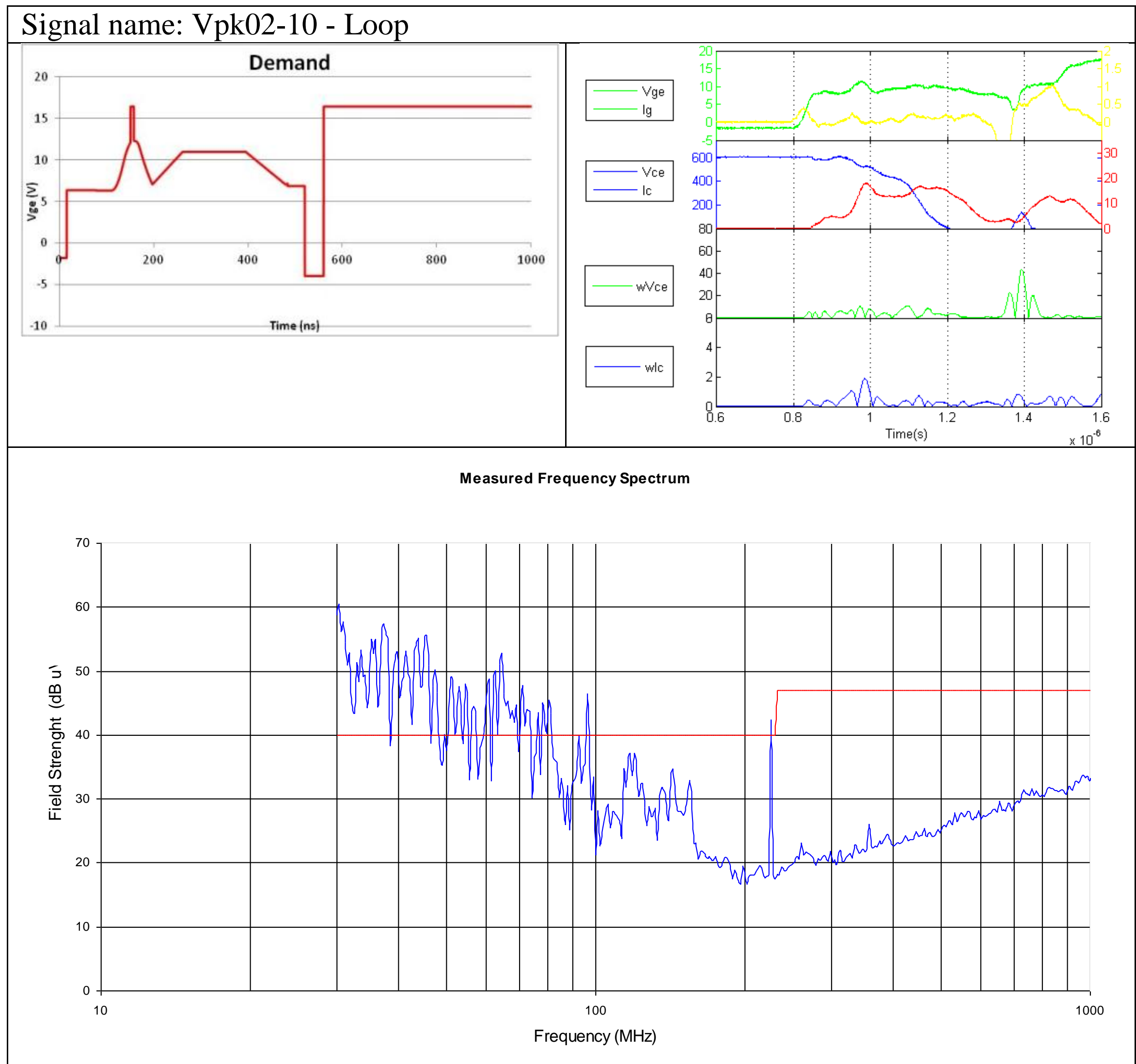


Figure D-3: RE from signal Vpk02_10

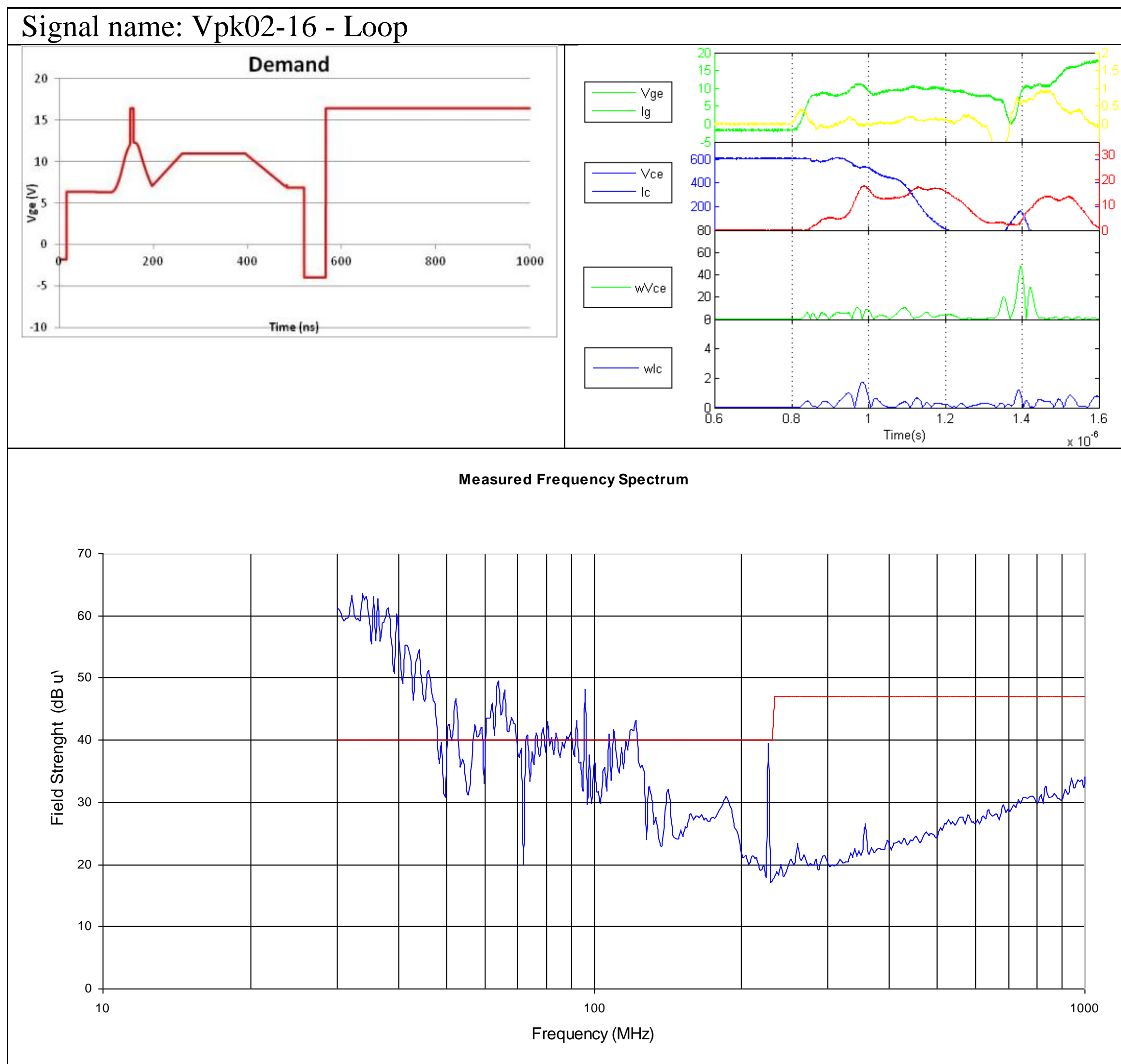


Figure D-4: RE from signal Vpk02_16

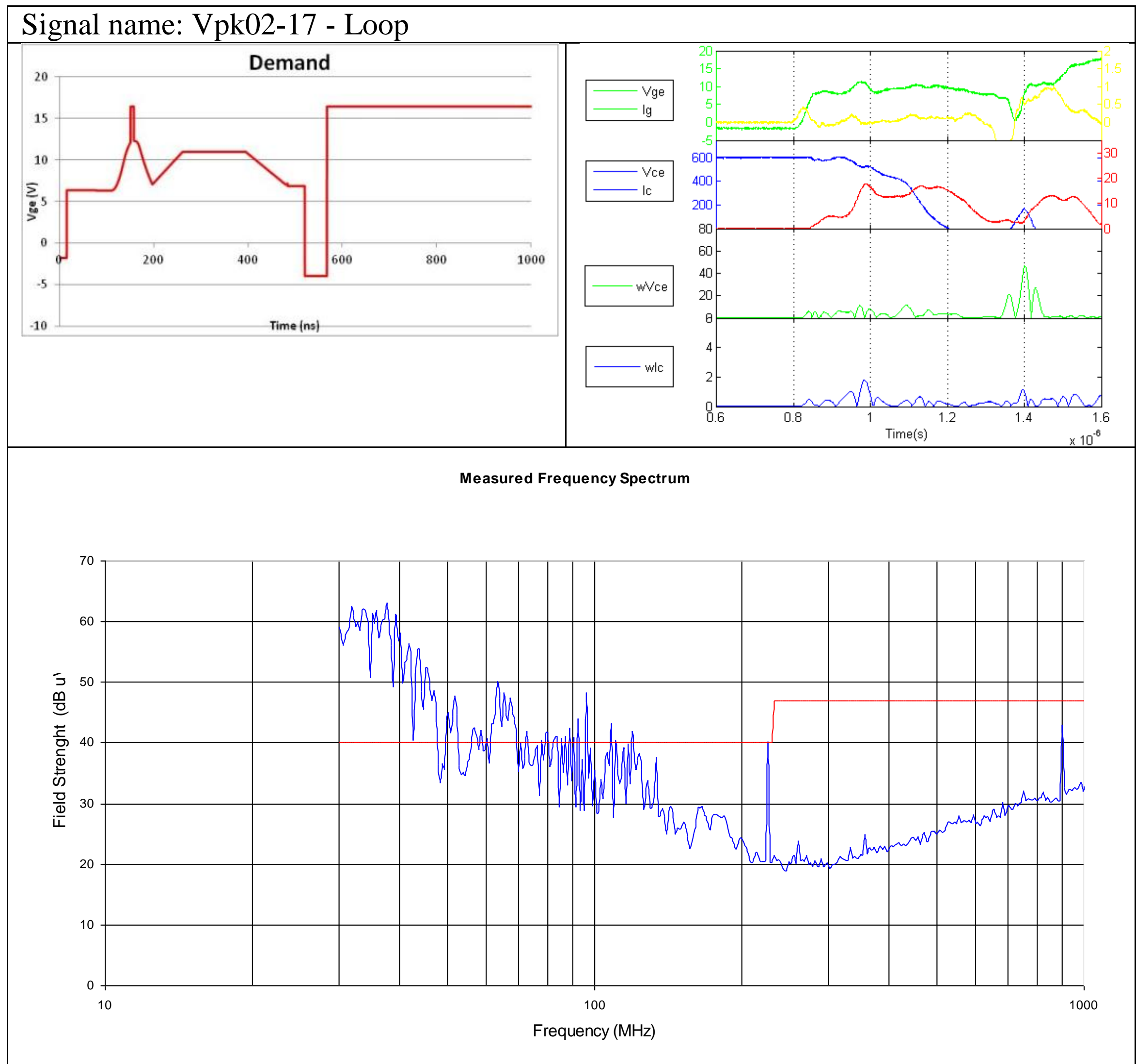


Figure D-5: RE from signal Vpk02_17

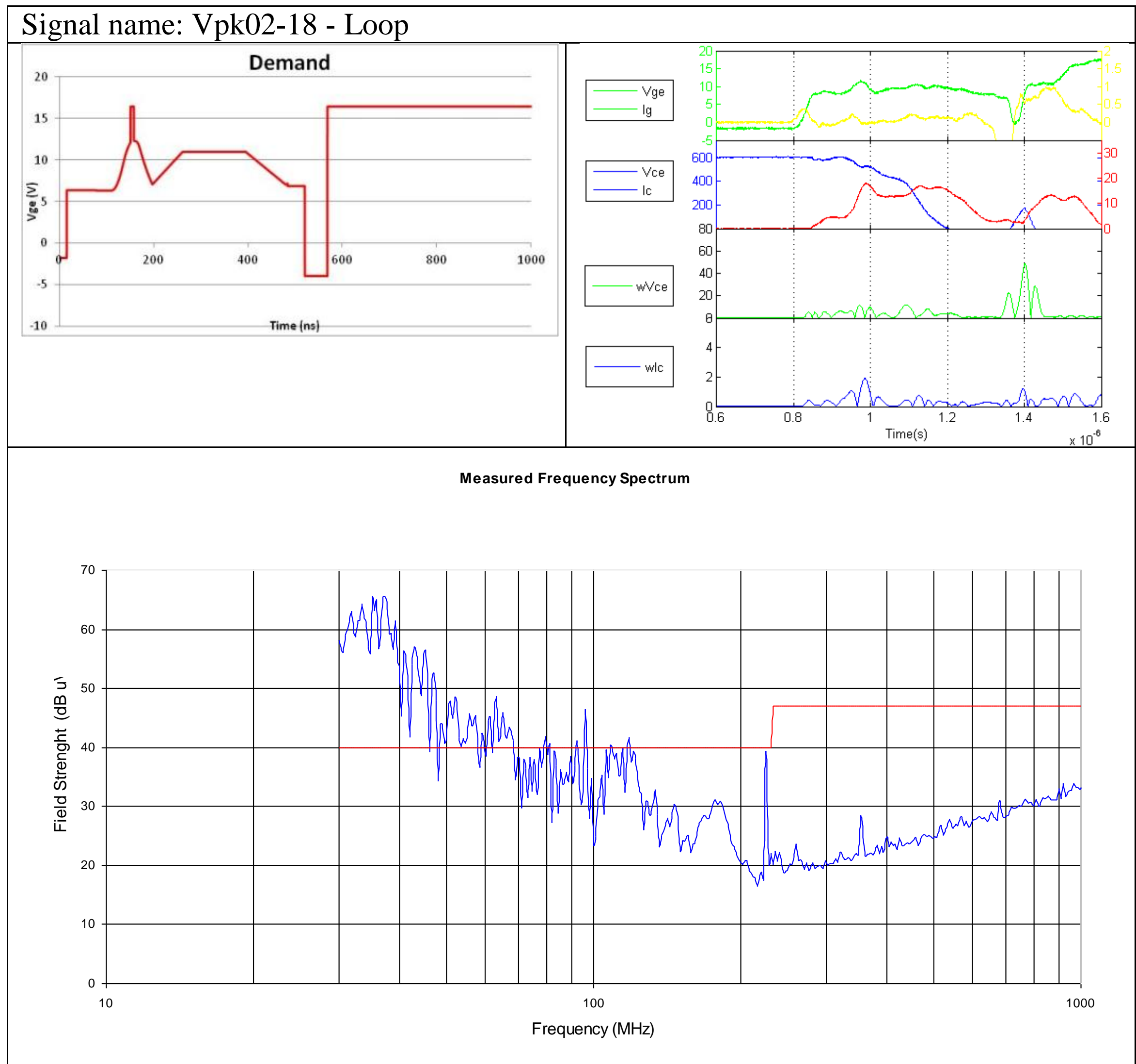


Figure D-6: RE from signal Vpk02_18

Appendix E: Temperature rise in IGBT die from pulse of energy loss

The duration of the switching transient for the IGBTs is from 100 to 200 ns. During this short time, it is assumed that and heat does not dissipate into the surrounding materials. The constants used to calculate the temperature rise are given in Table E-1. The temperature rise for different energy pulses as shown in Table E-2.

Table E-1: Physical constants and dimensions of IGBT die

Constants at room temperature (280.15 K)		
Density	2330	kgm^-3
Cp	705	J/(kgK))
IGBT measured dimensions		
Length	6.33	mm
Width	3.44	mm
Height	0.115	mm
Volume	2.5041E-09	m3

Table E-2: Temperature rise in Silicon for given energy pulse

Energy pulse (mJ)	ΔT (K)
5	1.22
10	2.43
15	3.65
20	4.86
25	6.08
30	7.29
35	8.51
40	9.72
45	10.94
50	12.16

List of References

1. Drury, B., *Drives and Control Handbook*. 2nd edition,2009: Institution of Engineering and Technology.
2. CISPR 11 Edition 5, 2009, Industrial, scientific and medical (ISM) radio-frequency equipment - Electromangetic disturbance characteristics - Limits and methods of measurement.
3. CISPR 22 Edition 6.0, 2008-09, Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement
4. IEC 61000-6-4:, 2007, Electromagnetic Compatibility (EMC) Part 6-4: Generic Standards- Emissions Standard for Industrial Environments
5. Cohen, L.S., et al. *The measurement of broad band over power line emissions*. in *International Symposium on Electromagnetic Compatibility, 2005. EMC 2005.* . 2005.
6. IEC 61800-3 Edition 2.1, 2008, Adjustable speed electrical power drive systems - Part 3: EMC requirments and specific test methods
7. Fukuda, J., S. Ogasawara, and M. Takemoto. *A basic study on inverter output filter for radiative noise suppression*. in *Power Electronics Conference (IPEC), 2010 International*. 2010.
8. Hanigovszki, N., J. Landkildehus, and F. Blaabjerg. *Output filters for AC adjustable speed drives*. in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*. 2007.
9. Skibinski, G.L., R.J. Kerkman, and D. Schlegel, *EMI emissions of modern PWM AC drives.* Industry Applications Magazine, IEEE, 1999. **5**(6): p. 47-80.
10. Khanna, V.K., *The InsulatedGate Bipolar Transistor - IGBT Theory and Design*2003: Wiley-Interscience.
11. Lutz, J., et al., *Semiconductor Power Devices, Physics, Characteristics, Reliability*2011: Springer.
12. Volke, A. and M. Hornkamp, *IGBT Modules - Technologies, Driver and Applications*2010: Infieon Technologies AG.
13. Cheng, D.K., *Fundamentals of Engineering Electromagnetics*1992: Prentice Hall.
14. Maxwell, J.C., *A Treatise on Electricity and Magnetism*1954: Dover Books.
15. Kraus, J.D., *Antennas*. Second,1988: McGraw-Hill.
16. Balanis, *Antenna Theory Analysis and Design*. Third Edition,2005: Wiley.
17. Paul, C.R., *Introduction to Electromagnetic Fields*1987: McGraw Hill.
18. Antonini, G., S. Cristina, and A. Orlandi, *EMC characterization of SMPS devices: circuit and radiated emissions model.* Electromagnetic Compatibility, IEEE Transactions on, 1996. **38**(3): p. 300-309.
19. Liu, Q., et al. *Experimental evaluation of IGBTs for characterizing and modeling conducted EMI emission in PWM inverters*. in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*. 2003.
20. Meng, J. and W. Ma. *Power converter EMI analysis including IGBT nonlinear switching transient model*. in *Industrial Electronics, 2005. ISIE 2005. Proceedings of the IEEE International Symposium on*. 2005.

21. Baliga, B.J., *Silicon Carbide Power Devices*2005: World Scientific Publishing Co.
22. Lidow, A., et al., *GaN Transistors for Efficient Power Conversion*, 2012, Power Conversion Publications.
23. Yu, A.Y.C., *Electron tunneling and contact resistance of metal-silicon contact barriers.* Solid-State Electronics, 1970. **13**(2): p. 239-247.
24. Sze, S.M., *Semiconductor Devices Physics and Technology*. 2nd Edition,2002.
25. Domeij, M., J. Lutz, and D. Silber, *On the destruction limit of Si power diodes during reverse recovery with dynamic avalanche.* Electron Devices, IEEE Transactions on, 2003. **50**(2): p. 486-493.
26. Semikron, *Semikron application manual*, Semikron, Editor 2004.
27. Linder, S., *Power Semiconductors*. 1st Edition,2006.
28. Baliga, B.J., *Power Semiconductor Devices*1995.
29. Baliga, B.J., *Fundamentals of Power Semiconductor Devices*2008: Springer.
30. Baliga, B.J. and E. Sun, *Comparison of gold, platinum, and electron irradiation for controlling lifetime in power rectifiers.* Electron Devices, IEEE Transactions on, 1977. **24**(6): p. 685-688.
31. Basu, S. and T.M. Undeland. *Diode recovery characteristics considerations for optimizing EMI performance of continuous mode PFC converters*. in *Power Electronics and Applications, 2005 European Conference on*. 2005.
32. Guerra, A., F. Maddaleno, and M. Soldano. *Effects of diode recovery characteristics on electromagnetic noise in PFCs*. in *Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998., Thirteenth Annual*. 1998.
33. Azar, R., et al., *Advanced SPICE modeling of large power IGBT modules.* Industry Applications, IEEE Transactions on, 2004. **40**(3): p. 710-716.
34. Johnson, C.M., *Current state-of-the-art and future prospects for power semiconductor devices in power transmission and distribution applications.* International Journal of Electronics, 2003. **90**(11/12): p. 667-693.
35. Laska, T., et al. *Optimizing the vertical IGBT structure-the NPT concept as the most economic and electrically ideal solution for a 1200 V-IGBT*. in *Power Semiconductor Devices and ICs, 1996. ISPSD '96 Proceedings., 8th International Symposium on*. 1996.
36. Laska, T., et al. *The field stop IGBT (FS IGBT) - A new power device concept with a great improvement potential*. in *12th International Symposium on Power Semiconductor Devices and ICs, May 22-25 2000*. 2000. Institute of Electrical and Electronics Engineers Inc.
37. Singh, M. and K. Khanchandani, *Power Electronics*2006: McGraw-Hill.
38. Eckel, H.-G. and K. Fleisch. *Turn-off behaviour of high voltage NPT- and FS-IGBT*. in *2008 13th International Power Electronics and Motion Control Conference, EPE-PEMC 2008, Sep 1-3 2008*. 2008. Piscataway, NJ 08855-1331, United States: Institute of Electrical and Electronics Engineers Computer Society.
39. Sheng, K., B.W. Williams, and S.J. Finney, *A review of IGBT models.* Power Electronics, IEEE Transactions on, 2000. **15**(6): p. 1250-1266.
40. Onishi, Y., et al. *Analysis on device structures for next generation IGBT*. in *Power Semiconductor Devices and ICs, 1998. ISPSD 98. Proceedings of the 10th International Symposium on*. 1998.

41. Shenoy, P.M., S. Shekhawat, and B. Brockway. *Application specific 1200V planar and trench IGBTs*. in *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE*. 2006.
42. Takahashi, H., et al. *Carrier stored trench-gate bipolar transistor (CSTBT)-a novel power device for high voltage application*. in *Power Semiconductor Devices and ICs, 1996. ISPSD '96 Proceedings., 8th International Symposium on*. 1996.
43. Wang, J. and B.W. Williams, *A simulation study of high voltage 4H-SiC IGBTs.* Semiconductor Science and Technology, 1998. **13**(13): p. 806-815.
44. Bock, B., *Switching IGBTs in parallel connection with enlarged commutation inductance*, in *Faculty of Electrical and Computer Engineering*2005, Ruhr-University.
45. Omura, I., W. Fichtner, and H. Ohashi, *Oscillation effects in IGBT's related to negative capacitance phenomena.* Electron Devices, IEEE Transactions on, 1999. **46**(1): p. 237-244.
46. Hefner, A.R., Jr., *Analytical modeling of device-circuit interactions for the power insulated gate bipolar transistor (IGBT).* Industry Applications, IEEE Transactions on, 1990. **26**(6): p. 995-1005.
47. Venkatesan, V., et al. *IGBT turn-off characteristics explained through measurements and device simulation*. in *Applied Power Electronics Conference and Exposition, 1997. APEC '97 Conference Proceedings 1997., Twelfth Annual*. 1997.
48. Maggs, J.D., T.N. Oliver, and M.T. Wright. *Electromagnetic compatibility of variable speed drives*. in *Power Electronics and Variable Speed Drives, 1996. Sixth International Conference on (Conf. Publ. No. 429)*. 1996.
49. Ott, H.W., *Noise Reduction Techniques in Electronic Systems*. 2nd Edition,1987: Wiley Interscience.
50. W.L.Weeks, *Electromagnetic Theroy for Engineering Applications*1964: Wiley.
51. Brown, J. and B. Whitlock, *Common-Mode to Differential-Mode Conversion in Shielded Twisted-Pair Cables (Shield- Current-Induced Noise).* 114th AES Convention, 2003.
52. Balanis, *Antenna Theory Analysis and Design*1982: Wiley.
53. Luszcz, J. *Modeling of common mode currents induced by motor cable in converter fed AC motor drives*. in *Electromagnetic Compatibility (EMC), 2011 IEEE International Symposium on*. 2011.
54. Bentley, J.M. and P.J. Link, *Evaluation of motor power cables for PWM AC drives.* Industry Applications, IEEE Transactions on, 1997. **33**(2): p. 342-358.
55. Ida, N., *Engineering Electromagnetics*2000: Springer.
56. Vance, E.F., *Shielding Effectiveness of Braided Wire Sheilds*, 1974, Stanford Research Institute.
57. Hoeft, L.O. and J.S. Hofstra, *Measured electromagnetic shielding performance of commonly used cables and connectors.* Electromagnetic Compatibility, IEEE Transactions on, 1988. **30**(3): p. 260-275.
58. Kerkman, R., D. Leggate, and G. Skibinski. *Interaction of drive modulation and cable parameters on AC motor transients*. in *Industry Applications Conference, 1996. Thirty-First IAS Annual Meeting, IAS '96., Conference Record of the 1996 IEEE*. 1996.

59. Adabi, J., et al. *Leakage current and common mode voltage issues in modern AC drive systems*. in *Power Engineering Conference, 2007. AUPEC 2007. Australasian Universities*. 2007.
60. Asmanis, G., et al. *Matrix frequency converter conducted and radiated emissions*. in *Electric Power Quality and Supply Reliability Conference (PQ), 2010*. 2010.
61. Skibinski, G., et al. *Generation, control and regulation of EMI from AC drives*. in *Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE*. 1997.
62. Oswald, N., et al., *Analysis of Shaped Pulse Transitions in Power Electronic Switching Waveforms for Reduced EMI Generation.* Industry Applications, IEEE Transactions on, 2011. **47**(5): p. 2154-2165.
63. Addison, P.S., *The Illustrated Wavelet Transform Handbook*2002: Taylor and Francis.
64. Mallat, S., *A Wavelet Tour of signal processing, the sparse way*2008: Academic Press.
65. Kuratli, C., A. Biber, and Q. Huang. *A 16 A IGBT-gate drive ASIC in a 18 V, 3um BiCMOS technology*. in *Industrial Electronics, 1995. ISIE '95., Proceedings of the IEEE International Symposium on*. 1995.
66. Valentine, R.J. *Power module control design*. in *Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE*. 1995.
67. Herzer, R., *Integrated Power Devicees and Smart Power*, in *ECPE Power Semiconductors and Devices*2008, ECPE: Nuremburg.
68. Mohan N., T.M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications and Design*2002: John Wiley & Sons.
69. Valentine, R., *Motor control electronics handbook*. 2nd edition. McGraw-Hill handbooks. Vol. 1. 1998, New York: McGraw-Hill.
70. Scheuermann, U. and F. Ebersberger, *Packaging of Large Area Power Chips Â¿ Extending the Limits of Standard Module Technology.* Integrated Power Systems (CIPS), 2006 4th International Conference on, 2006: p. 1-6.
71. IR, *IR Application Note AN-983*, 1997, 2005.
72. James, G.C., V. Pickert, and M. Cade. *A thermal model for a multichip device with changing cooling conditions*. in *Power Electronics, Machines and Drives, 2008. PEMD 2008. 4th IET Conference on*. 2008.
73. Palmer, P.R. and A.N. Githiari. *The series connection of IGBTs with optimised voltage sharing in the switching transient*. in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*. 1995.
74. Palmer, P.R. and H.S. Rajamani, *Active Voltage control of IGBTs for high power applications.* Power Electronics, IEEE Transactions on, 2004. **19**(4): p. 894-901.
75. Luniewski, P. and U. Jansen. *Unsymmetrical gate voltage drive for high power 1200V IGBT4 modules based on coreless transformer technology driver*. in *2008 13th International Power Electronics and Motion Control Conference, EPE-PEMC 2008, Sep 1-3 2008*. 2008. Piscataway, NJ 08855-1331, United States: Institute of Electrical and Electronics Engineers Computer Society.
76. IR, *Application Note AN-944 - Use Gate Charge to Design the gate Drive Circuit for Power MOSFETs and IGBTs*, 1996.

77. Weis, B. and M. Bruckmann. *A new gate driver circuit for improved turn-off characteristics of high current IGBT modules*. in *Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE*. 1998.
78. Grbovic, P.J. *The gate drive requirements for new generation of high current low voltage IGBTs employed in motor converters*. in *Sixth International Conference on Power Electronics and Drive Systems, PEDS 200, Nov 28-Dec 1 2005*. 2005. Kuala Lumpur, Malaysia: Institute of Electrical and Electronics Engineers Inc., Piscataway, NJ 08855-1331, United States.
79. Lee, J.-B. and D.-S. Hyun. *Gate voltage pattern analyze for short-circuit protection in IGBT inverters*. in *PESC 07 - IEEE 38th Annual Power Electronics Specialists Conference, Jun 17-21 2007*. 2007. Orlando, FL, United States: Institute of Electrical and Electronics Engineers Inc., Piscataway, NJ 08855-1331, United States.
80. Luo, J., Y.C. Liang, and B.-J. Cho, *Design of IGBT gate drive circuit with SOA consideration.* Proceedings of the 1998 2nd International Conference on Power Electronics Drives and Energy Systems for Industrial Growth, PEDES'98, 1998. **1**: p. 307-311 BN - 0-7803-4879-6.
81. IR, *IR Application Note AN-990 - Application Characterization of IGBTs*, S. Clemente, Editor 1997,2005.
82. Blaabjerg, F. and J.K. Pedersen. *An optimum drive and clamp circuit design with controlled switching for a snubberless PWM-VSI-IGBT inverter leg*. in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*. 1992.
83. Ross, J., *The Essence of Power Electronics*1996: Prentice Hall.
84. John, V., B.-S. Suh, and T.A. Lipo, *High-performance active gate drive for high-power IGBT's.* IEEE Transactions on Industry Applications, 1999. **35**(5): p. 1108-1117.
85. Sawezyn, H., N. Idir, and R. Bausiere. *Lowering the drawbacks of slowing down di/dt and dv/dt of insulated gate transistors*. in *Power Electronics, Machines and Drives, 2002. International Conference on (Conf. Publ. No. 487)*. 2002.
86. Musumeci, S., et al., *Switching-behavior improvement of insulated gate-controlled devices.* Power Electronics, IEEE Transactions on, 1997. **12**(4): p. 645-653.
87. Momota, S., et al. *Analysis on the low current turn-on behavior of IGBT module*. in *Power Semiconductor Devices and ICs, 2000. Proceedings. The 12th International Symposium on*. 2000.
88. Onozawa, Y., M. Otsuki, and Y. Seki. *Great improvement in turn-on power dissipation of IGBTs with an extra gate charging function*. in *Power Semiconductor Devices and ICs, 2005. Proceedings. ISPSD '05. The 17th International Symposium on*. 2005.
89. Grbovic, P.J., *An IGBT Gate Driver for Feed-Forward Control of Turn-on Losses and Reverse Recovery Current.* Power Electronics, IEEE Transactions on, 2008. **23**(2): p. 643-652.
90. Grbovic, P.J. *Gate driver with feed forward control of turn off performances of an IGBT in short circuit conditions*. in *Power Electronics and Applications, 2007 European Conference*. 2007.
91. Kazuyuki., H. and Y. Shinsuke.EP2015453.Drive circuit for voltage driven electronic element.E.P. Office

92. Igarashi, S., et al. *An active control gate drive circuit for IGBTs to realize low-noise and snubberless system*. in *Power Semiconductor Devices and IC's, 1997. ISPSD '97., 1997 IEEE International Symposium on*. 1997.
93. Gerster, C. and P. Hofer, *Gate-controlled dv/dt- and di/dt-limitation in high power IGBT converters.* EPE Journal (European Power Electronics and Drives Journal), 1996. **5**(3-4): p. 11-16.
94. Helsper, M. and F.W. Fuchs. *Adaption of IGBT Switching Behaviour by Means of Active Gate Drive Control for Low and Medium Power*. in *EPE 2003 10th European Conference on Power Electronics and Applications,*. 2003. Toulouse, Frankreich.
95. Han, W. and Z. Bo. *Optimization of switching losses and EMI in a gate driver circuit for IGBT devices*. in *Communications, Circuits and Systems (ICCCAS), 2010 International Conference on*. 2010.
96. Schmitt, G., R. Kennel, and J. Holtz. *Voltage gradient limitation of IGBTS by optimised gate-current profiles*. in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*. 2008.
97. Lihua, C. and F.Z. Peng. *Closed-Loop Gate Drive for High Power IGBTs*. in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*. 2009.
98. Sachdeva, R. and E.P. Nowicki. *Characterization of a gate drive technique for snubberless operation of gate controlled devices*. in *Electrical and Computer Engineering, 2001. Canadian Conference on*. 2001.
99. Abu-Khaizaran, M., P. Palmer, and Y. Wang. *Parameters influencing the performance of an IGBT gate drive*. in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*. 2008.
100. Shihong, P. and T.M. Jahns. *Flexible dv/dt and di/dt control method for insulated gate power switches*. in *Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE*. 2001.
101. Kagerbauer, J.D. and T.M. Jahns. *Development of an active dv/dt control algorithm for reducing inverter conducted EMI with minimal impact on switching losses*. in *PESC 07 - IEEE 38th Annual Power Electronics Specialists Conference, Jun 17-21 2007*. 2007. Orlando, FL, United States: Institute of Electrical and Electronics Engineers Inc., Piscataway, NJ 08855-1331, United States.
102. Busatto, G., et al. *EMI analysis in high power converters for traction application*. in *Power Electronics and Applications, 2005 European Conference on*. 2005.
103. Igarashi, S., et al., *Analysis and reduction of radiated EMI noise from converter systems.* Electrical Engineering in Japan, 2000. **130**(1): p. 106-117.
104. Rosales, A., A. Sarikhani, and O.A. Mohammed, *Evaluation of Radiated Electromagnetic Field Interference Due to Frequency Swithcing in PWM Motor Drives by 3D Finite Elements.* Magnetics, IEEE Transactions on, 2011. **47**(5): p. 1474-1477.
105. Revol, B., et al., *EMI Study of Three-Phase Inverter-Fed Motor Drives.* Industry Applications, IEEE Transactions on, 2011. **47**(1): p. 223-231.
106. Walt, K., *Taking the Mystery out of the Infamous Formula, "SNR= 6.02N + 1.76 dB" and Why You Should Care.* Analog Devices MT - 001, 2008.

107. Domurat-Linde, A. and E. Hoene. *Analysis and Reduction of Radiated EMI of Power Modules*. in *Integrated Power Electronics Systems (CIPS), 2012 7th International Conference on*. 2012.
108. IEC 60747-9:, 2007, Semiconductor Devices, Discrete Devices, Part 9, Insulated-gate Biploare Transistors, (IGBTs)
109. IEC 55022:2010, 2010, Information Technology Equipment - Radio Disturbance Characteristics - Limits and Methods of Measurements
110. Battermann, S. and H. Garbe. *Influence of the ground plane geometry on the normalized site attenuation of an OATS*. in *Antennas and Propagation Society International Symposium, 2004. IEEE*. 2004.
111. Maas, J., S. Connor, and D. Hoolihan. *Examining the effect of source type on the accuracy of inverse distance fall-off for radiated EMI measurements*. in *Electromagnetic Compatibility (EMC), 2011 IEEE International Symposium on*. 2011.
112. Kang, T.W. and H.T. Kim, *Electric field strength and extrapolation in radiated emission measurements at an open area test site.* Science, Measurement and Technology, IEE Proceedings -, 2001. **148**(6): p. 246-252.
113. CISPR 16-1-1ed 3.0 2009, Specification for radio disturbance and immunity measuring apparatus and methods - Part 1-1: Radio disturbance and immunity measuring apparatues - Measuring apparatus.
114. Gavenda, J.D., *Effect of Electromagnetic Source Type and Orientationon Signal Falloff with Distance*, in *IEEE International Symposium on Electromagnetic Compatibility*1987. p. 338-341.
115. Kriz, A. *Calculation of antenna pattern influence on radiated emission measurement uncertainty*. in *Electromagnetic Compatibility, 2008. EMC 2008. IEEE International Symposium on*. 2008.
116. Krug, F. and P. Russer, *The time-domain electromagnetic interference measurement system.* Electromagnetic Compatibility, IEEE Transactions on, 2003. **45**(2): p. 330-338.
117. Mohan, N., *Advanced Electric Drives: Analysis, Control and Modeling Using Simulink*2001: Mnpere.
118. Gambica_Technical_Guide, *Varaible Speed Drives and Motors, Technical Report No. 2*, 2006, Gambica.
119. Goldman, A., *Handbook of Modern Ferromagnetic Materials*1999: Springer.
120. Bjork, F., et al., *3rd Generation Silicon Carbide Schottky Diodes Pave the Way for Energy Efficient Power Solutions*, in *Power Electronics Europe*2009. p. 24-27.
121. Wang, L., et al., *Gallium Nitride Power FET Characterization and Application*, in *PCIM Asia 2011*2011: Shanghai, China.
122. Allende, S., et al., *Asymmetric hysteresis loop in magnetostatic-biased multilayer nanowires.* Nanotechnology, 2009. **20**(445707).
123. Blankenship, E., D. Arnett, and S. Chan. *Searching for the elusive correction factor between 3m and 10m radiated emission tests*. in *Electromagnetic Compatibility, 2009. EMC 2009. IEEE International Symposium on*. 2009.