Investigation of Methods for Loss of Mains Detection for Domestic Scale Distributed Generation

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To my family

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Abstract

The drive to lower the environmental impact of power generation has underlined the importance of distributed generation (DG). DG allows a multitude of dispersed renewable technologies to be included within the energy supply network. The energy generation of a DG installation doesn't necessarily coincide with local power consumption; grid connection allows surplus local power to be distributed using the wider power network. This results in a variety of DG units requiring grid connection. A power electronics interface is commonly needed to achieve connection between the DG unit and the distribution network. Whilst DG units are available in a multitude of sizes, the focus of this work is domestic scale DG. Single phase power inverters are commonly used to connect DG units to the utility.

An issue associated with the interconnection of generators within the distribution network is the formation of power islands. A power island is defined as a section of the power network, consisting of generators and loads, which becomes electrically isolated from the wider power network.

The majority of grid connection standards stipulate that the grid connection power electronics interface must include a robust loss of mains (LOM) detection routine. Once a LOM event has been detected the output power of the DG unit must be reduced to zero to guarantee no power island exists.

This thesis details the work carried out during the completion of an Engineering Doctorate (EngD) Degree in Power Electronics, Machines and Drives. A low voltage laboratory test bench and associated simulation model have been designed and constructed to allow multiple in-the-loop based LOM detection methods to be presented, analysed and compared.

A new LOM detection technique has been created, referred to as the proposed technique. The proposed technique is a hybrid LOM detection technique which uses a passive routine to signal when a LOM event may have occurred and an active technique to confirm the LOM event. The passive routine uses Fourier analysis to constantly monitor the magnitude and spread of high frequency voltage components present at the

DG unit connection point. The active confirmation routine is an active power shift function.

A fully rated 500W laboratory test bench was created which allows the proposed technique to be verified at power levels more realistic for a standard DG unit installation.

Contents

List of Figures

List of Tables

List of Publications

"Periodic Injection of a Second Harmonic Component With Fourier Isolation for the Detection Of Power Islands," in Power Electronics Machines and Drives. Sixth IET international conference on, March 2012.

"A Simulation Environment for the Investigation into Loss of Mains Detection Methods for Grid Connected Single Phase Inverters," in Environment Friendly Energies And Applications, 2012. Second Internationl Symposium on, June 2012.

Nomenclature

Roman Symbols

α	Current angle
C	Capacitance
e	Error
f_θ	Frequency calculated using phase angle
f	Frequency
f_{max}	Maximum valid frequency
f_s	Sampling frequency
$I_{fundamental}$	Current at balanced power
$\hat{I}$	Current magnitude
I	Current
I_{noise}	Additional current noise
k	Bin frequency number
k_p	Proportional gain
k_i	Integral gain
L	Inductance
N	Number of samples
ΔP	Active power mismatch
P	Real power
ΔQ	Reactive power mismatch
Q	Reactive power

R	Resistance
S	Complex power
T_θ	Summed phase angle
t	Time
V_{change}	Periodic voltage amplitude change
V	Voltage
x	Sampled value
X_k	Harmonic information for a specific frequency

Greek Symbols

κ	Inverter output power at balanced load
μ	Mean
$\hat{\omega}$	Angular velocity
ω_{ff}	Fundamental angular velocity
$\Delta\hat{\omega}$	Angular velocity modifier
ϕ	Phase difference
σ	Standard Deviation
$\hat{\theta}$	Output phase angle
θ	Input phase angle
θ_{2f}	Double of the fundamental phase angle
θ_f	Fundamental phase angle
φ	Phase difference

Superscripts

*	Demand

Subscripts

c	Cut-off
d	Direct axis component
I	Imaginary

INV	Inverter output
m	Measured
n	Sample number
PCC	Point of Common Coupling
PLL	Phase Locked Loop output
q	Quadrature axis component
REF	Reference
RMS	Root Mean Square
R	Real
t	Total

Acronyms

AC	Alternating Current
CHP	Combined Heat an Power
DC	Direct Current
DFIG	Doubly Fed Induction Generator
DFT	Discrete Fourier Transform
DG	Distributed Generation
DSP	Digital Signal Processor
DWT	Discrete Wavelet Transform
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
IEEE	Institute of Electrical and Electronics Engineers
LOM	Loss Of Mains
NDZ	None Detection Zone
PC	Personal Computer
PEM	Proton Exchange Membrane
PI	Proportional Integral

PLL Phase Locked Loop output

p-PLL Power Phase Locked Loop output

PV Photovoltaic

PWM Pulse Width Modulation

RMS Route Mean Square

ROCOF Rate Of Change Of Frequency

ROCOV Rate Of Change Of Voltage

SOFC Solid Oxide Fuel Cell

SRAM Static Random Access Memory

UK United Kingdom

USB Universal Serial Bus

VCO Voltage Controlled Oscillator

WFT Windowed Fourier Transform

Chapter 1

Introduction

The Newcastle University EngD Centre in Power Electronics, Machines and Drives is one of a small number of EPSRC funded centres set up with the intention of producing the next generation of leading engineers and managers. The four year EngD programme provides an equivalent academic challenge as a PhD degree whilst incorporating more industry driven aspects given by an industrial sponsor. The first three years of the programme include compulsory taught modules. Academic modules are included to provide an in depth engineering knowledge, with modules relating to power electronics, drives and control. The more business focussed modules, including business management and law, are intended to increase managerial career development.

In the early stages of the EngD programme the student must work with both an academic and an industrial supervisor to fully define the focus of the research work. The research project must match the needs of the industrial sponsor whilst providing an area of significant academic interest.

The industrial sponsor for the presented work is the National Renewable Energy Centre (Narec). Narec is the national centre for the UK dedicated to advancing the development, demonstration, deployment and grid integration of renewable energy and low carbon generation technologies. The company was founded in 2002 by One North East as part of the Strategy for Success programme. The intention of Narec as a company is to stimulate local business development to increase employment levels within the renewable and sustainable energy sector. This has led to Narec being involved in many different areas of work, with the company now operating with four distinct operating sectors:

- Distributed Generation
- Electrical Networks.
- Marine Renewables.

- Wind Energy.

These factors meant that Narec was an ideal sponsor for a cooperative research project with Newcastle University.

1.1 Objectives

Environmental issues have been well publicised in more recent times, with growing pressure on governments around the world to reduce the impact that the increased energy demands of modern day life has on the environment. Many forms of electricity generation contribute towards the production of environmentally harmful substances, with fossil fuel based electricity generation still providing a large proportion of the energy we use.

The need to increase the proportion of energy produced from renewable energy sources has led to the investigation of multiple technologies. By allowing small domestic scale generators to be connected to the distribution network, an increasingly diverse range of energy sources can be utilised.

The increased popularity of small scale DG has resulted in grid-connected single-phase power inverters becoming more common place. The main objective of this thesis is to investigate the loss of mains (LOM) issue associated with grid-connected single-phase power inverters. As this is a major stumbling block in the further deployment of grid-connected inverters, it is intended that the work completed in this project provides a feasible LOM detection technique. Looking at the wider picture, this work could therefore increase the applicability of single-phase grid-connected power inverters to energy produced from renewable energy sources.

More specifically, after discussions with industrial and academic partners, the following objectives where agreed:

- To design and build a scaled power laboratory test bench specifically to test different LOM detection techniques.
- To produce an accurate simulation model of the scaled power laboratory test bench.
- To develop a robust LOM detection technique, comparing it to an array of currently available techniques.
- To validate the results obtained using the scaled power laboratory test bench using a more realistic power rated laboratory test bench.

1.2 Results Capture and Presentation

The simulation results presented in this thesis are obtained using the Matlab/Simulink numerical computing environment. The results are presenting using developed Matlab routines to plot the data in a clear and consistent way.

The practical results presented in this thesis are plotted using the same Matlab routines as the simulation data uses. This allows for direct comparison of the results and a more consistent presentation style. The experimental data is captured and stored on the control board in RAM in real time. Once the experiment is completed the data is downloaded to the connected personal computer and can be treated in the exact same way as the simulation data.

1.3 Chapter Review

The second chapter in this thesis is a short literature review. The environmental and economic issues associated with the continued use of fossil fuel based energy generation as the main energy provider are introduced. This leads on to the prospect of DG being addressed, with possible benefits and technical implications discussed. A section follows which describes the more popular DG unit technologies. This section is included to communicate the reasons behind choosing a grid-connected single-phase inverter as the main focus of this project, by underlining the diverse nature of its use. Issues related to islanding are stated, to explain why the majority of utilities stipulate that islanding can not be allowed to occur. The different categories of LOM detection techniques are introduced and the general merits and drawbacks are discussed along with a selection of example techniques. Finally, the standard laboratory test bench, defined in IEEE standard 1547.1 [1], is introduced with a modular diagram and the intended operation is explained.

Chapter 3 describes the design and construction of a scaled power laboratory test bench. This chapter begins by stating the advantages of using a scaled power laboratory test bench over a fully power rated set-up. The circuit diagram is presented, showing the major components and how they are interconnected. A short description of the important hardware modules is included with key features described along with their contribution to the overall system operation. The Matlab/Simulink simulation model is described to indicate how the practical circuit operation can be fully represented within a safe simulation environment. A control section follows which explains the closed loop current control that has been implemented both in the simulation environment and on the hardware controller. The key functions within the controller are discussed and preliminary experimental results are presented to demonstrate how each part works. A short section is included with a derivation of

power mismatch calculations. This allows the operation of subsequent tests to be fully specified. A final section presents preliminary results for the system as a whole, showing how the test bench power flow can be controlled to allow LOM detection techniques to be fully tested. The final section also demonstrates the closeness of the simulation model relative to the hardware set-up in terms of overall operation.

Chapter 4 is the largest chapter in this thesis. The results obtained whilst testing a variety of LOM detection techniques are presented. The first section of this chapter introduces a standard LOM test which remains consistent throughout the testing of the different LOM detection techniques. In total, six LOM detection techniques are presented in this chapter: two passive routines and four active routines. The presentation of each LOM detection routine follows the same structured layout: firstly, the LOM detection routine is introduced with a description of its operation and a diagram; secondly, results are presented showing the important operational features of the specific LOM detection technique; thirdly, an array of results are presented which allows the LOM detection technique to be compared to techniques of the same type. The results from both the simulation and experiment are presented at each stage to allow direct comparison. Two discussions are including within this chapter: one comparing the two developed passive routines and the other comparing the four active routines. A short section at the end of this chapter discusses the results obtained whilst testing the techniques for an extended period of time.

Chapter 5 details the new LOM detection technique that has been developed during the completion of this project. The principles behind the operation of the proposed LOM detection method are stated at the beginning of this chapter. The passive and active elements of the proposed technique are discussed individually at first. The following section describes how the routines are scheduled in program code and states the factors that make the program switch between the two different operation modes: passive and active. The processes that are completed within the controller during the different operation modes are stated along with a complete system algorithm diagram. The first results that are presented demonstrate that the proposed LOM detection technique can detect a LOM event when the system is operating at the most challenging operating point. Further, results are presented which allow certain features relating to the system operation to be discussed. A comparison with the active techniques is completed to fully evaluate the proposed LOM detection technique.

Chapter 6 describes the design and construction of a 500 W laboratory test bench. The intention behind the work completed in this chapter is to fully validate the proposed technique at power levels similar to a standard DG unit installation. The laboratory test bench is introduced and the individual hardware components are briefly described. The operation of the constructed set-up is presented using results

which demonstrate how a LOM event can cause the formation of a power island and how this operation is similar to the scaled voltage laboratory test bench. Further results are given to verify that the proposed LOM detection technique can successfully detect LOM events when implemented on the higher power laboratory test bench.

Chapter 2

Literature Review

This chapter is intended to provide background information related to loss of mains detection for distributed generation.

The chapter begins with a short section which underlines the need for the future energy supply network to include more renewable energy sources. Both environmental and economic issues are discussed, along with various governmental initiatives that have been implemented to increase the attraction of renewable energy.

A definition of distributed energy generation is given, along with a description of classical energy generation to allow the differences to be highlighted. The possible benefits and technical implementation issues of distributed generation are discussed.

A section is included which describes some of the leading distributed generation technologies. This demonstrates the energy source diversity expected in the future energy supply network.

The selection of popular distributed generation technologies indicates that a common piece of hardware is appropriate to allow grid connection: a DC-AC single phase power inverter.

The next section explains in more depth the problems associated with the occurrence of power islands within the distribution network. The need for a robust loss of mains detection technique is stated along with relevant connection standards. A review of the more established loss of mains detection methods is included with the merits and drawbacks of each technique discussed.

The standard laboratory test bench that is used to evaluate loss of mains detection techniques is presented and the main features are explained.

2.1 Renewable Energy

Over the past 4-5 decades there has been an increased focus on a future energy supply network that is less dependant on fossil fuel based generation. This shift away from fossil fuel based energy generation has been caused by three main factors:

- *Exhausted fossil fuel supplies* - Since the industrial revolution, a sharp increase in energy consumption has resulted in a large reduction in the amounts of natural resources available [2]. This has two fundamental effects, an increase in cost and the inevitable outcome that supplies will eventually run out [3].
- *Pollution* - The by-products produced during fossil fuel based energy generation contribute towards climate change which has serious environmental consequences such as increased sea levels, more frequent extreme weather events, droughts and the spread of disease [4].
- *Security of supply* - Resource diversification is necessary to guarantee future energy generation is capable of meeting the rising demand [5].

These factors underline the need for an energy supply network that incorporates a larger proportion of energy generated from renewable energy sources [6], with the Stern Review, commissioned by the Treasury in July 2005, stipulating that the energy generation sector will need to be 60% de-carbonised by 2050 [7]. To remain economically and environmentally viable, governments around the world must introduce measures to ensure an increase in the proportion of energy generated from renewable energy sources [8].

To increase the appeal of renewable power generation use, many governments have implemented large financial incentives. These schemes include rewards such as renewable energy tax breaks, and penalties such as a carbon emissions tax. A good example is the scheme in China, where wind power has a 60% higher feed-in tariff than coal fuelled power generation [9].

The drive to increase the proportion of energy generated from renewable energy sources has resulted in many schemes and technologies being investigated. It is now commonly accepted that the future energy supply network will use energy generated from an increasingly diverse range of energy sources [10]. This larger range of power sources adds complexity to the energy supply network.

A further increase in the array of devices that are connected to the power supply network is brought about by the necessity to include energy storage devices when the level of renewable power generation is increased. The energy storage devices are

required to compensate for any mismatch in power generation and power consumption as the power output available from many renewable energy resources can be considered to be intermittent and largely unpredictable [11–13].

2.2 Classical Energy Generation

The classical energy generation and supply network is based on large centralised generation and long distance power transmission [14, 15]. This method of power generation and delivery generally incorporates similar stages [16, 17]:

- Large centralised generation.
- Generator transformer to increase the voltage.
- A high voltage transmission network to transfer power over long distances.
- Supply transformers to decrease the voltage.
- Distribution network to supply energy to individual loads.

This conventional energy supply configuration has many advantageous qualities, including:

- Generation can be large and efficient.
- The high voltage transmission network allows reasonable levels of loss to be achieved when transporting the power over long distances.
- The distribution network can be assumed to have unidirectional power flow, allowing for easier fault detection and location [18].
- The infrastructure for fossil fuel extraction and transportation is already established in many parts of the world.

The main disadvantage of large centralised generation is that the majority of technologies, excluding large hydro and to a certain extent nuclear, produce environmentally harmful by-products [19]. Whilst nuclear power generation does produce radioactive by-products, they can be sealed away to decay over time.

2.3 Distributed Generation

DG is considered one of the leading technology areas to increase the proportion of energy generated from renewable sources [20]. DG is normally defined as smaller generation located within the distribution network that is not centrally planned by the utility company [21]. These attributes are due to two main reasons:

- Renewable energy sources have a much lower energy density than fossil fuels, so the generators are generally smaller.
- The location of the generator needs to be near the energy source i.e. near a stream for micro hydro.

The power output for a distributed generator is normally smaller than 50-100 MW [22]. Distributed generators can be incorporated within the power supply network either in a grid-connected or standalone configuration [23].

2.3.1 Possible benefits

The integration of distributed generation into the current energy supply network has three main types of benefits [24]:

- Environmental:
  - Reducing the production of greenhouse gases, displacement of fossil fuel generated electricity in favour of renewable energy sources.
  - Avoid building new large centralised generators which are now considered as a source of noise and visual pollution.
  - Avoid more transmission lines being built. By shifting generation closer to the load, the need for transmission lines is reduced.
- Commercial:
  - Market uncertainty. With the energy market becoming less stable, the lower outlay required to build a DG site is becoming more attractive to prospective investors.
  - Avoid transmission line losses and costs.
  - Improved power quality. Moving the supply closer to the load can improve the supply voltage profile.

  - Enhanced system reliability. Allowing the DG to continue in the case of a grid fault can increase reliability. There is less reliance on a small number of large generators, so when a generator fails, a much smaller proportion of the generation capacity is lost.
  - Congestion relief in the transmission system.
  - Modular nature of DG can offer more flexibility.

- National/Regulatory:

  - Security of supply. In modern society the reliance on electricity is huge, with a disruption affecting everything from national security to the stock market. By increasing the penetration of DG, the energy supply system is diversified, making a complete outage more improbable.
  - Future Supply. By reducing the reliance on fossil fuels, a country can guarantee sufficient energy in the future using renewable energy sources.
  - Support for Competition. Allowing more DG sites would potentially result in an increase in energy suppliers due to the lower start up cost. This would result in more competition between the suppliers, resulting in lower costs and better service for the consumer.

2.3.2 Implementation Issues

With the number of DG sites being connected to the grid set to increase, the resulting technical implications need to be considered. The energy supply network was not originally designed to allow generators to be connected within the distribution network causing a multitude of technical issues to arise:

- *Increased fault levels* - The effect of DG on network fault levels depends largely on the type of generator that is installed. Synchronous generators contribute higher fault levels than induction generators [25].

- *Voltage rise affect* - A rise in supply voltage can occur as the generators are connected to the same electrical point as the consumer loads. As most renewable energy source are intermittent and largely unpredictable in nature it is difficult to accurately predict the instantaneous power generation. Therefore a sudden rise in power generation would result in a rise in the supply voltage. The worst case scenario is when the load is at a minimum and the generation is at a maximum [26]. The voltage rise effect becomes more apparent when installing DG units in networks with a comparable line impedance.

- *Protection* - When interconnecting loads and generators within the distribution network, all components involved must be correctly protected against damage. The main considerations include [24]:
  - Protection of the generators against grid faults.
  - Protection of the distribution network against generator faults.
  - Hardware allowance for the added bidirectional power flow resulting from the intermittent nature of the generators.
  - Anti islanding, islanding can occur when a section of the power network which includes both loads and generators becomes electronically isolated from the rest of the distribution network. Islanding can only occur when the DG connected to the islanded section of the power network can sustain the connected loads.
- *Power quality* - Utility companies have strict specifications for the supply voltage, mainly for the voltage frequency, amplitude and harmonic content. Due to the smaller size of distributed generators, it is more difficult for them remain within the supply restrictions during large changes in the load demands. Reactive power is a major concern with damage to generators a possibility during sharp changes in the load.
- *Stability* - This is considered one of the minor issues at the moment as the distribution network can still be considered passive. As the proportion of supply shifts in favour of DG, the network stability analysis and damping capability is of major interest. This is due to the comparatively low inertia of the smaller generators. The effect on network stability depends largely on the level of penetration and generator type [27].

2.3.3 Popular DG Technologies

There are many DG technologies that require connection to the grid. The work completed is based on domestic scale DG, meaning only micro and small generators are considered. Micro generation is usually defined as anything with an electric capacity under 5 kW and small generation refers to generators outputting between 5 kW and 5 MW [21]. This section introduces a variety of devices that could require grid-connection if small scale domestic DG is going to play a major role in the future energy supply network.

2.3.3.1 Micro-combined Heat and Power (micro-CHP)

Micro-CHP can be defined as an energy conversion unit which simultaneously generates heat and power with an electric capacity under 15 kW [28]. The principle of micro-CHP is that by generating heat and power within the same unit, the overall efficiency can be increased. Micro-CHP installation units are a similar physical size as traditional heating systems, allowing easy installation [29]. The main types of micro-CHP are [30]:

- *Steam Turbines* - The steam produced in a boiler is pressurised and used to drive a high speed turbine. The mechanical power is then used to drive a generator, converting it into electrical power. This method is advantageous due to it's fuel flexibility, as any fuel can be used to produce the steam.
- *Traditional Piston Engines* - Most commonly powered by natural gas, internal combustion engines can be used the drive electrical generators and the produced heat can be used in forced air heating.
- *Combustion Turbines* - A well established electricity generation technology, with natural gas being the most common fuel. However, landfill or biogas fuels can be used. The high temperature exhaust gas can be coupled to a heat exchanger to heat water.
- *Fuel Cells* - There are two main types of fuel cell that are applicable to CHP:
  - Solid oxide fuel cell (SOFC). This particular type of fuel cell has a very high operating temperature, between 500°C and 1,000°C, making a heat energy recovery system vital in increasing overall system efficiency. This technology is currently in development and no CHP specific SOFC system is currently commercially available.
  - Proton exchange membrane (PEM) fuel cell. This fuel cell operates between temperature of 50°C and 100°C. The system can be incorporated into a household heating system to allow the fuel cell to operate continuously.
- *Stirling Engines* - This is a very old technology that is currently being revived to be included in CHP systems. Sometimes called the external combustion engine, a Stirling engine uses any temperature differential to expand and contract gas in a sealed configuration of chambers to create a mechanical movement [31]. This mechanical movement can be used to drive a generator and produce electricity. If the heat used to drive the Stirling engine would have otherwise been wasted, the overall efficiency of the energy system is increased.

As well as the systems stated above, any combination of heating system and electrical power generation that can be optimised as a complete system can be categorised as a CHP system.

The main issue associated with micro-CHP is the large initial cost, however, with more development it is believed that micro-CHP systems could become more financially viable, especially when the savings gained from subsequent fuel reductions are considered [32].

2.3.3.2 Micro Turbines

Micro turbines are very small high speed gas combustion turbines which typically rotate between 50,000 and 120,000 rpm [33]. Micro turbines are one of the larger technologies that can be considered as domestic DG, with unit power ratings ranging from 25 to 300 kW [34]. Advantages include fuel diversity, controllable power output, and low maintenance costs due to the popularity of air bearings in these systems.

A common configuration is to have a single shaft construction, with the same shaft connecting the compressor, the turbine, and the permanent magnet generator. This results in the generated AC power having a very high frequency, meaning an AC-DC-AC power electronic converter is normally used to allow grid connection [35].

2.3.3.3 Internal Combustion Engines

Internal combustion engines are one of the older DG technologies, having been used for a substantial amount of time as a means of commercial site backup power [36]. Typically fossil fuel based, these engines are usually connected directly to a synchronous or induction type generator, meaning direct connection with the utility can be achieved [37]. This configuration means the only hardware necessary for grid connection is a synchroniser, which ensures a zero phase angle between the generator voltage and the utility voltage before connection is allowed.

More modern systems have been proposed that allow the variable speed operation. The main aim of this configuration is to allow the internal combustion engine to operate at the optimal efficiency point for a given load, whilst the power rating and weight of the machine can also be reduced [38]. As a variable speed internal combustion engine solution will generate a variable frequency voltage, an AC-DC-AC power electronic converter is necessary to allow connection to the utility [39].

2.3.3.4 Small Wind Power

Wind power is the most common distributed generation technology that uses a renewable energy source. Many commercial products are available that can be installed on houses or small businesses. Domestic scale wind power can be split into three main categories [40]:

- Systems without power electronics. These systems most commonly use an induction generator with a squirrel cage rotor. To allow grid connection of the system, power must be limited by operating within 1-2% of a fixed speed. Speed control is accomplished using one of four techniques:
  - Pitch control. This method uses electronic actuators to change the aerodynamic efficiency of the turbine by rotating the blades [41]. The pitch mechanism adds both mechanical and control complexity to the wind turbine, increasing the unit cost. The typical mechanism used to rotate the turbine blades is a hydraulic system which requires additional maintenance.
  - Passive stall control. This technique uses turbine blades at a fixed pitch. However, the blades are aerodynamically designed to create turbulence on the side of the blade when the wind speed exceeds the operational wind speed [42]. This method reduces the need for moving parts and complicated control, reducing cost and increasing lifetime. However, further issues are introduced including increased blade design complexity and blade vibrations. These systems generally suffer from a power drop at really high wind speeds as the stall torque increases further than necessary.
  - Active stall control. This technique incorporates extra hardware, slowing the turbine down in high wind speeds to avoid power overshoots. A multitude of solutions have been investigated that alter the aerodynamic profile of the blades, including flaps and rotating tips [42]. An alternative method is to use a generator that is over-rated. This way the generator torque can be used to actively control the turbine speed [43]. The added cost generally means this system is only employed for larger units.
  - Active yaw control. This method simply changes the direction the turbine is facing [44]. The turbine can be rotated about the horizontal or vertical axes. By facing slightly away from the wind at high wind speeds, rotor speed can be controlled. This adds mechanical complexity to the structure of the system and introduces the need for an intelligent controller.

The induction generator used in these systems requires a source of reactive power to operate. This reactive power is supplied either from the grid or from capacitors connected to the generator [45]. As with all grid connected induction generators a soft starter mechanism is usually adopted to prevent inrush currents at start-up [46].

- Systems with partial power control using some power electronics, operating within ±30% of the optimal speed. Two different types of variable speed wind turbines are often investigated, both requiring wound rotor induction generators:

  - Doubly Fed Induction Generator (DFIG). The use of a DFIG allows an AC-DC-AC power converter to be used to control the rotor excitation which in turn changes the stator output power. The stator is connected directly to the utility system without the need for any reactive compensation device.
  - Variable rotor resistance. A variable resistance is connected to the rotor windings. By controlling this resistance, the system allows for the necessary deviation in speed. Whilst not providing any reactive power control, as with the DFIG, the variable rotor resistance method decreases maintenance as slip rings are not needed to transfer power to the rotor. Instead the rotor resistance is controlled using an opto-coupling module [47].

- Systems with full power control using power electronics. These systems typically use a synchronous generator, removing the gear box associated with induction generators [48]. The synchronous generator produces AC power with varying frequency and voltage, depending on the wind speed. An AC-DC-AC power electronic converter is used to convert the variable frequency power into grid compatible power, with DC link capacitors being used as a short term energy store. Maintenance issues are added as the rotor is normally constructed using electromagnets which are supplied excitation currents using brushes. The efficiency of the system is limited by the power converter efficiency. An advantage of this configuration is that the power electronics can be used to supply reactive power to the grid. Also the turbine can be allowed to rotate over a larger speed range, meaning more wind energy is captured by the system [49].

2.3.3.5 Photovoltaic (PV) Systems

Photovoltaic systems, constructed from semiconductor materials, utilise the photovoltaic effect to produce usable electricity. Solar radiation is used to excite electrons

resulting in movement from the valence energy band to the conduction energy band, this means the electrons are no longer bound to an atom and can now flow freely. This effect results in a build up of free electrons, enough to produce a usable potential difference between two electrodes. PV panels produce DC power, meaning an AC-DC power electronic converter is needed to convert this power into grid compatible AC power. Typical domestic installations require multiple PV panels to be connected together to create a usable power source. There have been many topologies used to connect multiple PV panels and power converters, the two main types being [45]:

- *Centralised Inverter* - This is the most simple PV connection method. The PV modules are connected in series or parallel. A DC link capacitor is then connected in parallel to the entire PV array. The output is then turned into AC power using an inverter. Classically, this system is connected to the utility using a grid frequency transformer, needed to boost the voltage and provide galvanic isolation. Due to modern PV panels producing a higher voltage, recently systems without transformers are becoming more attractive because of a higher achievable efficiency and lower weight [50].
- *High Frequency Isolation* - This topology includes a DC-AC inverter coupled with a DC-DC converter with grid isolation. A DC-DC converter is located between the link capacitor and the inverter. A high frequency transformer can be added within the DC-DC converter to achieve galvanic isolation. This high frequency transformer is much smaller than a grid frequency transformer.

PV panels have become one of the more popular DG technologies as the electricity generation process emits zero pollutants and there is a free abundant supply of solar radiation. The decommissioning process of silicon based PV panels results in construction waste only.

The main issue with PV systems is cost, but this will reduce as the technology becomes more popular. Further financial viability will be brought about by increases in system efficiency and generation capabilities that will reduce the payback time for PV installations. PV systems are also not entirely suitable in all climates as they require reasonable periods of sunlight to operate.

2.3.3.6 Energy Storage Solutions

Generally the energy produced from a renewable energy source can not be fully controlled or predicted, meaning power generation can not always match power consumption. The addition of energy storage within the distribution network allows surplus energy to be stored when generation exceeds consumption, which is in turn

used when consumption exceeds generation. There are currently many types of energy storage suitable for connection within the distribution network. The selection of energy storage technology is based the following criteria [51]:

- *Reliability* - The failure rate and maintenance requirements related to the storage solution meeting the expected energy demand consistently.
- *Efficiency* - The amount of loss experienced by the system as a whole, taking into account energy leakage during prolonged periods of energy storage.
- *Cost* - The initial outlay plus installation costs taking into account energy capacity and expected number of charge/discharge cycles.
- *Technical Maturity* - The availability of the technology and the amount of information available about prolonged usage.
- *Life Span* - The length of time the technology will fulfil energy storage demands.
- *Environmental Impact* - The effect of the technology on the environment, from the manufacturing process through to the eventual disposal process, including the installation and usage stages.

There are three main energy storage technologies that are suitable for domestic scale grid connection [52]:

- *Battery Energy Storage Systems* - Battery energy storage systems use electrochemical components to store potential energy as chemical energy. Many different chemicals and configurations can be used, with efficiency normally being between 60% and 80% [53]. The leading battery technologies for distributed generation energy storage are [54]:
  - Lead acid based. These batteries are the most mature type of rechargeable batteries, making them low in price and easy to install and maintain. Other salient features include a high attainable efficiency of 90% and a low self discharge rate of 2% per month. An issue associated with lead acid based batteries is a short lifetime, made shorter by non-ideal charge/discharge cycles.
  - Nickel based. These batteries have a high energy density and long lifetime, however low efficiency and high costs has restricted use.
  - Lithium based. Commonly used in personal electronics, these batteries exhibit high energy densities, excellent operating efficiencies and low self discharge rates of 1% [55]. Complex packaging, charge protection and thermal management result in high system costs.

All battery technologies require power electronics to convert the DC power produced by the battery into grid compatibly AC power. The power converters used must provide bi-directional power flow to allow energy to flow into and out of the batteries. The most basic applicable power converter is a bi-directional DC-AC inverter. If added flexibility is needed, alternate voltage levels of battery can be used by adding a DC-DC power converter at the battery connection point. This allows the DC link voltage to be boosted so that the inverter output voltage matches the grid voltage. To add galvanic isolation, a transformer can be added. A large grid frequency transformer can be added at the utility connection point, or a smaller high frequency transformer can be added within the DC-DC power converter [56].

With the increasing popularity and availability of electric vehicles, many investigations have been completed regarding the possible use of the batteries within electric vehicles being used as grid storage, looking at both technical and economical issues [57, 58].

- *Flywheel Energy Storage Systems* - When local power generation is greater than local power consumption, an electric motor is used to rotate a mass, the flywheel. Conversely, when local power generation is less than local power consumption, the kinetic energy of the flywheel is used to spin an electric generator. Many features associated with flywheel energy storage make them an attractive choice for distributed storage [59]:
  - High power density.
  - High efficiency.
  - No degradation by repeated use.
  - Low maintenance.
  - State of charge is simply a function of rotational speed.
  - Scalable, allowing use in any size of system.
  - Production process and materials are environmentally friendly.
  - Short recharge time.

  Whilst charging the flywheel is straight-forward, complications arise when converting the kinetic energy back into electrical energy. As the system is discharged, the shaft will slow down, causing the electricity generated to change in frequency. As a constant frequency AC power is need to allow grid connection, extra hardware and control must be added.

  One method is to include a mechanical clutch within the system. By altering the level of contact between the flywheel shaft and generator shaft, a constant

generator speed can be obtained. This method adds maintenance, control and efficiency issues.

A second method involves the addition of a power electronic interface between the motor/generator and the grid connection point. A bidirectional AC-DC-AC power electronic converter can be used, having two operation modes [60]:

- Charging mode. In this mode the power electronic converter is used to convert grid power into variable frequency AC power, which drives the motor to store kinetic energy in the flywheel.
- Discharge mode. In this mode the power electronic converter is used to convert the variable frequency AC power produced by the generator into grid compatible AC power.

The power electronic interface method is favoured due to the variable speed operation of the electrical machine. The efficiency of the power electronic interface limits the overall system efficiency.

Other methods have been implemented which incorporate electrical and mechanical components, such as the use of a doubly fed induction generator. This allows the power rating of the power electronics to be reduced, however, introduces the use of brushes and slip rings.

- *Super Capacitor Energy Storage Systems* - Super capacitor technology has now advanced to become a legitimate alternative to battery based energy storage systems [61]. Salient characteristics of super capacitors that make them attractive for distributed energy storage are [62]:
  - High power density.
  - Fast simple charging.
  - Long life.

  The super capacitor can be connected to the DC side of a bi-directional AC-DC power converter. This eliminates the need for the voltage to be boosted, either by a DC-DC converter or transformer. The bi-directional AC-DC power converter operates as a rectifier during the charging process and an inverter during the discharge process.

2.4 Power Electronics Interface

Section 2.3.3 introduces a variety of DG technologies that are suitable for domestic scale grid-connected installations. The majority of technologies require a power electronics interface to convert the generated power into a suitable AC power for

grid-connection. That is, all power that is connected to the UK grid supply must have a frequency of 50 Hz and RMS voltage of 240 V (single-phase).

The most common power electronics converter module required is a DC-AC inverter. All DC power sources, such as PV panels, batteries and fuel cells use an inverter for grid-connection. As well as DC power sources, many AC power sources, including small wind power and micro turbines, are now favouring fully rated back to back rectifier/inverter topologies. This change is due to the reduced cost of power electronic components.

This increased need for DC-AC inverters shaped the focus of this work, along with the fact that only small scale domestic installations are to be considered. This means the project work completed is focused on single-phase grid-connected DC-AC inverters.

2.5 Loss Of Mains (LOM)

As stated in Section 2.3.2 islanding is a major technical issue associated with the increased penetration of DG. To allow a larger majority of the generated power to be used, grid connected DG units allow power to flow into the utility network. If the utility supply is lost, due to a fault or scheduled maintenance, the DG unit can form a power island. A power island can only form if the connected power generation is large enough to maintain the connected loads.

Figure 2.1 shows how a power island can exist within the distribution network. The generators are able to sustain the supply to the loads within the power island which is isolated from the grid. IEEE Std. 1547 defines a power island as a portion of the

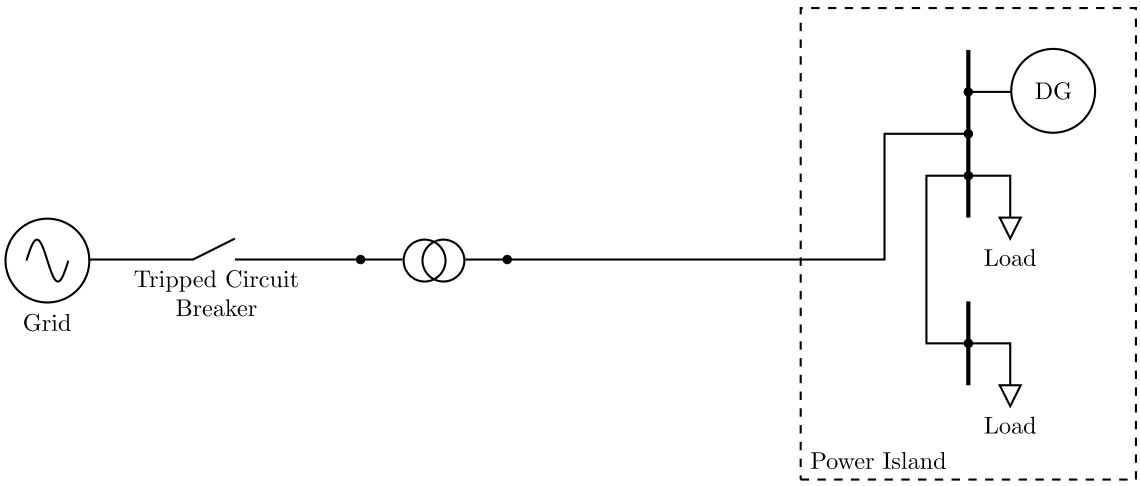

Figure 2.1: Island definition diagram

energy supply network that remains energised whilst electronically separated from the rest of the power system [1].

The main implications associated with power islands are [63–66]:

- *Safety* - Customers and line workers can be placed in danger if a portion of the supply network remains energised when it is thought to be inactive.
- *Power quality* - Fluctuations in the local network voltage may occur which could damage equipment.
- *Asynchronous reconnection* - During islanded operation, the local power network can drift in phase with respect to the utility, if the utility supply is re-established whilst a phase difference exists, large voltages and currents can occur, damaging hardware.
- *Inadequate grounding* - Depending on the type of DG connection, satisfactory grounding is not always provided during islanded operation.

These negative factors have caused the majority of utility companies to include within connection standards, the requirement that any power electronics interface used to connect DG units within the distribution network must include a robust anti-islanding routine [67, 68]. IEEE connection standards state that the maximum delay between the occurrence of an island and the disconnection of the DG unit is 2 seconds [69]. To prevent an islanding situation occurring, the control system must detect a loss of mains (LOM) condition quickly and accurately.

Many LOM detection systems have been proposed and evaluated, with a variety of schemes implemented in currently available grid connected inverters [63]. Islanding detection systems require further research so that an industrial standard can be developed. The main categories, including several examples, of LOM detection schemes are shown in Figure 2.2 [70].

To compare the different strategies a number of metrics are employed. The two most important metrics are, the size of the none detection zone (NDZ), and the detection delay.

The none detection zone is a collection of operating conditions that would result in a LOM event going undetected [71]. These operating conditions are defined by the amount of active and reactive power mismatch between local generation and local consumption, in other words, the amount of power exchange with the utility. The most difficult situation for LOM detection is the balanced power operating condition, where local power generation is equal to local power consumption. During this scenario there is little or no power exchange with the utility, meaning that only very small changes in the measured parameters will occur during a LOM event. As

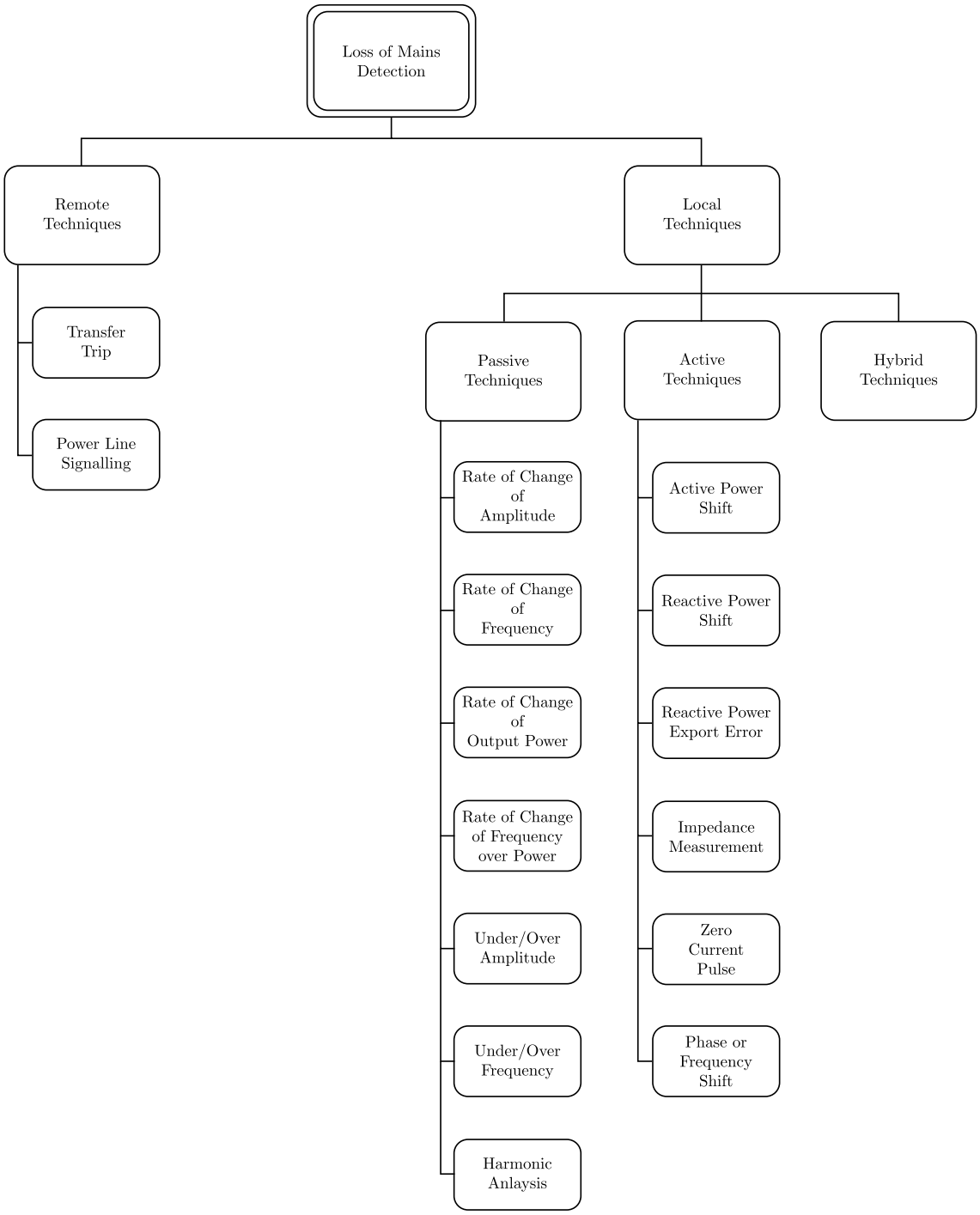

Figure 2.2: Categories of LOM detection techniques, including examples

power exchange with the utility increases, the resultant parameter change experienced during a LOM event will increase, making the LOM event easier to detect. Therefore, a NDZ is usually a collection of operating conditions around the balanced power scenario. $\Delta P\%$ and $\Delta Q\%$ are used to represent the local active and reactive power mismatch respectively. An example NDZ graph is shown in Figure 2.3. The rectangle encloses the operating conditions which would result in a LOM event going undetected. This particular NDZ graph demonstrates that a LOM event would only

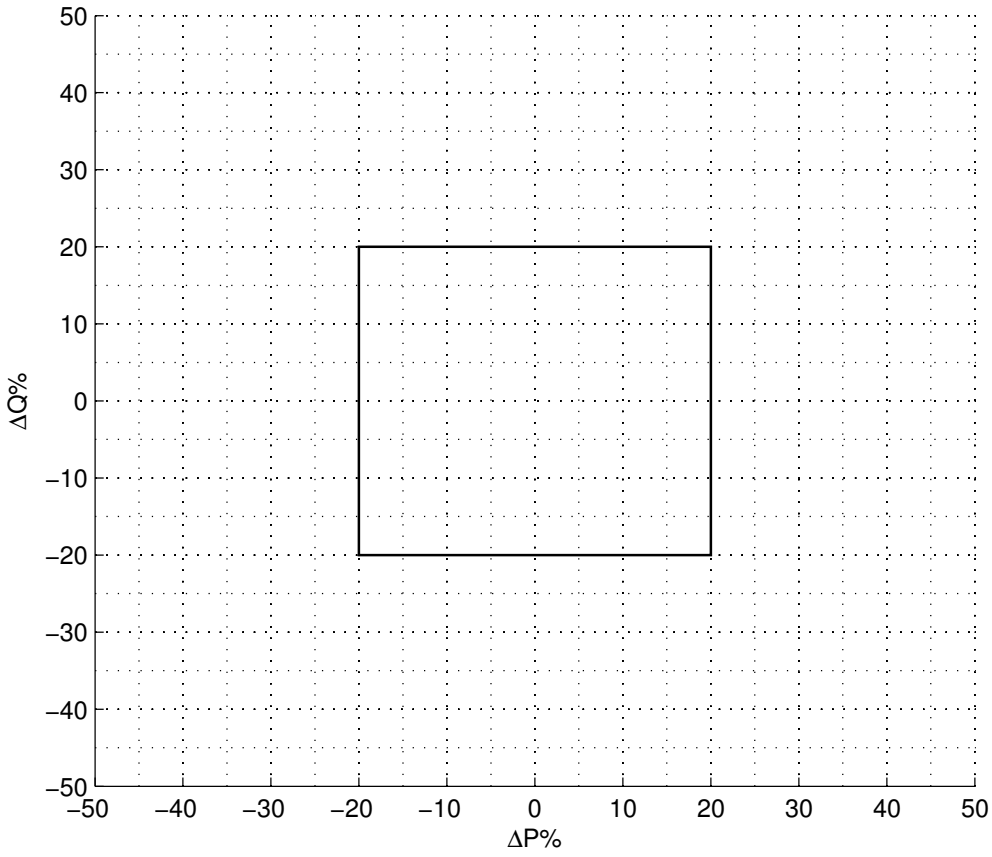

Figure 2.3: An example NDZ graph

be detected when a local real or reactive power mismatch larger than ±20% exists.

The detection delay is the amount of time between a LOM event occurring and it being detected by the system.

Other considerations include: the effect on power utilisation, detrimental effects caused by any inverter output change, the probability of a incorrect LOM signal, and how different LOM detection schemes would interact when implemented on devices within the same power network.

2.5.1 Remote Techniques

Remote LOM detection techniques rely upon a communication link between the utility and the grid connected inverter. These systems are considered very reliable with the communication method being the only source of error. A range of systems have been developed with the two most common being:

- *Transfer Trip* - This method involves consistently monitoring the status of circuit breakers and switches within the power network. A management system controls connections within the network to ensure no part becomes islanded. A dependable communication path between the controller, sensors and actuators is required for reliable operation. Multiple hardware improvements would be required and success would be reliant on an adequate number of sensors [72].

- *Data Line Communication* - Power line signalling relies on a high frequency signal being transmitted on the grid by the utility. DG units can detect this high frequency component relatively easily. A LOM situation is detected when the high frequency component is no longer received by the DG unit. This system requires little additional hardware to the transmission network and is suitable for multiple DG units connected to the same distribution network [73]. As with any power line communication, the signal injected into the power transmission network can have power quality and electromagnetic radiation issues [74].

To employ a communication system across the entire power supply network would require a large investment from the utility companies. Therefore, remote techniques are generally regarded as too expensive to implement so are quite often ignored [63, 75].

2.5.2 Local Techniques

Local techniques are based on measurements taken at the point of DG unit connection. No additional hardware is required by the utility on the transmission network. Local techniques include three main subsections, passive, active, and hybrid.

2.5.2.1 Passive Techniques

Passive techniques are based solely on parameters measured at the point of DG connection [76]. Analysis takes place with the result being compared to a preset threshold.

Some passive systems use the fact that when the DG unit is grid connected, the power network as a whole will have a much larger moment of inertia and generation capacity. This means that when a LOM even occurs the drop in these two attributes will cause measured network parameters to change. The following detection methods aim to detect this change in network parameters:

- *Rate of Change of Voltage and Frequency (ROCOV/ROCOF)* - In this scheme the voltage at the point of DG unit connection is measured and the amplitude and frequency are calculated, normally by the inverter controller. The rate at which these two parameters change is also calculated. During development the system is tested, and an acceptable grid connected range for the two rates is set using thresholds. The system works on the principle that, due to the lower generation capacity when islanded, a local load change will result in a higher rate of change of frequency or voltage [77].

- *Rate of change of power* - This is a well established technique, developed decades ago. In this method the output power of the DG generator is monitored. It works on the principle that the rate of change of power will be much larger for a given load change during islanded operation [78].

- *Rate of change of frequency over power* - This technique combines the rate of change in frequency and the rate of change in power to produce a new factor (df/dP). This new factor is said to be more sensitive during balanced load operation [79]. This theoretically allows the thresholds to be chosen more conservatively, resulting in fewer false trips.

- *Under/Over Voltage Amplitude and Frequency* - One of the most simple and widely used island detection techniques [80]. In this method the voltage at the point of DG unit connection is constantly measured. Routines can be implemented within the inverter control code that calculate the voltage RMS and frequency values. An acceptable range for the supply voltage amplitude and frequency is supplied by the utility. If the stiff grid signal is not present, the calculated values can stray beyond the acceptable range, signalling that a LOM situation has occurred.

Some passive detection systems aim to determine when a LOM event has occurred by monitoring parameters that would change due to a rise in impedance. It is assumed that the grid has much lower impedance than the DG units connected to the same network. Thus, when a LOM event occurs, the impedance of the system rises substantially. This causes the harmonic content to change significantly. This is especially true for inverter based distributed generation units [81]. Different methods can be used to gain the spectral information, the most popular being:

- The discrete Fourier transform (DFT).

- The windowed Fourier transform (WFT).

- The discrete wavelet transform (DWT).

The spectral information is then analysed and a decision algorithm signals when a LOM event has occurred.

As passive schemes rely completely on pre-set thresholds, the existence of a NDZ is a common issue [82]. A compromise is introduced when setting the LOM thresholds, with the NDZ size and the probability of an incorrect LOM signal being the two competing factors [83]. Passive schemes often exhibit a short detection time, however, the existence of a NDZ around the balanced load operation point is unacceptable according to grid connection standards.

2.5.2.2 Active Techniques

Active Techniques introduce some kind of disturbance within the output power of the inverter. The effect that this has on the measured parameters is used to signal whether or not the inverter is still connected to the grid [84]. Active techniques rely upon the utility maintaining the voltage at the point of DG unit connection, meaning any disturbance introduced can only affect this voltage when the system has become islanded. Six of the more commonly reported active techniques are:

- *Active Power Shift* - This method periodically changes the amplitude of the inverter output current. This alteration in active power output will only affect the voltage at the DG unit connection point if the utility is not connected.
- *Reactive Power Shift* - This scheme involves periodically changing the inverter output current phase, so that the system can never stay at the balanced power operating point for an extended period of time. If the utility is not connected, the change in ouput current will affect the voltage at the point of DG unit connection.
- *Reactive power export error* - In this scheme the DG unit deliberately exports reactive power. The reactive power at the DG connection point can only be maintained whilst the grid is connected. An island situation is detected when the reactive power deviates from the set value. This technique is very reliable but quite slow, so is often used as a backup system [85].
- *Impedance detection* - These schemes are similar to some passive methods in that they identify LOM by detecting a rise in network impedance. The impedance rise is normally detected using a technique belonging to one of the following categories:
  - Direct methods, these methods periodically connect a shunt inductor or resistor across the DG unit connection points, to calculate the impedance of the connected power network. An example of this type of project is described in [85].

  - Indirect methods using noise injection. There are various schemes which add a high frequency component to the inverter current demand signal. The same high frequency component in the connection point voltage is isolated using a digital filter or Fourier analysis. As the impedance of the utility is very low, the high frequency voltage component will have a small magnitude whilst the system is grid connected. The rise in impedance that occurs during a LOM event results in the high frequency current component becoming more visible in the measured voltage. An example of noise injection, is 2^{nd} harmonic injection, where a 100 Hz component is added to the inverter current demand signal, similar to [86].

- *Zero Current Pulse* - This method involves including a short period of zero current within the inverter output current. The connection point voltage is measured and the derivative is constantly calculated. Only when the system becomes islanded will the zero current pulse cause a voltage change. This in turn produces a large derivative value, which is used to signal that a LOM event has occurred.

- *Phase or frequency shift methods* - These methods output power with a slight shift with regards to the grid signal. When the stiff grid signal is not present, the power network will follow the output from the DG unit. This would then trip the under/over frequency protection [87].

Active techniques are generally regarded as more robust than passive techniques as higher success rates at balanced load conditions are achievable [88]. The main negative point associated with active techniques is the disturbance that is deliberately added to the inverter output.

2.5.2.3 Hybrid Techniques

Hybrid schemes utilise both passive detection and active detection. Passive detection is used to flag when there might be an island situation. Then an active technique is used to verify if islanding has in fact taken place. This means most island situations are detected without unnecessarily introducing the power quality issues associated with active techniques [89]. The sequential nature of the two methods means long detection times can be expected [63].

2.6 Laboratory Test Equipment

The standard laboratory test bench for testing island detection routines is shown in Figure 2.4. This standard test bench is stipulated in IEEE standard 1547.1 as the most suitable method for fully testing LOM detection techniques [1]. The DC supply, inverter, filter, and controller mimic a connected DG installation including associated power electronics and control. A grid transformer allows power to be exchanged with the utility. The local network load is represented by a 50 Hz resonant RLC load. The connection point between the utility, the inverter, and the local load is the point of common coupling (PCC).

The laboratory setup has been specifically designed to test LOM detection systems under the full range of operating conditions, including the worst case scenario i.e. the aforementioned balanced load. As the local power consumption is known, the inverter output current can be altered in both phase and magnitude so that LOM detection schemes can be tested during differing levels of active and reactive power mismatch, $\Delta P\%$ and $\Delta Q\%$ respectively.

To further test the LOM detection techniques, the RLC load is resonant at 50 Hz. This means the voltage and current will remain in phase when a 50 Hz supply is connected. Hence reducing the likelihood that the system will frequency drift or become unstable when the utility supply is lost as the control system is designed to run at unity power factor.

The controller only has two sensory inputs, the measured voltage at the point of common coupling, V_{PCC}, and the inverter output current, I_{INV}. These sensors are required for standard inverter control. No additional hardware is required for any of the LOM detection schemes that are investigated in this work.

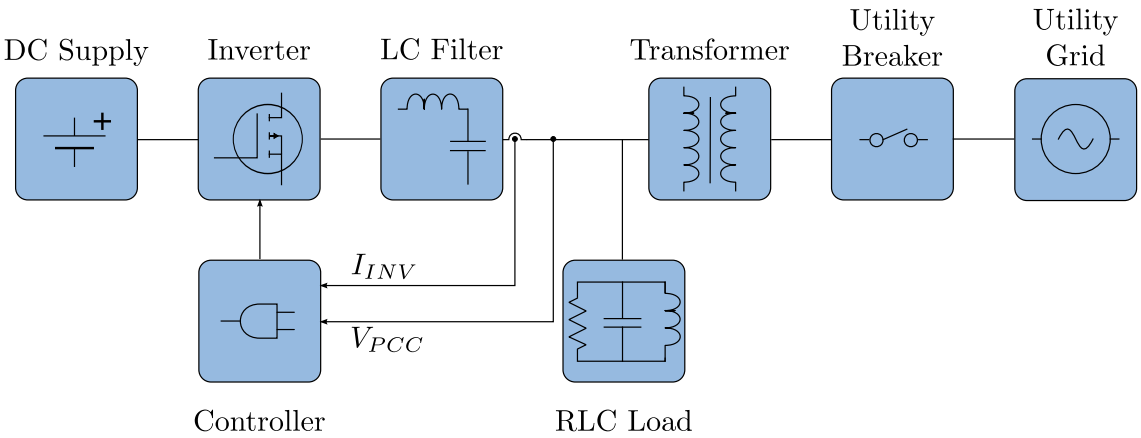

Figure 2.4: Standard laboratory test bench for testing island detection routines

Chapter 3

Scaled Power Laboratory Test Bench

This chapter describes the development and construction of a scaled power laboratory test bench. The test bench is fully specified, along with the reasoning behind various decisions that were made. The individual hardware components are briefly introduced to allow a full understanding of the set-up operation.

A Matlab/Simulink simulation model is then briefly described, which has been developed along side the laboratory test bench to accurately mimic the constructed hardware.

The control structure is explained fully, including experimental and simulation operation demonstrations, showing both the likeness of the model to the hardware set-up and how a LOM event can result in the formation of a power island.

3.1 Laboratory Test Bench

A scaled power laboratory test bench was designed and constructed to provide a suitable environment to test LOM detection techniques experimentally. The advantages of using a scaled power set-up over a fully rated set-up are:

- *Safety* - Working at a lower power level requires less voltage and fewer safety precautions to be considered when constructing the working environment.
- *Cost* - Using hardware devices with lower power ratings is generally less costly, this also allows for any early system failures to be repaired with minimal impact on the overall project budget.

- *Proof of concept* - The developed scaled power laboratory test bench can be used to accurately develop, evaluate and most importantly compare different LOM detection techniques.

To produce a scaled power laboratory test bench which allows the inverter to match the utility voltage, a 40:1 step down transformer was used as the connection to the utility. This allows fully tested and available hardware to be used to produce a 6V RMS inverter output voltage.

The circuit layout for the scaled power laboratory test bench is shown in Figure 3.1. The main hardware modules, which are described in more detail in Section 3.2, are:

- *Inverter board* - This H bridge, Mosfet based, inverter is used to convert DC power into AC power.
- *DSP* - This floating point, 150 MHz, digital signal controller is used for both inverter control and LOM detection.
- *Line filter* - This LC lowpass filter reduces the switching signal component in the inverter output power.

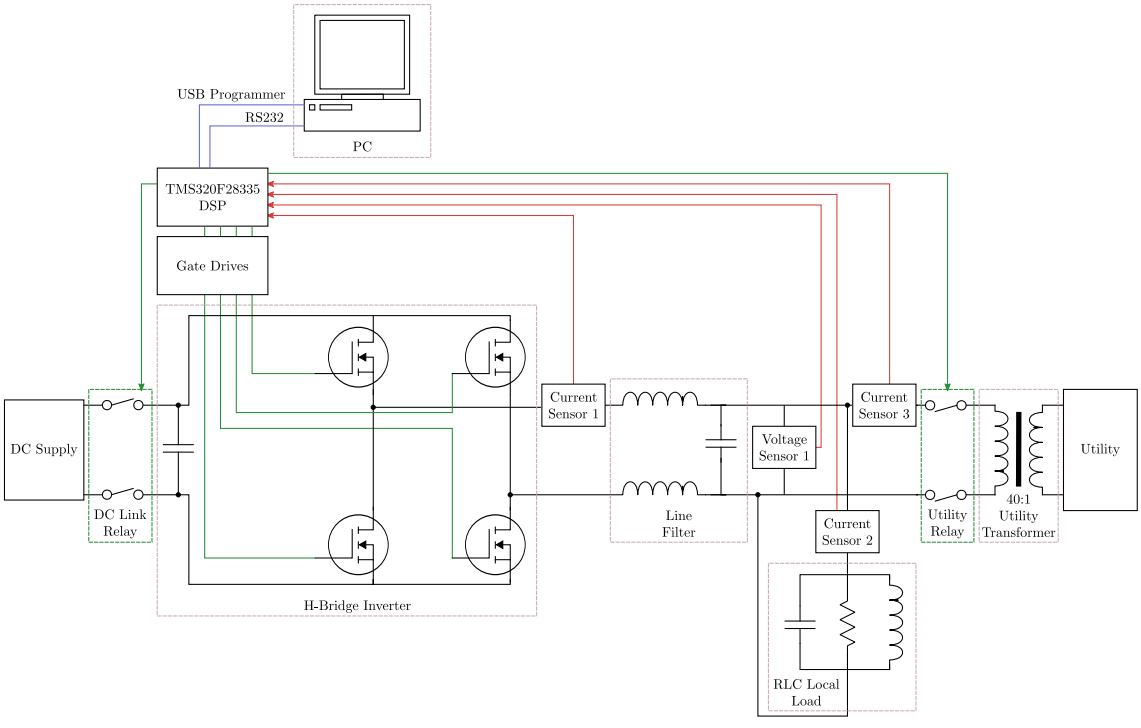

Figure 3.1: Scaled power laboratory test bench

- *RLC load* - The RLC load is the local power consumption, designed to be resonant at 50 Hz.
- *PC connection* - The connection with a PC is used to program the DSP,via the USB link, and to continuously exchange control and measurement parameters, via the RS-232 communications interface.

3.2 Hardware

Figure 3.2 shows the constructed laboratory test bench. An oscilloscope was used throughout the early stages of the installation to allow sensors to be accurately configured and the general operation monitored.

The intention of this section is to briefly introduce each of the main hardware components chosen, outlining key attributes and operational features.

3.2.1 Inverter Board

The inverter board used in the scaled power laboratory test bench is shown in Figure 3.3. The board is a standard project board designed at Newcastle University. The main features are:

- *Two 3 leg mosfet inverters* - The board includes two three leg mosfet based inverters using seperate DC links. Only two legs of one of the inverters are needed for this project.

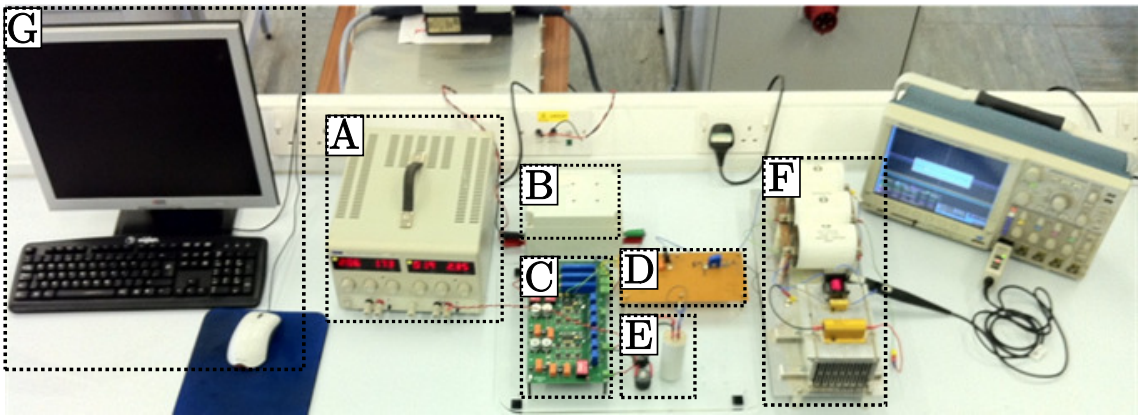

Figure 3.2: Photograph of the scaled power laboratory test bench. A, DC supply; B, isolation transformer with grid connection; C, power inverter and DSP; D, utility breaker; E, LC filter; F, local RLC load; G, PC

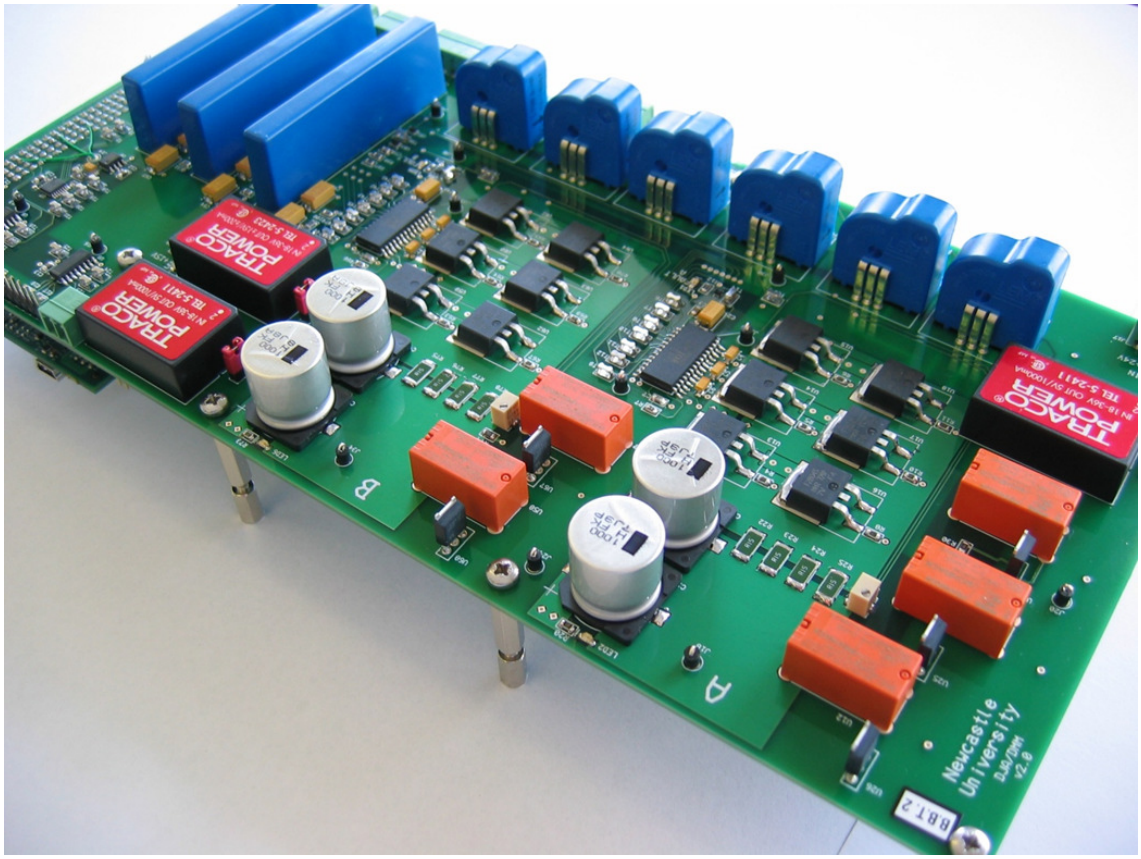

Figure 3.3: Inverter Board

- *6 on board current sensors* - A current sensor is connected between the mid point of each inverter leg and the output socket. Only one of these current sensors is used in this set-up. It is used to measure the inverter output current I_{INV}.
- *3 on board voltage sensors* - Isolated amplifiers are used to measure external voltage levels. One of these is used in this project to measure the voltage at the point of common coupling ,V_{PCC}.
- *DC link relays* - DC link relays are included to allow the input power to be turned off at any time using the DSP.
- *Direct DSP interface* - The DSP is directly connected to the underside of the inverter board, allowing control signals, PWM signals, and sensor output levels to be transferred.

The DC link voltage used in this project is 24 Volts, supplied by a standard 280 Watts DC laboratory bench supply.

3.2.2 DSP

The DSP used to control and monitor the scaled power laboratory test bench is a Texas Instruments F28335 eZdsp evaluation board. The salient features that resulted in the inclusion of this particular DSP evaluation board are:

- *A high clock speed* - The 150 MHz clock speed allows complex routines to be completed quickly.
- *Off-chip memory* - 128 KB × 16 off-chip SRAM modules for data storage.
- *RS-232 interface* - Allows the set-up to be controlled and monitored using a safe communications interface. Using the RS-232 communications link instead of the USB JTAG connection allows the controllable operations to be limited, reducing the likelihood that a communications fault could cause a dangerous situation.
- *Code Composer Studio* - Development environment, supplied with the DSP, which allows programming and real time debugging of control code.

3.2.3 LC Line Filter

The low-pass analogue line filter is connected to the inverter output to remove the high frequency switching component from the inverter output power. An LC filter was designed to have a cut-off frequency, f_c, of 1 kHz. Equation 3.1 is the equation for the cut-off frequency of a series connected LC filter.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{3.1}$$

The inductance, L, was chosen at the highest readily available value of 940 μH, using two 470 μH inductors connected at either side of the capacitor, this allows the value of the capacitor used to be kept as low as possible. Equation 3.1 was rearranged to give Equation 3.2 to allow the capacitor value to be calculated.

$$C = \frac{\left(\frac{1}{2\pi f_c}\right)^2}{L} \tag{3.2}$$

The resultant capacitor value is 26 μF. To test that the values obtained were correct, the circuit was created in the PSpice simulation environment, a full frequency sweep was carried out to obtain a Bode plot. The Bode plot for the LC filter is shown in Figure 3.4. It demonstrates that the gain of the filter decreases substantially at 1 kHz, meaning any higher frequencies within the inverter output power will be greatly diminished in amplitude.

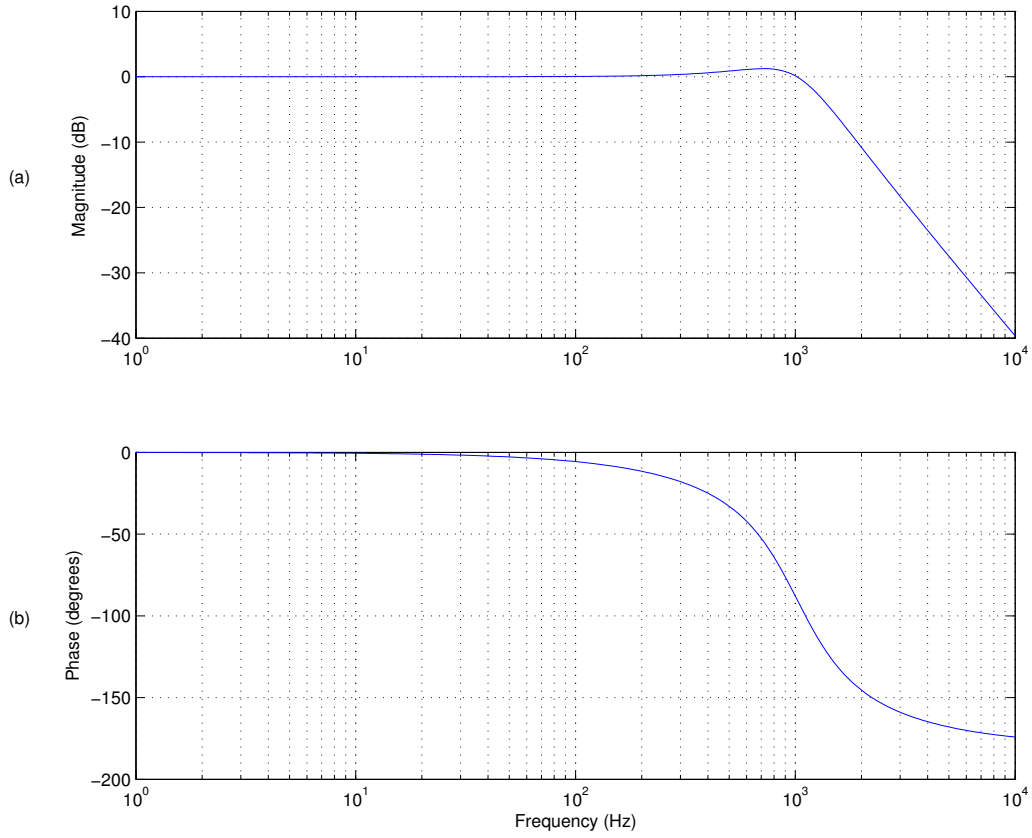

Figure 3.4: Bode plot for LC filter

3.2.4 Resonant RLC Load

The local network load is represented by a parallel RLC load, designed to be resonant at 50 Hz. This means the voltage and current remain in phase when a 50 Hz supply is connected. Hence, reducing the likelihood that the system will frequency drift or become unstable when the utility supply is lost as the control system is designed to run at unity power factor. The load is designed like this to provide a laboratory test bench which represents the hardest scenario for LOM detection with only small parameter changes occurring during a LOM event.

IEEE standard 929-2000 states that the quality factor, Q, of the resonant RLC load must be set at 2.5 or lower [90], where Q can be calculated using equation 3.3.

$$Q = R\sqrt{\frac{C}{L}} \tag{3.3}$$

Equation 3.4 can be arranged to make L the subject, by substituting this into equation 3.3, the equation 3.5 is derived.

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{3.4}$$

$$L = \frac{R}{2\pi f Q} \tag{3.5}$$

Choosing R to be 10.7 ohms, Q to be 2.3 and f to be 50 Hz, equation 3.5 is used to calculate the inductance, L, to be 0.0145 H. The calculated inductance is used with equation 3.3 to calculate the capacitance, C, to be 699 μF.

To test the resonance of the calculated values the circuit was simulated in PSpice to produce the Bode plot shown in Figure 3.5. The most important feature of the Bode plot is the required zero phase shift at 50 Hz, reducing the likelihood of substantial frequency drift when operating with unity power at 50 Hz. The constant gain of the load around the 50 Hz operational point means any slight change in frequency will not result in an amplitude change. These two factors confirm that the constructed load is ideally suited for providing the worst case scenario to test LOM detection routines.

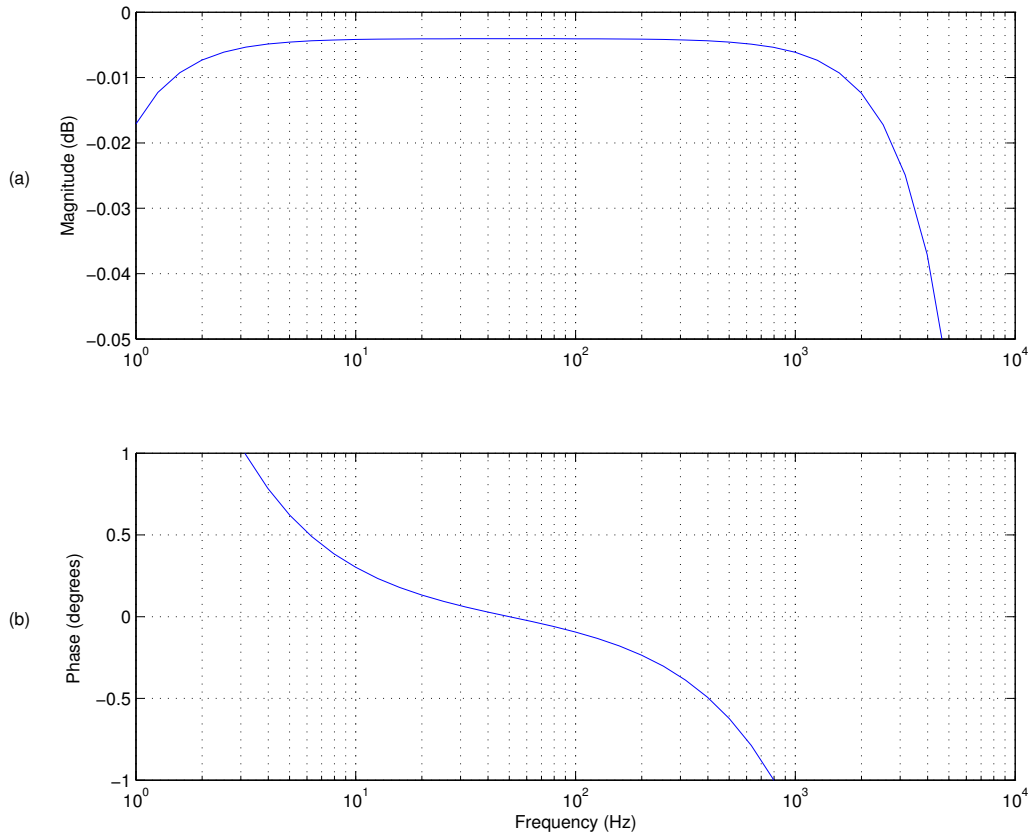

Figure 3.5: Bode plot for RLC load

3.2.5 Labview Control Panel

The constructed Labview control panel is shown in Figure 3.6. It is used as a safe way of communicating with the DSP during operation, both to upload control information and to download system parameter measurements. The communications link used is the RS-232 link. The main control data that is uploaded to the DSP includes:

- *Relay control* - The DC link relays and the utility relays are controlled using several two-way buttons.
- *Gate drive enable* - This allows the gate drive chips to be activated or deactivated.
- *Active and reactive power mismatch* - Both the $\Delta P\%$ and $\Delta Q\%$ are dictated by a drop down box on the Labview panel.
- *Island routine initiation* - A standard LOM detection test, detailed in Chapter 4, is started by the press of a button on the Labview control panel.

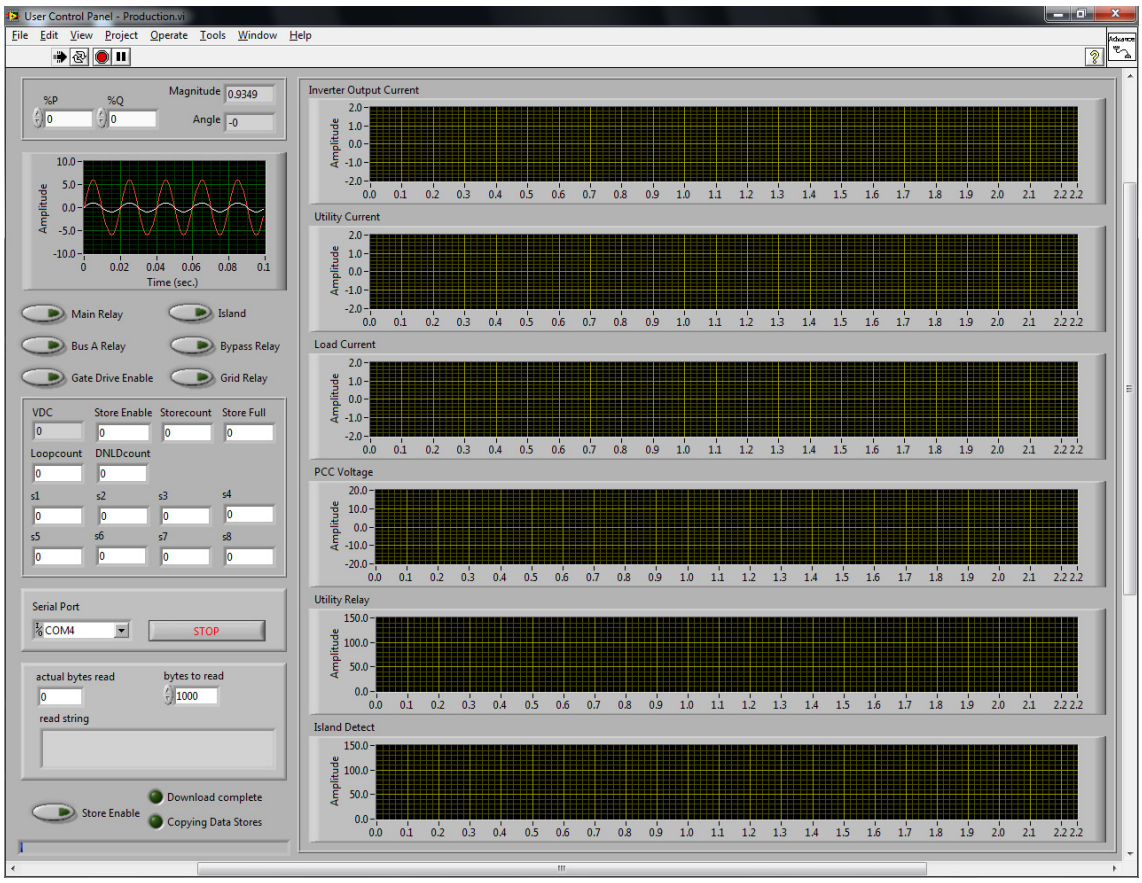

Figure 3.6: Labview control panel

The information that is downloaded from the DSP is displayed using a waveform plotter during the download process along with status indicators relating to the download progress. These quick data indicators are used to determine if the data is usable before any post processing is completed. The Labview program copies the data into created text files to allow the data to be imported into Matlab for post processing and presentation.

The data that is downloaded from the DSP is initially stored in external SRAM memory, mentioned in Section 3.2.2, located on the DSP development board. This allows data to be sampled and stored on the DSP development board at a high sampling rate before then being downloaded to the PC at the much slower data transfer rate when the storage routine is complete. 8 data storage arrays, 2 KB in length, are initialised on the external SRAM. The standard LOM detection test, detailed in Chapter 4, has a duration of 2.2 seconds. To allow the 8 data stores to be filled in 2.2 seconds data is sampled every 1.1 mS, meaning the sample rate is 909.1 Hz.

3.3 Simulink Model

The Simulink model of the laboratory test bench is shown in Figure 3.7. The SimPowerSystems tool box is used to simulate the power devices and sensors. The model includes the same hardware components that are used in the laboratory test bench, with the component parameters being modified to give a close match with the hardware set-up. The simulation environment was created at the same time as the hardware laboratory test bench to facilitate quick verification of the model results. The s-function control block has been implemented so as to allow C language control code to be compiled and executed, this allows for code to be developed using

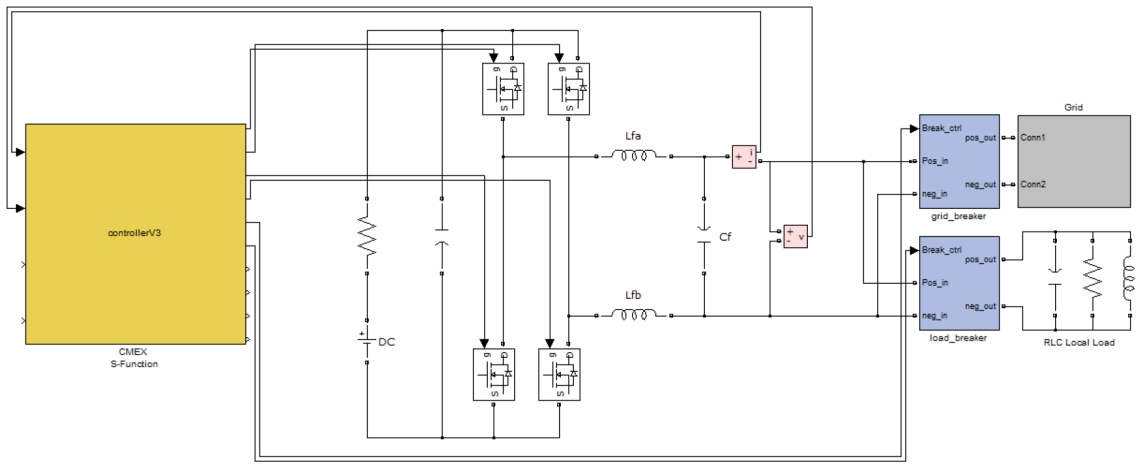

Figure 3.7: Simulink model of the laboratory test bench

the model before being copied over to the DSP used in the hardware implementation. The grid connection block comprises of a 50 Hz voltage supply with a parallel connected load resistor.

3.4 Control Structure

This section explains the power control structure that has been implemented both in the simulation model and on the DSP board. When the system operates in grid connected mode, the utility can be considered to be in control of the voltage at the point of common coupling, V_{PCC}, which in turn dictates the output voltage of the inverter, V_{INV}. The inverter itself operates with a closed loop current control structure. Using the V_{PCC} measurement as a reference, the phase and magnitude of the demanded current can be specified in such a way to accurately control the real and reactive power output of the inverter. As the rated power of the local load is known, it is possible to operate under the full range of real and reactive power mismatches, $\Delta P\%$ and $\Delta Q\%$, respectively. The full control structure is shown in Figure 3.8.

3.4.1 Implemented PLL

The phase locked loop is an integral part of the control system as it provides the voltage phase reference needed to control the power flow. It is imperative that the implemented PLL is robust enough to remain stable during utility disturbances. The implemented PLL is shown in Figure 3.9. This classical structure single phase PLL, presented in [91], is known as a power phase locked loop, p-PLL. The name originates from the operation of the phase detect method which has similarities

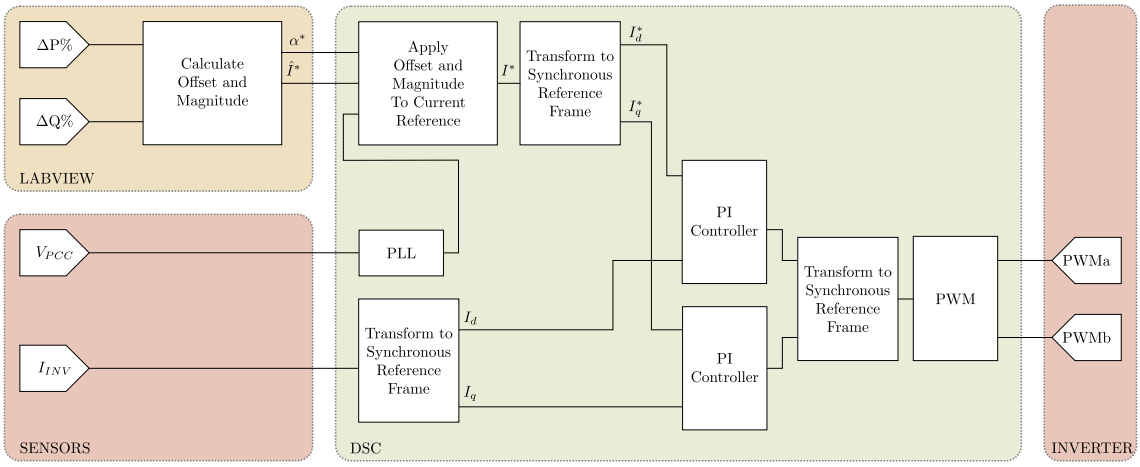

Figure 3.8: Full power control structure diagram

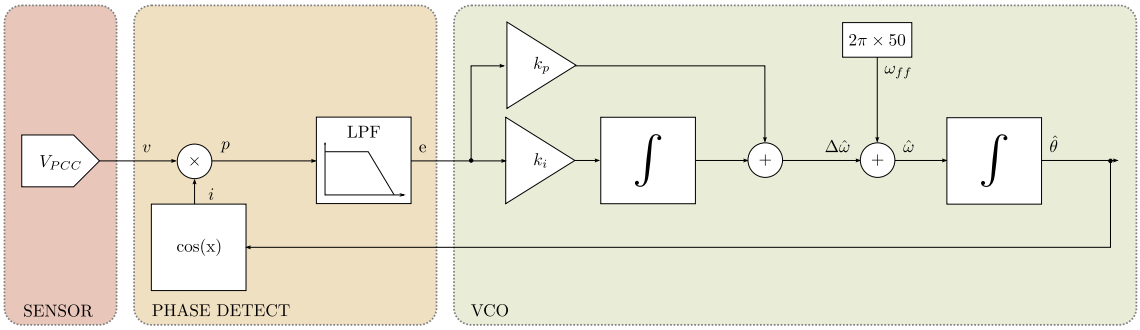

Figure 3.9: PLL block diagram

to an instantaneous power calculation. The input voltage, v, is multiplied by a created signal, i, which inherits the output phase of the PLL, $\hat{\theta}$, as per equation 3.6. Assuming a sinusoidal input voltage with the form $V \sin\theta$, equation 3.6 can be expanded to produce equation 3.7.

$$p = v \times \cos(\hat{\theta}) \tag{3.6}$$

$$p = V \sin(\theta) \times \cos(\hat{\theta}) \tag{3.7}$$

or

$$p = \frac{V}{2}[\sin(\theta - \hat{\theta}) + \sin(\theta + \hat{\theta})] \tag{3.8}$$

Given that $\theta = \omega t + \varphi$ and $\hat{\theta} = \hat{\omega} t + \hat{\varphi}$ and realising that under normal operation $\omega t \cong \hat{\omega} t$, p can be expressed as

$$p = \frac{V}{2}[\sin(\varphi - \hat{\varphi}) + \sin(2\omega t + \varphi + \hat{\varphi})] \tag{3.9}$$

The low pass filter is used to remove the high frequency component of p which can be seen to have a frequency of around twice the fundamental. The digital filter is a 13^{th} order finite input response (FIR) filter with a cutoff frequency of 50Hz. Assuming a small phase difference, $\varphi - \hat{\varphi}$, allows the sine function to be considered linear, hence giving the phase error, e, to be

$$e \cong \frac{V}{2}(\varphi - \hat{\varphi}) \tag{3.10}$$

The determined error is fed into a PI control loop which increases or decreases the angular velocity, $\hat{\omega}$, of the voltage controlled oscillator, VCO, to achieve a zero phase error. The angular velocity is modified by adding the PI output value, $\Delta\hat{\omega}$, to the

fundamental frequency angular velocity, ω_{ff}. The p-PLL was tested experimentally to produce the results shown in Figure 3.10. The PLL was deliberately turned on at a point where the internal VCO was π radians out of phase with the measured voltage, V_{PCC}, as this represents a worst case scenario in terms of phase error. The small oscillations present in the steady state phase error are present due to the limited order of the low pass filter, however, these are considered small enough to be absorbed by the control system.

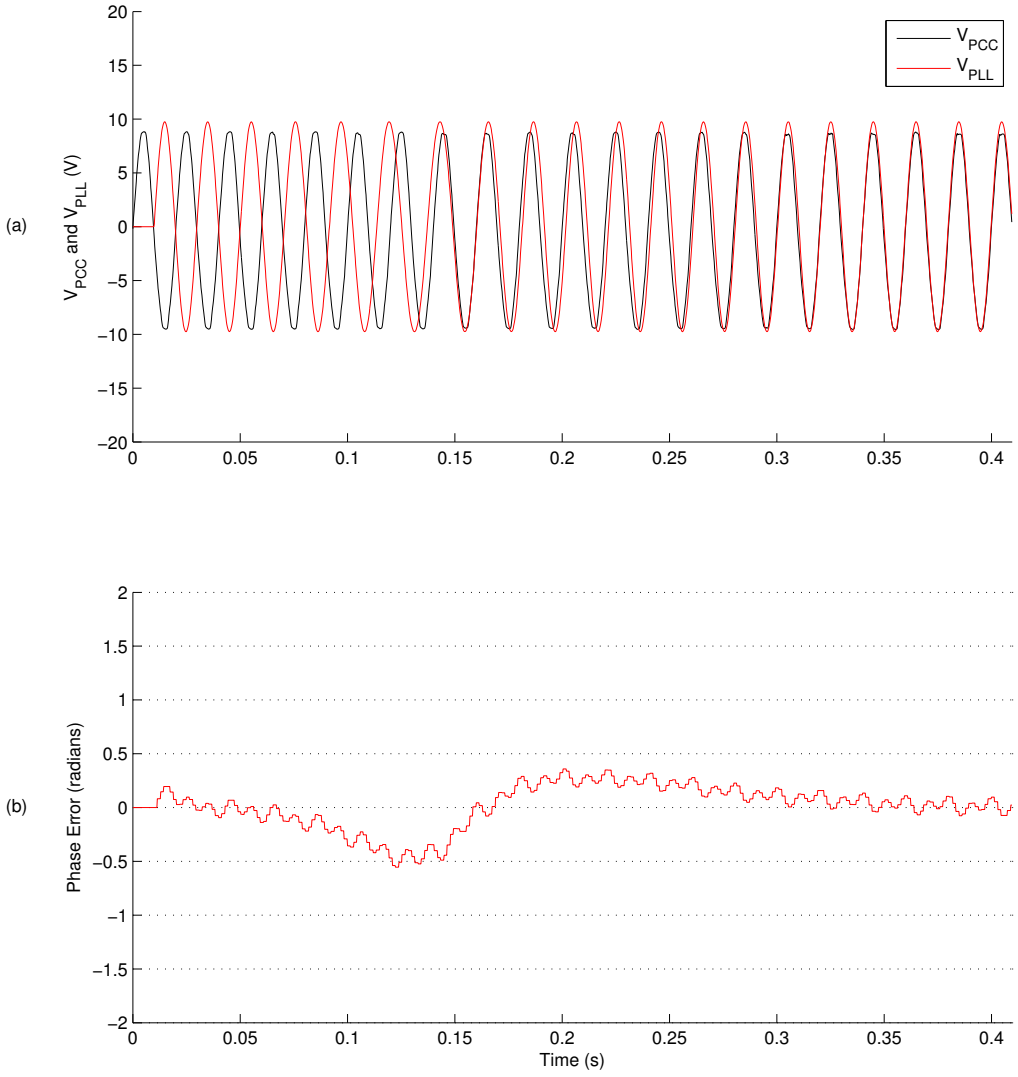

Figure 3.10: Experimental result for p-PLL implementation. a, the measured voltage, V_{PCC}, against the scaled PLL output, V_{PLL}; b, the low pass filter output, e.

3.4.2 Current Control

The aforementioned PLL structure is implemented simply to provide a current demand signal, I^*, which is needed so that closed loop current control can be achieved. The current control loop is a standard DQ control loop used in many single phase inverter projects [92–94]. It is necessary to transfer both the current demand, I^*, and the actual current, I, into the synchronous DQ reference frame. Single phase inverters require an additional imaginary signal, I_I, to move to the DQ reference frame. This signal is internally created on an orthogonal plane to the real current, I_R, so that

$$I_R = I_m \sin(\omega t + \phi) \tag{3.11}$$

and

$$I_I = I_m \cos(\omega t + \phi) \tag{3.12}$$

where ω is the fundamental frequency angular velocity, I_m is the current magnitude and ϕ is the phase difference. To create the imaginary current the real current is simply delayed by $\pi/2$. This is done within the DSP by sampling and storing the real current, then introducing a time delay of 1/4 of the fundamental period. The rotation matrix used to transform from the stationary to the synchronous DQ reference frame is

$$T = \begin{bmatrix} \sin(\omega t) & \cos(\omega t) \\ \cos(\omega t) & -\sin(\omega t) \end{bmatrix} \tag{3.13}$$

Giving the DQ currents

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & \cos(\omega t) \\ \cos(\omega t) & -\sin(\omega t) \end{bmatrix} \begin{bmatrix} I_m \sin(\omega t + \phi) \\ I_m \cos(\omega t + \phi) \end{bmatrix} \tag{3.14}$$

which simplifies to

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} I_m \cos(\phi) \\ I_m \sin(\phi) \end{bmatrix} \tag{3.15}$$

This transformation is applied to both the actual current, I, and the demanded current, I^*. Two separate PI controllers are used, one for the d-axis and one for the q-axis currents. The inputs to the two PI controllers are therefore

$$d_{error} = I_d^* - I_d, \qquad q_{error} = I_q^* - I_q \tag{3.16}$$

The two PI controllers are tuned using the Zeigler-Nichols routine. The following steps are used:

- The controller is set to purely proportional.
- The proportional gain is increased until the system exhibits constant output oscillations. The critical proportional gain and the period of the output oscillation is recorded, $K_{P(crit)}$ and T_{crit}, respectively.
- The controller gains are set at the final working values:
  - The proportional gain, K_P, is set at 0.45 $K_{P(crit)}$.
  - The integral gain, K_I, is set at 0.8 T_{crit}.

The PI controller outputs are again transformed to the synchronous DQ reference frame using the rotation matrix (3.13). Only one of the outputs is used as the modulation index for the PWM block as the other output relates to the created orthogonal signal.

A d-axis step in the current demand was used to experimentally test the current control structure. A d-axis current demand step was used as this represents operation of the power system at unity power factor. The step response is shown in Figure 3.11. The step response demonstrates that the system achieves a near zero error within 20 fundamental periods, which is an adequate response when considering that the system should only have to handle small changes in both d-axis and q-axis values. The short burst in the q-axis value, shown in trace (b), is caused by the creation of the imaginary orthogonal current, this will only occur once during system start up.

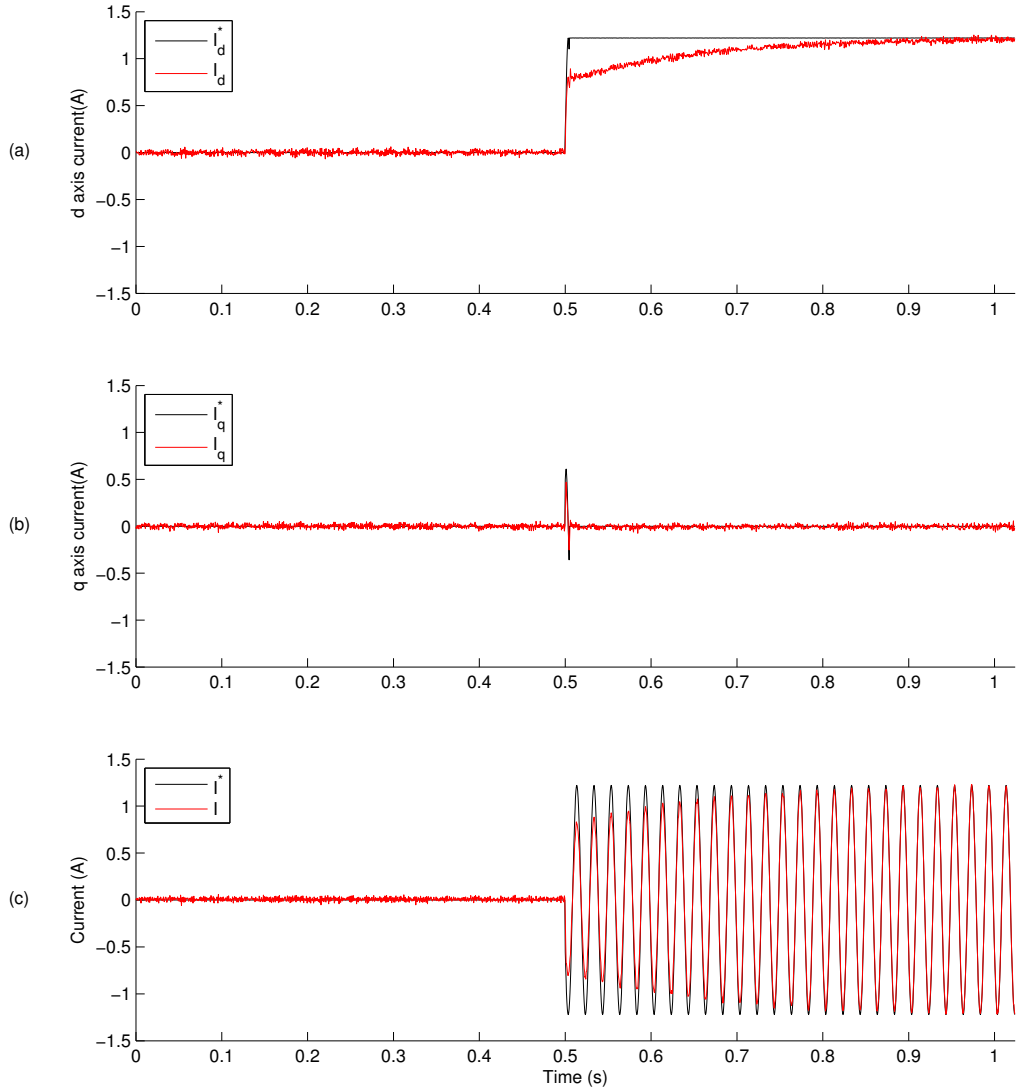

Figure 3.11: Step response experimental results for current control structure. a, the measured and demanded current d-axis values; b, the measured and demanded current q-axis values; c, the measured and demanded current waveforms

3.4.3 Current Offset and Magnitude Calculation

3.4.3.1 Balanced Power Operation

As the system is to be tested using various power mismatch conditions, it is important that the balanced power condition is thoroughly understood. Balanced power operation can be considered to be the condition in which the inverter provides the full amount of power for the local load, giving zero power flow to or from the utility. A vector representation of the inverter output power during balanced power

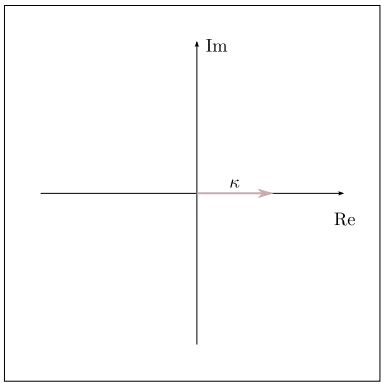

Figure 3.12: RLC load power during balanced power operation

operation, κ, is shown in Figure 3.12. As the load is resonant at 50 Hz, there is no reactive power exchange when operating at the fundamental frequency, meaning the system is operating with a unity power factor. The vector in Figure 3.12 shows that the power is along the real axis meaing the following statements can be made:

- Real power, P, equals apparent power,$|S|$.
- Reactive power, Q, equals zero.
- Current phase, α, equals zero.

To calculate the magnitude of κ, the RLC load was connected to the secondary winding of the grid connect transformer giving V_{RMS}= 6.78 V and I_{RMS}= 848 mA. Therefore at a balanced power condition, P_{RMS}= 5.78 W and $\kappa = 8.17\angle 0°$ W.

3.4.3.2 Power Mismatch Calculations

Section 3.4.3.1 describes operation at a balanced power condition, $\Delta P\%$=0 and $\Delta Q\%$=0. This section explains how the real and reactive power mismatch levels are used to calculate the current phase and magnitude. To allow a full understanding of the effect the power mismatch levels have on the inverter output power, Figure 3.13 shows the operation of the circuit under eight example mismatch conditions, where S_{INV} is the apparent output power of the inverter, P_{INV} is the real output power of the inverter and Q_{INV} is the reactive output power of the inverter. The resultant effect on the current angle, α, can be seen for the different power mismatch levels.

It is desirable to allow for any power mismatch between ±100% in both real and reactive directions. Two equations were derived, 3.17 and 3.18, to work out the demanded current phase and amplitude from the $\Delta P\%$ and $\Delta Q\%$ mismatch values.

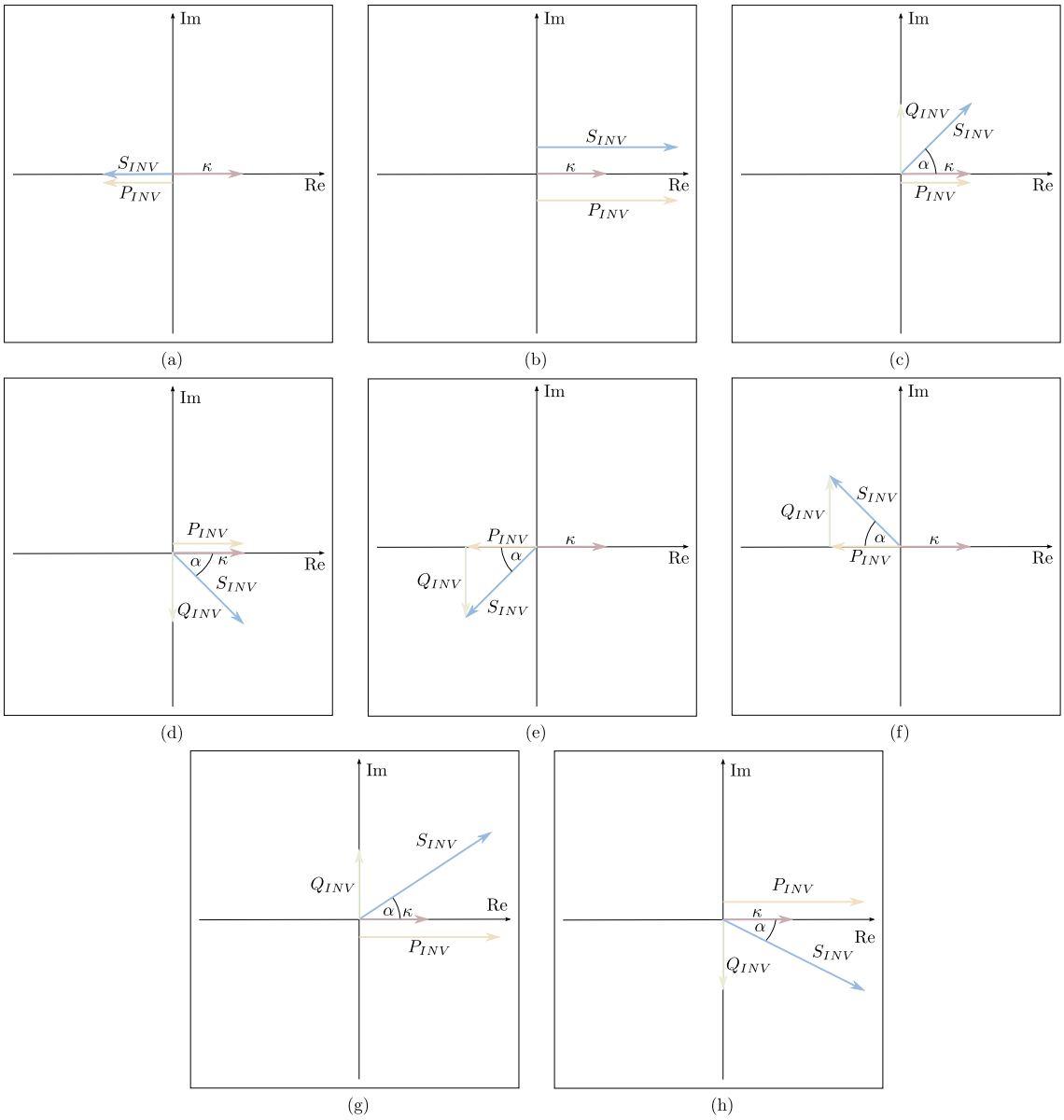

Figure 3.13: Power vectors for eight example mismatch conditions: a, $\Delta P\%$=-100, $\Delta Q\%$=0; b, $\Delta P\%$=100, $\Delta Q\%$=0; c, $\Delta P\%$=0, $\Delta Q\%$=100; d, $\Delta P\%$=0, $\Delta Q\%$=-100; e, $\Delta P\%$=-100, $\Delta Q\%$=-100; f, $\Delta P\%$=-100, $\Delta Q\%$=100; g, $\Delta P\%$=100, $\Delta Q\%$=100; f, $\Delta P\%$=100, $\Delta Q\%$=-100.

These equations are implemented within the Labview control panel allowing the board to receive only the phase offset, α^*, and amplitude of the desired current, $\hat{I}^*$.

$$\alpha^* = \arctan\left(\frac{Q^*}{P^*}\right) \tag{3.17}$$

$$\hat{I}^* = \sqrt{2}\left(\frac{|S^*|}{|V|}\right) \tag{3.18}$$

where

$$P^* = \frac{\Delta P\% + 100}{100} \times |\kappa|, \qquad Q^* = \frac{\Delta Q\%}{100} \times |\kappa|, \qquad |S^*| = \sqrt{P^* + Q^*} \tag{3.19}$$

with $|V|$ representing the V_{PCC} magnitude.

3.5 Operation Demonstration

To demonstrate the how the power flow of the system behaves under common operating conditions, and to verify the simulation model, the system was tested to check power flow is as expected.

A LOM routine was created, 1 second in duration, which follows the following steps:

- *Step 1* - The system operates with both the inverter enabled and the utility relay closed at the balanced power condition for 0.5 seconds.
- *Step 2* - At the routine time of 0.5 seconds the utility relay is opened to cease any power flow to or from the grid. This procedure is used to force a LOM event to occur, as the local power network is no longer connected to the wider power network.
- *Step 3* - The power flow of the set-up is monitored for a further 0.5 seconds to observe system parameters.

The simulation results obtained for this test are shown in Figure 3.14, with the corresponding experimental waveforms presented in Figure 3.15. The key feature visible in the results is the near zero utility current, shown in trace (b). The near zero utility current demonstrates that at the balanced power condition, all the power that is being consumed by the local RLC load is being produced by the inverter, resulting in very small amounts of power being exchanged with the grid. This LOM test results in the formation of a power island. That is, the output power of the inverter is large enough to sustain the local power consumption, causing the inverter output current to remain stable and synchronise with the inverter connection voltage. The small changes in the PCC voltage amplitude and phase that occur during the LOM event underline how challenging LOM detection can be, with such small parameter changes being hard to detect.

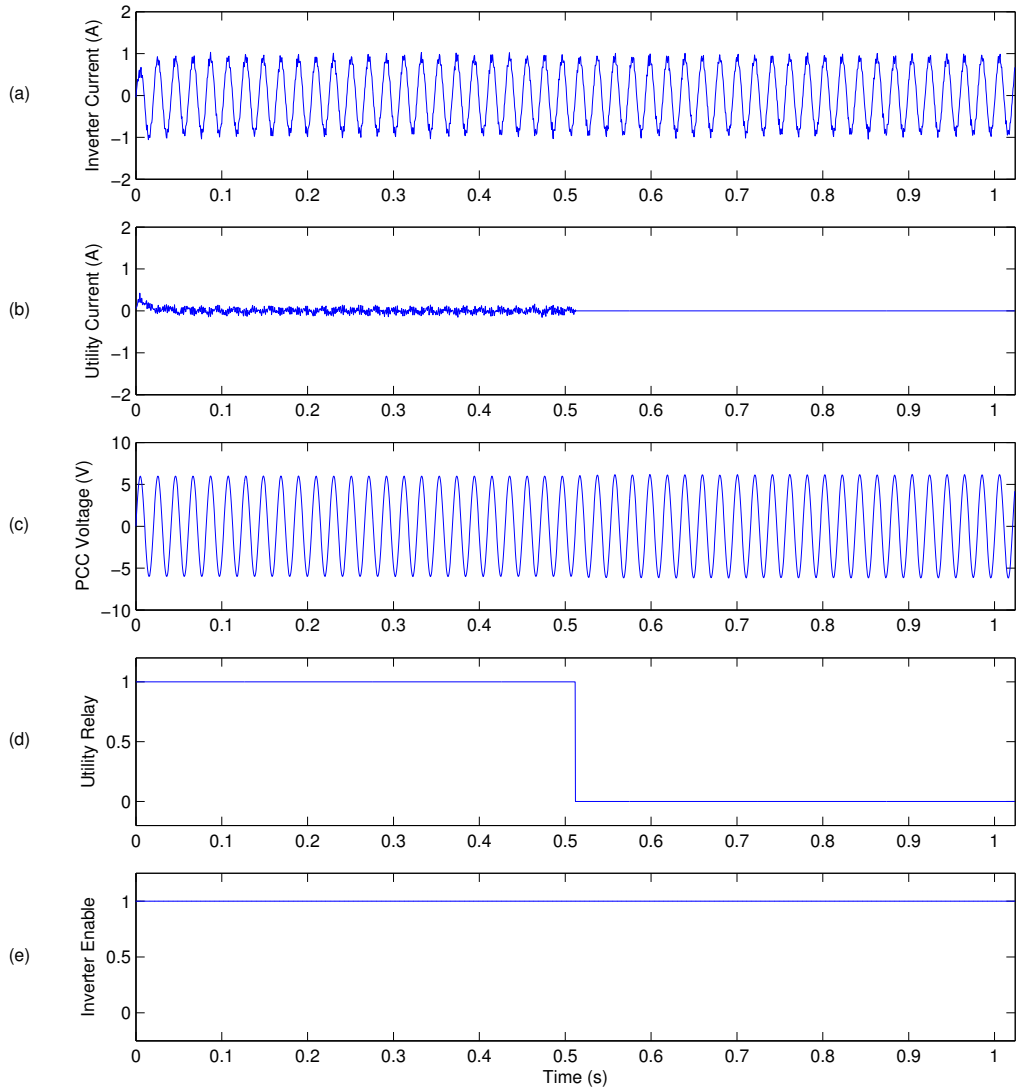

Figure 3.14: Simulation waveforms showing power flow during LOM event

To demonstrate how any short fall in local power generation, with respect to local power consumption, is compensated for by power exchange with the utility, a test was carried out to observe the power flow when the inverter output power is reduced to zero. The inverter disable test, 1 second in duration, follows the following steps:

- *Step 1* - The system operates with both the inverter enabled and the utility relay closed at the balanced power condition for 0.5 seconds.
- *Step 2* - At the routine time of 0.5 seconds the inverter output power is reduced to zero to cease any local power generation.

- *Step 3* - The power flow of the set-up is monitored for a further 0.5 seconds to observe system parameters.

The simulation results obtained for this test are shown in Figure 3.16, with the corresponding experimental waveforms presented in Figure 3.17. The main outcome of this test is that at the point of the inverter disable, at 0.5 seconds, the utility current increases to maintain the power consumption of the local RLC load. This test demonstrates that the output power of the inverter can be used to supply the power consumed by the local load, with any power mismatch resulting in power exchange with the utility.

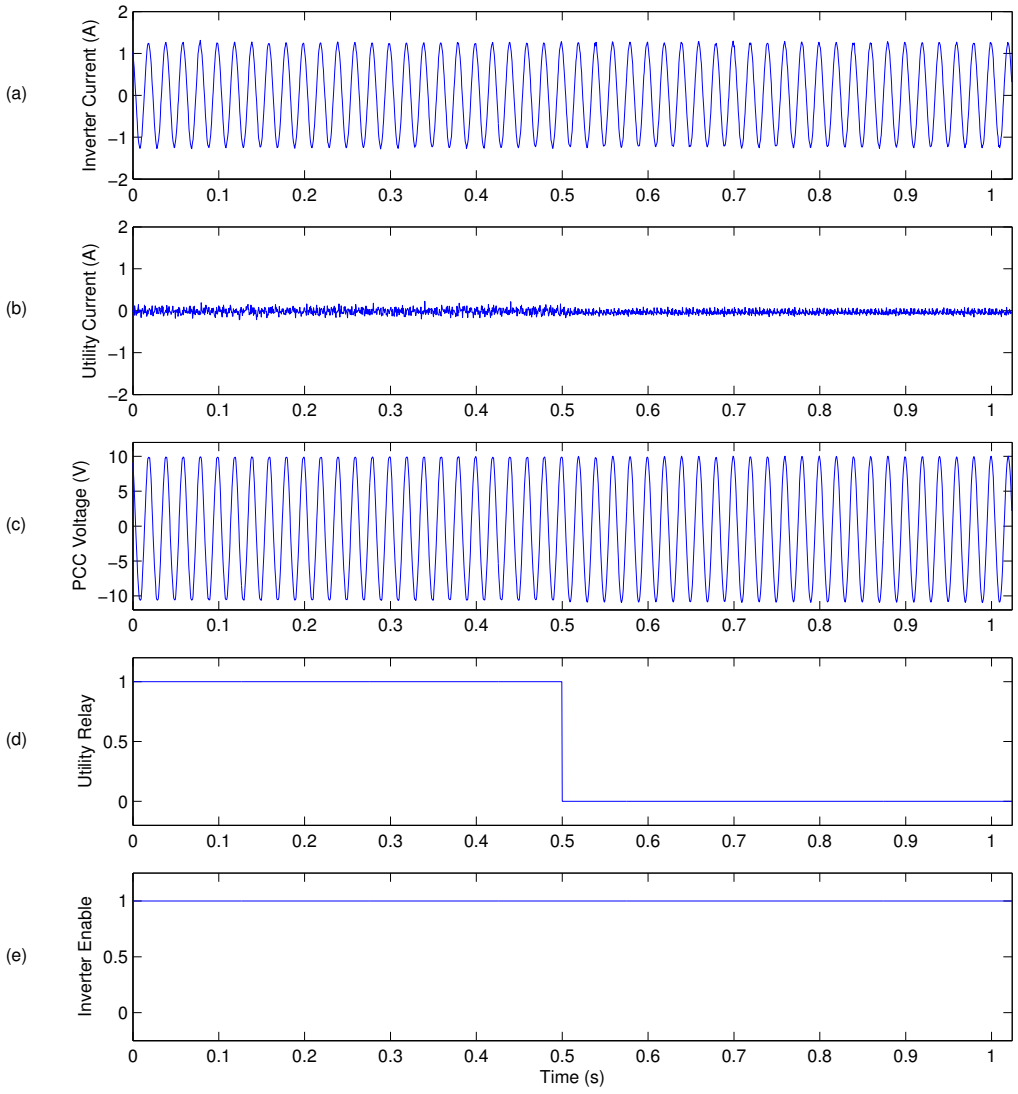

Figure 3.15: Experimental waveforms showing power flow during LOM event

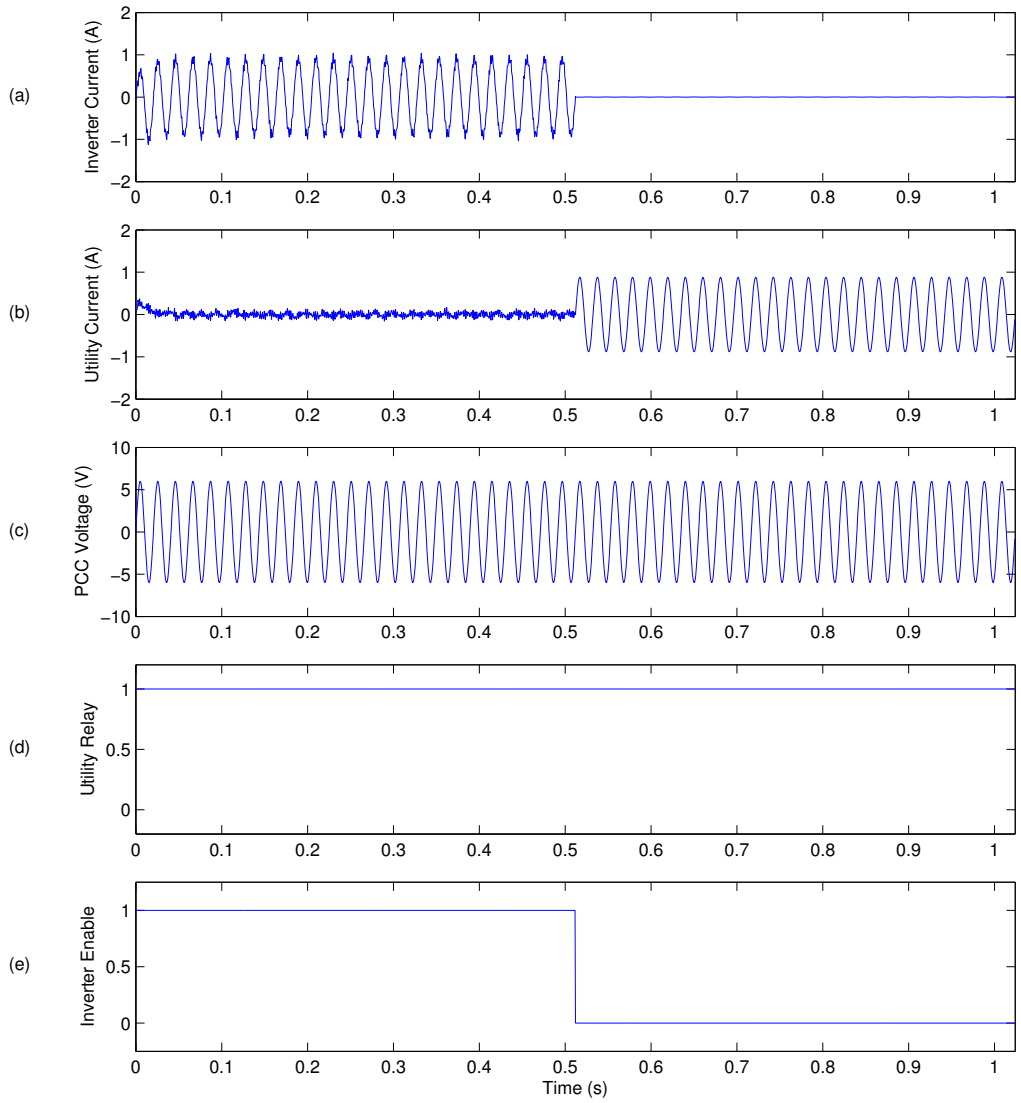

Figure 3.16: Simulation waveforms showing power flow during inverter disable

The results presented in this section demonstrate that the Simulink model accurately represents the laboratory test bench with the power flow for the two tests completed showing an acceptable level of similarity. The accuracy of the model allows LOM detection techniques to be developed in the simulation environment before being copied over to the DSP for hardware verification. The same power control structure is implemented in C++ in both environments, allowing LOM detection routines to be added within the exact same code.

The simulation environment operates at a slightly lower voltage level to the laboratory test bench, shown in the results presented in this section. This is due to some additional losses in the Simulink environment caused by additional resistances, such

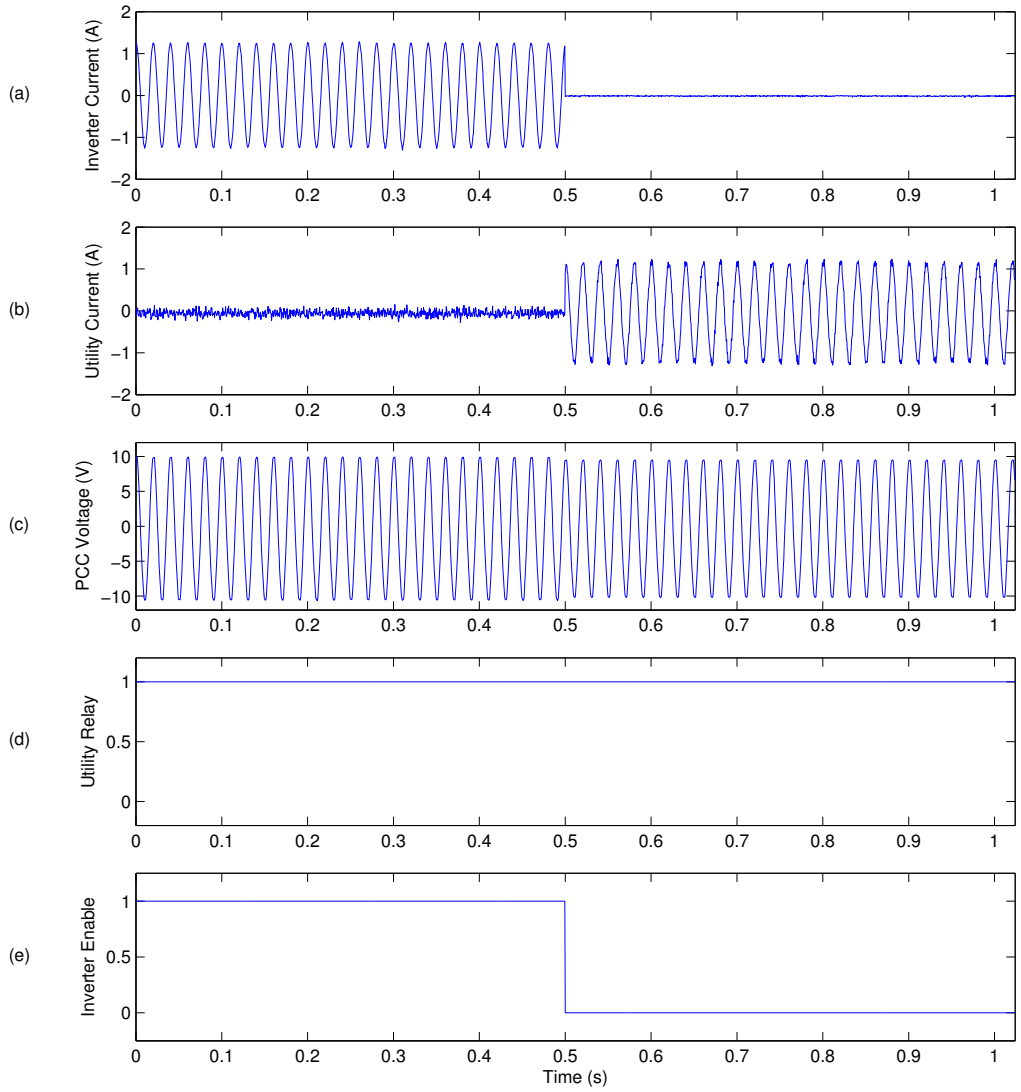

Figure 3.17: Experimental waveforms showing power flow during inverter disable

as the small resistor that is placed in series with the DC supply, needed to allow the numerical solver to simulate the circuit. As the power network operation is consistent with the laboratory test bench, this is not considered as important.

Chapter 4

Loss of Mains Detection

This chapter includes the presentation of results obtained whilst testing a variety of LOM detection techniques that are currently implemented in grid connection inverters or have been experimentally demonstrated in related research papers.

The aim of the work presented in this chapter is to determine the attributes and drawbacks associated with different types of LOM detection techniques, so that an informed analysis of any proposed technique can be made. Testing previously reported methods allows the difficulty of LOM detection to be understood.

The intention of this chapter is to inform of the general results that can be obtained using methods similar to currently implemented techniques. The results presented are not intended to dismiss or disregard any of the LOM detection methods. Instead, the results have been included to provide a suitable comparison to allow any proposed LOM detection technique to be fully evaluated. Therefore, whilst time has been spent developing the LOM detection techniques presented, they should not be considered to be exact replicas of existing techniques.

Each LOM detection technique is introduced and discussed with possible advantages and disadvantages stated. The simulation results obtained using the model described in Section 3.3 are presented including waveforms demonstrating the operation of each LOM detection technique. The experimental results gathered using the laboratory set-up introduced Section 3.2 are presented, including measured data showing how each LOM detection system works. To increase the computational efficiency of the DSP, some measurements are not converted to real world units. Instead, these are presented as the raw ADC value to show any change.

A short summary of each LOM detection technique is included, along with a comparison with LOM detection techniques that belong to the same category. The possible drawbacks that would occur if the system was to be implemented in a product are discussed.

All the presented results are based on the LOM detection systems running within the 10 kHz PWM interrupt sequence. Therefore, the sampling rate for all internal parameters is 10 kHz.

A standard LOM detection test, which is 2.2 seconds in duration, has been created which follows a set procedure:

- *Synchronisation* - The first 0.2 seconds is to allow the control system to reach steady state at the specified power mismatch level.
- *LOM event* - At the time 0.2 seconds a LOM event is forced by turning the utility relays to open circuit.
- *Detection time* - The system continues to operate for 2 more seconds to determine if the LOM event is detected within the maximum time specified in IEEE connection standards.
- *End* - The inverter output is turned off and the system is reset.

The standard LOM detection test remains constant for all the results presented within this chapter.

4.1 Passive Techniques

Two passive LOM detection techniques have been implemented and tested. This section describes the operation of the two methods and presents the simulation and experimental results.

Passive LOM detection techniques commonly exhibit a non zero NDZ as they rely solely on measured network parameters. As passive systems have no affect on the inverter output power, the size of the NDZ is the metric used to determine the performance of the LOM detection method. The performance of the two passive LOM detection methods presented in this section are to be compared using their NDZ's.

To establish the NDZ for each passive LOM detection technique, the standard LOM detection test was completed across a range of power mismatch levels. The results can then be plotted on a graph to show which operating conditions resulted in a non detect.

4.1.1 Under/Over Voltage and Frequency

This LOM detection technique continuously monitors the V_{PCC} amplitude and frequency and uses thresholds that dictate the acceptable grid connected range to determine when a LOM event has occured. The operation block diagram is shown in Figure 4.1. The PLL described in Section 3.4.1 is included to demonstrate how the system synchronises with the calculated phase of the V_{PCC} signal.

The amplitude of V_{PCC} is monitored by calculating the RMS value for each fundamental period. This is completed using an integration loop which sums the squared V_{PCC} values, each time the phase output of the PLL is reset, it triggers the LOM detection routine to calculate RMS of V_{PCC} and reset the integrator. Equation 4.1 is used to calculate the RMS of V_{PCC}.

$$V_{RMS} = \sqrt{\frac{\sum_{n=0}^{N} V_{PCC_n}^2}{N}} \tag{4.1}$$

Where N is the number of samples since the last RMS calculation and n is the sample number. Assuming V_{PCC} is a 50 Hz signal, N will be equal to 200.

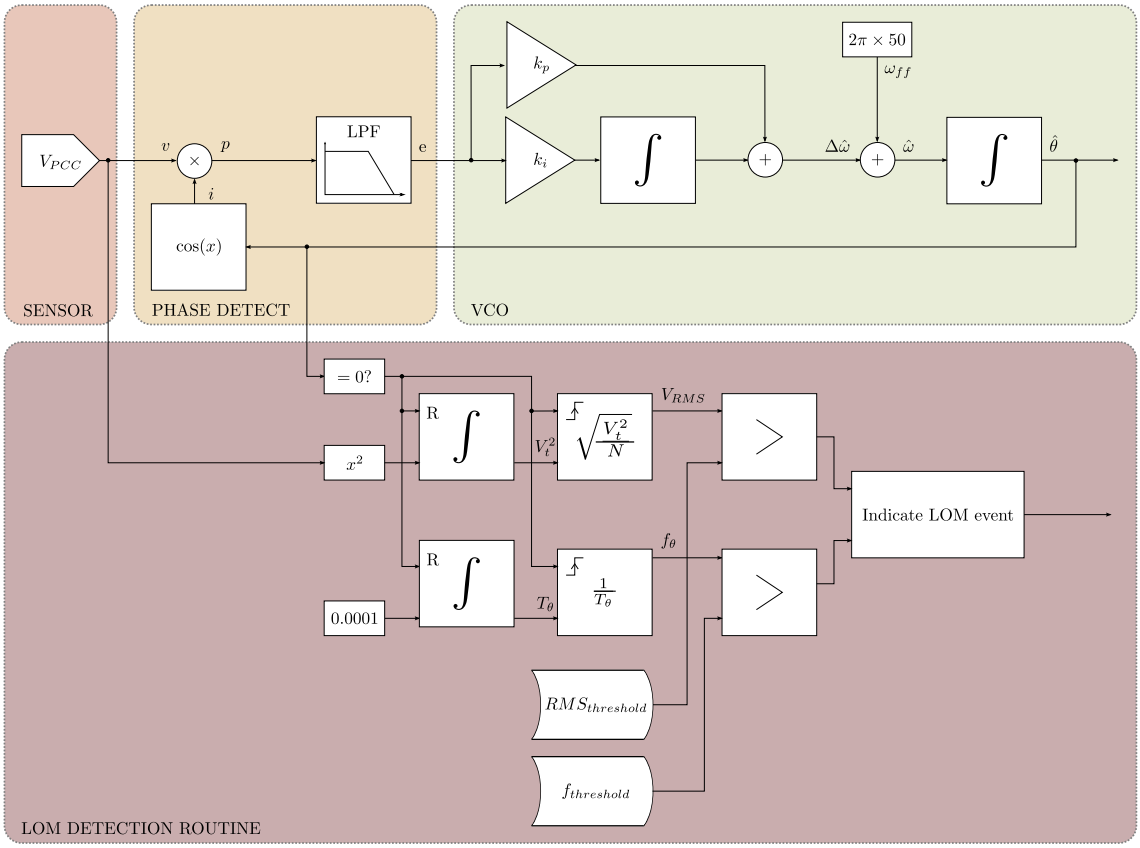

Figure 4.1: Under/over voltage amplitude and frequency operation block diagram

The frequency of V_{PCC} is calculated using a second integration loop which sums the sampling period, 0.0001 seconds, on each iteration. By resetting the integrator each time the output phase of the PLL is reset, the period of V_{PCC} can be determined, which can be used to calculate the frequency of V_{PCC} for each fundamental period. Equation 4.2 is used to calculate the frequency of V_{PCC}.

$$f_{\theta}(Hz) = \frac{1}{\sum_{n=0}^{N} 0.0001} \tag{4.2}$$

Where N is the number of samples since the last RMS calculation.

The new values for the V_{PCC} amplitude and frequency are calculated every fundamental period. The LOM detection routine completes a threshold comparison each time a parameter update occurs. A LOM event is indicated if the amplitude or frequency are outside the acceptable grid connected range. The national grid is responsible for delivering energy within the UK. The acceptable operating region, stated in the grid code reference document, for the single-phase domestic supply is 240 V $\pm$10% at 50 Hz $\pm$0.5Hz [95].

The results presented in Section 4.1.1.1 and Section 4.1.1.2 use the same percentage thresholds. The actual threshold values differ due to the different scaling that is used in the simulation environment. The under/over amplitude routine specifies the acceptable grid connected range at $\pm$15% of the nominal RMS voltage. The under/over frequency routine indicates a LOM event when the calculated frequency is outside the range, 49.25-50.75 Hz. The threshold values allow a slightly larger acceptable grid connected range than specified by the national grid, this reduces the likelihood of a false trip.

4.1.1.1 Results At Balanced Power Operation

To demonstrate how a LOM event can go undetected whilst the under/over voltage amplitude and frequency routine is operating, the standard LOM test was completed at the balanced power operating condition. The resultant simulation waveforms are shown in Figure 4.2, and the corresponding experimental waveforms are shown in Figure 4.3.

The results show that before the LOM occurs 0.2 seconds into the routine, the utility current, trace (b), is near zero; this indicates that the system is operating at the

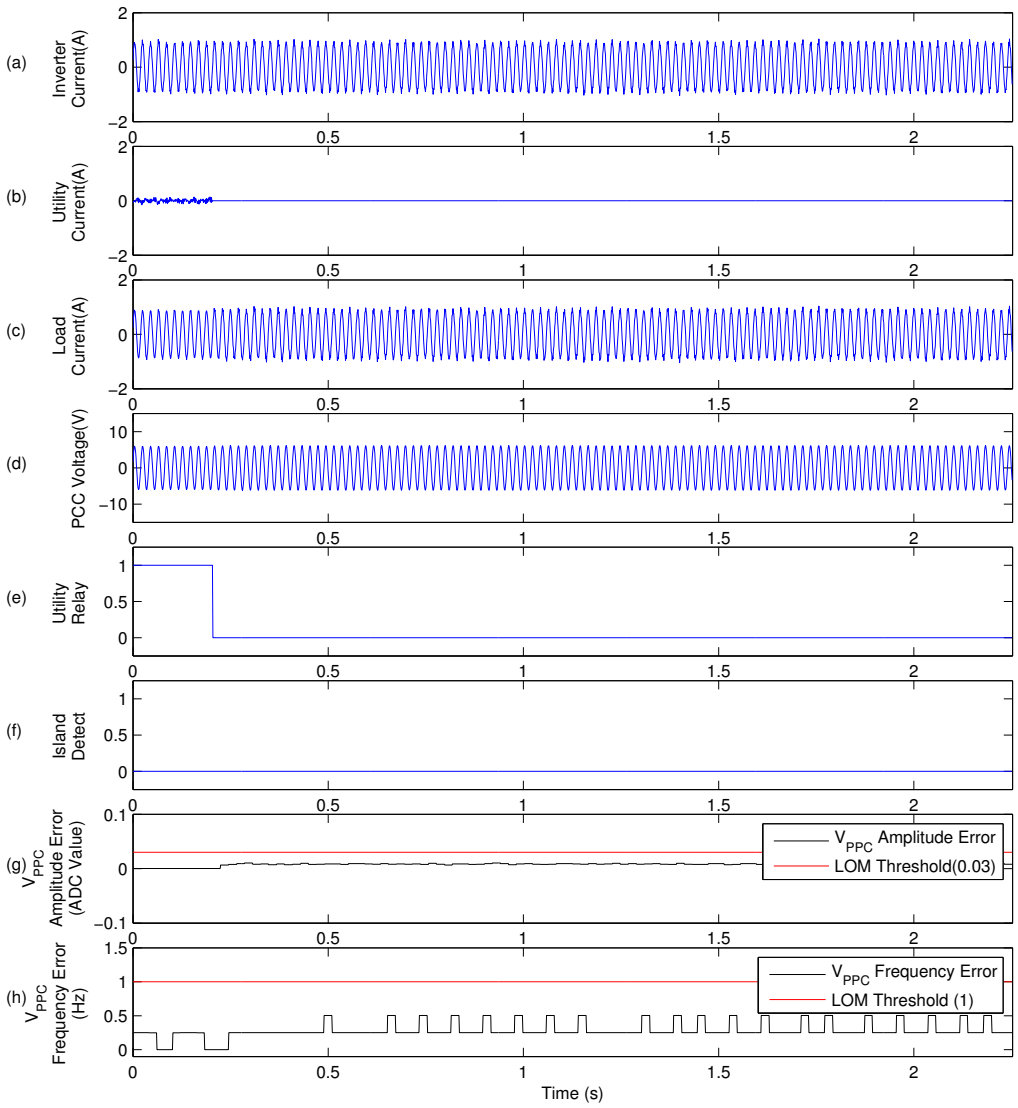

Figure 4.2: Under/over voltage amplitude and frequency simulation waveforms during a LOM event occurring at balanced power operation

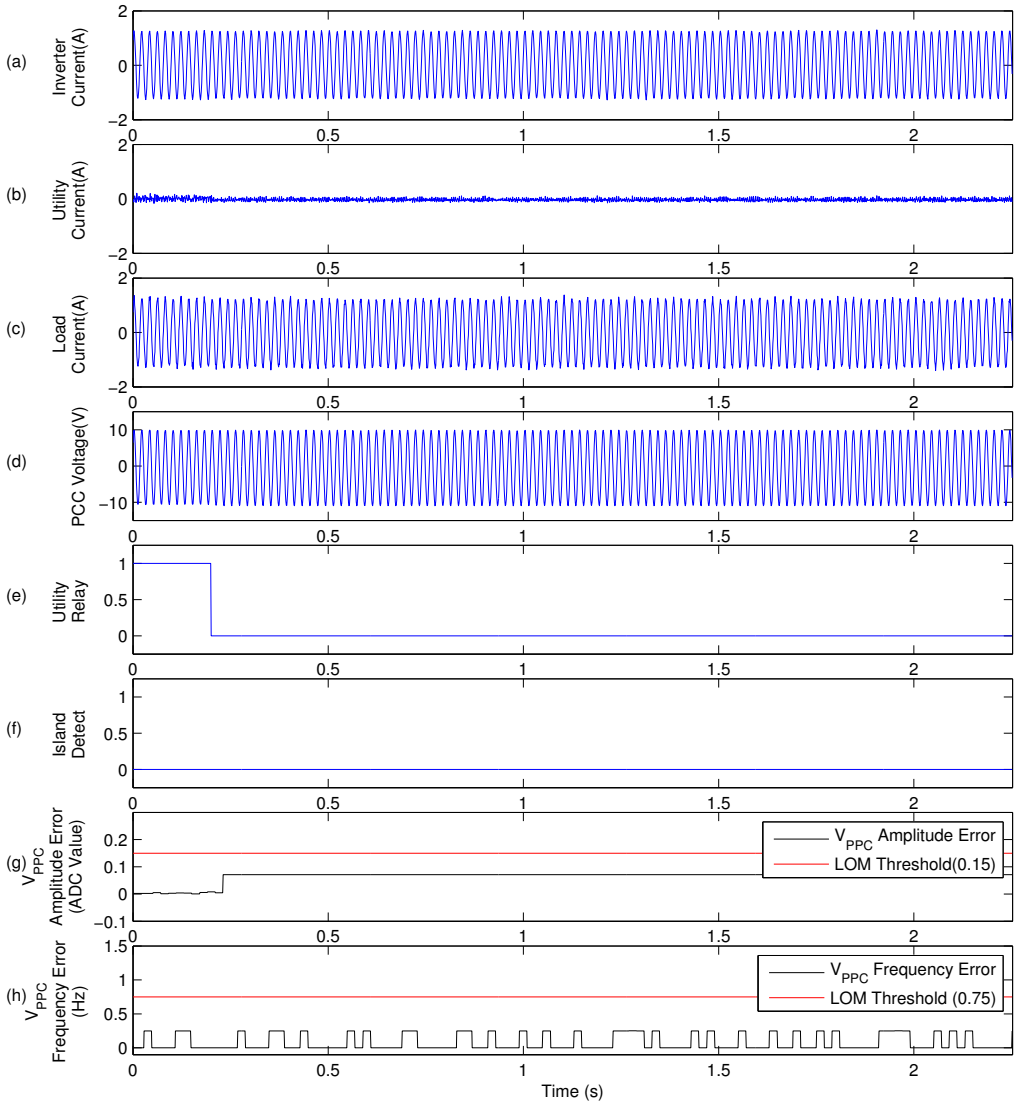

Figure 4.3: Under/over voltage amplitude and frequency experimental waveforms during a LOM event occurring at balanced power operation

balanced power condition. The inverter output current, trace (a), remains stable after the LOM event has occurred. This allows the V_{PCC} voltage, trace (d), to be maintained within the acceptable grid connected range. The internally calculated amplitude and frequency errors have been included, traces (g) and (h) respectively, to show the lack of a substantial parameter change during a LOM event when operating at the balanced power condition. The calculated parameters do not exceed the acceptable grid connected thresholds, hence, the LOM event is not detected, shown in trace (f).

4.1.1.2 Results At Power Mismatch Operation

To demonstrate how a LOM event is detected by the under/over voltage amplitude and frequency routine, the standard LOM test was completed whilst the inverter was producing 10% more real and reactive power than was being consumed by the local RLC load ($\Delta P\%$ =10 and $\Delta Q\%$ =10). The resultant simulation waveforms are shown in Figure 4.4, and the corresponding experimental waveforms are shown in Figure 4.5.

Trace (b) shows the utility current, it can be observed that power is exchanged with

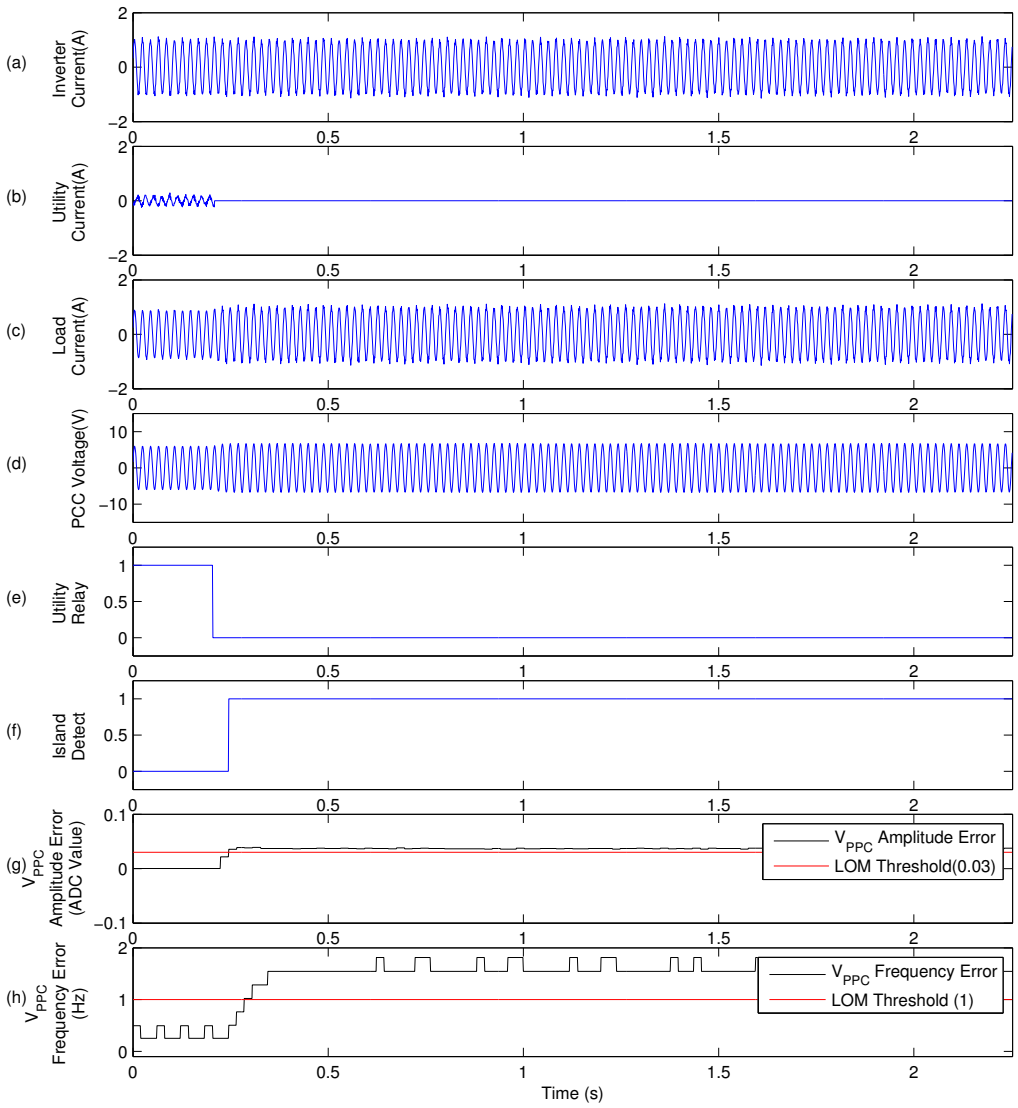

Figure 4.4: Under/over voltage amplitude and frequency simulation waveforms during a LOM event occurring at $\Delta P\%$ =10 and $\Delta Q\%$ =10 power mismatch operation

the utility before the LOM event occurs at 0.2 seconds. The fact that local power generation is larger than local power consumption is causing the excess current to be injected into the grid. After the LOM event occurs, the excess current flows into the local load, causing the load current, trace (c), and the measured V_{PCC}, trace (d) to visibly increase in amplitude. The calculated V_{PCC} amplitude and frequency, trace (g) and trace (h) respectively, exceed the acceptable grid connected range set by the thresholds.

Figure 4.4, trace (f), shows that the LOM event is detected with detection delay

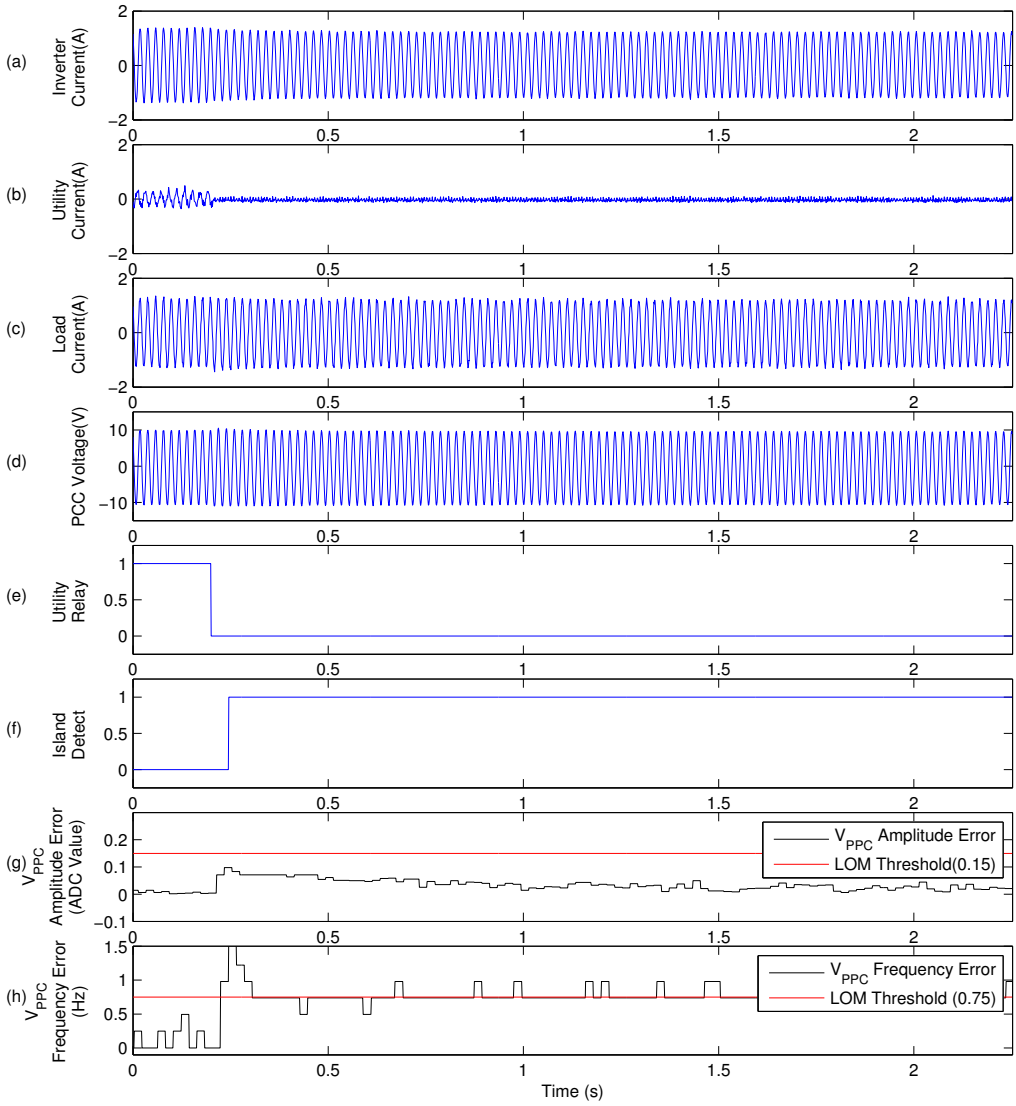

Figure 4.5: Under/over voltage amplitude and frequency experimental waveforms during a LOM event occurring at $\Delta P\%$ =10 and $\Delta Q\%$ =10 power mismatch operation

of around 0.02 seconds for the simulation implementation. Whilst the experimental detection delay time is around 0.04 seconds, shown in trace (f) of Figure 4.5.

4.1.1.3 None Detection Zone

The NDZ for the simulation implementation of the under/over voltage amplitude and frequency technique is shown in Figure 4.6. The standard LOM detection test was completed across a range of operating conditions (±15% in both real and reactive power mismatch). The graph clearly shows the collection of operating conditions, clustered around the balanced power condition, for which a LOM event would not be detected by the under/over voltage amplitude and frequency technique.

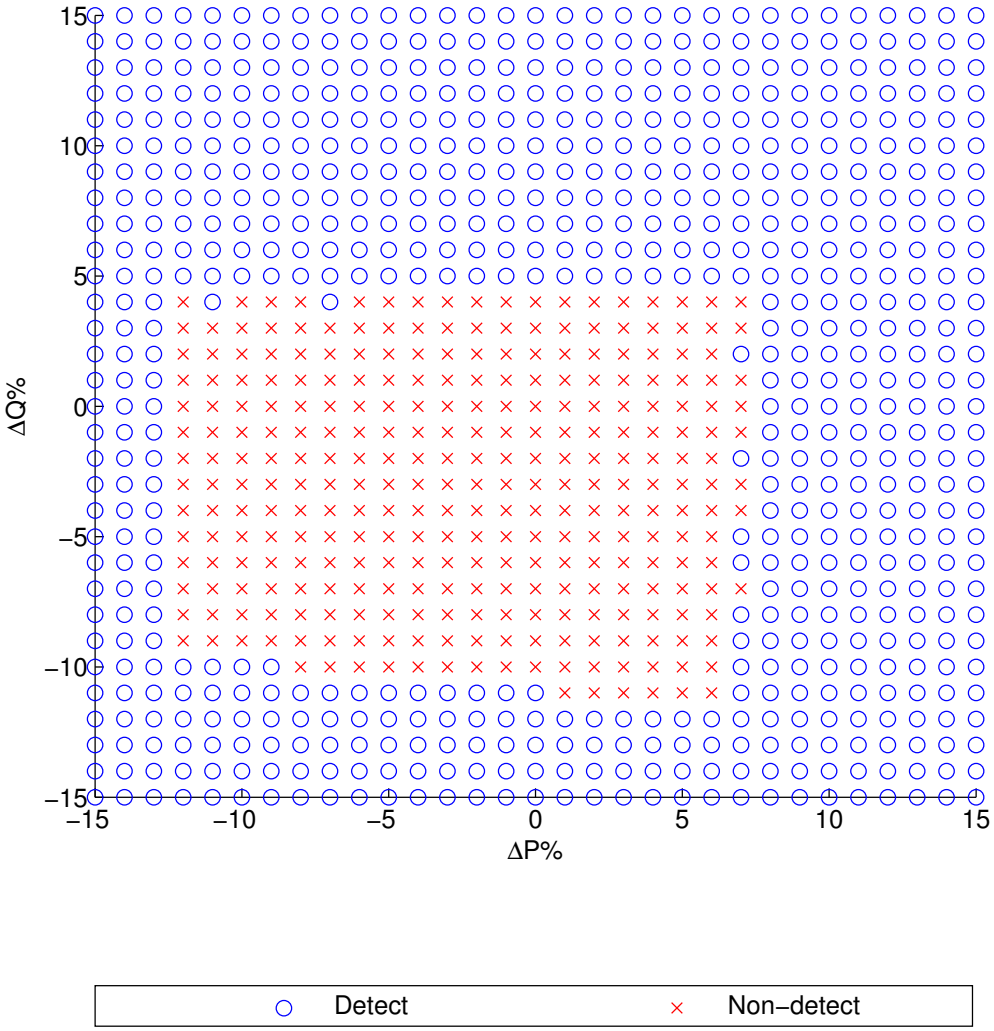

Figure 4.6: Under/over voltage amplitude and frequency simulation NDZ graph

The NDZ for the experimental implementation of the under/over voltage amplitude and frequency technique is shown in Figure 4.7.

The experimental NDZ is similar in size and shape with the simulation NDZ shown in Figure 4.6, demonstrating the accuracy of the model.

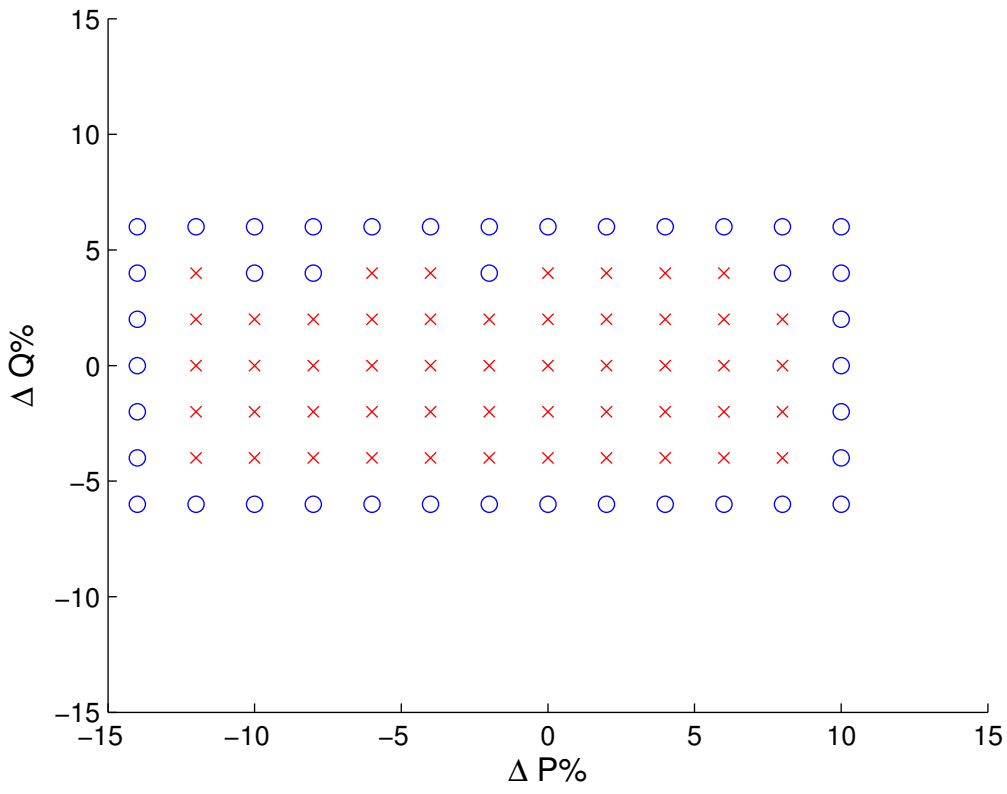

Figure 4.7: Under/over voltage amplitude and frequency experimental NDZ graph

4.1.2 ROCOV/ROCOF

This LOM detection technique continuously monitors the rate of change of both the amplitude and frequency of the measured V_{PCC} voltage. Thresholds are used to dictate the acceptable grid connected range for these two parameters, with a LOM event being indicated when either parameter is calculated beyond the thresholds. The LOM detection system is synchronised with the phase of the measured V_{PCC} voltage using the phase of the PLL. This means parameters are updated once every fundamental period (0.02 seconds). The operation block diagram is shown in Figure 4.8.

The rate of change of voltage, ROCOV, is determined using the RMS value of the measured V_{PCC} voltage. Each time the RMS value is updated, the difference between the previous and latest RMS values is calculated, this difference is used as the ROCOV parameter. The RMS value is calculated in the same way as with the under/over voltage amplitude and frequency technique, described in Section 4.1.1.

The rate of change of frequency, ROCOF, is determined using the phase error signal that is calculated within the PLL module. As any rapid change in V_{PCC} frequency would result in a substantial phase difference between the measured V_{PCC} signal

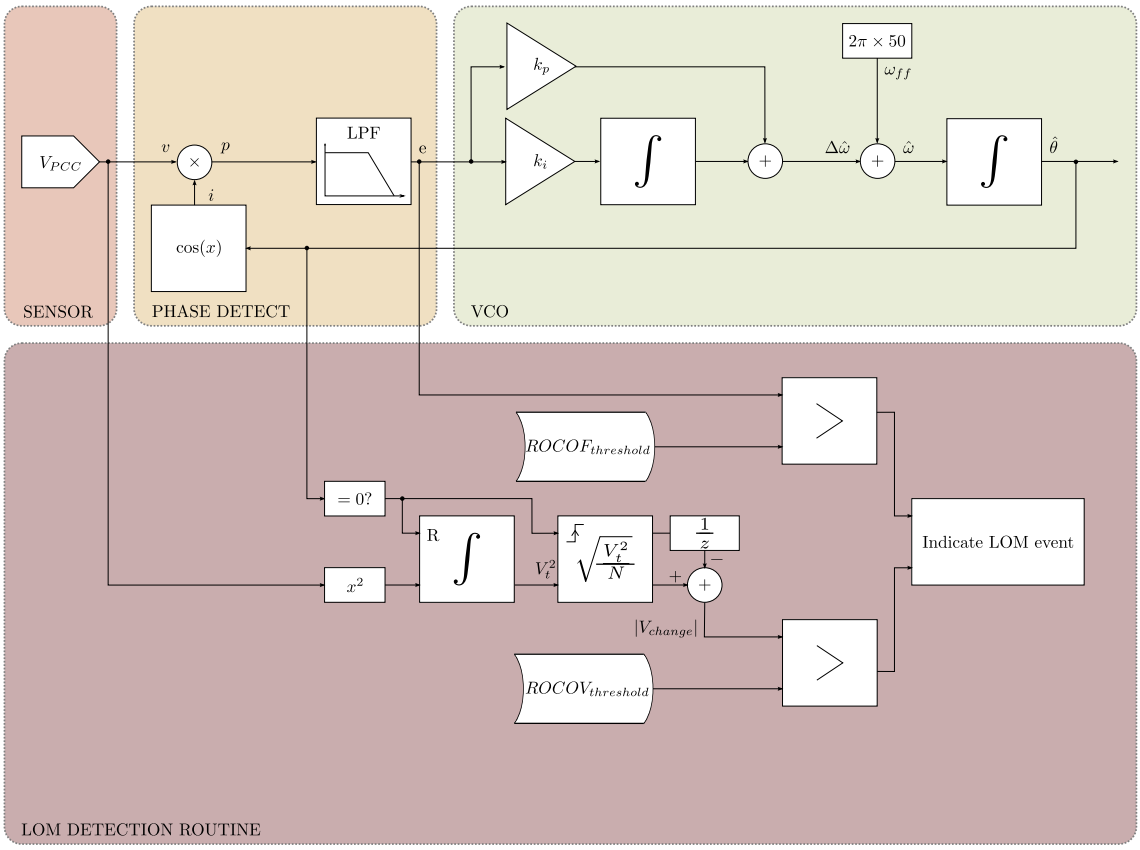

Figure 4.8: ROCOV/ROCOF operation block diagram

and the internal phase of the PLL, this error magnitude can be used as the ROCOF parameter.

The acceptable grid connected range for the calculated parameters, ROCOV and ROCOF, is specified using thresholds. The DS3 advisory council suggests possible values for the thresholds used [96]. However, no exact threshold is specified. As the threshold values are not specified, the thresholds are chosen and tuned during the system development. The ROCOV and ROCOF calculation routine was allowed to operate on a continuous grid voltage signal, with the maximum ROCOV and ROCOF values recorded. The thresholds were then set 15% above the test period maximums. The acceptable grid connected range is larger than the recorded maximums to reduce the likelihood of a false trip.

4.1.2.1 Results At Balanced Power Operation

The ROCOV/ROCOF routine was implemented using both the simulation environment and the hardware laboratory set-up. To show how the system cannot detect a LOM event whilst operating at the balanced power condition, the standard LOM test was completed with zero power mismatch. The simulation results obtained for the balanced power standard LOM test are shown in Figure 4.9, and the corresponding experimental waveforms are shown in Figure 4.10.

Trace (b) shows that no substantial power exchange with the utility occurs, either

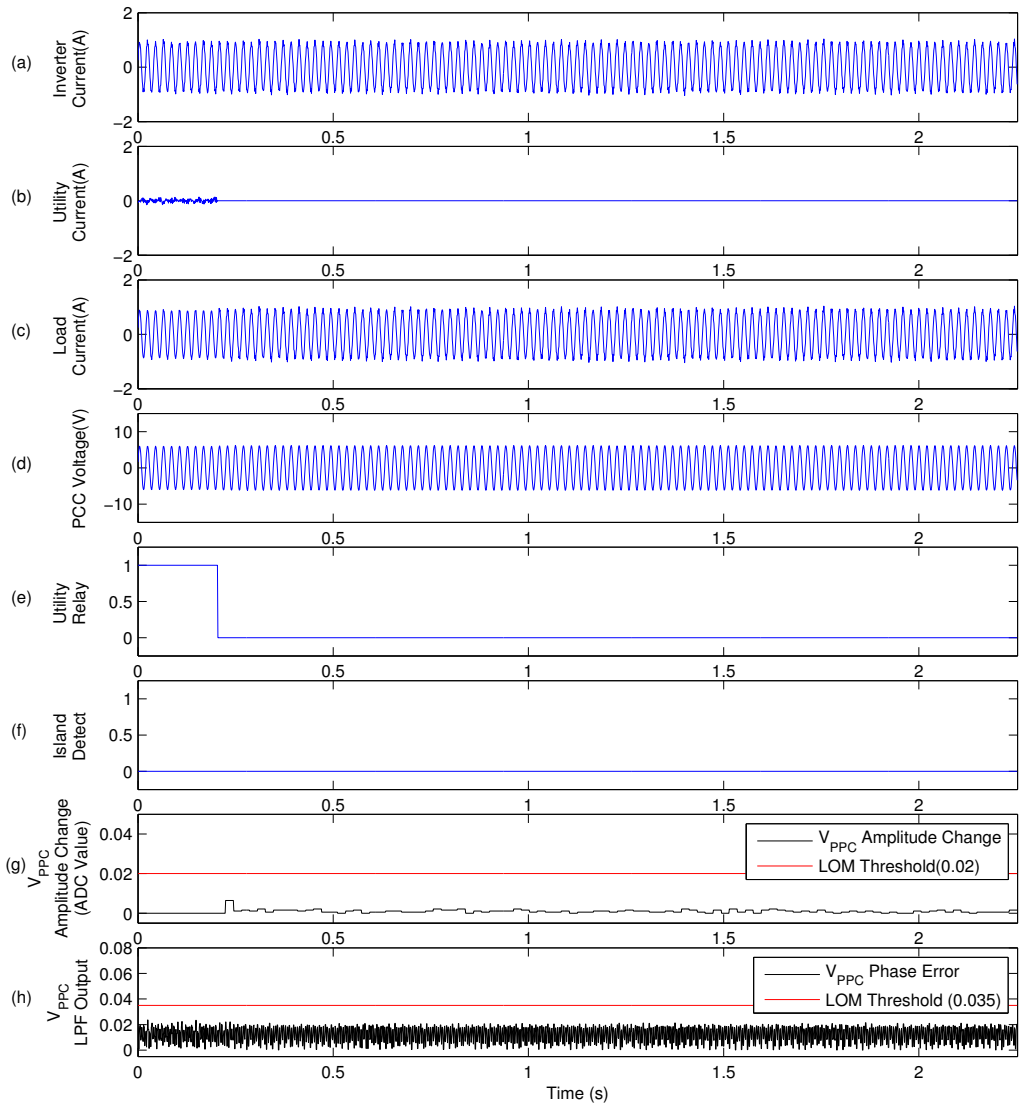

Figure 4.9: ROCOV/ROCOF simulation waveforms during a LOM event occurring at balanced power operation

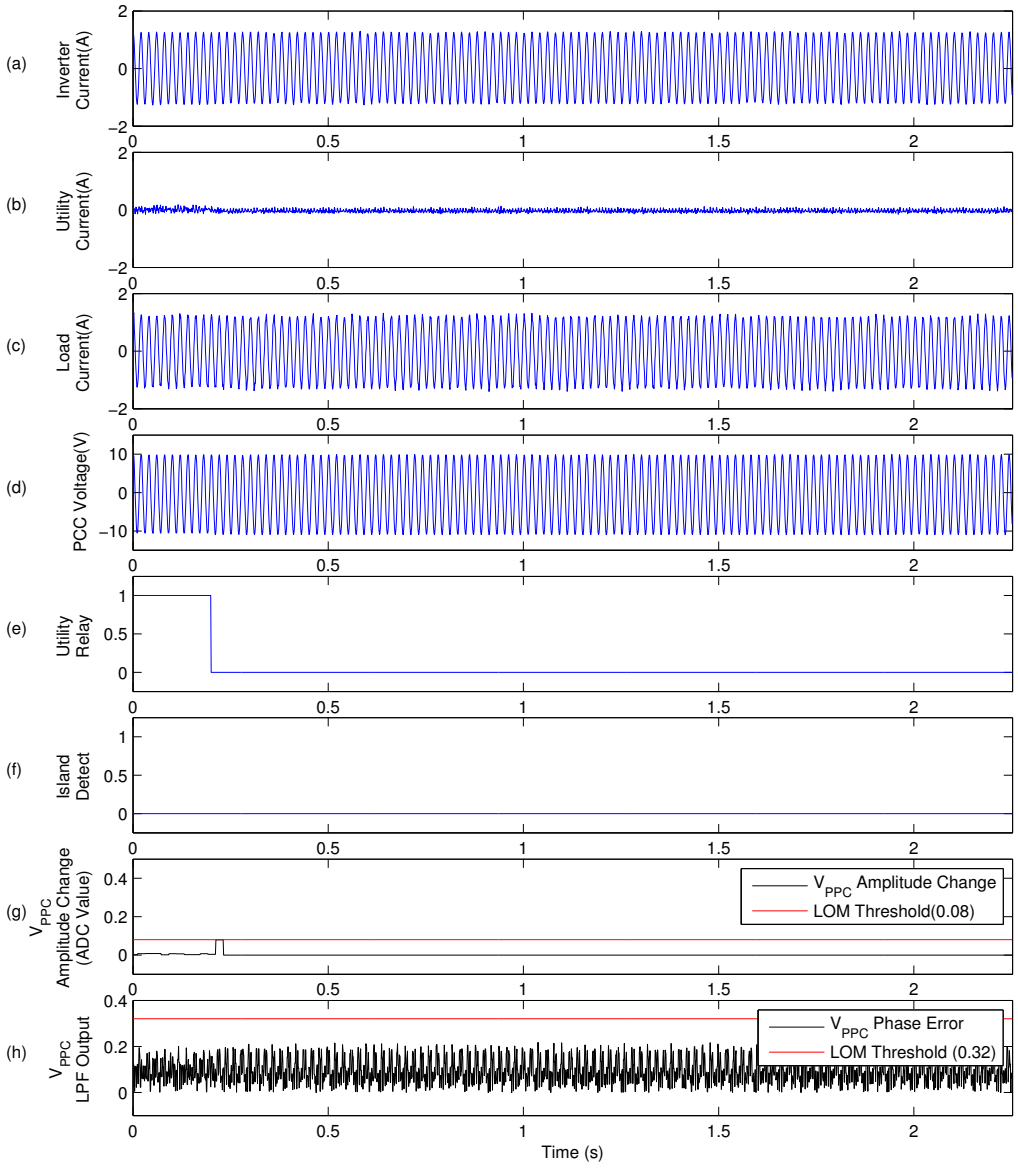

Figure 4.10: ROCOV/ROCOF experimental waveforms during a LOM event occurring at balanced power operation

before or after the LOM event at 0.2 seconds, demonstrating balanced power operation. After the LOM event, the measured V_{PCC} voltage, trace (d), remains fairly constant, meaning neither calculated parameter exceeds the acceptable grid connected range set by the thresholds, shown in trace (g) and trace (h). The lack of a substantial change in either amplitude or frequency parameter results in the LOM event going undetected, trace (f).

4.1.2.2 Results At Power Mismatch Operation

To demonstrate how a LOM event is detected by the ROCOV/ROCOF routine, the standard LOM test was completed whilst the inverter output was controlled to produce 10% more real and reactive power than is being consumed by the local load ($\Delta P\%$ =10 and $\Delta Q\%$ =10). Figure 4.11 shows the simulation results, and Figure 4.12 shows the corresponding experimental waveforms.

As the inverter is producing more real and reactive power than the local load is consuming, power flows into the utility, demonstrated by the non zero current shown

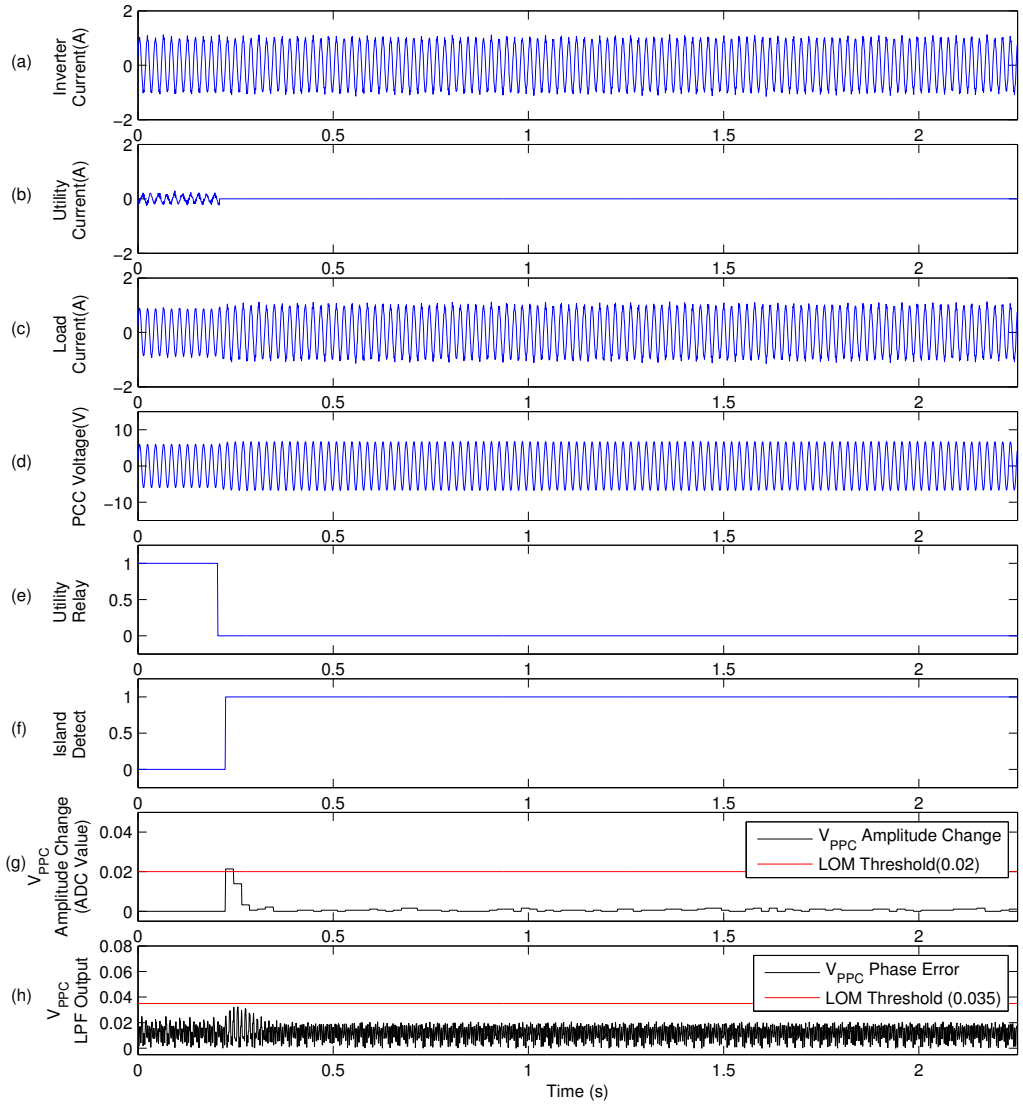

Figure 4.11: ROCOV/ROCOF simulation waveforms during a LOM event occurring at $\Delta P\%$ =10 and $\Delta Q\%$ =10 power mismatch operation

in trace (b). Trace (d) shows a clear step change in the V_{PCC} voltage amplitude when the LOM event occurs. This step change in amplitude causes the calculated ROCOV parameter to exceed the threshold, trace (g), and indicate the LOM event, trace (f). In the experimental results, Figure 4.12, the phase error also exceeds the LOM threshold, shown in trace (h). The simulation detection delay for this mismatch condition is around 0.025 seconds and the corresponding experimental detection delay is around 0.02 seconds.

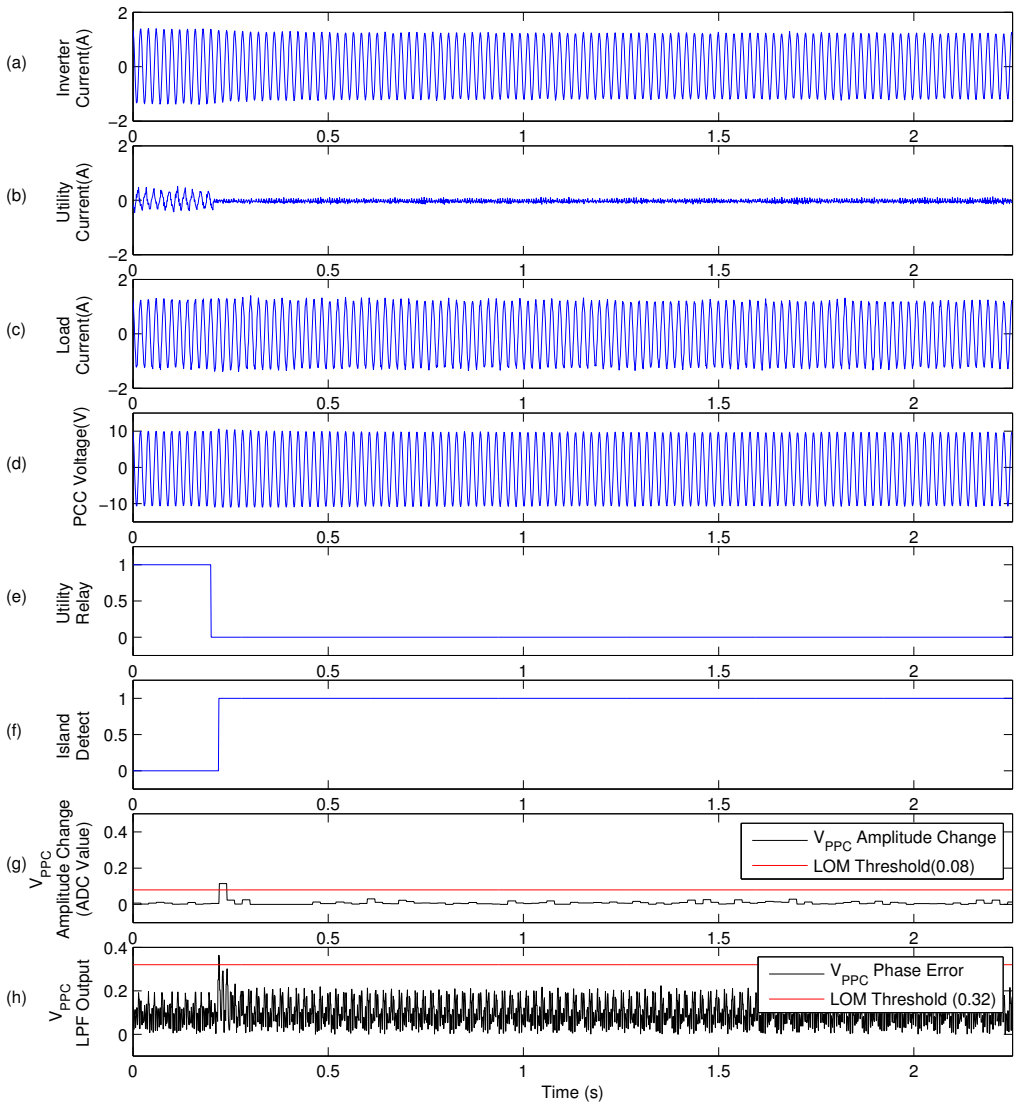

Figure 4.12: ROCOV/ROCOF experimental waveforms during a LOM event occurring at $\Delta P\%$ =10 and $\Delta Q\%$ =10 power mismatch operation

4.1.2.3 None Detection Zone

The simulation NDZ graph for the ROCOV/ROCOF LOM detection routine is shown in Figure 4.13. To generate the results for Figure 4.13, the standard LOM test was completed for operating conditions up to 20% in both real and reactive power mismatch either side of the balanced power condition. The graph shows the collection of operating conditions for which a LOM event would go undetected whilst using the ROCOV/ROCOF technique.

The NDZ for the experimental implementation of the ROCOV/ROCOF LOM detection method is shown in Figure 4.14. The standard LOM detection test was completed across a range of power mismatch operating conditions (±15% in both real and reactive power).

The NDZ for the experimental implementation is similar to the simulation NDZ

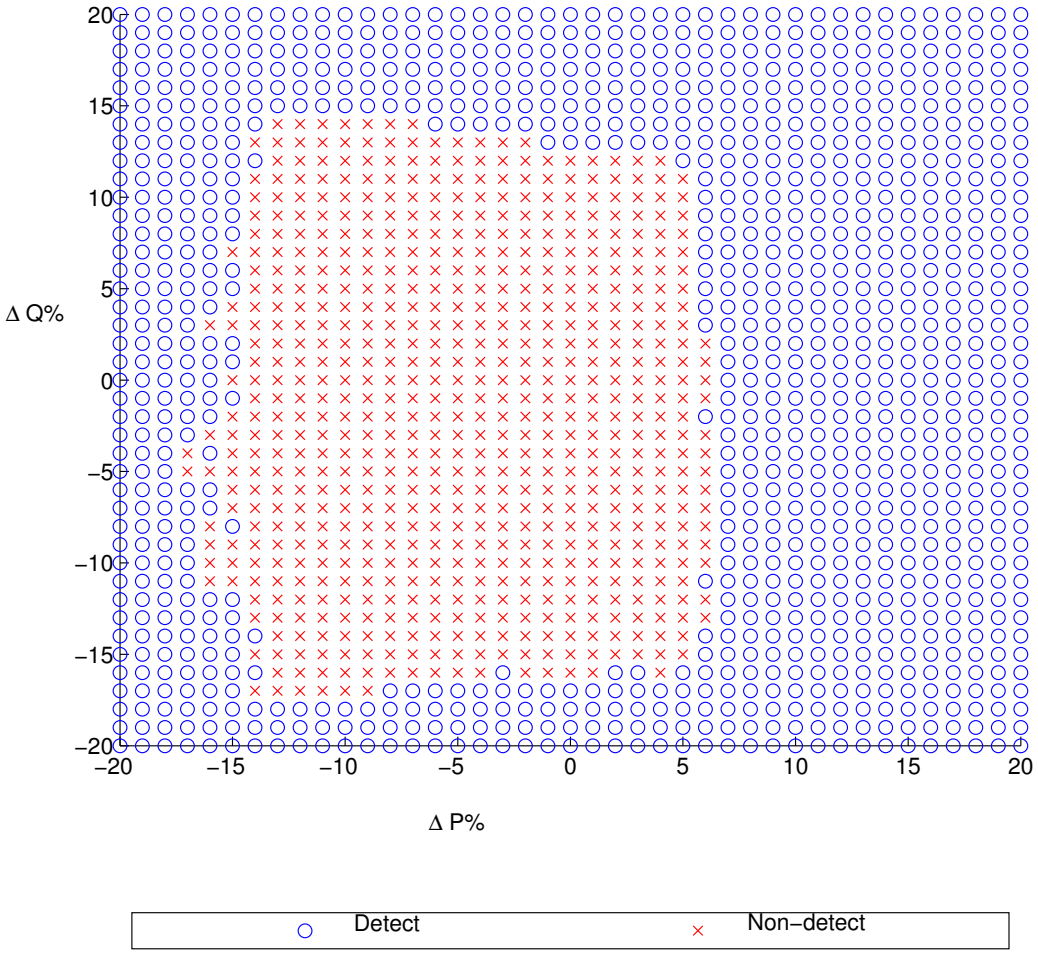

Figure 4.13: ROCOV/ROCOF simulation NDZ graph

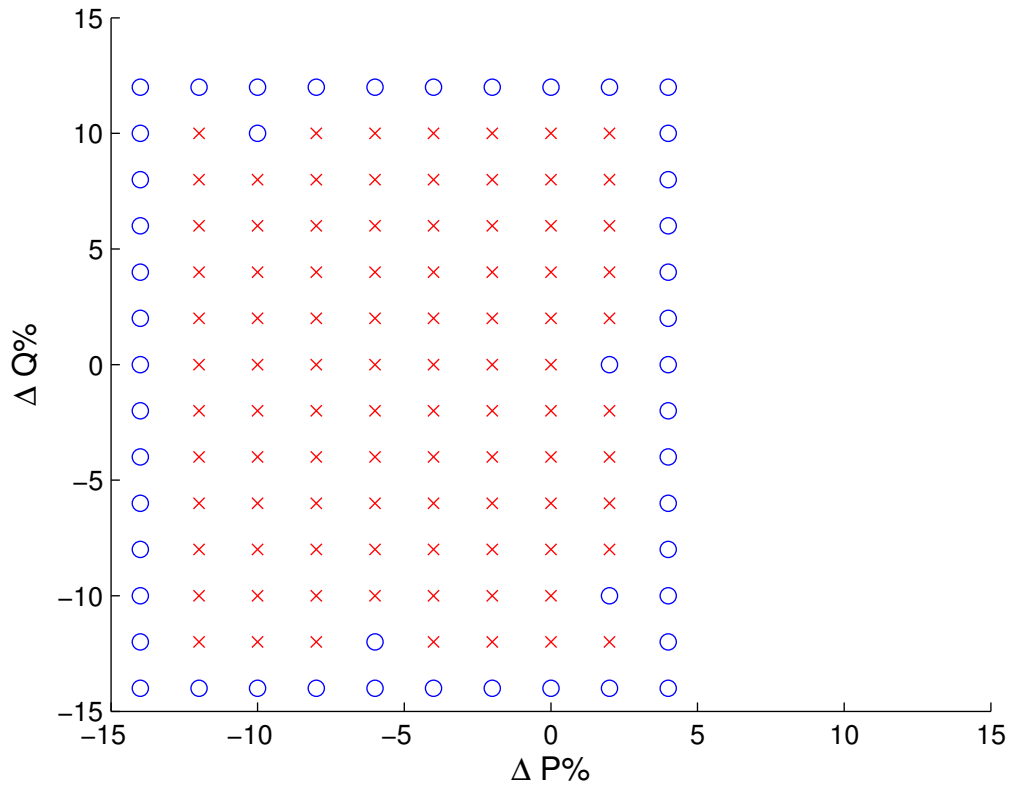

Figure 4.14: ROCOV/ROCOF experimental NDZ graph

shown in Figure 4.13 in size and shape, validating that the simulation model produces adequately accurate results for the ROCOV/ROCOF LOM detection technique.

4.1.3 Passive Techniques Discussion

The two techniques presented in this section exhibit common features normally associated with passive LOM detection techniques:

- *Non zero NDZ* - Both implemented techniques fail to detect LOM events when the power system is operating at, or close to, the balanced power condition.
- *Fast detection times* - As the systems update parameters regularly, LOM events are usually detected within one or two fundamental periods.
- *Threshold trade off* - During development the thresholds that dictate the acceptable grid connected range for the calculated parameters can be set at any level. A fundamental compromise occurs between the size of the NDZ and the probability of a false LOM indication signal being caused by grid signal fluctuations.
- *Zero effect on inverter output* - Passive LOM detection techniques have no effect on the power produced by the inverter, this is one of the main attractive attributes of passive methods.

Comparing the two systems, the under/over voltage amplitude and frequency technique was proven to have a smaller NDZ in both the simulation and experimental environments, meaning this technique successfully detects LOM events for a wider range of operating conditions.

The simulation results presented in this section match the experimental results to an acceptable degree, further validating the use of the simulation model for code development.

4.2 Active Techniques

Four active LOM detection techniques have been implemented and tested. This section describes the operation of the four methods and presents the simulation and experimental results.

As active LOM detection methods have a zero NDZ, they are instead evaluated by comparing the time it takes to detect island conditions. To demonstrate the lack of a NDZ and present a sample of typical detection delay times, each active technique undergoes the standard LOM test across a range of power mismatch levels. The detection delay times are used to compare the different active LOM detection techniques.

4.2.1 Active Power Shift

This LOM detection technique alters the demanded current magnitude periodically to prevent continuous balanced power operation occurring. By reducing the current magnitude to 80% of the rated power current demand, the real output power is reduced to 80% of the rated power. The duty ratio for the active power shift is set at 0.5, meaning the real output power is reduced every other fundamental period. The effect that this procedure has on the current reference signal, I_{REF}, is shown in Figure 4.15, with $I_{fundamental}$ representing the rated power current reference signal.

Whilst the system is grid connected, the utility maintains the measured V_{PCC} voltage during the active power shift periods by allowing active power to flow into the local load. When the constant grid voltage is not connected to the point of common coupling, the periodic change in inverter output current means that the local power generation can no longer constantly match local power consumption. This results in fluctuations in measured V_{PCC} parameters that are outside the acceptable grid connected range.

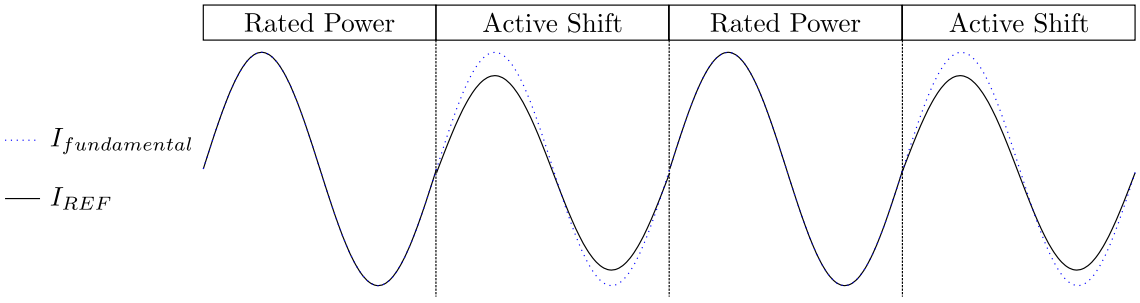

Figure 4.15: Active power shift current reference

The active power shift routine is used in conjunction with the under/over voltage amplitude and frequency LOM detection technique. The under/over voltage amplitude and frequency LOM detection technique is used to detect changes in the measured V_{PCC} parameters, caused be the active power shifting routine, that can not occur whilst the system is connected to the utility.

Figure 4.16 shows the operation block diagram of the active shift LOM detection routine. The under/over voltage amplitude and frequency routine remains unchanged from the description in Section 4.1.1 and it operates simultaneously with the active shift routine. The active shift routine is incorporated within the current control structure. The phase output of the PLL is used to allow the system to only apply the active power shift for every other fundamental period. When the routine is in the active shift sector, the amplitude demand signal from the labview panel is reduced by 20%.

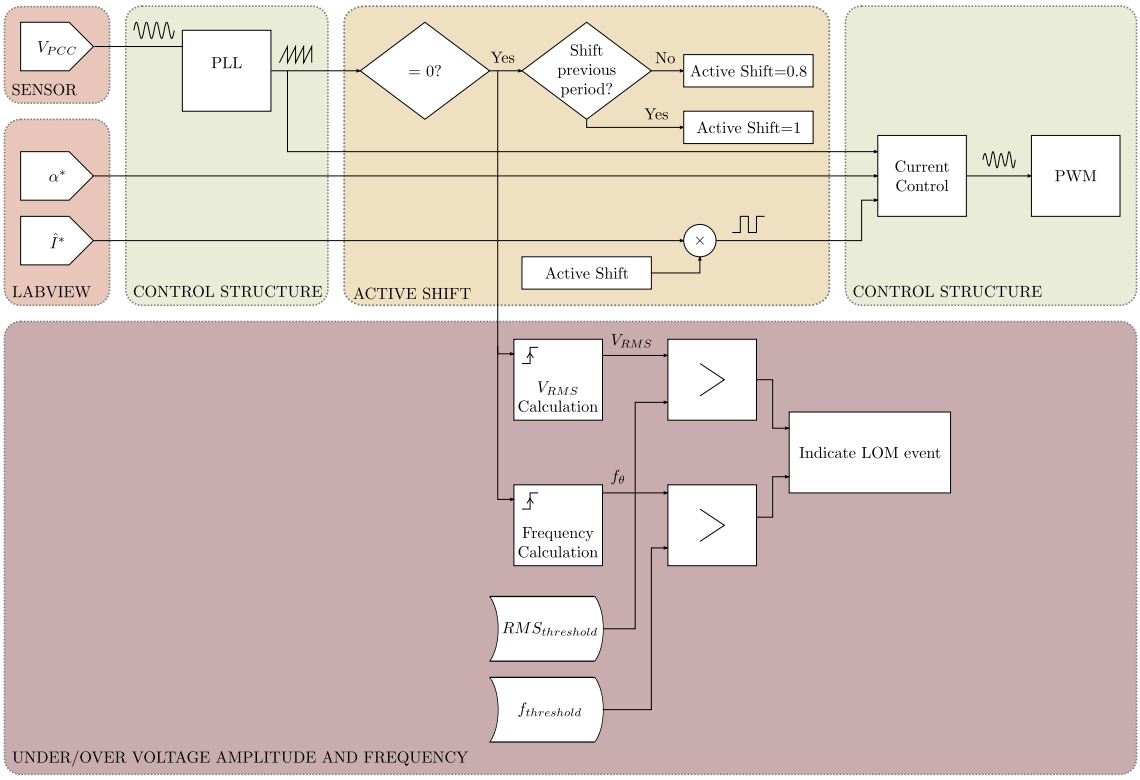

Figure 4.16: Active power shift operation block diagram

4.2.1.1 Results At Balanced Power Operation

The active shift LOM detection technique was implemented using the Simulink model and the hardware laboratory set-up. To test the routine worked, the standard LOM test was completed at balanced power, the simulation results are shown in Figure 4.17, and the corresponding experimental results are shown in Figure 4.18.

The inverter current, trace (a), can be seen to be fluctuating in amplitude because of the active shift routine. Trace (b), the utility current, can be seen to have small bursts of power flow, these bursts occur during the inverter output active shift

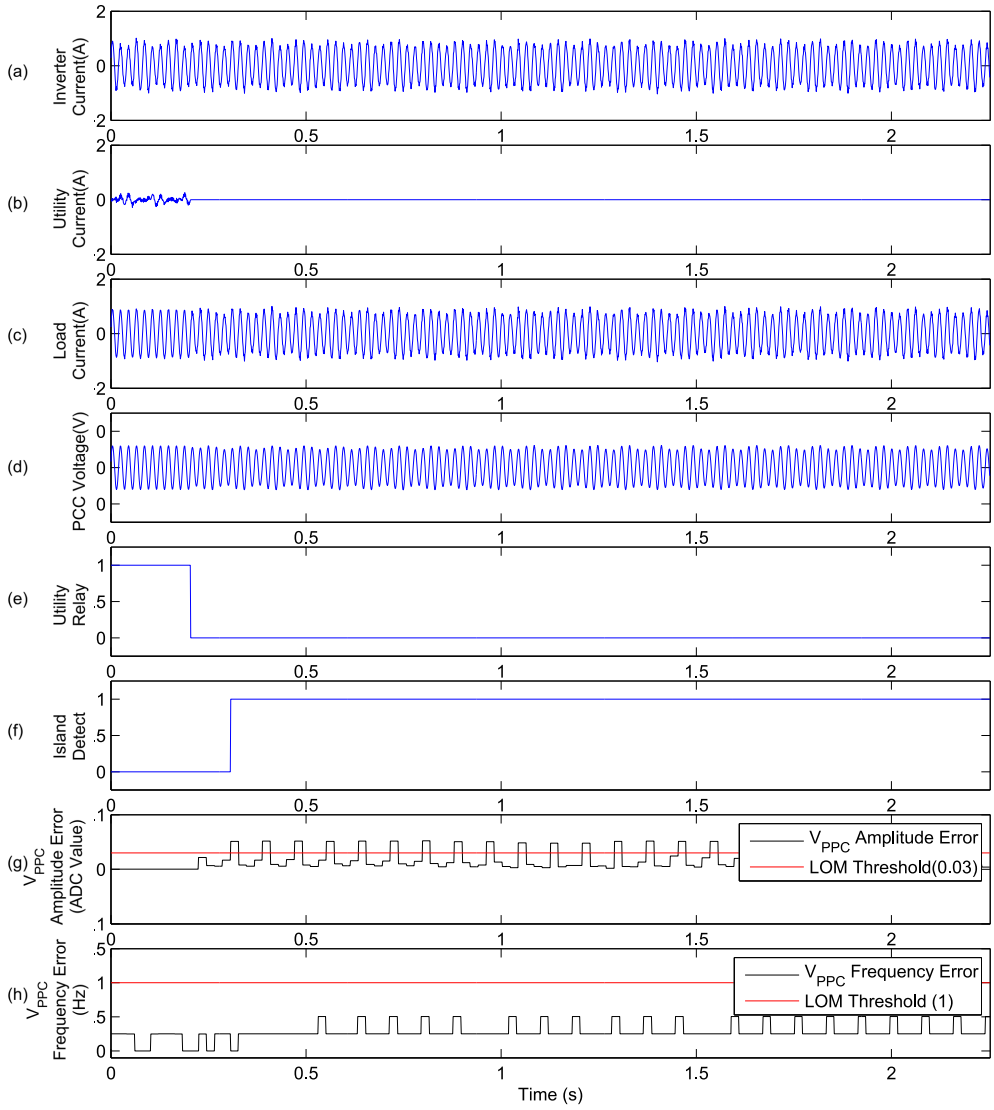

Figure 4.17: Active power shift simulation waveforms during a LOM event occurring at balanced power operation

sectors. The load current and PCC voltage, trace (c) and trace (d) respectively, show constant sinusoids before the LOM event occurs at 0.2 seconds. After the LOM event, the inverter current and PCC voltage fluctuate in amplitude, caused by the utility no longer being connected to compensate for the local power mismatch. The fluctuation of V_{PCC} causes the calculated amplitude to exceed the acceptable grid connected range, shown in trace (g), causing the system to indicate the LOM event. As the active shift does not change the frequency or phase of the inverter output current, the frequency error, trace (h), remains low and within the acceptable grid connected range.

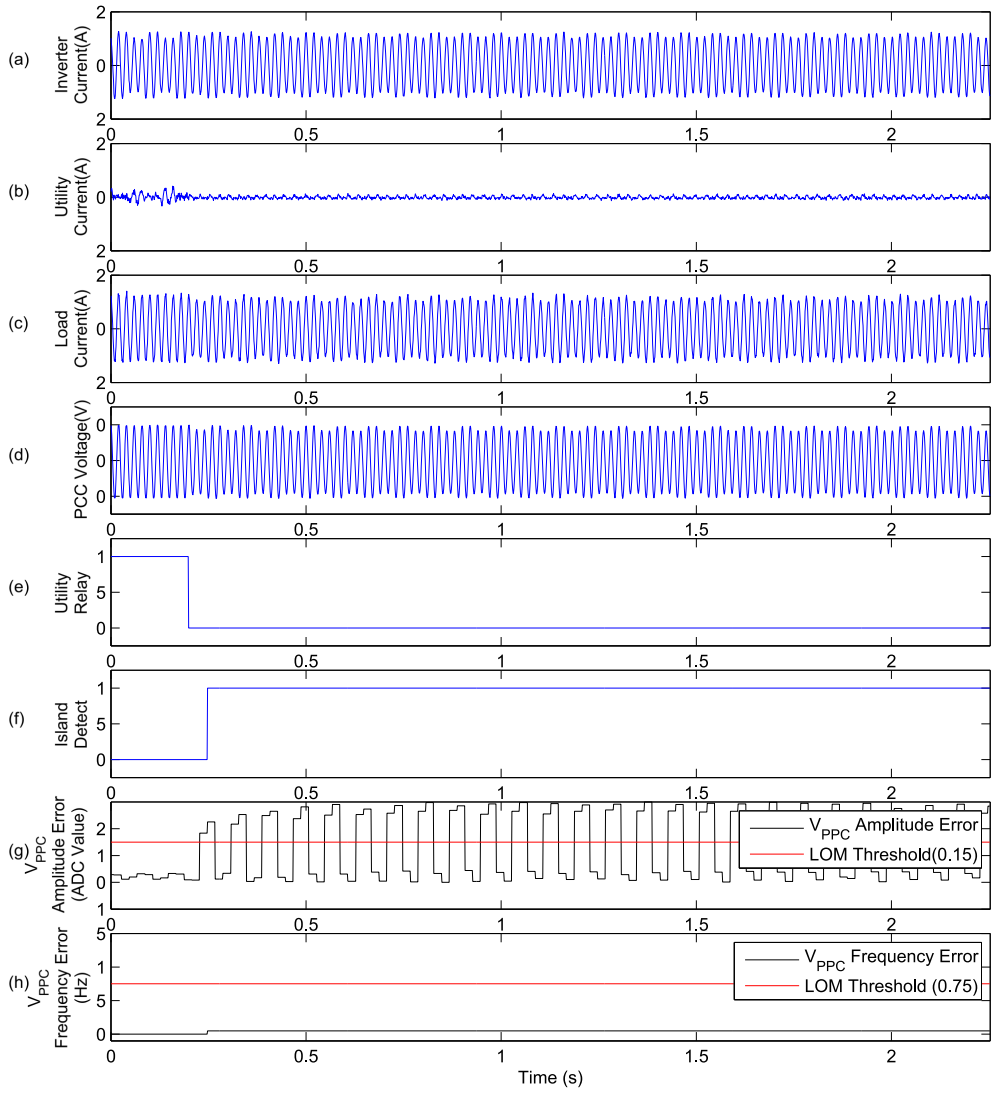

Figure 4.18: Active power shift experimental waveforms during a LOM event occurring at balanced power operation

Trace (f) shows that the LOM event is detected with a detection delay of around 0.06 seconds for the simulation environment and a detection delay of around 0.04 seconds for the experimental set-up.

4.2.1.2 Detection Delay Time

The active power shift LOM detection technique was tested across a range of operating conditions (±10% in both real and reactive power mismatch). The resultant simulation detection delay times are shown in Figure 4.19. The experimental detection delay times are shown in Figure 4.20. Both 3D plots indicate similar levels of magnitude of detection delay time for the active shift LOM detection routine. The detection delay times are generally below 0.1 seconds, meaning the LOM events are detected within 5 fundamental waveforms.

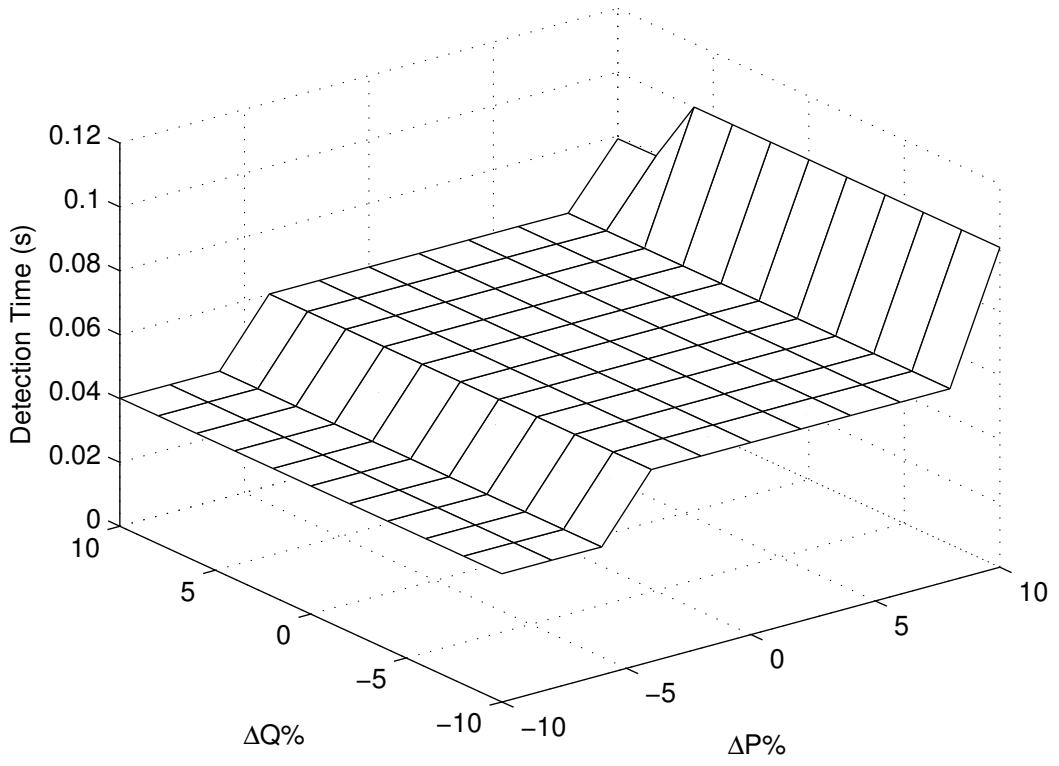

Figure 4.19: Active power shift simulation detection delay graph

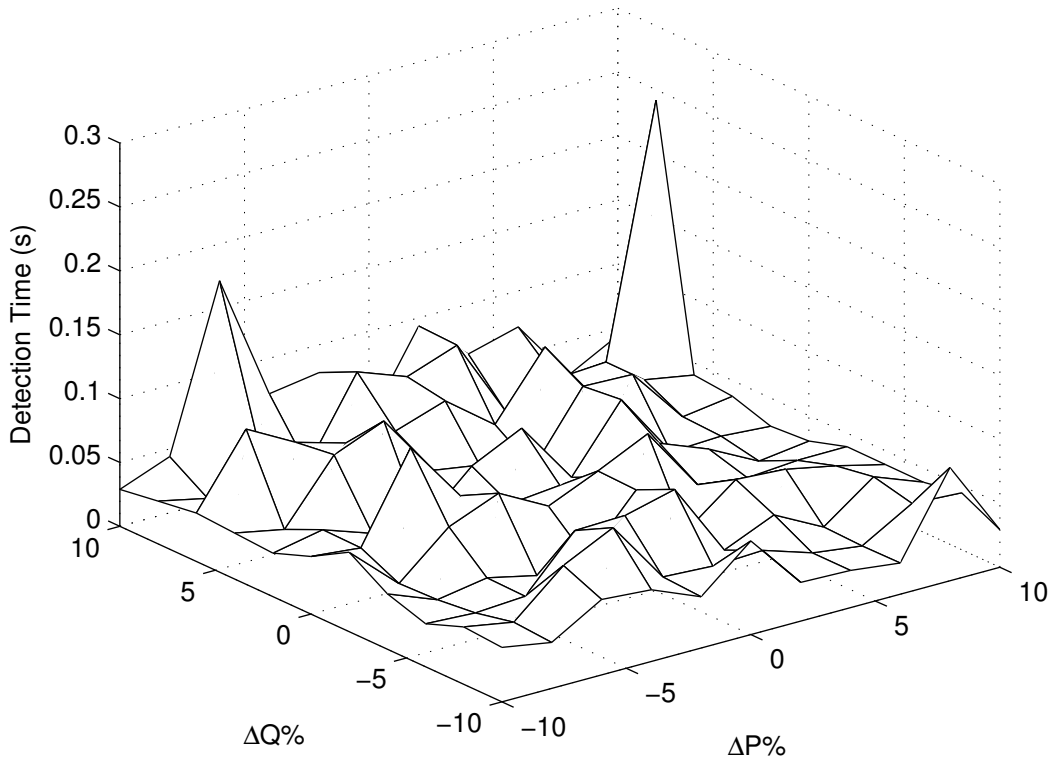

Figure 4.20: Active power shift experimental detection delay graph. Error analysis in Section 5.6.4

4.2.2 Reactive Power Shift

This LOM technique periodically changes the amount of reactive power the inverter is generating. By altering the phase and magnitude of the inverter output current, the reactive power can be changed so that the power system is less likely to continuously operate at the balanced power condition. The inverter current demand signal, I_{REF}, is shown in Figure 4.21, with $I_{fundamental}$ representing the reference current without the reactive shift routine operating.

Whilst the grid connection is present, reactive power is exchanged with the utility, compensating for the reactive power mismatch on the local power network. This facilitates the maintenance of the V_{PCC} voltage within the acceptable grid connected range. If a LOM event occurs, the local reactive power mismatch will result in fluctutions of the V_{PCC} voltage.

As with the active power shift LOM detection technique presented in Section 4.2.1, the reactive power shift routine operates in conjunction with the under/over voltage amplitude and frequency LOM detection technique. The under/over voltage amplitude and frequency routine is used to detect the fluctuations in V_{PCC} parameters caused by the periodic reactive power shift. The operation block diagram is shown in Figure 4.22. The reactive power shift routine is synchronised with the PLL output phase to allow the reactive shift procedure to be applied to every other fundamental period, giving a duty ratio of 0.5.

To complete the standard LOM test across a range of power mismatch levels, the communications with the Labview control panel had to be altered. Instead of the current phase and magnitude demand being calculated within the Labview program, as described in section Section 3.4.3.2, the calculation is completed within the current control structure to allow periodic alterations. The controller receives the demanded active and reactive power mismatch levels, $\Delta P\%$ and $\Delta Q\%$ respectively, from the Labview control panel. The reactive shift routine periodically reduces $\Delta Q\%$ by 20%,

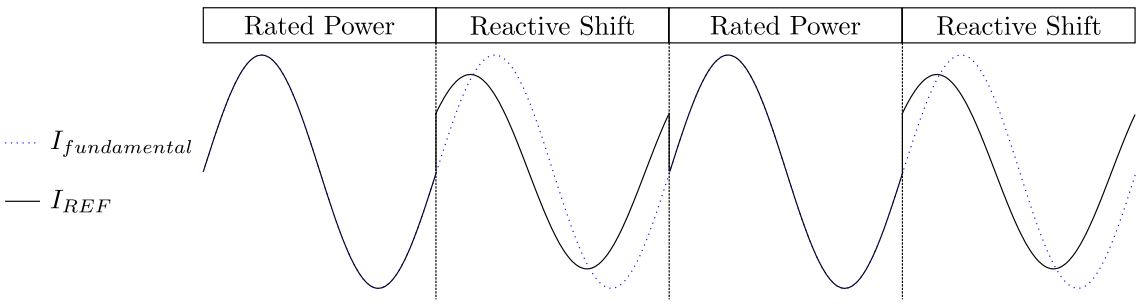

Figure 4.21: Reactive power shift current reference

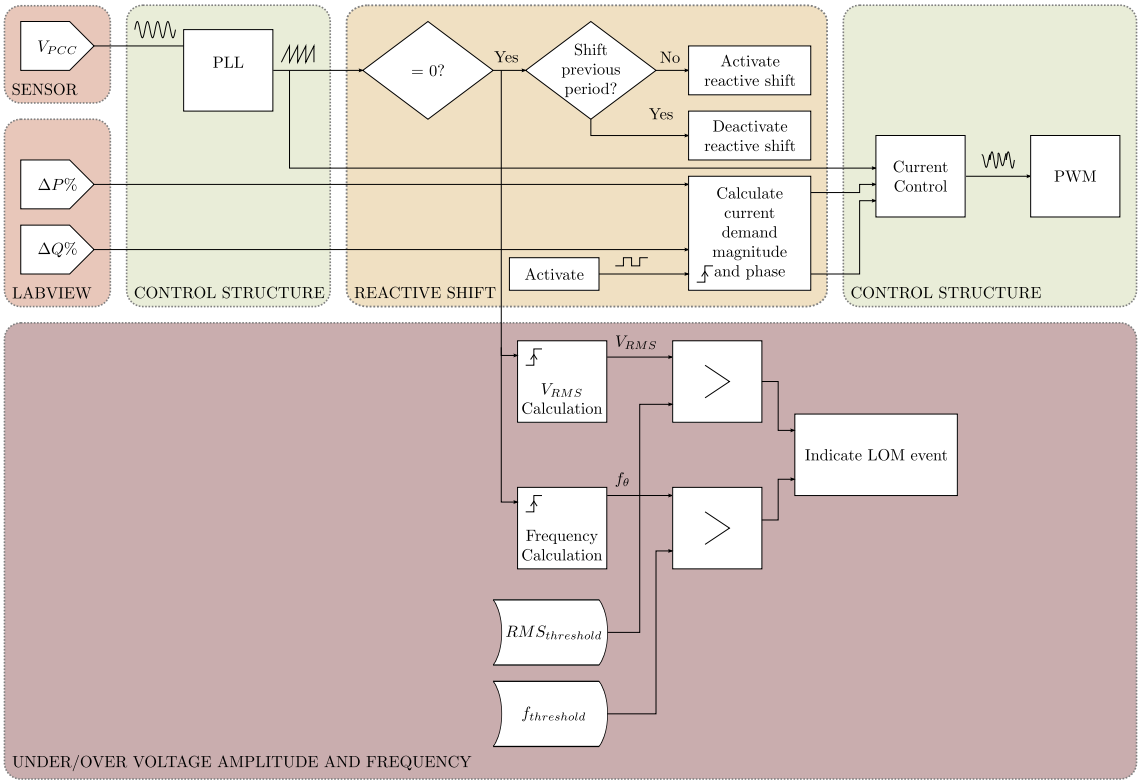

Figure 4.22: Reactive power shift block diagram

allowing Equations 4.3 and 4.4 to be used to calculate the current demand phase and magnitude, α^* and $\hat{I}^*$ respectively:

$$\alpha^* = \arctan\left(\frac{Q^*}{P^*}\right) \tag{4.3}$$

$$\hat{I}^* = \sqrt{2}\left(\frac{|S^*|}{|V|}\right) \tag{4.4}$$

where

$$P^* = \frac{\Delta P\% + 100}{100} \times |\kappa|, \qquad Q^* = \frac{\Delta Q\%}{100} \times |\kappa|, \qquad |S^*| = \sqrt{P^* + Q^*} \tag{4.5}$$

with $|\kappa|$ representing the power output at the balanced power operating condition and $|V|$ representing the V_{PCC} magnitude.

4.2.2.1 Results At Balanced Power Operation

The standard LOM detection test was completed during the balanced power condition with the reactive power shift routine operating. The resultant simulation waveforms are shown in Figure 4.23, and the experimental results are shown in Figure 4.24.

Trace (b) shows the periodic bursts in non zero utility current, caused by the reactive power shift routine, before the LOM event occurs at 0.2 seconds. The calculated voltage amplitude and frequency, trace (g) and trace (h) respectively, show that

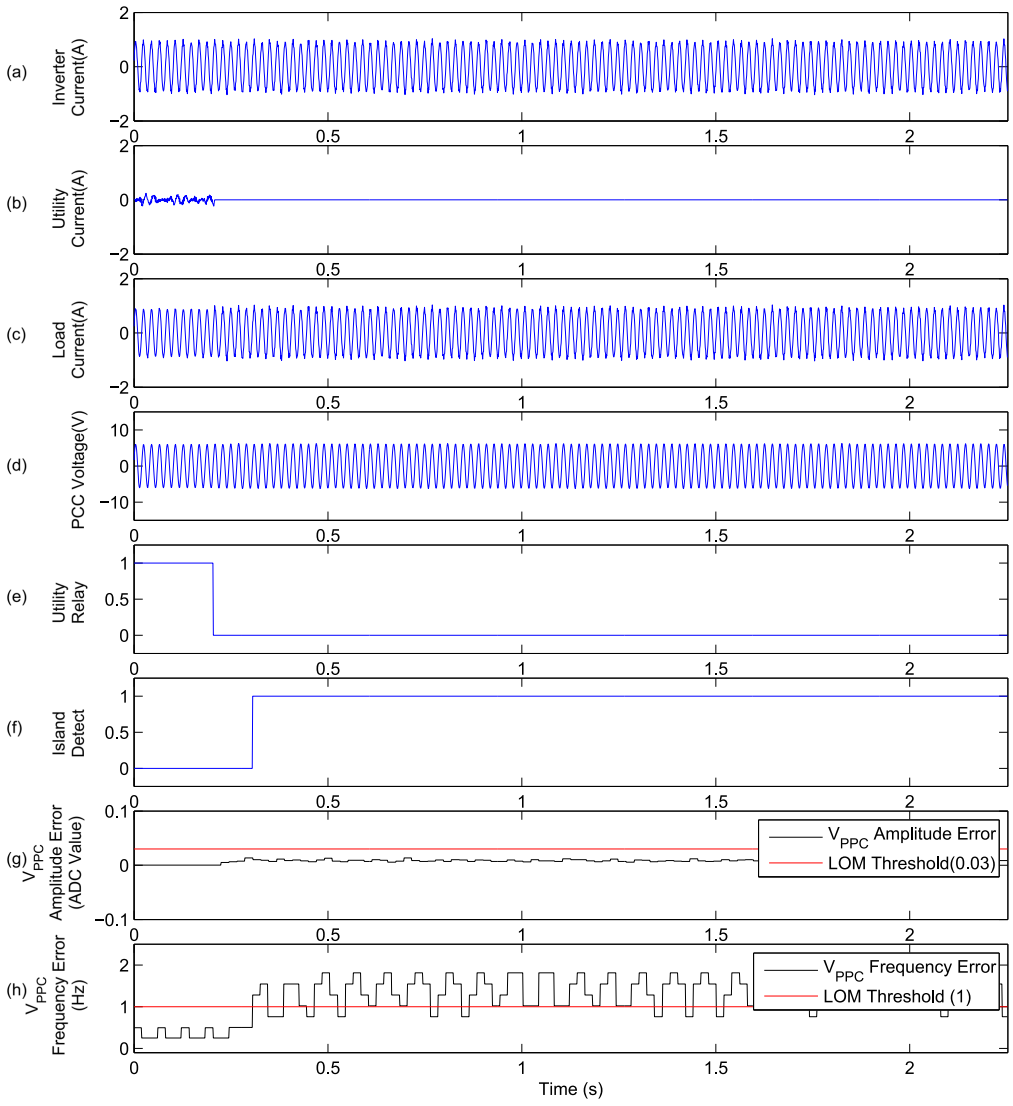

Figure 4.23: Reactive power shift simulation waveforms during a LOM event occurring at balanced power operation

the measured V_{PCC} parameters remain within the acceptable grid connected range before the LOM event. Although it is hard to display the changes in the V_{PCC} voltage, trace (d), that occur after the LOM event, the frequency parameter can be seen to quickly deviate outside of the acceptable grid connected range. This causes the under/over frequency routine to signal the LOM event, shown in trace (f).

The simulation detection delay, calculated using the standard LOM test, for balanced power operation is around 0.1 seconds and the corresponding experimental detection delay is around 0.06 seconds.

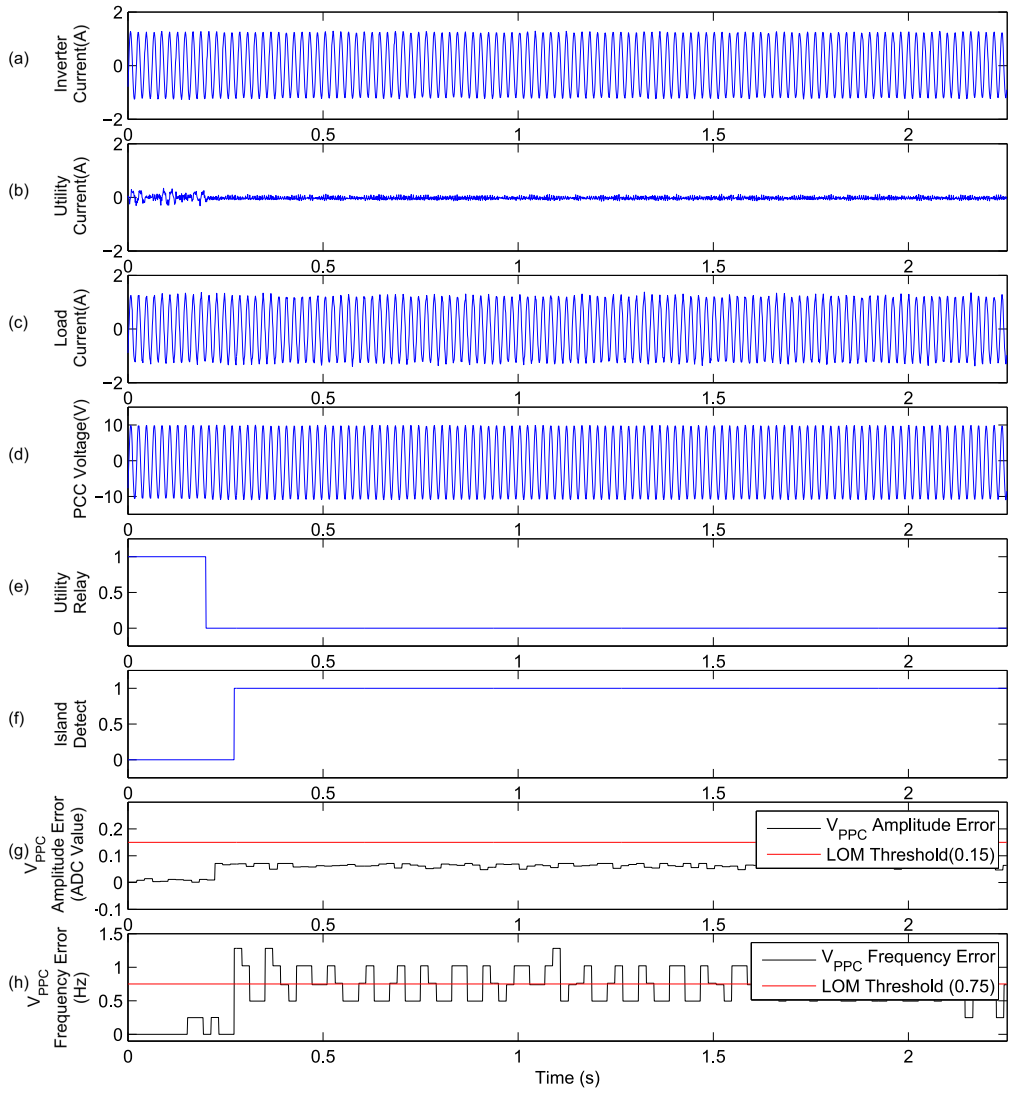

Figure 4.24: Reactive power shift experimental waveforms during a LOM event occurring at balanced power operation

4.2.2.2 Detection Delay Time

The reactive shift LOM detection technique was tested across a range of operating conditions (±10% in both real and reactive power mismatch) using both the simulation environment and the experimental set-up. The resultant simulation detection delay times are shown in Figure 4.25. The resultant experimental detection delay times are shown in Figure 4.26.

The simulation results, Figure 4.25, are very consistent with a maximum detection delay of around 0.35 seconds.

The experimental results, Figure 4.26, are generally shorter than the corresponding simulation results and show very consistent detection delay times. The spike experienced at the $\Delta P\%$ =-10 and $\Delta Q\%$ =6 operating point can be considered slightly anomalous, caused simply by the LOM event occurring part way through a parameter calculation, meaning the full effect of the reactive power shift routine takes longer to propagate through the detection process. Whilst it does not represent any flaw in the detection method, the anomalous result is included to demonstrate that large deviations from the average delay time can occur.

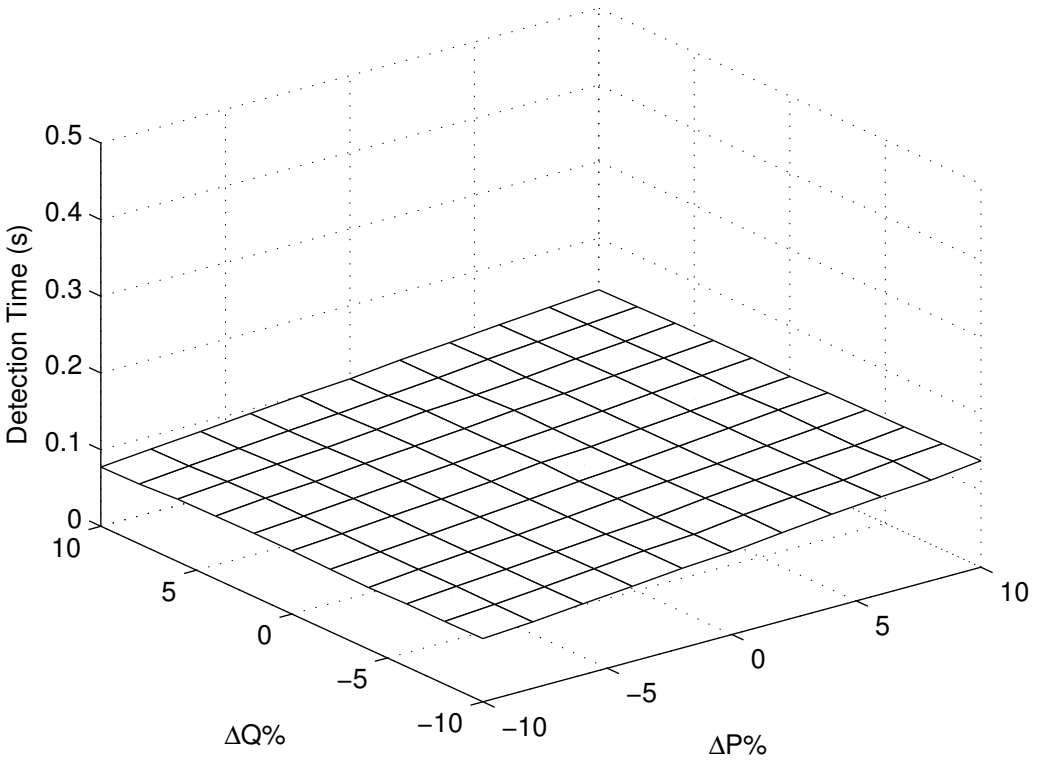

Figure 4.25: Reactive power shift simulation detection delay graph

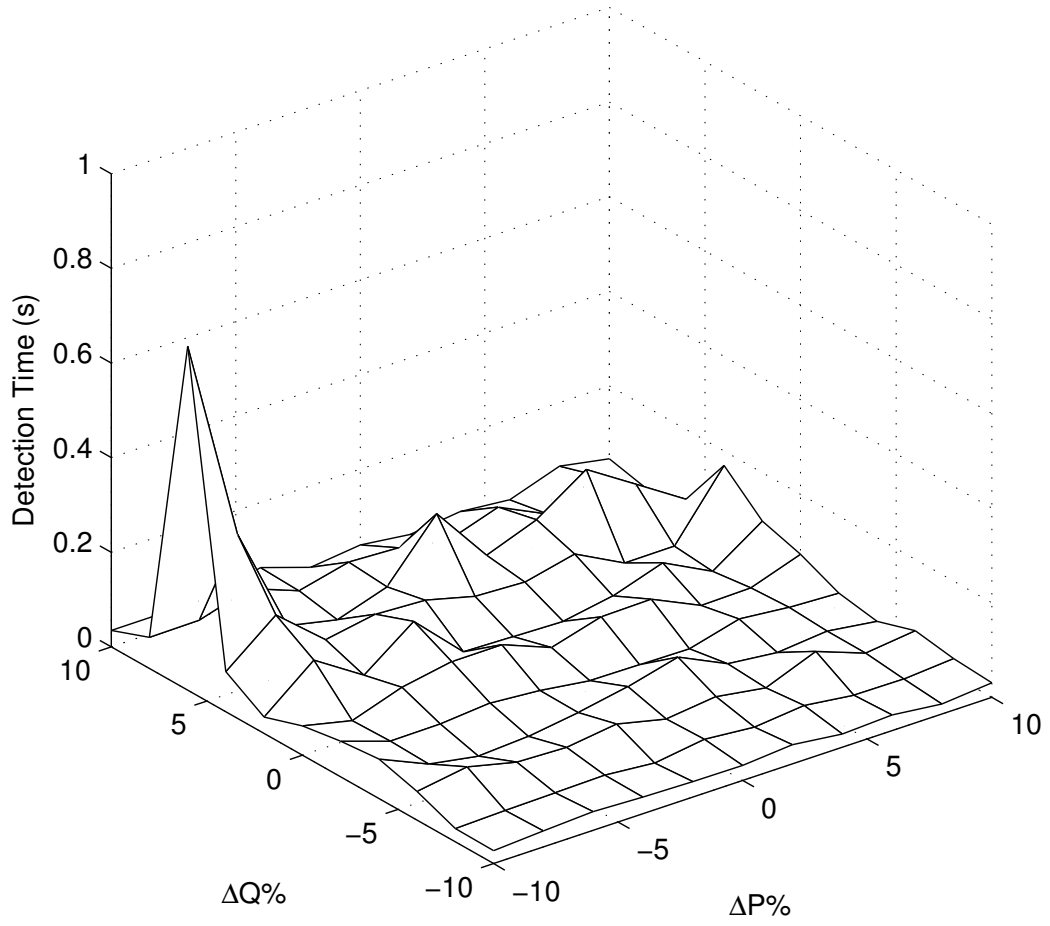

Figure 4.26: Reactive power shift experimental detection delay graph. Error analysis in Section 5.6.4

4.2.3 Second Harmonic Injection

This LOM detection method continuously injects a second harmonic component within the inverter output current. The level of the 100 Hz component in the measured voltage is constantly monitored. When the utility is connected, the low impedance of the grid means that the second harmonic component within the output current of the inverter flows into the grid. This causes the second harmonic level in the measured V_{PCC} voltage to be low. After a LOM event, the impedance of the power network rises considerably, causing the 100 Hz component in the current to appear in the measured V_{PCC}.

The operation block diagram for the second harmonic injection technique is shown in Figure 4.27. The addition of the 100 Hz current component is completed within the current control structure. The 100 Hz component is synchronised with the fundamental current waveform so as not to alter the zero crossing time of the final current reference. The injected harmonic level used is 2% of the fundamental amplitude.

A digital filter is used to isolate the 100 Hz component detected within the measured V_{PCC} voltage. The filter is a 32^{nd} order bandpass filter centred on 100 Hz. The output of the filter is proportional to the level of the 100 Hz component in V_{PCC}. To reduce the likelihood of false trips resulting from short fluctuations in the filter output signal caused by network changes, a new variable is calculated, named island strength. The island strength variable is a simple timer which dictates that the filter output must exceed the acceptable grid connected range, dictated using a

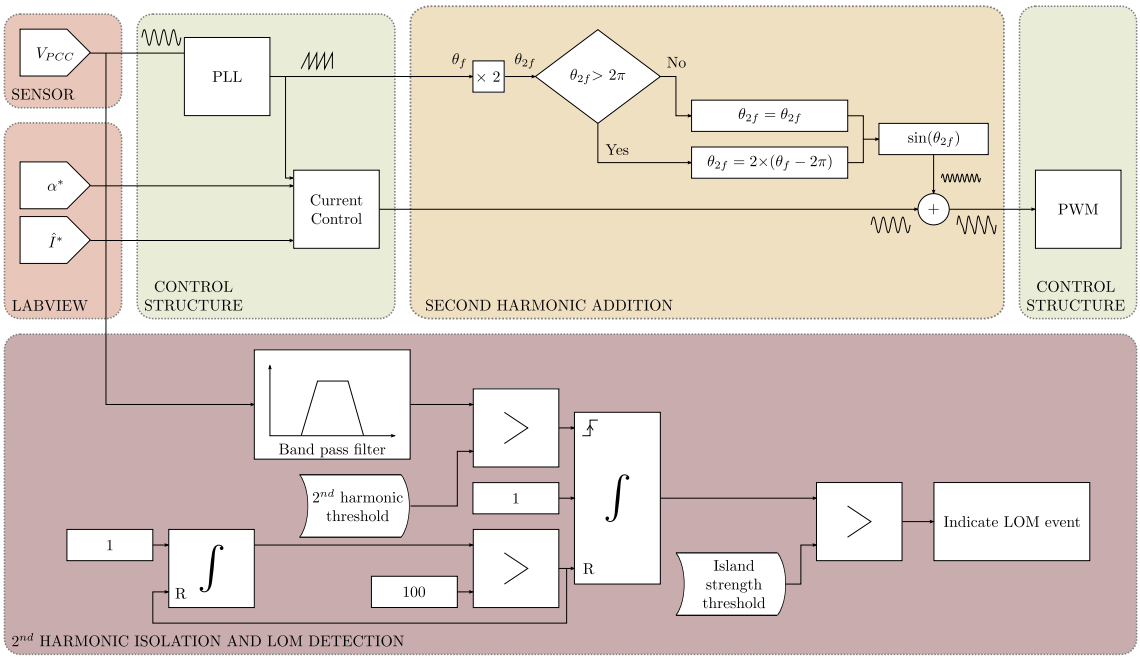

Figure 4.27: Second harmonic injection block diagram

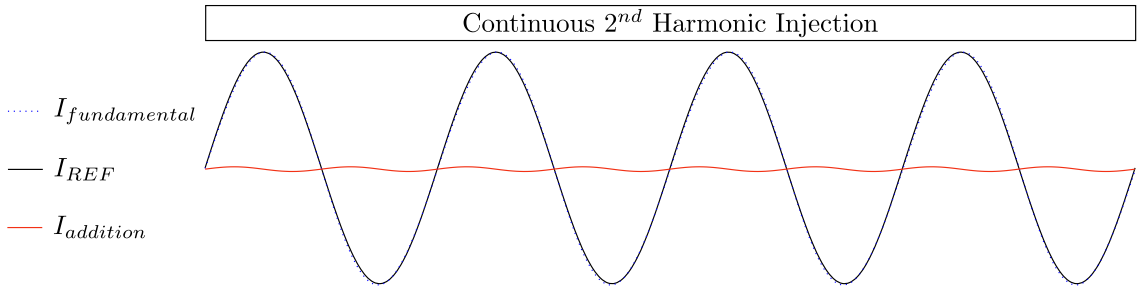

Figure 4.28: Actual second harmonic injection current reference

threshold, for more than 20 samples (0.002 seconds). The island strength variable is reset every 0.01 seconds, meaning the filter output must exceed the LOM threshold for a duration of 0.002 seconds within a period of 0.01 seconds for a LOM event to be indicated.

The threshold for the acceptable grid connected range of the V_{PCC} 100 Hz component magnitude was set during development of the routine. For the experimental laboratory set-up it was set at 10% above the maximum recorded filter output during a prolonged operation test.

The effect on the current reference, I_{REF}, caused by the second harmonic injection routine is shown in Figure 4.28

To clarify how the resultant I_{REF} signal will be altered, Figure 4.29 shows the injected signal, $I_{addition}$, and the effect that it has on I_{REF} at ten times the actual amplitude used. It can be seen that the second harmonic injection routine has no effect on the zero crossing times of the current reference signal.

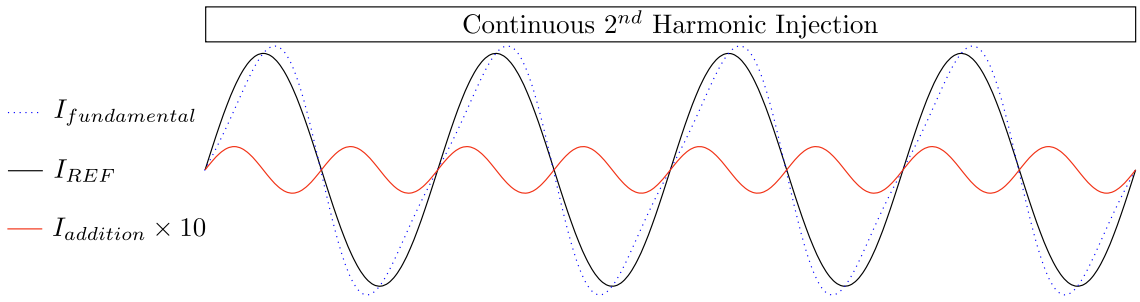

Figure 4.29: Multiplied second harmonic injection current reference

4.2.3.1 Results At Balanced Power Operation

The resultant waveforms for the simulation implementation of the second harmonic injection LOM detection technique are shown in Figure 4.30 and the corresponding experimental results are shown in Figure 4.31.

Both simulation and experimental results indicate that a very small amount of power is exchanged with the utility before the LOM event. This is indicated by the slightly larger fluctuations in utility current that can be seen before 0.2 seconds on trace (b). The small amount of utility power exchange is caused by the second harmonic

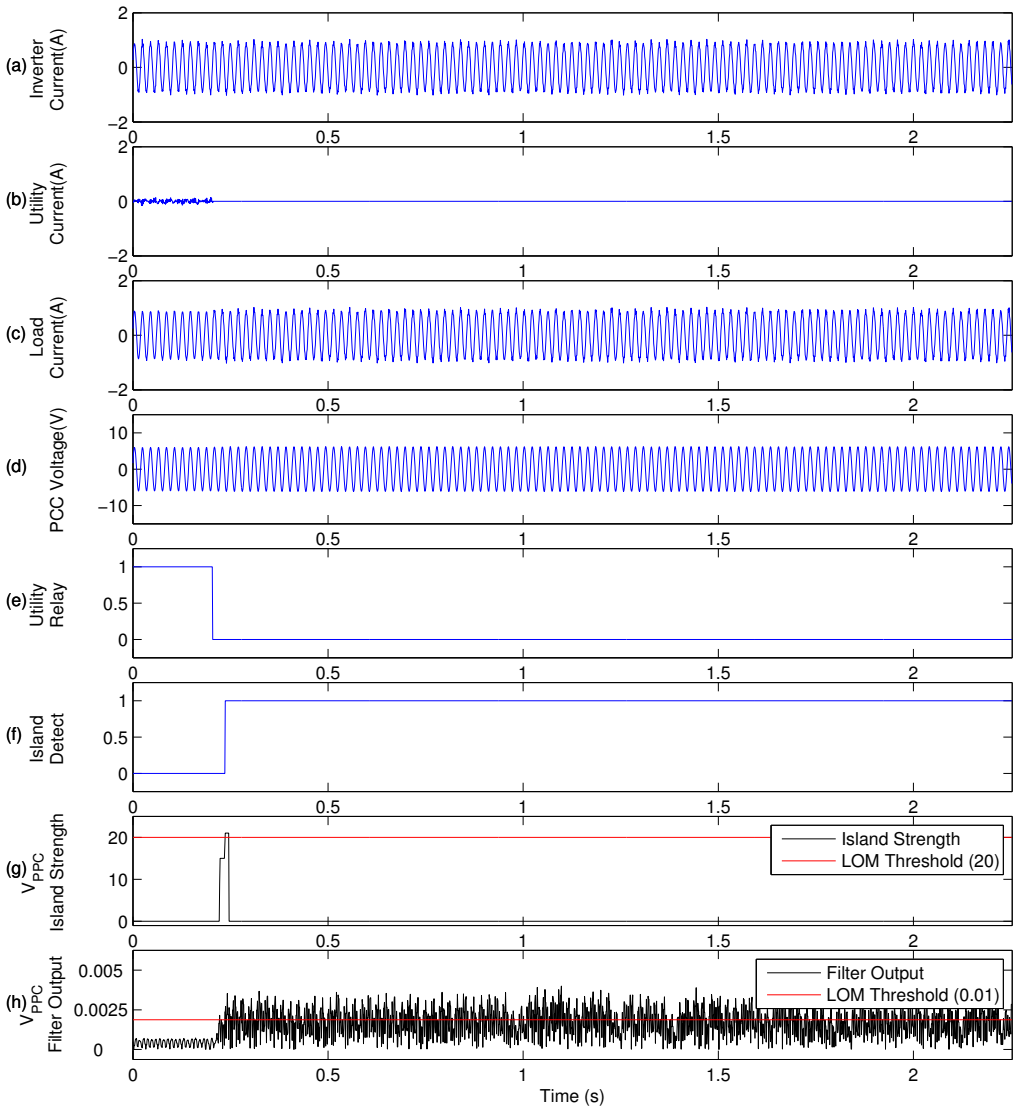

Figure 4.30: Second harmonic injection simulation waveforms during a LOM event occurring at balanced power operation

injection routine. Whilst no change in the measured V_{PCC} waveform can be observed on trace (d), the filter output value can be seen to rise substantially after the LOM event, as shown in trace (h). Each time the filter output value exceeds the LOM threshold, the island strength variable is incremented. Once the system experiences 20 filter output values that exceed the LOM threshold within a period of 0.01 seconds, as seen in trace (g), the LOM event is indicated, trace (f). During this LOM routine the system was allowed to operate until the end of the test, at 2.2 seconds, however, the island strength variable is no longer incremented once a LOM event has been detected.

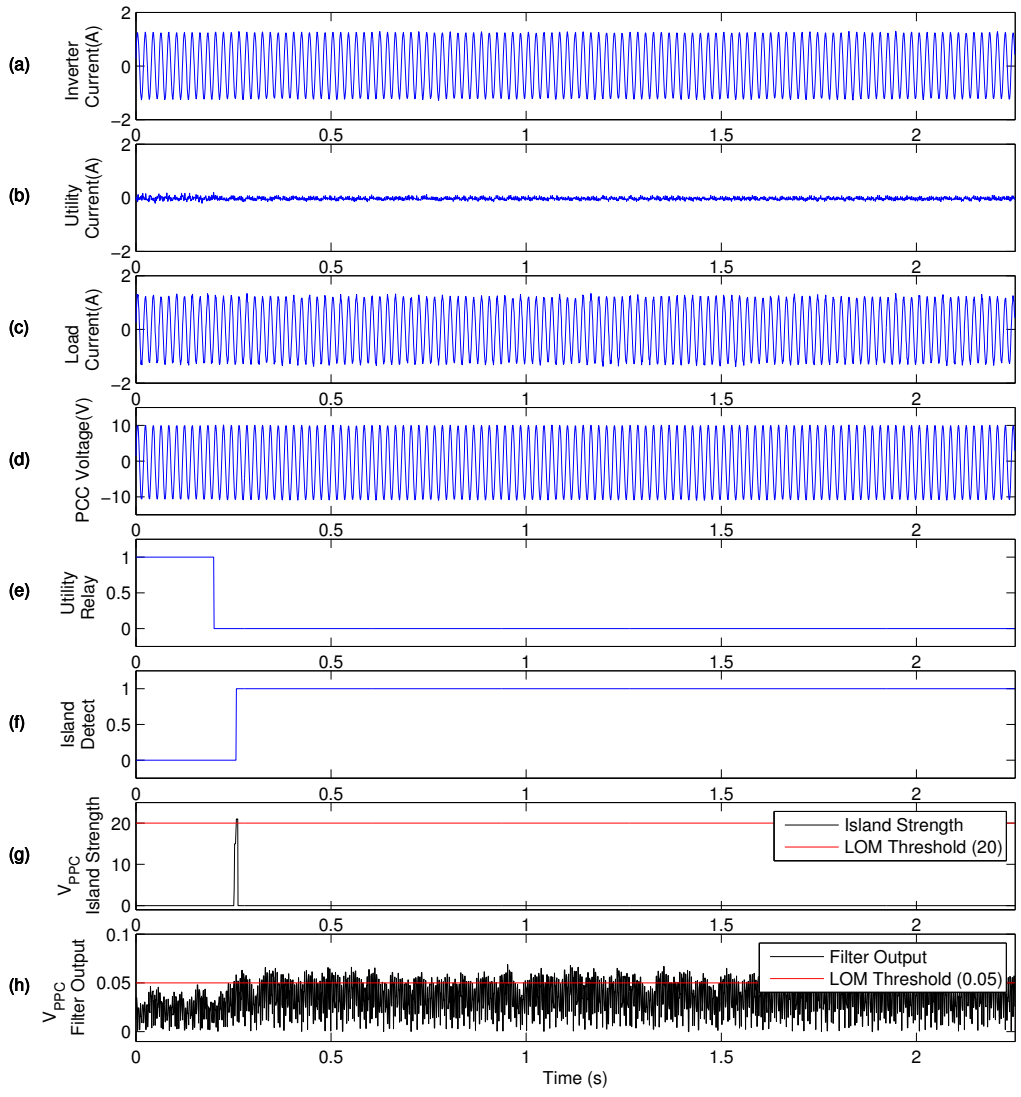

Figure 4.31: Second harmonic injection experimental waveforms during a LOM event occurring at balanced power operation

4.2.3.2 Detection Delay Time

The second harmonic injection LOM detection technique was tested across a range of operating conditions (±10% in both real and reactive power mismatch). The resultant simulation detection delay times are shown in Figure 4.32 and the experimental detection delay times are shown in Figure 4.33.

The results show that the second harmonic injection LOM detection method produces very short detection delay times, consistently detecting the LOM event within a time of around 0.05 seconds. The simulation implementation produces slightly faster detection delay times.

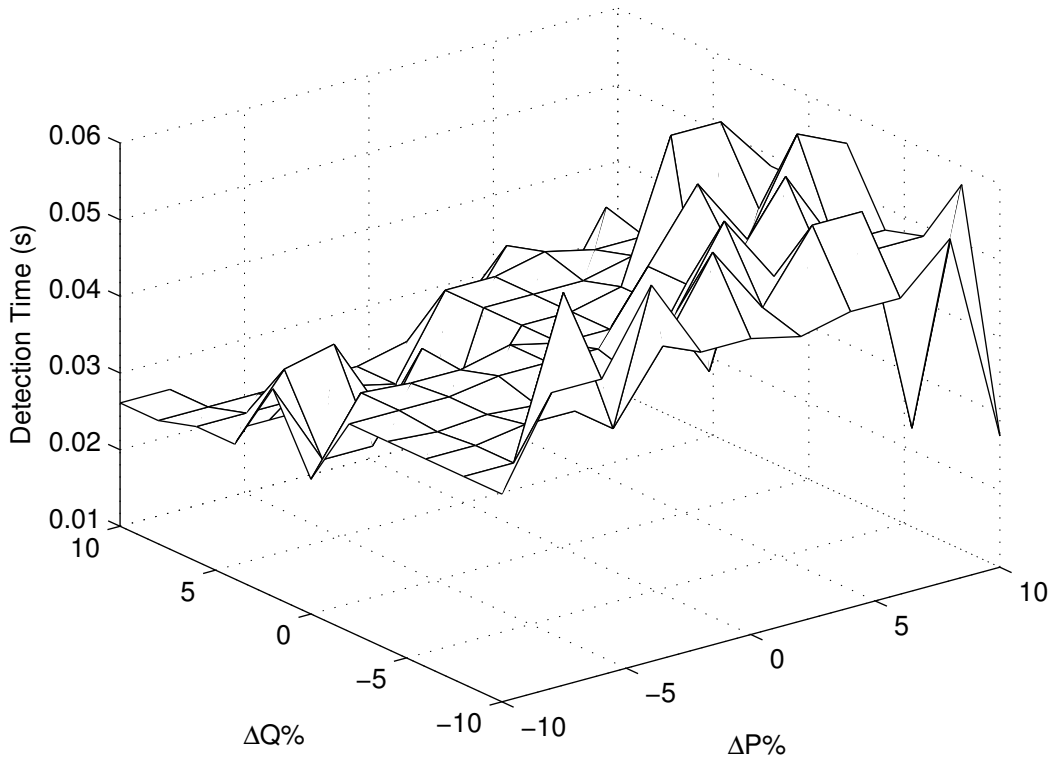

Figure 4.32: Second harmonic injection simulation detection delay graph

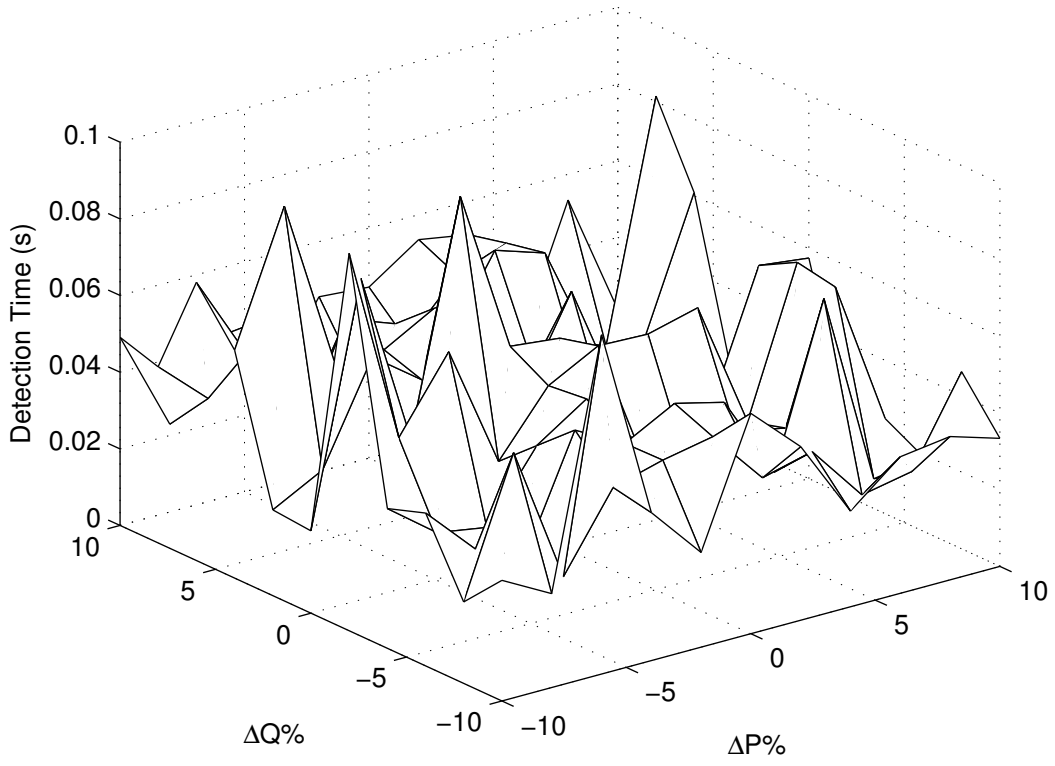

Figure 4.33: Second harmonic injection experimental detection delay graph. Error analysis in Section 5.6.4

4.2.4 Zero Current Pulse

This LOM detection technique intermittently outputs a short burst of zero current. When the system is connected to the utility, the grid can compensate for this short period of power mismatch, hence, the measured V_{PCC} voltage is not effected. If the connection with the utility is lost, the zero current burst affects the level of V_{PCC}, causing a rapid voltage change. As a zero current burst would result in a rapid change in V_{PCC}, the derivative of V_{PCC} is calculated and compared to an island threshold.

The resultant current reference, I_{REF}, is shown in Figure 4.34. During system development it was decided to only output a zero current pulse in one out of every four fundamental waveforms, however, this could be more or less frequent. The position of the zero current pulse is not constant with the position shown in Figure 4.34, with the actual position being chosen at random between 0 and 2π. This reduces the chance that any regular voltage disturbance will be mistaken for the effects of the zero current pulse. The zero current pulse duration is 0.001 seconds.

The operation block diagram for the zero current pulse technique is shown in Figure 4.35. The routine which modifies the current reference to include the zero current pulse is incorporated within the standard control structure to allow it to be accurately synchronised with the PLL output. A short code section includes a counter to signal once every four times the PLL phase is reset, this is used to activate the zero current pulse sequence. When the zero current pulse sequence is activated, the system calculates a random number between 0 and 2π. This is used as the centre point of the zero current pulse window. The zero current pulse window centre point is used to calculate the start point and the end point of the zero current pulse, by adding and subtracting $2\pi/36$, the equivalent of around 0.0005 seconds either side.

The same zero current pulse window centre point is used in the LOM detection routine. In the LOM detection routine the zero current pulse centre point is used to calculate an observation window. To reduce the likelihood of false trips, the

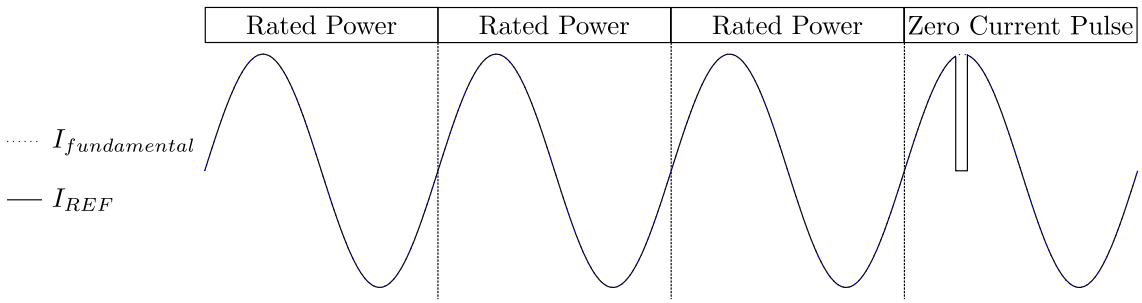

Figure 4.34: Zero current pulse current reference

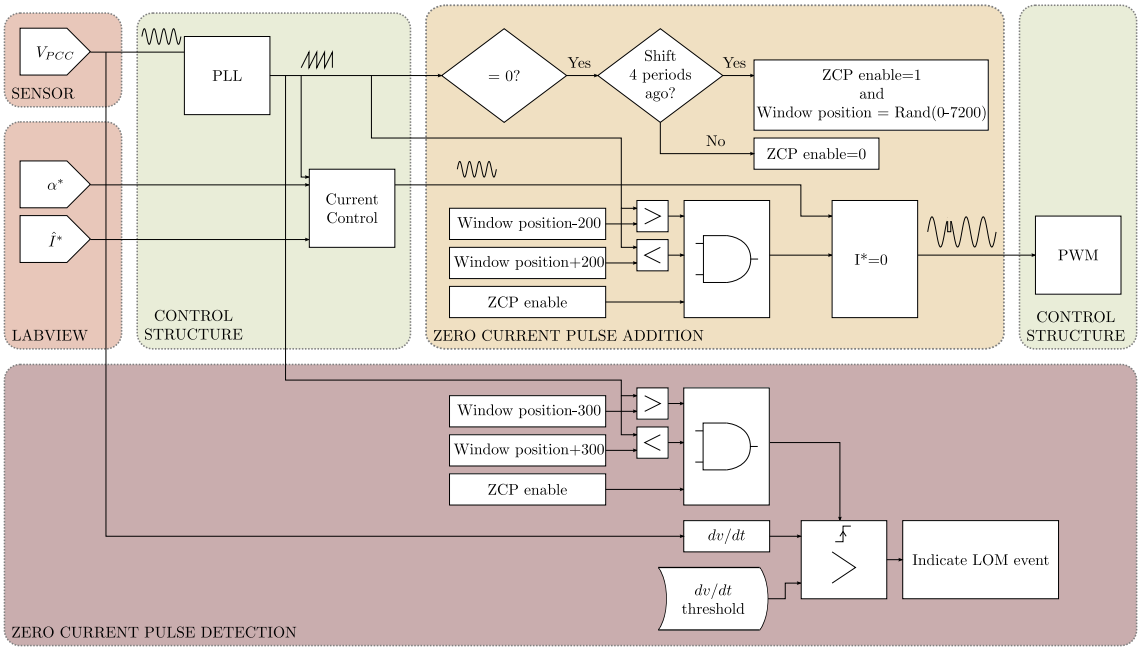

Figure 4.35: Zero current pulse block diagram

observation window is generated to restrict the routine to only check the differential of V_{PCC} against the LOM threshold at the same time that the zero current pulse is added to the output current reference. The observation window is generated by adding and subtracting $2\pi/24$, the equivalent of around 0.00083 seconds either side of the zero current pulse window centre point. The observation window is slightly larger than the zero current pulse window to allow any V_{PCC} voltage changes to propagate through the system within the observation window.

4.2.4.1 Results At Balance Power Operation

The simulation model waveforms obtained during the standard LOM test at balanced power are shown in Figure 4.36 and the experimental results are shown in Figure 4.37.

The changes in the inverter current, trace (a), are apparent throughout the test, however they only appear in the measured load current, trace (c), after the LOM event at 0.2 seconds, with the utility current, trace (b), compensating for the short bursts in local power mismatch. The power compensation means that the short bursts of power mismatch only result in V_{PCC} voltage changes after the LOM event. Hence, only large calculated V_{PCC} differentials appear after the LOM event, shown clearly in simulation trace (g). The experimental test procedure was altered slightly from the simulation tests. This was due to the relatively low sampling rate used to record the results. The short length of the changes in the voltage differential meant that they were not always recorded by the data logging process. Therefore, the

system was changed to record the maximum differential so that the increase in dv/dt can be presented in experimental trace (g). Trace (h) shows the observation window, during which, any dv/dt value above the LOM threshold will result in the indication of a LOM event. Both the simulation and experimental results demonstrate that the LOM event is detected, trace (f). The detection delay time for the simulation test is around 0.015 seconds, compared to a detection delay of around 0.04 seconds for the experimental set-up.

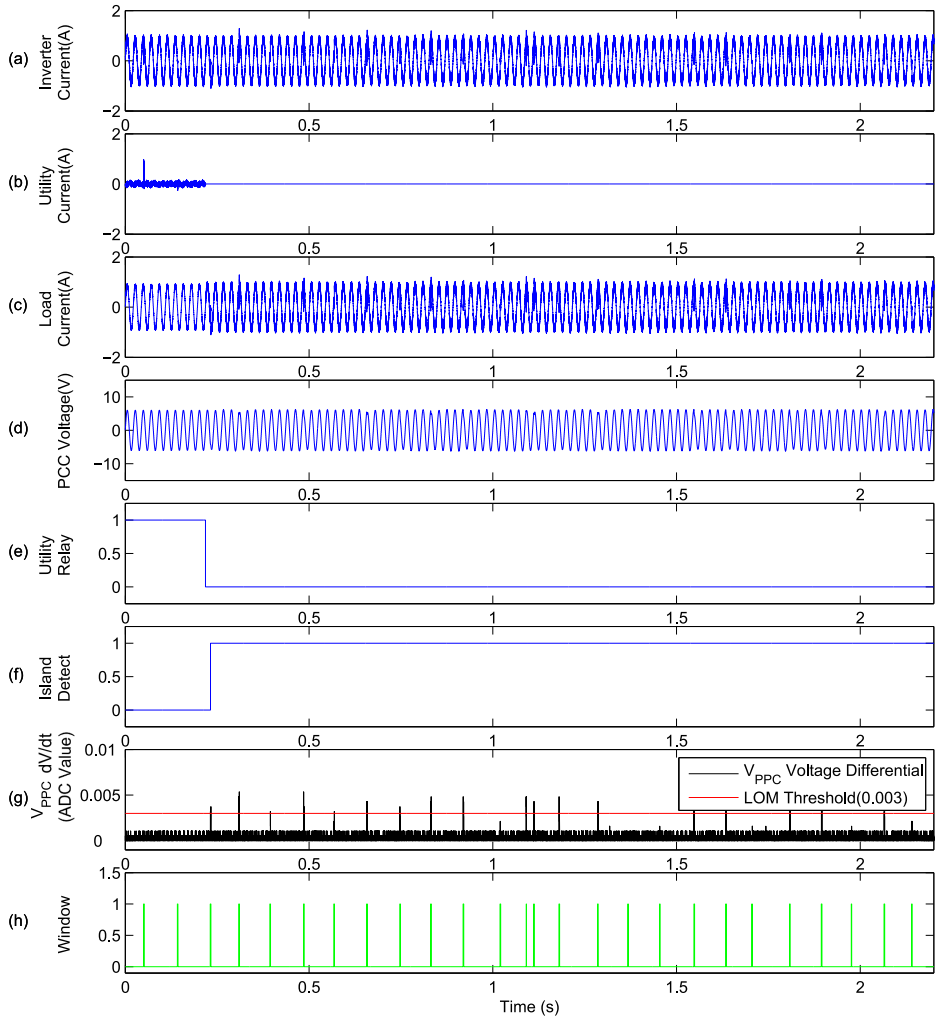

Figure 4.36: Zero current pulse simulation waveforms during a LOM event occurring at balanced power operation

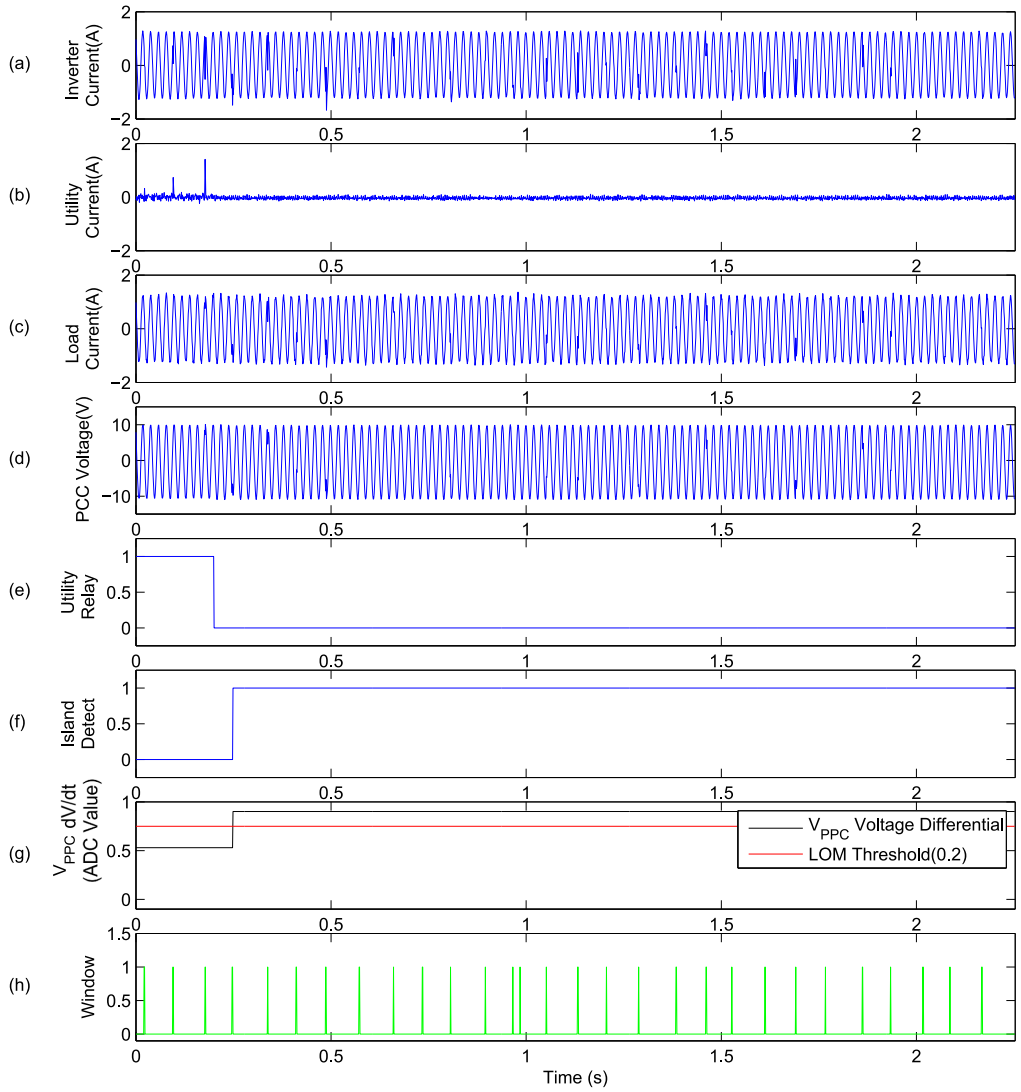

Figure 4.37: Zero current pulse experimental waveforms during a LOM event occurring at balanced power operation

4.2.4.2 Detection Delay Time

The zero current pulse LOM detection technique was tested across a range of operating conditions (±10% in both real and reactive power mismatch). The resultant simulation detection delay times are shown in Figure 4.38 and the resultant experimental detection delay times are shown in Figure 4.39. Whilst the detection delay times are the largest out of the active techniques, this is due to certain decisions made during development, mainly the decision to only activate the zero current pulse sequence in one out of every four fundamental waveforms. The detection delay times show an acceptable level of consistency across the different operating

conditions, with the simulation results generally shorter.

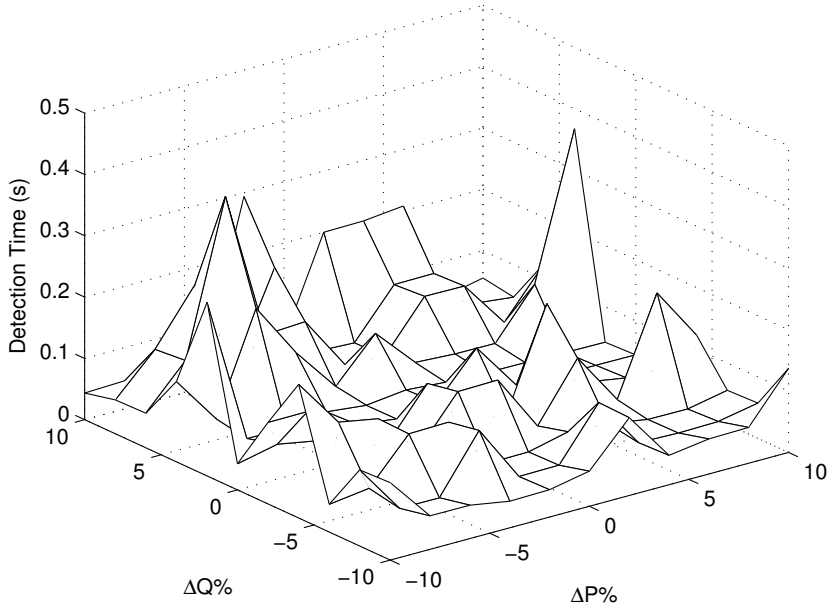

Figure 4.38: Zero current pulse simulation detection delay graph

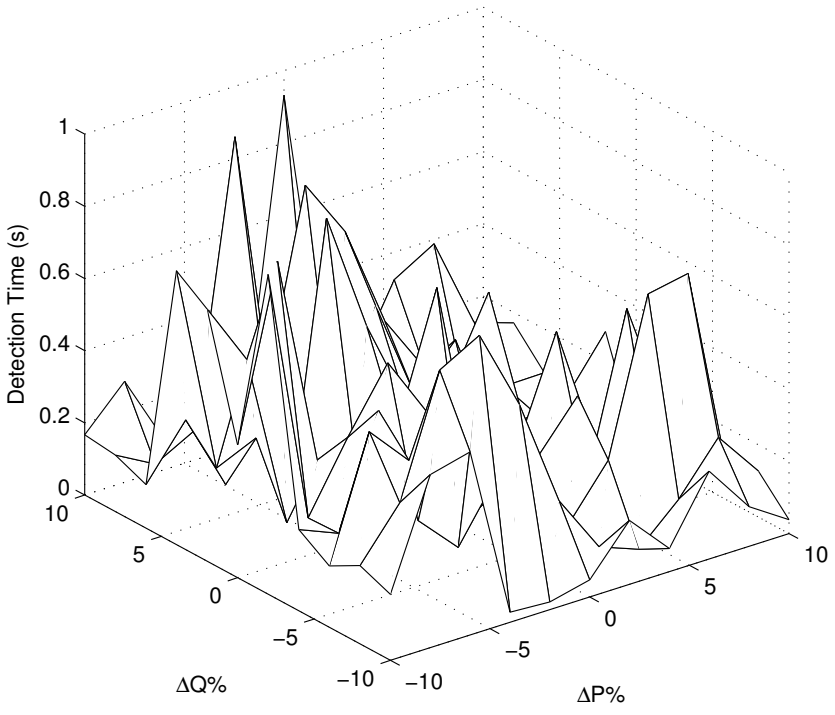

Figure 4.39: Zero current pulse experimental detection delay graph. Error analysis in Section 5.6.4

4.2.5 Active Techniques Discussion

The four active techniques presented in this section exhibit common features normally associated with active LOM detection techniques:

- *Zero NDZ* - All the implemented techniques detect LOM events when the power system is operating across the entire range of power mismatch conditions, including the balanced power condition.
- *Threshold trade off* - During development the thresholds that dictate the acceptable grid connected range for the calculated parameters can be set at any level. A fundamental compromise occurs between the detection delay time, the size of the disturbance introduced and the probability of a false LOM indication signal being caused by grid signal fluctuations.

The active power shift LOM detection technique results in relatively fast detection delay times. The detection delay times experienced in the presented system are relatively fast and consistent. However, the detection delay times are largely dependant on the size and frequency of the active power shift. An extra factor to take into account is that with a larger active power shift, the available generator power will not be fully utilised. In the developed system, the active shift size is 80%, with a duty ratio of 50%, giving an overall power utilisation of 90%. The under/over voltage amplitude and frequency routine that is incorporated within this technique remains constant with Section 4.1.1. However, another trade off exists here when setting the thresholds, between the chance of a non detect and the likelihood of a false trip.

The reactive power shift LOM detection technique exhibits relatively fast detection delay times, however, as with the active power shift routine, the detection delay times experienced are largely dependant on the size and frequency of the reactive power shift. The system presented was developed with an 80% reactive power shift and a duty ratio of 50%. This resulted in the system having very similar detection delay times as the active power shift routine. This technique may have limited real world application as many utilities have standards relating to the levels of reactive power that can be injected into the grid, with the majority of utilities generally preferring power generation to occur with a unity power factor.

The second harmonic injection LOM detection technique proved to have the shortest detection delay times when compared to the other three active LOM detection techniques that have been tested. There is a compromise when developing this system, with the amplitude of the injected signal and the detection delay time being the two competing factors. The injected signal level of 2% of the fundamental works in this

case. However, when implemented on power networks with differing levels of second harmonic background noise, erroneous LOM signals could become an issue. Another issue that could become meaningful if this system became common, is the multiple inverter case, where two inverters connected to the same local power network, both including the 100 Hz signal within their power output, could interfere with each other.

The zero current pulse demonstrated the longest detection delay times. However, if the zero current pulse frequency was increased, the detection delay times could be substantially reduced. Again a compromise exists between the frequency and severity of the introduced disturbance and the detection delay time. A negative associated with the zero current pulse technique is the high frequency current changes which are regularly injected into the utility. Another issue regarding this technique is the voltage changes that occur between the LOM event and the LOM detection, there is a possibility these voltage changes could damage or disrupt sensitive equipment.

4.3 24 Hour Test

All the systems presented in this chapter were subjected to a prolonged operation test which involved leaving the laboratory set-up running at the balanced power condition for a 24 hour period. Each LOM detection routine was implemented and subjected to the prolonged operation test to discover if any false trip signals were produced. A simple counter was included within the program code that counted the number of LOM signals produced by each routine individually.

All five presented LOM detection techniques resulted in zero false detect signals for the entire 24 hour operation test. This confirmed that the development of the LOM detection methods, and the threshold values chosen, produced viable real world solutions. Further work would be necessary to confirm that the developed systems remain robust and fault free when installed at different locations with different power network characteristics, however, the results obtained are suitable for the comparative needs required by this project.

Chapter 5

Proposed Loss of Mains Detection Technique

During the development and evaluation of previously reported LOM detection methods it became apparent that none of the tested methods could be considered as an ideal solution. Whilst there will always be a competing factors involved in the development of a new LOM detection method, it is believed that the proposed technique can be considered an attractive solution.

This chapter first provides an overview of how the proposed LOM detection technique operates and the principle factors that are exploited. Further detail is then given which explains how the proposed LOM detection technique has been implemented and discusses the reasons behind certain development decisions that were made. The system algorithm is included along with code timing diagrams to allow a full understanding of the procedures involved. Results are presented to allow the system to be compared to the LOM detection techniques presented in Chapter 4. The attractive features, along with possible drawbacks, of the proposed system are discussed allowing the possible merits to be fully considered.

5.1 Overview of Proposed Loss of Mains Detection Technique

The proposed loss of mains detection system is a hybrid method which involves a passive loss of mains flag and an active loss of mains check. The system has been designed to take advantage of the zero NDZ of an active method whilst only introducing a power output change when a passive method indicates to do so. The proposed method will be evaluated using three main criteria, the NDZ, the island detection delay and the proportion of time the active mode is engaged.

The passive routine that operates continuously is based on the principle that a network impedance change will occur during a LOM event. Using a Fast Fourier Transform, the passive routine produces the spectral data of the measured V_{PCC} signal. Spectral data analysis is used to determine parameters which can be used to monitor the amplitude and spread of the V_{PCC} frequency components. When a LOM event occurs, the spectral components detected in the V_{PCC} voltage will change because of two main factors:

- *Impedance change* - During a LOM event, the low impedance of the utility will no longer be connected to the local power network. This will alter the harmonic components in the measured V_{PCC} as high frequency components, such as the high frequency switching signal in the inverter output power, will no longer be filtered by the low impedance of the utility.
- *Altered harmonic sources* - After a LOM event, the connected power network will consist of a completely different variety of loads and generators. This change in connected devices increases the probability of a change in the V_{PCC} spectral data.

The passive routine is used to indicate situations when a change has occurred in the spectral data, which could have been caused by a LOM event. The passive routine activates an active LOM check routine. The active LOM check routine that is included in this solution is the same as the active power shift technique detailed in Section 4.2.1. During the active power shift LOM check, if a LOM event has been ruled out, an extra routine is used to reconfigure the passive monitoring routine. This allows the proposed technique to adapt to network changes without producing erroneous LOM indications.

5.2 Passive Monitoring Routine

The passive monitoring routine that has been implemented exploits the low impedance of the utility connection acting as a low pass filter. When a LOM event occurs, the impedance rises sharply, causing the high frequency components in the measured V_{PCC} to change. A 256 point FFT is used to produce the frequency spectrum for V_{PCC}. The FFT is a computationally efficient way to complete the DFT, Digital Fourier Transform, defined by Equation 5.1:

$$X_k = \sum_{n=0}^{N-1} x_n e^{i2\pi k \frac{n}{N}} \qquad k = 0, ..., N-1 \tag{5.1}$$

where X_k is the harmonic information for a specific frequency, k is the frequency bin number, x_n is the sampled data value and N is the length of the transform ($N = 256$ in this routine) [97].

The spectral data produced by the FFT routine is an array of complex values relating to the magnitude and phase of each harmonic detected in the measured data. The magnitude is calculated to give an array of data, with each value in that array representing the magnitude of a specific frequency component that is apparent in the measured V_{PCC} waveform.

The FFT routine is synchronised with the PLL phase output to allow each FFT routine to operate using the same parts of the measured V_{PCC} waveform. The FFT is completed every other fundamental waveform, meaning the spectral data is updated every 0.04 seconds.

By sampling V_{PCC} at 30 kHz it is ensured that the effect of the 10 kHz switching component in the inverter output current is included within the usable frequency spectrum, 0-15 kHz, according to Nyquist-Shannon sampling theorem, stated in Equation 5.2:

$$f_s \geqslant 2f_{max} \tag{5.2}$$

where f_s is the sampling frequency and f_{max} is the maximum valid frequency component to be sampled [98].

The mean harmonic magnitude is calculated each time the FFT routine updates the spectral data. The lower frequency spectral values are not included in the mean summation as they are several orders of magnitude larger than the high frequency components and thus, would dominate the mean calculation. This allows the switching component and all other high frequency harmonics to be constantly monitored, with the idea that the mean harmonic amplitude should rise due to the impedance increase that occurs during a LOM event. Specifically, the frequency range included in the mean summation process is 352 Hz to 15 kHz.

Another factor taken into consideration is the standard deviation of the harmonic magnitudes, over the same frequency range of 352 Hz to 15 kHz. During islanded operation there is less spread of the frequency components. Instead, there are spectrum nulls and peaks. This is due to a restricted amount of frequency sources connected to the local power network and the relatively large peak caused by the switching frequency. These nulls and peaks indicate that the standard deviation of the harmonic magnitudes rises after a LOM event.

For each FFT that is executed, a mean and standard deviation pair is produced. Both these factors are expected to rise when a LOM event occurs. To demonstrate

this difference, an experimental procedure was undertaken in which the system was allowed to operate in grid connected mode and then in islanded mode. The mean and standard deviation pairs calculated throughout this test were recorded. Figure 5.1 shows the experimental data obtained when running the system for 80 FFT cycles whilst grid connected at balanced power and a subsequent 80 FFT cycles whilst islanded. A clear separation between the grid connected and islanded mean and standard deviation pairs is apparent.

The passive monitoring algorithm has a threshold boundary which encloses the grid connected pairs. An example threshold boundary can be seen in Figure 5.1. If a pair is calculated outside of the thresholds the passive scheme initiates an active LOM check algorithm. The threshold boundary values are initialised to zero, meaning that when the system starts up the first mean and standard deviation pair will cause the system to activate the active LOM check routine. If the active check routine confirms that the utility connection is in fact present the threshold values are updated. This method of threshold determination was chosen to allow the system to self tune,

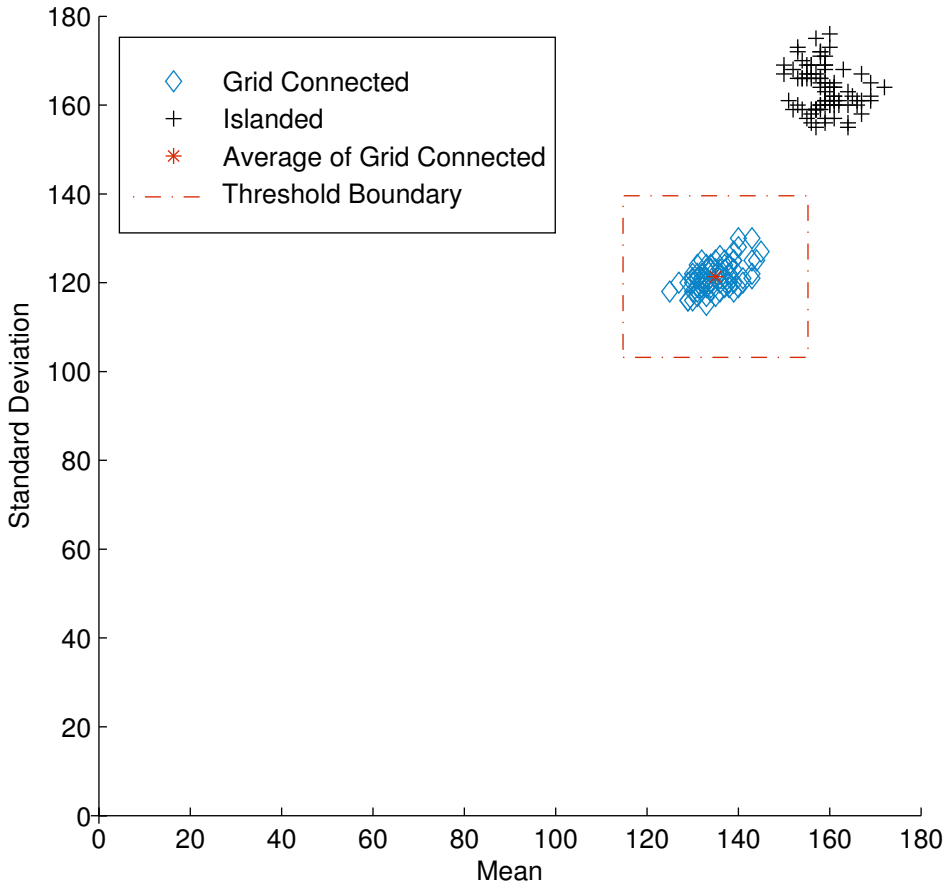

Figure 5.1: 80 example mean and standard deviation pairs for grid connected and islanded operation during balanced load condition

resulting in a routine that can be connected to any power network with no previous knowledge or training regarding the expected utility voltage signal.

The active LOM check routine calculates the new threshold boundary based on the five most recent calculated mean and standard deviation pairs. The boundary is calculated at ±15% the average value for the grid connected pairs.

5.3 Active LOM Check

As the passive monitoring sequence is based on frequency spectrum analysis, the active LOM check implemented has no dependency on any kind of measured frequency component, reducing the likelihood of a false detect signal when connected to a noisy grid.

The active method that has been included is a periodic active power shift procedure, detailed in Section 4.2.1. In this scheme the controller periodically alters the amplitude of the inverter output current. When the constant grid voltage is not connected to the point of common coupling, the periodic change in inverter output current alters the value of V_{PCC}.

The active power shift procedure is used in conjunction with an under/over voltage amplitude and frequency routine, detailed in Section 4.1.1. The fluctuations in the measured V_{PCC} voltage, caused by the active power shift procedure, result in the under/over voltage amplitude and frequency routine detecting the LOM event. The under/over voltage amplitude and frequency routine operates constantly, not only when the active LOM check routine is enabled. The thresholds for the under-/over voltage amplitude are set at ±10% of the average RMS, and ±1 Hz for the under/over frequency.

The active power shift procedure has a duty ratio of 50%, this means that the inverter output power is altered for every other fundamental waveform. The unaltered period of inverter output power is used to continue producing FFT data and mean and standard deviation pairs. When the LOM check routine ends, if the system has been proven to be grid connected, the averages of the recent mean and standard deviation pairs is calculated. The threshold boundaries used in the passive monitoring sequence are then redefined at 15% above and below the grid connected averages. This allows the system to adapt to network changes by reconfiguring the spectral amplitude and spread that defines grid connected operation.

5.4 Timing and Threshold Calculation

The proposed system is synchronised with the internal PLL, ensuring that the same section of the sampled V_{PCC} waveform is used for the FFT, this improves the consistency of the FFT output.

Figure 5.2 shows the sequence of completed processes in relation to the phase of the measured V_{PCC} signal. The diagram also shows the current fundamental, $I_{\text{fundamental}}$, which represents the current demand signal for balanced power operation and the current reference, I_{REF}, which is the actual current demand signal used to control the output power of the inverter.

The code can be seen to have two sectors, sector 1, and sector 2. The routine alternates between the two each time the V_{PCC} crosses zero, using the PLL phase reset command as the zero crossing point. There are four processes that are completed, using the sector to control the process order. The four processes shown in Figure 5.2 are:

- *Sample data* - The sample data process begins when the program enters sector 1 and has a duration of 0.0085 seconds which is the time take to fill the 256 point array when sampling at 30 kHz.
- *FFT* - As soon as the V_{PCC} data array is full, the FFT is activated which produces the frequency spectral data. The FFT completion time varies depending on the number of times it is interrupted by other program functions. Ample time is allocated for the completion of the FFT, with a check included to disregard any incomplete FFT spectral data. The length of the box in Figure 5.2 is indicative of the expected FFT duration.
- *Mean, μ, and standard deviation, σ, calculation* - The mean and standard deviation are calculated at the end of each sample sequence, before the old FFT data is overwritten by the FFT process. The new mean and standard deviation pair are compared with the threshold boundary to determine if the active LOM check routine should be enabled.
- *Under/over voltage amplitude and frequency* - This passive LOM detection technique operates constantly during the proposed LOM detection method.

If the passive routine enables the active LOM check procedure, the program switches to a sequence which involves more processes. Figure 5.3 shows the sequence of completed processes in relation to the phase of the measured V_{PCC} signal during an active LOM check sequence. The effect that the active power shift procedure has on the current reference signal, I_{REF}, is shown in Figure 5.3. The 20% reduction of

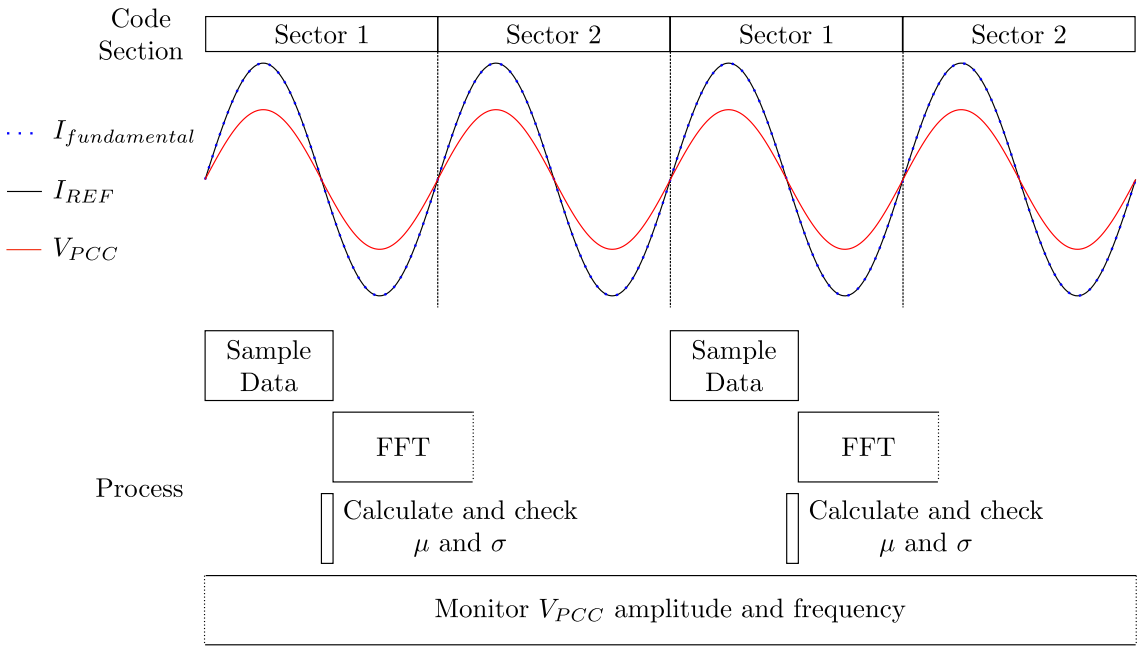

Figure 5.2: Timing diagram of processes during normal operation

the current reference signal can be seen during the active shift process. This change in output power is included to ensure fluctuations in the V_{PCC} voltage will occur if the utility connection has been lost, causing the under/over voltage amplitude and frequency routine to indicate the LOM event.

The system runs the active power shift routine for 10 fundamental periods (0.2 seconds). As the active LOM check only changes the amplitude of the output current every other fundamental period, it is still possible to complete the FFT for V_{PCC} data sampled during full inverter output power. During the LOM check routine the calculated mean and standard deviation pairs are stored in memory. This results in the calculation of five mean and standard deviation pairs during the LOM check procedure. The five sets of mean and standard deviation pairs are summed, an average for each variable is calculated, and then the new maximum and minimum thresholds are set at 15% either side of the averages.

The structured programming code automatically switches between the code sections shown in Figure 5.2 and Figure 5.3.

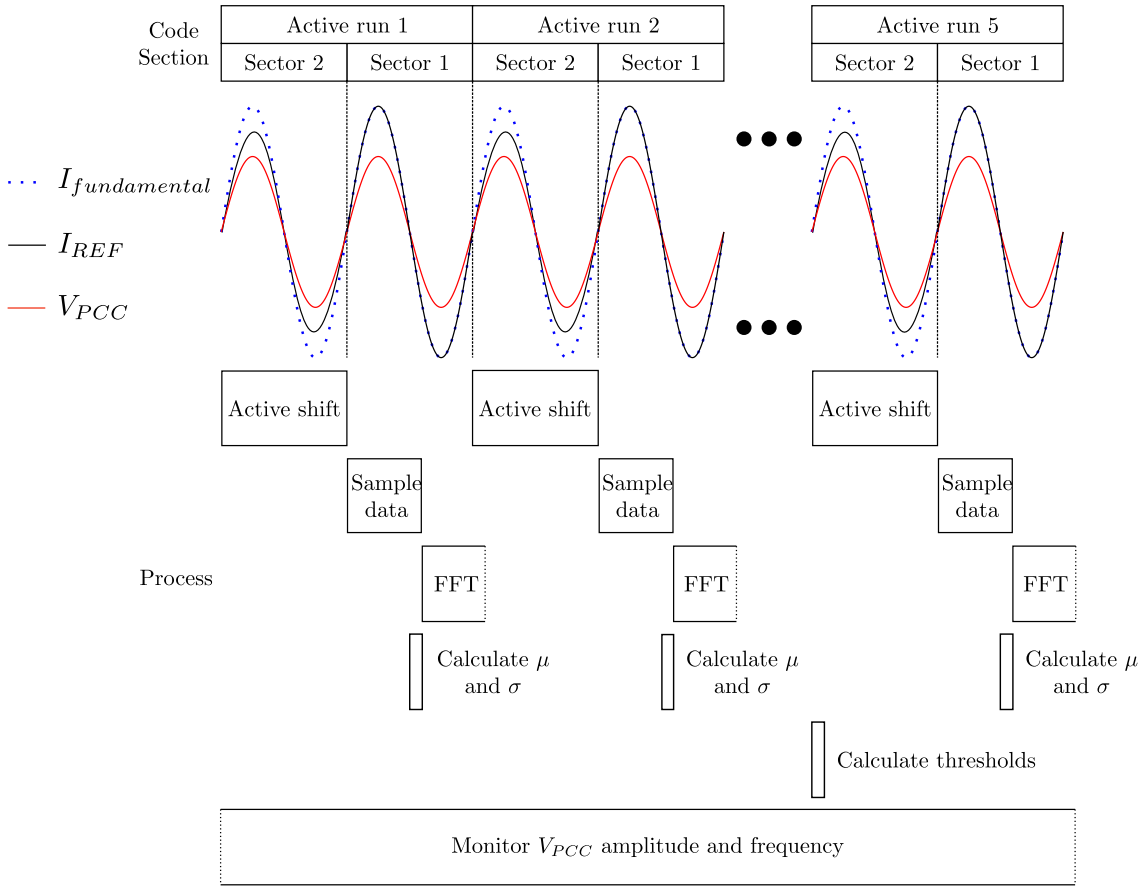

Figure 5.3: Timing diagram of processes during threshold recalculation and active shift

5.5 System Algorithm

The main program algorithm is shown in Figure 5.4 and the program code is given in Appendix A. The important details involved in the main program operation are:

- *Start point* - The system start point is visited many times during normal operation, meaning no initialisation or special start-up code is needed.
- *LOM indication* - A LOM event is only ever indicated by the under/over voltage amplitude and frequency routine. Whilst the calculation of these parameters is not shown in this diagram, the calculation is completed once every fundamental period.
- *2 sectors* - Each time the PLL phase is reset, the program switches code sectors. This means the system loops around the code for each sector in alternative fundamental periods.
- *Sector 1* - This sector completes three main processes:
  - Samples V_{PCC} and stores in an input array.

  - Waits for the V_{PCC} input array to be full, then actives the FFT routine, which operates in a different section of code. Once the FFT is activated it continues to operate until it has finished, unaffected by any sector change.
  - A mean and standard deviation pair is calculated once the V_{PCC} input array is full, a subsaquent check is completed against the relevant thresholds to determine if the the active LOM check routine should be enabled.

  The operation of this sector remains unchanged when the active LOM check routine is enabled. The active LOM check routine cannot be disabled in this sector.

- *Sector 2* - If the active LOM check is not enabled, only the background FFT routine operates during this sector. If the LOM check is enabled, the following operations are completed:

  - The active power shift is applied to the current reference by reducing the current demand by 20%.
  - The mean and standard deviation variables are stored until 5 iterations of sector 2 when the LOM check routine will have been completed.
  - Once five mean and standard deviation paris have been recorded they are used to determine the new passive thresholds, and the active LOM check is disabled meaning the system returns to passive operation with updated thresholds.

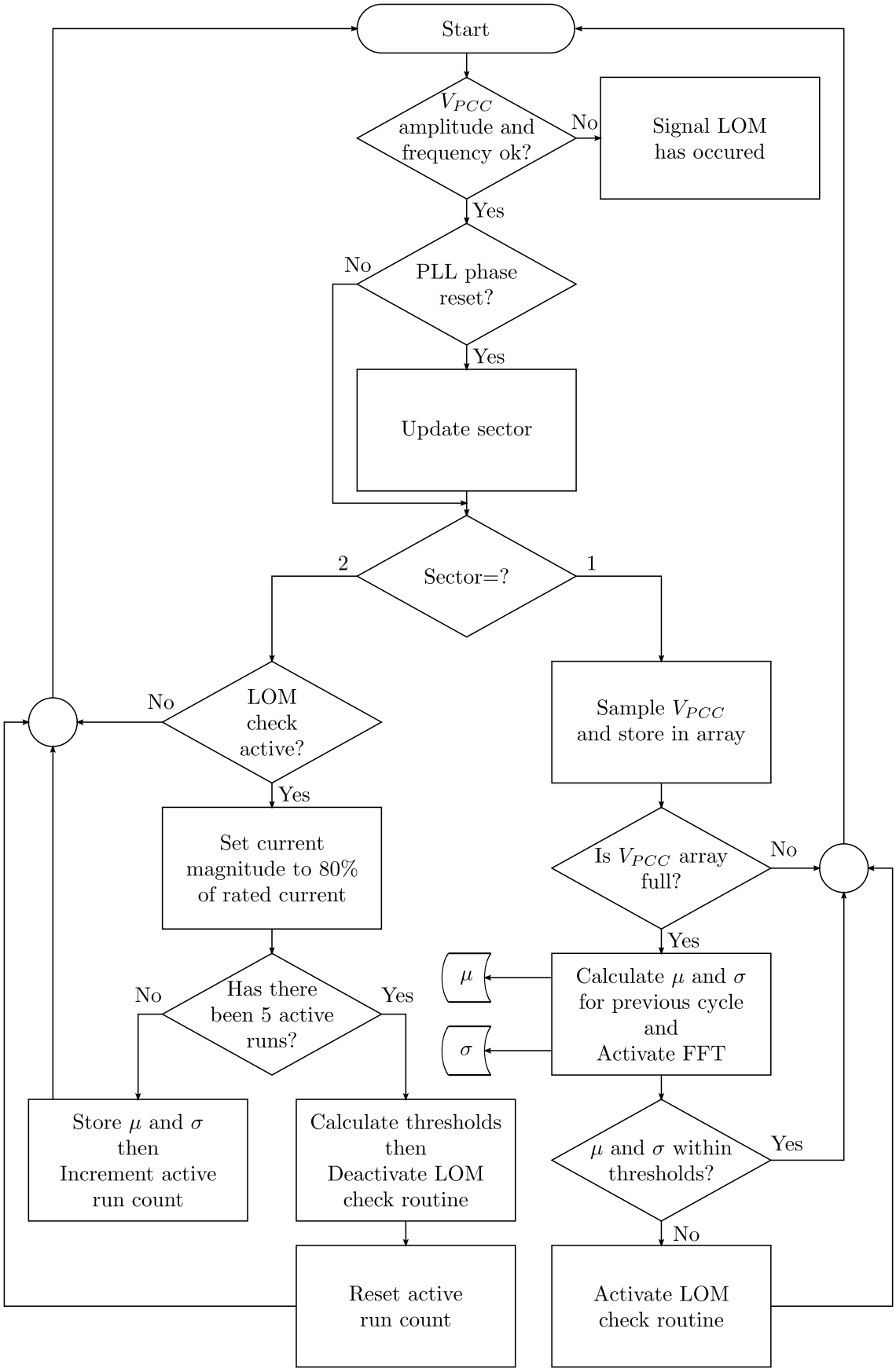

Figure 5.4: Program algorithm for the proposed LOM detection method

5.6 Experimental Results

5.6.1 Results At Balanced Power Operation

The initial testing of the proposed LOM detection technique was completed at balanced power to verify that a LOM event can be detected even when the system is operating at the most challenging operational point. The waveforms presented in Figure 5.5 show how the system parameters and calculated variables react to the LOM test. The short LOM test is 0.6 seconds in duration with the utility disconnection occurring 0.3 seconds into the routine. The short test is used so that the system parameters can be sampled at a high data rate, allowing more detailed presentation.

Trace (b) shows the utility current, this is near zero before the LOM event occurs, indicating that the system is operating at balanced power. The inverter output current, trace (a), can be seen to be consistent before the LOM event occurs, meaning the LOM routine is in passive mode.

After the LOM event occurs, the calculated mean and standard deviation values exceed the threshold boundaries for the passive monitoring routine. The active LOM check routine is enabled on the first mean and standard deviation pair update calculated using sampled V_{PCC} data from after the LOM event. The delay between the LOM event occurring and the active LOM check enable is around 0.05 seconds in this case. This delay will experience some variance, depending on which part of the routine is being completed when the LOM event occurs.

When the active LOM check routine is enabled it begins to reduce the amplitude of the inverter current for alternate fundamental periods, this can be seen in trace (a). As the the utility is not connected to compensate for these short periods of local power mismatch, the load current, trace (c), and V_{PCC} voltage, trace (d), fluctuate in amplitude. The fluctuation of V_{PCC} cause the calculated RMS, trace (e), to exceed the LOM thresholds set in the under/over voltage amplitude and frequency routine. The under/over voltage amplitude and frequency routine indicates the LOM event at 0.39 seconds, giving a detection delay in this case of 0.09 seconds.

In this test, when the LOM event is indicated, the system continues to output power. This would not happen in any real world application. The control structure is allowed to continue power output to demonstrate how the active LOM check routine only operates for 10 fundamental periods. This is most apparent on trace (e), the calculated RMS value for V_{PCC}, can be seen to alternate between the rated voltage and a reduced level five times before remaining at rated voltage. The duration of the active LOM check can also be seen in trace (a), trace (c) and trace (d), with five alternate period dips in amplitude clearly visible, before three consistent amplitude periods that indicate the active power shift is no longer enabled. When the active

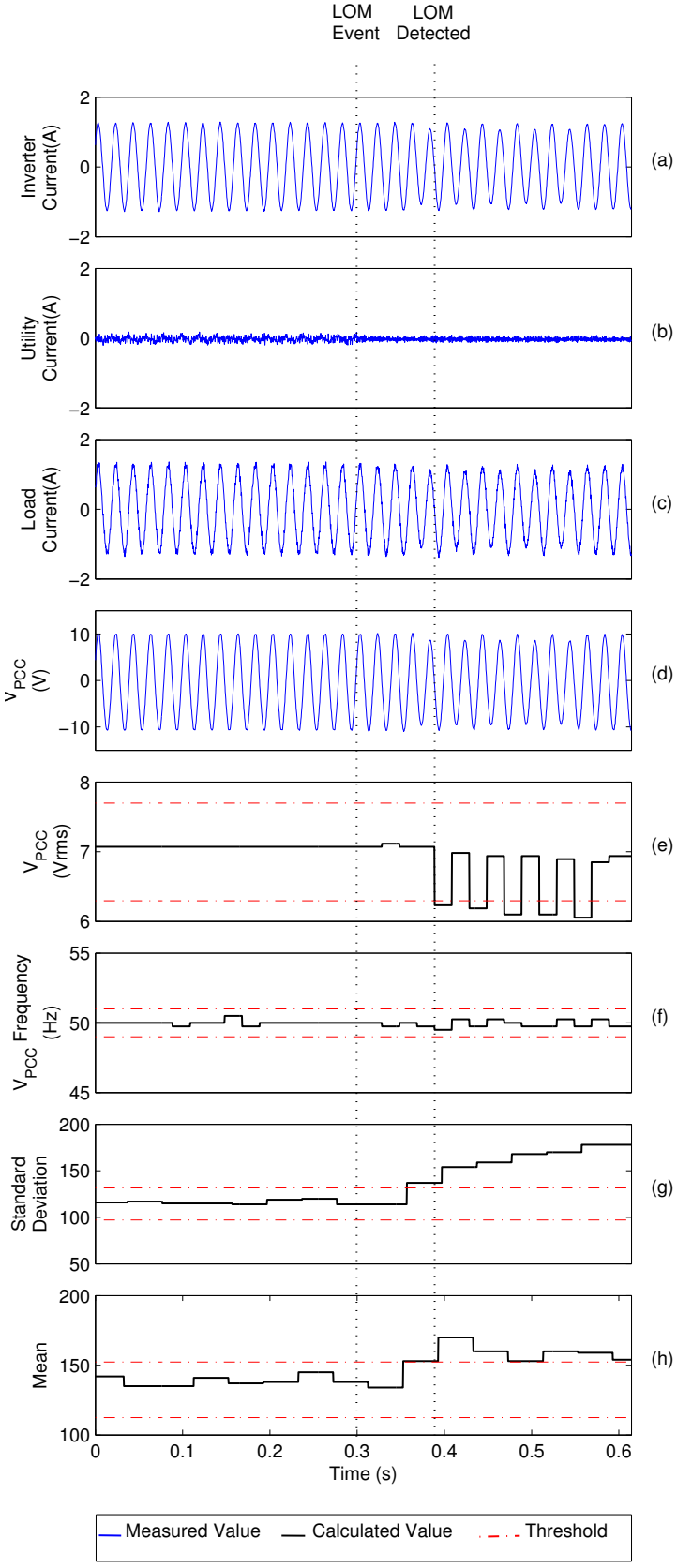

Figure 5.5: Balanced power operational waveforms for proposed technique

LOM check is disabled, new thresholds would be normally calculated for the mean and standard deviation, this is not included in this test as the system is known to be islanded.

This test indicates that the proposed LOM detection technique can detect a LOM event when the system is operating at the challenging balanced power condition. This is a strong indicator that the system will have a zero NDZ, however, further testing must be completed across a range of power mismatch conditions to verify that the proposed system can detect a LOM event independent of the network status.

5.6.2 Detection Delay Time

The proposed LOM detection technique was tested across a range of operating conditions (±30% in both real and reactive power mismatch). The resultant detection delay times are shown in Figure 5.6.

Figure 5.6 confirms that the proposed LOM detection technique has a zero NDZ, proving that the proposed system is robust enough to detect LOM events across all power mismatch levels.

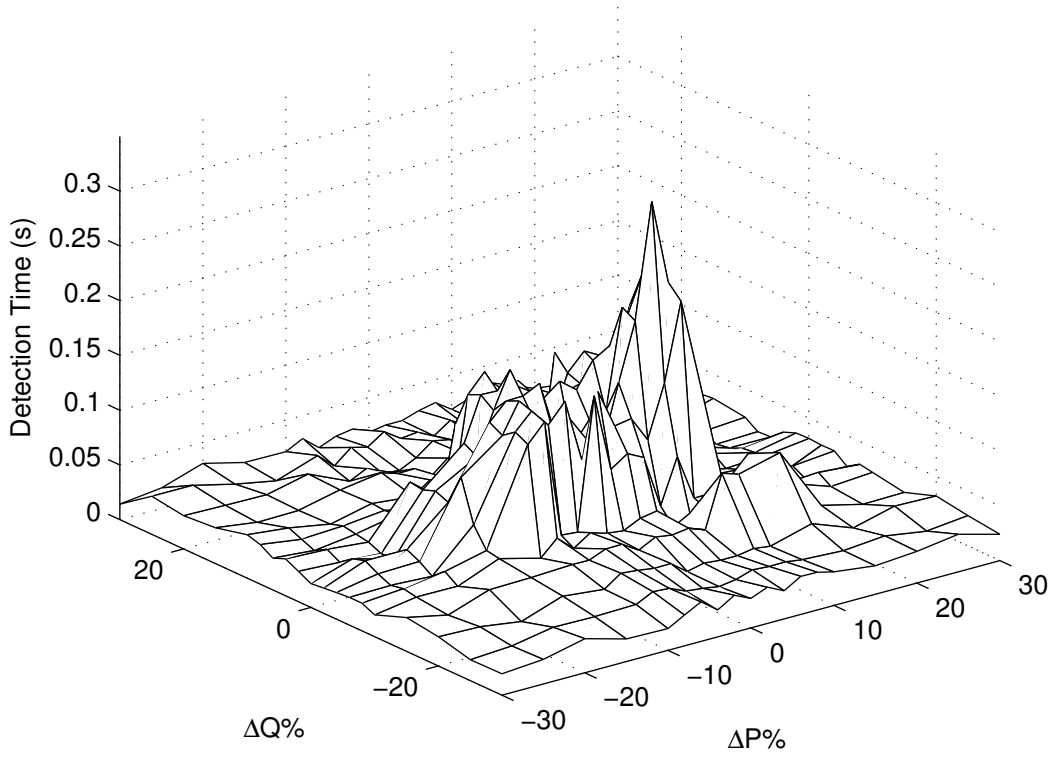

Figure 5.6: Detection delay times for proposed LOM detection routine

The graph shows that the proposed LOM detection technique experiences much larger detection delay times when the system is operating at, or near, the balanced power condition. The detection delay time test was completed for the extended range of operating conditions so that this feature could be presented. The reason the proposed detection technique has a smaller detection delay time for the larger power mismatch conditions is because of the continuous operation of the under/over voltage amplitude and frequency routine. As a substantial power mismatch will cause the measured V_{PCC} voltage to fluctuate beyond the acceptable grid connected range, the system can indicate the LOM event before entering the active LOM check routine. This means the active LOM check routine is only needed when the system is operating close to, or at, the balanced power condition. In other words, the active LOM check routine is only needed when operating within the NDZ of the under/over voltage amplitude and frequency routine.

5.6.3 24 Hour Test

The proposed LOM detection system was tested for a continuous period of 24 hours during balanced load operation. During this long test, zero false detect signals occurred, this is due to the constant grid voltage ensuring V_{PCC} remains within the LOM thresholds.

A concern when implementing a hybrid technique is the amount of time the system will spend operating the active LOM check routine. The only issue associated with the proposed technique is power utilisation, that is, when the active LOM check is enabled, the power output of the inverter is purposely reduced. The active LOM check routine reduces the current output to 80% for a total of 0.1 seconds each time it is enabled. A counter variable was including for the 24 hour test to record how many times the system enabled the LOM check routine. During the 24 hour test, the active routine was initiated 98 times, meaning the output power was reduced to 80% for 9.8 seconds in total. This reduces the overall test period power utilisation to 99.998%.

5.6.4 Proposed Technique Discussion

The proposed LOM detection technique has been proven to successfully detect LOM events across the entire range of power mismatch levels, shown in Section 5.6.2. This means the proposed technique outperforms the purely passive techniques presented in Section 4.1.

As the proposed LOM detection method has a zero NDZ, it is more appropriate to evaluate performance by comparing it to the tested active techniques, presented in

LOM Detection Technique	False Trips	Detection Delay Time (s)		
		Average	Standard Deviation	Maximum
2^{nd} Harmonic Injection	0	0.042	0.018	0.099
Active Power Shift	0	0.062	0.088	0.885
Reactive Power Shift	0	0.065	0.073	0.727
Zero Current Pulse	0	0.27	0.24	0.93
Proposed Technique	0	0.1	0.06	0.3

Table 5.1: Detection delay times for tested techniques

Section 4.2. The main factor that can be used for comparison is the detection delay time. Table 5.1 contains the key information gathered about the detection delay time for the active LOM techniques presented in Section 4.2, along with the same information about the proposed LOM detection technique for comparison. This data was produced using the detection delay times gathered whilst testing the techniques across the range of power mismatch levels of ±10% in both real and reactive power. The extended results for the proposed technique, presented in Section 5.6.2, are not included so as to maintain consistency for each technique. The inclusion of the extended power mismatch region would result in the average detection delay time for the proposed method being substantially reduced.

A graphical representation of the data in Table 5.1 is shown in Figure 5.7. Because

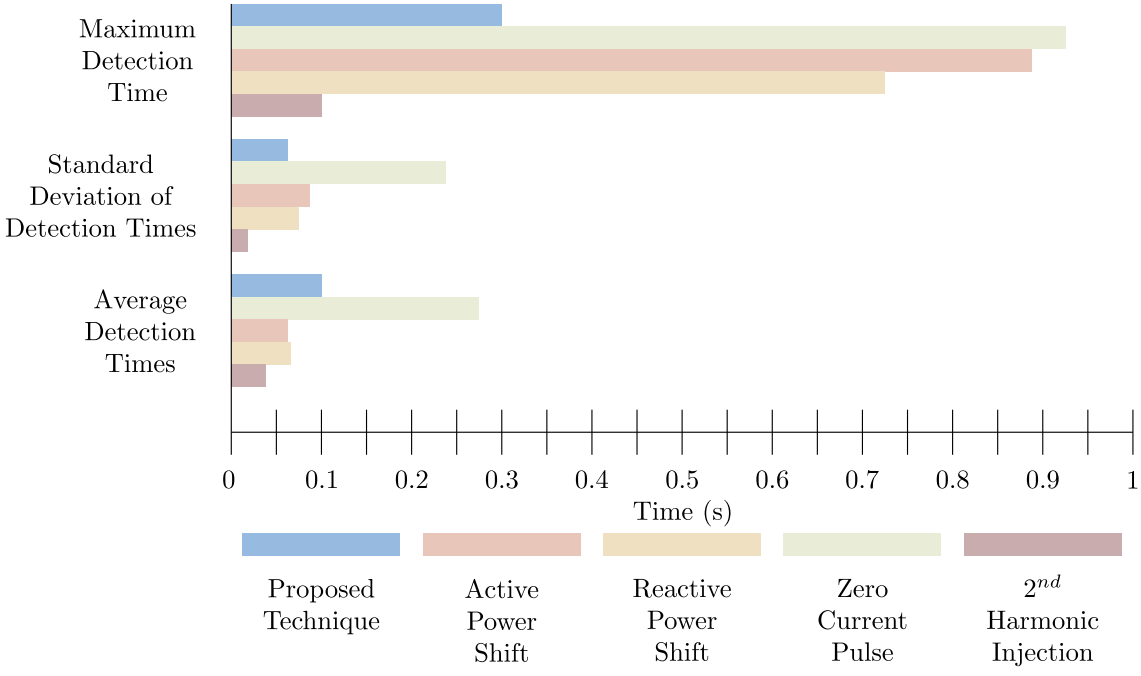

Figure 5.7: Graph showing detection delay times for tested techniques

of the sequential nature of hybrid LOM detection techniques, it is expected that they exhibit large detection delay times. Figure 5.7 clearly shows that the average detection delay time for the proposed technique is comparable to the average detection delay times for the tested purely active techniques. The standard deviation is included to show the range of detection delay times that can be expected for each LOM detection technique, the results show that the proposed method exhibits a fairly consistent LOM detection delay time. The maximum detection delay for the proposed technique is considerably lower than the majority of the tested active techniques, with only the 2^{nd} harmonic injection technique producing better results but of course the 2^{nd} harmonic injection technique introduces the issues discussed in Section 4.2.3.

Overall the detection delay times experience by the proposed LOM detection technique are comparable with the other, solely active, techniques that have been tested. All the systems developed detect LOM events well within the 2 second limit set by IEEE connection standards [69].

During the 24 hour test, presented in Section 5.6.3, the number of times that the system enabled the LOM check routine when the utility was still connected was recorded. This test was completed to understand the effect that the proposed technique has on power utilisation, as more time spent with the LOM check routine enabled would results in a lower power utilisation. The test period power utilisation was stated to be 99.998%, which relates to an acceptable reduction of 0.002% caused by the proposed technique. However, it is worth noting that this value is based on a power system with a constant balanced load. Changes in the devices connected to the local power network will have an impact on the harmonic content of the voltage, meaning the LOM check routine will be activated more often. The reduction in power utilisation caused by the proposed technique is expected to be larger in a real world scenario. Further work, including field trials, would need to be carried out to accurately quantify the reduction in power utilisation caused by the proposed technique.

Chapter 6

500 W Laboratory Test Bench

This chapter describes the development and construction of a 500 W laboratory test bench. It was decided that a laboratory test bench with a power rating similar to a typical DG unit installation should be constructed to allow the results obtained using the scaled power laboratory test bench to be fully validated. The power level of 500 W was chosen to mimic a PV installation with two standard domestic scale PV panels. The test bench is introduced and the individual hardware components are specified.

The 500 W laboratory test bench operation is presented to demonstrate how a power island can form during a forced LOM event.

The proposed technique is tested using the 500 W laboratory test bench and results are presented to show how the system operates at a power level more in line with an actual DG unit installation.

6.1 500 W System Layout

The 500 W laboratory test bench has the same system layout as the scaled power laboratory test bench, the main difference being the inclusion of a autotransformer as the grid connection device. This autotransformer allows the grid voltage to be stepped down to allow the inverter to operate at any voltage between 0 and 240 V RMS. The local operational voltage is set to 170 V RMS for the results presented in this chapter. This voltage was chosen as it allowed the use of available and fully tested hardware. The power inverter used is an IGBT based H-bridge inverter instead of the MOSFET based inverter that is used in the scaled power laboratory test bench. The circuit layout for the 500 W laboratory test bench is shown in Figure 6.1. The main hardware modules that differ from the scaled power laboratory test bench are explained in more detail in Section 6.2.

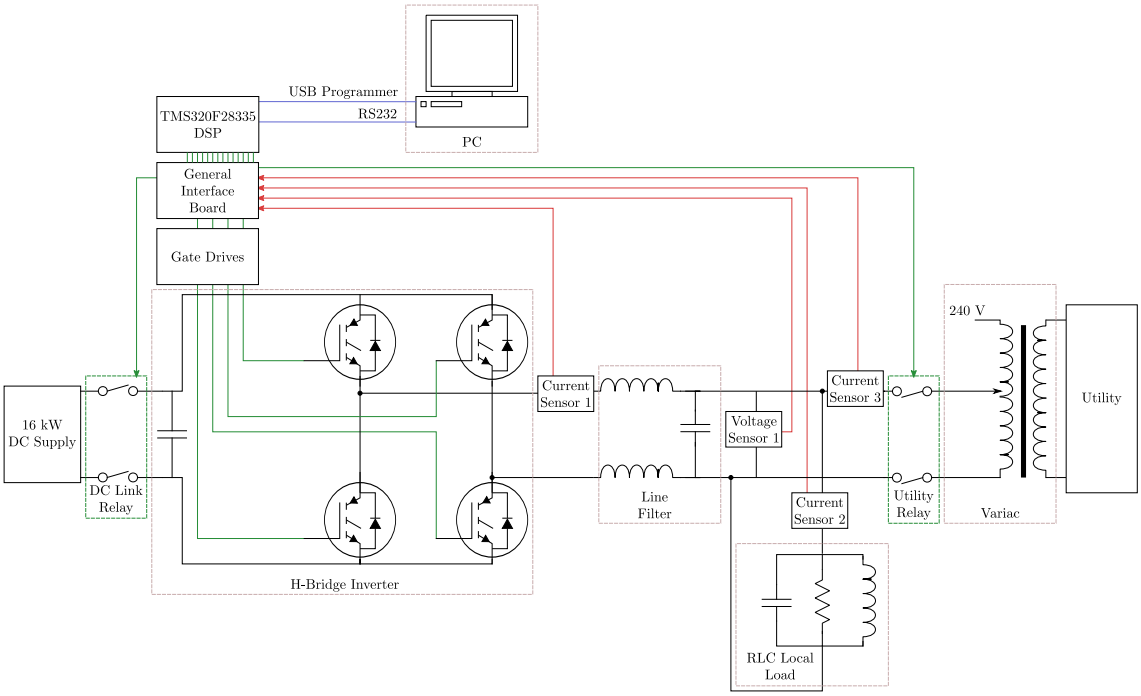

Figure 6.1: 500 W laboratory test bench

6.2 Hardware

Figure 6.2 shows the constructed 500 W laboratory test bench. The design of the high power test bench was similar to the process involved with the scaled power test bench. However, due to the larger operational voltages and currents, additional concerns and allowances were taken into account:

- *Isolation* - It was imperative that isolation boxes were included to restrict the access to any circuitry carrying high voltages. All equipment was earthed to ensure any fault did not result in a dangerous working environment.
- *Electromagnetic Interference (EMI)* - The voltage and current sensors were mounted in a metal isolation box to reduce any issues caused by the electromagnetic radiation produced by the switching IGBT's. Shielded cables were used to connect the general interface board to the gate drive circuitry.
- *General Safety* - The high voltages introduced the need for general safety requirements to be met, such as the installation of an emergency stop on the DC power supply, used to cease power output in the case of an accident.

The same DSP board and Labview control panel that are used in the scaled power laboratory test bench are used in the 500 W set-up. This allows for control code and testing procedures to remain consistent between the two testing platforms, meaning that the proposed LOM detection technique can be fairly evaluated.

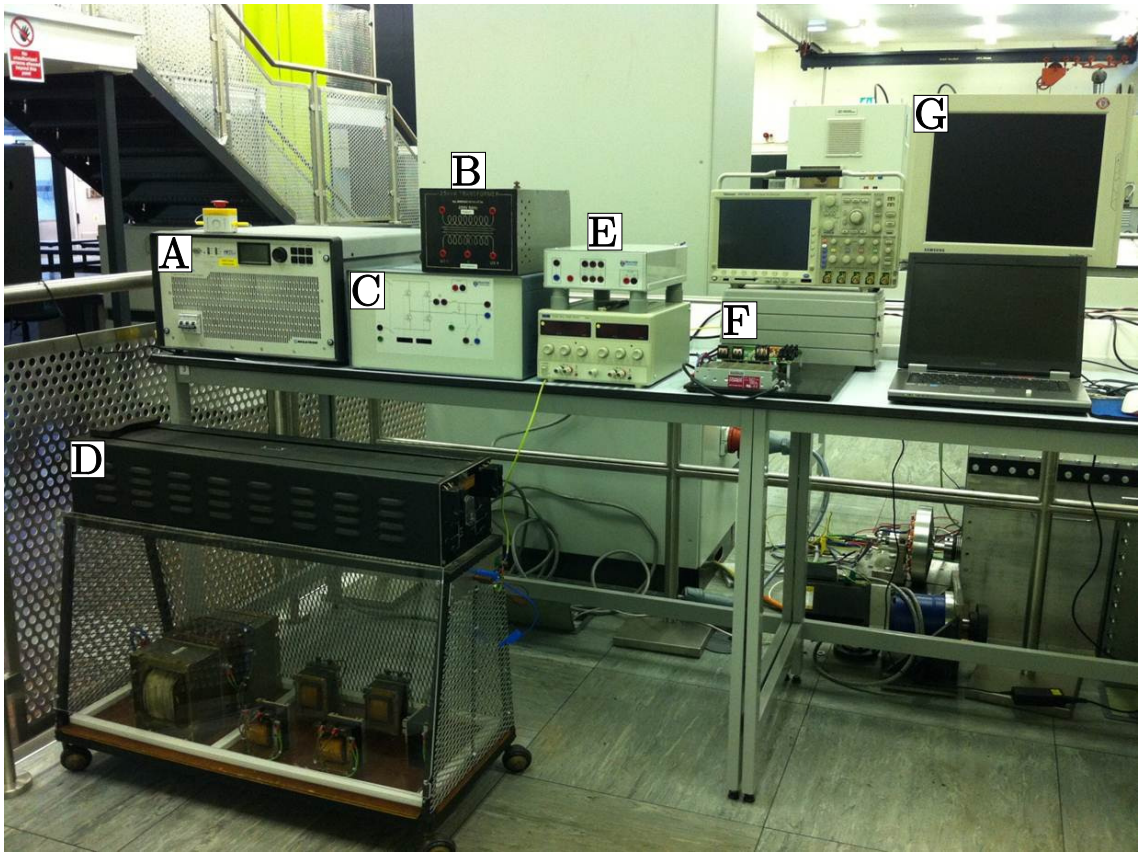

Figure 6.2: Photograph of the 500 W laboratory test bench. A, DC supply; B, autotransformer with grid connection; C, power inverter and line filter; D, 500 W RLC load; E, isolated sensor box; F, DSP and interface board; G, PC

6.2.1 Inverter Board

A four legged DC-AC inverter board was used as the grid connect power converter. Only two legs of the circuit are used in a single phase H-bridge topology. The inverter PCB is shown in Figure 6.3. The board is rated for any DC link voltage upto 500 V. The construction of the board allows the IGBT's to be directly mounted onto a large heat sink, this provides adequate passive cooling at the desired power levels.

6.2.2 General Purpose Power Interface Board

The general purpose power interface board is a standard project board designed at Newcastle University. The constructed PCB is shown in Figure 6.4. The board has been developed at the university to allow a multitude of motor drive and power converter research projects to be completed using the same hardware. The intention of the general power interface board is to provide many of the common functionalities required in power electronics projects. It provides an interface between the attached

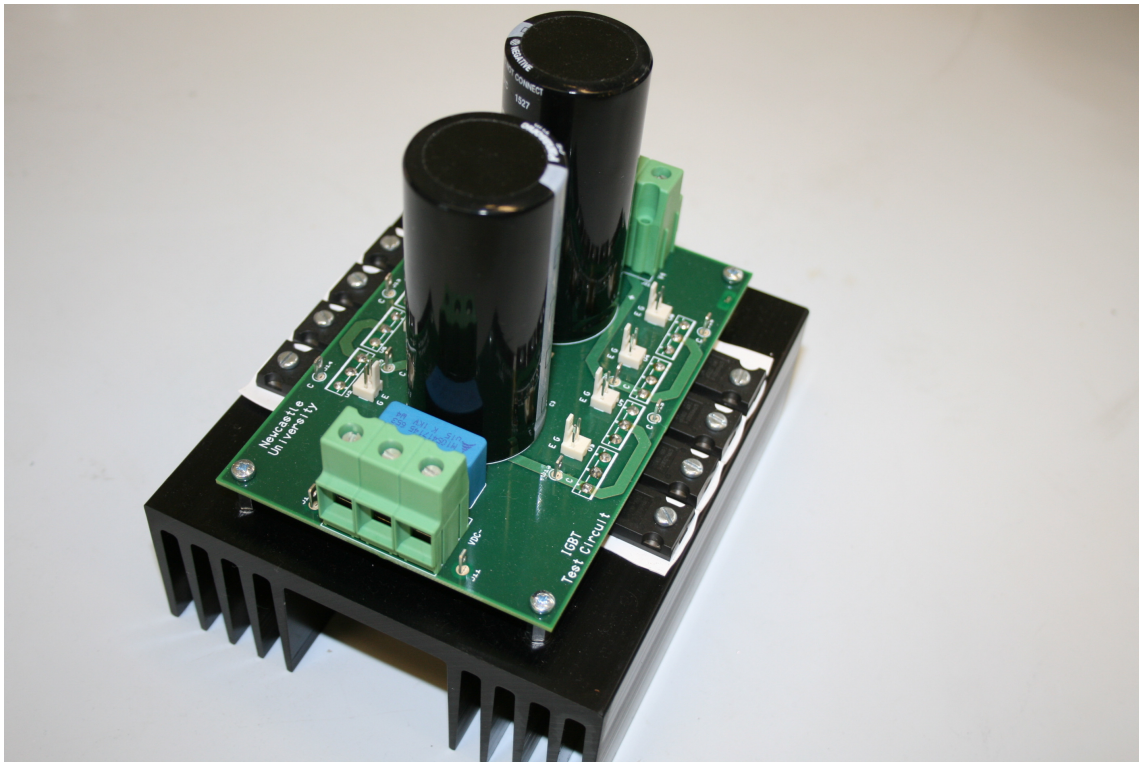

Figure 6.3: Inverter PCB

Texas Instruments F28335 eZdsp evaluation board and the connected power converter hardware. The main features included that are used in this project are:

- *Gate drive interface* - The gate drive interface includes connections for 6 pairs of PWM signals to be connected to external gate drive boards. Two of these connections are used in this project, one for each leg of the H-bridge inverter. The gate drive interface allows fault signals to be received from the external gate drive boards. A fault reset output is included to allow fault signals to be cleared.

- *Sensor interface* - Ten sensor connections are included, allowing external sensors to be powered from the general purpose power interface board and connecting the sensor signals to the processor ADC inputs via an op-amp. Two of these sensors are used for the control of the power inverter, a voltage sensor is used to detect the V_{PCC} voltage and a current sensor is used to measure the inverter output current. A further two current sensors are used to monitor the network power flow.

- *Sensor out-of-range trip circuit* - This circuit employs a voltage window detector to facilitate fast hardware over-current protection. The upper and lower limits of the voltage window are set using a pair of variable resistors. The dual

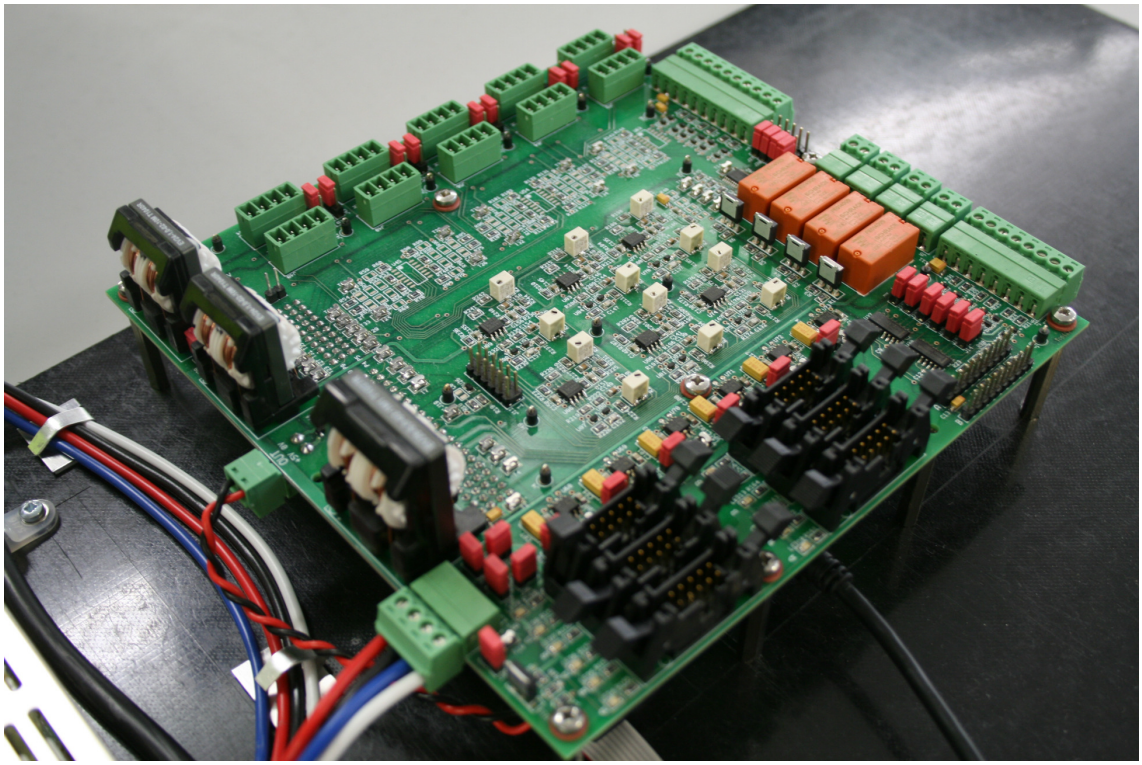

Figure 6.4: General Interface Board

signal voltage comparator is connected to a trip zone input on the DSP which is used to disable the PWM outputs.

- *On board relays* - The board has four individual MOSFET driven relay circuits which are all used in this project. Two relays are used as the DC-link relays to allow the DSP board to fully isolate the DC power source. The second pair of relays are used as the utility connection relays, allowing the connection to the utility to be controlled and LOM events to be forced.

6.2.3 Gate Drives

The gate drive PCB is shown in Figure 6.5. Two of these boards are used in this project, with each controlling a different leg of the inverter. Each board has a pair of opto-couplers which are used to provide full isolation for each PWM channel between the high voltage power converter and the low voltage DSP. Two isolated DC-DC converters, one for each channel, are used to provide sufficient voltage to turn the IGBT's on.

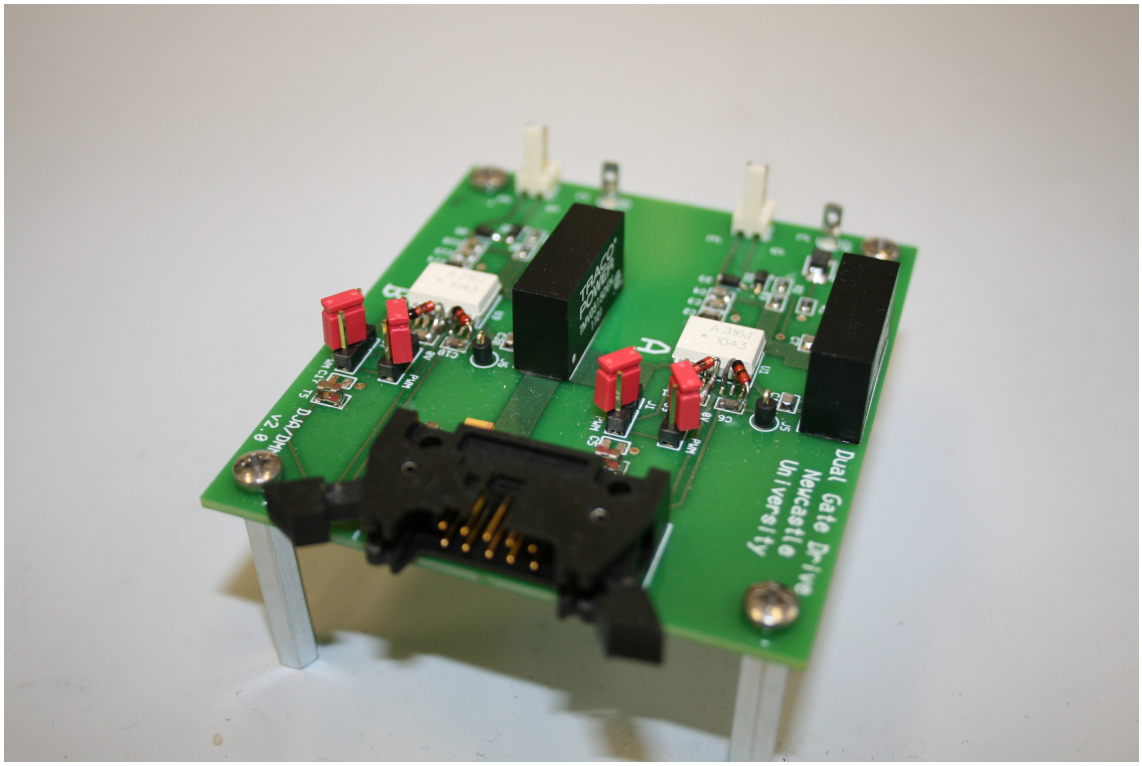

Figure 6.5: Gate Drive PCB

6.2.4 LC Line Filter

A series connected LC line filter is connected to the output of the inverter, as shown in Figure 6.1. This lowpass filter was designed to have a cut-off frequency, f_c, of 1 kHz. The filter is included to remove the high frequency switching component from the inverter output power. The same equation, 6.1, that is used to design the scaled power laboratory test bench LC filter is used to determine the values of L and C that are used.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{6.1}$$

The inductance, L, was chosen by selecting a reasonable level of inductance with a suitable current rating. The maximum inverter output current was set a 6 Amps, resulting in the selection of two 330 μH inductors with at 6 Amp current rating, giving a total filter inductance of 660 μH. The resultant calculated capacitor value is 40 μF. The PSpice simulation environment was used to confirm that the calculated values were correct. A frequency sweep was completed and the obtained bode plot is shown in Figure 6.6. The large decrease in gain at the 1 kHz point confirms that the filter will greatly reduce all signal components with a frequency over 1 kHz.

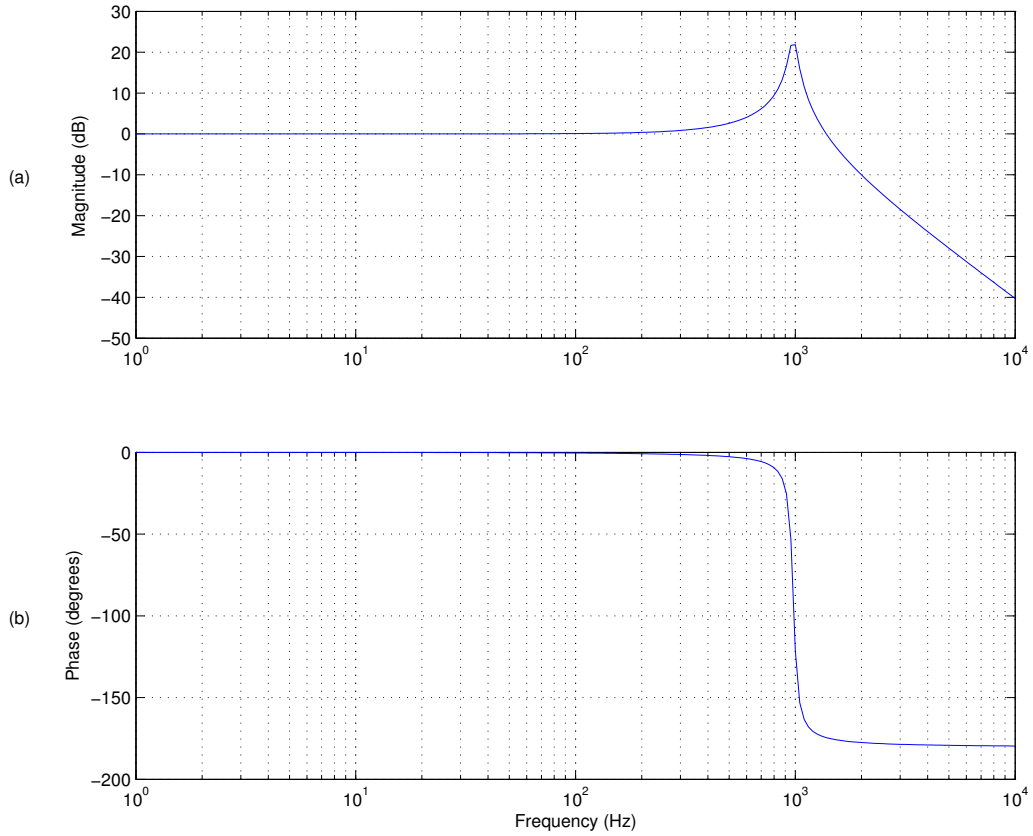

Figure 6.6: Bode plot for 500 W test bench LC line filter

6.2.5 Local RLC Load

The local RLC load, as in the scaled power laboratory test bench, represents any devices connected to the local power network. It is specifically designed to be resonant at 50 Hz. This will reduce the likelihood of any frequency drift or instabilities occurring during a LOM event. This is the case as the generators normal operating condition is to output power at a unity power factor and the RLC local load applies a zero phase shift at 50 Hz. Another factor to note about the RLC load is the reduced gain at high frequencies, meaning all high frequencies will be reduced in amplitude. These two characteristics mean that the RLC load represents the most challenging load for the detection of LOM events, hence why it is specified in the IEEE standard 929-2000.

R was chosen to be 60 ohms, as this hardware was readily available at Newcastle University. This decision sets the working voltage of the system as the local power generation has already been set at 500 W, meaning local power consumption must also be 500 W to allow balanced power operation. Using equations 6.2 and 6.3, the RMS inverter output current is calculated to be 2.9 Amps and the RMS network

voltage is calculated to be 173 Volts. This means the grid connect auto-transformer is set at 72% to allow the local network voltage to match the grid voltage.

$$V = IR \tag{6.2}$$

$$P = IV \tag{6.3}$$

The same equations, 6.4 and 6.5, that were used to design the scaled power laboratory test bench RLC load were used to determine the values of L and C.

$$Q = R\sqrt{\frac{C}{L}} \tag{6.4}$$

$$L = \frac{R}{2\pi f Q} \tag{6.5}$$

By setting Q to equal 1, L was calculated to be 0.191 H and C was calculated to be 50 μF. The RLC values were checked using the PSpice simulation environment. A

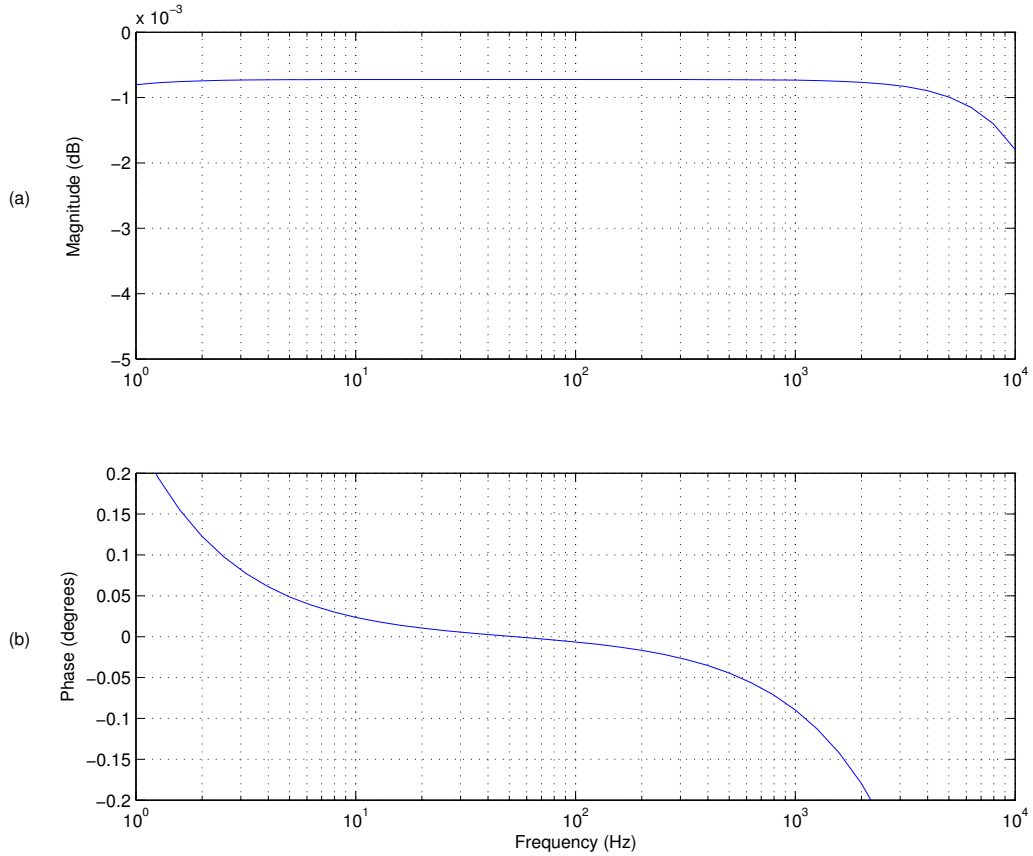

Figure 6.7: Bode plot for 1 kW RLC load

frequency sweep was carried out and the resultant Bode plot is shown in Figure 6.7. The notable characteristics of the Bode plot are the zero phase shift at 50 Hz and the reduced gain at high frequencies, indicating that the load is in fact resonant at 50 Hz.

The reduced gain at high frequencies is interesting as the proposed LOM detection technique is based on the measurement of the high frequency components detected within the V_{PCC} voltage. The Bode plot indicates that the magnitude of the high frequency components will be reduced by the load, meaning a thorough testing platform for the proposed LOM detection technique has been designed.

6.2.6 Operation Demonstration

As the control structure remains consistent with the scaled voltage laboratory test bench, a test was used to determine if the 500 W set-up behaved in the same way. A LOM test is used to indicate how the network power flow changes during a LOM test.

A LOM routine was created, 0.61 seconds in duration, which follows the following steps:

- *Step 1* - The system operates with both the inverter enabled and the utility relay closed at the balanced power condition for 0.31 seconds.
- *Step 2* - At the routine time of 0.31 seconds a LOM event is forced by opening the utility connection relays.
- *Step 3* - The routine runs for another 0.3 seconds to allow measured parameters to be sampled and the network power flow observed.

The LOM routine was completed at the balanced power operating point and the resultant waveforms are shown in Figure 6.8. Trace (d) shows that the utility relays are opened at 0.31 seconds.

Trace (b) shows that only high frequency current components are exchanged with the utility before the LOM event. This is because the system is operating at balanced power, meaning no substantial utility current exists. It is worth noting that this current waveform looks larger due to the low sampling rate used within the DSP. The system was monitored using a high bandwidth oscilloscope which indicated a near zero utility current at this particular operating condition.

Trace (a) shows the inverter output current, only a very small change occurs during the LOM event. This allows the inverter to sustain the V_{PCC} voltage, as shown in

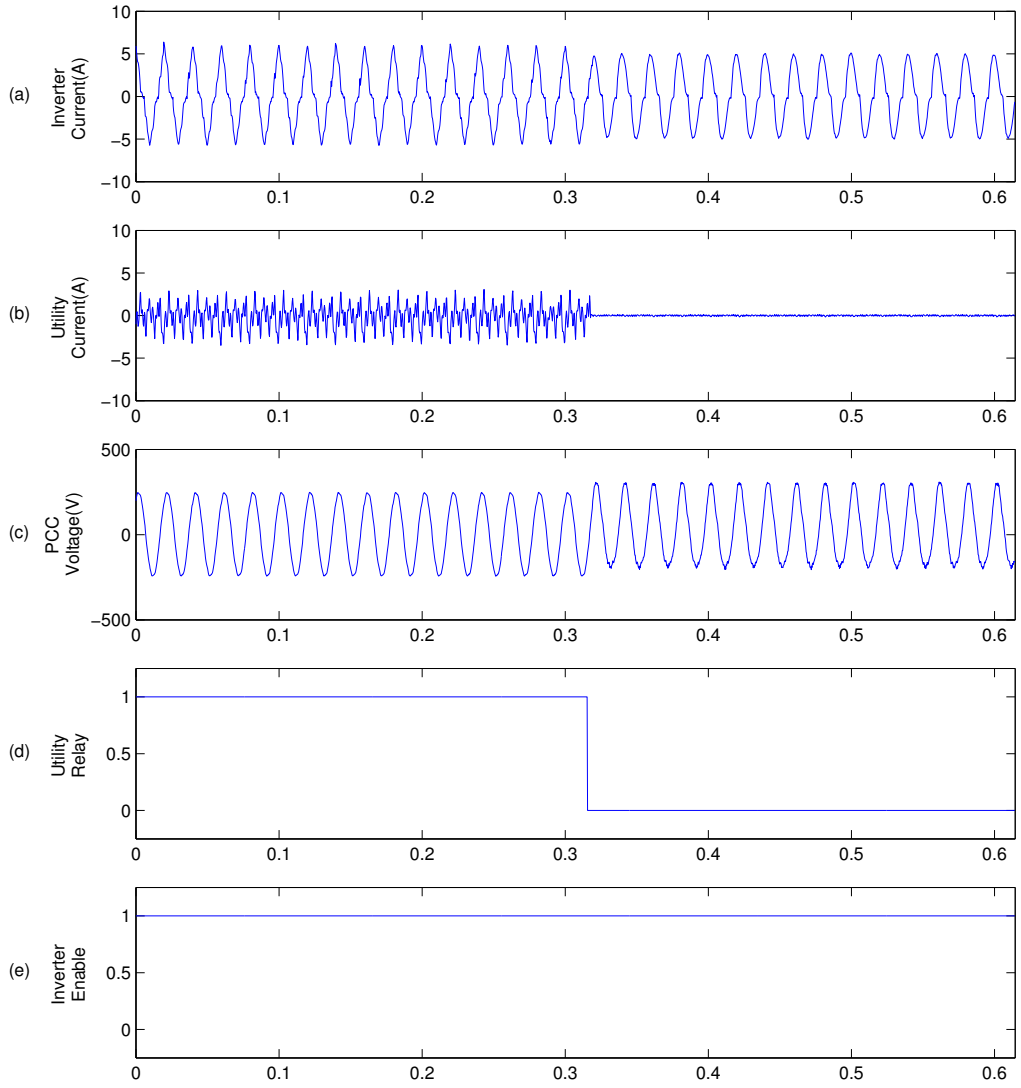

Figure 6.8: Operation demonstration at 170 V

trace (c). As the inverter has synchronised to a voltage that it is creating, a stable power island can be said to have formed. This shows that local power generation matches local power consumption for this operating condition.

The operation of the 500 W laboratory test bench is as expected and is very similar to the operation of both the low voltage laboratory test bench and the corresponding simulation environment.

6.3 Results

This section presents results obtained when testing the proposed LOM detection technique using the 500 W laboratory test bench. The results presented are intended to verify the results obtained whilst testing the proposed LOM detection technique using the scaled power laboratory test bench.

6.3.1 Passive Monitoring

The passive monitoring routine remains unchanged from the description in Section 5.2. As the proposed LOM detection technique relies on the passive monitoring routine working correctly, it was decided to test it independently.

The passive monitoring routine relies upon a LOM event causing a change in the calculated spectral data for the measured V_{PCC} voltage. Specifically, a change in the mean and standard deviation of the spectral data during a LOM event is required. The passive routine was tested using the following steps:

- *Step 1* - The system operates connected to the grid at the balanced power operating condition. During this time 100 example grid connected mean and standard deviation pairs are calculated and stored.
- *Step 2* - The example grid connected mean and standard deviation pairs are used to calculate example passive thresholds. These thresholds would be used to enable the active LOM check routine.
- *Step 3* - The utility relays are opened to force a LOM event.
- *Step 4* - The inverter continues to output the same 500 W in a power island configuration. During this time 100 example islanded mean and standard deviation pairs are calculated and stored.

The results are shown in Figure 6.9. It was noticed during this test that a large separation exists between the grid connected and islanded pairs. In fact both characteristics roughly triple in magnitude during a LOM event. This feature meant that a change could be made to the threshold boundary calculation. The threshold boundary could now be designated to be further away from the calculated average point. This would mean that the system does not enable the active LOM check routine as often, increasing the overall power utilisation. The threshold boundary calculation was changed from $\pm 15\%$ of the average value to $\pm 50\%$ of the average value.

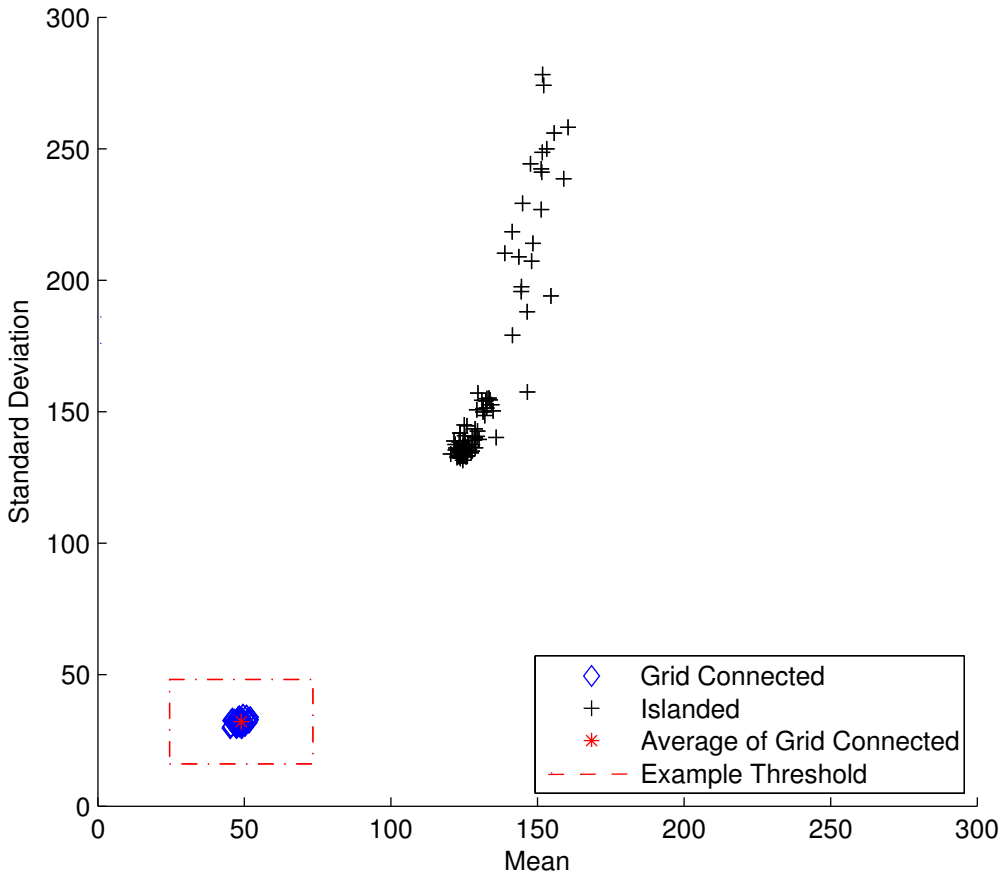

Figure 6.9: 100 example mean and standard deviation pairs for grid connected and islanded operation during balanced load condition

6.3.2 Balanced Power LOM Test

The active LOM check routine was added to the program to complete the proposed LOM detection technique. The active LOM check routine remains unchanged from the description in Section 5.3.

As the proposed LOM detection technique was complete it was tested at the balanced power condition to demonstrate the capability to detect a LOM event whilst the system is running at the most challenging operating condition. The LOM test, 0.6 seconds in duration, includes a LOM event being forced at 0.3 seconds. A further 0.3 seconds is included to observe both measured system characteristics and calculated internal parameters. The resultant experimental waveforms are shown in Figure 6.10.

Trace (d) shows that the utility relays are opened 0.3 seconds into the LOM test procedure ceasing any high frequency current exchange with the utility.

Trace (b) demonstrates that the system is running at the balanced power operating

condition. This trace can be seen to be the same as trace (b) in Figure 6.8 in Section 6.2.6.

Trace (g) and trace (h) show the calculated spectral data mean and standard deviation, respectively. After the LOM event occurs, there is a delay of 0.08 seconds before both variables exceed the respective thresholds. This delay is the time taken for the change in the measured V_{PCC} voltage harmonic content to propagate through the FFT and pair calculation procedures. After the delay, the mean and standard pairs can be seen to remain significantly above the internally calculated thresholds. This is indicative of a substantial change in the harmonic content in the measured

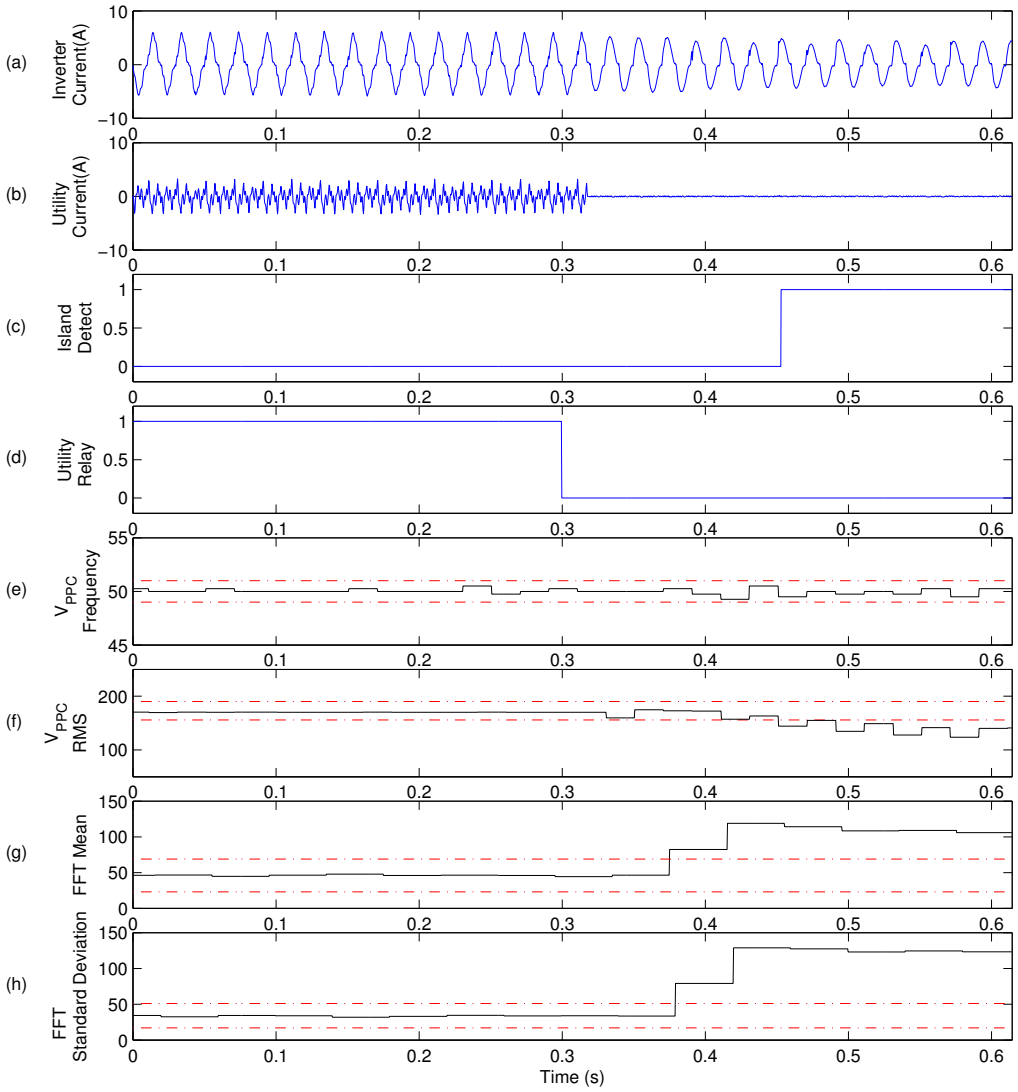

Figure 6.10: Balanced power operational waveforms for proposed technique using the 500 W laboratory test bench

V_{PCC}. As the threshold boundary has been exceeded, the system automatically enables the active LOM check routine.

The calculated V_{PCC} RMS, shown in trace (f), soon dips below the minimum threshold which is set within the under/over voltage amplitude routine. This change in V_{PCC} RMS is caused by the active LOM check routine. The effects of the active power shift can be observed in the slight dip in amplitude for alternate periods in the inverter output current, shown in trace (a). The current dips only occur after the active LOM check routine has been enabled. Trace(c) shows that the LOM event is indicated with a detection delay time of 0.15 seconds.

6.3.3 Extended Operation Test

The proposed LOM detection technique was tested at the balanced load operational point for a continuous period of 6 hours using the 500 W laboratory test bench. This test was completed to count the occurrence of two events:

- *False Detect Signal* - This event is counted to ensure that zero false detect signals occur as it is considered unacceptable for the system to turn off during normal operation.
- *Active LOM Check Enable* - This event is counted to determine the effect that the proposed LOM detection routine has on the overall system power utilisation.

During this extended operation test, zero false detect signals occurred, meaning the proposed LOM detection technique would not cause the inverter to cease producing power at unnecessary times.

As the threshold boundary within the passive monitoring routine is initialised to zero it is expected that the active LOM check routine is enabled during start up. The first few active LOM check enable events are needed to determine the correct position for the threshold boundary. During system start up in this test the active LOM check routine was required to operate 3 times before it settled on suitable values for the position of the passive threshold boundary. After the 3 start up enables, the system did not enable the active LOM check any more. This is due to the increase in the size of the threshold boundary box, detailed in Section 6.3.1. This means that for this test the system operates completely passively and has a near zero affect on power utilisation, with only a very short period of reduced power output being required during start up.

6.3.4 500 W Results Discussion

The results presented in this chapter have validated the operation of the scaled power laboratory test bench. The system operation is the same as the operation of the scaled power set-up and the formation of a power island occurs during the same testing procedures. The same LOM detection issue exists when testing using either platform: the small change in measured parameters occurring during a LOM event whilst the system is operating at the balanced power operating condition.

The testing of the proposed LOM detection technique indicates that a LOM event could be detected while the system was operating at the most challenging operational point. The detection delay time experienced at the balanced power operating condition of 0.15 seconds is very close to the detection delay observed for the same test completed on the scaled power laboratory test bench.

The early testing of the passive monitoring routine meant that the proposed technique was changed slightly, with the passive thresholds now being placed further away from the average point. The grid connected mean and standard deviation pairs, shown in 6.9, can be seen to be clustered very close together. This part of the system out performs the results obtained on the scaled power laboratory test bench. This could be related to an increase in high frequency components within the inverter output voltage, caused by an increase in the deadband delay and different filter characteristics.

The movement of the thresholds and the tightly clustered nature of the grid connected pairs resulted in the system remaining passive for long periods of time, as discovered during the 6 hour extended operation test. It was initially intended to complete the extended operation test over 24 hours, however, the fact that the calculated pairs remained consistently far from the passive thresholds meant that the test was cut short.

This improvement in system performance means that the proposed technique can be considered almost completely passive for the tests undertaken in this chapter. However, as with the scaled laboratory test bench, further tests would need to be completed, with changeable loads and a varying local generation capacity. The proposed LOM detection technique is thought to be able to adapt to any wider network change by simply repositioning the passive thresholds by operating actively for a short period of time. The improvements observed using the 500 W laboratory test bench simply indicate that these active periods may be less frequent.

Chapter 7

Conclusion

This chapter briefly explains the key results and important outcomes of the previous chapters and is split into two main sections. The first section draws together the important features of the low voltage laboratory test bench and how it was used to investigate a multitude of different LOM detection techniques. The second section provides a discussion of the results for the proposed LOM detection routine including preliminary testing using the low voltage laboratory test bench and verification using the more realistic 500 W laboratory test bench. Each section includes suggestions for further work and improvements.

7.1 Low Voltage Laboratory Test Bench

The literature review at the start of this thesis underlines the need for further development in renewable energy generation. Distributed generation can be considered one of the major technology areas involved in increasing the proportion of energy generated from renewable energy sources. According to IEEE connection standards, power islands can not be allowed to occur within the distribution network. A robust LOM event detection procedure must be included for any utility connected power converter. The power converter chosen for the focus of this work is the single-phase inverter. This decision was made due to the diversity of applicable domestic scale DC generation devices that are based on renewable energy sources. The IEEE connection standards fully specify the test bench that should be used to test different LOM detection routines. It was decided that a scaled power laboratory test bench should be used to allow safe and accurate testing of LOM detection routines.

7.1.1 Low Voltage Laboratory Test Bench Operation

The low voltage laboratory test bench was designed and constructed to mimic a standard DG unit installation, disregarding the type of the DC power source. The

system has three main power components, all connected to the same point, the PCC.

The first power component is the utility connection, this connection allows excess local power generation to be utilised using the larger power network. A controllable relay is included to remove this connection, forcing a LOM event.

The second power component is the RLC local load. This load provides a level of power consumption on the local power network, meaning the inverter can still output power after a LOM event has occurred. The RLC load is resonant at 50 Hz to reduce the likelihood of any phase drift when the inverter control is outputting power with a unity power factor.

The third power component is the single-phase inverter. The control of the H-bridge inverter is the focus of this work, incorporating a LOM detection routine within the normal control structure.

A power island is formed when a LOM is forced using the utility relay. This is due to way in which the control structure works. Using closed loop current control, the controller synchronises the output current with the sinusoidal voltage measured at the PCC. When the utility connection is present, the measured PCC voltage is dictated by the utility. However, after a LOM event, the control system can often maintain the PCC voltage which causes the inverter to synchronise the output current with the voltage it is creating. This causes a power island to be established and maintained by the inverter controller.

The most difficult situation for the detection of power islands is when local power generation matches local power consumption. By altering the magnitude and phase of the inverter output current the system is controlled to produce different levels of real and reactive power mismatch between local power generation and consumption. These different levels of power mismatch are needed to fully evaluate LOM detection routines.

7.1.2 Investigation of Currently Available LOM Detection Approaches

The lack of an industrial standard LOM detection method, along with the added complications of increased DG employment, results in the necessity for further research to be completed. As many LOM detection routines have been proposed and developed, both in literature and available products, it was decided that an array of currently available LOM detection routines should be tested. This was to allow the different approaches to be understood and to provide a base of results to allow direct comparison with the proposed LOM detection routine which has been developed during the completion of this work.

7.1.2.1 Passive LOM Detection Technique Investigation

Passive LOM detection techniques aim to detect LOM events solely using parameters measured at the terminals of the inverter. This means that there is no introduced negative affect on the inverter output power. As there is no delay whilst any introduced inverter output feature propagates through the power system, the tested passive LOM detection techniques exhibit fast detection delay times.

The two tested methods demonstrate a fundamental issue associated with passive LOM detection techniques, the existence of a NDZ. When the local generation is equal or close to the local power consumption, passive LOM detection techniques struggle to detect a LOM event. This is due to the small or zero power exchange with the utility, meaning only small changes in system parameters occur during a LOM event. The size of the NDZ is largely dependant on decisions made during the development process. There is a fundamental trade off between the size of the NDZ and the probability of a false LOM indication signal being produced. As IEEE connection standard 1547.1 stipulates that a NDZ cannot exist if the technique is to be used in a product, the two passive LOM detection techniques have to be disregarded for use as the sole method of LOM detection. This fact does not render the developed systems useless, instead, the passive LOM detection methods can be incorporated within a larger technique, as demonstrated in the later project work.

Comparing the two passive LOM detection techniques developed, the under/over voltage amplitude and frequency technique was shown to detect LOM events over a wider range of operating conditions. This meant it was chosen for use within the later work.

7.1.2.2 Active LOM Detection Technique Investigation

Active LOM detection techniques introduce a disturbance within the power output of the inverter. The effect that this disturbance has on the measured parameters is used to determine if the utility connection is present.

The big advantage of the tested active LOM detection techniques is the zero NDZ, meaning they can detect a LOM event for any operating condition. This is vital if the technique is to be employed in a product as it allows the system to comply with IEEE connection standards.

The development of the four tested active LOM detection techniques demonstrates a trade off between three factors:

- *Disturbance Size and Frequency* - An additional disturbance with a larger magnitude will result in a more substantial change in the measured parameters

during a LOM event, however, the power quality or power utilisation will normally be degraded further. The disturbance frequency also directly relates to the detection delay time.

- *Threshold Placement* - The placement of the thresholds can be widened to reduce the likelihood of a false LOM indication signal, however, this will increase both the probability that a LOM event is not detected and the average detection delay time.
- *Detection Delay Time* - A decrease in detection delay time can be achieved completing one of the following actions:
  - increasing the disturbance size so that the disturbance will propagate through the power system faster.
  - decreasing the acceptable grid connected range so that the thresholds are exceeded faster.

The active and reactive power shift LOM detection routines are similar in operation, producing similar detection delay times. The main negative associated with these two techniques is the power utilisation as the inverter will not always be producing 100% of the generated power. The reactive shift routine has the additional complication of grid connection standards relating to the allowable output power factor of connected generators.

The second harmonic injection LOM detection routine proved to be the quickest LOM detection routine. An issue with this LOM detection method is that the magnitude of the injected 100 Hz signal must be significantly larger than the background 100 Hz component of the utility. This needs to be done to create a rise in the 100 Hz component when a LOM event occurs, and to allow the threshold to be chosen at a suitable level to avoid erroneous LOM indication signals.

The zero current pulse LOM detection technique produced the longest detection delay times. Whilst this detection delay time is largely dependant on the position and frequency of the zero current pulse, an adequate LOM detection routine was produced, lying well within the 2 second limit set by the IEEE connection standards. A negative factor relating to the zero current pulse technique is the high frequency current and voltage spikes that occur, this reduces power quality and could damage any sensitive equipment that is connected.

7.1.3 Further Work

If further work was to be completed with the scaled power laboratory test bench it would be interesting to investigate a larger array of LOM detection techniques.

Whilst the work completed investigates the majority of the different types of LOM detection technique, more specific methods that have been proposed by companies and research institutions could be tested.

Another avenue of further work would be to expand the test bench to include two local generators. This would involve connecting another completely separate single-phase inverter to the PCC. With two inverters connected to the same local power network, the different LOM detection methods could be tested to see if they interact with each other. The dual inverter case could be operated with the same LOM detection routine running on both inverter controllers or a different LOM detection routine on each inverter controller. This investigation would provide an insight into which LOM detection technique performs the best when multiple inverters are connected to the same local power network, which is becoming a more likely scenario as the popularity of DG increases.

7.2 Proposed LOM Detection Technique

The proposed LOM detection routine is a completely self-tuning hybrid routine with two stages of operation.

The first passive mode of operation runs continuously and is used to indicate when a change in spectral data has occurred that could have been caused by a LOM event. This passive monitoring sequence works on the principle that the spectral analysis after a LOM event will never completely match the spectral data calculated whilst the system is operating connected to the utility. The change in the harmonic content of the measured PCC voltage is due to an altered variety of connected devices and a rise in network impedance.

The passive monitoring sequence is used to flag when a LOM event may have occurred, a second active mode of operation is needed to verify the status of the utility connection. An active power shift procedure is used to force the PCC voltage to exceed thresholds set within an under/over voltage amplitude and frequency checking routine. If the utility connection is proven to exist, the active check mode can re-specify the thresholds within the passive monitoring routine. This allows the system to be self-tuning and adaptive during network changes.

The basic idea of a hybrid LOM detection technique is to maintain the zero NDZ of an active technique whilst not introducing the active disturbance too often.

7.2.1 Low Voltage Laboratory Test Bench Results

The results obtained when testing the passive monitoring routine demonstrate a clear separation in the mean and standard deviation pairs between the grid connected

and islanded values. This indicates that the passive monitoring routine can initially detect that a LOM event may have occurred, before the active LOM check is used to verify the existence of the utility connection. This is integral to the success of the proposed LOM detection routine as if the passive monitoring routine did not flag that a LOM event may have occurred, the LOM event would go undetected, resulting in the existence of a NDZ.

The active LOM check routine had been proven to detect a LOM event regardless of the operating condition. This meant that it could be added to the proposed LOM detection technique to produce a robust system. The periods of full power output allow the placement of the passive threshold boundary to be based on results calculated from data sampled at full power output. This results in the thresholds being determined from data more consistent with the normal output power of the inverter.

The completed proposed LOM detection technique was proven to detect a LOM event at any power mismatch level, including the balanced load condition, demonstrating a zero NDZ.

The detection delay time graph shows that the system can detect LOM events very quickly for larger power mismatch levels due to the constant operation of the under/over voltage amplitude and frequency routine. In fact the shape of the graph indicates that the active shift procedure is only needed when operating within the NDZ for the under/over voltage amplitude and frequency method.

The detection delay times experienced across the different power mismatch conditions are similar to what can be expected from the solely active LOM detection techniques that were tested. As the detection delay time is one of the major concerns when implementing a hybrid LOM detection technique, this is considered successful.

The 24 hour extended operation test demonstrates that the proposed LOM detection technique does not enter the active LOM check routine very often. This means that the proposed LOM detection technique does not have a large effect on the power utilisation when operating with a constant load.

7.2.2 500 W Verification of Results

The 500 W laboratory test bench was designed and constructed with the aim of proving that the proposed LOM detection technique could operate successfully when using hardware more typical of a domestic scale DG installation. The operation of the test bench, along with island formation, was shown to be similar to that of the scaled power laboratory test bench and corresponding simulation model.

The initial testing of the passive monitoring routine showed that a much larger difference between the grid connected and islanded spectral data existed, when compared to the results obtained using the scaled power laboratory test bench. This meant that the passive thresholds could be placed further away from the average point. Another observed improvement was that the grid connected pairs appeared to be more tightly clustered together.

These system improvements meant that the proposed LOM detection routine can be considered almost completely passive when operating with a constant load. This improves the results considerably, with almost no overall reduction in power utilisation being caused by the operation of the proposed LOM detection technique.

7.2.3 Further Work

The range of different LOM detection techniques that have been evaluated throughout the completed work served to provide results for comparison with the proposed technique. Whilst techniques were chosen to cover LOM detection techniques that were based on the more popular fundamental principles, it would be interesting to investigate some of the more popular techniques more specifically. This could involve the purchase of a range of grid connect power converters to analyse the apparent effects of the implemented LOM detection techniques.

As the popularity of DG unit installations increases, the effects of having many connected generators on the same local power network needs to be explored. This would involve the design and construction of a multiple generator laboratory test bench. Different schemes could be tested to investigate the levels of interaction and the effects this has on the performance of the individual techniques. It would be interesting to test how the system reacts when inverters are installed that are operating with the same LOM detection scheme, as certain methods, such as harmonic injection, may experience issues leading to false detects and non detects.

A further experiment involving the proposed LOM detection technique would be an investigation in to how the system reacts to more realistic network conditions. This would involve monitoring the amount of time the system spends actively re-tuning the passive thresholds, indicated the actual effect that the system has on power utilisation. This test could be done in two ways:

- *Changeable Load* - The RLC load could be replaced with a controllable RLC load, this could then be programmed to follow a typical household load pattern.

- *Field Trials* - This would involve the installation of a power converter, operating with the proposed LOM detection technique, within a domestic environment. This would provide a robust and thorough evaluation of the proposed LOM detection technique.

Within the passive monitoring routine the passive threshold boundary is currently set by specifying maximum and minimum values for the mean and standard deviation pairs. This effectively draws a threshold rectangle around the spectral data pairs. Further work could be completed to investigate the possibility of a more intelligent way to distinguish between the grid connected and islanded information.

Appendix A

Proposed Technique Program Code

```
//###########################################################################
//
// FILE:    F28335_base.c (working proposed technique)
// Author:  A.Watts
//
// TITLE:  LV island detect setup control
//
//
#define PI 3.141592653589
#define TABLEN  720                                     // Set length of sine/cosine look-up tables
#define DATA_STORE_LEN          0x800   // Set length of data store records to 2k

// The following lines can be used to time code
#define PULSE_TP4 GpioDataRegs.GPASET.bit.GPIO14 = 1; GpioDataRegs.GPACLEAR.bit.GPIO14 = 1;
#define PULSE_TP5 GpioDataRegs.GPASET.bit.GPIO15 = 1; GpioDataRegs.GPACLEAR.bit.GPIO15 = 1;


#include "DSP2833x_Device.h"              // DSP2833x Headerfile Include File
#include "DSP2833x_Examples.h"            // DSP2833x Examples Include File
#include "F28335_drive_function_prototypes.h"   // F28335 drive header file
#include "DSP2833x_CpuTimers.h"

#include <stdlib.h>
#include <math.h>
#include <string.h>
#include <stdio.h>
```

```
// Function prototypes for functions defined in this file
// Code located in ext RAM
void set_up_data_stores(void);
void set_up_look_up_tables(void);
void panel_controls(void);

void spi_xmitDACA(Uint16 a);
void spi_xmitDACB(Uint16 a);
void spi_xmitDACC(Uint16 a);
void spi_xmitDACD(Uint16 a);

// Interrupt service routines defined in this file
interrupt void epwm1_isr(void);


// Global variables

int      *s1,*s2,*s3,*s4,*s5,*s6,*s7,*s8;// pointers for data store
float sinwt[TABLEN], coswt[TABLEN];      // look-up tables (code quicker when declared in INT RAM)

Uint16   flag1=0,flag2=0,flag3=0,flag4=0,flag5=0;

int      B0=0,B1=0,B2=0,B3=0,B4=0,B5=0,B6=0,B7=0,B8=0,B9=0,B10=0,B11=0,B12=0,B13=0,B14=0,B15=0,B16=0;

int par1=0,par2=0,par5=0,par6=0;         // Parameters passed in from control panel
Uint16 par4=0,par3=0;
Uint16   se=0;                                  // data store enable flag
Uint16   store_counter=0;                // data store index
unsigned long ISR_count1=0;              // ISR counter (increments every ISR execution)
```

```
unsigned long LoopCount=0;                  // RS232 data transfer counts
unsigned long download_counter=0;
Uint16 ErrorCount;                                  // used by RS232 code
Uint16 T0_count=0;
int DACA=0,DACB=0,DACC=0,DACD=0;//integers used as DAC output updates


//Data store variables
int Vdc=0;
float Vdcscaled=0;
Uint16 storefull=0;
Uint16 download_complete=0;
int store_sample=0;

//Status Monitoring Variables
int inverter_output=0;
int utility_relay=0;

//PLL variables
int k2=0;
int sample2=0;
float PLLmid2=0,PLLinput2=0,PLLoutput2=0;
float filterinput2=0,filteroutput2=0;
int thetaout2=0;
float smallin2[13],lp2[13];
float pro2=8,intg=0.01,PIout2=0,PIinteg2=0;

//current demand variables
int thetaoutoff=0;
```

```
float PLLoutputoffset=0;
float mag=0;
int theta=0;

//current control variables
float Istar=0;
int pointcount=0;
int x=0;
int record=0;
float Iactualmid=0;
float Iactual=0;
float Istarr[51];
float Iactualr[51];
float Istarcos=0;
float Iactualcos=0;
float dstar=0;
float qstar=0;
float Id=0;
float Iq=0;
float PIinD=0,PIintD=0,ig=0.002,pg=2,PIoutD=0;
float PIinQ=0,PIintQ=0,PIoutQ=0;
float Irefsin=0;
float Irefcos=0;
int PWM1=0,PWM2=0;
int PWMA=0,PWMB=0;

//island routine variable
int island_routine=0,routine_time=0,routine_finished=0,island_detect=0,island_time=0;
```

```
int sub=0,sub2=0;
int intera=0, interb=0;


float VPCC=0;
int r=0;


//island detect variables
#define N 256
int position=0;
int sector=0;
float n2=N;
float Ptotal=0;
int n1=0;
int j=0;
int k=0;
int p=0;
int q=0;
int a=0;
int b=0;
float c=0;
float xr[N];
float xi[N];
float twid[N];
float xmag[N];
float bfly[2]={0,0};
float FFT=0;
int count=0;
```

```
int activate_DFT=0;




float win[256];


int out=0;
unsigned long long start=0;
int activate_DFT2=0;
float FFT_switch=0;
float FFT_total=0;
float mean=0;
float sd=0;
float sd_total=0;
float mean_ave=0;
float last_mean=0;
float sd_ave=0;
float last_sd=0;
int active_shift=0;
float Vrms=0, PLLinput_tot=0;
float mean_thresh_tot=0, mean_thresh=0, sd_thresh_tot=0, sd_thresh=0;
int run=0;
int thresh_calc=0;
float mean_thresh_min=0, sd_thresh_min=0;
int start_delay=0;
int valid_thresh=0;
int count_thresh_calc=0;
```

```
int false_detect=0;
int in_DFT=0;
float freq_timer=0;
float freq=0;
float freq_trip=0;
float twid1=0, twid2=0;


static const unsigned int BitReverseTable256[] =
{
  0x00, 0x80, 0x40, 0xC0, 0x20, 0xA0, 0x60, 0xE0, 0x10, 0x90, 0x50, 0xD0, 0x30, 0xB0, 0x70, 0xF0,
  0x08, 0x88, 0x48, 0xC8, 0x28, 0xA8, 0x68, 0xE8, 0x18, 0x98, 0x58, 0xD8, 0x38, 0xB8, 0x78, 0xF8,
  0x04, 0x84, 0x44, 0xC4, 0x24, 0xA4, 0x64, 0xE4, 0x14, 0x94, 0x54, 0xD4, 0x34, 0xB4, 0x74, 0xF4,
  0x0C, 0x8C, 0x4C, 0xCC, 0x2C, 0xAC, 0x6C, 0xEC, 0x1C, 0x9C, 0x5C, 0xDC, 0x3C, 0xBC, 0x7C, 0xFC,
  0x02, 0x82, 0x42, 0xC2, 0x22, 0xA2, 0x62, 0xE2, 0x12, 0x92, 0x52, 0xD2, 0x32, 0xB2, 0x72, 0xF2,
  0x0A, 0x8A, 0x4A, 0xCA, 0x2A, 0xAA, 0x6A, 0xEA, 0x1A, 0x9A, 0x5A, 0xDA, 0x3A, 0xBA, 0x7A, 0xFA,
  0x06, 0x86, 0x46, 0xC6, 0x26, 0xA6, 0x66, 0xE6, 0x16, 0x96, 0x56, 0xD6, 0x36, 0xB6, 0x76, 0xF6,
  0x0E, 0x8E, 0x4E, 0xCE, 0x2E, 0xAE, 0x6E, 0xEE, 0x1E, 0x9E, 0x5E, 0xDE, 0x3E, 0xBE, 0x7E, 0xFE,
  0x01, 0x81, 0x41, 0xC1, 0x21, 0xA1, 0x61, 0xE1, 0x11, 0x91, 0x51, 0xD1, 0x31, 0xB1, 0x71, 0xF1,
  0x09, 0x89, 0x49, 0xC9, 0x29, 0xA9, 0x69, 0xE9, 0x19, 0x99, 0x59, 0xD9, 0x39, 0xB9, 0x79, 0xF9,
  0x05, 0x85, 0x45, 0xC5, 0x25, 0xA5, 0x65, 0xE5, 0x15, 0x95, 0x55, 0xD5, 0x35, 0xB5, 0x75, 0xF5,
  0x0D, 0x8D, 0x4D, 0xCD, 0x2D, 0xAD, 0x6D, 0xED, 0x1D, 0x9D, 0x5D, 0xDD, 0x3D, 0xBD, 0x7D, 0xFD,
  0x03, 0x83, 0x43, 0xC3, 0x23, 0xA3, 0x63, 0xE3, 0x13, 0x93, 0x53, 0xD3, 0x33, 0xB3, 0x73, 0xF3,
  0x0B, 0x8B, 0x4B, 0xCB, 0x2B, 0xAB, 0x6B, 0xEB, 0x1B, 0x9B, 0x5B, 0xDB, 0x3B, 0xBB, 0x7B, 0xFB,
  0x07, 0x87, 0x47, 0xC7, 0x27, 0xA7, 0x67, 0xE7, 0x17, 0x97, 0x57, 0xD7, 0x37, 0xB7, 0x77, 0xF7,
  0x0F, 0x8F, 0x4F, 0xCF, 0x2F, 0xAF, 0x6F, 0xEF, 0x1F, 0x9F, 0x5F, 0xDF, 0x3F, 0xBF, 0x7F, 0xFF
};
```

```
int main(void)
{
Uint16 ReceivedChar=0;
char *msg;
char sbuf[100],ibuf[100];                    // character buffer for RS232
char letter[100],temp=0;
Uint16 i=0,nc=0;
for (k2=1;k2<52;k2++)
        {
        Iactualr[k2]=0;
        Istarr[k2]=0;
        }


for (k2=1;k2<13;k2++)
{smallin2[k2]=0;}
lp2[1]=lp2[11]=0.0129;
lp2[2]=lp2[10]=0.0285;
lp2[3]=lp2[9]=0.0706;
lp2[4]=lp2[8]=0.1247;
lp2[5]=lp2[7]=0.1697;
lp2[6]=0.1872;


for (k2=0;k2<N;k2++)
    {
```

```
        twid[k2]=sin((2*PI*k2)/N);
    }
for (k2=0;k2<N;k2++)
    {
        win[k2]=0.54-(0.46*cos(2*PI*k2/(N-1)));
    }


   set_up_data_stores();                    // set up and initialise data stores in ext RAM
   set_up_look_up_tables();                 // set up sine and cosine look-up tables

// Clear RS232 input string buffer
        for (i=0; i < 100; ++i)
                letter[i]=0;


// Initialize System Control:
// PLL, WatchDog, enable Peripheral Clocks
// This example function is found in the DSP2833x_SysCtrl.c file.
   InitSysCtrl();
// Init the pins for the SCI-A port (RS232).
   InitSciaGpio();

// Init the pins for the SPI-A port (DAC).
   InitSpiaGpio();

// Initalize GPIO:
// This example function is found in the DSP2833x_Gpio.c file and
// illustrates how to set the GPIO to it's default state.
```

```
// InitGpio();  // Skipped for this example

// Init GPIO pins for ePWM1, ePWM2, ePWM3
// These functions are in the DSP2833x_EPwm.c file
   InitEPwm1Gpio();
   InitEPwm2Gpio();
   InitEPwm3Gpio();
   InitEPwm4Gpio();
   InitEPwm5Gpio();
  // InitEPwm6Gpio();



// Initialise GPIO (gate drives, relays, DAC and test points)
   gpio_init();



// Clear all interrupts and initialize PIE vector table:
// Disable CPU interrupts
   DINT;

// Initialize the PIE control registers to their default state.
// The default state is all PIE interrupts disabled and flags
// are cleared.
// This function is found in the DSP2833x_PieCtrl.c file.
   InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
```

```
   IER = 0x0000;
   IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell Interrupt
// Service Routines (ISR).
// This will populate the entire table, even if the interrupt
// is not used in this example.  This is useful for debug purposes.
// The shell ISR routines are found in DSP2833x_DefaultIsr.c.
// This function is found in DSP2833x_PieVect.c.
   InitPieVectTable();

// Interrupts that are used in this example are re-mapped to
// ISR functions found within this file.

   EALLOW;  // This is needed to write to EALLOW protected registers
   PieVectTable.ADCINT = &epwm1_isr;  // ADC triggered ISR
   EDIS;    // This is needed to disable write to EALLOW protected registers


// Set up ADC (function below is located in DSP2833x_Adc.c)
// The following function sets ADCCLK to 37.5MHz if CPS = 1
// Need to adjust ADCTRL3 to set to 25MHz
   InitAdc();

// Initialise ADC sequencer 1 to read in phase currents, Vdc and test points
   adc_seq_init();

   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;        // ePWM TBCLK stopped
```

```
    EDIS;

    InitEPwmMods();

    EALLOW;
    SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
    EDIS;


// Set up SPI for DAC
    spi_fifo_init();        // Initialize the Spi FIFO
    spi_init();             // init SPI

// Set up Eqep1 for position and speed measurement
    eqep1_init();

// Enable CPU interrupts
    IER |= M_INT1;        // Enable CPU INT1 which is connected to PIE group 1



    PieCtrlRegs.PIEIER1.bit.INTx6 = 1;           // Enable ADCINT in the PIE
// Enable global Interrupts and higher priority real-time debug events:
    EINT;   // Enable Global interrupt INTM
    ERTM;   // Enable Global realtime interrupt DBGM

     scia_fifo_init();       // Initialize the SCI FIFO
     scia_echoback_init();  // Initalize SCI for echoback
```

```
//        GpioDataRegs.GPACLEAR.bit.GPIO13 = 1;    // Disable gate drive A
          GpioDataRegs.GPACLEAR.bit.GPIO17 = 1;    // Disable gate drive B


     LoopCount = 0;
          download_counter=0;
     ErrorCount = 0;
          i=0;


// IDLE loop. Just sit and loop forever:
    for(;;)
    {

          i=0;     //reset input character counter
          do {

                    // Wait for incoming character from RS232 port
                    while(SciaRegs.SCIFFRX.bit.RXFFST !=1){
                    LoopCount=LoopCount+1;
                    start=start+1;
                    if (start<8000)//complete FFT
                    {activate_DFT2+=1;}
                    else
                    {activate_DFT2=0;}
                    if ((activate_DFT2>4000)&&(activate_DFT==1))
                    {
                    in_DFT=1;
                    if (n2!=1)
```

```
{
            n1=n2;
n2=n2/2;
            j=0;
            do{
                  k=N*j/n1;
            p=j;
                        twid1=twid[k%N];
                        twid2=twid[(k+3*N/4)%N];
                        do{
                                    q=p+n2;
                                    ////////////////////////////////////////
                        a=p;
            b=q;
            c=xr[b];
            bfly[0]=xr[a]+xr[b];
            bfly[1]=xi[a]+xi[b];
            xr[b]=(xr[a]-xr[b])*twid1-(xi[a]-xi[b])*twid2;
            xi[b]=(xr[a]-c)*twid2+(xi[a]-xi[b])*twid1;
            xr[a]=bfly[0];
            xi[a]=bfly[1];
            xmag[(BitReverseTable256[a])]=sqrt((xi[a]*xi[a])+(xr[a]*xr[a]));
            xmag[(BitReverseTable256[b])]=sqrt((xi[b]*xi[b])+(xr[b]*xr[b]));
                                    ////////////////////////////////////////
            p=p+n1;
                        }while(p<N);
                        j+=1;
            }while(j!=n2);
```

```
                        }
                        ////////////////////////////////////
                        if (n2==1)
                {
                        activate_DFT=0;
                                in_DFT=0;
                }
                }

                }       // wait for XRDY =1 for empty state
                start=0;
                activate_DFT2=0;
                //n2=N;
                ReceivedChar = SciaRegs.SCIRXBUF.all;           // Get character
                temp = ReceivedChar & 0xFF;     // strip off the error bits
                letter[i]=temp;
                i++;
        }while(temp != '\n');

// Get incoming parameters from Labview GUI
        nc = sscanf(letter,"%d %d %d %d %d %d",&par1,&par2,&par3,&par4,&par5,&par6);

// Send values to Labview GUI -
        nc = sprintf(sbuf,"%u %u %u %d \r\0",se,store_counter,storefull,Vdc);
    scia_msg(sbuf);
        nc = sprintf(sbuf,"%lu %lu %u %d \r\0",
        mean_thresh,download_counter,
        download_complete,s1[download_counter]);
    scia_msg(sbuf);
```

```
    nc = sprintf(sbuf,"%d %d %d %d %d %d %d\r\n\0",s2[download_counter],s3[download_counter],
s4[download_counter],s5[download_counter],s6[download_counter],
s7[download_counter],s8[download_counter]);

scia_msg(sbuf);

    if (island_routine!=1)
    {
            if (par3 & 0x0001)
            {GpioDataRegs.GPBSET.bit.GPIO33 = 1;}//turn main relay on
            else
            {GpioDataRegs.GPBCLEAR.bit.GPIO33 = 1;}//turn main relay off
            if (par3 & 0x0002)
            {GpioDataRegs.GPBSET.bit.GPIO32 = 1;}//turn Bus A relay on
            else
            {GpioDataRegs.GPBCLEAR.bit.GPIO32 = 1;}//turn Bus A relay off
            if (par3 & 0x0004)
            {GpioDataRegs.GPASET.bit.GPIO27 = 1;}//turn Bus A Bypass relay on
            else
            {GpioDataRegs.GPACLEAR.bit.GPIO27 = 1;}//turn Bus A Bypass relay off
            if (par3 & 0x0008)
            {
            GpioDataRegs.GPASET.bit.GPIO13 = 1;//enable gate drive A
            inverter_output=1;
    //      se=1;
            }
            else
            {
            GpioDataRegs.GPACLEAR.bit.GPIO13 = 1;//disable gate drive A
```

```
        inverter_output=0;
        }
        if (par3 & 0x0010)
        {
                GpioDataRegs.GPASET.bit.GPIO10 = 1;//turn on grid relays (top)
                GpioDataRegs.GPASET.bit.GPIO11 = 1;//turn on grid relays (bottom)
                utility_relay=1;
        }
        else
        {
                GpioDataRegs.GPACLEAR.bit.GPIO10 = 1;//turn off grid relays (top)
                GpioDataRegs.GPACLEAR.bit.GPIO11 = 1;//turn off grid relays (bottom)
                utility_relay=0;
        }

}




if (storefull==1)
{
download_counter++;
}
if (download_counter==DATA_STORE_LEN)
{
download_complete=1;
se=0;
```

```
        storefull=0;
        }



   }//end forever loop
        return 0;
} // end main()

//////////////////////////////////////////////////////////////////////////////////////////
//////////////////////////////////////////////////////////////////////////////////////////
//      Primary ISR for current control synchronised to EPWM1                           //
//////////////////////////////////////////////////////////////////////////////////////////
//////////////////////////////////////////////////////////////////////////////////////////
// The ADC SEQ1 is triggerred on the positive apex of the carrier
// The CPU INT1.6 is triggered on end of sequence (EOS)
interrupt void epwm1_isr(void)
{

sub+=1;
if (sub==3)
sub=0;
   intera+=1;
   if(intera>=1000)
   intera=0;

//////////////////////////////////////////////////////////////////////////////////////////
//                                                    sweep ADC inputs
//////////////////////////////////////////////////////////////////////////////////////////
```

```
B0 = AdcRegs.ADCRESULT0 >>4;//Iactual
B1 = AdcRegs.ADCRESULT1 >>4;
B2 = AdcRegs.ADCRESULT2 >>4;
B3 = AdcRegs.ADCRESULT3 >>4;
B4 = AdcRegs.ADCRESULT4 >>4;
B5 = AdcRegs.ADCRESULT5 >>4;
B6 = AdcRegs.ADCRESULT6 >>4;
B7 = AdcRegs.ADCRESULT7 >>4;
B8 = AdcRegs.ADCRESULT7 >>4;
B9 = AdcRegs.ADCRESULT8 >>4;
B10 = AdcRegs.ADCRESULT9 >>4;//Vpcc
B11 = AdcRegs.ADCRESULT10 >>4;
B12 = AdcRegs.ADCRESULT11 >>4;
B13 = AdcRegs.ADCRESULT12 >>4;
B14 = AdcRegs.ADCRESULT13 >>4;
B15 = AdcRegs.ADCRESULT14 >>4;

////////////////////////////////////////////////////////////////////////////////////////////////////
//                                                                    Data store for FFT
////////////////////////////////////////////////////////////////////////////////////////////////////

VPCC=B10-2175;

if (sector==1)
{
active_shift=0;
        if (r<256)
        {
                FFT=xmag[r];
```

```
            xr[r]=VPCC*win[r];
            xi[r]=0;
            if((r>2)&&(r<127))
            FFT_total+=xmag[r];
            r+=1;
}
            if(r==127)
{
            last_mean=mean;
            mean=FFT_total/127;
            mean_ave=(mean+last_mean)/2;
            FFT_total=0;
            if((valid_thresh==1)&&((mean_ave>mean_thresh)||(mean_ave<mean_thresh_min)))
            thresh_calc=1;
}
if  ((r>129)&&(r<253))
{sd_total+=pow((xmag[r]-mean),2);}
if(r==255)
{
            activate_DFT=1;
            n2=N;
            last_sd=sd;
            sd=sqrt(sd_total/127);
            sd_ave=(sd+last_sd)/2;
            sd_total=0;
            if((valid_thresh==1)&&((sd_ave>sd_thresh)||(sd_ave<sd_thresh_min)))
            thresh_calc=1;

}
```

```
        if(r==256)
        {
        FFT=0;
        }
}


if (sector==0)
{
        r=0;
        if(thresh_calc==1)
        {
                active_shift=1;
                if (run>=5)
                {
                        run=0;
                        thresh_calc=0;
                        count_thresh_calc+=1;
                        mean_thresh=(mean_thresh_tot/5)*1.15;
                        sd_thresh=(sd_thresh_tot/5)*1.15;
                        mean_thresh_min=(mean_thresh_tot/5)*0.85;
                        sd_thresh_min=(sd_thresh_tot/5)*0.85;
                        mean_thresh_tot=0;
                        sd_thresh_tot=0;
                        valid_thresh=1;
                }
        }
```

```
}
```

```
////////////////////////////////////////////////////////////////////////////////////////////////
//                                                                10KHz Code
////////////////////////////////////////////////////////////////////////////////////////////////
if (sub==1)//every 3 interrupt sequences run the control code(10kHz)
{
```

```
////////////////////////////////////////////////////////////////////////////////////////////////
//                                                                Safety-monitor bus Vdc
////////////////////////////////////////////////////////////////////////////////////////////////
Vdc=B3;
Vdcscaled=Vdc*0.0115;
if ((Vdcscaled > 24)||(false_detect >20))//monitor Vdc level for safety
{

        GpioDataRegs.GPACLEAR.bit.GPIO13 = 1;    // Disable gate drive A
```

```
        GpioDataRegs.GPACLEAR.bit.GPIO17 = 1;   // Disable gate drive B
        GpioDataRegs.GPBCLEAR.bit.GPIO33 = 1;   //turn main relay off
        GpioDataRegs.GPBCLEAR.bit.GPIO32 = 1;   //turn Bus A relay off
        GpioDataRegs.GPACLEAR.bit.GPIO27 = 1;   //turn Bus A Bypass relay off
        GpioDataRegs.GPACLEAR.bit.GPIO10 = 1;   //turn off grid relays (top)
        GpioDataRegs.GPACLEAR.bit.GPIO11 = 1;   //turn off grid relays (bottom)

}

////////////////////////////////////////////////////////////////////////////////////////////
//                                                                  Island routine code
////////////////////////////////////////////////////////////////////////////////////////////
if (par3 & 0x0040)
{
        island_routine=1;
        se=1;
}
if(island_routine==1)
{
        routine_time=routine_time+1;
}
if (routine_time==3000)
{
        GpioDataRegs.GPACLEAR.bit.GPIO10 = 1;//turn off grid relays (top)
        GpioDataRegs.GPACLEAR.bit.GPIO11 = 1;//turn off grid relays (bottom)
        utility_relay=0;
//      GpioDataRegs.GPACLEAR.bit.GPIO13 = 1;//disable gate drive A
//      inverter_output=0;
}
```

```
if (routine_time==22500)
{
        routine_time=0;
        island_routine=0;
        routine_finished=1;
}
if ((routine_time>=10)&&(island_detect==0))//only check for island after 1mS
and if an island hasn't already been detected
{

        if ((Vrms<1.4249)||(Vrms>1.7415)||(freq>51)||(freq<49))
        {
            island_detect=1;
            island_time=routine_time-2000;
        }
}

if (par3 & 0x0020)
{
island_detect=0;
routine_time=0;
island_time=0;
island_routine=0;
mean_ave=400;
sd_ave=400;
}

if (par3 & 0x0008)//only start control code when
gate drive is enabled (stop system becoming unstable in start up time)
```

```
{

if (start_delay>=0)
start_delay+=1;
if(start_delay==2000)
{
start_delay=-1;
thresh_calc=1;
}
////////////////////////////////////////////////////////////////////////////////////////////////////
//                                                PLL code
//
////////////////////////////////////////////////////////////////////////////////////////////////////
//=============================================//
//              Input scale and phase detect   //
//=============================================//
sample2=sample2+1;
PLLinput2=(B10-2160)*0.0012;
PLLinput_tot+=(PLLinput2*PLLinput2);

filterinput2=(coswt[thetaout2/10])*PLLinput2;//multiply input with cos of thetaout
if (sample2%15==0)
        {
        smallin2[1]=smallin2[2];
        smallin2[2]=smallin2[3];
        smallin2[3]=smallin2[4];
        smallin2[4]=smallin2[5];
        smallin2[5]=smallin2[6];
        smallin2[6]=smallin2[7];
```

```
        smallin2[7]=smallin2[8];
        smallin2[8]=smallin2[9];
        smallin2[9]=smallin2[10];
        smallin2[10]=smallin2[11];
        smallin2[11]=filterinput2;
        filteroutput2=(smallin2[1]*lp2[1])+(smallin2[2]*lp2[2])+
    (smallin2[3]*lp2[3])+(smallin2[4]*lp2[4])+(smallin2[5]*lp2[5])+
    (smallin2[6]*lp2[6])+(smallin2[7]*lp2[7])+(smallin2[8]*lp2[8])+
    (smallin2[9]*lp2[9])+(smallin2[10]*lp2[10])+(smallin2[11]*lp2[11]);
        if (sample2==150)
                {sample2=0;}
        }

//=========================================//
//                frequency calc
//=========================================//
    freq_timer=freq_timer+1;
//=========================================//
//                      PI within PLL
//=========================================//
PIinteg2 = (intg*filteroutput2)+PIinteg2;
PIout2= PIinteg2+pro2*filteroutput2;
//=========================================//
//                      VCO
//=========================================//
thetaout2=thetaout2+36+PIout2;
if (thetaout2>=7200)
        {thetaout2=0;
        freq=10000/freq_timer;
```

```
    freq_timer=0;
        }
PLLoutput2=sinwt[thetaout2/10];

////////////////////////////////////////////////////////////////////////////////////////////////////
//                                                    Apply current offest and magnitude
////////////////////////////////////////////////////////////////////////////////////////////////////
mag=par2*0.004166;
theta=par1;
if (active_shift)
{mag=0.3099504;
}//mag*0.75;}

thetaoutoff=thetaout2+theta;
if (thetaoutoff>7200)
{thetaoutoff=theta-(7200-thetaout2);}
if (thetaoutoff>=7200)
        {thetaoutoff=0;}
if (thetaoutoff<0)
        {thetaoutoff=0;}
PLLoutputoffset=mag*sinwt[thetaoutoff/10];



///dft sector switch

if(thetaout2==0)
{
Vrms=sqrt(PLLinput_tot/200);
```

```
        if ((Vrms<1.4249)||(Vrms>1.7415)||(freq>51)||(freq<49))// island detect condition
        {
                false_detect+=1;
                freq_trip=freq;
                }
PLLinput_tot=0;
sector=sector+1;
if(sector==2)
{
sector=0;
if(thresh_calc)
{
        run=run+1;
        mean_thresh_tot+=mean_ave;
        sd_thresh_tot+=sd_ave;
}
}
}
//////////////////

////////////////////////////////////////////////////////////////////////////////////////////////
//                                                Current control loop
////////////////////////////////////////////////////////////////////////////////////////////////
Istar=-PLLoutputoffset;
pointcount=pointcount+36;
if (pointcount>=7200)
pointcount=0;
x=pointcount/10;
```

```
record=record+1;
Iactualmid=B0-2036;
Iactual=Iactualmid/825;
Istarr[record]=-Istar;
Iactualr[record]=-Iactual;
//=========================================//
//              Calculate delayed signals
//=========================================//
if (record == 51)
        {
    record=0;
        Istarcos=Istarr[1];
        Iactualcos=Iactualr[1];
    }
Istarcos=Istarr[record+1];
Iactualcos=Iactualr[record+1];
//=========================================//
//              Calculate d and q
//=========================================//
dstar=(Istar*sinwt[x])+(Istarcos*coswt[x]);
qstar=(Istar*coswt[x])-(Istarcos*sinwt[x]);
Id=(Iactual*sinwt[x])+(Iactualcos*coswt[x]);
Iq=(Iactual*coswt[x])-(Iactualcos*sinwt[x]);
//=========================================//
//      PI within current control
//=========================================//
PIinD=dstar-Id;
if(PIinD>2)
{PIinD=2;}
```

```
if(PIinD<-2)
{PIinD=-2;}
PIintD = (ig*PIinD)+PIintD;
PIoutD= PIintD+(pg*PIinD);

PIinQ=qstar-Iq;
if(PIinQ>2)
{PIinQ=2;}
if(PIinQ<-2)
{PIinQ=-2;}
PIintQ=PIintQ+(ig*PIinQ);
PIoutQ=(PIinQ*pg)+(PIintQ);
//=========================================//
//                          e(-jtheta)
//=========================================//
Irefsin= (PIoutQ*coswt[x])+(PIoutD*sinwt[x]);
Irefcos= (PIoutD*coswt[x])-(PIoutQ*sinwt[x]);
//=========================================//
//                          PWM out
//=========================================//
PWM1=1250-1250*Irefsin;
PWM2=1250+1250*Irefsin;
if (PWM1>2490)
        {PWM1=2490;}
if (PWM1<10)
        {PWM1=10;}
if (PWM2>2490)
        {PWM2=2490;}
if (PWM2<10)
```

```
        {PWM2=10;}
EPwm1Regs.CMPA.half.CMPA = PWM1;
EPwm2Regs.CMPA.half.CMPA = PWM2;
}

////////////////////////////////////////////////////////////////////////////////////////
//                                                    Send variables to data stores
////////////////////////////////////////////////////////////////////////////////////////
store_sample++;
if ((se==1) & (store_counter<DATA_STORE_LEN) & (store_sample==3))
{
s1[store_counter]= (int) B0;
s2[store_counter]= (int) B11;
s3[store_counter]= (int) (3392-B13);
s4[store_counter]= (int) (2111-B10);
s5[store_counter]= (int) Vrms*1000;
s6[store_counter]= (int) freq*1000;
s7[store_counter]= (int) sd_ave;
s8[store_counter]= (int) mean_ave;
store_counter++;
}
if (store_sample==3)
{store_sample=0;}

if ((store_counter==DATA_STORE_LEN) & (download_complete==0))
{
storefull=1;
}
////
```

```
}



//////////////////////////////////////////////////////////////////////////////////////////
//                                          Complete end of interrupt
//////////////////////////////////////////////////////////////////////////////////////////
AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;                  // Reset SEQ1
AdcRegs.ADCTRL2.bit.RST_SEQ2 = 1;                  // Reset SEQ2
AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;               // Clear INT SEQ1 bit
AdcRegs.ADCST.bit.INT_SEQ2_CLR = 1;               // Clear INT SEQ2 bit
PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;// Acknowledge this interrupt
T0_count = CpuTimer0Regs.TIM.half.LSW;  // Latch lower 16-bits of timer0
}



//////////////////////////////////////////////////////////////////////////////////////////
//////////////////////////////////////////////////////////////////////////////////////////
//      Function to set up and initialise data stores in external RAM (ZONE7A)
//////////////////////////////////////////////////////////////////////////////////////////
//////////////////////////////////////////////////////////////////////////////////////////
// Each integer array is 2k long
// The arrays are global
#pragma CODE_SECTION(set_up_data_stores, "codeA")
void set_up_data_stores(void)
{
```

```
        Uint16 i;

        s1 = (int *)calloc(DATA_STORE_LEN, sizeof(int));
        s2 = (int *)calloc(DATA_STORE_LEN, sizeof(int));
        s3 = (int *)calloc(DATA_STORE_LEN, sizeof(int));
        s4 = (int *)calloc(DATA_STORE_LEN, sizeof(int));
        s5 = (int *)calloc(DATA_STORE_LEN, sizeof(int));
        s6 = (int *)calloc(DATA_STORE_LEN, sizeof(int));
        s7 = (int *)calloc(DATA_STORE_LEN, sizeof(int));
        s8 = (int *)calloc(DATA_STORE_LEN, sizeof(int));

        for (i=0; i < DATA_STORE_LEN; ++i)
                {
                s1[i] = 0x0;
                s2[i] = 0x0;
                s3[i] = 0x0;
                s4[i] = 0x0;
                s5[i] = 0x0;
                s6[i] = 0x0;
                s7[i] = 0x0;
                s8[i] = 0x0;
                }
}
```

```
////////////////////////////////////////////////////////////////////////////////
////////////////////////////////////////////////////////////////////////////////
```

```
//      Function to set up floating point sine and cosine tables in internal RAM
////////////////////////////////////////////////////////////////////////////////
////////////////////////////////////////////////////////////////////////////////
#pragma CODE_SECTION(set_up_look_up_tables, "codeA")
void set_up_look_up_tables(void)
{
    Uint16 i;
        float angle;

        for (i=0; i < TABLEN; ++i)
                {
                angle = 2*PI*i/TABLEN;
                sinwt[i] = 1.0*sin(angle);
                coswt[i] = 1.0*cos(angle);
                }
}


////////////////////////////////////////////////////////////////////////////////
////////////////////////////////////////////////////////////////////////////////
//      Functions to transmit characters to SPI-A port
////////////////////////////////////////////////////////////////////////////////
////////////////////////////////////////////////////////////////////////////////
void spi_xmitDACA(Uint16 f)
{
    SpiaRegs.SPITXBUF=0x1000 | f;
    SpiaRegs.SPITXBUF=0x1000 | f;
}
```

```
void spi_xmitDACB(Uint16 f)
{
    SpiaRegs.SPITXBUF=0x5000 | f;
    SpiaRegs.SPITXBUF=0x5000 | f;
}
void spi_xmitDACC(Uint16 f)
{
    SpiaRegs.SPITXBUF=0x9000|f;
    SpiaRegs.SPITXBUF=0x9000|f;
}

void spi_xmitDACD(Uint16 f)
{
    SpiaRegs.SPITXBUF=0xD000|f;
    SpiaRegs.SPITXBUF=0xD000|f;
}
//===========================================================================
// End of code
//===========================================================================


%%% Local Variables:
%%% mode: latex
%%% TeX-master: "../thesis"
%%% End:
```

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