Voltage Equalisation Techniques for High Capacitance Device Modules

Simon Lambert

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School of Electrical and Electronic Engineering

Newcastle University

To my wife and family, without whom I may not have started and could never have finished

Abstract

Traditionally, the electrochemical battery has been the prime medium by which electrical energy is stored for future use. Increasingly, the demands of modern systems such as electric vehicles, renewable energy, distributed generation, smart grid and others has stretched the development of new chemistries, materials and assembly techniques for electrochemical batteries. Additionally, some load profiles in these applications demand extremely high dynamic behaviour which is either undeliverable by conventional electrochemical batteries or is undesirably damaging to these technologies. As such, a family of electrochemical storage, known generally as supercapacitors or ultracapacitors, have been developed and implemented for such applications. In recent years advancements in electrochemical technology has led to hybridisation of high capacitance devices. Lithium-ion capacitors that are used in this work are, with their higher cell voltage and modern packaging, expected to be among the next emerging families of state-of-the-art electrical energy storage devices.

The relatively low cell voltage of high capacitance cells requires them to be connected in series to attain a system level voltage. During charging and discharging, manufacturing tolerances between the cells results in voltage mismatch across the stack. Mismatched voltages are an inefficient use of the energy storage medium and can lead to dangerous failures in the cells. Several techniques exist to limit the variance in cell voltages of supercapacitors across a series connected stack. These range from simple systems which discharge the cells at higher voltages through resistors to more complex active converter systems which equalise the cell voltages through charge redistribution via a power electronic converter. Whilst the simpler schemes are effective they are very inefficient and as such are not suitable for use in many applications.

A number of active converter voltage equalisation schemes have been proposed in literature, however, each of these equalisation schemes exhibit flaws which either makes them less desirable or less effective for a broad range of applications. Therefore, a new equalisation converter topology is proposed which is designed for greater equalisation effectiveness, modularity and size. The proposed equalisation converter differs from previously published equalisation schemes by allowing energy transfer between any pair of cells without the cumbersome multi-winding transformers employed in existing equalisation converters. The new equalisation scheme uses a bi-directional arrangement of MOSFET switches for galvanostatic isolation allowing the converter to be multiplexed to the stack. This arrangement allows the total size of the equalisation scheme to be reduced whilst maintaining performance.

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Nomenclature

The terms supercapacitor, ultracapacitor and electrochemical-double-layer-capacitor (EDLC) are commonly used interchangeably in both academic literature and technical journalism. Where the context is that of a particular product the author has attempted, where possible, to use the commercial term for that particular product. Elsewhere the term employed usually relates directly to how it is presented in a referenced work or datasheet. For other purposes the terms can generally be considered interchangeable. A Lithium-ion capacitor is a separate technology.

Abbreviations

AC	Alternating current
ADC	Analogue to digital converter
DC	Direct current
CAD	Computer aided design
CMOS	Complementary metal–oxide–semiconductor
EDLC	Electric double-layer capacitor
EIS	Electrochemical impedance spectroscopy
ESR	Equivalent series resistance
EPR	Equivalent parallel resistance
ESS	Energy storage system
ICE	Internal combustion engine
IEEE	Institute of Electrical and Electronic Engineers
Li-ion	Lithium-ion
MEMS	Micro-electro-mechanical systems
MOSFET	Metal oxide surface field effect transistor
MMF	Magneto motive force
MIPS	Mega instructions per second
PV	Photovoltaic
PCB	Printed circuit board
PWM	Pulse width modulation
RC	Resistor-capacitor
SOC	State of charge
SOH	State of health
UPS	Uninterruptable power supply
VA	Voltage-ampere rating

Symbols

A	Area of plate in parallel plate capacitor
C	Capacitance
C_d	Delayed branch capacitance (3 branch model)
C_{diff}	Combination of C_{i0} and C_{i1}
C_{i0}	Immediate branch fixed capacitance (3 branch model)
C_{i1}	Immediate branch variable capacitance (3 branch model)
C_L	Long term branch capacitance (3 branch model)
D	Electric flux
d	Distance between parallel plates
ΔV	Step change in voltage
ΔI	Step change in current
∇	Divergence function
E	Electric field strength
E_c	Energy stored in a capacitor
ϵ	Equalisation efficiency
ε_0	Permittivity of free space
ε_r	Relative permittivity
f_c	Filter corner frequency
I	Current (constant)
$\hat{I}$	Peak current
I_{avg}	Average current
I_{eq}	Equalisation current
i	Current (time variant)
i_{Cn}	Current in capacitor n
j	Imaginary operator
k_V	Coefficient of variable capacitance (2 branch model)
L	Inductance
L_P	Primary winding inductance
L_S	Secondary winding inductance
M	Coupling coefficient
N_P	Number of primary turns
N_S	Number of secondary turns
P	Polarisation
ρ	Surface charge density
ϕ	Phase difference

Q	Charge
R_d	Delayed branch resistance (3 branch model)
R_i	Immediate branch resistance (3 branch model)
R_L	Long term branch resistance (3 branch model)
R_{Leak}	Leakage resistance (3 branch model)
R_S	Switch resistance
R_{ch}	MOSFET channel resistance
S	Reluctance
s	Lapacian operator
t	Time
τ_2	Time constant of second branch (2 branches model)
V	Voltage (constant)
$\hat{V}$	Peak voltage
V_C	Capacitor voltage
V_{Cn}	Voltage of capacitor n in a capacitor stack
V_{Ci}	Coefficient of immediate branch variable capacitance (3-branches model)
V_{Df}	Diode forward voltage
v	Voltage (time variant)
ω	Angular velocity
φ	Depression factor
X_L	Reactance of an inductor
χ	Dielectric material susceptibility
Z	Complex impedance
Z_{CPE}	Impedance of constant phase element
Z_{im}	Imaginary impedance
Z_{re}	Real impedance
Z_{Zarc}	Impedance of a Zarc element
$\|Z\|$	Impedance magnitude
Z_p	Porous electrode impedance

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1 Introduction

This chapter introduces the themes of this work; the technology and history of high capacitance electrical energy storage systems, the applications of such devices, the specific introduction of Lithium-ion capacitor devices, power electronic interaction and the requirements for voltage equalisation.

1.1 Objectives and contribution

The author's work contained in this thesis was carried out as part of an Engineering and Physical Sciences Research Council (EPSRC) funded project. The project (number EP/F06151X) is a UK-China partnership combining the work of seven UK and nine Chinese PhD studentships. The consortium consists of five UK universities with four industrial partners and four of China's key universities, one research institute, and three commercial organisations.

The objectives of the research project as a whole were to research increased reliability in renewable energy generation systems and networks. To that end, this work relates to essential safety and efficiency issues with electrical energy storage and its applicability to renewable generation but also many other applications.

Upon commencement of the project the objectives of this work were as follows;

- Study state of-the-art high capacitance technologies
- Establish safety critical, failure mode, lifetime and efficiency issues
- Develop progressive technology to positively contribute to one or more of the above identified issues

After review of the first two points, the voltage equalisation of high capacitance electrical energy storage systems was considered an area of interest as there was little published work on active converters for the purpose. The objectives of the project were then more closely specified as:

- Establish a family of electrical energy storage systems with a suitable requirement for voltage balancing when assembled into modules
- Study modelling techniques of these devices and establish a suitable modelling process for the study of equalisation schemes
- Carry out a critical review of published equalisation schemes including simulation of performance
- Establish weaknesses, if any, in the existing solutions and propose improvements or an enhanced design specification
- Develop from the above research an improved equalisation scheme and demonstrate its effectiveness

The contributions of this work, which the author believes to be previously unpublished, are as follows;

- Electrochemical impedance analysis of Lithium-ion capacitors (see section 1.3.2 for description of these devices) developed by the company JSR Micro
- Critical comparison between the JSR Micro Li-ion capacitor and a Maxwell carbon electrode double layer ultracapacitor
- Development of modelling technique for Li-ion capacitors which is analogous to a previously published method for traditional ultracapacitors
- Simulation of published equalisation schemes for critical analysis
- A unique method for grouping published equalisation schemes into families either based on constituent parts or energy flow paths – although the latter is a development of work which is referenced within
- A development of energy flow path concepts into power flow paths to demonstrate wasted power overhead in equalisation schemes. This leads to the conclusion that an equalisation scheme can be designed with lowered aggregate power rating but maintained performance
- A new equalisation converter topology based on the ideas developed above designed to reduce wasted overhead in power rating and therefore mass and volume issues, whilst maintaining effective equalisation performance

Whilst this work was undertaken as part of a collaborative project the work contained herein is in no way a repetition or collaboration of other work within the FRENS programme.

1.2 Thesis Overview

Chapter one introduces high capacitance technology; the historical background, applications and general principles of the double layer effect. An introduction into modules of cells and power electronic interface is given. A general overview of design considerations and modelling is shown.

Chapter two describes modelling techniques for high capacitance cells. Initially, a study is undertaken into the supercapacitor devices themselves comprising of a brief overview of the electrochemical processes followed by a review of modelling techniques. A new family of devices, the Li-ion capacitor, is presented. A new method to model this device which is analogous to a modelling method of more traditional devices, identified as a suitable method for modelling power electronic interface, is also developed.

Chapter three is a representative review of published equalisation schemes. Individual description of operation, critique and simulation is made. A method of grouping the existing solutions into families of equalisation schemes is proposed which allows conclusions about

equalisation scheme performance depending on topology types, constituent components and energy flow paths to be generalised. This leads to a specification of a more idealised equalisation scheme based on the advantages and failings of existing schemes.

Chapter four uses the ideas established in chapter three for an improved specification to develop a new equalisation scheme using an entirely new equalisation scheme converter topology which negates some of the failings in existing schemes. The development of the new topology through an understanding of the power flow requirements in an equalisation scheme is shown. Simulation of the proposed system is shown with discussion on control methods and expected efficiencies.

Chapter five outlines the experimental arrangements of the prototype hardware setup. An overview is made of the experimental setup describing the function of each section. The hardware issues and mitigations are described.

In chapter six it is concluded that the proposed system, as constructed, whilst showing significant advantages also shows potential for improvement both in the practical implementation of the prototype and in the control of the system.

1.3 Introduction to capacitance, double layer effects and advances in Li-ion technology

The ability to store energy is a fundamental building block in engineering. As uses for electricity grew throughout the nineteenth and twentieth centuries the facility to store electrical energy became essential. In modern times electrical energy storage is utilised in millions of devices and pieces of equipment and is vital to the running almost every industrialised system.

As applications and demands have evolved the demands and requirements for electrical energy storage systems (ESS) has grown and diversified greatly. Consequently, many families of electrical ESS exist today. These range from tiny batteries which power watches or small medical equipment to very large capacitor banks in electricity distribution systems. The progression of development of the many forms of electrical ESS has led to the growth of multiple, very large, industries to support the technology.

Initially, research centred on the development of electrochemical batteries such as lead-acid technology. The development of new battery chemistry carries on in a multi-billion pound industry as new more challenging demands are made of battery technology.

Electronic double layer capacitors (EDLCs) are commonly known as ultracapacitors, a term which was trademarked by NEC Tokin in 1975 [1], however other terms such as supercapacitors or power capacitors are in common use [2]. Early patents for the EDLC exist for General Electric in 1957 [3] and Standard Oil Company of Ohio (SOHIO) in 1970 [4]. Unlike

the electrochemical battery, which stores energy in chemical bonds that follow redox reactions in which occurs mass transfer, the EDLC effect is purely electrostatic where energy is stored in an electric field. Energy storage for capacitors does not involve mass transfer elevating the wear out failures associated with such reactions. The EDLC effect relates to the utilization of an electrostatic field across the interface boundary between an electron conductor and an ion conductor [1].

Evaluation of the effectiveness of an electrical energy storage technology may be considered in a number of ways. Principally a cost-benefit analysis may be undertaken to establish one technology's performance in comparison to another. In the case of energy storage, the two benefit factors are energy and power. There are a number of cost factors but it may be considered for engineering purposes that the three most important are monetary cost, volume and mass. The economic factors of electrical energy storage systems are beyond the scope of this work and it is noted only notionally that all forms of modern electrical energy storage employ chemicals and minerals which are expensive. A common way to display electrical energy storage devices in terms of cost-benefit is to compare their energy density and power density on a Ragone plot. Electrochemical capacitors have a specific energy (energy stored per kilogram) of around 10Wh/kg and an energy density of approximately 15Wh/L [1]. This is considerably smaller than for example an AA alkaline primary battery which has specific energy of around 120Wh/kg and energy density of around 500Wh/L. However, the advantage of the electrochemical capacitors is in the power density available which can be as high as 100 times that of lead acid batteries and even ten times that of a Lithium-ion battery. A Ragone plot showing various electrochemical specific energy and power is shown in Figure 1-1.

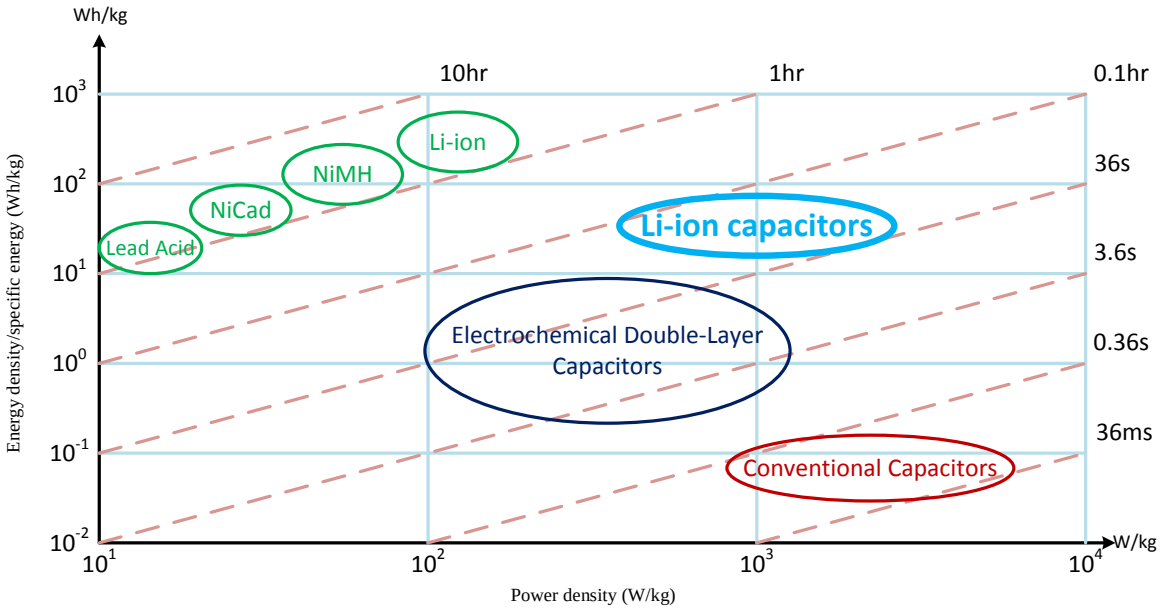

Figure 1-1 - Ragone plot showing power and energy density of various electrical energy storage systems

1.3.1 Capacitance – basic principles

Considering the separation of two bodies with opposing charge, an electric field is understood to exist between them according to Gauss's law. Since a force exists exerting on the two separated bodies, energy must be stored in the arrangement. The amount of energy that may be stored in such a system is governed by the system capacitance.

The Oxford English dictionary defines capacitance as, "The ratio of the change in an electric charge to the corresponding change in potential" [5]. Put mathematically, the capacitance is the constant of proportionality in the relationship between charge and potential, or, where Q denotes charge in Coulombs, C is capacitance in Farads and V is potential in Volts;

$$Q = CV \tag{1.1}$$

Since current is a measure of charge flow per unit time as per (1.2) then for a constant current flow (1.1) may be re-written as (1.3).

$$I = \frac{Q}{t} \tag{1.2}$$

$$V = \frac{I}{C}t \tag{1.3}$$

According to (1.3), given a constant charging current the voltage of the capacitor ramps linearly with time as per Figure 1-2.

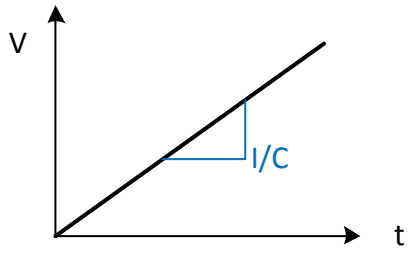

Figure 1-2 - Voltage profile for ideal capacitor

Moreover, since current is defined as the rate of change of charge differentiating (1.1) gives the general expression;

$$i = C\frac{\mathrm{d}v}{\mathrm{d}t} \tag{1.4}$$

Considering the power flow, the energy stored in the capacitor may be calculated through an integral over time of this power;

$$E_C = \int_{-\infty}^{T} vi\,\mathrm{d}t = \int_{-\infty}^{T} v\left(C\frac{\mathrm{d}v}{\mathrm{d}t}\right)\mathrm{d}t = \frac{1}{2}Cv^2(t) \tag{1.5}$$

The capacitance may be derived from knowledge of the surface charge density, ρ (C/m^2), on a conducting plate of area, A, given by

$$Q = \rho \cdot A \tag{1.6}$$

From Maxwell's equations the source, ρ, of an electric field, E, is given as the divergence of the electric flux, D, within the field;

$$\nabla \cdot D = \rho \tag{1.7}$$

For a given dielectric medium, the constitutive relation plus dielectric polarisation define the total electric flux;

$$D = \varepsilon_0 E + P \tag{1.8}$$

where P is the polarisation and is given as

$$P = \varepsilon_r \varepsilon_0 \chi E \tag{1.9}$$

Dielectric material susceptibility, χ, is a measure of the material contribution to total permittivity, ε_r which is the relative permittivity, a function of the material used and ε_0 is the permittivity of free space and has a value 8.85×10^{-12} F/m.

Therefore, considering a system of a parallel plate capacitor, consisting of two conducting parallel plates each with surface area, A, separated at uniform distance, d, by a dielectric of material susceptibility, χ, and given the definition of electric field in (1.10) the capacitance is calculated based on the total surface charge in (1.11) [1].

$$E = \frac{V}{d} \tag{1.10}$$

$$C = \frac{\varepsilon A}{d} = \frac{(\varepsilon_0 + \varepsilon_0 \chi) A}{d} = \frac{A \varepsilon_r \varepsilon_0}{d} \tag{1.11}$$

Relative permittivity, ε_r, accounts for the presence of material (i.e. non-vacuous) in the dielectric and is given as

$$\varepsilon_r = (1 + \chi)\varepsilon_0 = k\varepsilon_0 \tag{1.12}$$

Hence the K-factor represents polarisation of the dielectric material.

The effect of a non-vacuous dielectric is to introduce nonlinearity into the state equation, (1.1). For example in ceramic type dielectrics, dielectric saturation results in lowered capacitance at higher voltage. Saturation of the dielectric results in the total energy storage availability is lower than for an ideal, linear capacitor.

Physically EDLCs use a structure much like that of an electrochemical battery; utilizing two electrodes which are immersed in or impregnated with an electrolyte. The energy storage occurs where positive and negative ionic charges within the electrolyte accumulate at the boundary between the electrolyte and the electrode (on the solid surface of the electrode) compensating for an imposed electronic charge (via an external circuit) at the electrode surface [2].

As described in (1.5) energy is stored when a potential is applied allowing polarised charge accumulation. As electrons flow from the supply negative terminal into the negative electrode of the EDLC an ionic layer is created between the electrode and the electrolyte. As with parallel plate capacitors the negative charge build up repels electrons from the positive electrode and electrolyte. In reality the actual depth of the ionic layers (two layers, one on each electrode, hence the double layer effect) depends on carrier concentration in the electrolyte and the physical size of the ionic bodies.

The EDLC has a relationship with the capacitance state equation (1.1) where capacitance increases nonlinearly with potential [1].

The actual effects of increasing potential along with temperature variation and charging current variation are extremely complex to describe and are beyond the scope of this work. Whilst the sources of this behaviour are not pursued, the effects must be modelled accurately to understand the behaviour of the devices when interacting with power electronic converters. This work is discussed in more depth in chapter 2.

1.3.2 Li-ion capacitor introduction

In 2008 JSR Micro, a materials and chemicals company, completed construction of the world's first commercial production plant for Lithium-capacitors. JM Energy, a subsidiary of JSR Micro is the commercial manufacturer and distributor of these Li-ion cells. Since 2009 the family of cells has grown and at the time of writing includes 1100F and 2200F pouch cells and 2300F and 3300F prismatic cells [6].

1.4 Applications of high capacitance devices

High capacitance cells may be used wherever high power delivery or electrical storage is required. This section outlines a small number of typical applications.

- Transport

The dynamic response requirements in many transport applications are ideal for supercapacitor usage.

Large internal combustion engines are currently started using the vehicle battery. The vehicle's battery is often oversized to accommodate this high power load. It also takes longer to recharge a battery due to higher internal resistance. Cold climates can also have a negative effect on battery performance. Therefore to provide power to the starter motor supercapacitors are considered an excellent alternative to large lead acid batteries [7, 8].

Supercapacitor technology is an excellent candidate for hybrid drivetrains (either using internal combustion engine or fuel cell power plants) in electric cars as they can provide the high dynamic response required for good acceleration and regenerative braking [9-14].

Applications for heavy transport include cranes [15], shuttle, hybrid and fully electric busses [16-19], earth moving equipment[20] and DC traction applications [21-23].

- Renewable generation

Many renewable sources of energy are characterised by their transient nature; such as wind and solar generation. The variations in source energy and load demand cause shortfalls and surpluses in energy. Therefore, intermediate energy storage, capable of fast transients to match the energy source, is required and is an ideal application for supercapacitors.

Supercapacitors can be used, either stand-alone or in hybrid with other energy storage systems, to control the power quality of PV array generation plants [24, 25] or wind generation [26-28] and are usually connected via DC/DC converter to the DC link to stabilise generator output. There are also applications for direct integration with the grid-side converter [29, 30].

Microgrids or remote communities often have small renewable generation plants which can be supplemented by intermediate energy storage to improve performance [31-34].

- Micro-grid

Micro-grids are proposed in a number of different forms however many contain the requirement for some form of energy storage.

Micro-grids with distributed generation can utilise energy storage for power quality during load transients [35, 36].

- Distribution

Good low voltage ride through capability is an important quality for distribution applications as well as distributed generation. Supercapacitors have been proposed as energy storage media to provide the injected current to withstand fast grid voltage drop-out [37-39].

Voltage sag compensation for sensitive loads using supercapacitor energy storage systems can be used to reduce outages caused by periodic dips in grid voltage [40].

- Other applications

Supercapacitors have been proposed as energy storage on far smaller scales such as in bio-medical devices which harvest energy from MEMS piezoelectric generators [41].

Short term UPS applications which can withstand several hundred microsecond energy surges – as defined in IEEE C62-41 series – have been proposed using topologies incorporating supercapacitors and energy circulation techniques [42].

Wireless sensor modules have high peak power demands but very low base load which make supercapacitors a preferable energy source to batteries because of the relative power densities [43, 44].

Supercapacitors can be used in drive applications for peak load ride-though helping to alleviate stress on the DC-link capacitor and grid-side converter [45, 46].

1.5 Multiple cell assemblies

The limited cell voltage of supercapacitor technologies, typically around 2 to 3 volts, requires that to attain a system level, perhaps 600V in a modern electric vehicle, voltage a series string of cells must be connected. As with traditional battery technology, manufacturing discrepancies in individual supercapacitor cells leads to capacitance variations [47]. This becomes important when considering that for a simple bank of supercapacitor cells connected in series, variations in capacitance will result in varying cell voltages which could lead to an overvoltage condition on one cell even if the bank terminal voltage is below rated voltage. Considering Figure 1-3, a system of series connected supercapacitors where $C_2<C_1<C_3$ it is clear that for a constant current, I, the voltage will rise more quickly on the lower capacitance cells (C_2 and C_1) than the higher capacitance cell (C_3).

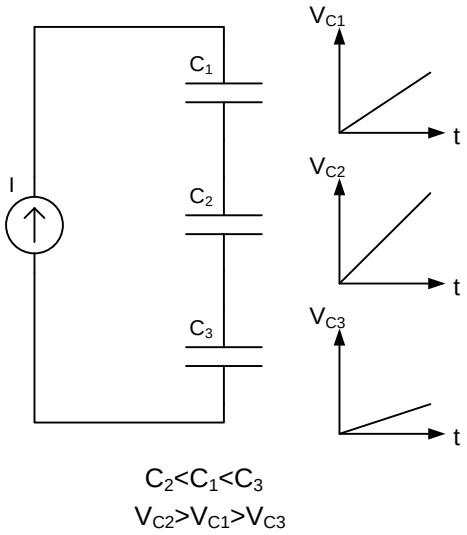

Figure 1-3 - Constant current charging of three unequal capacitances

Exceeding the maximum voltage on a supercapacitor cell can result in dangerous failure of the cells. Therefore a system must be in place to monitor cell voltages and cease charging when cells attain the rated voltage. For supercapacitor systems with varying cell capacities it is clear that charging must stop when any one of the cells reaches its rated voltage. This will result in some of the cells not being fully charged and hence not being fully utilised. For example, if there is a 20% difference in capacitance between a pair of supercapacitor cells (C_1 = 1000F and C_2 = 800F) then for a situation where charging is halted when C_1 reaches maximum voltage C_2 will not be fully charged. Table 1-1 shows the possible energy storage for a situation where the capacitors are firstly, unbalanced and secondly, balanced, it shows there is a 20% increase in stored energy as a result of voltage balancing [48].

Table 1-1 - Comparison of possible energy storage for a pair of supercapacitor cells. C_1 = 1000F, C_2 = 800F [48]

	Unbalanced cells	Balanced cells
Vc_1	2.5V	2.5V
Vc_2	2V	2.5V
Bank Voltage	4.5V	5V
Total energy stored	4500J	5623J

As discussed above, to ensure voltage ratings are not exceeded the cell voltage must be monitored on safety grounds, however, the above energy storage analysis makes a clear case for the addition of voltage balancing which would also increase efficiency.

There are a number of equalisation schemes presented in literature; some have active components and computation whilst others are passive.

Simple equalisation schemes do not employ active devices in order to attain a balanced cell voltage. These clearly have the advantage of being far less complicated schemes to implement but generally have poor global efficiency.

Active balancing systems use techniques which monitor, either directly or indirectly, cell voltage and operate active devices to reallocate energy or redistribute charge flow. There are a number of variations of active balancing systems presented in published literature ranging from simple switched versions of the passive circuits to complex converter topologies and control schemes. Some systems are derived from battery cell balancing technologies however these must be adapted for the smaller time constants associated with supercapacitors [48].

1.6 Voltage equalisation – definition of techniques

Methods of voltage equalisation of series connected stacks vary. For the purposes of this work equalisation schemes, at macro level, are split into two techniques. These are termed *dissipative* and *non-dissipative.* The dissipative equalisation schemes operate by reducing the voltage of a cell which has a higher voltage than other cells in the stack – usually though a resistor; there is no form of energy transfer between the cells within the stack. Non-dissipative schemes aim to align the cell voltages by passing energy between cells in the stack. Since the conversion process is never 100% efficient the equalisation scheme is not truly non-dissipative however the term in this case refers to the method by which the voltages are equalised. Since, for many applications, the dissipative schemes are too inefficient – and require little investigation nor have much scope for improvement – the emphasis in this work is on non-dissipative equalisation schemes.

1.7 Power electronic converters for supercapacitor applications

As has been described in section 1.4, many of the applications of high capacitance energy storage require the combination of the storage elements with some form of power electronic-based energy conversion. On a macro scale this is usually the linking energy storage subsystem to another part of the application such as to the DC-link of a drive or directly to the grid via a voltage source inverter.

Internally to the energy storage system, the use of power electronic converters for both battery and electrochemical capacitor equalisation schemes is already a moderately well discussed topic in literature [48-56]. The advantages over simple discharging circuits in terms of efficiency and speed are clear however the disadvantages are in component cost and physical size of the power converter.

In principle, a single power electronic converter can be designed to deliver a wide range of power flows. However, the specific circumstances around the voltage equalisation of single cells, namely the requirements for galvanic isolation and the relatively low individual cell voltage, lead to limitations in what can be delivered by a particular equalisation scheme. The limitations of the energy delivery are individual to the topologies and are discussed at length.

A great advantage of power electronic converters is the breadth of controllability which is allowed by running the converter in conjunction with a microprocessor, which are becoming less and less costly. The computational power of these devices allows more complex control algorithms to be used which can improve performance.

With modern CAD software it is also possible to simulate the performance of a power electronic converter with a great degree of accuracy, including the control algorithms. This process allows simpler fine tuning of the system.

1.8 Design considerations for active electronic systems in floating reference applications

Operating power electronic converters within a floating reference application is not unique to high capacitance energy storage – it is applicable to voltage source inverters for example. However, the number of floating reference points is far greater than is usually encountered in most applications. There are, therefore, a number of considerations which impose constraints on the design process. These, and their mitigations, are discussed more thoroughly in chapter 5 but principally consist of the requirement for;

- Isolated, centralised control processor
- Isolated control signals
- Isolating control power supplies

- Differential voltage measurement with high common mode voltage

1.9 Modelling single cells

Measurement and modelling of cells is an important part of understanding the interaction between the energy storage medium and the power electronic converter. To that end, there is much work published on measurement and modelling of high capacitance cells (discussed in more depth in chapter 2).

The correct measurement and modelling technique to use is always dependant on the application and what the model is required to tell the user about the cell. There are various techniques for both measuring and modelling single cells. Common measuring techniques are static and load profile monitoring, step change and electrochemical impedance spectroscopy (EIS).

2 Cell measurement and modelling

This chapter describes methods for modelling electrochemical energy storage devices with analysis of a range of methods. A measurement and modelling technique is demonstrated for Maxwell 2700F EDLC capacitors and JM Energy 2200F Li-ion capacitors.

Although most EDLC devices are supplied with datasheet information on nominal capacitance, series resistance and temperature effects these parameters are simplifications of the EDLC system. The behaviour of the devices is more complicated than a simple table of nominal data would suggest. The dependence of device characteristics on both internal and external factors such as cell voltage and temperature mean that under dynamic influence the cells behave in a more complicated manner.

Cell measurement is therefore a more complicated process and characterisation of the device must go beyond the simple information of the datasheet for any in-depth understanding of the device interaction. Development of models to demonstrate the characterisation of the devices is an essential tool predicting and simulating the effects of external influences on the device and in the development of any application which uses them.

This chapter is structured firstly as a literature review of methods of characterisation of supercapacitors. Following the literature review new work is carried out; a suitable characterisation method for this work is identified and the Maxwell cells are characterised using this measuring method. The models generated are tested against real load profile measurements and compared. The characterisation method is modified to allow characterisation of the JM energy Li-ion capacitors and the model generation and testing procedure is repeated for these cells.

2.1 Descriptions of sample cells

During the undertaking of this work a new technology, Lithium-ion capacitors, became available on the general market. As work characterising a standard EDLC technology was already undertaken the new Li-ion capacitor technology was also explored and compared to the traditional EDLC cell. The two cell types made available to the author were standard EDLC architecture in mass production (Maxwell PC2500, 2700F ultracpacitor) and a new asymmetric Li-ion capacitor developed by JM Energy. Measurements were made and averaged for the three examples of each technology which were available at the time of experimentation.

2.1.1 Maxwell PC2500, 2700F ultracapacitor

A symmetric capacitor is defined as a cell where both electrodes, in this case carbon-carbon, of the capacitor are fabricated identically. The Maxwell capacitor behaves in a way similar to the processes described in section 1.3.

The datasheet data supplied by the manufacturer for this cell is shown in Table 2-1.

Table 2-1 - Datasheet information for Maxwell PC2500 ultracapacitor

	Value	Tolerance	Standard
Mounting	Bus bar		
Capacitance [F]	2700	±20%	
Voltage [V]	2.7		
Internal resistance DC [Ω]	0.001	±25%	
Internal resistance 1kHz [Ω]	0.00055	±25%	
Rated current [A]	625		
Leakage current [mA]	5		
Operating temperature range [°C]	-40 to 65		
Storage temperature range [°C]	-40 to 85		
Capacitance endurance [F]	< 20% decrease		1000hrs, 2.5V at 70°C
Resistance endurance [Ω]	<40% increase		1000hrs, 2.5V at 70°C
Energy density [Wh/kg]	3.8		
Energy density [Wh/l]	4.5		
Power density [W/kg]	1030		
Power density [W/l]	1250		

The Maxwell PC2500 is packaged in an aluminium can, a photograph of the packaging is shown in Figure 2-1.

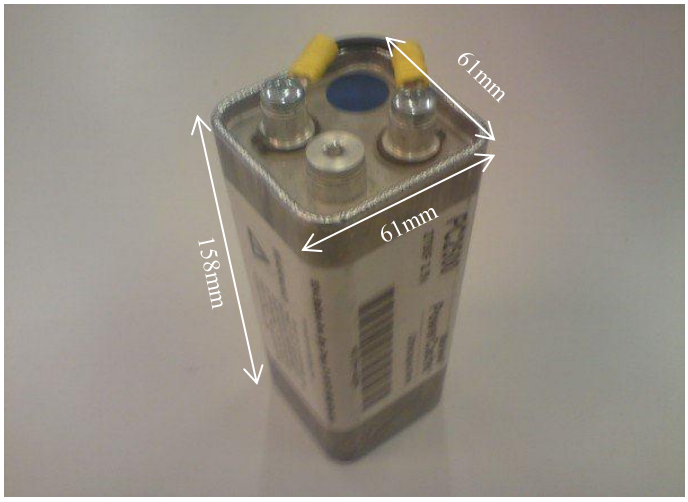

Figure 2-1 - Can packaging of Maxwell PC2500 ultracapacitor

2.1.2 JS Micro 2200F Lithium-ion capacitor

Whilst the traditional EDLC capacitor follows the symmetric architecture described in 2.1.1 it is possible to hybridise the technology whereby one electrode is a battery-like, ideally non-polarisable electrode, such as a metal oxide, that is paired with a carbon electrode double layer electrode. For the case of a Li-ion capacitor, which may be termed a hybrid capacitor, the approach is to pre-dope the graphite negative electrode with lithium so that a ready source of Li^+ ions is available and to construct an opposing electrode of activated carbon to act as the double layer capacitor. The lithium pre-doping biases the positive, EDLC, electrode by several volts where after it still acts as a conventional capacitance with the exception of the calculated energy storage. The voltage bias increases the stored energy as the energy is proportional the square of the capacitor voltage as given in (1.5). A typical symmetric EDLC with several thousand farads capacitance stores 3.2 times less energy than a hybrid capacitor of the same capacity [1].

The JS micro 2200F Li-ion capacitor datasheet data is shown in Table 2-2.

Table 2-2 - Datasheet information for JM Energy 2200F capacitor [6]

	Value	Tolerance	Standard
Capacitance [F]	2200	±10%	
Voltage [V]	2.2 – 3.8		
Internal resistance DC [Ω]	0.0023	±15%	
Internal resistance 1kHz [Ω]	0.0014	±20%	
Rated current [A]	250		
Operating temperature range [°C]	-20 to 70		
Temperature dependence on capacitance (-20°C) [F]	1700	±18%	
Temperature dependence on capacitance (70°C) [F]	2300	±10%	
Cycle performance – capacitance [F]	2000	±15%	100C at 25°C, 100k cycles
Self-discharge voltage drop [%]	<1%/ 5%		24h/3months at 25°C
Energy density [Wh/kg]	14		
Energy density [Wh/l]	25		
Power density [W/kg]	750		
Power density [W/l]	3333		

The lithium-ion capacitor packaging is pouched; a photograph of the test cell is shown in Figure 2-2.

Figure 2-2 - Pouch cell packaging of JS micro Li-ion capacitor

2.2 Introduction to modelling electrical energy storage

Most physical systems may be considered as a data flow consisting of an input, a process and an output. A time dependant signal, $x(t)$, can be applied to the system as an input then a time dependant signal, $y(t)$, may be observed as the system output. Given the system input, or stimulation, the system response is observed as depicted in Figure 2-3.

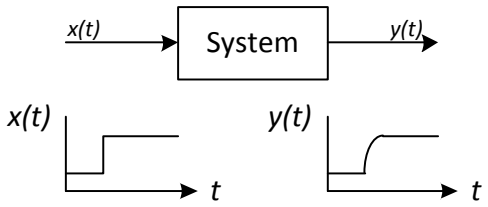

Figure 2-3 - A dynamic system response $y(t)$ to input stimulus $x(t)$

A dynamic system's behaviour may be described by a set of governing equations:

$$y(t) = f[y(t), x(t)] \tag{2.1}$$

In the case of non-linear systems the equation set, equation (2.1) will be non-linear also.

An electrochemical storage device may easily be considered as a system, moreover a non-linear system since the complex electrical, chemical, mechanical and thermal interactions present a intricate system with many dependencies. For an electrical energy storage system, (ESS), it is common to define the current and cell temperature as scalar inputs. Outputs may include terminal voltage, state of charge (SOC), state of health (SOH) or many others [57]. The outputs are effectively functions of the current states of the ESS and the input perturbation. It may be considered that for the case of an electrochemical cell, the cell voltage and temperature is a function the cell current and temperature which can be described as a differential equation set of the form

$$\begin{bmatrix} v(t) \\ \tau(t) \end{bmatrix} = f[i(t), \tau(t)] \tag{2.2}$$

where $v(t)$ is the terminal voltage, $\tau(t)$ is the cell temperature and $i(t)$ is the cell current.

There are many variations of (2.2) depending on the desired level of complexity and output parameters.

As the system response can be characterised through mathematical expressions such as (2.1) then models can be derived to predict dynamic response to given input criteria. In terms of a model which describes the behaviour of an electrochemical power source a number of modelling techniques for the process may be used.

Characterisation of cells often leads to behavioural models. Many models exist for predicting various aspects of cell status and are widely used in simulation of systems incorporating ESS technology for predicting response to system behaviour. Models are also embedded into systems in the field to aid the general overseer of the system to make judgements on cell status in real time. If a model's parameters can be discovered through direct measurement of the cell then quantitative conclusions may be drawn and model parameters extracted.

Electrochemical cell modelling is a very well discussed topic in published literature. The motivations for development of a model to describe the cell behaviours are numerous and are motivated from a broad range of application requirements. The most appropriate performance measure is, as is often the case, dependant on the application of the energy storage system and which of its attributes are required to be described.

Broadly, there are two directions from which motivation to develop a modelling technique may arise; the first is that in development of the technology utilised to create the storage system an understanding of how the physical construction, dimensions and chemistry behaves is useful. A model which has the physical properties of the cell assembly as input parameters can be used to predict effects of altering some aspect of its production or manufacture from which the developer may make conclusions on future development of the technology. Most fundamentally the cell may be described by the series of chemical reactions which are designed to occur within. A series of equations may be developed to describe the chemical processes occurring within the cell from first principles. These equations describe the physical interactions occurring at molecular level within the cell and ultimately the electrochemical state of the cell. These interactions are however very difficult or impossible to directly observe with any accuracy without direct access to the cell. The special nature of the required differential equations also makes migration of models between different devices difficult as the expressions will be specific to the dimensions and chemistry of a single device. Models which are derived in this way are referred to in this work as physical models.

The second motivation is that in order to utilise the energy storage device within a system its behaviour under external influences must be understood. From this perspective the underlying physical makeup of the device is not necessarily important and in reality generation of behavioural models does not automatically require any knowledge of the specific cell makeup – although many behavioural models are developed from a general, macro understanding of the operational principals. This style of models are referred to in this work as characterised models.

When describing the EDLC as an energy storage system (ESS) the important features are energy and power densities (absolute values are often subject to large tolerances). In this measure the dominant parameter is the series resistance (ESR). When describing the EDLC as a circuit feature it is required that its response in relation to both steady state and dynamic performance is evaluated. The weighting of the importance of either is determined by the specific application at hand. Hence datasheet information is not always sufficient to develop models for power electronic systems simulation.

The purposes of this work requires an understanding of the behaviour of the cells interacting with a power electronic system and as such attention has been focused on characterised models rather than models concerned with the underlying electrochemical interactions.

In terms of characterised models there are essentially two methods to develop an electrochemical ESS model; firstly as an energy storage component whereby the ESS is described as a deposit of potential energy analogous to a power source. The second method is to describe the ESS purely in terms of its response to electrical inputs – i.e. as an electrical impedance. Both methods result in models of varying structure which range from equivalent circuit models, transfer functions or behavioural differential equations.

Development of a model to predict the behaviour of devices interacting with power electronic systems has some specific requirements. Clearly the cell will be operating over the whole range of its energy storage capacity thus any variation in behaviour as a function of energy stored, usually defined as voltage dependence, is important. Using a power electronic system it is possible to alter the magnitude and rate of change of the electric parameters – the current in the case of the EDLC – therefore the bandwidth of the model is important and should be related to the application.

It is common to use computer simulations of power electronic systems to predict and tune the behaviour of the system prior to construction. In order to integrate the model of the ESS into such simulations the model of the ESS clearly must be compatible with the power electronic model simulations. There are many methods for integrating a system model into an electrical circuit model however the most common is to use an equivalent circuit approach. Whilst the motivation, accuracy and applicability surrounding the various ESS modelling

methods vary widely, most modelling techniques ultimately are derivations of, or from, an equivalent circuit.

Fundamentally a model is simply a means by which to describe the behaviour of a system and therefore the range of models are merely differing methods of describing the same effects with varying purposes as motivation. Attempting to ascertain the advantages and disadvantages of every method published is neither practical nor particularly relevant to this work.

Therefore, the remainder of this chapter details a number of modelling methods representative of a wide range of published literature in an attempt to identify a suitable modelling technique for this work. This is based on the requirement for the model to be

- Suitable for simulation with models for power electronic converters
- Descriptive of cell behaviour over temperature and state of charge ranges
- Have a high bandwidth

2.3 Review of modelling techniques

As described in the previous section behavioural models can broadly be grouped into sub methodologies driven from different motivations. Therefore this section explores a small number of published modelling techniques which are representative of different methodologies in ESS modelling.

2.3.1 Representation of double layer capacitance effect

An understanding of the double layer capacitance has been used in the development of multiple modelling methods to represent its electrical behaviour using RC ladder arrays as an equivalent electrical circuit.

Using first principals the equivalent circuit of the EDLC can be treated as an infinite branch transmission line with voltage dependant distributed capacitance [58]. The transmission line model (shown in figure 2-4) approximates the behaviour of each branch to have a discrete time constant dependant on pore size, resistance of the electrode and apparent resistance of the electrolyte and physical connections [2, 59].

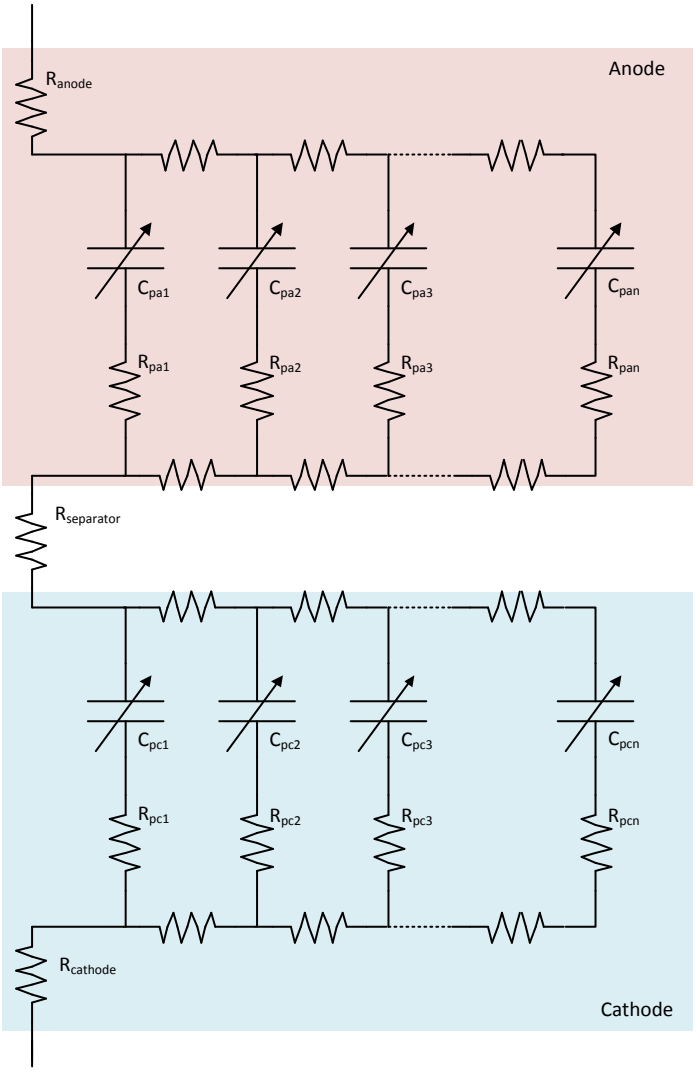

Figure 2-4 - Theoretical Model of an EDLC [2]

The physical basis for the model can be represented as in Figure 2-5 to show the electrical effect of the porous electrode. If the ionic charge is assumed to move from the bulk electrolyte material in effect up the pores and their mobility is not high (in relation to the cycle period) then the duration of any charging current effects how far up the pore the ion travels. In essence, for high frequency dynamic charging the ionic charge never travels the depth of the pore. Low frequency or sustained charging reveals a more distributed pattern of ion location [2]. The effective surface area of the electrode is a function of how far the ionic charge is able to travel and hence a shorter effective pore depth gives a smaller available surface area which in turn affects the capacitance as per (1.11). In Figure 2-5 this behaviour is modelled as a series RC transmission line with each branch having increasing time constant with pore depth. The transmission line is assumed to have infinite branches representing the behaviour across infinite frequency.

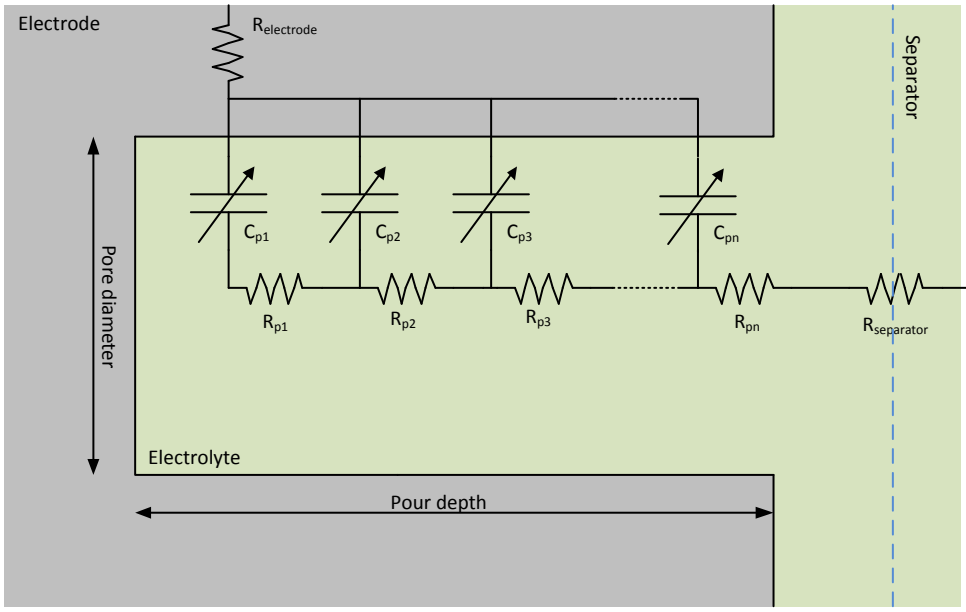

Figure 2-5 - Equivalent Circuit Representation of distributed resistance and capacitance within a pore with a 5 element transmission line [2]

Whilst this distributed parameter model may be considered a close match of the physics of a double layer capacitance it is of little practical use; there are a large number of complex parameters which are very difficult and time consuming (if not impossible) to calculate from experimental results [59, 60].

There have therefore been numerous attempts to simplify this model in order to most accurately describe the response of an EDLC with the simplest to parameterise, least computationally expensive model [58-63].

Simplification of the ideal model (Figure 2-4) to an infinite RC transmission line with series inductance is not an unreasonable assumption since it essentially lumps the two transmission lines associated with the two electrodes and the series resistances together and includes the effect of current collector (measurement probe) and wiring parasitic at high frequency. The transmission line model is widely used as the basis for more simplified models.

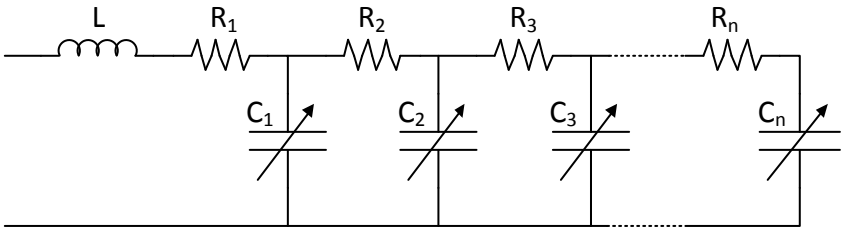

Figure 2-6 - RC Transmission Line EDLC Model

Experimental results [2, 58]show the voltage dependency of the capacitance which is modelled as variable capacitances in Figure 2-6. To further simplify the model this variability is sometimes disregarded and/or the number of branches is limited which effectively limits the

bandwidth of the model. The simplification process is largely application specific but clearly the transmission line model is still very complex to simulate and defining the individual parameters is still a difficult process.

Lumping the parameters into a generic transmission line block with R and C elements giving an effect of the combined response of the network is discussed in [63] and effectively changes the order of the model – varying from a 6^{th} order system to a 2^{nd} in the example given – depending on the time-base resolution of the results required. This method therefore tailors the model to the needs of the simulation being run but the individual parameters to the maximum order accuracy are required and thus this process cannot reduce the complexity of the parameter extraction process.

Where it is used there are often various additions to the ladder model such as relaxation effects or parallel resistance simulating self-discharge effects.

2.3.2 Modelling cells as an energy storage component

In terms of energy storage or constant current charging, or discharging, the ladder circuit can be considered as a series of charge re-distribution events where the time constant of each RC branch is distinct and, depending on the model, quite diverse.

For long term energy storage modelling this style of model can reproduce the effect of charge redistribution and voltage dependence of the capacitance more easily [64]. The usefulness of such models is debatable since long term storage effects of EDLCs are generally of less concern than they would be for batteries as the applications for EDLCs tend to have faster time constants [61].

At its simplest the ladder model becomes a single RC pair representing the device capacitance (C) and perceived electrolyte resistance, equivalent series resistance (ESR), as well as a parallel self-discharge resistance (EPR). The parameters of this classical model are easily obtainable from standard laboratory equipment such as an oscilloscope [60], however, the model lacks the ability to characterise the terminal behaviour in a wide range of frequencies [61].

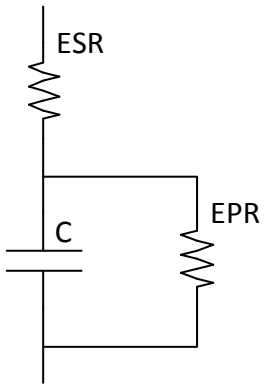

Figure 2-7 - Classical EDLC Model

The simplest way of calculating series resistance for this model is to measure the instantaneous response to constant current charge. It is assumed that the initial conditions are zero stored charge – in practice it can be difficult to completely achieve this without conditioning or prolonged terminal shorting. At t = 0 all the voltage is assumed dropped across the series internal resistance (EPR effectively shorted by the zero voltage on the capacitor). The step voltage at this point can be divided by the current to produce a value for ESR (2.3).

$$ESR = \frac{\Delta V}{\Delta I} \tag{2.3}$$

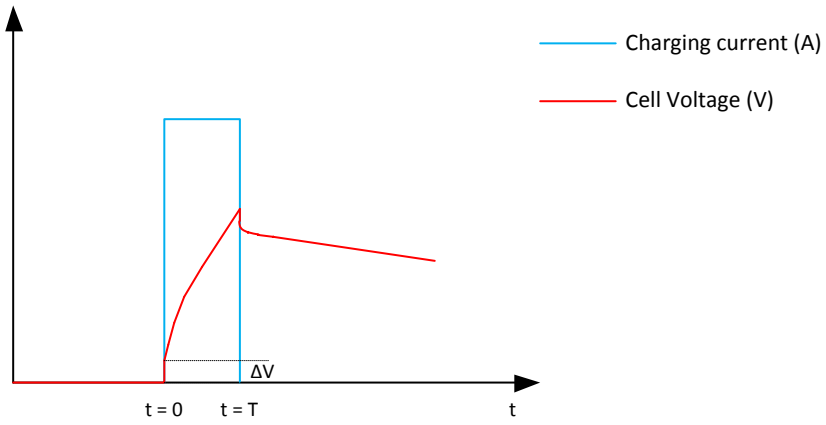

Figure 2-8 - Voltage response to constant current charge

More detailed analysis in [60] uses a precision switching circuit with shunt resistance for accurately measuring charge current and terminal voltage although the principal is the same.

The equivalent parallel resistance (EPR) models the long term self-discharge effect observed in EDLCs. Derivation of EPR is common to most models where it appears and concerns measurement of terminal voltage over a long period. Since the effect is still generally small even over long periods it is usually sufficient to assume the capacitance as the rated value and therefore using (2.5) derived by substituting EPR for R in (2.4) .

$$V_2 = V_1 e^{-t/RC} \tag{2.4}$$

$$EPR = R = \frac{-t}{ln\left[\frac{V_2}{V_1}\right] C} \tag{2.5}$$

In [60] it is assumed that meaningful measurements can be obtained over a period of 3 hours.

This model has two major flaws in that it describes neither the frequency nor voltage dependence on capacitance and resistance and thus the retrieved parameters are only relevant to the conditions in which they were derived – constant current charge. It is far more likely that the demanded or supplied current is a function of the load which is likely to be highly transient.

In order to achieve more accurate results a parallel branch model with three branches is proposed in [64]. The main factors in the design of this model are its ability to model behaviour over 30 minutes. In order to achieve this, the three branches are designed to have three distinct time constants representing the phenomena of ionic charge redistribution after a charging event has ceased. The issue of voltage dependence is also addressed. However, to simplify the extraction of the parameters it is only applied to the first branch.

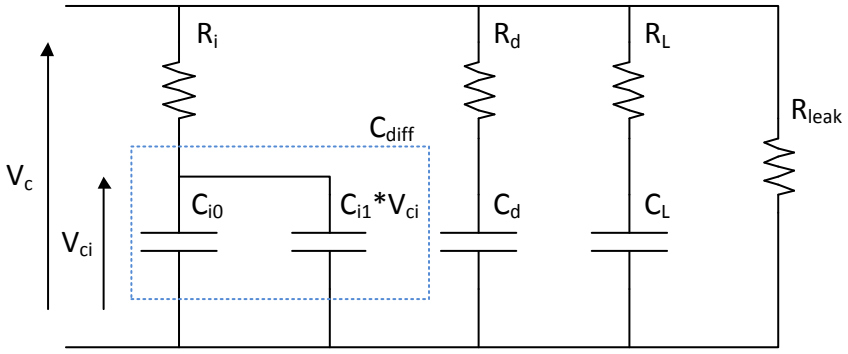

Figure 2-9 - 3 Branches EDLC Model

The non-linearity of the capacitance in the first branch rescinds the validity of (1.1). Therefore the relationship between incremental increases charge stored does not represent a constant increment in voltage. Instead a differential must be considered where an incremental increase in charge, dQ, is related to an incremental increase in voltage, dV for a given voltage level, V' in such a way that satisfies (2.6) .

$$C_{diff}(V) = \frac{dQ}{dV}\Big|_{V'} \tag{2.6}$$

The voltage dependence on the capacitance has been approximated with good accuracy to have a linear relationship [59, 64].The parallel capacitances in the first branch, C_{i0} and $C_{i1}V_{Ci}$, represent the non-zero capacitance at zero volts and the linearly dependant component which are summed together to create the total dependence effect. This gives a value for the capacitance of the first branch as a function of voltage in terms of the model parameters (2.7) .

$$C_{diff} = C_{i0} + VC_{i1} \tag{2.7}$$

The parameter extraction process in the three branch model requires the assumption that only the immediate branch is active during a constant current charge. The stored charge then re-distributes itself firstly to the delayed branch (R_D-C_D) in two distinctive and separate time periods and then to the long term branch (R_L-C_L) modelling the effect of charge relaxation. The time constants for the other branches are chosen to follow experimental data.

The three branch model's description of redistributed charge through two distinctive time constant capacitor charges may as well be simplified to a single redistribution event with a time constant representative of measured results thus the model is simplified in [59] to a two branch model.

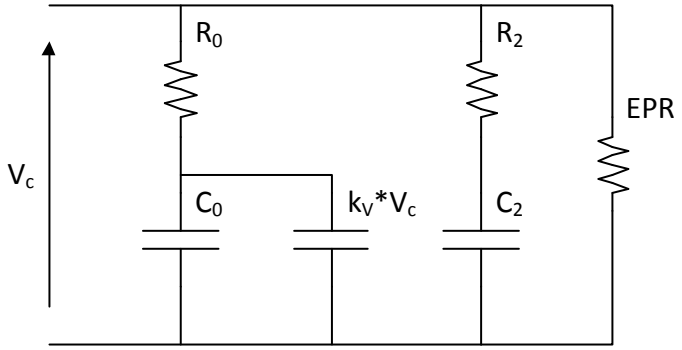

Figure 2-10 - 2 Branch Model

The two branch model shown in Figure 2-10 assumes that the majority of the energy storage is in the first branch and that the second branch has no effect during constant current charging. R_0 is defined in the same way as for the classical model using the initial voltage drop on the charging characteristics.

The charging current under these conditions is given by (2.8).

$$i = (C_0 + k_V \cdot v_c)\frac{dv_c}{dt} \tag{2.8}$$

where $k_V \cdot v_c$ is a voltage dependant capacitance. Integrating (2.8) over the charging time for a constant charge current and separating the variables yields (2.9)

$$t = f(V) = \frac{C_0}{I_C} \cdot V + \frac{1}{2} \cdot \frac{k_V}{I_C} \cdot V^2 \tag{2.9}$$

(2.9) is a polynomial equation in V (zero order coefficient = 0 because initial time t = 0). If constants are defined as in (2.10) then (2.9) may be rewritten as (2.11) .

$$\begin{aligned} C_0 &= c_1 \cdot I_1 \\ k_V &= 2 \cdot c_2 \cdot I_c \end{aligned} \tag{2.10}$$

$$t = c_2 \cdot V^2 + c_1 \cdot V \tag{2.11}$$

Since I_c is imposed (constant current charge) defining c_1 and c_2 is enough to find the model parameters. The voltage on the capacitor can be calculated by subtracting the voltage across the resistor R_0 from the terminal voltage. V_{R0} is always constant since there is constant current charge and R_0 is assumed to be totally ohmic.

Subtracting V_{R0} from the terminal voltage-time curve and taking two arbitrary points (but chosen to cover as much of the charging phase as possible) yields four measures; $P_1(t_1, V_1)$ and $P_2(t_2, V_2)$. From (2.11) it must be true that

$$\begin{cases} t_1 = c_2 \cdot V_1^2 + c_1 \cdot V_1 \\ t_2 = c_2 \cdot V_2^2 + c_1 \cdot V_2 \end{cases} \tag{2.12}$$

Solving (2.12) as a pair of simultaneous equations and substituting solutions for c_1 and c_2 into (2.10) gives expressions for C_0 and k_V in (2.13)

$$\begin{cases} C_0 = \left[\dfrac{t_1}{V_1} - \dfrac{V_1 \cdot t_2 - t_1 \cdot V_2}{V_2^2 - V_1 \cdot V_2}\right] \cdot I_C \\ k_V = 2 \cdot \left[\dfrac{V_1 \cdot t_2 - t_1 \cdot V_2}{V_1 \cdot V_2^2 - V_1^2 \cdot V_2}\right] \cdot I_C \end{cases} \tag{2.13}$$

In order to evaluate the values of the parameters in the second branch a time constant, τ_2, must be chosen. Time constants which are too small would lead to errors in the long term and time constants which are too long would not represent shorter term effects. Once the time constant is chosen (this will depend on the size of the cell and its relaxation characteristics) the voltage is measured at a time three times τ_2 after charging has ceased.

Since the total charge injected into the EDLC is known ($\int_{t=0}^{t=T} I_C dt$) and under the assumption that after three times τ_2 has passed there is no more charge redistribution and all capacitors are at the same voltage and the total charge can be assessed as (2.14) [59].

$$Q_{total} = I_C \cdot T = C_2 \cdot V_{3\tau} + \left(C_0 + \frac{k_V}{2} \cdot V_{3\tau}\right) \cdot V_{3\tau} \tag{2.14}$$

and the resistance R_2 from the time constant equation

$$R_2 = \frac{\tau_2}{C_2} \tag{2.15}$$

This approach does model both voltage and time (up to a few minutes) effects on the model parameters and it is extremely simple to get the parameter models from the most basic equipment. The model does, however, only remain representative for constant current charging and, as is the case with the three branch model, does not have a wide bandwidth representation of cell response. Indeed, for both of these models under short transients the second and third (where it exists) branches are not considered which effectively reduces these models back to the classical circuit model with added voltage dependence. Equally it is debatable whether the behaviour due to the third branch is actually more of a self-discharge process that cannot be identified by the simple parallel resistance in the given time frame.

These reduced branch models are simple and easy to use in the laboratory and do not require expensive equipment or complicated experimentation. They are clearly ideally suited to simple modelling of a small range of inputs – i.e. constant current charging.

2.3.3 Modelling cells as a complex impedance

The majority of applications for EDLC energy storage systems operate with cycles in the range of seconds [61]. The two and three branch models operate under the assumption that a branch's time constant, which is distinct from the other branches', is operating to produce independent effects and principally that only one branch is responsible for the response under conditions where current flow is not zero and that current flow has only two states; off and on. Different applications for electrochemical ESSs have a wide variation in charging current magnitude and frequency. Indeed, within a single application the variance in charging behaviour can be large – in the driving cycle for electric vehicles for example. It is therefore important to consider the bandwidth of the model and whether a particular model is suitable for the application at hand. As an illustration the two and three branch models have very fixed time constants which are an integral part of the parameter determination procedure for these models. This in turn leads to a narrow bandwidth for which the model behaviour is representative.

Another approach to designing a model for high capacitance devices is to approach the device as a circuit component which responds to temperature, voltage and current profiles in a given manor. Ultimately, the number and range of a cell's possible measurable parameters are limited and in fact only three measurements may be directly observed; terminal voltage, charging current and surface temperature. By looking at any one or a combination of these measurements and merging those with knowledge of the electrochemical processes occurring within some conclusions may be drawn about the electrochemical state of the interior, however, these are at best educated guesses and may only divulge a small insight into projected behaviour.

By basing the model solely on what is measurable the emphasis shifts from the physical processes occurring to observable effects. Taking this theory to logical extreme, the cell may simply be described as a mathematical expression linking the three measurable parameters described above.

As has been shown above the advantage of being able to describe the behaviour of an electrochemical cell through the perception of an internal circuit has qualitative value in that the model user can easily visualise the effect each aspect of the model has on overall performance. However, since many of the complexities of the other models arise mainly due to the need to realise the discrete values of equivalent circuit parameters the approach in [65] is to return to the simplified version of the idealised model shown in Figure 2-4 however to consider the transfer function of this model rather than the equivalent circuit. The method in [65] describes the determination of the transfer function of the EDLC by considering the transfer function of the

ladder model in an attempt to simplify model parameter identification. Although it is possible to use this model based on any number of branches in practice there is a computational limit to the order of such a system. The example of a three branch model is presented below for simplicity. The s-domain transfer function of a three branch RC transmission line model would be (2.16).

$$\frac{V(s)}{I(s)} = \frac{As^3 + Bs^2 + Cs + 1}{Ds^3 + Es^2 + Fs} \tag{2.16}$$

where the coefficients A through F are dependent on the RC line values.

Rather than attempt to define these values individually from separate measurements this method attempts to identify the coefficients A through F directly. Transforming (2.16) into a differential equation and using forward Euler Approximations for the derivatives yields a difference equation. Written in terms of the first differences of v and i the difference equations takes the form

$$[\nabla v_{n+3} + \nabla v_{n+2} + \nabla v_{n+1} + \nabla i_{n+3} + \nabla i_{n+2} + \nabla i_{n+1}] \begin{bmatrix} \frac{D}{T^3} \\ \frac{ET - 2D}{T^3} \\ \frac{D - ET + FT^2}{T^3} \\ \frac{-A}{T^3} \\ \frac{2A - BT}{T^3} \\ \frac{BT - A - CT^2}{T^3} \end{bmatrix} = [i_n] \tag{2.17}$$

where ∇v_n denotes $\nabla v_n - \nabla v_{n-1}$ and T is the sampling period. A least squares method can now be used to identify the parameters A-F [65].

There is a circuit described in [65] which shows a setup for measuring current and voltage levels at intervals of T whilst the capacitors are subject to various charge/discharge effects.

Experimentation shows that the neglected branches (in this case all but the first three) are not insignificant to describe the behaviour under the test conditions set out in [65]. Therefore two parameters are added to the transfer function in effect to approximate the missing branches. Parameter w would arise in effect from a parallel resistance at the end of the truncated transmission line. The parameter w is determined through a long self-discharge test where terminal voltage is measured and a value best describing the behaviour in the chosen time frame is chosen. There is also a DC bias which is accounted for after w is identified by the constant k so that the final transfer function is (2.18).

$$\frac{V(s)}{I(s)} = k\frac{As^3 + Bs^2 + Cs + 1}{Ds^3 + Es^2 + Fs + w} \tag{2.18}$$

This method is simple to implement and relatively inexpensive and quick for parameter extraction. Because it is designed for short term transient modelling it does accurately describe this sort of response. However, as the authors note to accurately describe the longer term effects of redistribution transients the model higher order, or more likely fractional order, systems would have to be introduced [65].

The drawback of not implementing an equivalent circuit approach is that the implementation of such models in power electronics simulations is more difficult. Simulation packages such as SPICE are not geared for integration of such transfer function behavioural models and those that are, such as MATLAB Simulink, do not have good provision for power electronic circuit simulation.

A compromise solution is to define an equivalent circuit whose parameters are derived from a governing characteristic equation, such as (2.18), and can be represented in simulation software as an equivalent circuit. The individual equivalent circuit component parameters are not directly related to any physical process but to a component of the characteristic equation.

Electrochemical impedance spectroscopy (EIS) is an analysis technique which is widely used technique to study the complex impedance of electrochemical energy storage systems [66].

The general principal of EIS is to apply a sinusoidal signal to the cell and measuring the characteristic response from the cell which is defined by the cell impedance. The input, or drive, signal can either be current (galvanostatic) or voltage (potentiostatic). The process can be repeated across a range of cell voltages and temperatures to give a representative lookup table of parameters.

By taking the voltage signal as the reference the complex impedance is defined as the complex ratio of the voltage signal to the current signal including its phase shift (2.19).

$$Z = \frac{v(t)}{i(t)} = \frac{\hat{V} \cdot \sin(\omega t)}{\hat{I} \cdot \sin(\omega t + \phi)} = |Z| \cdot \frac{\sin(\omega t)}{\sin(\omega t + \phi)} \tag{2.19}$$

where $\hat{V}$ is the peak voltage, $\hat{I}$ is the peak current, ω is the angular velocity (frequency), $|Z|$ is the absolute value of the impedance and ϕ is the phase difference between the current and voltage. Furthermore, the extrapolation of the real and imaginary parts of the impedance may be given by (2.20) and (2.21).

$$Z_{\text{re}} = |Z| \cdot \cos(\phi) \tag{2.20}$$

$$Z_{\text{im}} = |Z| \cdot \sin(\phi) \tag{2.21}$$

Plotting these values on a Nyquist chart gives the relationship between real and imaginary impedance over a frequency range. An idealised schematic of a Nyquist impedance plot for a typical EDLC cell is shown in Figure 2-11. Each point on the plot line represents a frequency at

which the impedance is measured. These impedance plots vary with SOC and temperature as can be seen in Figure 2-16 and Figure 2-17.

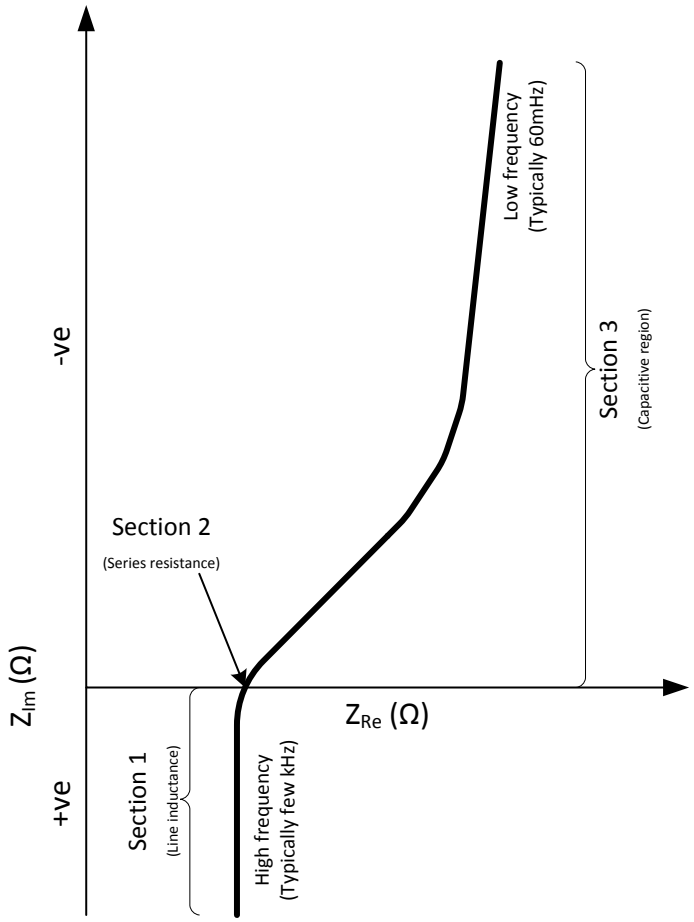

Figure 2-11 – Idealised impedance frequency response of EDLC

In EIS analysis it is common to lump individual parts of the impedance spectrum into distinctive and independent impedances. The extent to which these lumped parameters are then subdivided represents the complexity of the behaviour of that part of the impedance spectrum.

For the case of the EDLC the number of sections to which the impedance plot may be split is smaller than that of an electrochemical battery. This is principally because the energy storage mechanism for EDLCs is only in polarisation rather than the mass transfer process which is present in the battery system.

In [67] it is suggested that the complex impedance response of the cell, as shown in Figure 2-11, may be split into three separate and independent sections and represented by three lumped impedances as shown in Figure 2-12.

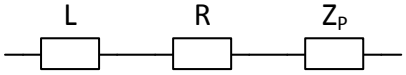

Figure 2-12 - Representation of lumped parameter model for EDLC impedance response

The first two lumped parameters, series inductance, L, and series resistance, R, are common to nearly all EIS technique models and are derived in nearly all cases in the same way.

The vertical asymptote in the positive imaginary Z plane (section 1, Figure 2-11) represents the behaviour of the cell at high frequencies and describes a point in its frequency response at which the cell behaves inductively. Since in the ideal case this line is vertical it may be represented by a single inductance parameter given the equation for the impedance of a pure inductor yields a pure reactance as is given by (2.22).

$$X_L = \frac{Z_L}{j} = \omega L \tag{2.22}$$

where Z_L is the impedance of the first lumped parameter and consists simply of an inductor L. The value of L may be calculated from a measured impedance plot by fitting the reactance of section 1 to (2.22).

The point at which the impedance response intersects with the real axis the impedance response shows no reactive behaviour. At this point the inductive behaviour of the high frequency response and the capacitive behaviour more readily associated with the EDLC are in balance and the cell behaves as purely resistive impedance. This is usually termed the equivalent series resistance (ESR) and forms the second part of the lumped parameter model shown in Figure 2-12. The value of this resistance parameter is simply the value of impedance at which the response crosses the real axis. Having no reactive component this section of the model may be represented as simply a series resistor which has the value of the crossing point.

The 45° region at medium frequencies (at the beginning of section 3 on Figure 2-11) describes the number of active RC branches diminishing as frequency increases – effectively moving the region of ionic activity down the electrode pore [2, 67] – the physical concept may be understood schematically as depicted in Figure 2-5. The relative magnitude of the elements at the high frequency end of the ladder reduce, thus the addition of an extra active branch in the high frequency region has less relative bearing on the overall complex impedance. The 45° region is commonly known as the Warburg impedance.

The porous electrode impedance $\underline{Z}_p$ is responsible for the 45° slope at mid frequency as well as the approach to ideal capacitor behaviour towards DC. A characteristic equation for Z_P (2.23) is presented in [67].

$$\underline{Z_p(j\omega)} = \frac{\tau \cdot \coth\left(\sqrt{j\omega t}\right)}{C \cdot \sqrt{j\omega\tau}} \tag{2.23}$$

This expression has only two independent parameters; C and τ, which means combining these with the calculated parameters for the first two sections of the model, series resistance and inductance as shown above only four parameters need to be extracted from the measured

spectra. Since the series inductance, L, and resistance, R_i, can be computed directly from inspection of the impedance response these may be subtracted from the complex impedance response leaving only Z_p. The response over the remaining frequency range may be curve fitted using an appropriate algorithm to gather the coefficients of (2.23).

As has been discussed, the response of the EDLC cell is by no means linear and is dependent on cell temperature and voltage. Therefore an impedance response spectrum measurement must be made over a range of cell temperatures and terminal voltages to create a three-dimensional lookup table for each of the four parameters required for the model.

The inverse Laplace transform cited in [67] for (2.23) can be shown in the following steps. Take (2.24).

$$\frac{k_1}{\sqrt{s}} \cdot \coth\left(\frac{k_2}{k_1}\sqrt{s}\right) \overset{L^{-1}}{\Longrightarrow} \frac{k_1^2}{k_2} + \frac{2k_1^2}{k_2}\sum_{n=1}^{\infty} e^{\left(-n^2\pi^2 k_1^2/k_2^2\right)t} \tag{2.24}$$

Comparing the coefficients of (2.23) and (2.24) leads to (2.25)

$$\begin{aligned} k_1 &= \frac{\sqrt{\tau}}{C} \\ k_2 &= \frac{\tau}{C} \end{aligned} \tag{2.25}$$

Given the general transformation for an RC circuit;

$$\frac{R_*}{sR_*C_* + 1} \overset{L^{-1}}{\Longrightarrow} \frac{1}{C_*} \cdot e^{-(t/R_*C_*)} \tag{2.26}$$

A comparison of coefficients between (2.26) and (2.24) and substituting values from (2.25) allows a series expansion to *n* RC circuits. Since this is a mathematical operation there is no increase in the number of model parameters and hence the only limit on the number of RC circuits is computational power [67].

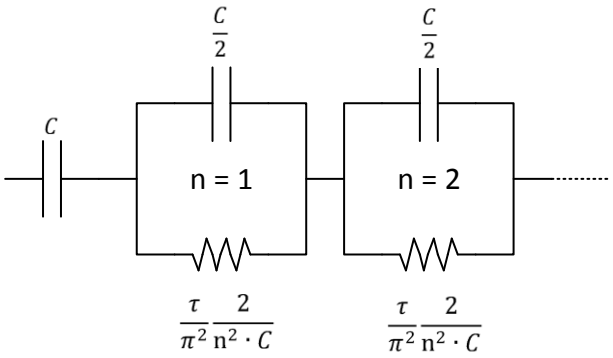

Figure 2-13 - Approximation of complex impedance of EDLC through a series expansion of RC circuits

This model is an elegant solution to modelling frequency dependence and the very few parameters required from experimental measures is a strong advantage for this model. The fact

that it can be augmented to cover voltage and temperature ranges makes this a particularly powerful model. The ability to form an equivalent circuit with which to model the behaviour from only four parameters also greatly improves the usefulness of the model in simulating cell behaviour in conjunction with power electronic interface.

The drawback to this is that to be able to model any particular capacitors response to a given operating point a large number of measurements for τ, C and R_i have to be performed close to that operating point, if a large range of operating points is expected the amount of data that must be gathered is large. This model predicts response to an input based on having already observed the behaviour in response to that input, thus taking too few readings will lead to extrapolation errors.

The procedure above describes a series expansion model as a summation of RC circuits. There is a corresponding method described in [61] presenting a model based on an expansion of parallel RC branches similar concept to the idealised and reduced branch models however with many more branches and related time constants. It has the advantage of being able to describe behaviour across a wide range of frequencies and its topology is much simpler than that of the transmission line models making it less intensive to model.

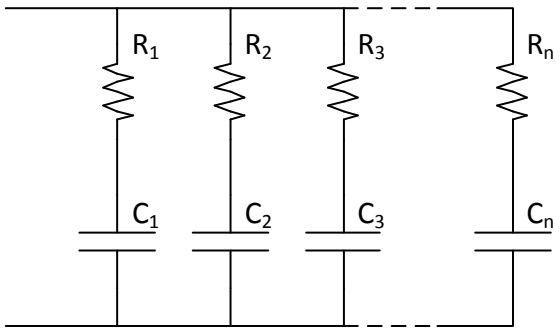

Figure 2-14 - Transfer Function Model Equivalent Circuit

The core of this model's parameter extraction process is the nonlinear least-squares fitting of time response data to a transfer function derived from the equivalent circuit.

With any ladder circuit the proposed circuit can be firstly written in Laplace form, the response of the circuit then derived under current charge profile or AC impedance analysis and the inverse transform returns the time domain response. Using the example of the ladder circuit in Figure 2-14 the parameters R_1, R_2, …, R_n and C_1, C_2, …, C_n can be obtained using the nonlinear least squares fitting algorithm. Unfortunately this method alone results in a large number of non-related parameter values which each have to be computed separately when the model is subjected to analysis. This results in poor computation losses and increased parameter calculation time.

Reduction of parameters can be realised by defining:

$$R_i = r^i R_1$$
$$C_i = \frac{C_1}{r^{2i}} \tag{2.27}$$

Where r is a positive constant with value greater than 1 and $i = 1,2,3,\dots,n$. Substituting (2.27) into the above procedure requires only three parameters, C_1, R_1, and r. With (2.27) imposed the proposed equivalent circuit in Figure 2-14 is simplified to a series of RC branches where the time constant of each branch decreases by *r* times from left to right [61].

This makes the frequency domain transfer function extremely easy to derive; each RC element is represented in s domain as

$$G(s) = \left[(n-1)rR_1 + \frac{(n-1)r^2}{sC_1}\right] \tag{2.28}$$

Thus a two branch model containing two parallel RC branches would be represented in the s domain by

$$G(s) = \frac{\left(R_1 + \frac{1}{sC_1}\right)\left(rR_1 + \frac{r^2}{sC_1}\right)}{\left(R_1 + \frac{1}{sC_1}\right) + \left(rR_1 + \frac{r^2}{sC_1}\right)} \tag{2.29}$$

When the circuit is charged by constant current the time response of the circuit can be derived using inverse Laplace transformation

$$f(t) = r\frac{-R_1 r(r-1)^2}{(1+r)(1+r^2)^2} e^{\frac{-(1+r^2)}{R_1C_1+rR_1C_1}t} + r\frac{(1+r^2)t + R_1C_1(1+r)(r^2-r+1)}{C_1(1+r^2)^2} \tag{2.30}$$

Finally the nonlinear least-squares fitting process is used to get the parameters of the circuit model. The entire process, however, is easily implemented in software such as MATLAB.

One drawback with both the series expansion model and the parallel expansion is the order of the transfer function that will be used to calculate response in the background of the simulation. Models with high orders are more computationally expensive and result in long simulation times. The order of the circuit can be reduced by deliberately choosing the bandwidth of the model by setting the time constant parameters and reduction rate based on the frequency range and resolution required. In the parallel expansion model this process is fairly simple but would require some alteration to the series expansion method.

For the case of the parallel expansion if the parameters of a one-branch model are defined using the nonlinear least-squares fitting algorithm as above then the time constant of this first branch can be said to be the base time constant, or T_{base}. It is now possible to define the time constant of

each branch since the application of (2.27) yields that each time constant decreases as n increases; $T_{base}, \frac{1}{r}T_{base}, \frac{1}{r^2}T_{base}, \ldots, \frac{1}{r^n}T_{base}$. The latter being the smallest time constant which means the frequency range is $\frac{1}{T_{base}}$ to $\frac{r^n}{T_{base}}$.

For any given frequency range the value of r (from (2.27)) defines the number of branches. Thus as r approaches its minimum value, 1, the number of branches gets extremely high. As r increases the number of branches decreases however the resolution of the model decreases also. Therefore there is a trade-off between performance and accuracy of the model. In [61] a value of between 1.5 and 3 is suggested as appropriate.

Once r is defined the number of branches can be determined by establishing a frequency range for the model (2.31) .

$$\text{where } f_{max}=\frac{r^n}{T_{base}} \qquad n=\frac{\log[T_{base}\cdot f max]}{\log[r]} \tag{2.31}$$

2.4 Summary on modelling techniques for power electronics interface simulation

The range of modelling methodologies for electrochemical energy storage systems is large, partially because the available parameter extraction facilities are varied and partly because the motivations for developing a model are varied and require models which are applicable to different behavioural analysis techniques.

For the case of integration into power electronic systems the models which use measurement of response to external input to derive their parameters are the most appropriate. Within this group of models it is possible to define the model type either as an energy storage method or as an impedance model. The energy storage models are simple to define and parameterise and are not computationally expensive, however, they lack accuracy over for dynamic response. Impedance based models are much more accurate over a range of charging dynamics but require large datasets of experimental measurements to define the parameters and can be more computationally expensive. The impedance based models which can be extrapolated into series or parallel expansions are useful in that although they require large datasets the model variable count is low and the order of the model can be selected to control simulation time.

All the summarised techniques in this chapter are published showing good results for their given application, however, it is deemed most appropriate for the cases of research of power electronic interface that the impedance based models with order selection are the most appropriate.Table 2-3 shows a summary of the advantages and disadvantages associated with each model

Table 2-3 - Summary of EDLC advantages and disadvantages

Model	Advantages	Disadvantages
Idealised/Physical models		
Stern Theoretical Model	• Clearly shows and enables understanding of double layer, porous and electrochemical effects.	• Impractical for design and simulation purposes
RC Transmission Line	• Good simplification of theoretical model • Good basic structure guidance for simpler models	• Still impractical as parameter extraction is difficult • Computationally expensive
Characterised models - Energy Storage Models		
Classical Model	• Conceptionally very simple • Parameter extraction uncomplicated	• Does not model wide frequency response leading to poor transient modelling • Does not model voltage dependence capacitance
3-Branch Model	• Accurate for medium term charge redistribution effects • Partially models voltage dependency on charging response • Attempts to model long term self-discharge effects	• Poor transient modelling • Effectively becomes classical model under transient conditions • Only relevant for fixed value, constant current charging
2-Branch Model	• Similar advantages to 3-Branch model however parameters are simpler to extract	• Poor transient modelling • Effectively becomes classical model under transient conditions • Only relevant for fixed value, constant current charging
Characterised models - Impedance measurement models		
Series Expansion Model	• Large possible bandwidth • Requires only two parameters from EIS • Yields good accuracy for realistic charging current profiles • Can be implemented across user specified ranges and resolutions of temperature and terminal voltage • Order selection, and therefore model bandwidth is defined by the user • Implementable as an equivalent circuit, signal flow or transfer function.	• Requires a large collection of look-up table data to be used during simulation • Order can be very high resulting in increased computational cost • EIS can be an expensive tool
Parallel Expansion model	• Large possible bandwidth • Can be implemented across user specified ranges and resolutions of temperature and terminal voltage • Order selection, and therefore model bandwidth is defined by the user	• Order can be very high resulting in increased computational cost • Mathematics involved in model derivation can result increased computational cost compared to series expansion model • Difficult to implement as equivalent circuit with order selection
Transfer Function	• Transfer function is easily obtainable from simple experimentation • Order selection and therefore bandwidth is defined by the user	• No equivalent circuit makes interfacing model in power electronics simulation difficult • Employs performance compensation coefficients • Long term effects are difficult and computationally expensive to simulate

For the purposes of this work the series expansion method, as described in [67], has been identified as the most appropriate method for cell modelling.

2.5 Development of a modelling technique for direct comparison

This section describes the development of the series expansion model for direct comparison of the Maxwell supercapacitor and the JM Energy Li-ion capacitor. The work presented in this section is original work carried out by the author. EIS measurements are made for both traditional Maxwell PC2500 ultracapacitors and also for JM energy Li-ion capacitors. The modelling technique selected in the previous section is used to characterise the Maxwell cell and a model generated. The model is then tested against a measured load profile response. The modelling technique is then extended to develop a similar characterisation technique for the Li-ion cells. The model validation process is repeated using load profiles.

The direct comparison of the datasheet information given by the manufactures of the Li-ion capacitor and the PC2500 is the most simply accomplished comparison. As is expected from the assembly process described for the Li-ion capacitor in section 2.1.2 the maximum voltage of the Li-ion capacitor is 1.5 times larger than that of the PC2500 however the voltage range is smaller. Since capacitors must be stacked in series to attain systems level voltages a higher voltage cell not only has higher energy storage capabilities but also requires fewer cells to attain the system voltage. Fewer cells results in fewer power interfaces for voltage equalisation/protection and measurement are required. This reduces cost and size of ESS systems employing cells with higher maximum voltages. The pouched packaging also makes the integration of the Li-ion cell into applications such as electric vehicles more flexible since the energy/power densities are better.

Datasheet analysis allows a macro analysis of the technology and may be sufficient to generate simple models such as the classical model simply from the data presented. However, true dynamic response data is rarely presented in electrochemical ESS datasheets.

The dynamic response measurements can be split into two types; constant current measurements and AC current analysis. The response to step current changes has been proposed as a method for gathering simple model parameters. The AC analysis has been shown as a good measurement technique for developing models with better dynamic representation.

2.5.1 Constant current charging response of sample cells

A simple constant current discharge test was performed on both sample technologies described in 2.1. The discharge of 80A was performed from cell maximum voltage to cell minimum voltage for three of each device and the results averaged. The resulting discharge profile is shown in Figure 2-15.

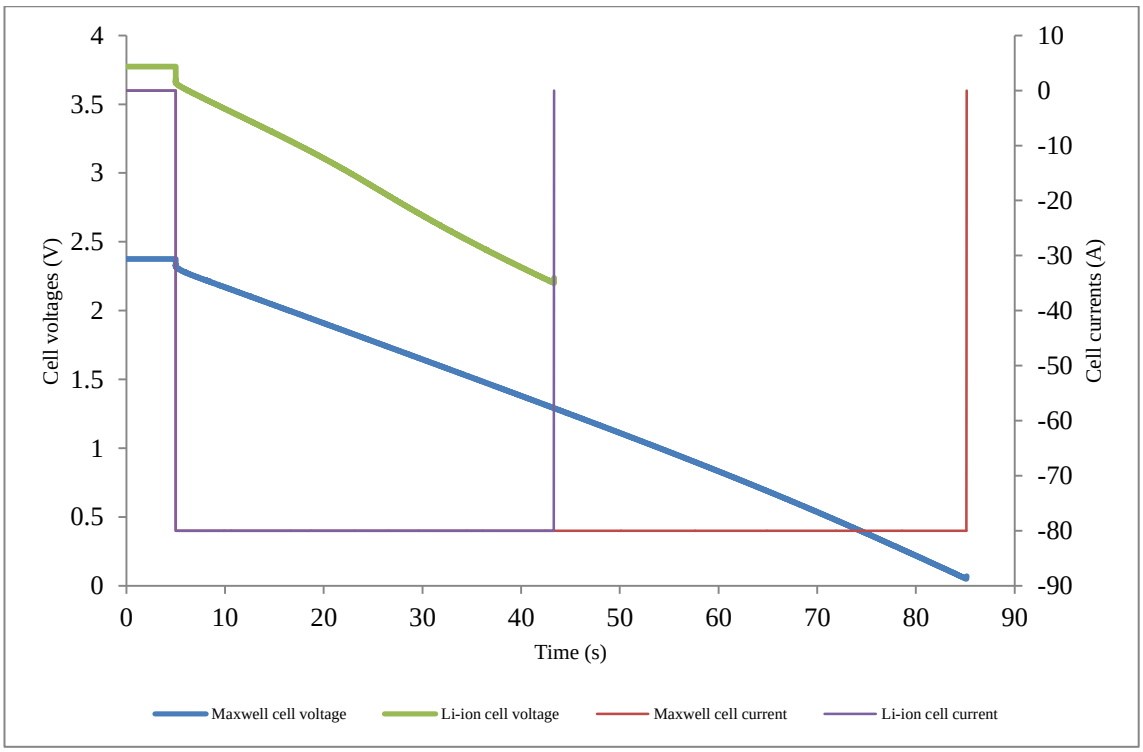

Figure 2-15 - 80A constant current discharge profiles for both Li-ion capacitor and PC2500 ultracapacitor

If the assumption is made, as is in [60, 61, 64], that the step voltage change in the profile due to the step current change is wholly a result of the voltage drop across the series resistance, then the ESR for each cell can be calculated using (2.3). The DC discharge current was controlled to be a constant 80A therefore the ESR values for the supercapacitor and Li-ion capacitor can be calculated as 0.9mΩ and 1.4mΩ respectively.

The limitation of this method for ESR calculation is that it cannot take into account the effect series inductance would have on a step current change – the effect would be an exaggeration of the step in voltage – although the measured values appear to match the quoted values well which would indicate that the quoted values may have been derived in a similar way. There is no way to separate the inductance from ESR in this step analysis thus the ESR values quoted above are specific to a step current change. Also, voltage converters do not generally employ step current changes, a step voltage change on a coil resulting in trapezoidal current profiles is more common.

2.5.2 Electrochemical impedance spectroscopy measurement of sample cells

AC impedance measurements were made for three of each of the PC2500 and Lithium-ion cells at a range of voltages. The Maxwell device impedance spectrum was measured at 0.5V, 0.7V, 0.9V 1.1V, 1.3V, 1.5V, 1.7V, 1.9V, 2.1V, 2.3V and 2.4V and the Li-ion capacitor spectrum was measured at each of 2.4V, 2.6V, 2.8V, 3V, 3.2V, 3.4V, 3.6V and 3.8V. The frequency range was a sweep from 20kHz down to 60mHz. The impedance spectra for the Maxwell device and the JS micro device are shown in Figure 2-16 and Figure 2-17 respectively.

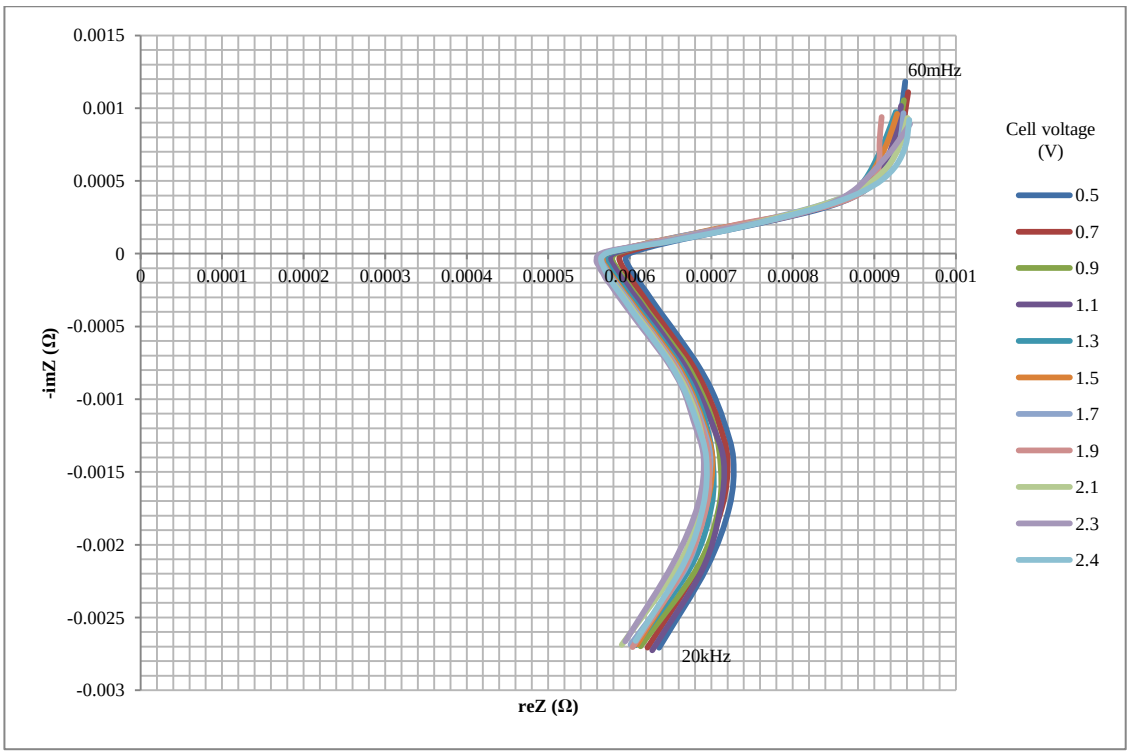

Figure 2-16 - Impedance spectrum for PC2500 ultracapacitors at cell voltages of 0.5V - 2.4V

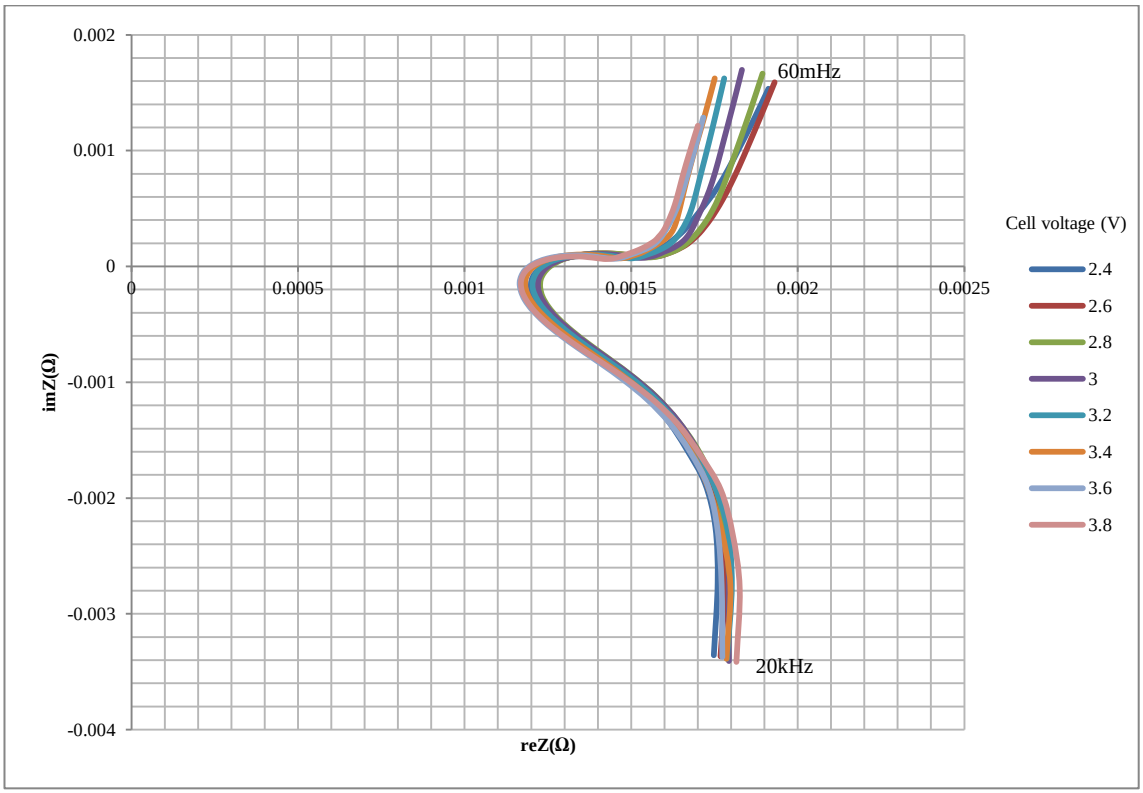

Figure 2-17 - Impedance spectrum for Li-ion capacitors at cell voltages of 2.4V - 3.8V

As might be expected from the description of the assembly of the Li-ion cell the impedance spectra for these devices exhibit a small semi-circular area before the Warburg impedance. This behaviour is similar to that which would be expected from the cathode of a Li-ion battery which exhibits a Zarc impedance. The Zarc element consists of a constant phase-element (CPE) [68].

Since the Li-ion capacitor also has a Lithium doped cathode the presence of a CPE in its impedance spectrum is unsurprising. CPEs consist of a generalised capacity θ and depression factor ψ as defined by

$$Z_{\text{CPE}} = \frac{1}{(j\omega)^{\psi}\theta} \tag{2.32}$$

The Zarc element is completed by the addition of a parallel resistance, *R*, which yields

$$Z_{\text{Zarc}} = \frac{1}{\frac{1}{R} + (j\omega)^{\psi}\theta} \tag{2.33}$$

Comparing (2.33) to a single RC element from shows that the form of the expressions for the total impedance of the equivalent circuit would be identical except for the inclusion of the depression factor, ψ. The depression factor exists between 0 and 1 and is responsible for the depression of the semi-circular form of the impedance of a Zarc element when represented on a Nyquist impedance plot [69]. Figure 2-18 shows an example of a Zarc impedance from [69].

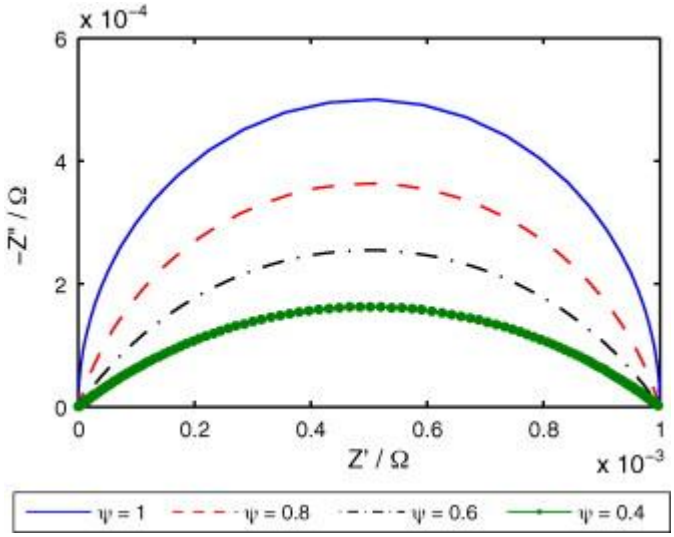

Figure 2-18 - Nyquist plot of impedance of Zarc element [69]

In this way, a depression value $\psi = 0$ would indicate a purely ohmic resistance and $\psi = 1$ would represent an ideal RC element. Clearly this gives an advantage in being able to represent the depressions which occur in real measurements; however there is no Laplace transformation for this form so it is impossible parse the parameter sets to the frequency domain without linear approximations [69].

It has been shown that the Zarc impedance can be approximated to a variable number of RC elements [69, 70]. The approximation with five elements is shown in Figure 2-19.

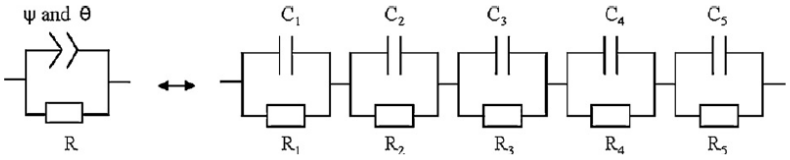

Figure 2-19 - Approximation of Zarc with five elements [69]

The Zarc impedance can be inserted into the idealised impedance spectrum in Figure 2-11 between sections two and three as another impedance and its parameters derived either in isolation of the rest of the impedance spectrum or by combining (2.33) and (2.23) and reforming the coefficients of (2.25) so that the RC branches are defined differently.

2.5.3 Model development from measured impedance response

The measured response of impedance produces a large amount of data which must be processed to produce the whole model. Since the dataset is large automating the parameter extraction is an ideal method to produce the model. For each of the DC voltage levels a dataset of frequency versus complex impedance exists. From this dataset the model parameters are extracted for each voltage level. The method for parameter extraction is shown in Figure 2-20.

The parameter extraction process results in a lookup table for the equivalent circuit parameters against each voltage level. Figure 2-21 shows the measurements for series resistance and inductance of the Maxwell PC2500 cells. It shows a decreasing trend as voltage increases for both measurements. The trend for the Li-ion capacitor appears less stable over voltage range with significant variations in inductance compared to the Maxwell and an order of magnitude higher. The levels of metallic salts in the device and their distributions at various states of charge are likely to account for this variance.

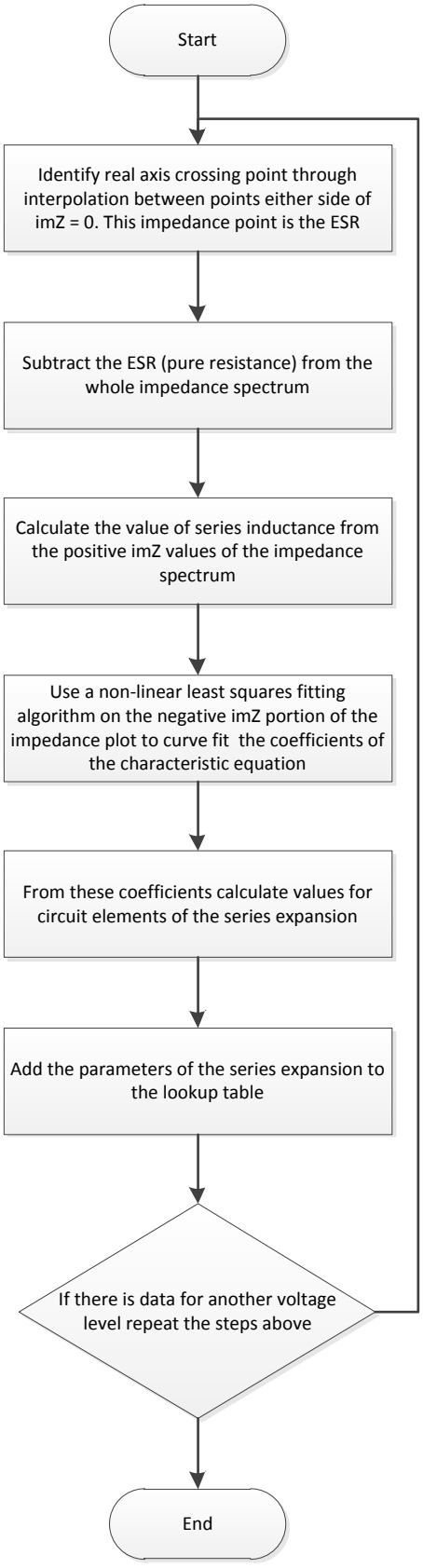

Figure 2-20 - Flowchart describing method for model parameter extraction

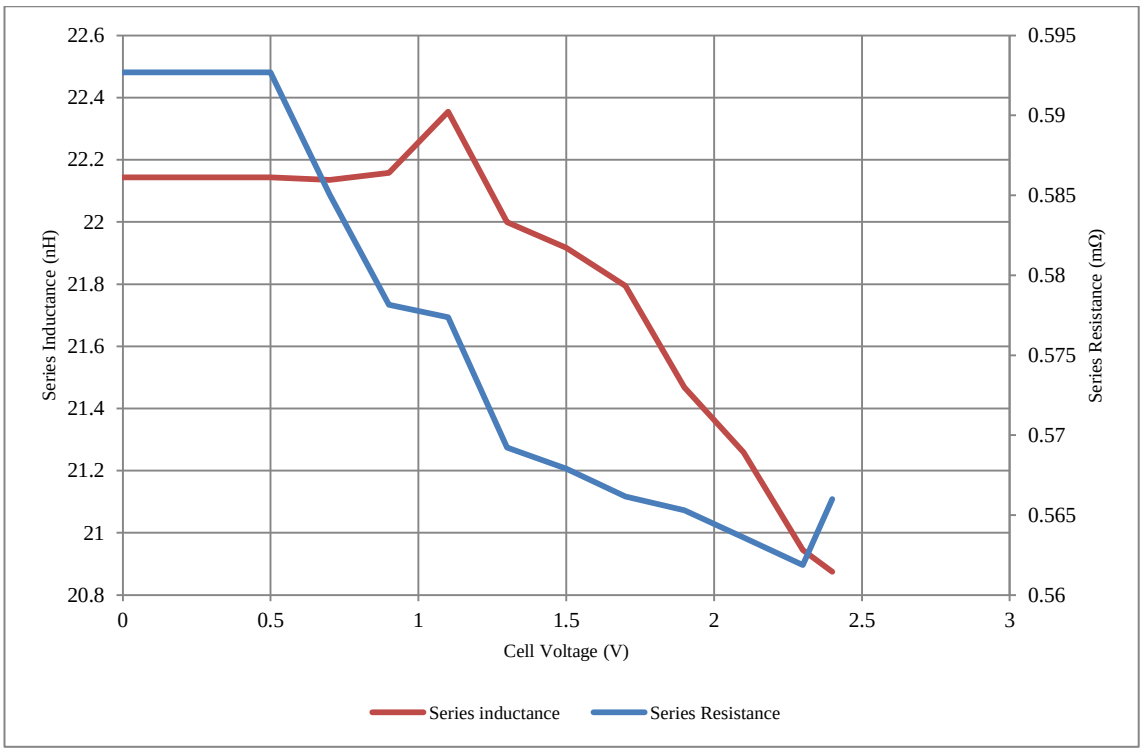

Figure 2-21 - Series resistance and inductance measurements for PC2500

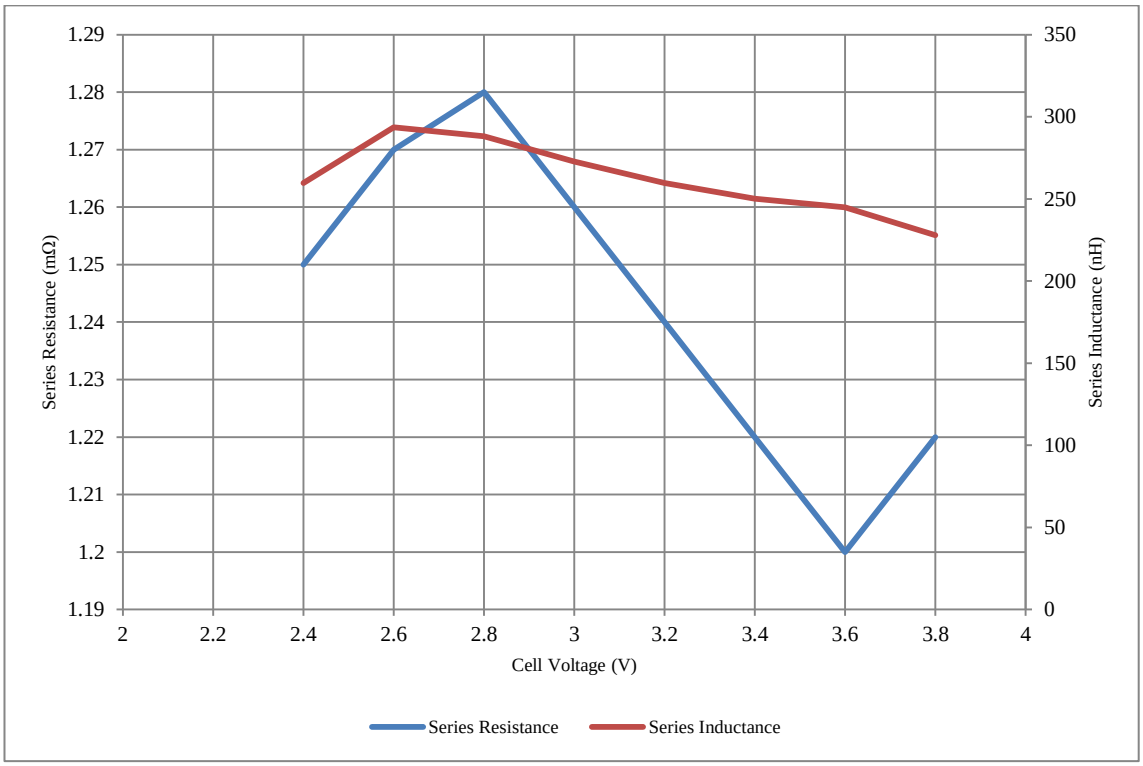

Figure 2-22 - Series resistance and inductance for JS Micro 2200F Li-ion capacitor

The remaining parameters of the series expansion of RC elements for the Maxwell cell are realised through mathematical expansion as described in section 27. The additional elements which represent the Zarc impedance are included for the Li-ion cell. This results in a large dataset for each technology which is used as a lookup table for modelling.

The realisation of these elements in an equivalent circuit model for use within power electronics simulation requires the storage of this lookup table as a header file for the simulation. Each equivalent circuit element has an associated vector which is may be compared terminal voltage according to the lookup table. An interpolation must be performed to determine points at voltages between the measured data. Therefore at each step in the simulation the equivalent circuit parameter is calculated from a measurement of the total cell voltage and following interpolation of the lookup table. The lookup tables may be used to drive the model parameters for either a network simulation which is familiar to circuit modelling, or a signal flow simulation which is more commonly used in control algorithm simulation. Both of these methods are discussed in more detail in chapter 3. Figure 2-23 shows a schematic representation of how the lookup tables may generally be used to generate equivalent circuit parameters.

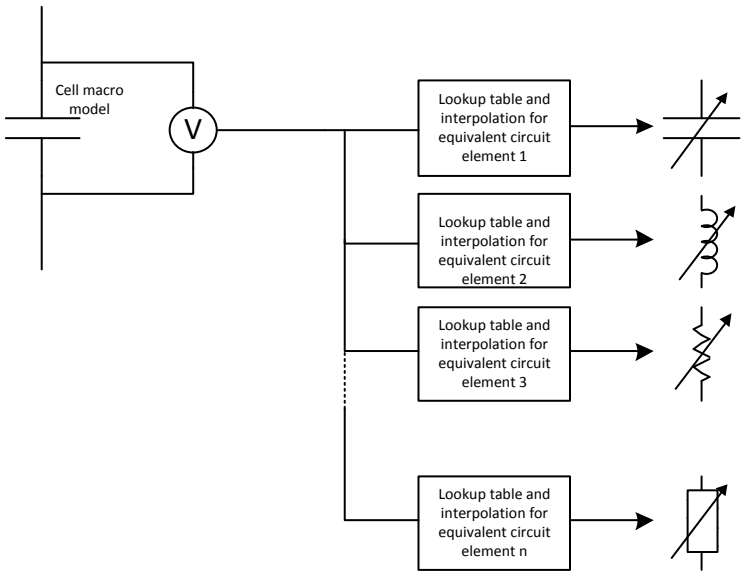

Figure 2-23 – Implementation of model from lookup tables

The models developed for each of the cells were tested against a load profile. Because of the difference in voltage ranges the profiles for each cell were necessarily altered to allow the cells to remain within their correct voltage range. The measured values may be compared to the simulated data in Figure 2-24 for the Maxwell PC2500 and in Figure 2-25 for the Li-ion capacitor.

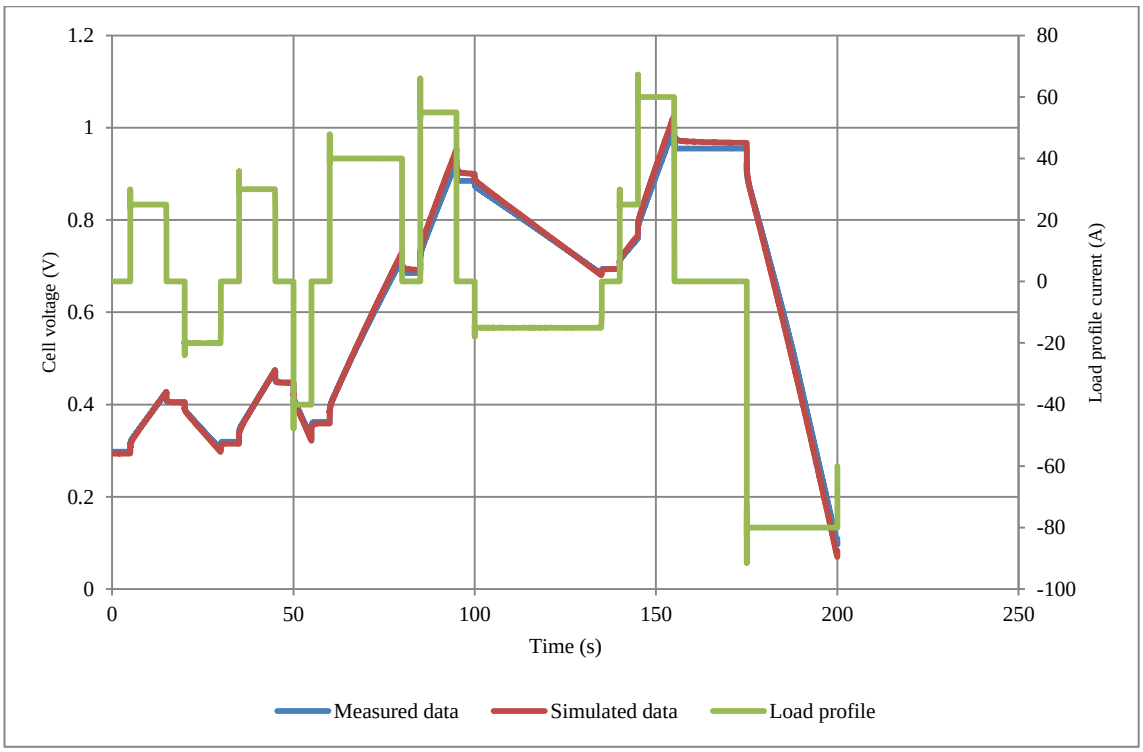

Figure 2-24 - Measured and Simulated load profile for PC2500 EDLC model

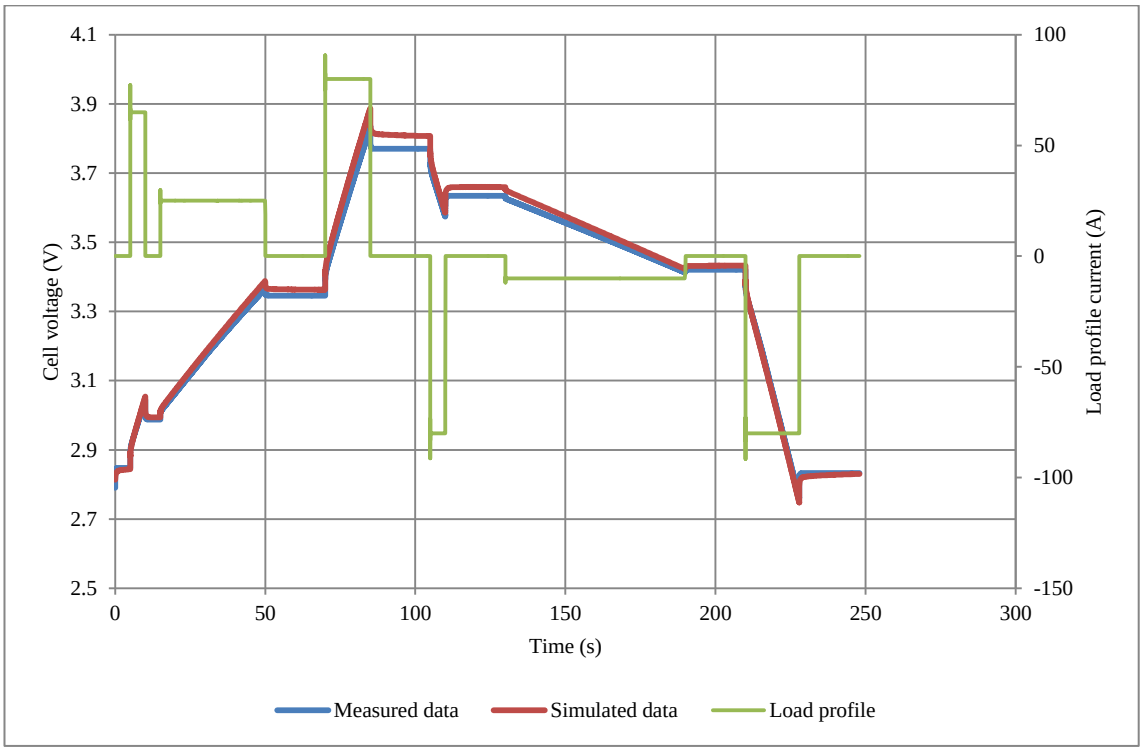

Figure 2-25 - Measured and Simulated load profile for JS 2200F Li-ion capacitor model

The simulated traces show excellent correlation to the measured trace when excited with the measured current trace. Some discrepancies occur during and just after heavy charging events.

2.6 Summary – Cell measurement and modelling

Cell measurement and modelling encompasses a wide multi-discipline study of cell behaviour from the perspective of electrochemistry and power electronics engineering. The motivations for development of behavioural models are varied and result in a wide variation of model types, methodologies and parameter extraction. For the purposes of power electronic interface analysis a model which describes behaviour over a wide frequency range with good representation of the voltage dependency of the model parameters has been shown to be effective for representation of cell behaviour. A method for extraction of model parameters for a traditional symmetric carbon-carbon EDLC and for an asymmetric Li-ion capacitor have been shown and comparison of load profile results for each are indicated as good representations of behaviour although there is some discrepancy at very high current levels for both methods. A method for integration of the models into a power electronics simulation has been presented.

In the results gathered from three sample cells of each technology the variation in parameters is far less than the 20% quoted in the datasheet. Although the sample number is small it is possible to conclude that within a particular batch the variation is not as wide as quoted.

3 Assessment of equalisation schemes

This chapter outlines a study into existing equalisation schemes covering their operation, simulation and summarising advantages and disadvantages. Conclusions on the suitability of each method are described and an ideal design specification is created for a new equalisation scheme.

Firstly, a representative selection of existing solutions is gathered as a literature review exercise. Then, as original work, each of these schemes is simulated to assess the performance.

Equalisation schemes may be grouped by considering various properties of each of the schemes. As has been described in section 1.6, dissipative voltage equalisation is not considered here due to its poor global efficiency. This chapter first outlines equalisation scheme groupings, or families, followed but the analysis of selected schemes from literature.

Note – The results shown in this chapter were gathered using a number of simulation platforms. This was a result of some platforms becoming available to the author whilst the work was being undertaken and hence the results are presented in slightly differing formats. This was mainly due to the majority of the work being carried out whilst studying in China where different software was available.

3.1 Overview of active equalisation families

Non-dissipative equalisation schemes may be deemed to belong to a family grouped either by topology (a study of the energy flow paths) or constituent components. Grouping by constituent components gives a good indication of the physical properties of the equalisation circuit such as mass, volume, component count, modularity and cost. Energy flow path families give indications of equalisation rate and flexibility. Both considerations are important for analysing an equalisation solution and relating its performance to a given application. Figure 3-1 shows the taxonomy of equalisation schemes which will be discussed in this chapter and how they may be grouped into families.

This work represents the first time existing equalisation schemes have been described and analysed in this way.

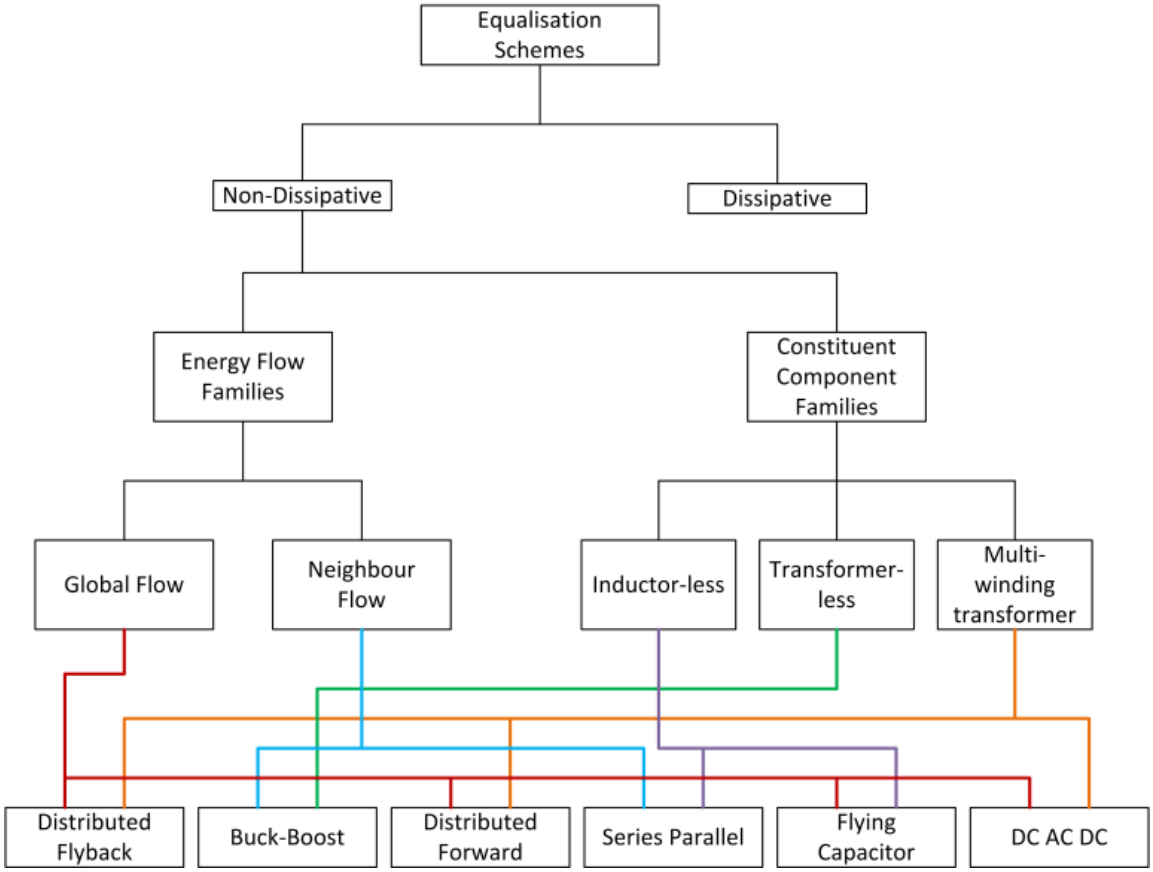

Figure 3-1 – Taxonomy of equalisation scheme families

3.1.1 Energy Flow Paths

Considering a stack of capacitors such as those shown in Figure 3-2 and assuming a system of equalisation exists to transport energy from a capacitor C_n, which is deemed to require discharging, to target cell(s) then two possible energy flow path types are possible; either the equalisation scheme is able to transport energy from one cell to either of its adjacent cells – such as in the left hand side of Figure 3-2 – or it is able to transport energy from the source cell to any of the other cells in the stack – as shown in the right hand side of Figure 3-2. These energy flow path types will be referred to as neighbour energy flow paths and global energy flow paths respectively. The concept of energy flow paths in voltage equalisation is introduced in [53].

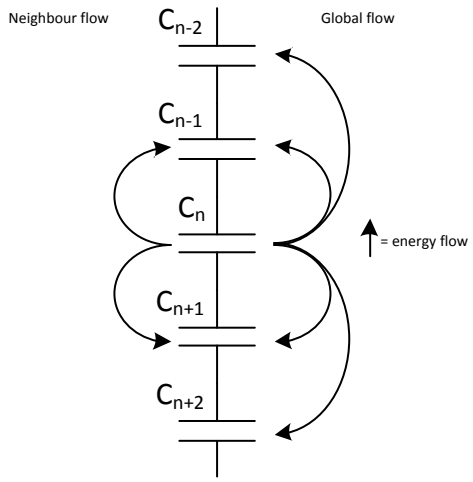

Figure 3-2 - Energy flow paths in a series connected stack of capacitors for neighbour energy flow (LHS) and global energy flow (RHS).

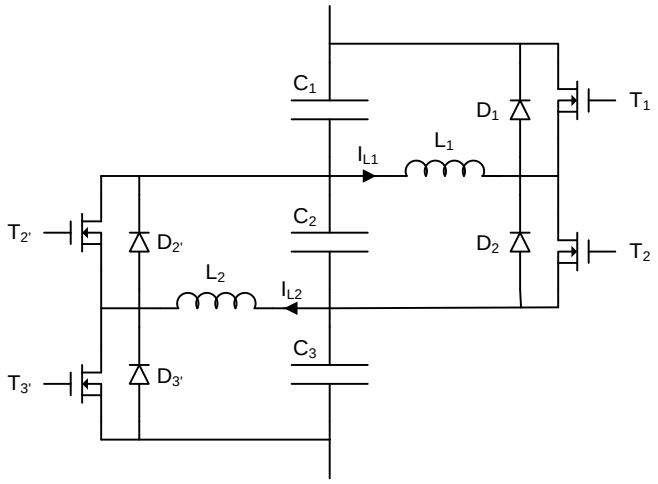

Figure 3-3 - Voltage equalisation through utilizations of bi-directional buck-boost converters

Neighbour energy flow paths offer some advantages over global energy flow paths; it is far easier to create a modular system for a neighbour energy flow path since each energy flow path is isolated from one another. This property lends itself to small independent converters, which make it simpler to add or subtract cells. An excellent example of a neighbour energy flow equalisation scheme is the interleaved buck-boost converter shown in [71]. In this converter energy may pass from a cell to either of its neighbours but it cannot directly move to a cell to which it is not adjacent. The modularity of this equalisation scheme is clear – only a few extra components are required to increase the number of cells and each buck-boost converter operates independently. Neighbour flow equalisation schemes become less attractive when considering a long stack of cells where energy may be required to move between cells which are longer distances apart (in terms of number of cells apart on a stack). For the worst case, energy would be required to move from the very top cell to the very bottom cell. Under a neighbour flow scheme the energy would have to ripple through the entire stack incurring efficiency and time delay penalties as a function of the number of cells. Most industrial applications have working levels in the hundreds of volts and a typical supercapacitor stack may have several hundred

cells. Without time consuming testing at the manufacturing stage it is impossible to be certain the locations of cells with high or low relative nominal capacitances and therefore it must be considered that the worst case scenario described above is a valid situation for all stacks. The effectiveness of neighbour flow equalisation schemes is therefore limited by requirement to design for the worst case situation in line with the size of the stack. However, with a bell curve distribution of nominal capacitances throughout the stack the likelihood is that the scheme will be heavily overrated leaving a large, unnecessary power headroom. This is discussed in more detail in section 3.2.3 and chapters 4 and 5.

Global equalisation schemes therefore present themselves as more desirable solutions for large stacks of cells that would typically be found in any system of any appreciable power level. An example of a global equalisation scheme is the forward converter with distributed primary shown in Figure 3-4.

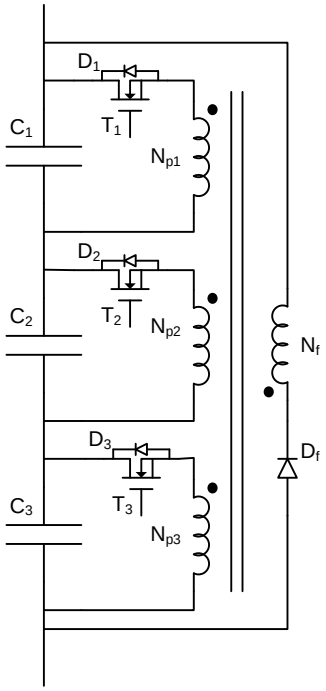

Figure 3-4 - Forward converter with distributed primary windings equalisation scheme

3.1.2 Constituent Component Analysis

Constituent component analysis in this context is an analysis of the actual circuit components which make up the equalisation scheme. This section identifies particular component classes which are common to one or more equalisation converters and analyses the effect these components have on equalisation.

The obvious difficulty which is presented by global energy flow systems such as the distributed flyback and distributed forward converters [48] is the galvanically isolated energy flow required when transporting energy from one relative potential level to another – i.e. from a cell to a non-

adjacent cell. In all other presented cases in this thesis, the isolation is achieved using magnetic coupling of coils via a central magnetic core. Figure 3-4 shows the flyback converter with distributed secondary windings as described in [48]. Galvanic isolation is achieved by associating a separate transformer winding with each cell in the stack.

There are two main drawbacks to isolating the energy flow using this method; firstly the requirement for a bespoke transformer means that there is little or no scope for modularity of the system and secondly such a transformer becomes extremely large and difficult to physically manufacture and make connections to for systems with large numbers of cells. Since a stack of supercapacitors may have several hundred cells the associated transformer will have several hundred isolated windings.

For neighbourly sharing equalisation schemes the constituent components maybe considered as either transformer-less or inductor-less. Table 3-1 shows the groupings of equalisation schemes either by energy flow path or by constituent component class.

Table 3-1 - Grouping of families of existing equalisation schemes

	Passive	Active	Dissipative	Coupled-Coil	Transformer-less	Inductor-Less	Neighbourly sharing	Global Sharing
Parallel resistors	*		*					
Zener diodes [47]	*		*					
Switched resistors [47]		*	*					
Buck-Boost [48]		*			*		*	
Series-Parallel [72]		*				*	*	
Flying Capacitor [47]		*				*		*
Distributed Flyback [48]		*		*				*
Distributed Forward [48]		*		*				*

3.1.3 Transformers with distributed primaries/secondaries

The family of coupled coil equalisation schemes utilise a transformer with either distributed primary windings or distributed secondary windings. Taking the example of a converter with distributed secondary windings, such as the centralised flyback equalisation scheme the transformer is made up of a single primary winding and *n* secondary windings – where *n* is the number of supercapacitor cells in the stack. Consider the transformer shown in . The primary winding is a single coil of N_P turns and an inductance of L_P. In this case there are three secondary windings which have equal turns and inductance; N_S and L_S respectively. For the

purposes of this comparison the magnetic circuit is assumed to be ideal, i.e. a coupling factor of 1 between all of the coils.

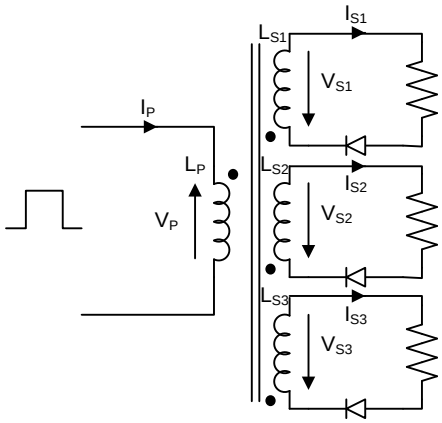

Figure 3-5 – Flyback converter transformer with distributed secondary

When considering a transformer of only a single primary and single secondary winding the inductance of the primary coil can be described as

$$L_P = \frac{N_P^2}{S} \tag{3.1}$$

where S is the reluctance of the magnetic circuit. The inductance of the secondary is given by:

$$L_S = \frac{N_S^2}{S} \tag{3.2}$$

Since the assumption is that the coils are coupled perfectly, the magnetic reluctance seen by each coil must be equal. Therefore, and can be equated to give

$$\frac{L_P}{L_S} = \frac{N_P^2}{N_S^2} \tag{3.3}$$

For a common transformer, the voltage of the secondary compared with the voltage on the primary is related to the turns ratio of the two coils. The coupled coil transformers require that for a square wave voltage pulse of 1V on the primary would a give a peak voltage on the secondary during its conduction phase of $\frac{1}{n}$V (where n is the number of cells in the stack). This yields

$$N_P = nN_S \tag{3.4}$$

Thus,

$$L_P = nL_S \tag{3.5}$$

However, analysis of the multi coil transformer in flyback converter configuration shows that these relationships do not hold true for distributed coils.

There are three secondary windings shown in therefore using a primary inductance of 5mH gives a secondary inductance of 0.55mH. The circuit in has been simulated with a 1kHz square wave voltage signal applied to the primary coil. The resulting traces are shown in . A 12V square wave signal applied and the primary coil is shown in the yellow trace in . During the on time the coil primary coil has 12V across it. This causes a rising current which peaks at about 1.17A. During the on time the secondary windings show negative 4V across them. No current flows because of the blocking diode. At switch off, the primary coil is open circuit. The diode in the secondary circuit is now forward biased and current flows.

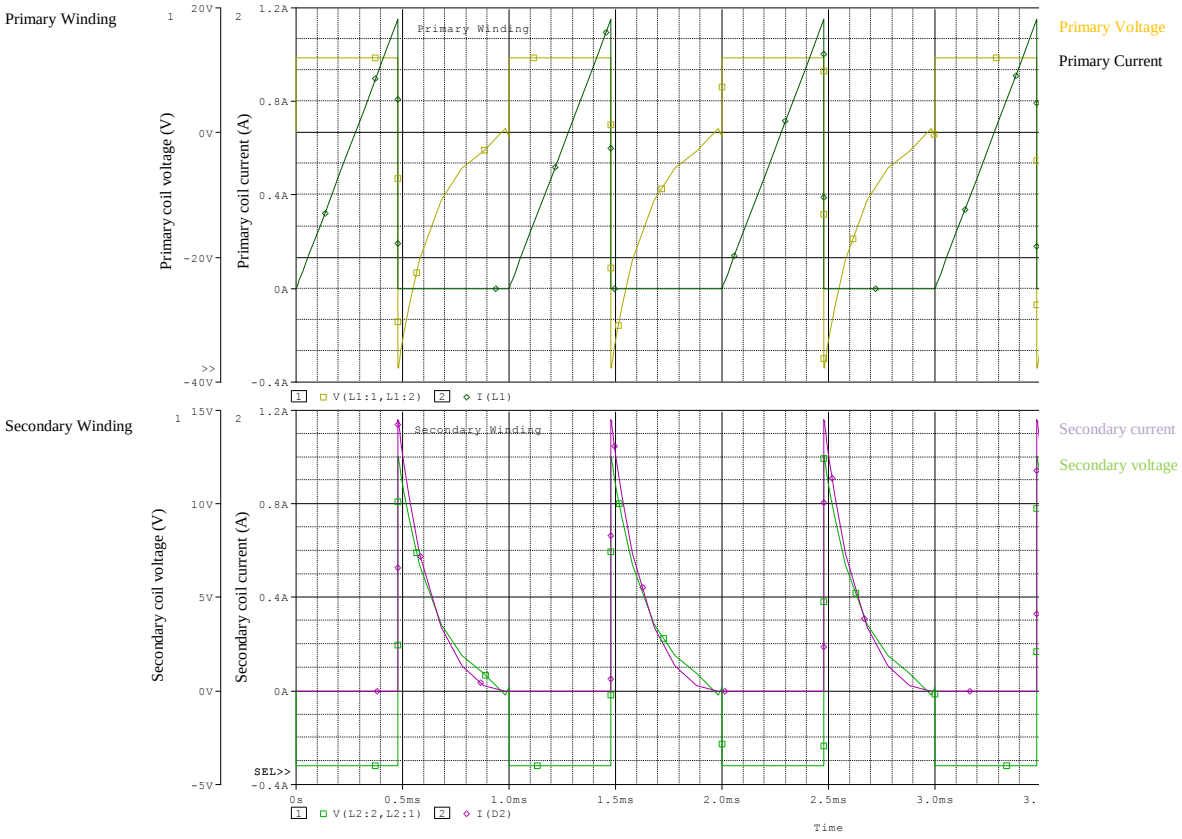

Figure 3-6 - Simulated voltage and current traces of circuit shown in with 1 kHz square wave voltage applied to the primary coil.

As the impedance seen from the transformer is equal across each of the secondary coil circuits all three secondaries have the same current profile. Because each of the secondary coils is not only coupled to the primary but also to each other, currents which flow in each of the secondary coils induce voltage in the other two secondary coils. Therefore, the peak secondary voltage is actually much higher than the simple equations above would indicate. The relationship between the coils cannot therefore be considered using the simple relationships above. The discontinuous nature of the current flow in the secondary coils means that the relationships of interest are only when the secondary coils are conducting, i.e. when the primary coil is not. This allows the consideration that, providing it is understood that only the secondary coils conducting period is of interest, the relationships between the coils may be considered continuous. This

simplification gives the relationship shown in where M_{nm} denotes the coupling coefficient between coil n and coil m.

$$\begin{bmatrix} V_P \\ V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} i_P \\ i_1 \\ i_2 \\ i_3 \end{bmatrix} \begin{bmatrix} M_{PP} & M_{P1} & M_{P2} & M_{P3} \\ M_{P1} & M_{11} & M_{12} & M_{13} \\ M_{P2} & M_{12} & M_{22} & M_{23} \\ M_{P3} & M_{13} & M_{23} & M_{33} \end{bmatrix} \begin{bmatrix} Z_P \\ Z_1 \\ Z_2 \\ Z_3 \end{bmatrix} \tag{3.6}$$

However, since there is no current in the primary coil and the coupling between each of the secondary coils is equal, and without considering the open circuit voltage on the primary a further simplification may be made as in .

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} [M_{SS}] \begin{bmatrix} Z_1 \\ Z_2 \\ Z_3 \end{bmatrix} \tag{3.7}$$

where M_{SS} is the coupling coefficient between secondary windings and Z_S is the secondary winding inductance. Since it can be assumed that the impedance of each secondary coil is equal it is therefore clear from that each secondary voltage is equal and independent of the individual coil currents but dependant on the relative magnitude of all of the secondary currents as shown in .

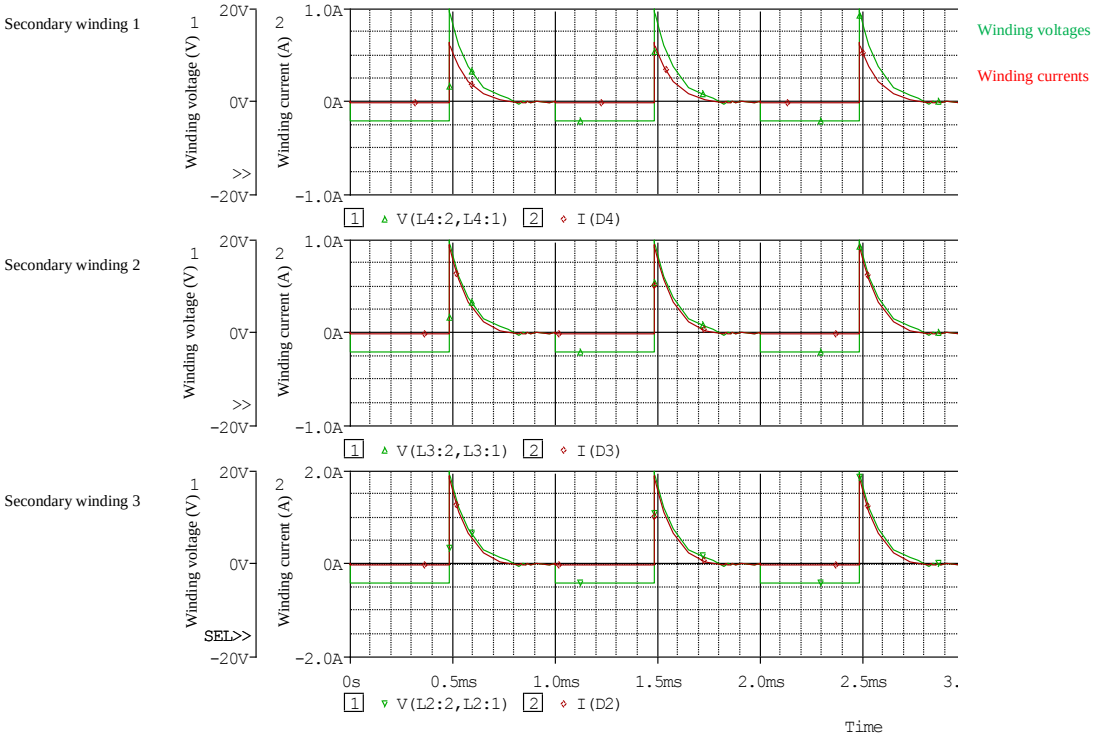

Figure 3-7 - Voltage and current waveforms of circuit in with secondary resistances of 10, 20 and 30Ω and 12V square wave primary excitation signal

3.2 Description and assessment of existing schemes

There are a number of DC-DC converter topologies which are suitable for voltage balancing. The efficiency advantages in using DC-DC converters are significant since the only losses are those suffered in the converter itself. The controllability of the converter is also a huge advantage for application optimization. As power converter component costs continue to fall it is expected that the case for investigation into viability of converters, particularly for high power supercapacitor systems, is strong. DC-DC converters are suitable for both global and neighbourly balancing schemes. Although some DC-DC converter topologies have been suggested specifically for supercapacitor voltage equalisation, there are also a number of systems for battery cell balancing which could be proposed as possibilities for a supercapacitor balancing application however the specific time constant demands of EDLC equalisation render some of these techniques inappropriate.

3.2.1 Series-parallel connection equalisation scheme [72] (Figure 3-8)

A possible objective to consider when choosing a voltage balancing scheme is the converter mass. In applications such as electric vehicles, reducing the energy storage system mass is a big concern. Voltage equalisation schemes with a large number of components, or large VA rating, of electromagnetic components – transformer cores, large inductors etc. – may be undesirable. Thus, schemes whereby voltage averaging is accomplished without these large mass components are of interest.

In [72] it is proposed that a bank of supercapacitors be arranged in such a way that allows paralleling two auxiliary stacks with the main bank on a cell by cell basis as shown in figure 3-8.

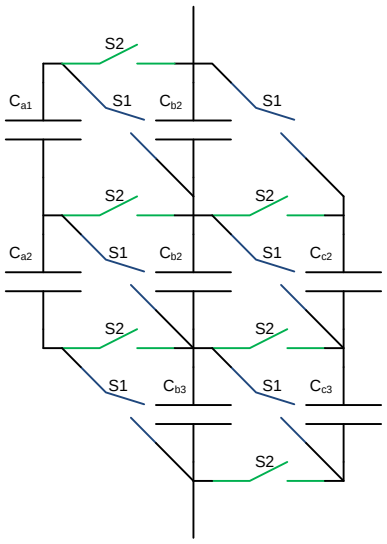

Figure 3-8 - Series-parallel connected equalization circuit

The arrangement is designed so that each capacitor has a nominal capacitance, C, with the exception of the two end capacitors in stack B, i.e. C_{1b} and C_{3b} , which have twice the nominal capacitance.

The parallel banks of supercapacitors have two functions, firstly, additional supercapacitors in the system as a whole increases energy storage capacity; secondly they act to balance each other by means of paralleling capacitors in turn.

The operation of this system is simple; the switches are grouped into two groups – S1 and S2 – which are switched alternately (figure 3-9). A dead time is included between the switching to avoid the possibility of creating a short circuit across individual cells.

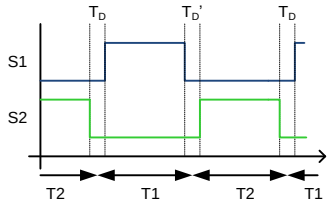

Figure 3-9 - Switching scheme for series-parallel equalisation

Once a cell is paralleled to another, the cell with the higher terminal voltage will discharge into the lower voltage cell, in the following switching step the process is repeated but crucially with a different cell grouping structure as shown in Figure 3-10. With no external charging/discharging (and assuming no self-discharge effects), after the switching sequence is repeated a number of times the cell voltages will be identical through a statistical averaging process of cell voltages.

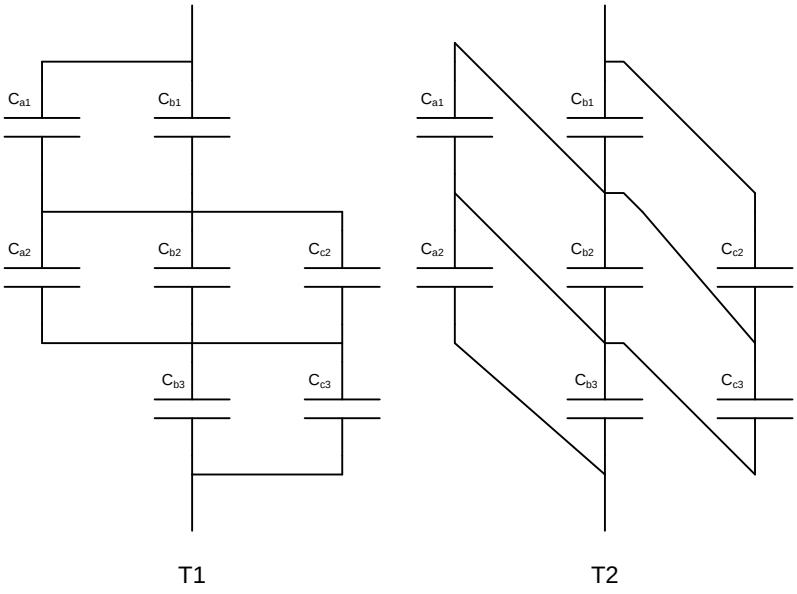

Figure 3-10 - Switching states for series-parallel equalization technique

Other advantages of this system cited in [72] are that the component count and control complexity can be driven down using this topology.

3.2.1.1 Series-parallel scheme modification – original work

In the series-parallel scheme it is necessary to have a large number of individual cells, indeed for a given stack voltage nearly three times as many cells are required. This increases the cost of the system as well as the size because supercapacitor cell volume is not linearly related to capacitance. Also, the requirement of having two capacitors in the stack which are of different nominal capacitances may pose a problem – they need to be exactly twice the capacitance.

As a modification, it is proposed by the author of this thesis that the same scheme be set up using only two stacks of supercapacitors, with all cells having the same nominal capacitance. The series-parallel connection can still be achieved through the inclusion of two extra switches on the second stack. The proposed modified topology of the series-parallel equalisation scheme is shown in Figure 3-11 with the extra switches donated as 'Sn_a'.

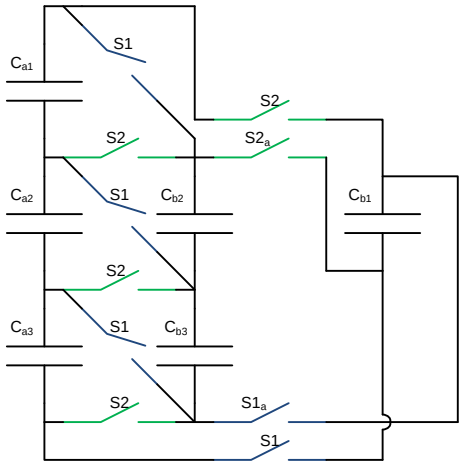

Figure 3-11 - Modified topology of series-parallel equalisation scheme

This modification has a number of advantages; firstly the same simple switching scheme shown in Figure 3-9 is retained preserving the simplicity of the scheme control. Secondly, the number of cells is reduced allowing higher capacitance devices to be used which reduces cost and volume. Thirdly, the loss associated with the equalisation current is lower since fewer switches are required overall. Lastly, all of the devices have the same nominal capacitance which, apart from having obvious component sourcing advantages, makes the scheme far easier to analyse and ultimately model.

3.2.1.2 Circuit analysis

In a parallel connection of two cells which are of unequal voltage a current flows from the higher voltage cell to the lower. The magnitude of this current is proportional to the series resistance in the conduction loop as per Ohm's law.

The modification described above has one significant drawback in that during the two switching periods not all of the parallel connections have equal series resistances. Figure 3-12 shows the switching states for the modified topology with the switch resistances represented as resistors.

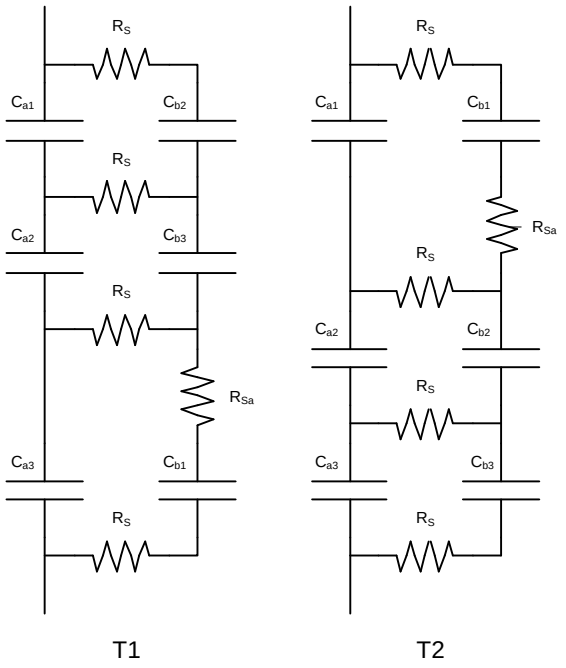

Figure 3-12 - Switching states for modified series-parallel connection equalisation scheme

Whilst the circuit in Figure 3-11 shows two parallel stacks of three capacitors, a stack of any length can be connected in this manor without increasing the number of extra switches relative to the number of capacitors - i.e. the number of 'Sn_a' switches is always two. Reducing the switch resistance of the two additional 'Sn_a' switches by using a small number of parallel switches is therefore possible without the addition of a large of number of switches even for a very large stack number. Field effect transistor (FET) switches may be arranged in anti-series connection to achieve bi-directional semiconductor switches either in a single package [73] or discretely which can be adapted for use in this application without a significant volume penalty. It is therefore assumed that the switch resistance of the additional 'Sn_a' switches can be neglected in comparison to a single switch resistance R_s. Thus the switching states can be simplified to that shown in Figure 3-13.

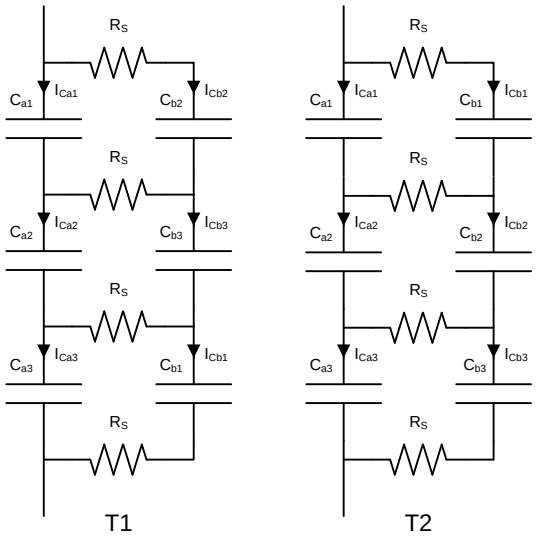

Figure 3-13 - Simplified switching states for modified series-parallel connection scheme

If a single parallel pairing of supercapacitor cells is considered then the equalisation current that flows between them is dictated in magnitude by the difference in cell voltage and the series switch resistances and in direction by the relative magnitude of the cell voltages. Thus for the two considered cells, the equalisation current is equal and opposite. Since there is no equalisation current flowing between series connected supercapacitors during each switching state each pairing may be considered in isolation. The stack current is divided in each pairing, however the additional resistances in the parallel stack (the '*b*' stack in Figure 3-13) means that slightly more stack current flows into the primary '*a*' stack cells, however the difference is small as shown below.

3.2.1.3 Circuit simulation

The cell simulation of the series-parallel circuit may be accomplished by considering the current of each cell. The cell current may be split into two components; the equalisation current which arises from a difference in cell voltage and the stack current. The cell current is the sum of these component currents. Considering a system of four cells – the minimum number of cells that may be considered is four since each cell is associated with two cells in parallel and at least one in series – then the equalisation current is easily calculated in each switching state. For each pairing of cells, as Figure 3-14, the cell currents are calculated as in (3.8) and (3.9) .

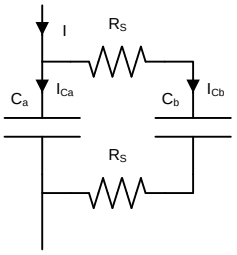

Figure 3-14 - Single pairing of parallel connected cells

$$i_{Ca} = \frac{v_{Cb} - v_{Ca}}{2R_s} + \frac{I}{2} \tag{3.8}$$

$$i_{Cb} = \frac{v_{Ca} - v_{Cb}}{2R_s} + \frac{I}{2} \tag{3.9}$$

In (3.8) and (3.9) the assumption is made that the switch resistance has negligible effect on the division of the stack current, I. This assumption is validated using a simulation of the circuit shown in Figure 3-14. The difference between I_{Ca} and I_{Cb} is extremely small and for prolonged parallel connection converges to zero. This convergence occurs because the voltage drop across C_a normalises to the voltage dropped across the two switches and the capacitor C_b. Figure 3-15 shows the difference in the cell currents is extremely small in comparison to the equalisation currents required for supercapacitor stacks showing that the assumption that the stack current is split equally between the two cells is valid. The stack current was a constant 10A, the two cells have a nominal capacitance of 2500F and the switches are assumed to have a conducting resistance of 30mΩ.

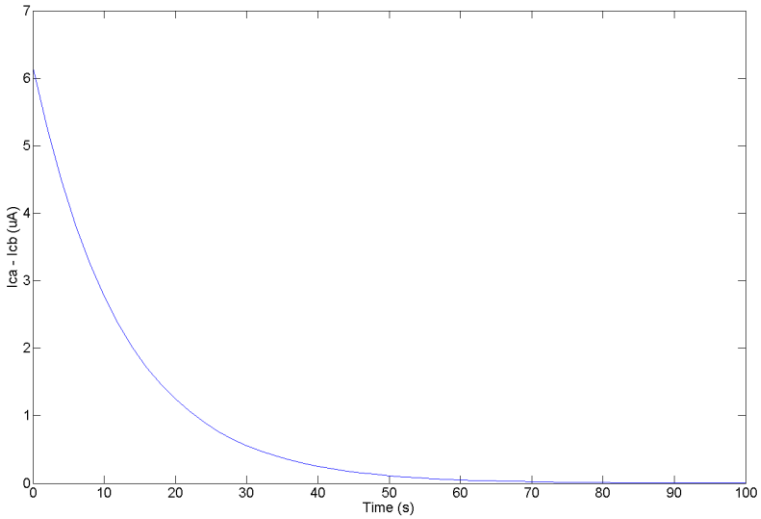

Figure 3-15 - Difference in capacitor currents for parallel connected cells

The circuit proposed in [72] (Figure 3-8) is operated at a switching speed of 100Hz where equalisation performance is reported as good. However, the authors state that the stack current is only 1.46A which is very low for supercapacitor applications. Larger stack currents expose the limitations of this scheme.

The series-parallel connection supercapacitors have been simulated using pre-set cell voltages and a range of stack currents. The simulation for the series-parallel connection scheme is based upon a stack of four supercapacitor cells. Two of the cells belong to stack '*a*' and two to '*b*'.

The effect of ever diminishing equalisation current with closer voltages means that in effect the cells must always start in a near balanced state.

This is demonstrated in Figure 3-16 which clearly shows that the scheme struggles to perform equalisation with an initial voltage difference of 0.5V even without any external stack current. The series-parallel scheme performs poorly with large initial cell voltage dispersion.

For a larger discharging current, as shown in Figure 3-18, the equalisation process is even less evident. The equalisation rates (measured as rate of change of the standard deviation of cell voltages) for the zero stack current simulation and the 10A stack current simulation are almost identical at $0.5mVs^{-1}$ showing that a small stack current does not reduce the performance any further. The performance at higher current levels is slightly better (at $1mVs^{-1}$) despite the initial voltages being closer together.

These results demonstrate clearly that the series parallel equalisaiton is not suitable for conditions where cell voltages are dispersed more than a few hundred mV. Also, an equalisation rate of $1mVs^{-1}$ is too slow to compensate for a dispersion caused by capacitor tollerances from device datasheets which confirms the statement in [72] that equalisation is possible only at low stack current levels.

The simplicity in control method and lack of magnetic components cannot outweigh this scheme's lack of suitability to a high power charging/discharging energy storage system.

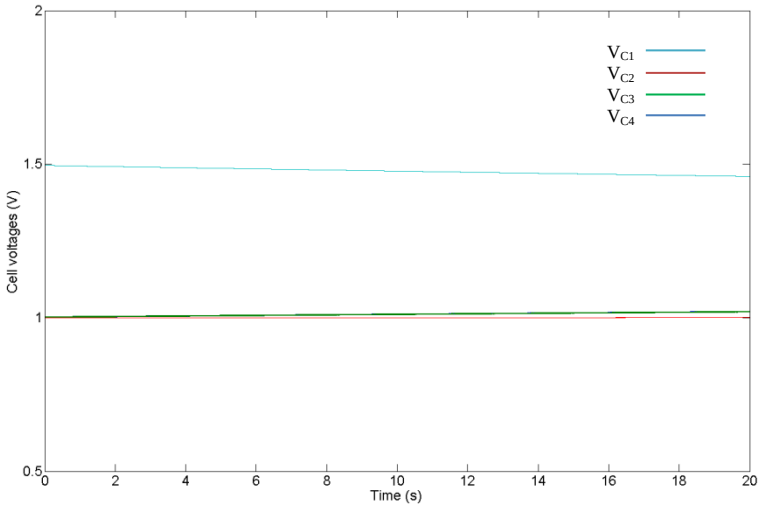

Figure 3-16 - Cell voltages with series-parallel scheme operating at 100Hz over 20s with 0A stack current – four 2700F cells. Initial cell voltages are 1.5V, 1V, 1V, 1V.

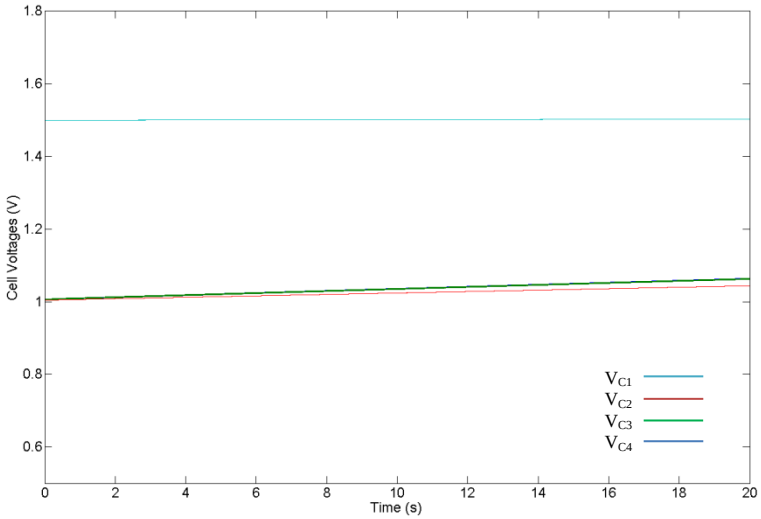

Figure 3-17 - Cell voltages with series-parallel scheme operating at 100Hz over 20s with 10A charging current – four 2700F cells. Initial cell voltages are 1.5V, 1V, 1V, 1V.

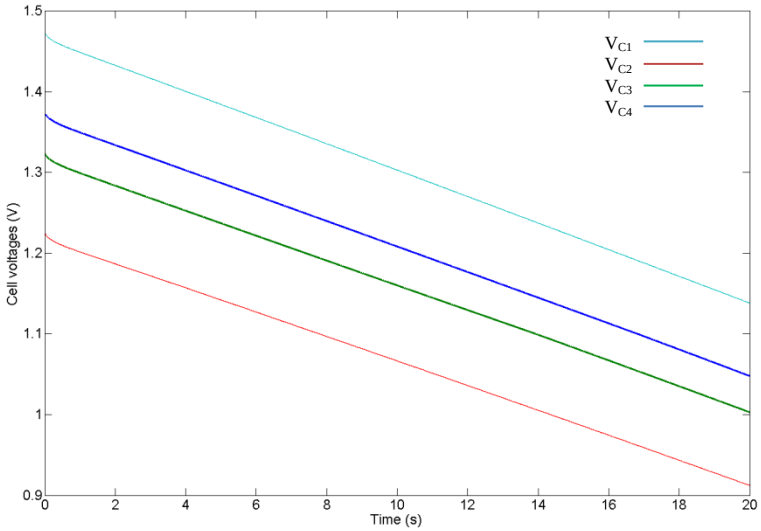

Figure 3-18 - Cell voltages with series-parallel scheme operating at 100Hz over 20s with 80A discharging current – four 2700F cells. Initial cell voltages are 1.5V, 1.4V, 1.35V, 1.25V.

3.2.2 Flying capacitor equalisation scheme [47] (Figure 3-19)

The flying capacitor equalisation scheme employs a technique outlined for battery equalisation in [47] which has been adapted here for use with supercapacitors. The principal is similar to that of the series-parallel connection scheme however rather than having two full stacks of capacitor cells where each cell is at any one time connected in parallel with one of the other stack, the flying capacitor scheme simply sequentially connects individual cells in a series connected stack with a single flying capacitor.

Figure 3-19 shows the implementation for the flying capacitor system. The principal of operation is that the flying capacitor (FC) operates as a reference voltage for the individual cells in the stacks. At steady state, the flying capacitor cell voltage will be the average cell voltage for the stack. The flying capacitor is connected, in parallel, sequentially to every cell in the stack. Since the stack cells will each have a slightly varying cell voltage, those which are at a higher voltage to the average will discharge through the switches into the flying capacitor. Cells which

are at a lower voltage to the average will be charged through the switches by the flying capacitor because it is at a relatively higher voltage. A more complex control strategy may be devised whereby specific cells are targeted – those which are furthest away from the average – to be connected to the flying capacitor more frequently. However, this advanced control method must be comprehensive since where capacitors are connected to the flying capacitor for unequal amounts of time they will receive unequal shares of the stack current.

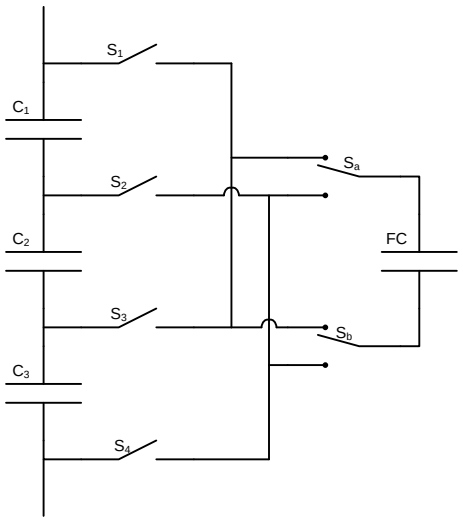

Figure 3-19 - Flying capacitor equalisation scheme

3.2.2.1 Circuit analysis

As for the series-parallel connection scheme, the equalisation current flows due to a cell voltage imbalance between two cells connected in parallel. The equalisation current is therefore limited by the switch resistance (as for the series-parallel scheme). Each parallel connection has exactly the same number of switches involved thus each parallel connection can, in terms of switch resistance, be seen to be identical when assuming the same resistance for each switch.

The stack switches, S_1 to S_n, are considered to connect to one of two busses – A or B. The odd numbered stack switches – S_1 S_3 S_5 etc. – connect to bus A and the even numbered switches to buss B. Each terminal of the flying capacitor may connect to either bus but not the same bus at the same time.

In Figure 3-20 the busses are shown including the four bi-directional switches. For the flying capacitor to be connected with each stack capacitor in turn, the switching sequence must follow a predetermined pattern. The stack switches are always closed in consecutive pairs, i.e. the two closed stack switches are always S_m and S_{m+1}. The switching sequence may be split into two states; State 1 (T1) is where buss A has a positive voltage with respect to buss B and State 2 (T2) where buss A is negative with respect to buss B. Thus T1 is defined as when *m* is odd and T2 when *m* is even.

The flying capacitor switches are operated dependant on the current state. During T1 buss A is positive with respect to buss B therefore S_{a1} and S_{b2} are closed. During T2 buss B is positive with respect to buss A so S_{a2} and S_{b1} are closed.

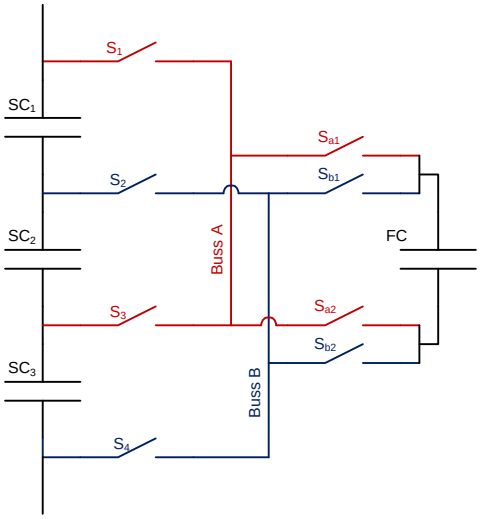

Figure 3-20 - Flying capacitor buss diagram

During both T1 and T2 there are four switches in the flying capacitor circuit and thus for either T1 or T2 the circuit can be described as in Figure 3-21.

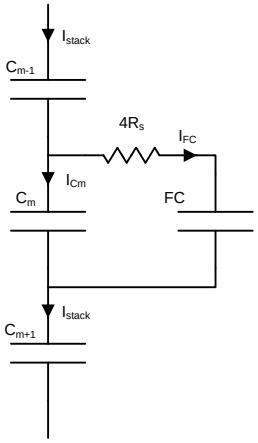

Figure 3-21 - Equivalent circuit of flying capacitor scheme

Using the same simplification for splitting of stack current as was shown to be valid for the series-parallel connection circuit, the magnitudes of I_{FC} and I_{Cm} are given as in (3.10) and (3.11).

$$i_{FC} = \frac{v_{Cm} - v_{FC}}{4R_s} + \frac{I}{2} \tag{3.10}$$

$$i_{Cm} = \frac{v_{FC} - v_{Cm}}{4R_s} + \frac{I}{2} \tag{3.11}$$

The switching sequence for a sequential connection of the flying capacitor is shown in Figure 3-22. This control scheme is very simple to implement giving advantages in cost and system

complexity. The control system and topology as a whole is also quite modular allowing greater flexibility in a final system.

The limitations of this scheme are similar to that of the series-parallel system in that the equalisation current is limited by the difference in voltage between the stack cells and the flying capacitor cell. The advantage however, is that particular cells may be targeted for equalisation rather than relying on a natural progression of equalisation.

3.2.2.2 Circuit simulation

Using the switching sequence for sequential connection shown in Figure 3-22 identical stack current simulations were carried out as for the series-parallel connection scheme with the same initial cell voltages. Figure 3-23, Figure 3-24 and Figure 3-25 show the cell voltages for stack currents of 0A, 10A and --80A respectively. For the flying capacitor scheme operating with sequential connection at 100Hz the average equalisation rates are $1mVs^{-1}$, $1mVs^{-1}$ and $0.5mVs^{-1}$ respectively. These are similar values to that of the series-parallel scheme however, the complexity of the system is less; requiring fewer cells and switches. The control logic is marginally more complex but in real terms offers no greater difficulty in development than the series parallel control scheme.

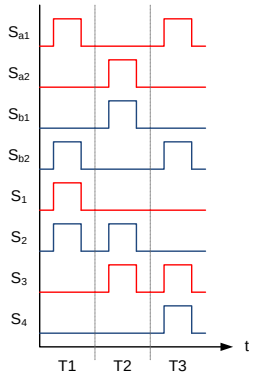

Figure 3-22 - Switching sequence for sequential connection of flying capacitor

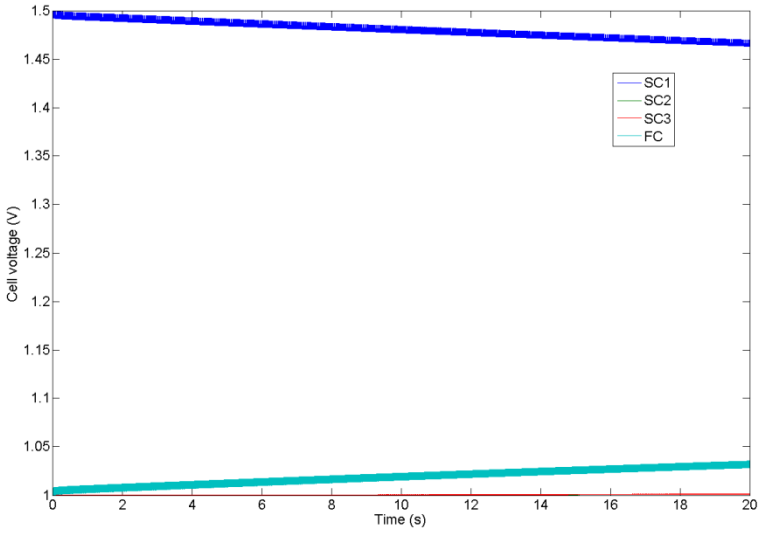

Figure 3-23 - Cell voltages with flying capacitor scheme operating at 100Hz over 20s with 0A stack current - four 2700F cells. Initial cell voltages are 1.5V, 1V, 1V and 1V

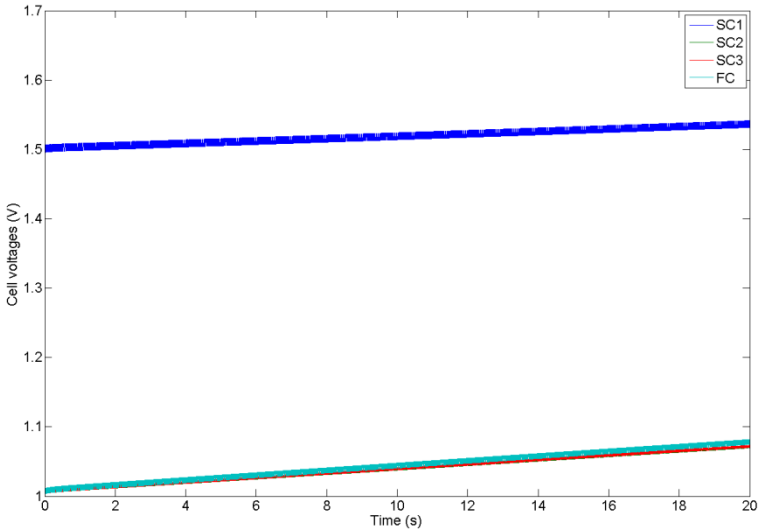

Figure 3-24 - Cell voltages with flying capacitor scheme operating at 100Hz over 20s with 10A charging current - four 2700F cells. Initial cell voltages are 1.5V, 1V, 1V and 1V

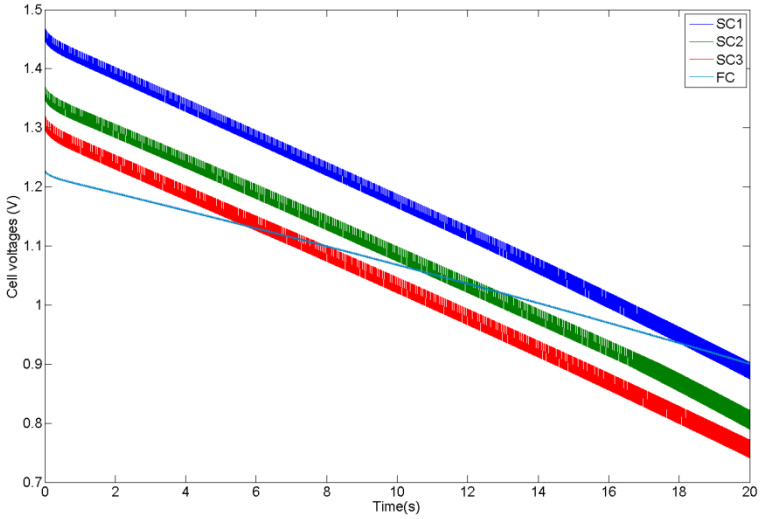

Figure 3-25 - Cell voltages with flying capacitor scheme operating at 100Hz over 20s with 80A discharging current - four 2700F cells. Initial cell voltages are 1.5V, 1.4V, 1.35V and 1.25V

3.2.3 Bi-directional buck-boost DC-DC converter equalisation scheme [48] (Figure 3-3)

One of the drawbacks of the inductor-less equalisation schemes is that they cannot be inherently designed for a specific equalisation current. This is due to the fact the constituent parts have no electromagnetic storage which means that the limitation of the equalisation rate is a function of the topology of the equalisation scheme. The equalisation current, and therefore rate, is then limited by its constituent parts – i.e. the resistance of the switches. Schemes with electromagnetic components have a design option that the inductor-less schemes lack, namely the size of the electromagnetic energy storage medium. This greatly affects the ability to stipulate a specific equalisation current.

In this equalisation scheme a bi-directional buck-boost topology is assigned to each consecutive pair of supercapacitors in the series string. This equalisation scheme uses single inductor converters and therefore belongs to the transformer-less equalisation scheme family outlined in section 3.1.2.

The bi-directional buck-boost converter equalisation scheme is one of the more developed solutions in the literature with practical implementations presented in [74] and [53]. In a single stack, each capacitor pair has an associated bi-directional buck-boost converter. Thus each supercapacitor – with the exception of the top and bottom in the stack - is associated with two buck-boost converters. With this arrangement, energy can flow from one supercapacitor to either of its neighbours.

shows the buck-boost arrangement for three series connected supercapacitors. In this arrangement when C_1 is perceived to have a smaller voltage than C_2 then T_2 is pulsed. During the on time, (when T_2 is conducting) current rises in L_1 so that I_{L1} is positive. During the off time, L_1 continues to conduct through the diode D_1. Therefore, during the on time, current flows from C_2 and during the off time current flows into C_1. In this way, energy flows from C_2 to C_1.

There is no direct route for energy to flow from C_1 to C_3, thus energy must first pass from C_1 to C_2 and then from C_2 to C_3. The effect of this is that the equalisation rate becomes a function of both the performance of the equalisation converter and the size of the stack. This can be demonstrated by assuming a worst case scenario whereby for a given stack energy must pass from the top cell in the stack to the bottom. As the size of the stack increases the number of cascaded steps of energy transfer increases. The length of time a given energy transfer between two cells therefore increases with the size of the stack.

In [48] and [74] discontinuous conduction mode is used to reduce the switching losses in the converter diodes with the balancing current levels set by the switch frequency and duty – although in [53] it is suggested that generally duty is fixed at 50% and that current flow is controlled as a function of frequency alone.

For a fixed frequency, as soon as the difference of voltages in the two adjacent cells is less than the forward voltage of the diode and given a 50% duty cycle the converter operates in discontinuous conduction mode [74].

The main advantage of this topology is the high degree of modularity of the scheme since each converter works independently of the others [48]. Modularity has two main benefits to supercapacitor stack design; it allows a varied size of stack to be created from one base unit and also allows easier and far cheaper replacement of individual cells (and their associated equalisation circuits) should a failure occur.

3.2.3.1 Circuit Analysis

The modularity of this converter allows analysis of the scheme considering a single pair of supercapacitor cells and their associated buck-boost converter. Additionally since the converter is symmetrical, energy flow in a single direction may be considered. Figure 3-26(A) shows an alternative schematic of the bi-directional buck-boost equalisation scheme for a single pair of capacitors.

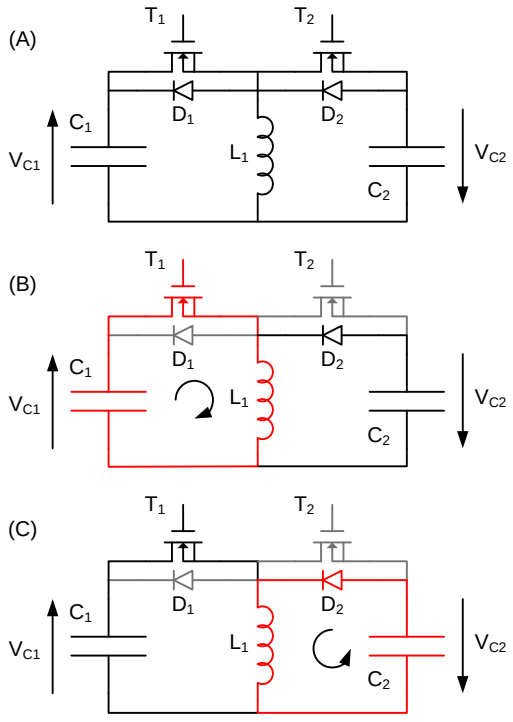

Figure 3-26 - Operation of buck-boost voltage equalisation scheme

The derivation of inductor sizing in [53] is modified here for the case shown below.

Referring to Figure 3-3, consider a situation where $V_{C1} > V_{C2}$ current must flow from C_1 to C_2. In this direction of energy flow T_1 and D_2 are the conducting components and T_2 and D_1 are non-conducting. During a single switching period, the operation of the converter may be divided

into three modes; Mode 1 ($0 \leq t \leq D_1T$), Mode 2 ($D_1T \leq t \leq (D_1 + D_2)T$) and mode 3 ($(D_1 + D_2)T \leq t \leq T$) where T is the switching period, $D_1$is the duty ratio and $(D_1 + D_2)T$ is the total inductor conduction time. The converter waveforms are shown in Figure 3-27.

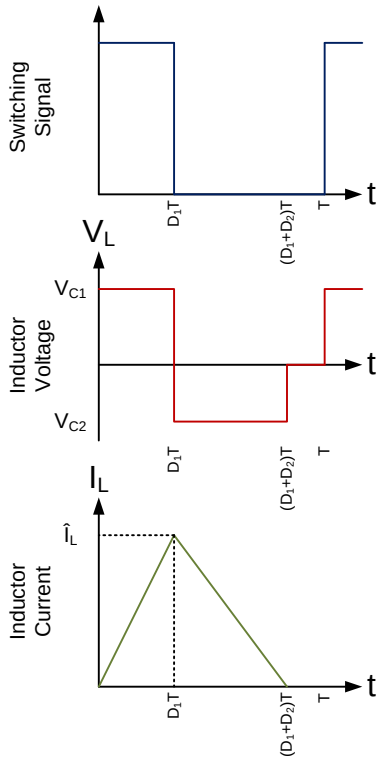

Figure 3-27 - Buck-boost equalisation converter waveforms for $V_{C1} > V_{C2}$

Figure 3-26(B) shows the conduction path during Mode 1. Assuming there is no significant voltage change in V_{C1} the peak current (at the end of Mode 1) is estimated by (3.12) .

$$\hat{I} = \frac{V_{C1} D_1 T}{L} \tag{3.12}$$

Because the converter operates in discontinuous mode, the peak current can also be given by (3.13) .

$$\hat{I} = \frac{V_{C2} D_2 T}{L} \tag{3.13}$$

During mode three there is no conduction.

In order to simplify the analysis, from (3.12) and (3.13) it can be concluded that

$$V_{C1} \cdot D_1 = V_{C2} \cdot D_2 \tag{3.14}$$

At steady state, it can be approximated that the difference between V_{C1} and V_{C2} is very small and therefore

$$V_{C1} = V_{C2} = V_C \tag{3.15}$$

Also, as the circuit operates in discontinuous mode,

$$\begin{gathered} D_1 + D_2 < 1 \\ D_1 = D_2 = \ D < 50\% \end{gathered} \tag{3.16}$$

Thus the peak current is expressed as:

$$\hat{I} = \frac{V_C DT}{L} \tag{3.17}$$

From Figure 3-27 and (3.16) the average current in the inductor can be expressed as,

$$I_{avg} = \frac{D\hat{I}}{2} \tag{3.18}$$

Substituting (3.17) into (3.18) expresses the average current as

$$I_{avg} = \frac{D^2 T V_C}{2L} \tag{3.19}$$

In [48, 74] active equalisation circuits are described in the general case as relating to one of two notional circuits. One of these circuits, which relates to the buck-boost equalisation scheme. The principal is that of current dividing whereby the aim of such a device is to deviate the charging current by means of transferring energy from the most highly charged cell to the lowest.

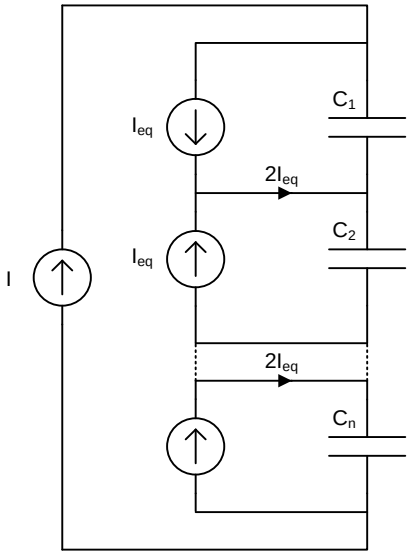

Figure 3-28 - Representation of equalisation converters through deviation of stack current

For equalisation to occur, the equalisation currents to the charging currents yields (3.20)

$$I_{eq} = I\frac{d}{d + 200} \tag{3.20}$$

For the buck-boost equalisation scheme the average inductor current is the equalisation current, $2I_{eq}$. In order to attain equalisation I_{avg} must be greater than $2I_{eq}$. Thus the inductor can be sized according to

$$L \leq \frac{D^2 T V_C (d + 200)}{2Id} \tag{3.21}$$

Since it is impractical to measure the value for d for each pair of capacitors it is assumed that these are worst case values. Supercapacitors capacitance toleration may be as 20% thus (3.21) may be estimated as,

$$L \leq 5.5 \frac{D^2 T V_C}{I} \tag{3.22}$$

Clearly the inductor size is fixed for all operating conditions therefore the control strategy must be established prior to inductor sizing. The limiting factors for the inductor sizing are the minimum cell voltage and maximum current. Thus, there are two control strategies to choose from; fixing the switching period means the equalisation current becomes a function of the cell voltage, if the switching period is varied with cell voltage the equalisation current can be fixed [53].

3.2.3.2 Circuit simulation

The relative simplicity of the inductor-less equalisation schemes means that it is possible to simulate them by simply using a signal flow model which integrates well with the supercapacitor model. It is also possible to model the circuit using a network diagram with an interface between the circuit network model and the signal flow model of the supercapacitors. The complexity of the supercapacitor models and the limitations in the circuit component models available and computing power means that it is impractically complicated and computationally expensive to attempt to model the supercapacitor equivalent circuit as a network. However, it is advantageous to use existing part libraries, which generally exist in network model form (such as SPICE models), to model complex equalisation circuits in order to make understanding of various simulated results less complex. The buck-boost equalisation system has been modelled using the network method to make the simulation simpler and to show the analysis of the equalisation circuits is possible for both signal flow and network models.

Since, as described above, the supercapacitor models exist as signal flow models an interface to a network model is required. At a high level, it may be considered that a supercapacitor is a variable voltage source whose terminal voltage is controlled via an external signal and which is able to withstand bi-directional current flow. The terminal voltage of the voltage source equates to the terminal voltage on the supercapacitor cell and the current flowing into or out of the source is the cell current. The voltage source should be considered to have a nominal internal

resistance whereby if a second voltage source is connected across the pseudo supercapacitor voltage source then a finite current flows between the two. The direction of flow is naturally dictated by the relative magnitudes of the two voltage sources but is unimportant in this analogy. The current which flows between the two sources may be measured. Since cell current is one of the inputs to the capacitor models described in chapter 2, this measured current may be fed to the supercapacitor model as a numerical signal. The supercapacitor model simply sees the current flow into the cell and outputs the relevant cell voltage – the initial voltage is a constant defined in the simulation initialisation. The supercapacitor cell voltage signal which is outputted from the supercapacitor model is used to feed back to the variable voltage source and is used to set the cell voltage. If the second voltage source is kept constant the pseudo supercapacitor voltage source will eventually match the second source. When this occurs there is no current flow between the two sources therefore there is a zero signal to the supercapacitor model and – ignoring the effects of self-discharge – the pseudo supercapacitor variable voltage source will remain constant. Figure 3-29 shows a top level diagram of the interface between the network model structure and the signal flow model structure.

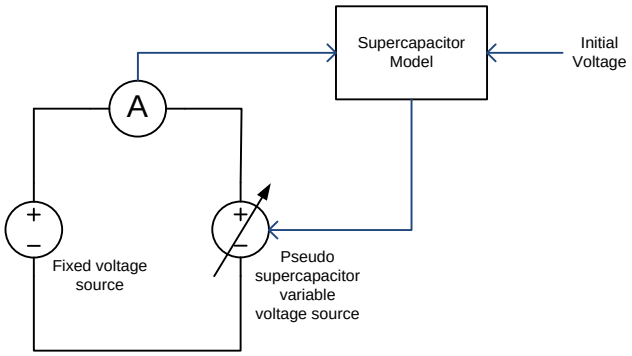

Figure 3-29 - Signal flow model/network model interface diagram

Using the method described above the supercapacitor models have been integrated into a more common network model of the buck boost equaliser as shown in Figure 3-30. The blue subsystems labelled SC1, 2 and 3 comprise the pseudo supercapacitor variable voltage source coupled with the current measurement and supercapacitor model as described above.

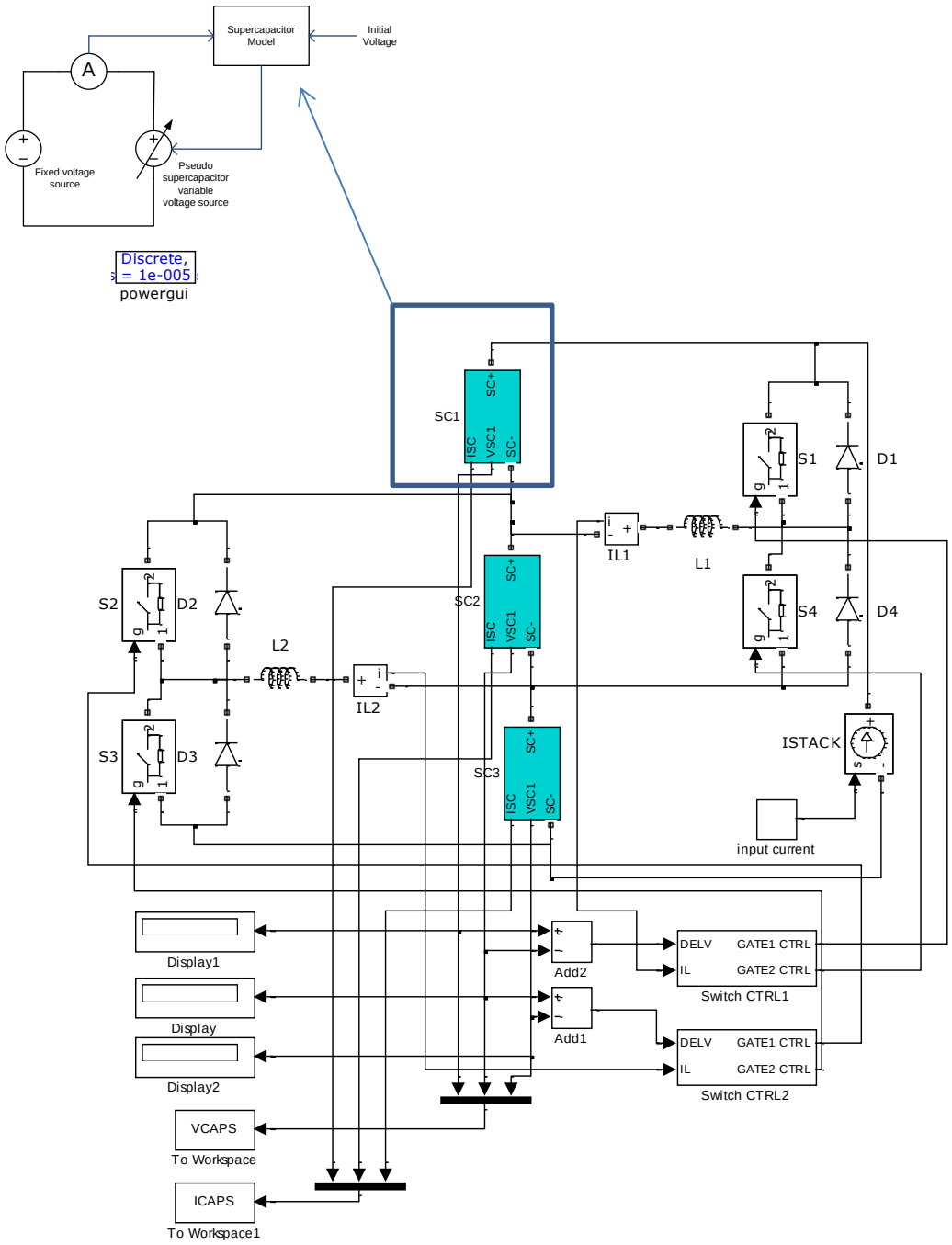

Figure 3-30 - Network model of buck-boost equalisation scheme

The buck-boost equalisation scheme has been modelled using the network model described above with three different stack currents, 0A, 10A and 80A. This allows analysis of the equalisation performance under zero, low and high stack current conditions. Figure 3-31 shows the cell voltages for the 0A stack current condition operating over 20s. The standard deviation of cell voltages decreases at a rate of $6.5mVs^{-1}$. The equalisation rate is far better than for the inductor-less cases but it should be noted that the simulation results which are based on only three cells, a necessity due to of simulation complexity and number of available cells for modelling, does not show sufficiently the effect of a much longer stack of cells.

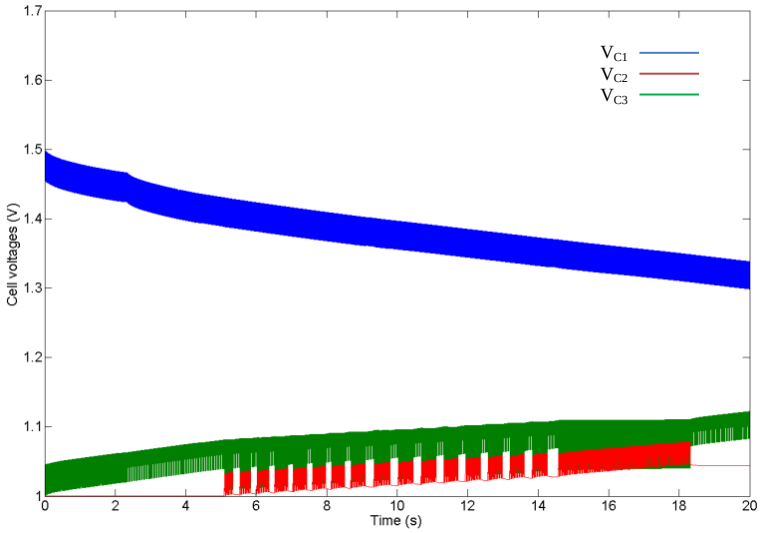

Figure 3-31 - Cell voltages with buck-boost equalisation scheme operating over 20s with 0A stack current – three 2700F cells. Initial cell voltages are 1.5V, 1V, 1V.

With a stack current of 10A (as shown in Figure 3-32) the equalisation is marginally slower however in realistic terms the small stack current can be considered not to effect equalisation time. Thus, if the circuit can be tuned to operate more efficiently through choice of inductor size and better knowledge about predicted cell parameter dispersions it is assumed that it will also operate well at low stack currents.

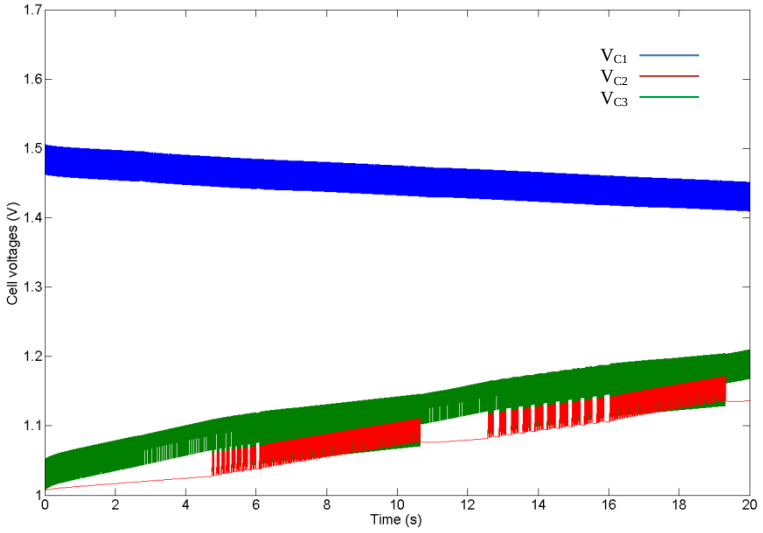

Figure 3-32 - Cell voltages with buck-boost equalisation scheme operating over 20s with 10A stack current – three 2500F cells. Initial cell voltages are 1.5V, 1V, 1V.

The higher stack current simulation results (Figure 3-33) whilst ultimately attaining equalisation – a result of closer starting cell voltages – is in fact slower giving an average change in standard deviation of cell voltages of $5mVs^{-1}$ as opposed to $6.5mVs^{-1}$ as is the case for the zero stack current simulation.

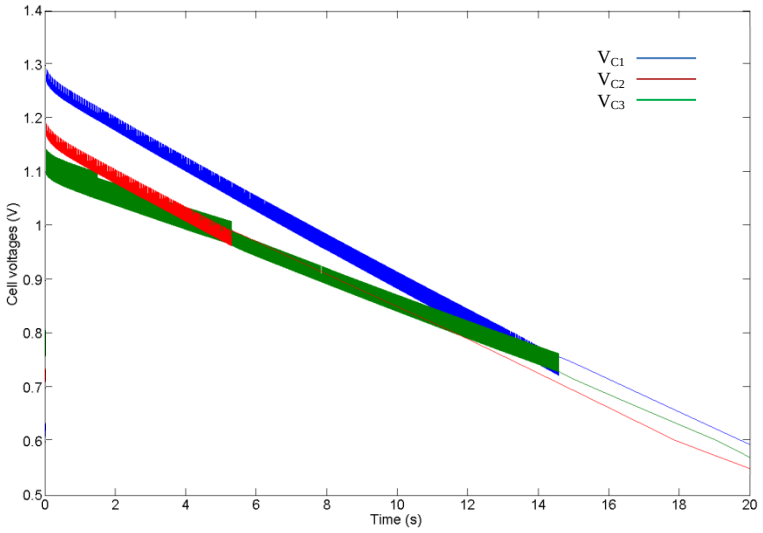

Figure 3-33 - Cell voltages with buck-boost equalisation scheme operating over 20s with 80A discharging current – three 2500F cells. Initial cell voltages are 0.6V, 0.7V, 0.75V.

3.2.4 Centralised flyback DC/DC converter with distributed secondary [48] (Figure 3-5)

The use of a multi output flyback converter for energy storage cell balancing has been suggested for both supercapacitors [48] and Lithium based electrochemical batteries [47]. The main advantage to such a system is that it employs a self-regulating centralised equalizing converter. An example with three capacitors is shown in Figure 3-34. As soon as a cell voltage is detected to be significantly different from another cell the transistor switch T is turned on. During the transistor conduction period current flows through the primary winding and energy is stored. The orientation of the secondary coils in conjunction with the diodes mean current will not flow in the secondary coils hence the energy is stored in the magnetic circuit. When T is switched off there is no electrical conduction path on the primary therefore the inverted MMF is transferred to the secondary windings transformed as a negative coil voltage allowing a current flow through to diodes to the capacitor cells. As shown above, the voltage across each of the secondary coils is equal and clamped to the lowest cell voltage through the diode. The forward voltage across the diodes is lower for cells of greater voltage hence a smaller current flows to higher voltage cells as per the conduction curve of the diode.

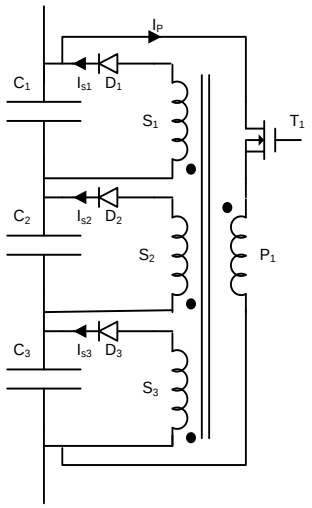

Figure 3-34 - Equalization with a flyback converter with distributed secondary winding

Although the power electronic component count in this equalization solution is relatively low the individual ratings for each component are quite high; The transistor must support the entire stack voltage and also the magnetization current which is immediately defined by the switching frequency and duty cycle of the control signal to T but more generally by the time constant associated with cell equalization since this defines the transformer sizing and hence the control signal scheme. The diodes must also support the entire stack voltage plus its associated cell voltage as a reverse bias voltage and during conduction should withstand maximum magnetizing current defined as above. The greatest disadvantage to this solution by far is the transformer itself; even moderate stack sizes would require a complicated transformer design which would likely be expensive and quite large. A solution described in [47] suggests a multiple transformer approach where each cell has its own associated transformer. The primaries of which are wired in parallel thus each core has equal MMF. The advantage of this solution is that much smaller off-the-shelf transformer devices are able to be used and system modularity is possible. However, the associated mass with any transformer based solutions deeply disadvantages the system with regards to mass and volume.

3.2.4.1 Circuit analysis

For the purposes of this analysis the transformer is firstly to be assumed to act as directly coupled inductors with equal inductances on the secondary.

Equation shows the interdependencies between the windings. The choice of relative coil sizing, duty cycle and switching period is therefore a balancing act between attaining enough equalisation current without dissipating too much energy in the diode bulk resistance due to a large forward bias voltage.

Selecting a switching frequency of 5 kHz, a primary and secondary inductance of 50µH and a duty cycle controlled to give conduction at the discontinuous limit – in this case around 0.35 – yields the voltage and current waveforms shown in Figure 3-35. The second cell which is 0.5V

greater than the other two sees a much smaller diode forward bias voltage and barely any current flows to that cell. The other two cells are at a lower voltage therefore the voltage drop across the diode is greater than the threshold voltage and thus the current which flows into them is also greater – since the secondary coil voltages are coupled and therefore equal.

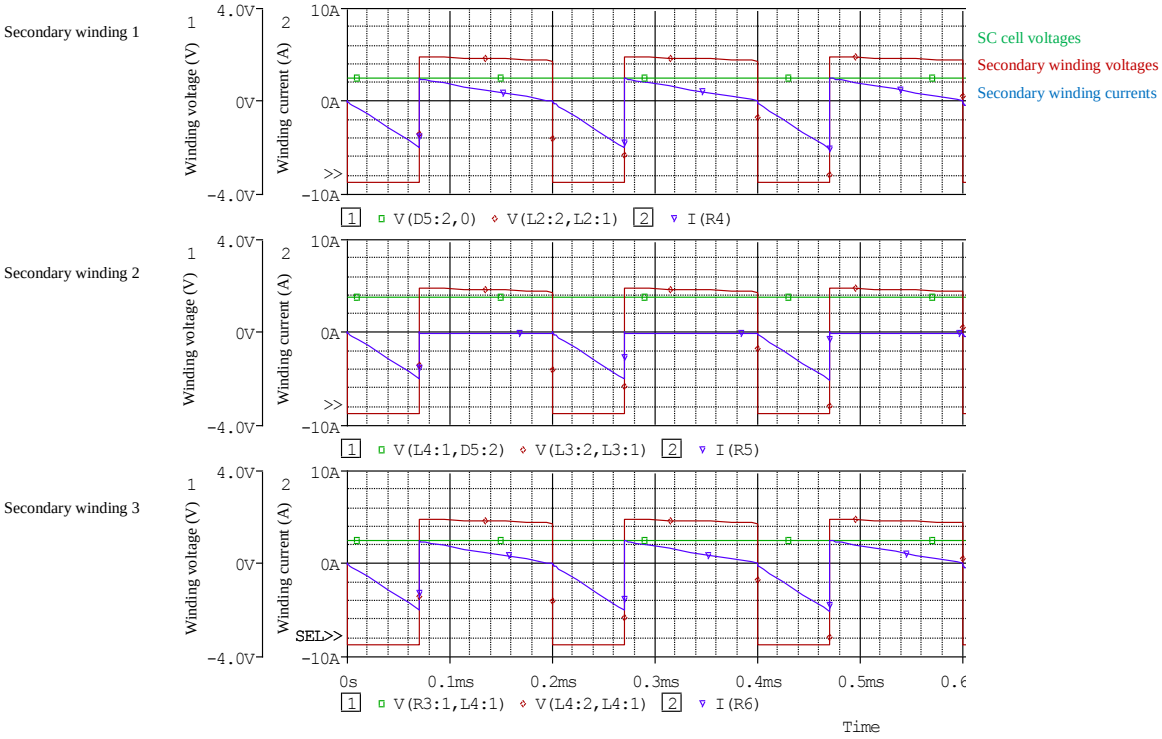

Figure 3-35 - Voltage traces for secondary windings (red) and supercapacitor cells (green) and supercapacitor current (blue) for the scheme shown in Figure 3-34 operating discontinuously at frequency of 5 kHz. Initial cell voltages; 1V, 1.5V and 1V, stack current; 0A.

Optimisation of the scheme is achieved with the understanding of the relationships in (3.6) and the effect of the bias voltage of the diode. Since the discharge current profile is common to all capacitors, clearly the optimum solution is to provide a pulse of primary current at the correct duration so as to provide maximum secondary conduction time in all but the highest voltage capacitor – which should have no conduction time. As the pulse duration of the primary increases the peak current in the conducting secondaries also increases thus the self-induced voltages in the secondaries also increases. When the voltage difference between the secondary coil voltage and the highest value supercapacitor increases beyond the forward bias voltage of the diode, the secondary with the highest voltage cell also conducts and the equalisation efficiency drops. As a design rule the effect is shown in Figure 3-36 whereby increasing the pulse length increases the charge transferred to a point where the losses in the system begin to reduce the transfer efficiency. This effect is explored in depth in chapters 4 and 5.

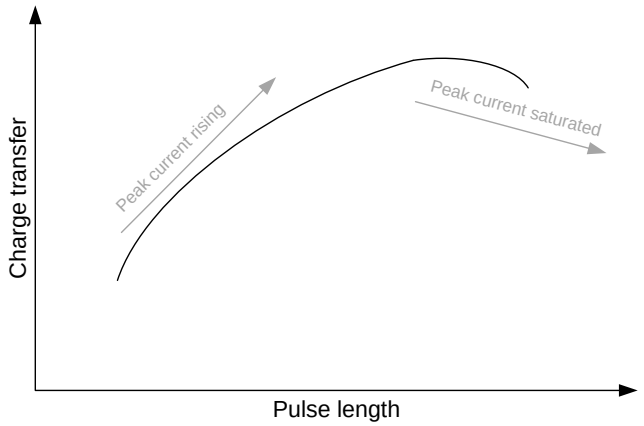

Figure 3-36 – Design consideration for the effects on equalisation efficiency from primary pulse length for the distributed flyback equalisation scheme

The effective average equalisation current is therefore not controlled by the sizing or switching frequency of the converter but the forward diode voltage drop. Since increasing the current in any one of the other secondaries also increases the voltage in all three so paradoxically the current in the highest supercapacitor voltage secondary circuit increases decreasing the peak current in the lower voltage secondaries.

The voltage and current traces in Figure 3-37 show that the primary pulse is extended to 0.1ms at which point the higher supercapacitor voltage secondary circuit begins to conduct. The value of peak current is less than one thousandth of the peak currents in the other two circuits and is considered insignificant. Increasing the primary pulse time would result in conduction in the higher voltage supercapacitor recharging what has just been discharged. Decreasing the pulse time reduces the peak current and conduction time in the lower voltage secondaries. The pulse length is therefore considered optimised for the situation where cells are dispersed over 0.5V. A higher dispersion would require a new optimisation and therefore the pulse width should be controlled either as a function of the fixed frequency duty cycle or as a variable pulse length in a variable frequency system – the latter increasing equalisation speed through reduction of non-conducting periods.

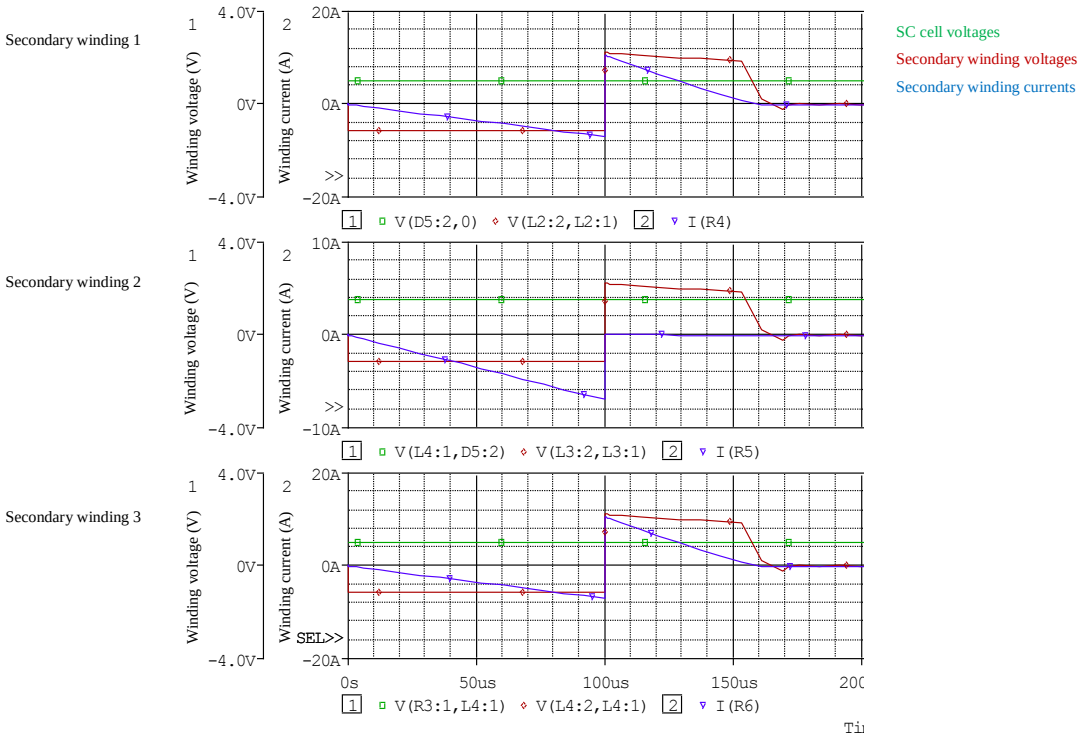

Figure 3-37 - Voltage traces for secondary windings (red) and supercapacitor cells (green) and supercapacitor current (blue) for the scheme shown in Figure 3-34. Optimised primary pulse time = 0.1ms. Initial cell voltages; 1V, 1.5V and 1V, stack current; 0A.

To achieve the same optimization at a different frequency range/pulse length the relative sizes of the transformer coils can be changed as demonstrated in Figure 3-38 and Figure 3-39. In Figure 3-38 the pulse is extended to 0.3ms requiring an increase in coil inductances by fivefold. Another fivefold increase allows the optimisation at 0.9ms. The scaling applies in the opposite direction also.

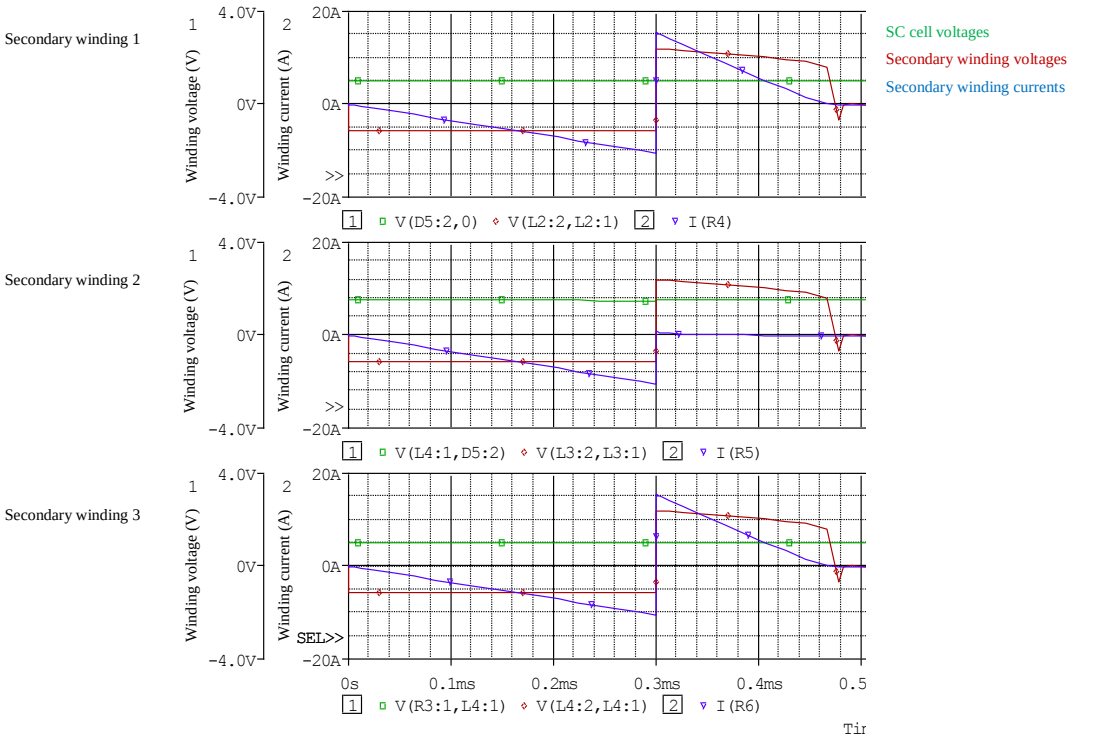

Figure 3-38 - Voltage traces for secondary windings (red) and supercapacitor cells (green) and supercapacitor current (blue) for the scheme shown in Figure 56. Optimised primary pulse time = 0.3ms. Initial cell voltages; 1V, 1.5V and 1V, stack current; 0A.

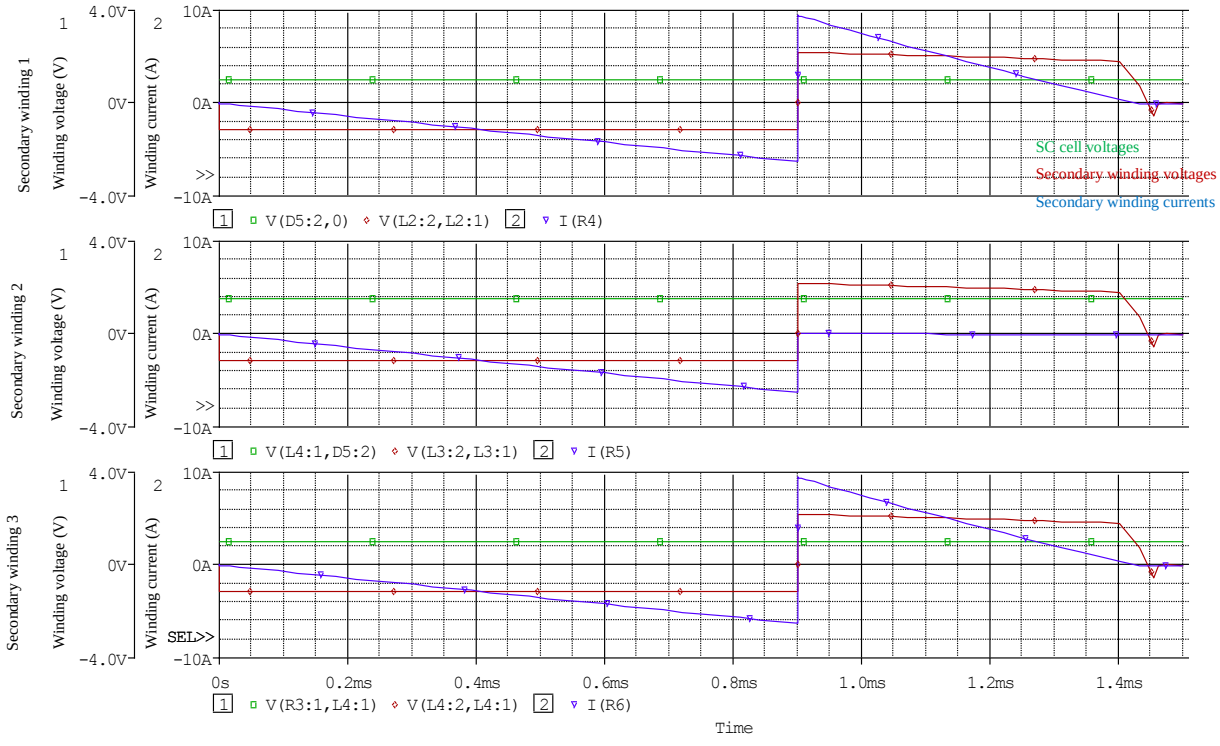

Figure 3-39 - Voltage traces for secondary windings (red) and supercapacitor cells (green) and supercapacitor current (blue) for the scheme shown in Figure 56. Optimised primary pulse time = 0.9ms. Initial cell voltages; 1V, 1.5V and 1V, stack current; 0A.

3.2.4.2 Circuit simulation

The control of this circuit can be very simply implemented using a simple logic circuit and current transducers as well as voltage measurement on each supercapacitor. The voltage measurement dynamic is not fast and therefore a moderately quick multiplexor would be adequate however, the current measurement dynamic is much faster and depending on the desired switching frequency may require dedicated measuring ports for each transducer. Variable frequency operation can simply be realised by monitoring the diode conduction time. To ensure full demagnetisation of the transformer after each switching period the currents in the secondaries must all fall to zero before the primary coil can be pulsed again. The same monitoring coupled with the identification of highest voltage supercapacitor (this would have triggered the equalisation scheme operation and requires no extra computation) allows optimisation of the primary pulse time to produce the smallest possible conduction in the highest supercapacitor voltage secondary.

The control code simply triggers a primary pulse when one of the supercapacitors is detected beyond a dispersion threshold. The next pulse cannot be generated until all of the secondary coils have ceased conducting. This allows for the demagnetisation of the transformer core. The length of the new pulse is controlled by measuring the error from zero of the highest supercapacitor voltage secondary peak current. If no current had flowed then the pulse may be increased, if the peak current that flowed was beyond a notional, small level the pulse length would be decreased. This is automated through a PI controller feedback system. The scheme can be augmented to cease production of the new pulse with the addition of a counter which does not allow the new pulse if the time between the first diode current and the last diode current falling to zero is within a narrow margin. This simulation however is simply designed to show the speed at which equalisation occurs and therefore uses the simpler control to conserve computation time.

Fixed frequency operation would simply have a variable duty which was controlled using the same feedback from the diode conduction times. Fixed frequency, as described above has two disadvantages, firstly there is a limit on the maximum duty since the core must be demagnetised (this would be achieved using an additional demagnetising coil) and the non-conducting time is likely to be higher making equalisation slower.

As with the transformer-less schemes, the distributed flyback equalisation scheme has been simulated under zero stack current, 10A charging and 80A discharging. The circuit has been optimised to give maximum current in the lower voltage secondaries with negligible positive current in the higher voltage secondary.

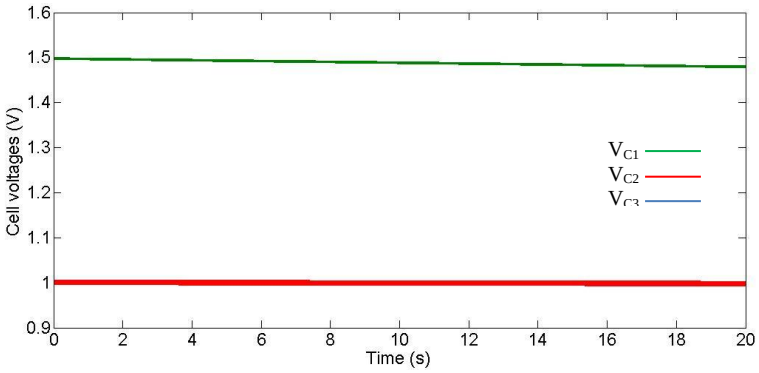

Figure 3-40 - Cell voltages with distributed flyback equalisation scheme operating at 5 kHz over 20s with 0A stack current - three 2700F cells. Initial cell voltages are 1.5V, 1V and 1V

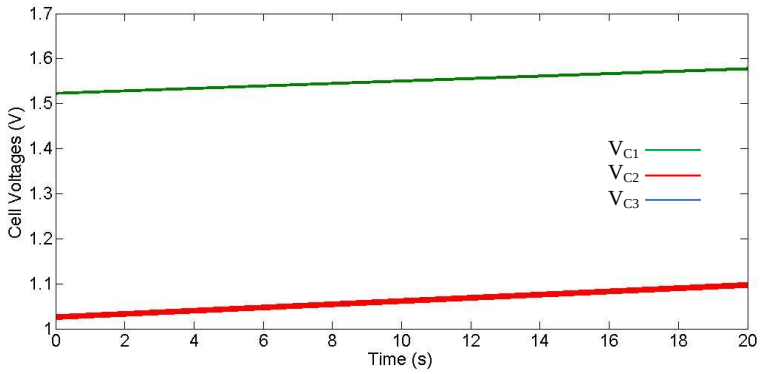

Figure 3-41 - Cell voltages with distributed flyback equalisation scheme operating at 5 kHz over 20s with 10A charging stack current - three 2700F cells. Initial cell voltages are 1.5V, 1V and 1V

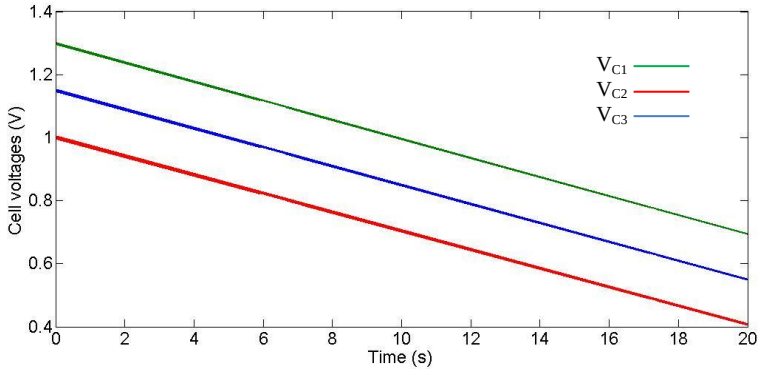

Figure 3-42 - Cell voltages with distributed flyback equalisation scheme operating at 5 kHz over 20s with 80A discharging stack current - three 2700F cells. Initial cell voltages are 1.5V, 1V and 1V

The 0A, 10A and -80A stack current simulations show that for the voltage dispersion over 0.5V the equalisation scheme achieves an equalisation speed of around 0.5mV/s for both the 0A and 10A case. The -80A case performs worse equalising at a rate of 0.28mV/s.

The equalisation speed of this scheme is severely hindered by the requirement of discharging the stack in order to energise the transformer magnetic field. This discharge applies to all supercapacitors in the stack and therefore the lower voltage supercapacitors need to be recharged as much as possible without the higher voltage supercapacitors being charged. The inefficiencies of this discharge/charge behaviour is what leads to the slow equalisation schemes.

3.2.5 Forward DC/DC Converter with Distributed Primary

Although similar in topology to the flyback converter described above, the distributed forward converter (shown in Figure 3-4) effectively changes the energy flow through the converter to combine a direct cell-to-cell energy transfer and cell to stack conversion. The flow of energy for balancing is not deviated from the charging supply (or stack energy storage). Energy from overcharged capacitors is transferred, via the converter and distributed across the entire stack.

As a supercapacitor is detected to have charged/discharged to a voltage above a threshold value beyond the average voltage levels of the rest of the supercapacitors in the bank, the associated switch is turned on. The energy is immediately transformed to the most distributed (lowest potential) other coils via the core and to the capacitors via the diodes. In this way there is no intermediately energy storage in the transformer. The non-zero forward voltage drop on the diodes requires the coil N_f (Figure 3-4) to de-magnetize the core when the switch is turned off and current has stopped flowing to capacitor cells.

This method also has the advantage that energy is automatically be transferred from an over charged cell to cells that are most distributed, thus the global efficiency of the balancing system is greatly increased. However, since the core is common to all capacitors, only one energy transfer may take place during one switching period.

3.2.5.1 Circuit analysis

The distributed primary configuration of the circuit is an interesting concept since in theory it allows there to be no intermediate energy storage; when the switch is closed, the highest cell voltage appears equally across each of the primary windings. Therefore, a forward voltage appears across the diodes of the lower voltage supercapacitors and current flows. Clearly, the disadvantage is that the higher voltage supercapacitor must be greater in voltage than the lower voltage cells by more than the forward bias voltage of the diode. The effect is demonstrated in Figure 3-43 where the highest voltage supercapacitor is only 0.5V higher than the other cells. The forward bias voltage, 0.6V, is greater than the voltage difference between the primaries and the lower voltage cells thus no current flows. This limitation means that the smallest voltage difference which can be achieved by this equalisation scheme is the same as the forward bias voltage of the diodes. Typically this value is greater than 0.5V and therefore the smallest voltage difference is 20% of the maximum cell voltage. In itself this limitation brings into question the validity of this equalisation scheme, however, the equalisation current, like the buck-boost converter, is a function of the inductor value and switching frequency and therefore theoretically will be much faster than the flyback or inductor-less alternatives.

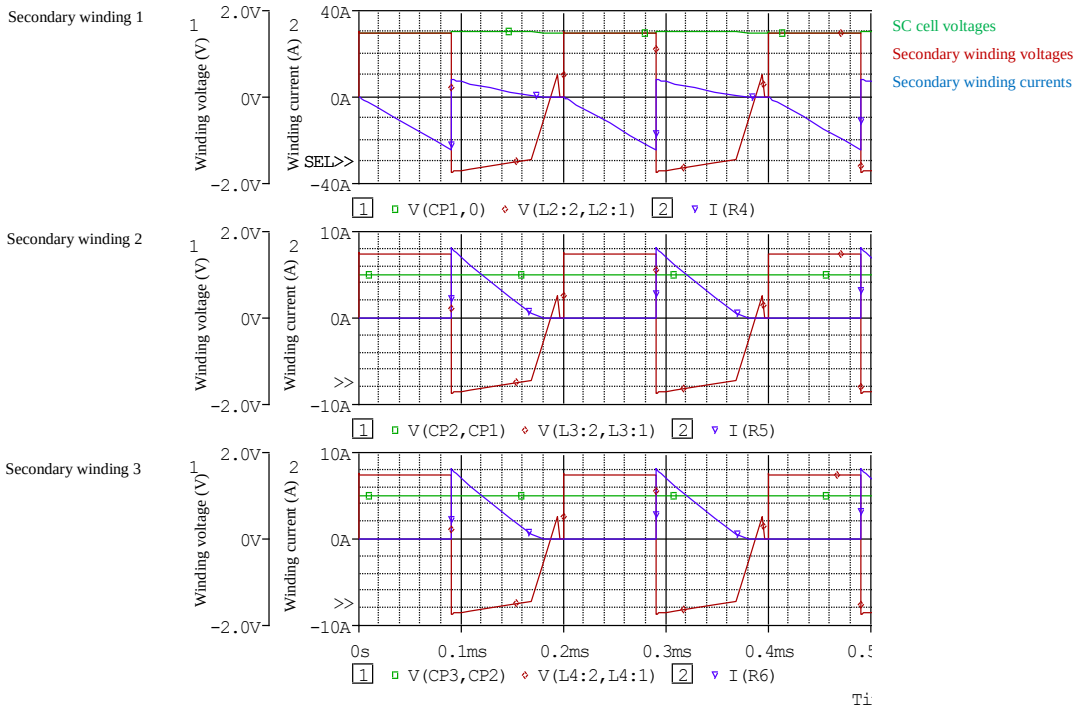

Figure 3-43 – Voltage traces for primary windings (red) and supercapacitor cells (green) and supercapacitor current (blue) for circuit shown in with C_1 = 1.5V and C_2 and C_3 = 1V. T_1 switching at 5 kHz with a duty of 0.45

Increasing the voltage differential to 1V yields the waveforms in Figure 3-45 showing that the increased voltage differential across the diode permits a current flow of around 5A in the lower voltage primary windings.

Unlike the flyback converter from 3.2.4 the consideration of the current in the supercapacitor side coils inducing a higher voltage in each other is no longer relevant since the switching coil (N_{p1} in this case) is clamped at the cell voltage. Thus, increasing the current in the switching primaries will not overcome the problem associated with the forward diode voltage described above.

The switching signal for T_1 is described as in Figure 3-44 where the on-time (switch conducting) is T1 and the off time is T2.

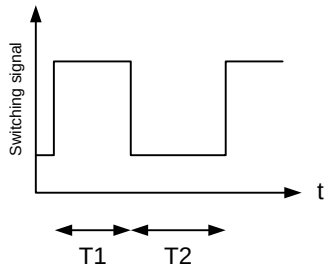

Figure 3-44 - PWM switching period

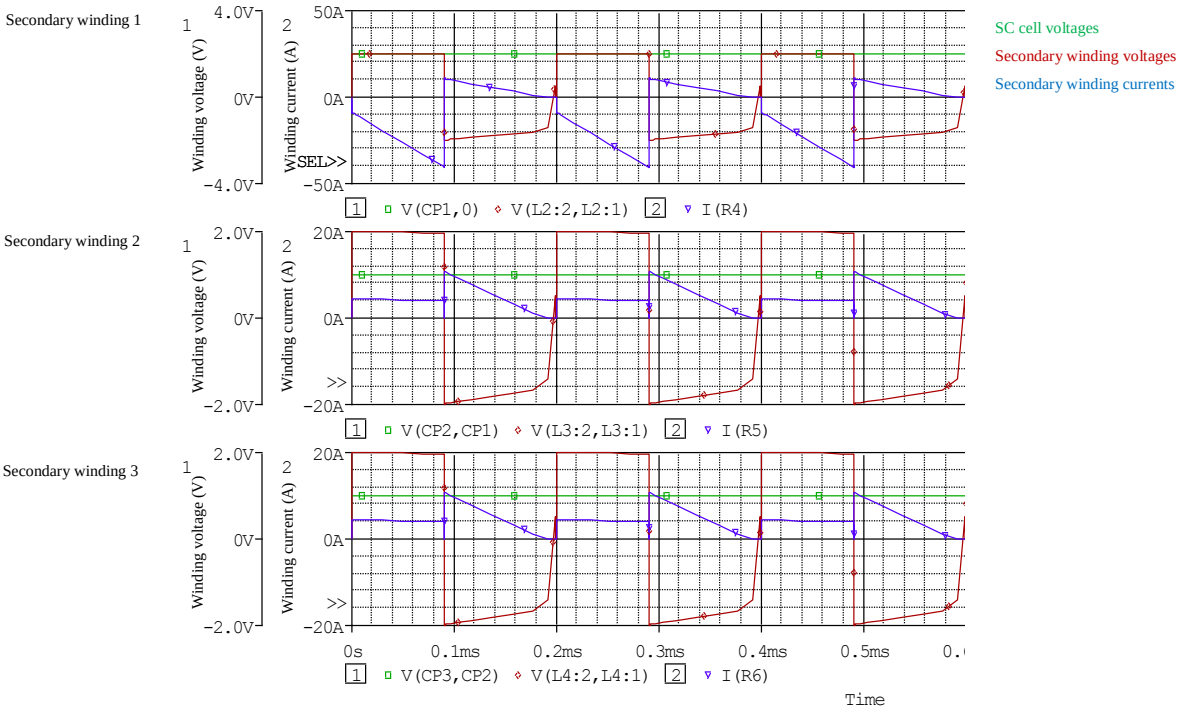

Figure 3-45 - Voltage traces for primary windings (red) and supercapacitor cells (green) and supercapacitor current (blue) for circuit shown in Figure 66 with C1 = 2V and C2 and C3 = 1V. T1 switching at 5 kHz with a duty of 0.45

One significant advantage of this forward converter topology over the flyback converter is that only the target (highest voltage) supercapacitor is discharged during T1. Also, the magnitude of this discharge current is not dependant on optimising the circuit for efficiency rather the maximum discharge current can be controlled via the switching frequency and coil sizing.

The predominate mechanism for equalisation in this scheme is the discharge of the high voltage cell. The charging current during T1 of the lower voltage cells is relatively low compared to the magnitude of the discharge current for the discharging supercapacitor. The stack charging during T2 stack demagnetisation is common to all cells and in fact does undo some of the discharging of the higher voltage cell however it also augments the charging of the lower cells from T1.

3.2.5.2 Circuit simulation

The choices available for management of the energy flow in this control scheme are more numerous than for the other schemes described above. Like the buck-boost and flyback schemes the advantage in variable frequency control allows the equalisation current to be controlled. This can be as a function of the voltage dispersion across the stack, the absolute cell voltages, the stack current or a combination of these. The most efficient fixed frequency operation fixes the equalisation current as a function of absolute cell voltage. This can be reduced to leave dead time in the current conduction waveforms however this naturally reduces equalisation speed. Therefore a fixed frequency solution with a fixed duty at just less than 50% gives the fastest fixed frequency equalisation.

The choice of which cell to discharge also leads to interesting questions; the simplest scheme would be to simply target the highest voltage cell at each switching period. This, of course would lead to equalisation however for cases where one or more is significantly lower in voltage to the others or where two or more are significantly higher targeting the higher voltage cells together by alternating the switching between the two (or more).

For simplicity, the scheme has been modelled using a simple controller which targets the highest voltage cell only. The duty cycle is lowered slightly to allow a voltage reading to take place when the demagnetisation current falls to zero. The circuit is designed to give a realistic value of equalisation current; the peak primary current of around 80A when the cells are at maximum voltage.

Figure 3-46 shows the voltage trace for the forward converter operating under 0A stack current. The equalisation rate for the 0A, 10A and 80A stack currents is 2.5mVs^{-1}.

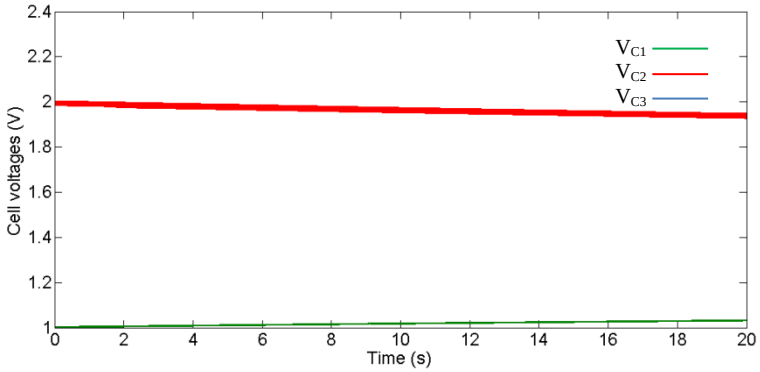

Figure 3-46 - Cell voltages with distributed forward equalisation scheme operating at 5 kHz over 20s with 0A stack current - three 2700F cells. Initial cell voltages are 2V, 1V and 1V

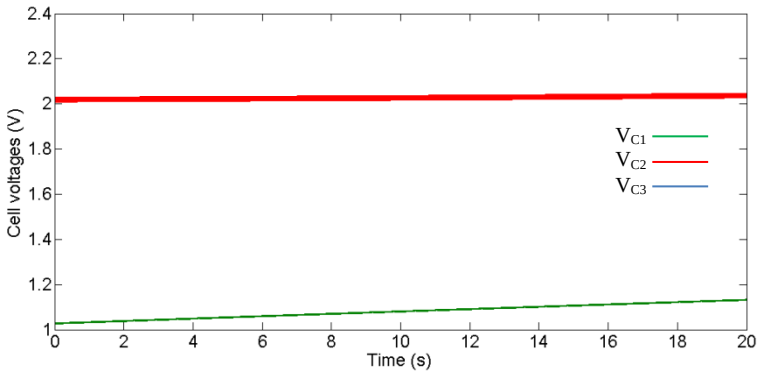

Figure 3-47 - Cell voltages with distributed forward equalisation scheme operating at 5 kHz over 20s with 10A charging stack current - three 2700F cells. Initial cell voltages are 2V, 1V and 1V

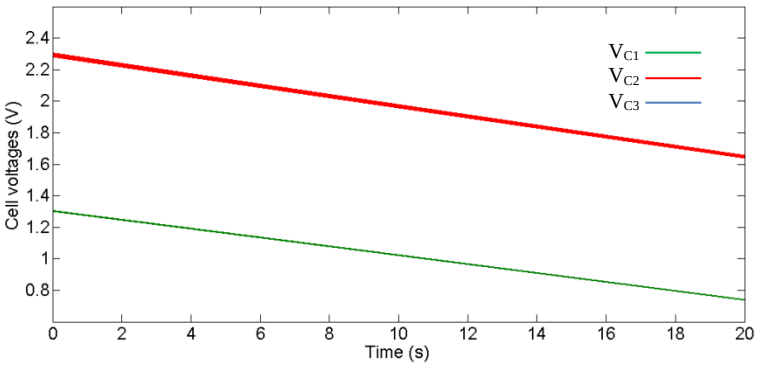

Figure 3-48 - Cell voltages with distributed forward equalisation scheme operating at 5 kHz over 20s with 80A discharging stack current - three 2700F cells. Initial cell voltages are 2.3V, 1.3V and 1.3V

3.3 Summary of existing equalisation schemes

The supercapacitor energy storage system is uniquely placed as an excellent storage system for the medium and short term. A supercapacitor energy storage system, like that of a battery system, usually comprises of a number of cells which are connected in series to achieve a system level voltage. This requirement stems from the limited cell voltage (usually around 2.7V) which is achievable from supercapacitor technology. The manufacturing processes and materials used in supercapacitor production result in not insignificant variations in the parameters of each cell. These varied parameters, such as equivalent series resistance or nominal capacitance, mean that in a series connected stack of supercapacitors, subjected to a common DC current, different cells will achieve different cell voltages.

A variance in cell voltage particularly over a number of charging periods could result in a situation where the stack terminal voltage is below the rated value for the stack but some of the supercapacitors have reached a voltage beyond their maximum value. Exceeding the maximum voltage of a supercapacitor cell can result in cell failure and dangerous explosion. Equally, if charging was ceased when one of the cells reached its maximum voltage the energy storage capacity of the supercapacitor system would not be being fully utilised.

Therefore, a scheme whereby the voltage of each individual cell can be controlled in order to equalise the voltages of the cells is desirable. This chapter has documented a number of equalisation schemes with different advantages and disadvantages, critically analysed them and shown results for simulation of five active equalisation circuits.

The dissipative equalisation schemes have been deemed too inefficient for use in a system which demands high energy storage efficiency – which would apply to electric vehicles for example – and have therefore not been analysed further.

The active circuits have a greater efficiency in terms of energy dissipation and have various advantages and disadvantages relating to component count and rating, control strategy and complexity and possible equalisation speeds.

The grouping of the schemes into families has been a useful addition to this work allowing an understanding of how both constituent components and energy flow paths dictate an equalisation scheme's effectiveness.

The simulation results for all schemes indicate that the equalisation speed is largely unaffected by the stack current.

Table 3-2 gives a summary of the analysis and simulation results for the active equalisation schemes.

Table 3-2 - Summary of equalisation scheme advantages and disadvantages

Equalisation Scheme	Advantages	Disadvantages
Bi-directional buck-boost equalisation scheme	• The fastest equalisation scheme at $5mVs^{-1}$ • High level of modularity • No transformer core • Choice of control schemes • Simple optimisation • Low-rated switches • Simulated equalisation speed up to $5mVs^{-1}$	• Equalisation speed limited by neighbourly sharing • High component count • High switch count
Series-Parallel equalisation scheme	• No magnetic components reduces size and cost • Very simple control scheme • Low switch ratings	• Equalisation very slow ($<1mVs^{-1}$) • Two parallel stacks required • Bi-directional switches increases component count
Flying capacitor equalisation scheme	• No magnetic components reduces size and cost • Simple control structure, can be improved to increase equalisation speed • Low switch ratings • Global energy sharing • Same equalisation speed as series-parallel with simpler circuit and fewer components	• Equalisation very slow ($<1mVs^{-1}$) • Bi-directional switches increases component count
Flyback converter with distributed secondary equalisation scheme	• Only one switch required • Control extremely simple • Global energy sharing	• Equalisation speed not significant improvement on inductor-less scheme • Transformer core adds cost, mass and complexity • Transformer must be specially constructed • Equalisation current limited by circuit architecture rather than sizing or switching control • Switch rating higher • Optimisation using current and voltage sensors increases transducer count
Forward converter with distributed primary equalisation scheme	• The seconds fastest equalisation scheme at $2.5mVs^{-1}$ • Equalisation current and hence speed is only a limitation of the transformer size • Variety of available control strategies • Fewer current transducers required compared to flyback converter	• Minimum voltage difference is the forward bias voltage of the diodes • Transformer core adds cost, mass and complexity • Transformer must be specially constructed • Switch rating higher

The forward converter has the second best equalisation rate however it has drawbacks relating to the special multi-winding transformer that must be used. This is not a common component

and will require special manufacturing. Equally, for a large equalisation current the transformer is also very large. This is disadvantageous in situations where mass and volume are at a premium – in an electric vehicle for example. Another disadvantage is that the minimum voltage difference between the capacitors is equal to the forward diode voltage. This is 20% of the overall cell voltage and is therefore a not unsubstantial minimum voltage difference.

There is good scope to improve the forward converter topology. Inserting a boost converter into the active primary would reduce the minimum voltage difference and also increase the equalisation current to recharge current ratio increasing the equalisation speed. The drawback here clearly is that a separate boost converter is then required for each primary coil, i.e. for each cell in the stack. The component count obviously increases significantly.

Purely in terms of equalisation performance the buck-boost converter is clearly the best converter topology; the main disadvantage with this scheme is that there is little scope to improve the actual circuit. Coupling the inductor cores is an option but basically has the same disadvantages as the forward and flyback converters regarding mass and cost. Depending on the required equalisation speed the topology may be adequate. The variability of control strategies makes optimisation more flexible. However, the relatively small number of cells simulated in this case means that the effect of long strings on the neighbourly type of equalisation scheme type. Extrapolation of the equalisation rate would mean that the rate becomes comparable, at worst case scenarios with other equalisation schemes for relatively low stack numbers whereas other schemes would not be so susceptible.

The flyback converter introduces all the disadvantages of the coupled coil transformer without giving any significant performance advantage. The main advantage to draw upon is the extremely simple control structure and fact there is only one active switching component. This simplicity would greatly decrease the cost of the switch and control aspects of the scheme. Fundamentally however there is a built in limit to the equalisation speed in this scheme and further development would not yield better performance.

Both of the inductor-less options perform quite poorly for such large capacitance devices; it is predicted that the performance using smaller supercapacitors would probably be better. The simplicity of these schemes is a great bonus reducing the size, cost and complexity of the equalisation significantly. Both schemes perform more or less identically however the flying capacitor is a much simpler topology with simpler control making it the logical choice over the flying capacitor scheme. There is also scope for improving the flying capacitor scheme by introducing a converter on the flying energy busses. This would negate the converter's inductor-less status but would provide slightly better performance at low voltage deltas.

Some of the presented schemes therefore have the possibility of being improved through further investigation and addition of components or control schemes.

The required equalisation speed is of course application driven, however, increasing the equalisation speed allows the supercapacitor stack to perform well at faster time constants improving the performance of the supercapacitor energy storage system and therefore should be pursued.

Table 3-3 - Simulated equalisation rates for existing converters

Rates in mV/s	Series-parallel	Flying capacitor	Buck-boost	Flyback	Forward
Static stack current	0.5	1	6.5	0.5	2.5
10A charging current	0.5	1	6.5	0.5	2.5
80A discharging	1	0.5	5	0.28	2.5

It could be argued that none of the equalisation rates look particularly successful and in light of the lack of convergence in almost all results this is accepted as the case. This is mainly due to the starting voltages being very far apart. This was done in part to give the inductor-less schemes a measurable equalisation rate (close starting voltages would have resulted in indeterminate rates). Another reason for such small equalisation rates is the large size of the test cells themselves. These were unfortunately the only cells available to the author and as such it was necessary to use them. It is sufficient to say that the results are different and measurable between the various schemes and particularly between the various families.

4 Development of an equalisation scheme from power flow principals

This chapter outlines the development of a new equalisation scheme with the motivation of increasing the utilisation of the equalisation converter. Firstly the motivation for the development of a new equalisation scheme is presented based on experience of existing published equalisation schemes outlined in chapter 3. A study of the power flow paths in an equalisation scheme is then presented representing a unique study of equalisation scheme energy flow.

A new converter and interface topology is presented in line with the new specification. Design considerations are explored extensively including the circuit analysis, operation, predicted waveforms and control scheme.

Finally, the proposed equalisation converter is simulated and conclusions drawn on its performance.

4.1 Motivation

The specific design specifications of an equalisation scheme, and their individual importance, are usually dependent on the application, however, some properties of an equalisation scheme may be considered to be desirable in general;

- Flexible equalisation rate
- Large number of energy flow paths
- Modularity
- Low volume/mass
- Readily available, cheap components

Equally, some aspects of the equalisation schemes studied in chapter 3 may be considered undesirable;

- Low maximum equalisation rate
- Low energy flow path number/flexibility
- Complex, bespoke transformers
- Lack of modularity

As has been discussed in chapter 3 the relative advantages and disadvantages of the existing published equalisation schemes vary. Often, when one equalisation scheme exhibits one of these advantages this forces it to exhibit one of the disadvantages. In order to consider the possibility of integrating as many of the desired properties with as few of the undesired properties as

possible a departure should be made from design considerations which all of the existing schemes have in common.

4.2 Analysis of the required power flow for equalisation

A property that all of the existing equalisation schemes have in common is that they treat each energy flow path identically – whether it be a global or neighbourly energy flow path is irrelevant. Aside from the inductor-less schemes whereby the equalisation rate is a limitation of the constituent components, each of the other equalisation schemes assumes that each energy flow path must be able to take the maximum power and therefore each of the possible energy flow paths are rated for this power flow. However, over time the average power flow as a proportion of the number of energy paths is not identical to the maximum possible flow because of the stochastic variance of the nominal capacitances.

Consider a generalised equalisation scheme attached to five cells whereby there is an even distribution of cell nominal capacitances over the published tolerance range (typically 20%) [75] under constant current the flow of energy is not evenly distributed.

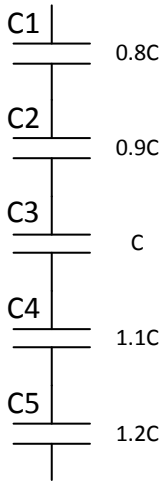

Figure 4-1 - Evenly distributed nominal capacitances across tollerance range

For equalisation to occur under a period of constant stack charging current each cell will have either a net negative or positive energy flow into the equalisation scheme. Assuming there is no loss in the equalisation converter the net energy flow for each capacitor may be seen as a function of its dispersion from the nominal rated capacitance. Over the period of charging the net energy flow equates to an average power flow to or from the individual cell that is therefore also a function of the dispersion from nominal rated capacitance. This effect is shown in Figure 4-2.

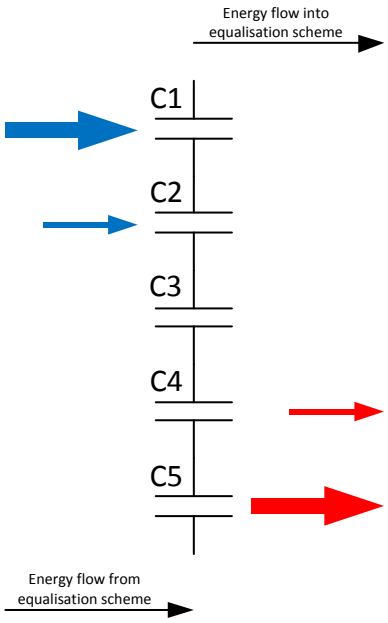

Figure 4-2 - Average power flow to and from stack in idealised equalisation scheme

Regardless of the topology of the possible energy flow paths the average power delivered to/from each cell is not constant across the stack of cells therefore rating the equalisation converter as the sum of all energy paths rated at the maximum power flow creates a power rating overhead in the equalisation converter.

There are clear advantages in being able to reduce the wasted overhead in power rating for the converter; the volume and mass of a power electronic converter is, to a large extent, a function of its power rating. To that end improvements in maximising usable power rating would lead to a lower rated, and therefore smaller and lighter, equalisation converter.

Another point to consider is that given an equalisation system with all possible energy flow paths available, i.e. a truly global energy flow path converter, and assuming it equalises the voltages in the most time efficient manner, the path with the highest average power flow would be the path between the two most dispersed capacitors. This effect can be extrapolated as shown in Figure 4-3 to a simplification of the average power flow between cells being greatest between the most dispersed and lowest between least dispersed with the capacitor with nominal rated capacitance having zero net energy flow.

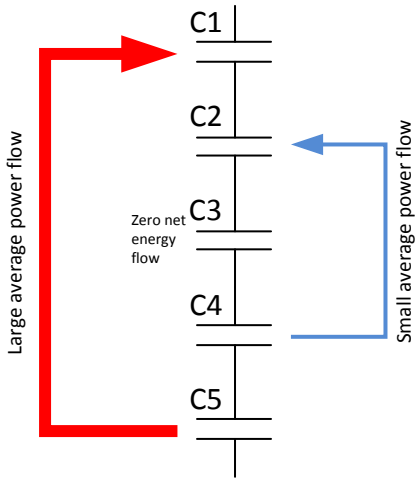

Figure 4-3 - Average power flow between cells in idealised global equalisation converter

In an ideal case the level of dispersion from rated capacitance would be known for each cell in the stack. This would allow the creation of an equalisation scheme where each energy path could be constructed and rated for the required power flow. Measurement of each cell before stack assembly is however impractical, as is constructing non-identical energy flow paths.

A compromise must therefore be reached whereby the equalisation scheme is capable of equalising the stack with any arrangement or variation of individual cells in a stack however with lowest overhead in the converter power rating.

An improved specification may therefore be created by adding a sixth point to the desired properties described above;

- Flexible equalisation rate
- Large number of energy flow paths
- Modularity
- Low volume/mass
- Readily available, cheap components
- Low power rating overhead

4.3 Proposed converter topology and operation

This section describes the inception process drawn from the improved specification and experience analysing existing solutions.

4.3.1 Stack-converter interaction

If the equalisation converter is viewed as a separate entity to the capacitor stack then its constitution may be considered to have two parts. Firstly there must be means of interaction with the capacitor stack and secondly there must be means of energy transfer.

In terms of interaction with the stack the assumption derived in section 4.2, that not all energy flow paths are required to be equally rated, unfortunately cannot be used. The reason for this is that there is no way to know the location of the variously dispersed capacitors in the stack. Instead, the interaction to the stack may be reduced to its most basic level; a bank of switches connecting the equalisation converter to any of the inter-capacitor nodes on the stack. There is no energy storage component in this interaction process it is simply a means by which to connect and isolate different point on the stack. The principal of this interaction is shown in Figure 4-4 whereby the interaction is via ideal, controlled switches. The switches are bi-directional allowing current to flow in either direction. This arrangement allows a circuit to be made isolating particular cells in the stack. For example, if C1 were to be isolated and connected to the equalisation converter in Figure 4-4 then switches S1 and S2 would be closed.

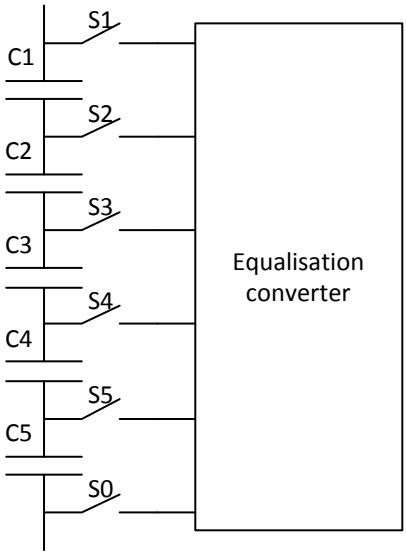

Figure 4-4 - Interaction between equalisation converter and capacitor stack

The ideal, bi-directional switches can be realised in hardware through anti-series connected FET switches as described in section 3.2.1 for the series-parallel equalisation scheme. An anti-series connected pair of FETs can be operated using the same switching signal providing the two sources are connected as shown in Figure 4-5. The FET switches are operated by applying a voltage between the gate and the source. Therefore if two sources are connected then a single differential voltage signal can be applied to operate both switches. The switches can be found in a single package as described in [73], however, for the purposes of building a prototype they are treated as two separate entities. This is useful when considering the converter operation described in section 4.3.3.

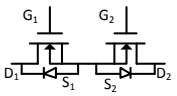

Figure 4-5 - Two MOSFET switches arranged in anti-series to form bi-directional switch (Gate, Drain and Source indicated)

4.3.2 Bi-directional, multiplexed equalisation converter

Taking equalisation of one pair of cells whereby an energy flow path exists between the two cells consider that the equalisation process in two distinct and separate time periods. These are the discharging period where the source cell is discharged into a temporary energy storage medium and the charging period where the target cell is charged from the energy storage medium. Consider also that, as discussed above, there is no way to economically know the direction that energy must flow down this energy flow path. For the purposes of economy of power flow path rating the mechanism by which the cell is connected to the equalisation scheme should be the same when the energy flow path is operating in either direction. These constraints therefore dictate that the equalisation converter is bi-directional. Moreover, since these constraints hold true for all energy flow paths the converter must also have a multiplexed input which, by the nature of the bi-directional properties of the converter, is also a multiplexed output.

Since using the above assumption regarding time periods results in a situation whereby only a single cell is ever electrically connected to the converter at any one time to complete the charging/discharging circuit requires two connections to the converter. These two connections form the interface between the bi-directional switches described in section 4.3.1 and the converter energy storage medium. For the purposes of clarity the two connections to the converter may be termed busses and named Blue and Red (Figure 4-6).

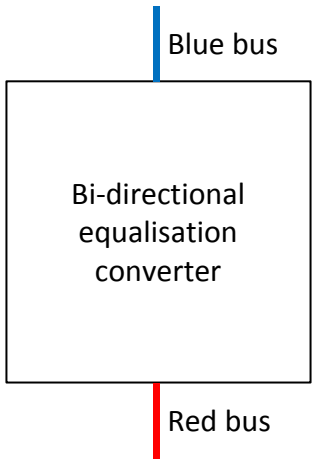

Figure 4-6 - Bi-directional equalisation converter with red and blue energy busses

If the converter is bi-directional then the current flow along each of the energy busses must also be bi-directional.

Each of the bi-directional switches connected to the stack nodes are alternately connected to the blue or red energy busses to form a multiplexor similar to the principle of the flying capacitor equalisation scheme in section 3.2.2 as shown in Figure 4-7.

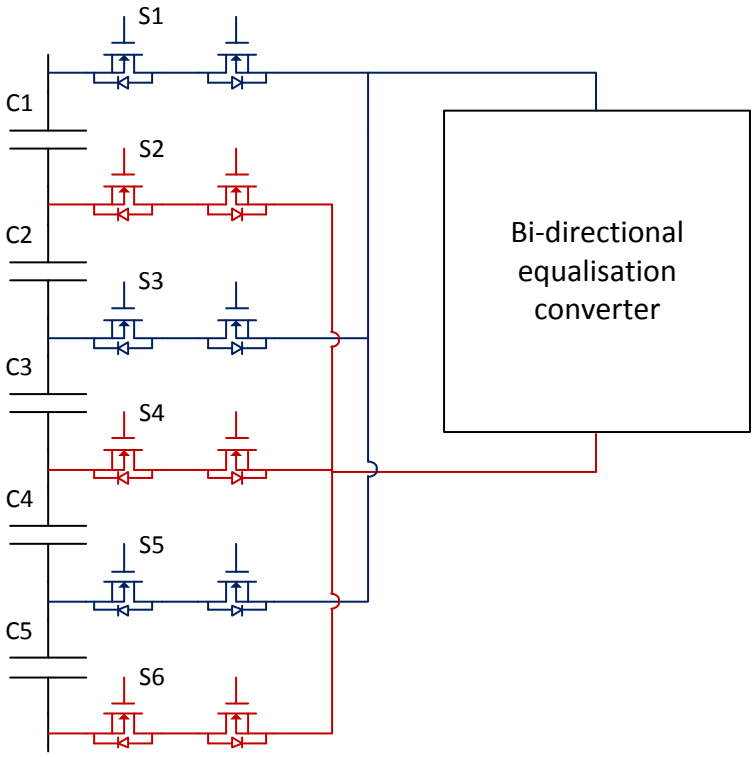

Figure 4-7 - Multiplexed input/output to equalisation converter using bi-directional switches and energy busses

By switching combinations of pairs of adjacent stack switches the differential voltage across blue to red busses is the respective cell voltage in either negative or positive polarity. This method allows direct cell connection to the converter whilst maintaining isolation of the other cells and using the smallest number of switches. It does however add a constraint to the converter properties requiring it to also be bi-polar with regard to input/output voltage.

For the purposes of simplicity, the polarity of the busses is always assumed to be measured from blue to red, i.e. if the absolute voltage of the blue bus is greater than the absolute voltage of the red bus then the polarity of the two busses is deemed to be positive and vice-versa.

The polarity of the blue-red differential voltage during the two equalisation time periods depends on the energy path considered with each individual equalising event. For example, the energy flow path which is required to discharge C1 into C5 results in positive bus voltage in both the discharging and charging time periods. The energy flow path required to discharge C1 into C2 results in positive bus voltage in the discharging period and negative in the charging period. The polarity of the busses can be shown in a lookup table for a stack of cells, an example for five cells is shown in Table 4-1.

Table 4-1 - Lookup table for bus polarity for five cells

Source cell	Target cell	T1 Bus polarity (discharging)	T2 Bus polarity (charging)
C1	C2	+ve	-ve
C1	C3	+ve	+ve
C1	C4	+ve	-ve
C1	C5	+ve	+ve
C2	C1	-ve	+ve
C2	C3	-ve	+ve
C2	C4	-ve	-ve
C2	C5	-ve	+ve
C3	C1	+ve	+ve
C3	C2	+ve	-ve
C3	C4	+ve	-ve
C3	C5	+ve	+ve
C4	C1	-ve	+ve
C4	C2	-ve	-ve
C4	C3	-ve	+ve
C4	C5	-ve	+ve
C5	C1	+ve	+ve
C5	C2	+ve	-ve
C5	C3	+ve	+ve
C5	C4	+ve	-ve

Assuming that cells are connected and numbered in the same manner as in Figure 4-7 a simplification can be made by looking at the cell designator. For an odd source cell the discharging polarity is always positive and negative for an even cell. The same is true for target cells; an odd target cell has a positive charge polarity and vice-versa. The simplification is shown in Table 4-2 and shows that the bus polarity is common to any length of stack making the proposed equalisation scheme modular.

Table 4-2 - Reduced look-up table for bus polarity

Source cell	Target cell	T1 Bus polarity (discharging)	T2 Bus polarity (charging)
Odd	Odd	+ve	+ve
Even	Odd	-ve	+ve
Odd	Even	+ve	-ve
Even	Even	-ve	-ve

The evidence from examining currently published equalisation schemes is that using electromagnetic energy storage as the intermediate energy storage facility in an equalisation

converter allows a greater degree of flexibility and greater equalisation rate than electrostatic as is shown in chapter 3. Energy stored in an electromagnetic core also has the added advantage that there are no polarity limitations as can be the case with electrostatic energy storage.

With electromagnetic energy storage as the intermediate energy storage mechanism the discharge period effectively becomes the magnetisation period and the charging period is the demagnetising period.

Assuming energy storage is accomplished with a single coil the polarity of the coil voltage during magnetising dictates the polarity of the coil during demagnetising. However, as Table 4-2 shows there is not necessarily a correlation between magnetising and demagnetising polarity. A mechanism is therefore required by which the output polarity can be selected regardless of the input polarity.

Coils coupled on the same core which oppositely orientated have opposing potentials. This effect can be used, with a coil selection method, to regulate the polarity of the output voltage. The equalisation converter can therefore be seen as an intermediate energy storage medium using electromagnetic energy storage which is realised via connection of selected coupled coils to the energy busses.

Selection of the coupled coils may be achieved in much the same way as selection of the capacitor nodes described above. Namely, a combination of switches may be used to connect the desired coil to the energy busses. An arrangement which allows this is shown in Figure 4-8 in the context of the entire equalisation scheme.

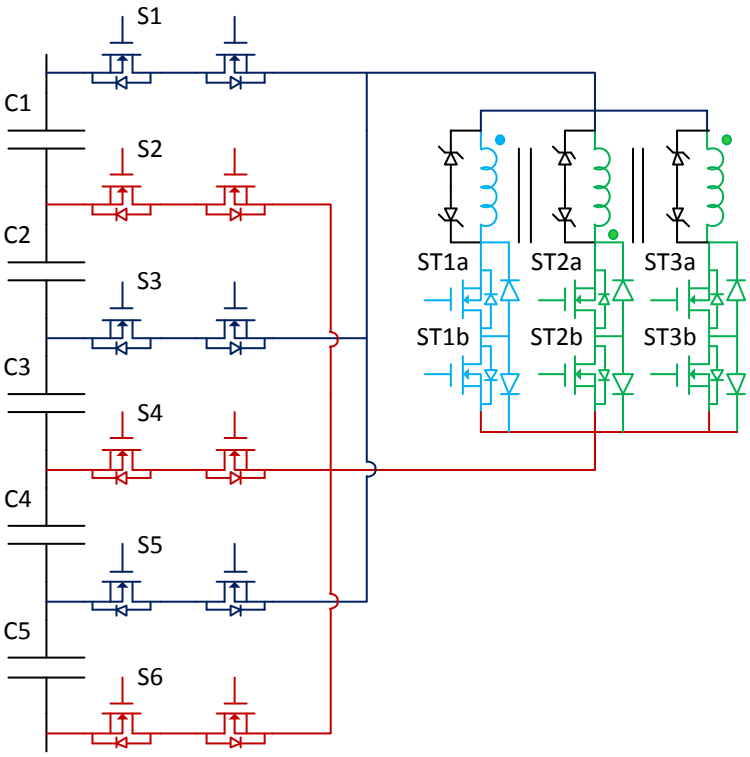

Figure 4-8 - Equalisation through multiplexed selected coil converter

4.3.3 Principles of operation

The equalisation scheme shown in Figure 4-8 operates under the principle described in section 4.3.2 whereby the equalisation occurs in two distinct periods via intermediate energy storage.

The following description of circuit operation assumes that source and target cells have been identified. For the purposes of this explanation energy is assumed transferred from C1 to C3 as shown in Figure 4-8. This initial explanation assumes idealised components.

- S1 and S2 are switched on to connect the source cell, C1, to the equalisation converter.
- A positive differential voltage (as defined above) is therefore applied across the energy busses.
- Switches ST1a and ST1b are switched on.
- A magnetising current flows through the primary (blue) winding.
- After a defined period of time S1, S2, ST1a and ST1b are switched off. Simultaneously S3, S4 and STb2 are switched on.
- The target cell, C3, is connected to the bus.
- A positive bus voltage is applied.
- Current flows from the inverted secondary (green) winding into C3.
- The secondary windings are wound so that the demagnetising current conduction period is slightly less than the magnetising current. This allows up to 50% duty cycle in fixed frequency operation.

- When the current drops to zero the parallel diode to STb1 stops any reverse conduction resulting from the potential of C3 applied across the secondary coil.
- The process is repeated as required.

The conduction paths for the above explanation are shown in Figure 4-9 and the idealised converter waveforms are shown in Figure 4-10.

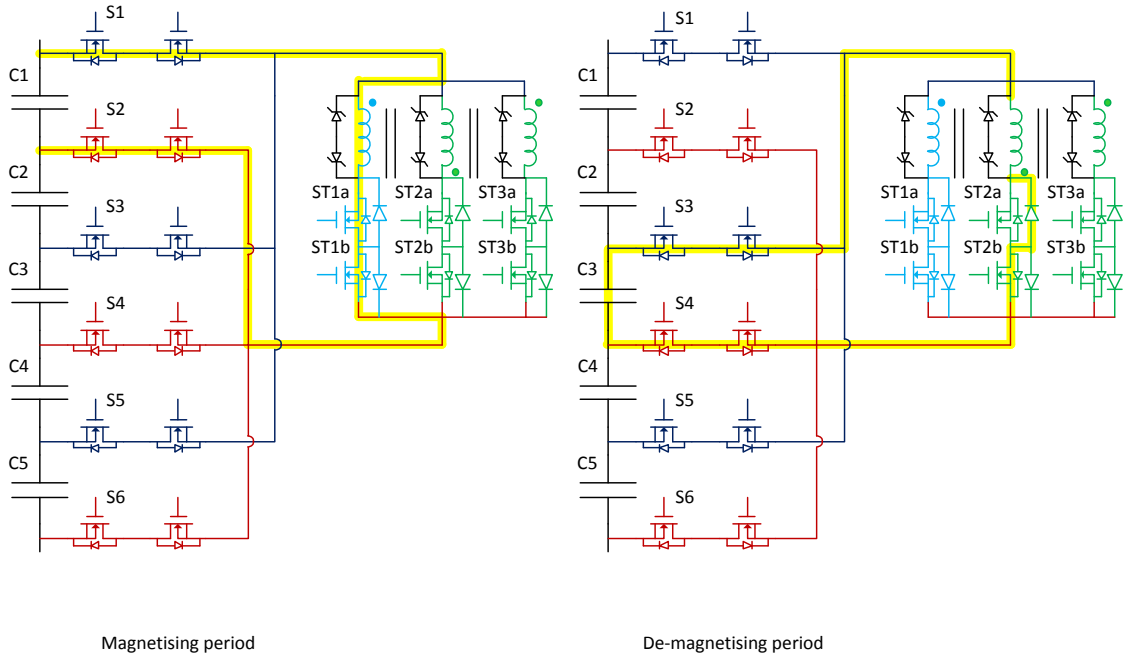

Figure 4-9 - Conduction paths relating to description of operation

The point at which the magnetising period ends and the demagnetising period begins, or commutation, requires the simultaneous deactivation of four MOSFETs and activation of three. Even with high-end gate drive electronics and microprocessor control this can never be guaranteed to be instantaneous.

The integrity of the devices is at risk for both cases of overlapping switch conduction period and for a dead-time period. If the switches conducting period overlaps then there is a capacitor short via one or other or both of the energy busses through the multiplexor depending on the switching sequence. If this is very short it is unlikely to cause damage to the capacitor cells particularly in the case of carbon-carbon EDLCs which can be shorted directly [75]. However, the MOSFET devices will suffer particularly if the abuse is repeated many times.

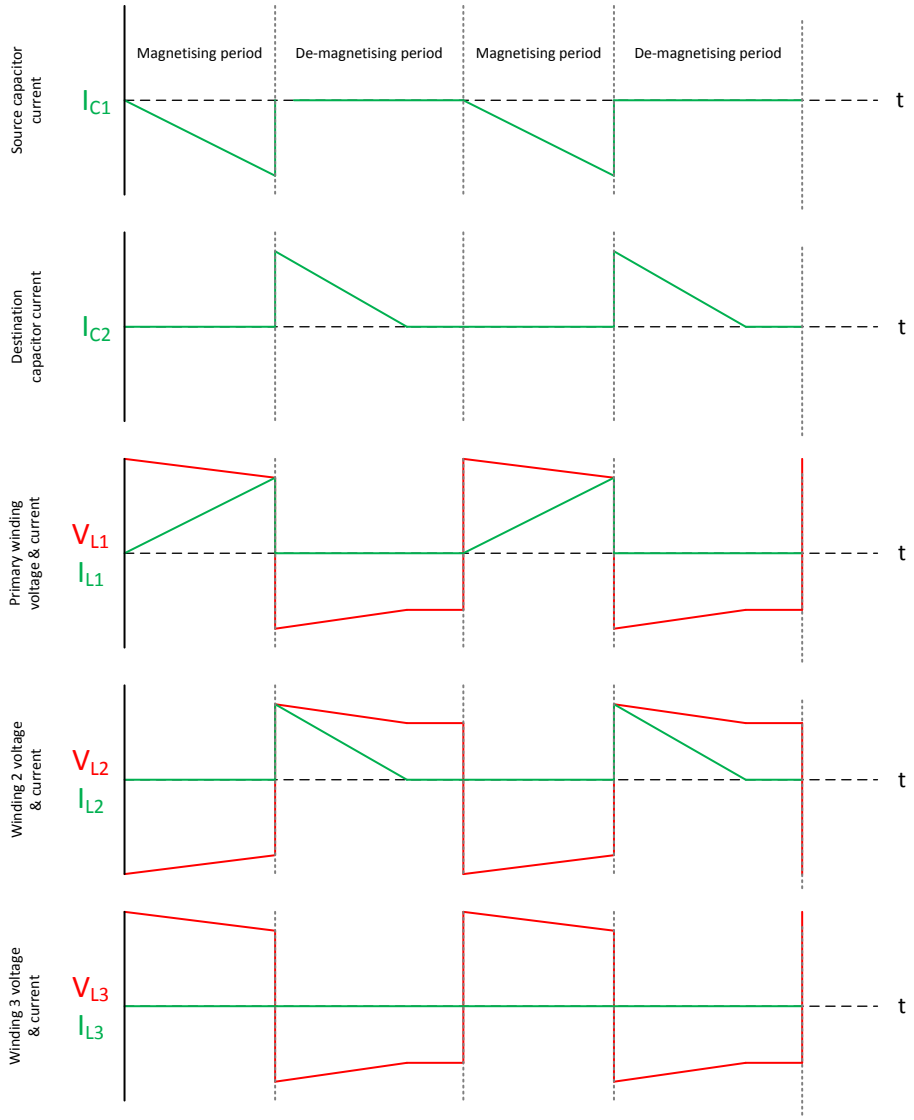

Figure 4-10 – Predicted converter waveforms

Conversely, if there is a dead-time between the conducting periods the magnetised core will cause a large voltage spike on the converter coils. This voltage could easily damage the converter switches.

To attempt to mitigate conduction time overlap a small amount of dead-time can be inserted into the switching sequence by addressing the gate drive signals from a microcontroller in two separate register writing instructions. This will be explained more thoroughly in chapter 5 along with the switching control and driver hardware.

By the nature of the speed at which the register writing instructions are carried out any dead-time in the switching signals will be small. To ensure that the gate drive circuits swing the gate voltage signal quickly and well into saturation and depletion a double-ended gate drive voltage supply will be used. Also, to arrest any voltage spikes on the coils each one has a pair of anti-series Zener diodes which are chosen to have Zener voltages well above the expected coil

voltages during normal operation but also well below voltages that might damage the transistor switches. If the coils go open circuit the voltage will rise quickly until one of the coils reaches a voltage which is the sum of the Zener voltage and forward voltage of the associated pair of Zener diodes. A freewheeling current will flow until the switches all activate and clamp the coil voltage to the cell voltage whereby the flywheel current will cease and current will flow to the target cell. Theoretically the two secondaries will have slightly higher voltages and should conduct first, and simultaneously, however tolerances in the Zener diodes and variances of Zener voltage due to device temperatures may mean that any of the coils conducts first therefore as added redundancy to protection there is an associated pair of Zener diodes for each coil.

The extra rectifier diodes in parallel with the converter switch body diodes are used to provide better forward conduction characteristics than the body diodes but are not strictly necessary.

The relatively low voltage operation of the converter means that the voltage drops across the conducting devices, which can usually be more-or-less discounted in higher voltage converters, shows as a sizable percentage of the conduction loop voltage drop. Making the assumption that the only reactive impedance component in either conduction period is the coil in the converter (for the purposes of single conduction period analysis the capacitor will be assumed to be so large as to be able to be modelled as an ideal voltage source with internal resistance) then the voltages may be written as in (4.1) for magnetisation period with an odd numbered source

$$V_{Cn} = 4i(\mathrm{t})R_{ch} + L_1 \frac{\mathrm{d}i(\mathrm{t})}{\mathrm{d}t} \tag{4.1}$$

where R_{Ch} is the channel resistance of the switches and positive current in the primary coil is defined as per the coil dot convention, i.e. positive current flows in the coil one and three from blue to red bus and positive current flows in coil two from red to blue bus.

During de-magnetisation the voltage drops may be described as in (4.2) for odd numbered targets and (4.3) for even numbered targets.

$$-V_{L2} = L_2 \frac{\mathrm{d}i(\mathrm{t})}{\mathrm{d}t} = 3i(\mathrm{t})R_{ch} + V_{Df} + V_{Cn} \tag{4.2}$$

$$V_{L3} = -L_3 \frac{\mathrm{d}i(\mathrm{t})}{\mathrm{d}t} = 3i(\mathrm{t})R_{ch} + V_{Df} + V_{Cn} \tag{4.3}$$

For an even source the sign conventions are reversed.

To examine the energy flow first consider the case whereby the windings all have equal turns. At the point of commutation the total MMF in the core is equal to the peak primary current multiplied by the number of primary turns as per (4.4).

$$\widehat{MMF} = n\hat{\imath} \tag{4.4}$$

Although commutation changes the conduction coil the MFF is common to both sides of the commutation event as the coils are coupled on the same core. Since the assumption is made that the coils are identically wound then the peak current must be identical for both coils. In order to drive the identical peak current the magnitude of the secondary voltage at the point of commutation will be higher than the primary voltage at commutation. This is due to the inductor voltage, as the current driver in the de-magnetisation period, being equal to the sum of the conduction voltages in the switches, diode voltage and cell voltage as per (4.2) and (4.3) whereas in the magnetisation period the inductor voltage is the sum of the cell voltage minus all the conduction drops as per (4.1).

Higher secondary voltage at commutation with equal current means that the instantaneous power output of the converter during demagnetisation is higher than the instantaneous power input during magnetisation. Therefore, for conservation of energy, the demagnetisation conduction time is shorter than the magnetisation conduction time unless the differences in cell voltage is larger than the diode voltage and the conduction voltage drops.

When the MMF in the coil falls to zero there is no coil voltage and the blocking diode holds the capacitor voltage in reverse bias.

4.3.4 Limitations of efficiency

As with the converters described in chapter 3 there are limitations on the level of current which may be conducted to and from cells. In the case of the proposed converter the limitation is easily seen from equations (4.1) to (4.3). As previously discussed the low voltages in the conduction loop mean that for significant current flow the parasitic voltage drops across the devices is not negligible. Indeed, as current continues to rise the voltage across the coil falls, eventually to zero. As the voltage across the coil starts to fall the amount of energy which is being stored in the core as a proportion of the current flow also begins to fall. This is because more and more energy is being burned up in the switches as conduction loss with higher current flow. At the point where the voltage across the coil tends towards zero the discharging current will level off to a fixed value proportional to the switch resistances and the source cell voltage. At this point the source cell is still discharging but the energy is being dissipated wholly in the silicon and no more is being stored in the core. As this period gets longer the amount of energy dissipated gets larger as a proportion of the amount of energy that may be transferred to the target cell and thus energy transfer efficiency is lowered. There are however instances, whereby this method of discharging may be beneficial to equalisation rate particularly if a single cell has a significantly higher voltage than the rest of the stack. This may result from failed or failing cells which have lower capacity. If the converter is to be operated in this dissipative mode then the effect on the requirements for the thermal control of the switches must be considered.

4.3.5 Advantages of using li-ion capacitor for proposed topology

As described in the previous section the limitations on the converter efficiency are driven by the limitations on current flow in the conduction loops during equalisation. Since these limitations are proportional to the cell voltage and the number of switches in the conduction path then there is a clear advantage to using the Li-ion capacitor which has a higher voltage range than the traditional EDLC. This does demonstrate a drawback of the proposed converter topology where particularly for large devices such as those discussed in chapter 2 then device resistance and number of devices in a series conduction path cause limitations on equalisation performance. As such, the work on development on this topology has concentrated on use of Li-ion capacitors since for very large cells the topology may not be appropriate at lower cell voltages.

4.4 Proposed converter simulation

As with the converters described in chapter 3 a simulation of the proposed converter is required to assess the performance. The converter is simulated using a network model as described in chapter 2.

4.4.1 Open loop control

As described in section 4.3 the converter can be seen to operate over two repeating periods; the magnetising period and the demagnetising period. Although there are significant advantages to operating a converter in closed loop current control this generally requires a significant number of additional sensors to the converter increasing cost and volume. This said, should the proposed equalisation scheme be required to operate in closed loop mode the penalty in increased current sensors is lower than for the converters in chapter 2, particularly the distributed winding converters. This is because in any possible energy flow path the current flow always flows on the energy busses. Therefore only one current sensor would be required. Closed loop current control is discussed in chapter 6 describing further work.

As has been described in section 4.3.3 for small differences in cell voltage the de-magnetisation period is always shorter than the magnetisation period because of the conduction voltage drops of the switches and the diode voltage. This means that the magnetisation period can safely be up to 50% duty cycle to attain discontinuous conduction (in a closed loop system this could even be extended beyond 50% by looking at the conduction time in the de-magnetisation period).

For the purposes of proof of concept an open loop control scheme is proposed whereby the primary winding conduction time is fixed at 50% duty cycle. Since the diode blocks any re-magnetising after the demagnetising current falls to zero due to the potential of the target cell the switches in the demagnetisation conduction loop can remain activated for the duration of the demagnetisation period.

The switching signals may therefore be divided into the two periods; magnetising and demagnetising. The switching signals SW1 and SW2 are shown in Figure 4-11.

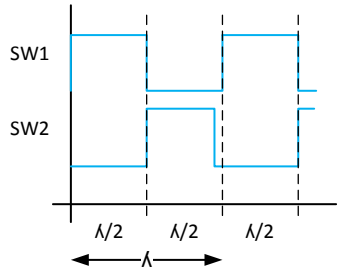

Figure 4-11 - Switching sequence for proposed converter

The switching signals SW1 and SW2 apply to different switches in the converter depending on the required energy path. The distribution of the switching signals is shown in table 4-3.

Table 4-3 - Distribution of switching signals by energy flow path

Energy Path	S1	S2	S3	S4	S5	S6	ST1a	ST1b	ST2a	ST2b	ST3a	ST3b
C1-C2	SW1	SW1 SW2	SW2				SW1	SW1			SW2	
C1-C3	SW1	SW1	SW2	SW2			SW1	SW1		SW2		
C1-C4	SW1	SW1		SW2	SW2		SW1	SW1			SW2	
C1-C5	SW1	SW1			SW2	SW2	SW1	SW1		SW2		
C2-C1	SW2	SW1 SW2	SW1				SW1	SW1				SW2
C2-C3		SW1	SW1 SW2	SW2			SW1	SW1				SW2
C2-C4		SW1	SW1	SW2	SW2		SW1	SW1	SW2			
C2-C5		SW1	SW1		SW2	SW2	SW1	SW1				SW2
C3-C1	SW2	SW2	SW1	SW1			SW1	SW1		SW2		
C3-C2		SW2	SW1 SW2	SW1			SW1	SW1			SW2	
C3-C4			SW1	SW1 SW2	SW2		SW1	SW1			SW2	
C3-C5			SW1	SW1	SW2	SW2	SW1	SW1		SW2		
C4-C1	SW2	SW2		SW1	SW1		SW1	SW1				SW2
C4-C2		SW2	SW2	SW1	SW1		SW1	SW1	SW2			
C4-C3			SW2	SW1 SW2	SW1		SW1	SW1				SW2
C4-C5				SW1	SW1 SW2	SW2	SW1	SW1				SW2
C5-C1	SW2	SW2			SW1	SW1	SW1	SW1		SW2		
C5-C2		SW2	SW2		SW1	SW1	SW1	SW1			SW2	
C5-C3			SW2	SW2	SW1	SW1	SW1	SW1		SW2		
C5-C4				SW2	SW1 SW2	SW1	SW1	SW1			SW2	

In operation, the equalisation converter controller must decide which energy flow path is the most appropriate and activate the associated switching sequence as per Table 4-3. This will usually be to transfer energy from the cell with the highest voltage to that of the lowest. This

decision requires measurement of the individual cell voltages which will be discussed in chapter 5. For the purposes of simulation the energy flow path is dictated by pre-defining the cell voltages and switching sequences.

4.4.2 Simulated converter waveforms

As is described in section 4.3.4 there are limitations to the peak current which can be drawn from the source cell due to the switch resistances. This effect is demonstrated in Figure 4-12 to Figure 4-15 where, as the primary inductance is lowered (the secondary inductance is also lowered to maintain the ratio) and the frequency held constant the peak current initially rises but starts to level off. The ratio of the charge flow through the secondary to that of the primary (integrals of the current) also falls off as peak current increases.

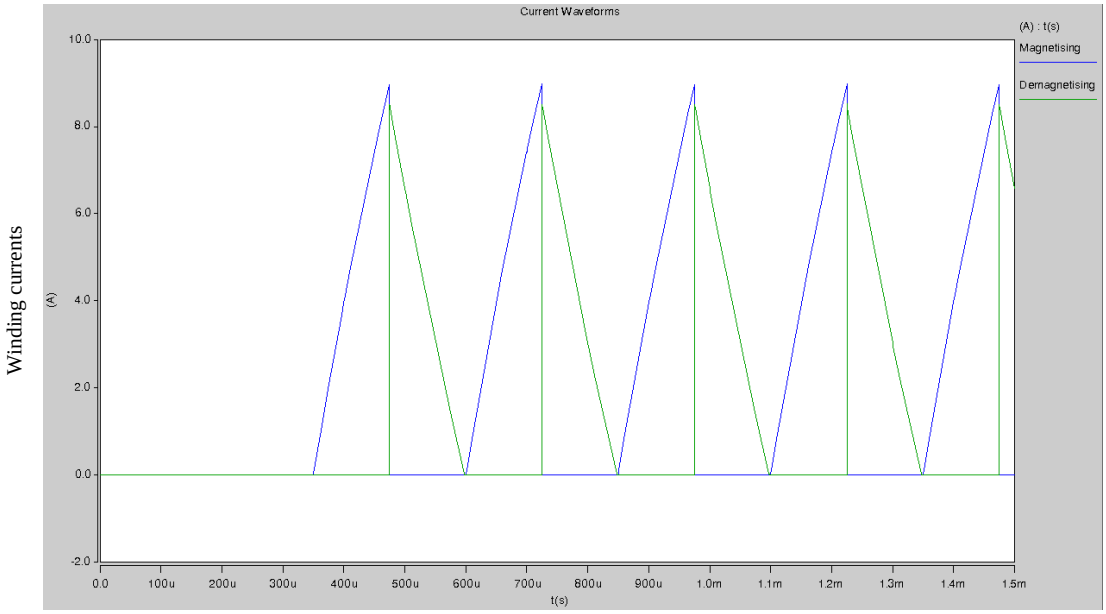

Figure 4-12 - Converter current waveforms, f = 4kHz, Lp = 40µH

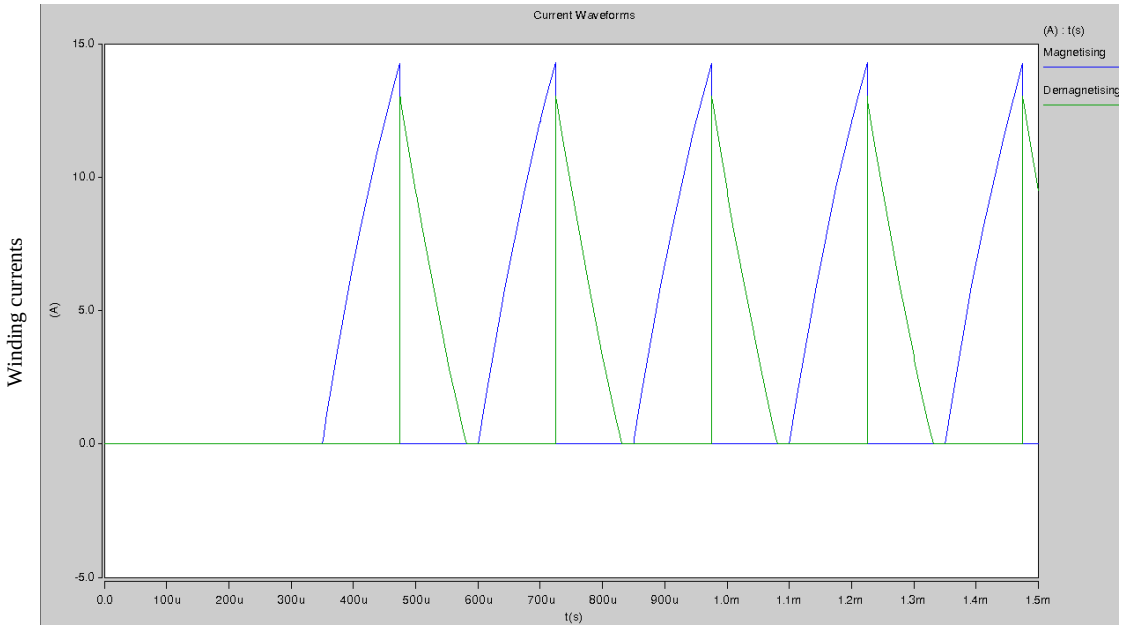

Figure 4-13 - Converter current waveforms, f = 4kHz, Lp = 20µH

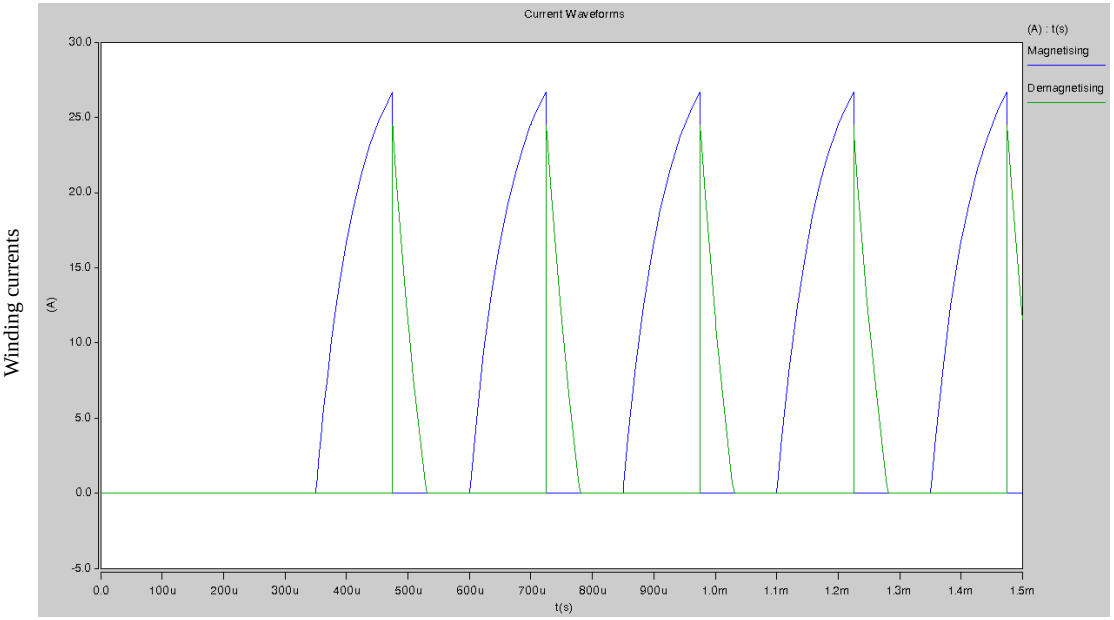

Figure 4-14 - Converter current waveforms, f = 4kHz, Lp = 6µH

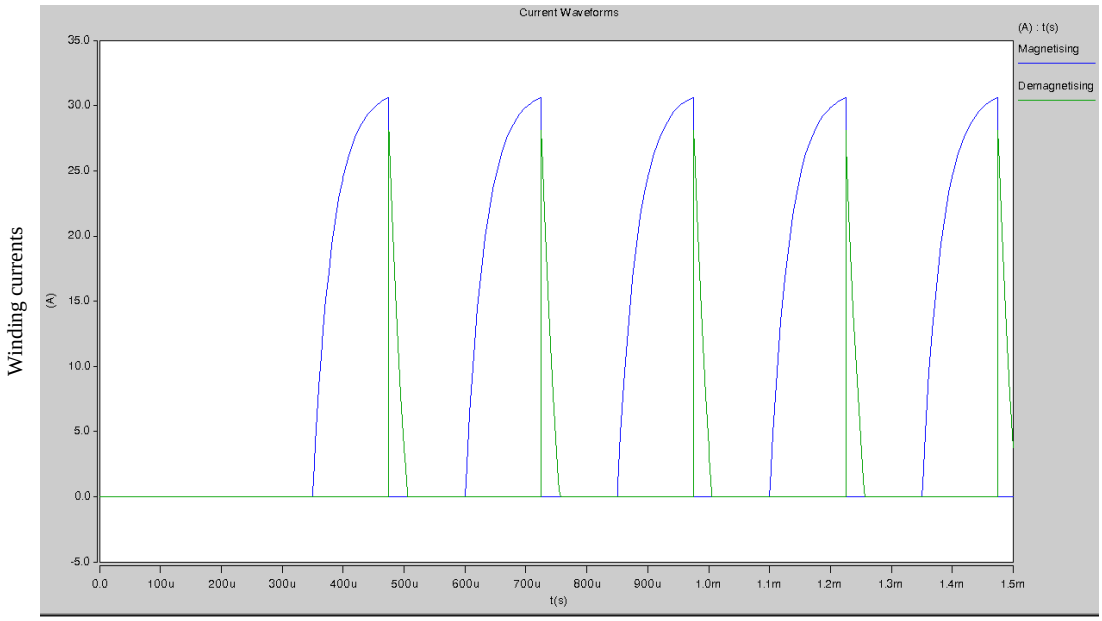

Figure 4-15 - Converter current waveforms, f = 4kHz, Lp = 4µH

The maximum attainable peak discharge current for the proposed converter is lower than that of some of the converters in chapter 3 because the number of switches in each conduction path is greater. For example, the buck boost controller (section 3.2.3) has only one switch in the conduction path during discharging thus has four times the peak current of the proposed converter for a given coil inductance and frequency. The advantage however of the proposed converter is that only one switching period is required for a given energy transfer route. Therefore, assuming efficient energy transfer in the converter the same energy transfer is achievable between adjacent cells in four times the time of the buck-boost converter. However, for cells non-adjacent the disadvantage is smaller, indeed for cells more than two apart the proposed scheme is actually quicker.

For discontinuous conduction, a higher peak current in the magnetising period results in a greater magnitude of discharge (the charge released is the integral of the current in the magnetising period). The equalisation efficiency measured as the amount of charge released in the magnetising period as compared to the amount of charge delivered in the de-magnetising period (integral of the current in the demagnetising period) is lower. This can be seen in the sequence of figures above. Clearly increasing the peak current gives faster equalisation time but it does decrease the equalisation efficiency. The equalisation efficiency may be quantified by using the ratio in (4.5) defining it as the ratio of the charge delivered to the target cell to the charge released from the source cell.

$$\epsilon = \frac{\int_{D\lambda}^{\lambda} i_s \, \mathrm{d}t}{\int_{0}^{D\lambda} i_p \, \mathrm{d}t} \tag{4.5}$$

Where D is the duty cycle and λ is the switching period. The importance of energy efficiency over equalisation rate is an application specific decision so for the purposes of this study the converter will initially be run at the most efficient energy transfer mode which is on the limit of discontinues conduction as per Figure 4-12. Figure 4-16 shows the cell voltages over 20 seconds running the equalisation converter at maximum efficiency.

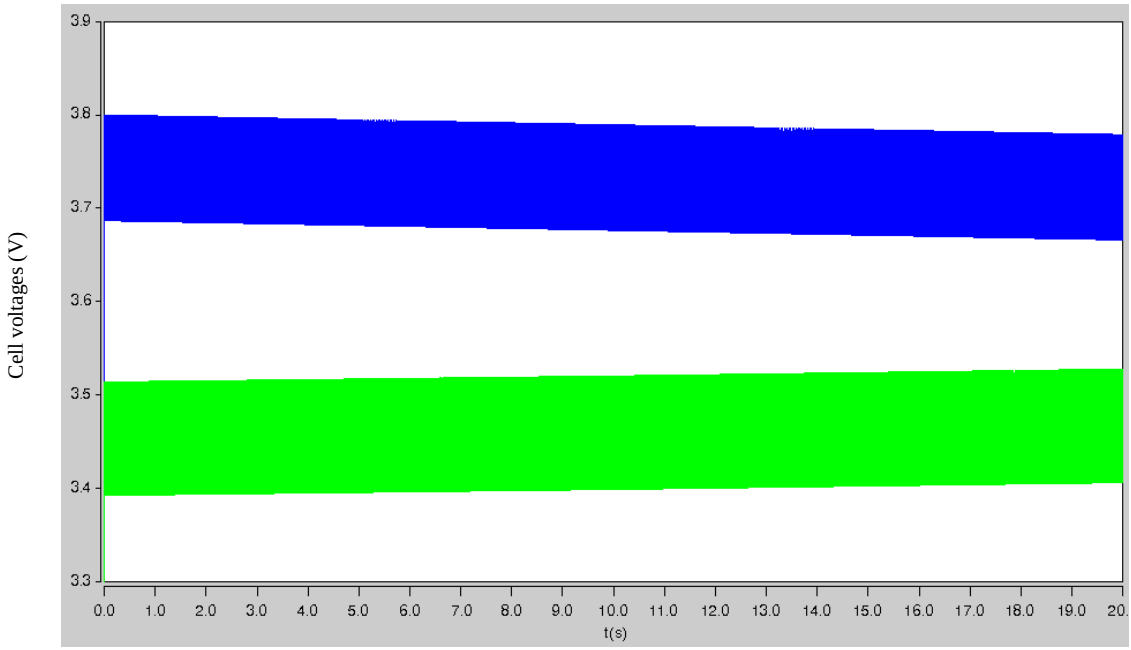

Figure 4-16 - Cell voltages for C1 and C3 over 20s equalisation at limit of continuous conduction. Initial Voltages C1 = 3.8V and C3 = 3.4V

Operating in this mode the equalisation converter performs similarly to the multi-winding transformer based converters described in chapter 3. The rate of change of standard deviation for this configuration and operation is $5\mathrm{mVs}^{-1}$.

The converter is also simulated at a less efficient winding configuration from Figure 4-14 initially at the indicated switching frequency. This yields the equalisation profile in Figure 4-17.

This mode of operation yields a rate of change of standard deviation of 9.1mVs^{-1} which is clearly faster than the above case but is less efficient.

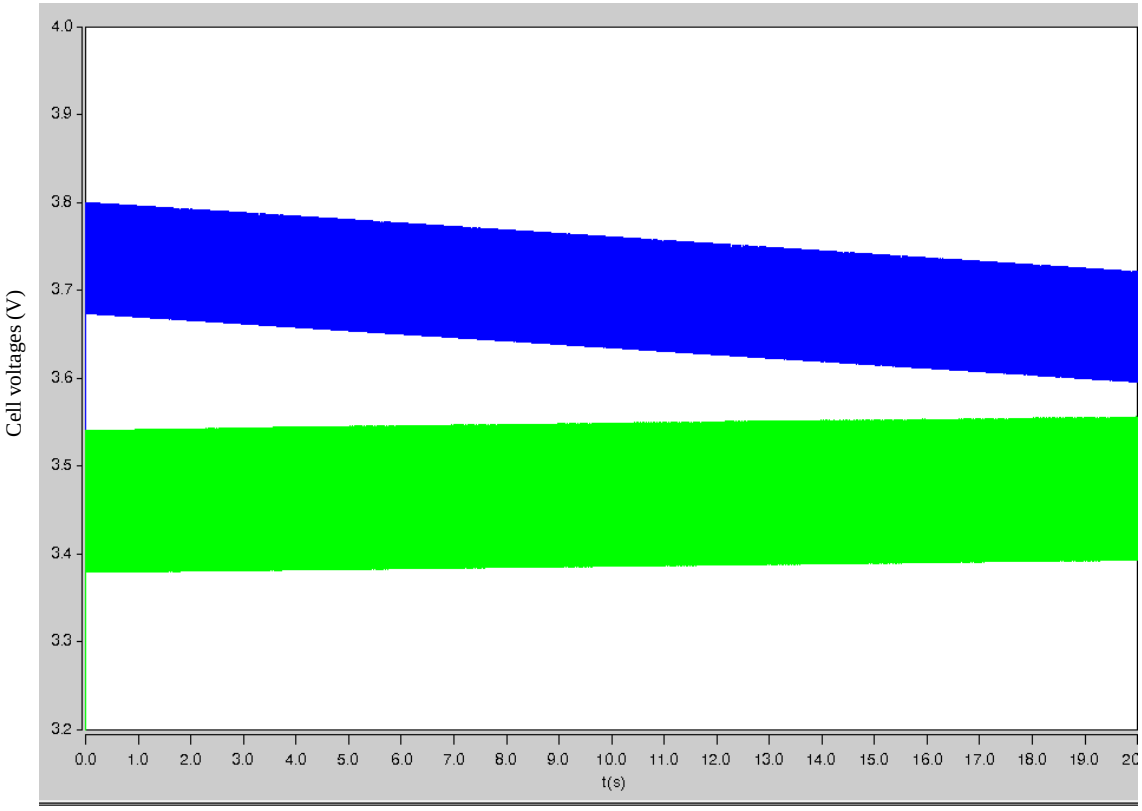

Figure 4-17 - Cell voltages for C1 and C3 over 20s equalisation at $\in = 0.33$. Initial Voltages C1 = 3.8V and C3 = 3.4V

Operating at these levels of efficiency it is possible to increase the equalisation rate without decreasing the efficiency further by altering the switching frequency but maintaining an identical magnetising period. The current waveforms for this operation are shown in Figure 4-18. The cell voltage profiles for this operation are shown in Figure 4-19 and the rate of change of standard deviation is 12.6mVs^{-1}.

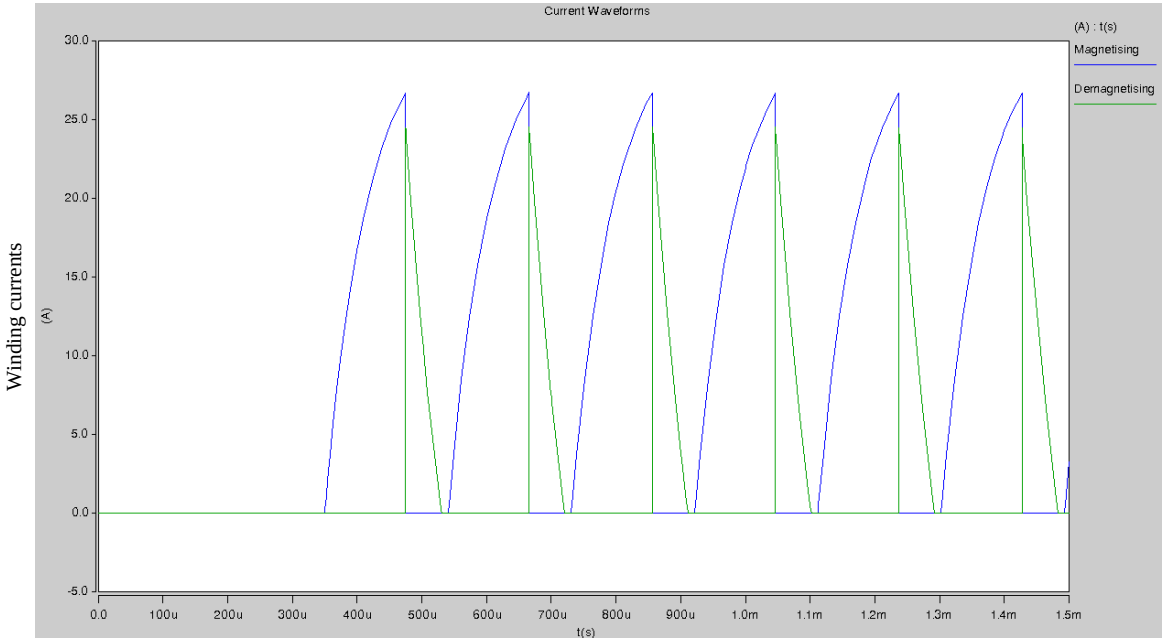

Figure 4-18 - Converter current waveforms with increased duty ratio$\in = 0.33$, f = 5.25kHz, Lp = 6µH

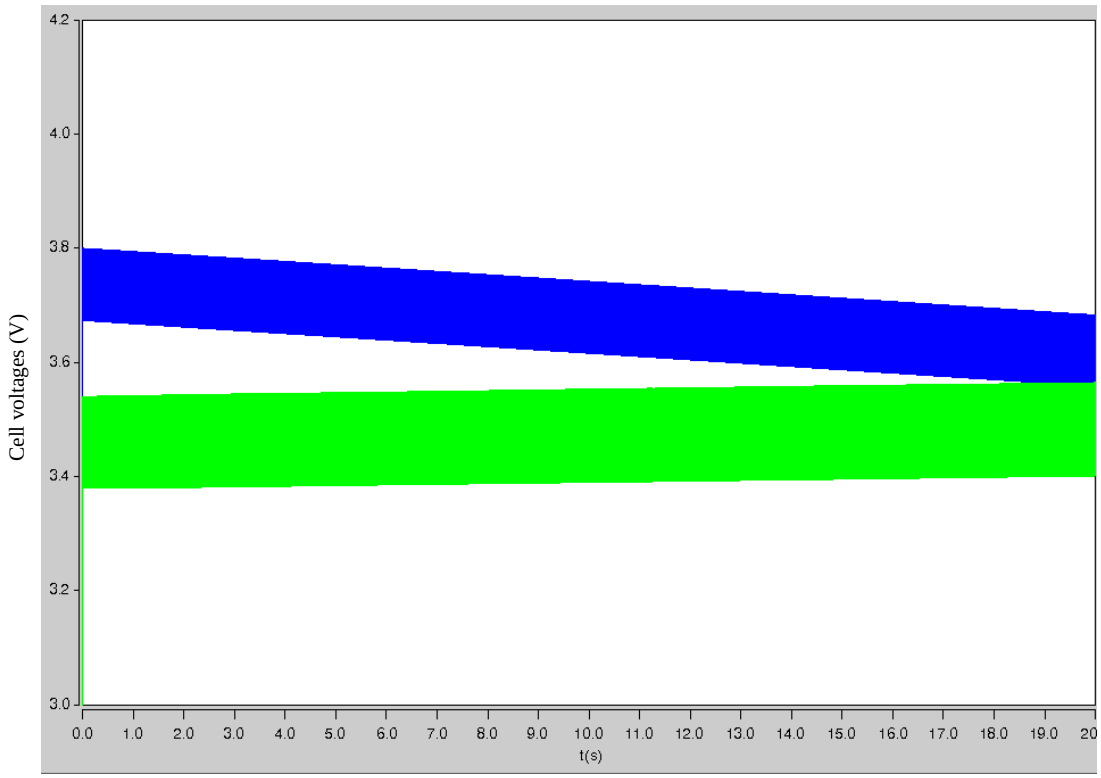

Figure 4-19 - Cell voltages for C1 and C3 over 20s equalisation at increased frequency and duty cycle $\in = 0.33$. Initial Voltages C1 = 3.8V and C3 = 3.4V

4.5 Summary

A new equalisation converter topology has been presented which has been designed specifically to accommodate a reduction in power rating overhead throughout the converter. Secondary design goals were to create a converter whereby the location of cells with more widely dispersed capacitances within the stack has no impact on achievable equalisation rate which was identified as the greatest shortcoming of the most successful converter topology discussed in

chapter 3. For a fixed control set-up the equalisation rate is fixed for every possible energy flow path which is a massive advantage over the buck-boost converter particularly for large numbers of series connected cells.

A simple control scheme has been implemented to operate the converter at various levels of equalisation rate. The limits of efficient equalisation are dictated by the hardware used, specifically by the switch resistance which is a shortcoming of the design since it requires a number of switches in series connection to operate. The control scheme has been shown to be adaptable to increase equalisation rate with given efficiency penalties by decreasing the switching frequency or winding inductances. At these less efficient operating points the equalisation rate can be further enhanced by altering the duty cycle to remain at the limit of continuous conduction. Depending on the equalisation rate required and the acceptable reduction of equalisation efficiency the equalisation rate can be increased to a point whereby the converter is almost wholly dissipative which is clearly not an ideal mode of operation but may be of use in extreme cases, such as under capacitor fault conditions if the system is required to maintain reduced operation in situations such as *limp home* mode.

Table 4-4 shows the simulated equalisation rate of the new proposed converter compared to the simulated equalisation rates of the five existing solutions.

Table 4-4 - Simulated equalisation rates for existing converters

Rates in mV/s	Series-parallel	Flying capacitor	Buck-boost	Flyback	Forward	Multiplexed 44µH	Multiplexed 20µH	Multiplexed 6µH
Static stack current	0.5	1	6.5	0.5	2.5	5	9.1	12.6

There are a number of improvements which may be made to the converter operation particularly regarding the control structure which will be discussed as future work in chapter 6.

5 Experimental arrangement, hardware considerations and measurements

This chapter documents the experimental arrangements to verify the validity of the converter proposed in chapter 4. Included are the experimental goals and limitations, hardware topology and safety requirements, the considerations and mitigations required for realising the converter in hardware and the means by which the converter is controlled via microprocessor and the control scheme. Finally, the operational waveforms are presented and evaluated against the performance of the simulated converter and a loss analysis is carried out.

5.1 Hardware considerations and mitigations

The deployment of power electronics interface onto a stack of series connected cells, either battery or capacitor, poses some unusual design considerations some of which are not common to power electronic converter design. Some of these considerations are common to all types of equalisation converter. Those which are relevant to the proposed converter are discussed in this section below.

5.1.1 Floating switches and gate drives

Most modern power electronic converters use either MOSFET or IGBT power switching technology. These discrete devices are operated by controlling the voltage applied between the gate and source (MOSFET) or gate and emitter (IGBT) legs of the transistor switch. The devices operate, depending on their mode, when the applied voltage between the two legs is increases beyond a threshold. Most power electronic converters operate the devices in saturation where the switch is seen to have a binary state of open or closed. Typically, a MOSFET's threshold voltage may be around 1 to 2 volts with a maximum range of ±20V [76]. Typically, the gate drive signals may therefore swing between 0 and 15V for single ended operation and -15 to 15V for double ended operation.

Considering the bi-directional switch S1 in Figure 4-7, the pair of transistors have a common source connection. This means that a single differential voltage may be applied to both gate legs and to the common source pins to operate the switch. During switch activation the source pins are connected through the left hand transistor's channel to node C1 (as defined in Figure 5-2). The node C1 has an absolute voltage with reference to node C0 of between 11 and 19V (as is shown in Table 5-1). Similarly, operation of any of the other switches S2-S6 results in this coupling of the source pins to the respective capacitor node each of which has a varying absolute voltage dependant on the states of charge of each of the cells in the stack.

This variance in absolute value of the source pins during operation both of an individual switch as the stack SOC varies and across the range of switches poses a problem when considering the supply voltage for the gate drive circuits. To achieve a gate-source voltage of 15V independent

of the switch or state of charge of the cells in the stack requires that each of the gate drives has an independent voltage source which is isolated from any reference node and is floating. This problem exists also in bridge-inverters where the upper device's source pin is alternating between 0V and the DC link voltage. In some simple systems a bootstrap capacitor is employed to provide a differential voltage which effectively floats to the upper rail when the lower transistor is switched off. However, this operation requires than the lower switch be regularly turned on returning the bootstrap capacitor to the 0V rail where is can be charged from the gate drive circuit power supply which usually sits at reference to the 0V rail. A bootstrap capacitor based gate drive is therefore not appropriate for the proposed converter since the sources of the switches are never pulled to the ground rail allowing the bootstrap capacitor to charge up.

Instead the gate drive circuit must have a floating voltage supply via an isolated DCDC converter. Moreover, each gate drive must have its own isolated DCDC converter since the sources are all clamped to different nodes of the circuit. An isolated DCDC converter power supply along with an opto-coupled gate drive allows total galvanic isolation between control electronics and the equalisation converter allowing complete electrical isolation in the gate drives.

5.1.2 Differential voltage measurement with high common mode

Although for the purposes of this work measurement of the cell voltages is not required since the prototype converter operates from pre-conditioned stack voltages nevertheless the concept whereby the central controller can operate independently and in closed loop choosing the correct energy flow path a method by which the controller can measure the differential cell voltages must be demonstrated. As has been established in previous sections electrical connection to the nodes of the stack of cells can prove troublesome due to the varying common mode voltage associated with the state of charge of the cells in the stack. In order to measure the individual cell voltages a differential amplifier with large common mode rejection is required. Although optically isolated solutions for common mode rejection are available and more accurate over the mV range, solid state solutions are a more cost effective solution [77].

Once the common mode has been removed from the differential signal by the amplifier, the remaining signal can be converted to digital directly by the microprocessor using on-board analogue to digital converters.

5.1.3 Current measurement

Current measurement in the equalisation converter is achieved using a current transducer powered from the controller board and eliminates any common mode issues associated measurement with common mode voltages. The resulting signals, realised as analogue voltage signals around a DC bias are converted to digital within the microprocessor as with the voltage measurements.

5.1.4 Filtering considerations

The variances in the various measured quantities within the converter are over two main time scales. The switching frequency, in the order of kHz, dictates the bandwidth of interest for current measurement whereas the voltage measurement associated with the decision over which energy path to use is a far slower time constant. Since for the purposes of this work the main motivation for looking at the measured quantities is demonstration of the operation of the converter the filtering of the signals is achieved using only simple RC low pass filter. The purpose is mainly to filter out much higher frequency background noise. In practice, an in-field converter, particularly operating in closed loop current control, may require a more comprehensive filter. The voltage signals should have a cut-off frequency well below the switching frequency and the measurement should be made during non-conducting periods to avoid errors from voltage drop due to ESR.

5.2 Experiment overview

The construction of hardware for controlling the proposed equalisation scheme has a number of objectives both within the scope of the project and as a provision for further work. As such, attention has been made to design the hardware so that further analysis on equalisation converters may be made in future work. For the purposes of this work the experiment is limited to proving the assertions made in the development of the new topology in chapter 4 and demonstrating that operational effectiveness of the this novel equalisation converter topology.

The experimental hardware consists of four parts; the first part is the arrangements of Li-ion cells. The second part is the hardware responsible for the energy transfer in the equalisation converter. The third part is the control electronics for the converter operation including the microprocessor controller and gate drive electronics and the fourth part consists of hardware interlocks for safety and converter protection and a pre-charge assembly for setting initial stack SOC conditions. The systems level topology of the experimental apparatus is shown in Figure 5-1. The function of each part of the experimental setup is described in the following sections.

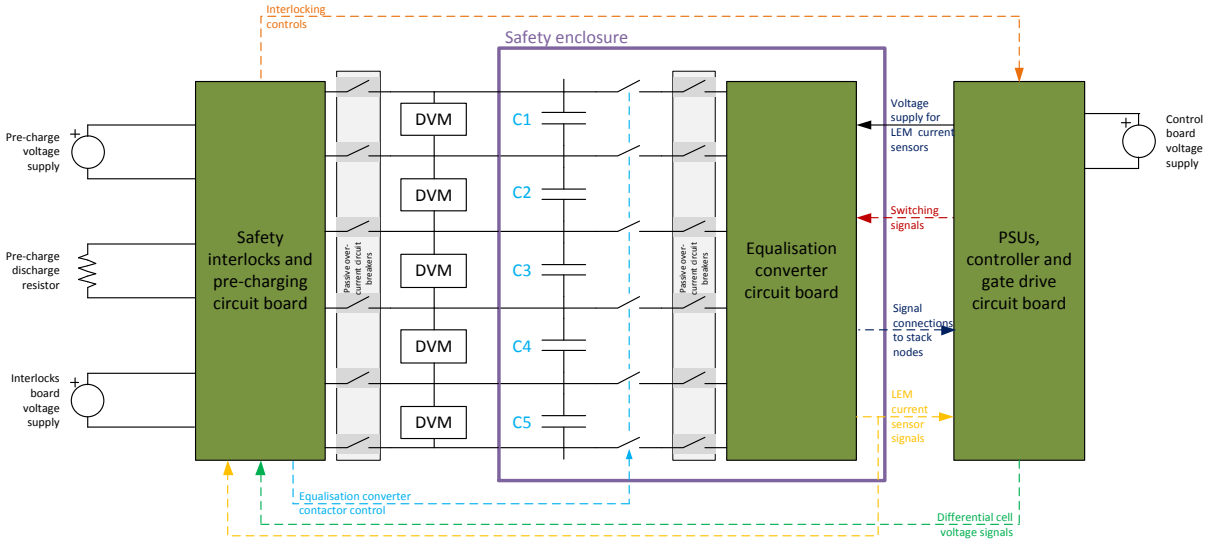

Figure 5-1- System level diagram of experimental apparatus

5.2.1 Hardware topology 1 – stack of series connected cells

A stack of five cells has been constructed each being one of the 2200F cells described in section 2.1.2. The cells are numbered sequentially from the top cell to the bottom C1 to C5 and each of the six nodes on the stack are numbered so that the node name corresponds to the next cell down the stack as is shown in Figure 5-2.

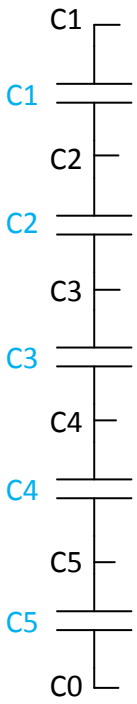

Figure 5-2 - Arrangements of five cells in series connected stack, cells numbered in blue and nodes in black

Depending on the state of charge of each of the cells each node voltage must lie between two values with the exception of the bottom node C0 which is the reference node and always sits at 0V. Table 5-1 shows the possible range of absolute node voltages with reference to C0.

Table 5-1- Range of absolute voltages for nodes in the stack of five cells

Node	Voltage range
C1	11-19V
C2	8.8-15.2V
C3	6.6-11.4V
C4	4.4-7.6V
C5	2.2-3.8V
C0	0V

5.2.2 Hardware topology 2 – equalisation converter

The equalisation converter and the equalisation stack are the two aspects of the hardware which could be hazardous if an operational fault occurs. This hazard is principally from thermal runaway due to high currents which could lead to fire. For laboratory conditions the converter and the stack must be constructed in a protective enclosure to avoid any foreign bodies from accidentally causing damage through short circuit of any of the stack nodes. As such, the converter components and cells are by necessity enclosed together in a sealed container. For the purposes of converter and cell protection each of the current paths to the converter, i.e. each of the six multiplexing switch paths and each of the transformer coils, includes an active current measurement device. This allows a governing circuit to monitor current levels in the converter and terminate operation remotely if required. It also allows simple measurement of the conduction path currents for circuit analysis. As is described in section 4.4.1 this level of measurement is not necessary for operation, even in closed loop, but is utilized here for the robustness of the prototype circuit protection and the simplicity of waveform measurement. A photo of the assembled equalisation stack and converter is shown in Figure 5-3.

The equalisation converter part of the experimental apparatus consists of the hardware required for the energy transfer process as well as the current measuring devices described above. These devices are mounted on a single circuit board and hard wired to the nodes of the capacitor stack. The power supplies and switching signals originate for the converter on another circuit board described in section 5.2.3.

Although anti-series connected switches which are used in the multiplexor system are available in single packages the MOSFET devices for the converter have been selected as discrete components. This is to enable individual switching of individual devices should further work require this facility. For this work the gate pins are simply tied with a jumper connector. The

MOSFET switches used are IRF540N devices. These are selected for the high current capability (33A continuous) and low on state resistance (44mΩ) [76].

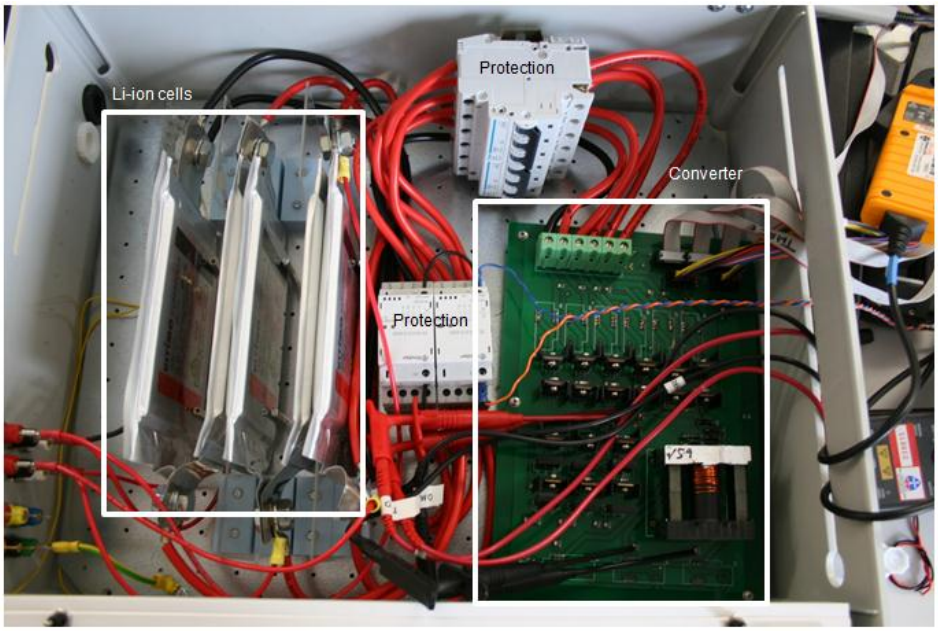

Figure 5-3 - Photograph of Li-ion stack and equalisation converter

Current measurement is achieved with LEM LAS 50-TP current transducers. These devices have a linear voltage response for ±50A. This means that the current measurement will be totally linear for operating window of the MOSFET switches selected. Since the voltage swing of the transducer output is 0-5V and the input to the ADC on board the microprocessor has a maximum value of 3.3 the output is reduced through a potential divider. The voltage reducer is integrated with a single RC low-pass filter with a corner frequency of 400kHz calculated using (5.1).

$$f_c = \frac{1}{2\pi RC} \tag{5.1}$$

The three-winding transformer is included as an interchangeable component. This is to allow for changes in turns ratio and inductance. The coils are wound around exchangeable bobbins which can be fitted with a combination of magnetic cores. For flexibility and ease of construction a large 49mm E-core was selected. The core has an average cross sectional are of 211mm^2 and is made by Epcos from material N87. The core material in this size has an A_L value (inductance per turn) of 3800nH for ungapped cores and 525, 314 and 188nH for 0.5, 1 and 2mm respectively [78]. Using a combination of different cores and windings four primary inductance values of 44, 20, 6.5 and 3.5uH were assembled (measured values).

5.2.3 Hardware topology 3 – converter controller and gate drive circuits

The low voltage control hardware containing the microprocessor, signal processing and gate drive electronics are located on an exterior board to the safety enclosure. This is primarily to aid

simple, fast attachment of oscilloscope probes during apparatus commissioning and experimental work.

The controller board is responsible for the generation of the gate drive signals that operate the converter module within the safety enclosure. It is also responsible for conditioning the signals from the equalisation converter, namely conduction path currents and cell voltages, for the microprocessor. These functions will be explored in more depth below as they pose some more complicated hardware considerations.

The microprocessor controller is responsible for the generation of the switching signals which are converted to gate drive signals by the gate drive circuits.

The processor is a Microchip 33FJ64GS610 dsPIC; a 16-bit 50MIPS architecture. This model processor has eight independent PWM channels which have individually addressable frequency, duty and phase values. Each PWM channel comprises of a pair of outputs which are in themselves independently addressable. The first five PWM channels are used to control the multiplexing switches. The second output for these channels is not used. PWM channels 6-8 are used to control the converter switches. Since there are six switches both outputs for these channels are used.

Within the microprocessor code there is a function which sets the control registers for the PWM module. Each energy flow path requires a different registry setting as different switching patterns are used (as shown in Table 4-3). When the processor identifies the energy flow path that will be used this function assigns the correct registry settings which will ensure that the correct switches operate, as per Table 4-3, when the PWM module is activated. For the case of the prototype the required energy flow path is predetermined by setting the initial voltages of the cells.

The switching signals SW1 and SW2 (Figure 4-11) are created by using the master PWM counter and offsetting one signal with a phase advance. Therefore there is a standard control registry setting which is applied to each of the PWM channels dependant on whether the channel is assigned to SW1, SW2 or is inactive.

The processor has 24 10-bit analogue to digital converters (ADC). There are 4 independent sample and hold channels and two multiplexed sample and hold channels with nine and 13 inputs each. In order to set the appropriate registry settings for the PWM module the cell voltages will be measured at the same instance during a time of non-conduction in the equalisation converter. The cell voltage measurements are therefore assigned to the four independent ADC inputs and to one of the multiplexed inputs in the nine input array. The current measurements are assigned to the 13 input array. For any further work in closed loop

current control the current will only need to be measured in any one sensor at any one time therefore multiplexing the signals is acceptable.

In open loop control mode the processer performs an ADC measurement on the cell voltages at the end of each 256 PWM pulses as part of an interrupt service routine (ISR) which is invoked after the PWM counter is reset 256 times. The ADC conversion is used to decide whether the converter is required to operate and which energy flow paths are used. This is achieved by requiring the converter to operate if there is more than 1mV difference in the cell voltages and by using the two most dispersed voltages (i.e. the highest and lowest) as the energy flow route. The PWM module is switched off while the control registers are reassigned if necessary it is then switched back on.

The PWM output signals are 3.3V logic (as are all the processor outputs) which are upscaled to 5V logic using a pair of MM74HC244 octal CMOS buffers. This allows the signals to operate with the voltage ranges of the gate drive circuits.

The gate drive circuits are powered using Traco Power TMR 3-2423 isolated DCDC converters. These power supplies have a wide input voltage range (18-36V) with 1500V isolation between the input and output. The output is ±15V and can deliver up to 100mA continuous which is very easily enough for the purposes of charging two gates. The supplies also have a remote functionality which enables them to be switched on by the processor. The remote pins are all connected so that the supplies can also be simultaneously activated when the processor is ready to begin switching and also deactivated when an over current is detected by the safety interlocks.

The gate drive circuit is centred on the HCPL-316 chip. This chip features optically isolated signal path to 1500V, a fault feedback signal and under voltage lockout. The desaturation feature which measures the on state voltage drop across the device must be disabled since the drive is operating two switches which will have different collector voltages. The fault pins are open collector so they can be cascaded to provide a single feedback signal to the processor. The under voltage lockout is a secondary safety aspect which should ensure that failure in any of the power supplies will result in a fault condition turning all of the gate drive circuits off. A clamp resistor is included to ensure that the gate pin is clamped to the source when the chip is not in operation.

The differential voltage measurements of the cells are achieved using the AD629 high common mode rejection difference amplifier. The chip features ±500V common mode protection. The chip is supplied from the 5V CMOS supply that is also used for the logic. The outputs therefore have to be stepped down to 3.3V via a potential divider which is fed to the processor ADC inputs.

5.2.4 Hardware topology 4 – safety interlocks and pre-charging

The safety interlocks and pre-charging section of the experimental apparatus is responsible for the protection of the converter, controller and capacitors in the event of a failure which could cause damage. This is principally a protection against over current and over or under voltage. As the experimental apparatus is a prototype system an active current measuring device has been included in each conduction path as redundant overcurrent protection.

Although the current measurements are also fed to the microcontroller which has software interrupts designed to protect against over current a redundant hardware-only interrupt system is implemented in the interlocking system which cuts the power to the gate drive circuits under over current events.

Similarly, a hardware only protection system is included to protect the cells from over or under voltage by similarly removing power to the converter controller. Upon loss of power to the controller board the gate drives to the equalisation converter are designed to fail with all switches open to avoid any short circuit conditions arising.

The pre-charging element of the interlock section is to enable pre-conditioning of the stack voltages before experimental readings are taken. The interlocking system must disengage the connection of the stack from the equalisation converter to avoid damage whilst pre-conditioning is taking place. Pre-conditioning the stack may consist of either raising or lowering the voltage of a given cell hence the requirement for both a charging power source and a discharging load.

5.3 Operational measurements

For the purposes of analysis of the proposed equalisation scheme performance the operation of the hardware described above is identical to that of the simulated system described in section 4.4 whereby equalisation takes place between the first and third cells on the stack. These cells are pre-charged to a fixed initial state before each experiment so that C1 is at 3.8V C3 is at 2.2V and all the other cells are at 3V. A number of winding inductances have been used to compare with the simulated results shown in section 4.4.2.

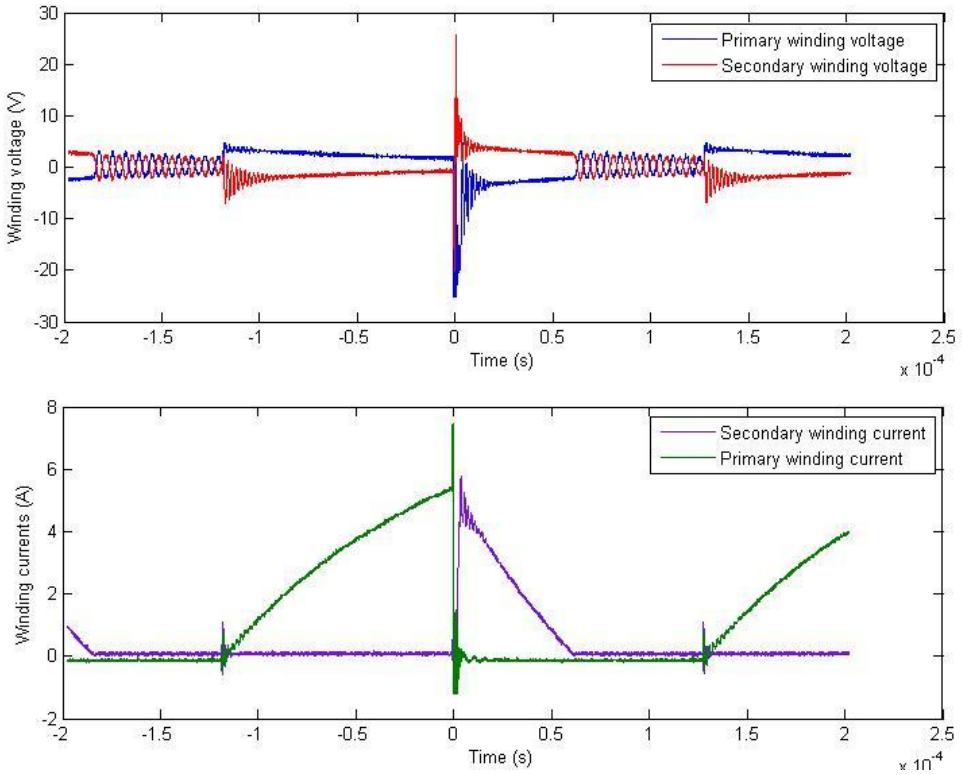

Figure 5-4 - Voltage and current waveforms for converter operation. f = 4kHz, Lp = 44uH

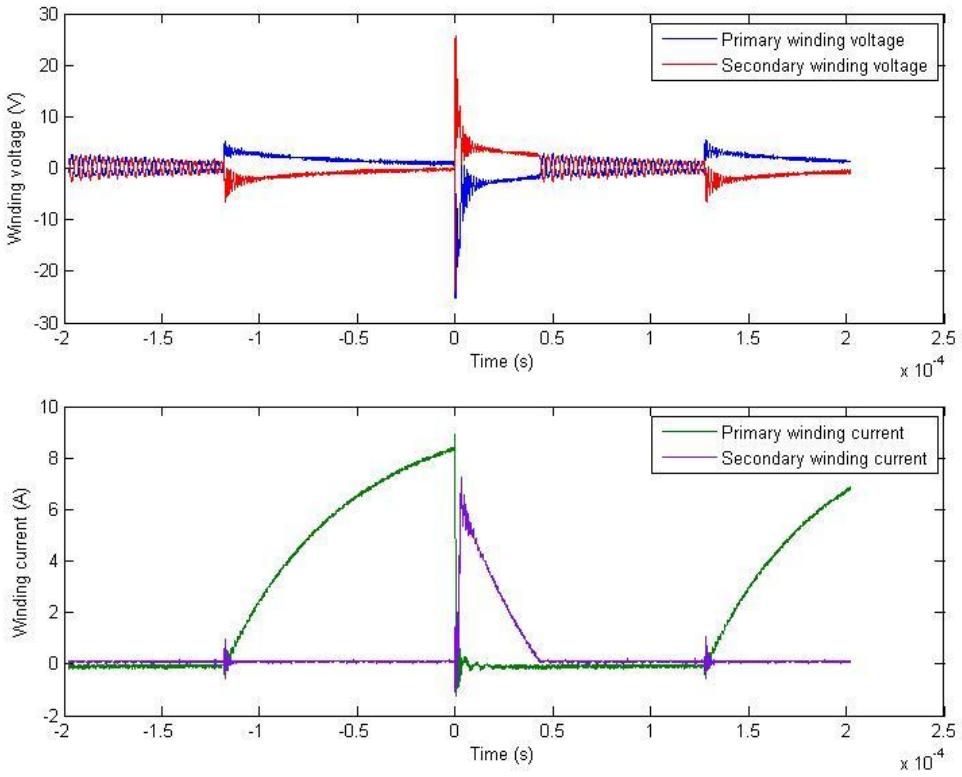

Figure 5-5 - Voltage and current waveforms for converter operation. f = 4kHz, Lp = 20uH

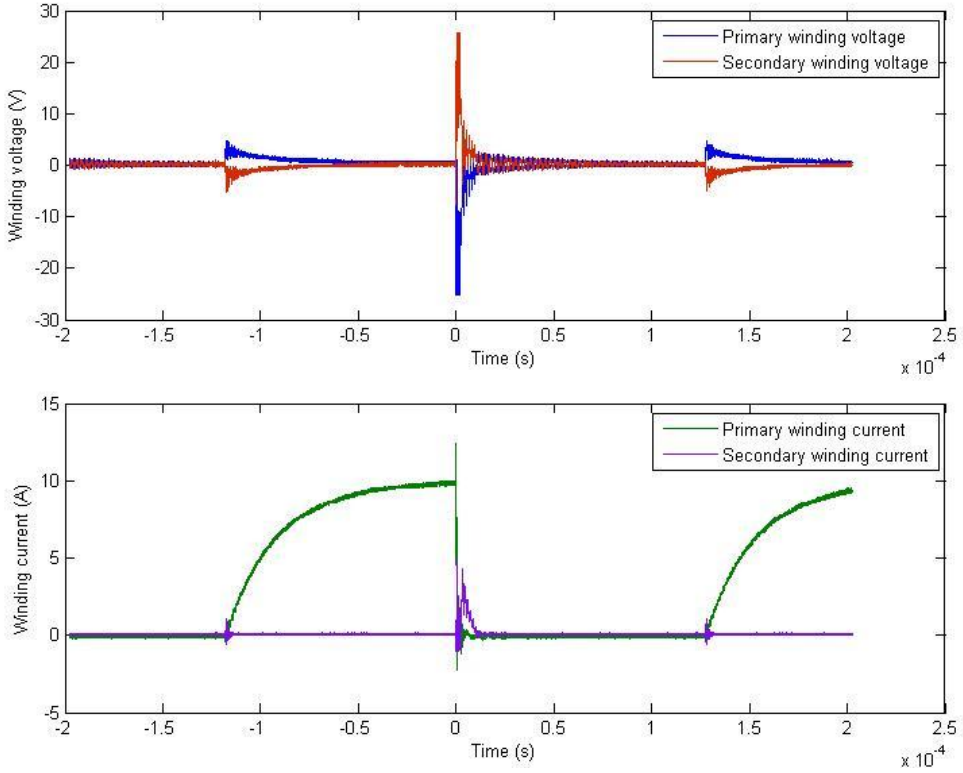

Figure 5-6 - Voltage and current waveforms for converter operation. f = 4kHz, Lp = 6.5uH

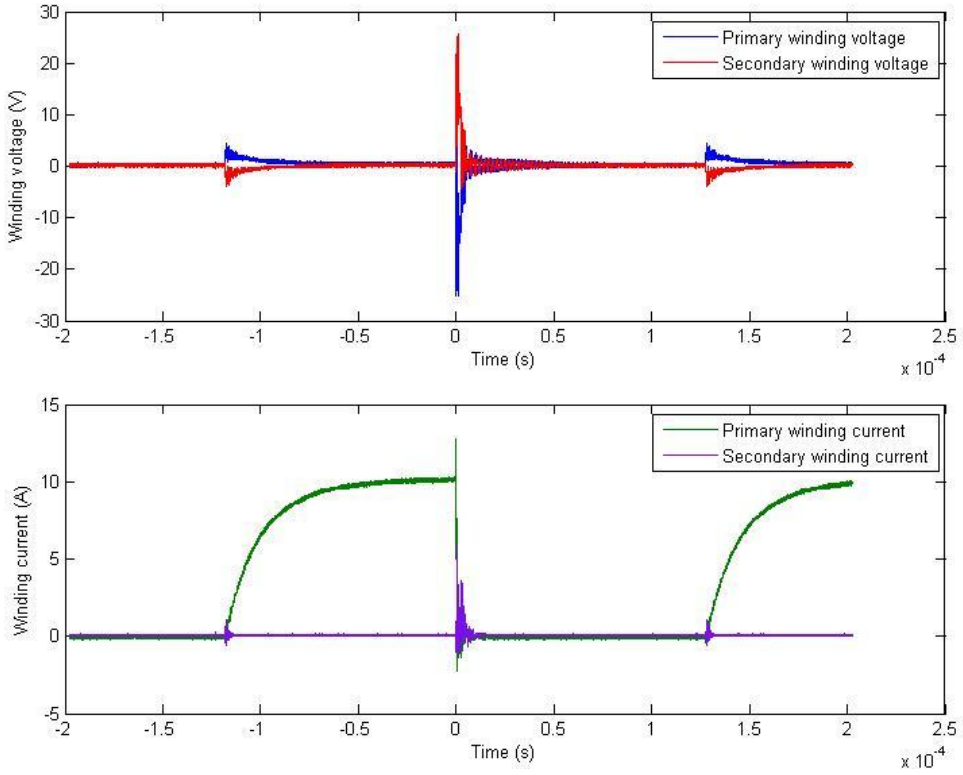

Figure 5-7 - Voltage and current waveforms for converter operation. f = 4kHz, Lp = 3.5uH

Comparing these results to the simulated results in chapter 4 shows that the peak currents actually attained for the various winding inductances are lower than predicted in the simulations. For the case in Figure 5-4 the magnetising period can be studied to obtain an

explanation of this. Figure 5-8 shows a magnified image of the waveforms during the magnetisation period.

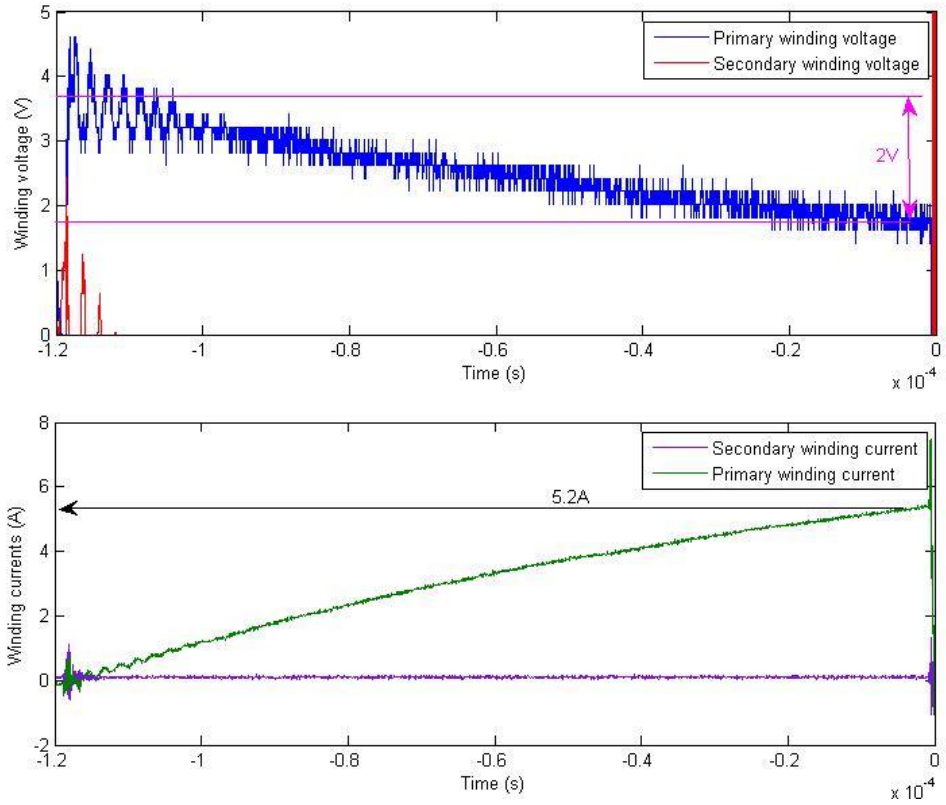

Figure 5-8 - Analysis of voltage drop during magnetisation. f = 4kHz, Lp = 44uH

As shown, at a time just before the commutation point the instantaneous primary winding current is approximately 5.2A. The corresponding drop in voltage applied to the primary coil – which is a result of the conduction voltage drops of the cell, switches and conduction loop as described in (4.1) – is approximately 2V. The series resistance of the conduction loop, excluding any resistance of the coil since the voltage is measured across it, can therefore be calculated using simple Ohm's law as 380mΩ. This value is higher than the value of around 250mΩ which was calculated from the hardware datasheets. The explanation for this increased series resistance may lie with the added resistance of the protection circuit breakers which, although essential for prototype commissioning and testing would not be present in a more developed version of the hardware. Equally, the addition of an active current sensor to each conduction path may have led, to a lesser degree, to a higher conduction path resistance than was envisaged.

Figure 5-9 shows simulated waveforms with an adjusted series resistance in the conduction loop during magnetisation. These waveforms more closely show the results as measured with the correction for higher than expected resistance.

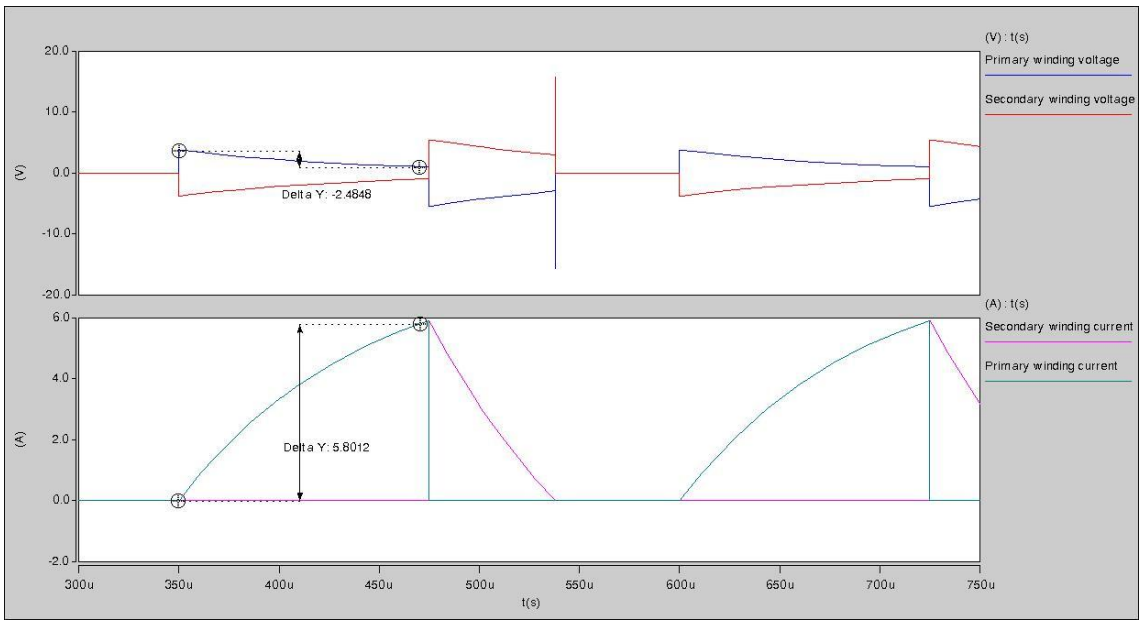

Figure 5-9 - Adjusted simulation results for greater series resistance of conduction loop

The voltage oscillation ringing present in the measured results after conduction has ceased in the secondary winding is another significant difference from the simulated data. The simulated system employs an idealised transformer with no intra nor inter-winding capacitance modelled. As an approximation a parallel capacitance to each of the transformer windings may be used to model these effects. The result is shown in Figure 5-10 and roughly approximates the effect. A more accurate representation may be to more accurately model the transformer with a coupled transmission line.

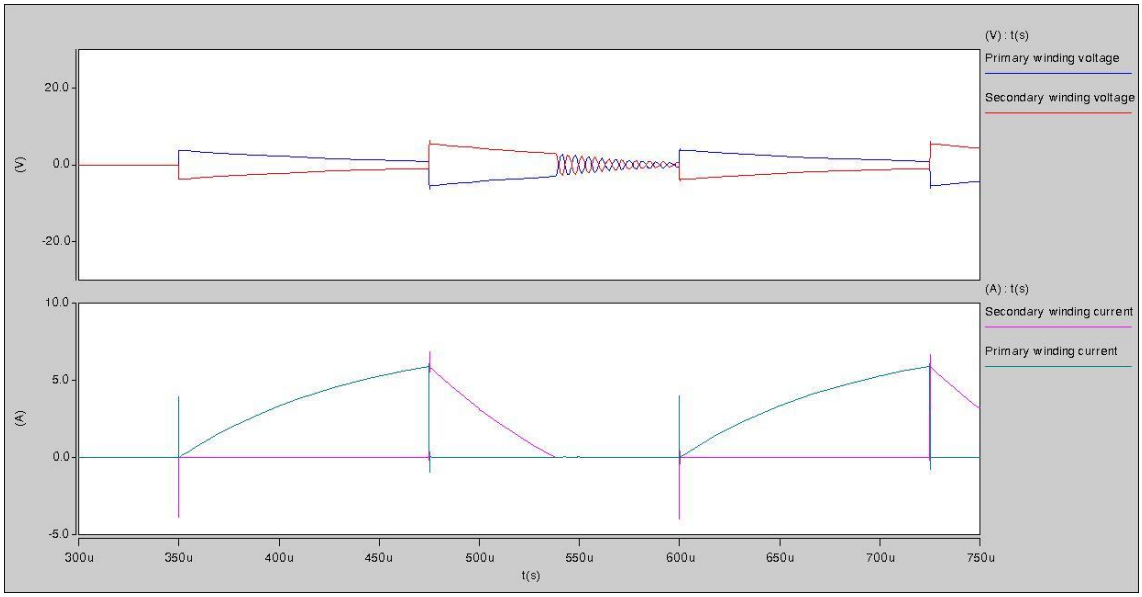

Figure 5-10 - Simulated voltage waveforms with lumped transformer winding capacitances to approximate ringing effect

The voltage spike and associated noise at commutation is perceived to be an effect of finite current rise time in the secondary coil. The voltage peaks are in accord with the Zener voltage on the arrest diodes which in this particular case is nominally 25V. The associated freewheeling

current is not shown as winding current was measured outside of the Zener parallel loop to avoid damage to current measurement devices.

5.4 Loss analysis

Since the series resistance of the conduction loops was shown to be greater than expected the tuning for the efficiency ratios is also misaligned to that of the simulated results. Whilst maintaining the same hardware it is possible to retune the converter's frequency, assuming that the component ratings allow, attaining various degrees of equalisation efficiency. The greatest efficiency transfer, as is described in chapter 4, is where the converter operates with 50% magnetising current duty ratio and on the limit of continuous conduction operation. In the case of the prototype hardware described above (and using a 44uH primary winding) the frequency can be increased to 20kHz to the limit of discontinuous conduction. However, as is shown in Figure 5-11, the magnitudes of the discharging and charging currents are considerably smaller. Using a smaller primary inductance would increase the theoretical maximum current achievable at this conduction state however this requires an increase of frequency which would soon be beyond attainable levels for the equipment employed. Therefore the effectiveness of the converter as an equalisation scheme should be thought of in two separate measures. Firstly the amount of charge which is taken on by the target cell as a ratio of that released from the source cell, defined as the efficiency, $\in$, in (4.5) and secondly the equalisation rate – which may be defined in any number of ways but which is effectively a function of the average current flow over one conduction cycle. Consequently, since a desired efficiency effectively sets the average current and a desired average current in turn sets the efficiency the operator of such a converter would need to reconcile a payoff between efficiency and rate.

Assuming the converter controller has the ability to vary duty cycle and frequency the converter may therefore be operated across the whole range of efficiency between equal conduction time and zero demagnetisation time with the limit of equalisation rate being the constant short-circuit of the source cell – assuming the components are rated correctly and recognising that the converter is clearly operating in totally dissipative mode.

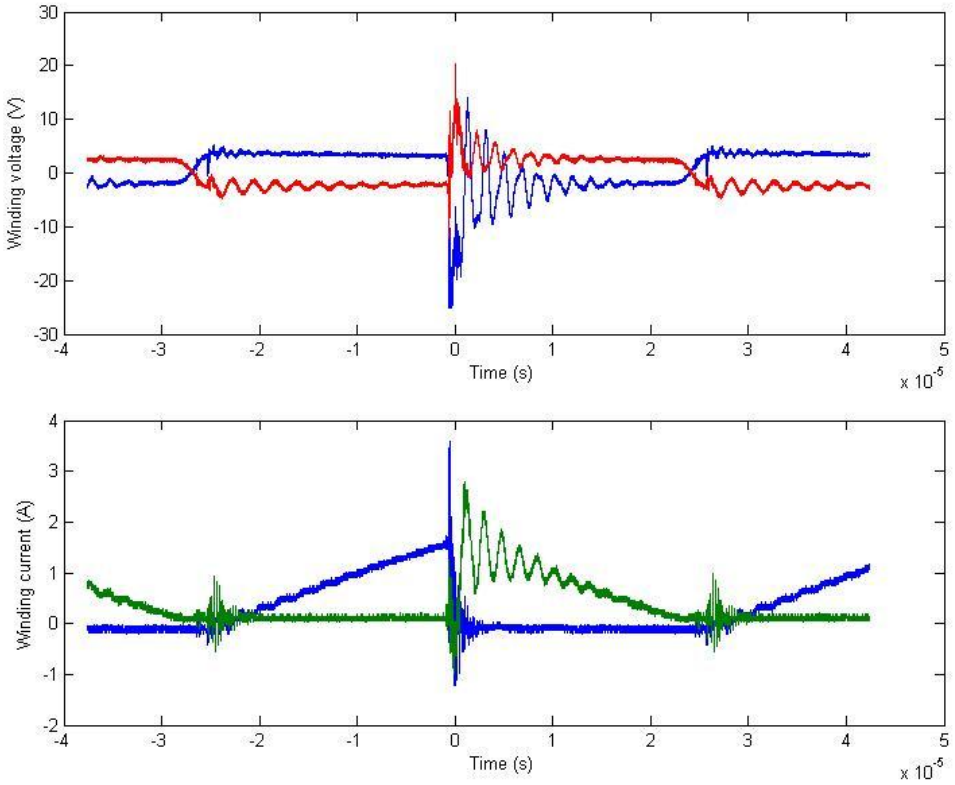

Figure 5-11 - Voltage and current waveforms for converter operation. f = 20kHz, Lp = 44uH

5.5 Equalisation performance

The equalisation converter has been operated with three values of inductance (6.5, 20 and 44µH) over 20s. Unfortunately the noise present at the measurement terminals means that a figure of the voltage trace is inconclusive. Measurements can, however, be made before and after the experiments to make a linear approximation of the cell voltage changes. Table 5-2 shows the equalisation rates calculated from this linear approximation.

Table 5-2 - Equalisation rate for each winding inductance

Inductance (µH)	Rate of change of standard deviation (mV/s)
6	9.6
20	5.7
44	3.1

The low inductance results show better performance in the low inductance experiments however as has been shown these are when the converter is operating at low efficiency. Better performance would be expected if the series resistance in the conduction loops could be reduced. This could be achieved by using lower resistance switches as well as removing other parasitic such as the circuit breakers.

5.6 Experimental arrangement summary

The equalisation converter and control system proposed in chapter 4 has been built as a prototype, proof of concept apparatus. The converter has been shown to operate as expected with the exception of increased losses in the actual built apparatus which is perceived to be due to the nature of the prototype requiring extra measurement and protection hardware as part of the conduction loops.

Various operating conditions have been presented and show correlation between the expected trends of the simulated system and the working prototype. The increased loss in the prototype has reduced the expected equalisation rates for given efficiencies which shows an area suitable for future work.

Table 5-2 shows a comparison between the simulated equalisation rates for the existing solutions, the simulation results for the proposed system and the measured system.

Table 5-3 - Simulated equalisation rates for existing converters

	Series-parallel	Flying capacitor	Buck-boost	Flyback	Forward	Multiplexed 44µH (simulated)	Multiplexed 20µH (simulated)	Multiplexed 6µH (simulated)	Multiplexed 44µH (measured)	Multiplexed 20µH (measured)	Multiplexed 6µH (measured)
Rates (mV/s) for static stack current	0.5	1	6.5	0.5	2.5	5	9.1	12.6	3.1	5.7	9.6

6 Conclusions

This chapter summarises the work presented in this thesis and concludes with suggestions for further work on the subject.

6.1 Summary of work

Energy storage requirements in modern applications such as renewable generation, transport, electricity distribution and smart grid has led to the development of a number of electrical energy storage technologies. Power density and dynamic response requirements in some of these application areas are such that traditional battery technology and even modern Li-ion battery technology is not suitable as an electrical energy storage medium for some tasks. Therefore the more power dense and responsive technology based on the electric double layer capacitance (EDLC) effect, devices known commercially as supercapacitor or ultracapacitor, has been employed to accomplish these needs.

Supercapacitor technology yields devices with extremely high levels of capacitance by conventional electrostatic standards; commercially available cells are available upwards of 5000F. This high capacitance, combined with very low series resistance results in a cell which can provide very large current levels. However, the process which allows the high capacitances, namely the ionic boundary between the electrolyte and two electrodes, is a limiting factor on the maximum cell voltage of any given EDLC cell. The voltage limit of such cells is commonly around 2.7V. This limitation in cell voltage means that to attain a system-level voltage, so that the supercapacitors may be utilised within an application, a number (for example around 225 cells in a 600V system) of cells are required to be stacked in series connection.

Across a series connection of cells the nominal capacitance, as well as other parameters, varies from device to device due to manufacturing tolerances. These differences result in mismatched voltages of the stack cells after a period of charging and discharging. For purposes of safety and efficiency it is necessary to limit the cell individual voltages and desirable to maintain equalised voltages across the stack.

Reducing the required number of series connected cells in a stack is therefore a clear advantage. Fewer cells reduces volume and cost and require fewer ancillary devices for voltage limiting or equalisation for a given energy storage system. To maintain the same voltage the only way to reduce the number of cells in a stack is with an increased cell voltage. Since the cell voltage limitation is based on a physical property of the double layer effect increasing the cell voltage is achieved only through a bias of the cathode. This effect has been achieved with the recent development of the Lithium-ion capacitor which is now commercially available.

Methods for dealing with mismatched voltages range from simple, almost passive systems which simply limit individual cell voltages through a resistive discharge to complex power electronic converter topologies. For some applications the simple passive systems may be the most appropriate method, on cost grounds for example, however their poor efficiency may render them unsuitable for certain specific uses. Power electronic converter topologies allow equalisation to take place without penalty of wasted energy through a discharge process. Instead the energy is shared among the cells to maintain equilibrium. Just as with the choice of energy storage medium, the most suitable equalisation technique may be a function of the application at hand however with an active converter some generic features are likely to be preferred.

Development of electronic systems which are to interact with an energy storage system require that some knowledge of the behaviour of the energy storage medium is known in order to anticipate the result of given operations. Therefore considerable effort is undertaken in order to model the behaviour of electrochemical cells. The work involved in this thesis requires that a good working model of supercapacitors and Li-ion capacitors is used when designing an equalisation converter. Many models have been published for supercapacitors and a review of these is made within this work in order to select an appropriate model for use in hardware development. Since Li-ion capacitors are a new technology at the time of writing little published work on modelling these devices existed. Therefore a method for modelling Li-ion capacitors, analogous to the selected supercapacitor modelling method has been developed and has been shown to be accurate portrayal of Li-ion capacitor behaviour.

This work has demonstrated the limitations of previously presented equalisation schemes as well as advantages some have over others. Limitations of existing equalisation converters may be due either to the topology of the converter not allowing flexible energy paths between cells or because the constituent components themselves limit the possible equalisation rates. The inductor-less equalisation schemes analysed cannot perform satisfactorily because the equalisation current is very small, particularly for cells which are close to equilibrium. There is also no simple way to control the equalisation rate for these converters. The bi-directional buck-boost converter topology performed well under simulation however extrapolation of the performance of this equalisation scheme exposes the limitations of the energy flow path possibilities. Since energy can only pass between adjacent cells the performance shown in the small sample used in this work would scale negatively as the stack gets longer. The multi-winding transformer topologies tested in this work have the advantage of global energy flow paths but the constituent parts of the converter, namely the transformers themselves, could be cumbersome and costly to construct for large numbers of cells. The flyback converter, whilst having the advantage of low component count, is also not particularly suited equalisation since much of the source cell discharging is undone during the recharging event. The forward

converter topology has the advantage over the flyback of controllable energy flow path but has more floating transistors and the multi-winding transformer.

Moreover, study of the power flow paths in existing equalisation schemes leads to the conclusion that there is wasted overhead in the scheme itself; there is no need for the equalisation converter to be rated for the sum of each of the power flow paths because energy flow is not required at maximum power in each energy path.

The motivation to design a new converter topology, which both reduces unneeded power rating overhead in the equalisation scheme as well as removes the requirement for complex components such as the multi-winding transformer whilst maintaining a flexible, global energy flow path is clear.

This work has presented the process of conception of a new equalisation topology which utilises a solid state multiplexor to a single converter. The concept of the proposed converter is that in any given stack of cells the majority of energy flow is between only a few, most dispersed in terms of capacitance, cells. Therefore including power converter parts onto every energy flow path is unnecessary. Naturally, since there is no way to predict which energy paths are required the interface between the stack and the converter needs to be fully rated but this part of the equalisation scheme can be kept relatively small.

Simulation of the proposed converter shows the limitations in efficiency and equalisation rate of the proposed converter. Various control algorithms are also suggested to maximise the performance of the scheme however complex closed loop control is beyond the scope of the work presented here.

The proposed equalisation converter has been constructed and tested and shown to operate almost as expected. Some behaviour, such as the voltage ringing, has been attributed to parasitic effects of the prototype as constructed and further study may allow for the mitigation of these effects. The limited performance compared to the simulation has been shown to be a factor of the prototype system having higher than expected resistance in the conduction loops. This is likely to be due to resistance of the protection devices, measurement transducers and assembly imperfections which were not originally accounted for in the simulation of the converter. It seems likely that all of the converters analysed in this work may suffer from similar issues when realised in hardware and thus the simulated performances may be expected to scale as was the case with the proposed converter.

All of the converters analysed in this work, including the new proposed converter, have relatively slow equalisation rates when operating in conjunction with the cells of the size used for this work. Smaller cells clearly equalise faster since a smaller amount of charge movement is required to change the cell voltage. One conclusion of this is that for very large cells even

relatively fast equalisation converters may not be suitable or fast enough for equalisation, particularly if the voltage dispersion is expected to be high.

In this light the proposed converter is deemed to be successful and advantageous over previously proposed schemes. The subjective nature of whether the performance of any of the equalisation schemes studied is sufficient is very difficult to quantify since the individual applications in which the energy storage systems are utilised drive the result. It therefore should be sufficient to speculate that the proposed scheme offers advantages over previously published equalisation schemes and would therefore necessarily be considered a candidate in a given energy storage application.

6.2 Future work

Whilst a number of conclusions are able to be drawn from this work regarding the effectiveness of both existing and published equalisation schemes as well as modelling techniques there are still many issues in energy management for high capacitance devices.

This work, for example, has not included thermal management of cells in its scope. Thermal management could be accomplished passively or actively and in the case of the latter as an integrated part of the voltage management process.

The proposed converter has been simulated and operated using a very simple control structure. Optimisation of the converter both with an improved control algorithm and hardware configuration should yield a greater performance.

Limitations in the availability of sample devices also meant that both the cell modelling and converter prototype were necessarily limited in scope. Scale-up of the equalisation scheme to full voltage levels would yield a better understanding of the performance of both the existing and proposed converter.

The topology of the proposed converter as constructed for the prototype can be simplified. Using closed loop, asynchronous PWM control the transformer may be reduced to two windings with equal turns. The multiplexor topology can also be improved by using a package where the anti-serial switches are packaged together. The gate drive circuits for these switches are expensive due to the common mode voltage – this is a problem which is common to all equalisation converters which have floating transistor switches. The gate drive power supplies could be integrated into the stack to reduce component cost.

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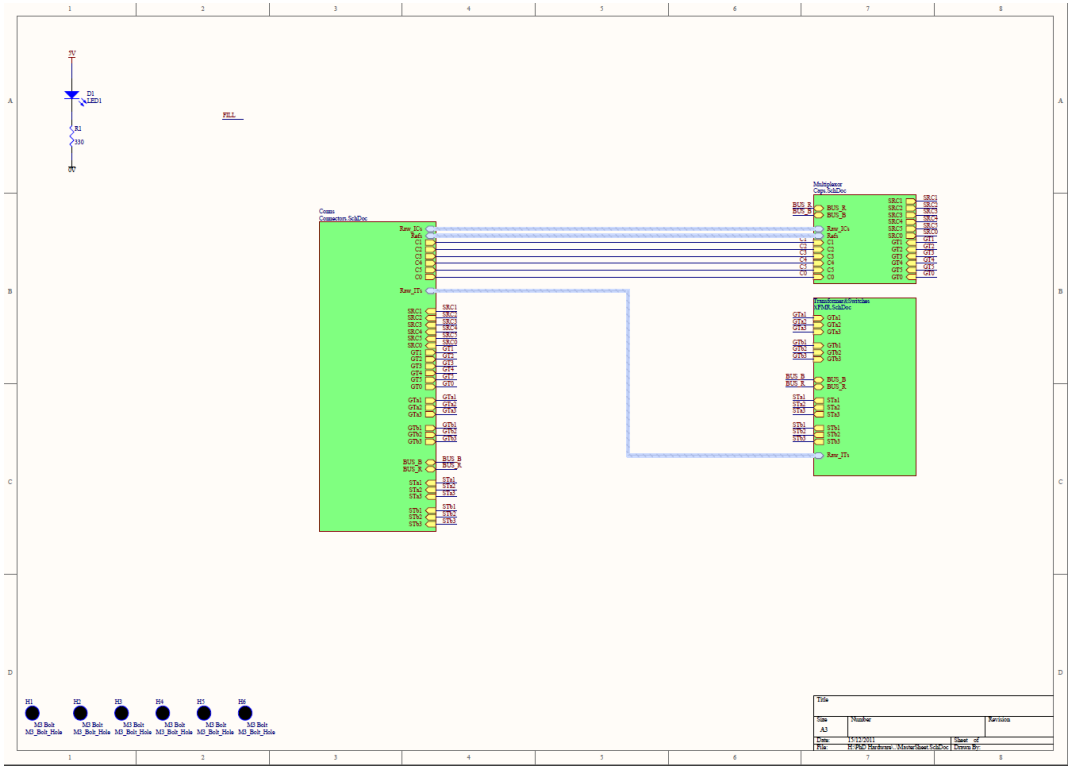
A. Appendix – Hardware schematics

Equalisation converter



This is the top level diagram for the converter PCB. The schematics are split into three sections; the connectors subsystem contains all the hardware for inter-board connections, the multiplexor subsystem contains the MOSFET switches for the interface to the busses and the transformer subsystem contains the transformer and selector switch.

Figure A-1 - Top level schematic of converter board

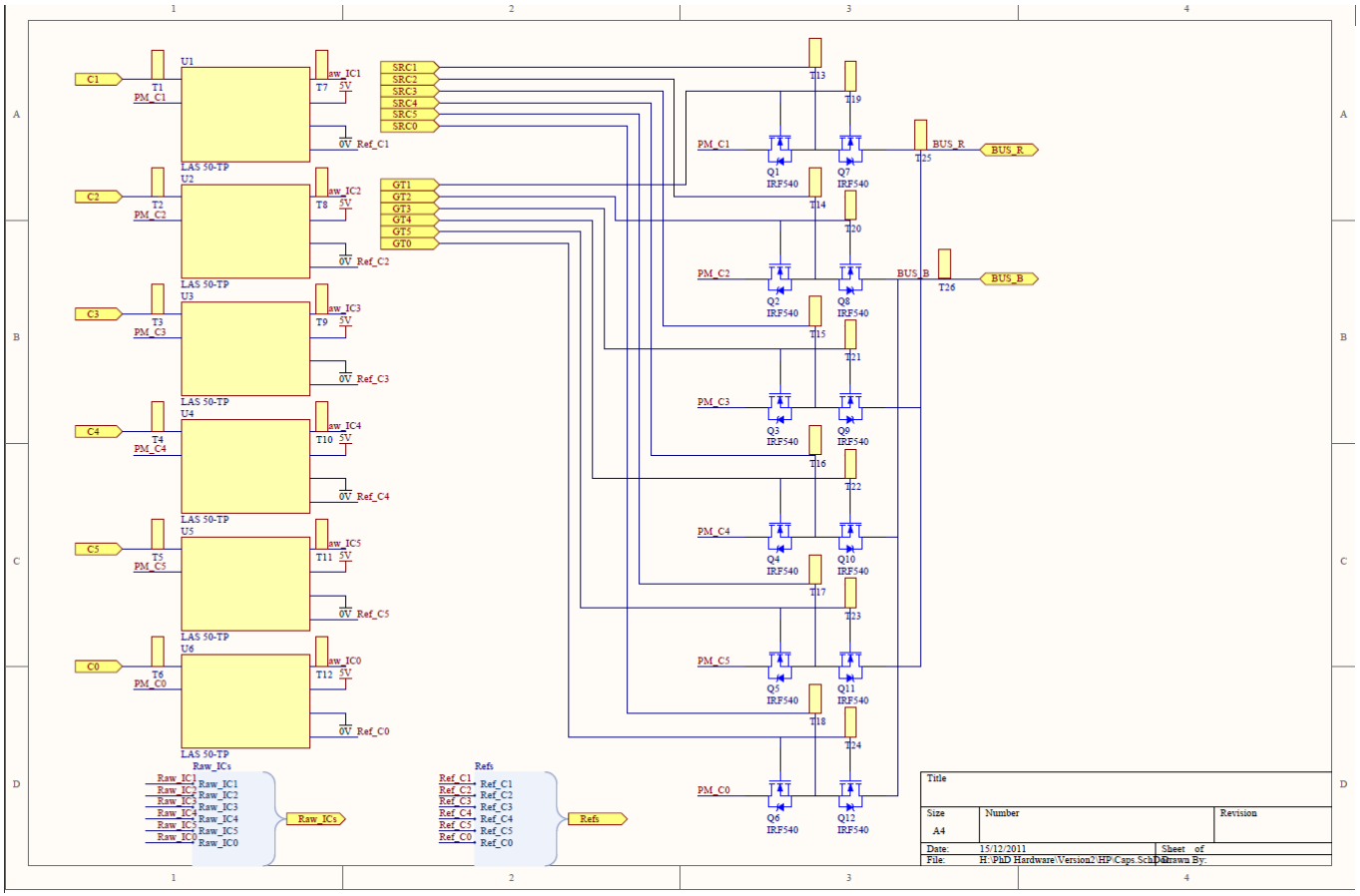
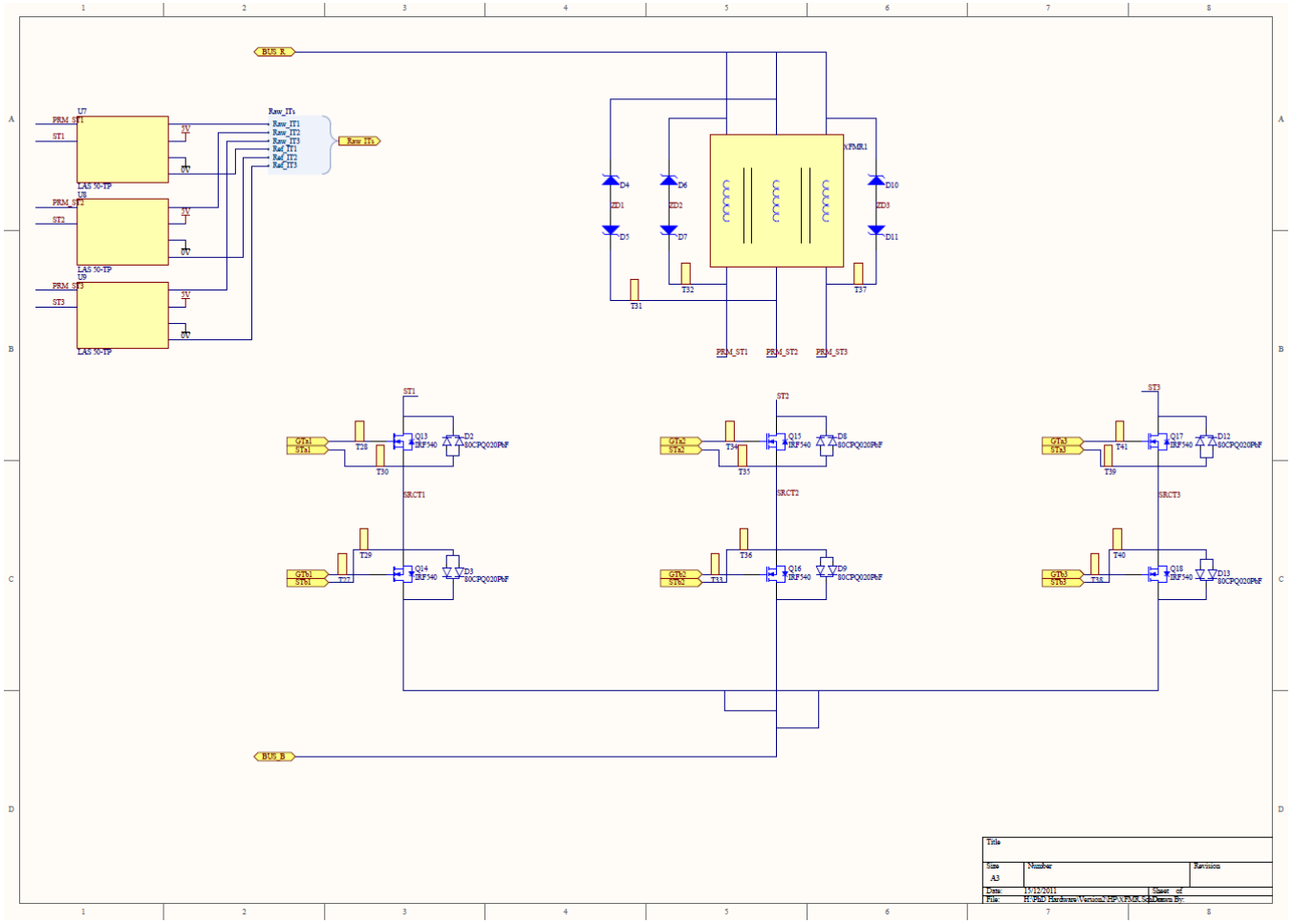


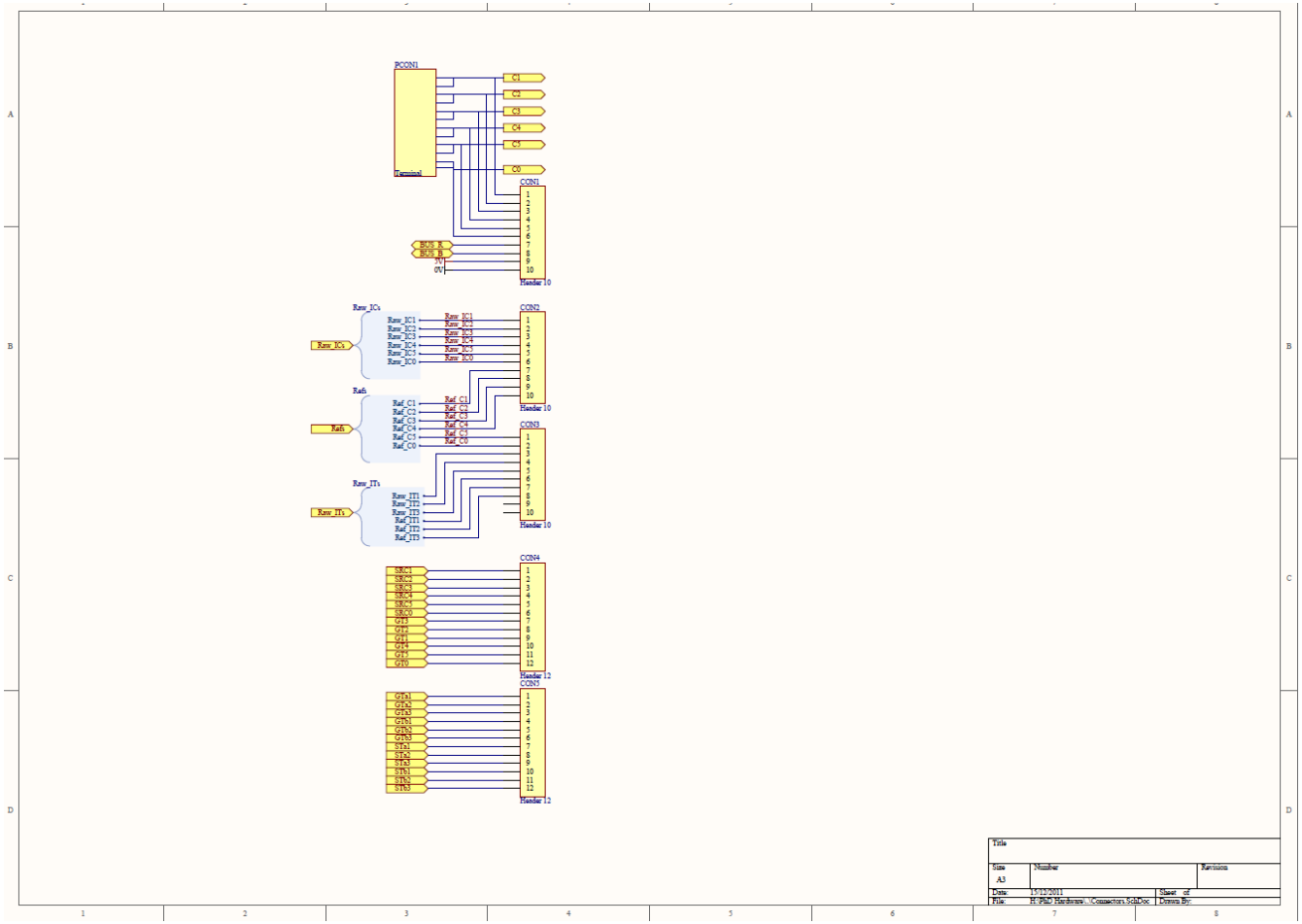
Figure A-2 – Converter board multiplexor subsystem schematic

The multiplexor subsystem contains the MOSFET bi-directional switches as well as current measurement for each multiplexed channel



The main equalisation converter is made up of the three winding transformer and the selector MOSFETs. Current measurement transducers are also included.

Figure A-3 – Converter board converter subsystem schematic



The connectors connect the board to the Li-ion capacitor stack. The gate drive signals and voltage and current measurements are connected via ribbon cable to the processor board.

Figure A-4 – Converter board connectors subsystem schematic

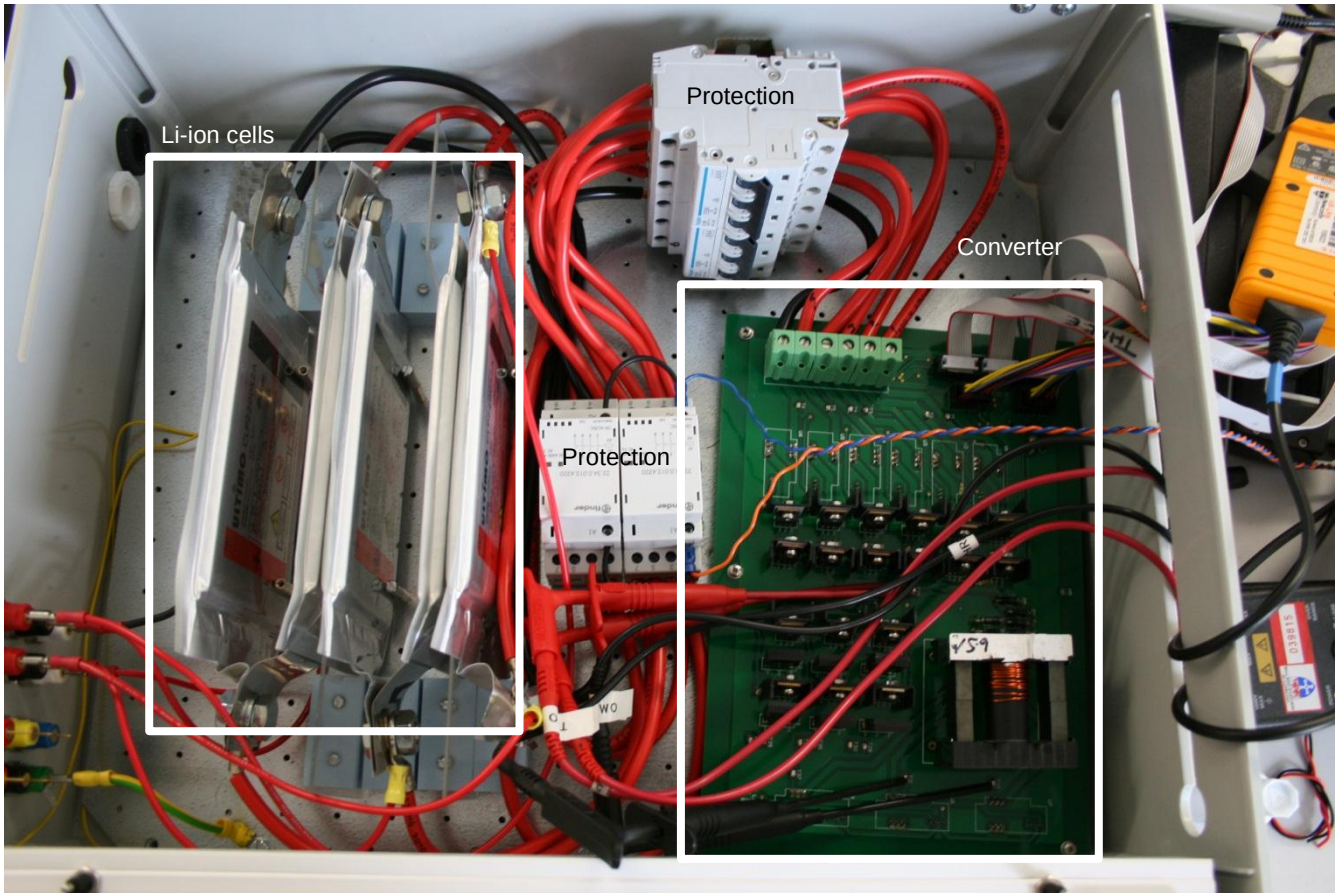
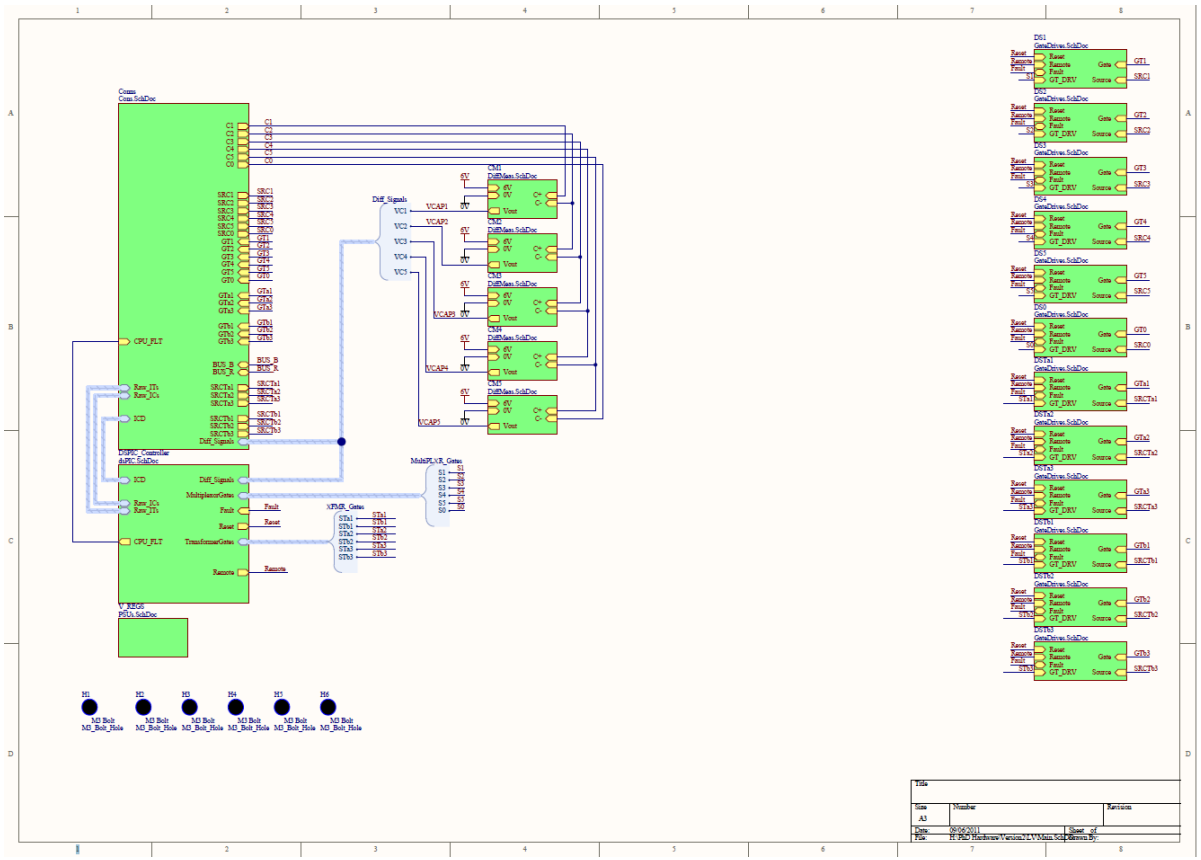


Figure A-5 - Photograph of converter board and Li-ion cell stack

Controller board



The controller board houses the microprocessor, gate drive circuits and differential measurement circuits. There are twelve identical gate drive circuits and five identical differential measurement circuits. The connectors subsystem interfaces with the converter board.

Figure A-6 - Controller board top level schematic

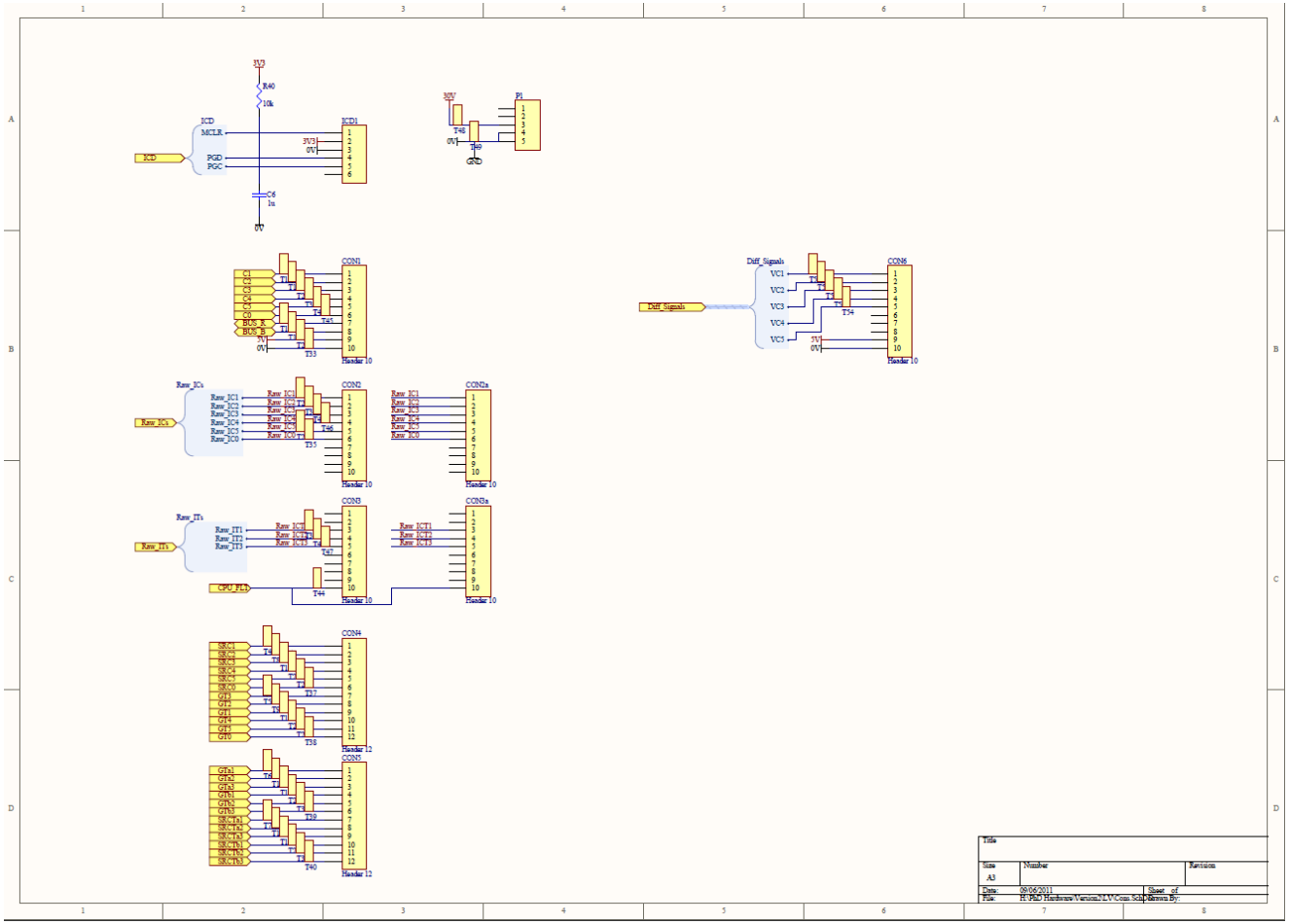
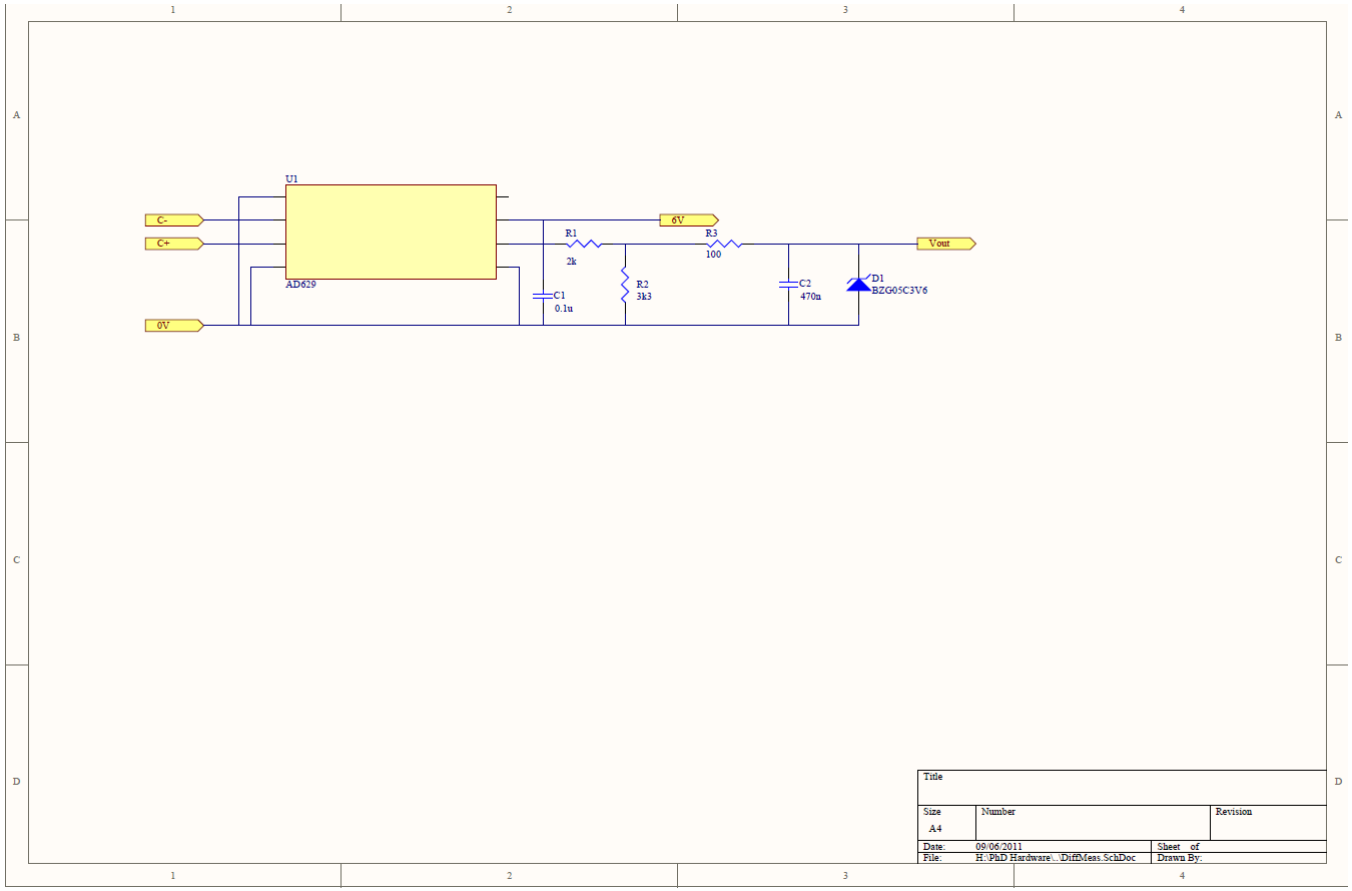


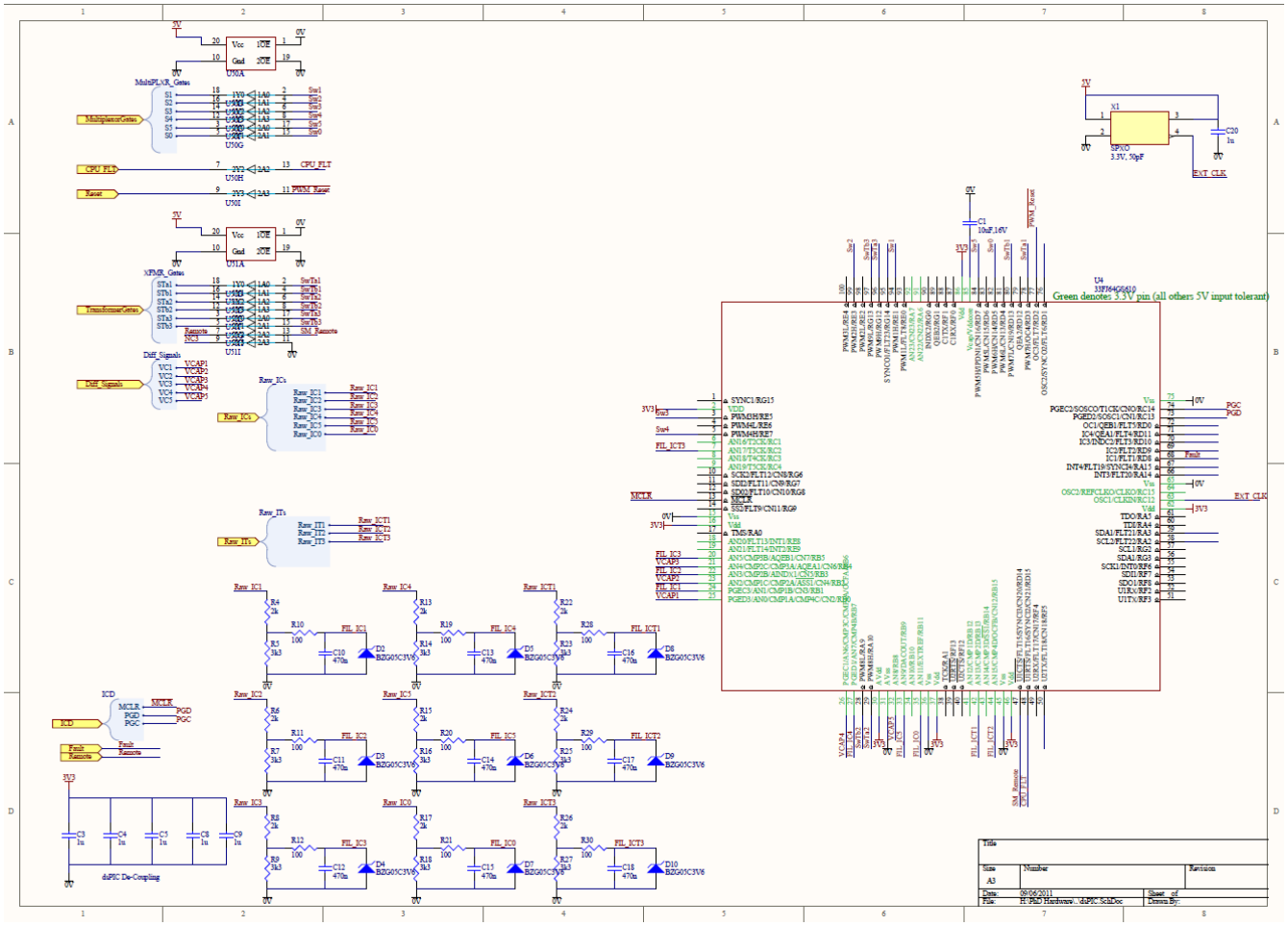
Figure A-7 – Controller board connectors subsystem schematic

The connectors are for gate drive signals to the converter board and voltage and current signals back. There is also a programming socket for the microprocessor and power supply header.



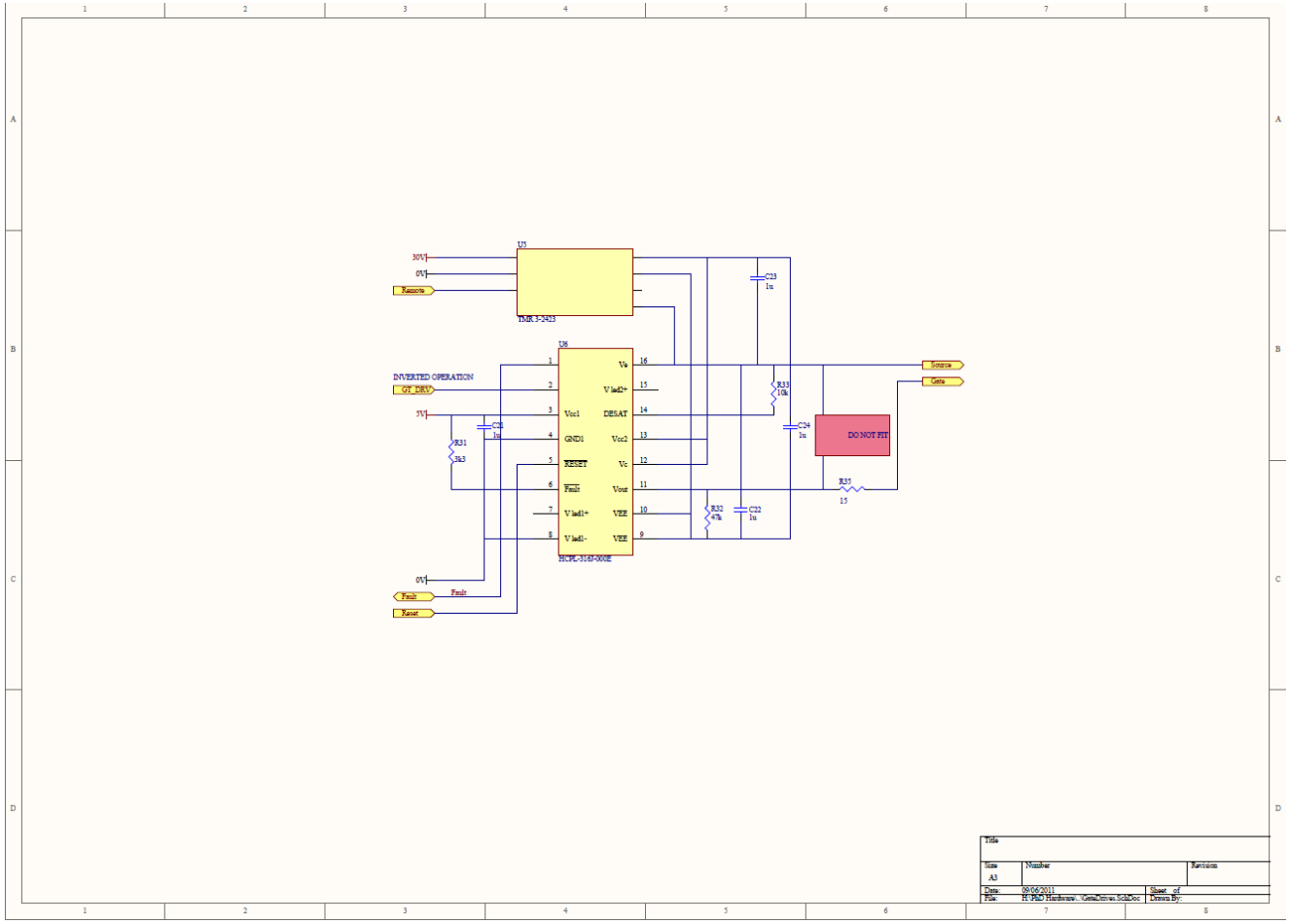
The differential measurement centres around the AD625 differential amplifier chip.

Figure A-8 - Controller board differential measurement subsystem schematic



The DSPic microprocessor is the heart of the control board. It manages the analogue and digital signals to the rest of the control board and converter board. The processor runs on 3.3V so a CMOS up-scalar and potential divider down-scalar are required.

Figure A-9 - Controller board microprocessor subsystem schematic



The gate drive circuit centres around the HCPL316 gate drive chip. An isolated DCDC converter is used to provide an isolated power supply to the gate drive circuit so it can operate at high common mode.

Figure A-10 - Controller board gate drive circuit subsystem schematic

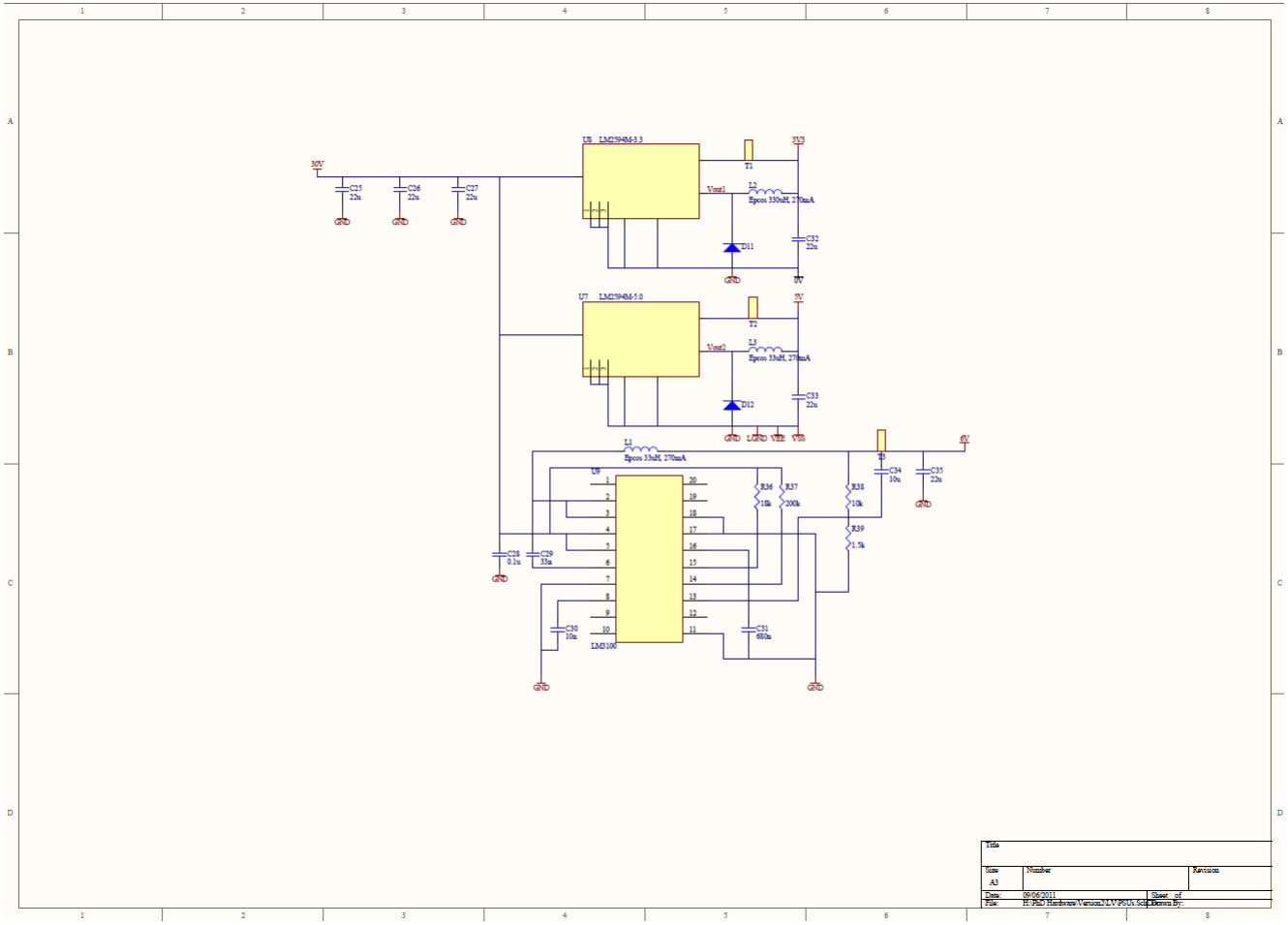


Figure A-11 - Controller board power supplies subsystem schematic

The circuit operates on three voltage levels. Three independent DCDC converters are used to provide 3.3V, 5V and 6V.

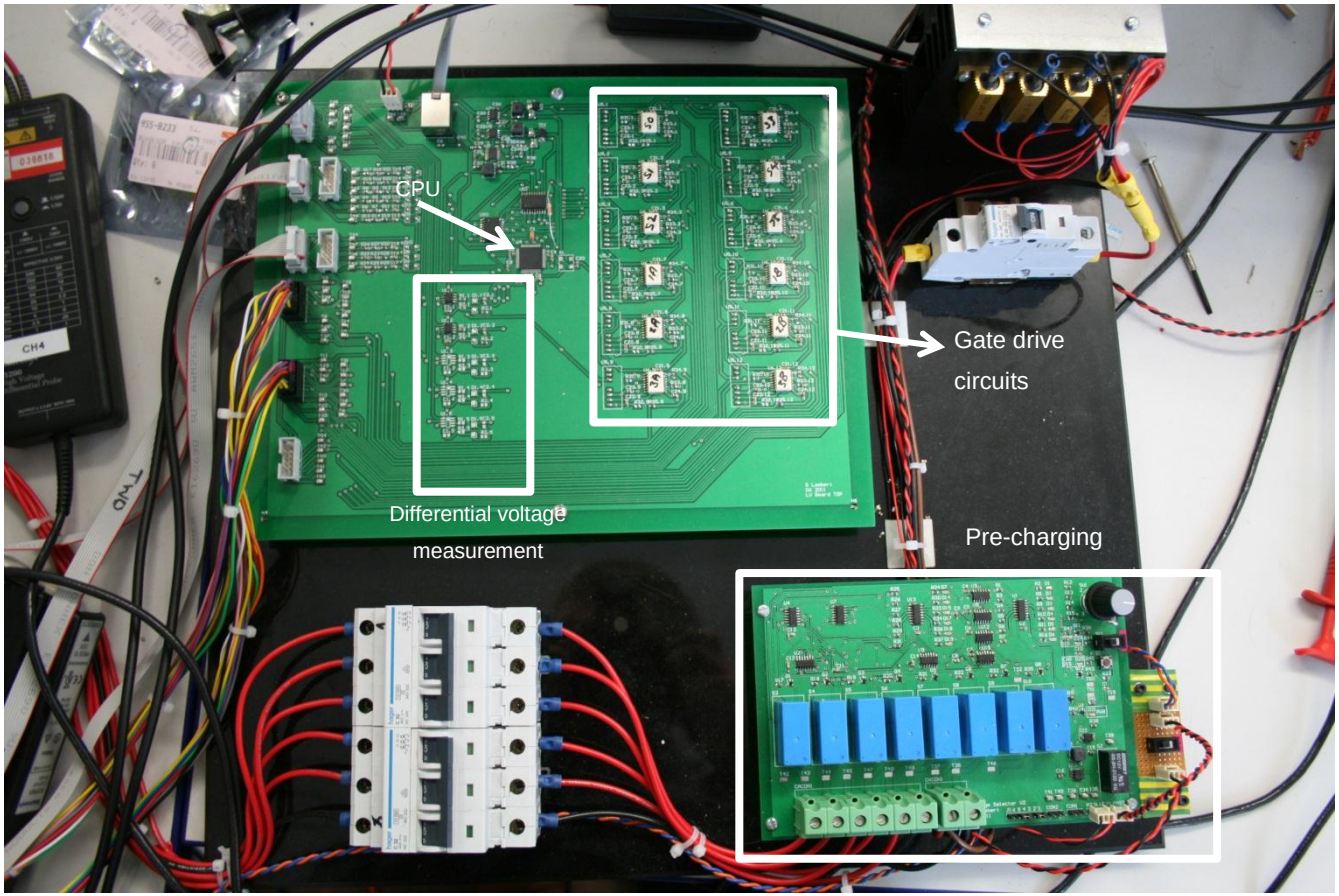


Figure A-12 - Photograph of controller board and interlocks board