Resilient Energy Harvesting Systems

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A thesis submitted for the degree of

Doctor of Philosophy

August 2011

Abstract

Developing resilient sensor systems for deployment in extreme environments is a challenge which silicon carbide, along with other wide band gap materials, stands to play a major role in. However, any system developed will be hindered in its usefulness unless the problem of providing a power supply in these extreme conditions is addressed.

This work addresses this need; a wireless sensor node conceived of standard off the shelf components was first developed and used as the basis for the design considerations required for a silicon carbide sensor node. The silicon system developed uses a piezoelectric energy harvester for the power supply and exhibits favourable operating characteristics for low vibration environments. It is capable of continuous operation at 120 mg (1.177 ms^{-2}) and at 40 mg operates with a system duty cycle of 0.05.

PZT, a standard piezoelectric energy harvesting material, was characterised to 300 °C to test its resilience to the conditions found in hostile environments. The material degrades considerably with temperature, with a decrease in Youngs modulus from 66 GPa at room temperature to 8.16 GPa at 300 °C. The room temperature value is repeatable once cooled with an observed hysteresis in the upper temperature range. The peak output voltage at resonance also varies with temperature, resulting in an 11.6% decrease in room temperature voltage once the device is heated to 300 °C. The output voltage at 300 °C is found to be 2.05 V, a considerable decrease from the initial 11.1 V output at room temperature. The decrease in voltage with temperature is not monotonic as maybe expected, the data showing that at 473 K there is an increase in output voltage which is caused by a decrease in mechanical damping.

SiC pin diodes were fabricated with wide drift regions to promote a large depletion width, in order to maximise the capture cross section of incident light on the devices. The large drift region produces a high series resistance. However, fill factors above 0.7 show that the device is not significantly affected. SiC is shown to be an effective UV harvester with an observed increase in output power from 0.17 mWcm^{-2} at room temperature to 0.32 mWcm^{-2} at 600

K. Fill factor also remains stable with temperature, indicating that the device is not affected by variation in parameters such as shunt and series resistances or the ideality factor. There are current technological difficulties which preclude the manufacture of large area silicon carbide solar cells and as such, an alternative networking solution is presented as a way to increase the output power of the devices. Given that these devices would be subject to long term high temperature exposure, a 700 hour thermal stress test is carried out at 450 °C to explore the failure mechanism of the devices. There is an observed decrease in device fill factor which indicates that the device suffers increasing degradation. The data shows that this is caused by increasing series resistance, which reduces the devices ability to output power. SEM imaging and SIMS analysis show this is likely caused by significant metal diffusion in the contact stack which could potentially be overcome by the addition of an alternative diffusion barrier.

Once energy is generated by an energy harvester is must be stored so that it can be used when required. To this end both substrate and on chip storage technologies are discussed in the forms of AlN and HfO_2 metal insulator metal (MIM) capacitors. To test the feasibility of both solutions, AlN and HfO_2 MIM capacitors were characterised to 300 °C. The HfO_2 device leakage has a strong temperature dependence as observed in the IV characteristics and the capacitance density does not scale according to parallel plate theory. However, the devices can be effectively networked and their leakage reduced with series connection. The internal voltage decay of the device is reduced with series connection, due to the differing work functions of the metal-insulator contacts. The alternative AlN solution exhibits substantially weaker temperature dependance and significantly improved film quality. The data shows no existence of a barrier at the insulator - metal interface, as observed in the HfO_2 device IV characteristics. The extracted activation energy is stable with temperature at 1.26 +/- 0.15 eV indicating a trap assisted leakage mechanism. This method is more suitable to fabrication of large area storage as it can be fabricated off chip on a less expensive substrate and the devices fabricated exhibit a higher yield than the HfO_2 devices.

To Leonie

Acknowledgements

Throughout the course of my PhD I have had the great fortune to be supported and influenced by a remarkable group of people. The support of those mentioned below, as well as many others, has been invaluable.

Thank you to my supervisors, Dr Alton Horsfall and Prof. Nick Wright, who have guided me through my PhD. I am grateful to Alton for taking a chance and allowing me the freedom to do a project which encompasses a vast range of disciplines. The trust he placed in me to undertake this boundless project to the fullest of my abilities is inspiring to say the least. The freedom and range he has given me over the last three years has made me realise that there is no predefined path of what one must do with an electrical engineering degree. I thank him also for his commitment to getting the best out of me during both my undergraduate and postgraduate studies, his guidance and feedback has been invaluable and is reflected in the publications and awards associated with this work.

I would like to thank some of the other academics who made this PhD possible. I would like to thank Dr Jon Goss for his marvellous pre-conference presentation preparation and brilliant explanations of materials and physical concepts, without which I would have lost many more days in the library. I would also like to thank Dr Steve Beeby at Southampton University for giving me a tour of his lab in the first year of my PhD, much of what I learnt on that tour has formed the foundation of part of this thesis.

I would like to thank my friends, who have provided years of brutally honest advice interspersed with outrageous comedy, without which this PhD would have been much harder. Special mentions to Dan, Bear, Ben, Mark, Frank, Dave and Gerry among many others.

My parents have been a constant source of support and encouragement throughout the two decades which my education has now spanned. The sacrifices they made for my education have allowed me to develop the skills and determination needed to complete this thesis.

Finally, I wish to thank Leonie, who, as my girl friend, has suffered the great misfortune of being the one person who asks me, everyday, how my day was. To say that these answers have the tendency of becoming a relentless diatribe would be an understatement, however she has shown unwavering support, enlightened advice and guidance throughout my PhD. She has done all this whilst spanning the two worlds of neuroscience and electrical engineering herself, I am truly grateful for her love and support.

Journal and Conference Publications

S. Barker, R.C. Stevens, K. Vassilevski, I.P. Nikitina, N.G. Wright and A.B. Horsfall, "Silicon Carbide UV Based Photovoltaic for Hostile Environments", Presented as a poster at the "The 7th European Conference on Silicon Carbide and Related Materials" 2008, Barcelona, Spain.

S. Barker, B. Miao, D. Brennan, N. G. Wright and A. B. Horsfall, "High Temperature Storage for Energy Harvesting in Hostile Environments", Presented at "The 8th Annual IEEE Conference on Sensors" 2009, Christchurch, New Zealand.

S. Barker, B. Miao, D. Brennan, K. Vassilevski, N. G. Wright and A. B. Horsfall, "Silicon Carbide based Energy Harvesting Module for Hostile Environments", Presented as a poster at "The 13th International Conference on Silicon Carbide and Related Materials" 2009, Nurnberg, Germany.

S. Barker, K. V. Vassilevski, N. G. Wright and A. B. Horsfall, "High Temperature Vibration Energy Harvester System", Presented as a poster at "The 9th Annual IEEE Conference on Sensors" 2010, Hawaii, USA.

S. Barker, D. Brennan, N. G. Wright and A. B. Horsfall, "Piezoelectric powered wireless sensor system with regenerative transmit mode", Wireless Sensor Systems, IET, 1 (2011)

S. Barker, K.V. Vassilevski, I.P. Nikitina, N.G. Wright, A.B. Horsfall, "Thermal stress response of Silicon Carbide solar cells", Accepted as a poster presentation at "The 14th International Conference on Silicon Carbide and Related Materials" 2011, Cleveland, USA.

M. H. Weng, **S. Barker**, R. Mahapatra, B. J. D Furnival, N. G. Wright, A. B. Horsfall, "Study of the Interface Properties of $TiO_2/SiO_2/SiC$ by Photocapacitance", Presented as a poster at "The 8th European Conference on Silicon Carbide and Related Materials" 2010, Oslo, Norway.

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Symbol	Meaning	Units
PZT	Lead Zirconate Titanate	
4H-SiC	4H poly type silicon carbide	
AC	Alternating Current	A
g	Acceleration expressed as an amount of gravity	
ϵ_0	Permittivity of free space	Fm^{-1}
d	Separation of capacitor plates	m
C	Capacitace	F
Q	Electric charge	C
CMOS	Complimentary Metal Oxide Semiconductor	
CIGS	Copper indium gallium selenide	
CdTe	Cadmium Teluride	
V_L	Load Voltage	V
d_{33}	33 Mode Piezoelectric coefficient	pC/N
d_{31}	31 Mode Piezoelectric coefficient	pC/N
f_0	Resonant Frequency	Hz
DC	Direct Current	A
C_p	Piezoelectric device capacitance	F
PWM	Pulse Width Modulation	
MOSFET	Metal Oxide Field Effect Transistor	
JFET	Junction Field Effect Transistor	
V_{dd}	Supply voltage	V
V_{ref}	Voltage of reference voltage	V
$V_{ref-sample}$	Digital representation of V_{ref} as a portion of V_{dd}	
MEMS	Micro Electro Mechancical Systems	
AlN	Aluminium Nitride	

Symbol	Meaning	Units
ZnO	Zinc Oxide	
BaTi	Barium Titanate	
k	Stiffness	N/m
m_t	Tip Mass	kg
m_c	Mass of cantilever	Kg
ζ_m	Mechanical Damping Coefficient	
ζ_e	Electrical Damping Coefficient	
ζ_e	Total Damping Coefficient	
PID	Proportional Intergral Differential	
K_{sys}^2	Electromechanical system coupling coefficient	
ω_{oc}	Open circuit resonance	rad/s
ω_{sc}	Short circuit resonance	rad/s
R_{sh}	Shunt resistance	Ω
Y_0	Peak vibration amplitude	m
m	Mass	Kg
ω	Frequency	Hz
Z_1	Peak displacement	m
P	Power	Watts
T	Temperature	Kelvin
T_h	Hot electrode	
T_c	Cold electrode	
R_n	Resiance of n-type material	Ω
R_p	Resiance of p-type material	Ω
R_L	Load Resistance	Ω
ZT	Figure of Merit of thermoelectrics	
σ	Conductivity	S
Bi_2Te_3	Bismuth Telluride	
PbTe	Lead Telluride	

Symbol	Meaning	Units
SiGe	Silicon Germanium	
Ni	Nickel	
J	Current density	Am^{-1}
k_B	Boltzman constant	J/K
A	Area	m^2
α	Seebeck coefficient	V/K
I	Current	Amps
l	Length	m
t	time	s
I_o	Reverse saturation current	Amps
V	Voltage	Volts
I_{ph}	Photocurrent	Amps
n	Ideality factor	
V_{bi}	Barrier height	Volts
N_A	Acceptor doping concentration	cm^{-3}
N_D	Donor doping concentration	cm^{-3}
N_B	Bulk carrier concentration	cm^{-3}
E_c	Conduction band energy	eV
E_v	Valence band energy	eV
E_D	Donor energy level	eV
C	Capacitance	Farads
q	Elementary charge	C
N	Incident photo flux	
D_n - D_p	n- and p-type Einstien coefficient	
τ_n - τ_p	Carrier lifetimes	s
DIL	Dual Inline Package	
I_{sc}	Short circuit current	A
V_{oc}	Open circuit voltage	V

Symbol	Meaning	Units
I_{max}	Current at peak power point	A
V_{max}	Voltage at peak power point	V
ε_m	Maximum electric field	Vm^{-1}
W	Depletion region width	m
n_i	Intrinsic carrier concentration	cm^{-3}
ϵ_s	Dielectric constant	
x_n	$n-$side depletion region distance	m
φ	Potential	V
μ_n	Electron mobility	$cm^2V^{-1}s^{-1}$
μ_p	Hole mobility	$cm^2V^{-1}s^{-1}$
σ	Conductivity	Siemens
E_g	Energy gap	eV
λ	Wavelength	m
h	Planc constant	J s
c	Velocity of light	ms^{-1}
FF	Fill Factor	
SEM	Scanning Electron Microscope	
Ti	Titanium	
Al	Aluminium	
Cr	Chrome	
Au	Gold	
Si	Silicon	
O	Oxygen	
HfO_2	Hafnium dioxide	
PVD	Physical Vapour Deposition	
SAW	Surface Acoustic Wave	
SiO_2	Silicon dioxide	
Pt	Platinum	

Symbol	Meaning	Units
Hf	Hafnium	
A*	Richardson Constant	
E$_a$	Activation Energy	
MIM	Metal Instulator Metal	
OCVD	Open Circuit Voltage Decay	

Contents

Chapter 1

Introduction

1.1 Background

As we strive to understand more about our surroundings and our impact on the planet, we are increasingly turning to electronics and sensor systems to help collect the necessary data to make accurate predications and adjustments. The size, cost and power consumption of such electronics has decreased considerably over the last decade and, where it was once necessary to install a hardwired sensor system, we are now able to place ad hoc wireless sensor nodes which can transmit relevant data back to a central hub. This has vastly reduced the cost of monitoring systems and has allowed the installation of wireless monitoring in environments previously thought impractical. Although the power consumption of such sensor systems has significantly decreased, there is still a need for a large onboard battery to power the system electronics. The space requirement for this battery is often considerably larger than any other component in the system and, for a sensor deployed for a long period of time, can often make up the majority of the system size.

Consider a wireless gas sensor which is designed to operate for 10 years with an average power consumption of 1mW. Using current battery technology, with an energy capacity density of 3.78kJ/cm^3, the battery required to power this would need to be 83cm^3. Such a battery will significantly reduce the deployability of the system and a smaller one would lead

to regular replacements which could be expensive or even dangerous. It is possible, however, to convert ambient environmental energy into electrical energy which can be used to power the system. Such devices are called energy harvesters and can be used to supplement a secondary battery or replace it altogether.

1.2 Resilient Technology

Our desire to understand more about the built and natural environment means that there is an ever increasing array of places in which we want to deploy sensor systems. From the mundane requirements of a farmer's field to the extreme conditions of a volcano, there is an enormous variety of potential deployments for sensor systems. The more extreme an environment however, the more difficult it is to design a system suitable for it.

Traditional silicon based electronics operate well in benign environments. Once extreme levels of temperature, corrosive gas or radiation are introduced however these begin to fail. Given this limitation, it is apparent that some of the most interesting processes and environments are too extreme for silicon. With this in mind it is important that we explore new technologies which can be used to make sensor nodes that are deployable in these inhospitable environments.

Silicon carbide electronics and other wide band gap materials have enabled the development of resilient electronics which can operate in such environments. These resilient materials have made it possible to design and make simple circuits which are ideal sub systems to be used in a simple wireless sensor node. Although simple circuits can be manufactured and operated at elevated temperatures there is no portable power source suitable for use with them, as current batteries can not operate in extreme environments. It is the aim of this thesis to outline the research and results found in studying energy harvesting technologies for hostile environments with particular focus on high temperature environment such as that of a volcanoe fumarole or a car exhaust.

1.3   Thesis Outline

Chapter 2 presents a review of the current literature in the relevant fields. Little work has been carried out into the field of high temperature energy harvesting, or indeed high temperature wireless sensor nodes, and so a basic discussion of easy aspect of a system is discussed and it's merits for potential use in a hostile environment discussed where appropriate.

Chapter 3 discusses the development of a room temperature silicon system, it is extensively characterised and used to show some of the unique considerations in developing these systems. The development of the silicon system is used as the basis for identifying the limitations of the current technology and where developments must be made for the realisation of a resilient sensor node.

Chapter 4 presents work carried out in the field of piezoelectric energy harvesting. The chapter presents a discussion of piezoelectric theory related to the needs of experimental characterisation at elevated temperatures. The experimental method is presented and the test system discussed. The bulk of the chapter is spent on discussing the experimental results obtained from high temperature tests of PZT piezoelectric devices and highlights the limitations of current technology.

Chapter 5 focusses on photovoltaic energy harvesting and how some of the limitations of silicon technology can be over come with the use of silicon carbide devices. The chapter presents the fundamentals of the photovoltaic theory and then discusses results collected from extensive high temperature characterisation of silicon carbide pin photovoltaic devices. An investigation is undertaken in how the device response varies with wavelength and temperature and a solution to some current technological limitations of silicon carbide technology with regards to solar cells is also discussed. It concludes with an investigation into the effects of prolonged temperature exposure and shows how the devices respond to long term thermal stress.

Chapter 6 introduces two potential solutions to storing the harvested energy, one focussing on on chip storage which could be incorporated into a monolithic silicon carbide system and

the other on integrating storage into the substrate of a hybrid system. To investigate this potential, metal insulator metal (MIM) capacitors were fabricated for high temperature characterisation relevant to their intended application. The capacitance variation with respect to temperature and voltage are analysed for both 35 nm and 60 nm HfO_2 MIM capacitors, which are representative of those that would be incorporated for on chip storage. It is found that these devices are heavily temperature dependant, but series networking improves their operation at elevated temperatures. 390 nm thick AlN MIM capacitors were also fabricated and their high temperature leakage and capacitance behaviour characterised. The reduced leakage of these films and the overall higher device yield means that they do not require series or parallel connections and given the reduced cost of implementing such a storage system this is identified as a more viable option.

Chapter 7 is the conclusion which brings together the threads from all the experimental results and concludes that although steps can be taken in to resilient energy harvesting technologies there are still basic areas development which need to be undertaken before a self powering resilient wireless sensor system can be realised.

Chapter 2

Literature Review

2.1 Energy Harvesting Introduction

With the advent of low power wireless communication, it is now feasible to deploy wireless sensors for long periods of time, with little maintenance required other than to replace the onboard battery. Deploying large scale, self healing wireless sensor networks in industrial environments to analyse processes, machinery and environmental health will enable us to further improve the efficiency of some of the most energy intense processes. The finite energy stored in the batteries of these sensor nodes remains a limit on the deployability of these systems. Although they can be designed to make the onboard battery last in excess of 10 years, the volume taken up by, and the disposal upon exhaustion of, these batteries limits the overall usability of wireless sensor networks.

Energy harvesting stands to make significant improvements to this by mitigating the need for an onboard primary battery and replacing it with a renewable source of electrical power harvested from the environment in which the node is placed. From vibrations to thermal gradients, there is significant amounts of energy available in industrial and natural environments. This wasted energy is often sufficient to power a wireless sensor node for the duration of its life.

Much research has been conducted into the field of energy harvesting in the past decade in the search of the highest power density in a variety of environments. Harvesters which can power a system from the vibrations of an air conditioning unit [1] or the impact of a human foot with the ground [2] have been demonstrated and show promise of what can be achieved. Spin out companies such as Perpetuum, in England [3], and Enocean [4], in Germany, demonstrate the commercial value and impact of energy harvester technology for the industrial and commercial spaces.

The impact that energy harvesting can have on many applications and environments has recently been demonstrated, however extreme environments such as those found in jet engines, volcanoes and car exhausts have been left largely untouched by these developments. Environments such as these are problematic for standard electronics as they are high temperature, chemically corrosive and experience massive mechanical stress variations. With the exception of SOI devices, tranidional silicon electronics is limited to a maximum operating temperature of 150 °C and so monitoring the gas variations in the exhaust of a car or a volcanic fumarole are beyond the capabilities of traditional electronics.

2.2   Silicon Carbide

Silicon carbide is a wide band gap semiconductor and as such can be used to produce electronic devices which can operate in conditions far more extreme than what is currently achievable with silicon. The 4H-SiC polytype has a room temperature band gap of 3.23 eV [5] making it operable at temperatures in excess of 300 °C [6, 7, 8], receive a total ionising dose of radiation greater than an unshielded return trip to Jupiter [9] and operate, unprotected, in a stream of corrosive gases, such as those produced by volcanoes [10]. Over the last two decades the prospect of what silicon carbide can do for the high power industry has been widely discussed in the literature [11]. It is only recently however, that it's true potential for signal level devices has been realised [12] even though it has larger diode and transistor turn on voltages than silicon [13, 14].

Developing resilient sensor systems for deployment in these environments is a challenge which silicon carbide, along with other wide band gap materials, stands to play a major role in. However, any system developed will be hindered in its usefulness unless the problem of providing a power supply in these extreme conditions is addressed. Conventional batteries are incapable of high temperature operation and alternative technologies, such as sodium chloride cells which ideally operate at temperature in excess of 300 °C [15], are so large that no system could be feasibly be powered by them. Running power cables to sensors placed in inhospitable places is not a credible alternative, as long lengths of cable degrade with time, are expensive and maintenance would pose unnecessary risk to personnel.

2.2.1 Requirements and Concessions

Standard wireless sensor nodes have a battery onboard and so the system designers have the benefit of knowing how much energy is stored, within the tolerances of the specifications. They can then design the system around the project requirements, find suitable operating parameters and hence components to meet the demands. Such systems tend to be designed with the main focus on the quantity of data which can be transmitted in the shortest time frame, before the battery needs replacing. The focus is on verbose data logging rather than appropriate data logging. In situations where the monitored parameters are highly dynamic and vary rapidly, such as the gas concentrations emitted from a combustion engine, then high speed, high bandwidth data logging is required. If, however, the system is stress monitoring in a bridge that is designed to survive 200 years, then transmitting data every 100 ms is not useful. In fact a system designed to transmit once a day and then more often if it discovered a significant change would be more realistic. In such a system it would be possible to harvest energy from small solar cells for surface sensors or micro virbration systems for those embedded into the concrete structure.

Designers implementing energy harvester powered systems do not have the luxury of an onboard battery and so more energy efficient and flexible, methodologies must be implemented. The focus in energy harvester powered systems is not to transmit the highest

quantity of data in the shortest time but, instead, to transmit information when possible based on the energy that the system has harvested. This leads to sporadic data transmission which is ideal for monitoring systems which are less prone to highly dynamic change. For instance, the wear on a piece of industrial equipment can be measured over a period of weeks and months and would be ideal for an energy harvester powered sensor system transmitting a number of times an hour dependant on the energy available.

Although using an energy harvester powered system adds design complications, it can significantly reduce the through life cost of deployed systems. It also reduces the number of wasted batteries disposed of each year, which will have beneficial environmental impacts as the deployment of these systems increases.

2.3 The challenge of deploying sensor nodes in hostile environments

Using the case of a sensor designed for permanent placement in a volcanic fumarole the process of designing and developing a resilient wireless sensor node can be discussed. It is believed that monitoring the gas concentrations emitted by a volcano can give insight into its current state and could accurately predict an eruption [16]. However, the gas emitted by a volcano is highly corrosive and would very quickly render a silicon solid state gas sensor inoperable when exposed to the gas [17]. The problem of the gas sensor being destroyed by corrosive gases can be solved with alternative materials such as silicon carbide, which is resistant to the gasses emitted from a volcano [10]. Using a solid state MOS silicon carbide gas sensor array a resilient sensor can be made which is able to differentiate between the individual gasses emitted from the volcano.

These gas sensors change both capacitively and conductively when exposed to different gases [17] and so the response can be monitored in either manner. Figure 2.1 shows the response of a silicon carbide gas sensor in a combustion engine, it shows how the sensor is able to detect that cylinder 1 is operated in excess fuel conditions. It is clear that the

voltage across the sensor changes and so a problem in the engine can be more accurately pin pointed. Although this sensor is only detecting the change in one gas, multiple sensors could be fabricated on to an array to give more in depth measurements.
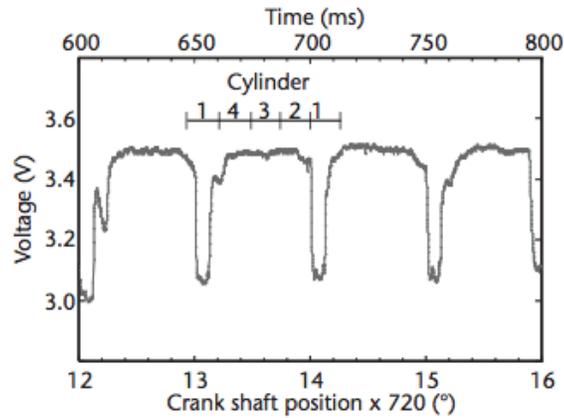
Figure 2.1: Silicon carbide gas sensor response at high temperature showing the change in sensor voltage level when one engine cylinder is fuel rich and not operating correctly

Silicon carbide gas sensors are resilient to corrosive gasses and they operate well at elevated temperatures, such as those in a car exhaust or a volcano. Simply replacing the gas sensor in a wireless system and then protectively packaging the silicon electronics will not solve the issue as the these environments can reach over 500 °C [18]. The gas sensor needs to be placed, unshielded, inside the fumarole to give an accurate measurement, the temperature of which will exceed the operating point of silicon [19].

One solution would be to connect the sensor to the end of long wires and place the silicon system further away in a cooler location. This would degrade the measurement signal from the sensor and potentially render the system useless. This means the system also needs to be fabricated from resilient electronics so that it can be packaged along with the sensor and placed in the same location.

Silicon carbide JFETs provide a reliable alternative to silicon MOSFETs at elevated temperatures and can be used to amplify and transmit signals from a hostile environment. Work has shown that simple AM modulated signals can be transmitted at elevated temperatures using a Colpitts oscillator with 2 SiC JFETs [12]. Figure 2.2 shows this incorporated into a proposed high temperature wireless sensor node, whereby the variation in capaci-

tance with respect to gas concentration of C_{sense} modulates the oscillators output signal amplitude.
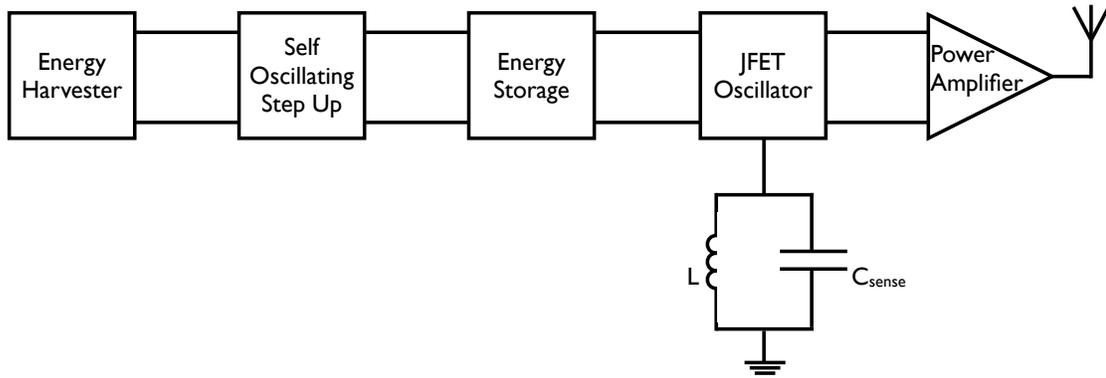
Figure 2.2: System diagram shows core components to a high temperature wireless sensor node

This system would be capable of operating at elevated temperatures for extended periods of time, however the power supply suitable for this would either make the system awkward to install or inoperable in these conditions. This is because standard battery technology is limited to operating temperatures of around 60 °C and so is unable to sit in the fumarole due to the high temperatures [20]. High temperature batteries do exists, in the form of sodium based batteries but these can be quite large and are generally better suited to higher power applications [15]. With this in mind it is important to develop suitable alternatives based on energy harvesting technologies. This would allow for the creation of long deployment wireless gas sensing which can be used in conjunction with other systems such as that developed by Geoffrey Werner-Allen which uses an array of wireless infrasound detectors to monitor volcanic activity at Volcan Tungurahua [21]. Their work shows the feasibility of instrumenting a volcano and giving more detailed information than previously possible with wired systems.

2.4 Harvesting Techniques

The examples above outline the differences between battery powered and energy harvester powered systems and highlights the primary design consideration. There are a number of other factors which must be taken into account when designing such systems, and these will be outlined in the following sections.

2.4.1 Vibration

Electromagnetic

Kinetic is the easiest form of energy to convert into electrical power, from large scale power stations to wind farms, the process of using magnetic fields to generate electricity is exploited daily to power our towns and cities. These two examples rely on the interaction of rotating elements as the power generating mechanism. However, this method does not scale well to portable energy harvesters. It is much easier to implement an inertial based system which relies on the relative displacement of a magnetic mass around a fixed coil to produce electrical energy. Research at both the micro [22] and milli scale [23] on this form of energy harvesting has been carried out and systems have been effectively powered from very small input vibrations. An example of which has been published by Beeby *et al* at both the micro [22] and milli scale as part of the VIBES project. The device is shown in figure 2.3 and consists of 4 magnets attached to the tip of a small cantilever which moves about a fixed coil. The magnets are each 1 x 1 x 1.5 mm^3 and the cantilever beam is 9 mm long, the first 7 mm of which are 3 mm wide with the remaining being 4 mm wide. The resonant frequency of the structure is further tuned to 52 Hz with tungsten tip masses [23].

An alternative is to have a fixed magnet and the coil move about that to harvest the energy, this adds further complication however as the wires are no longer fixed. At elevated temperatures such weaknesses are likely system failure points.

The final device produced a peak power of 46 μW from an acceleration of 60 mg (0.06 x
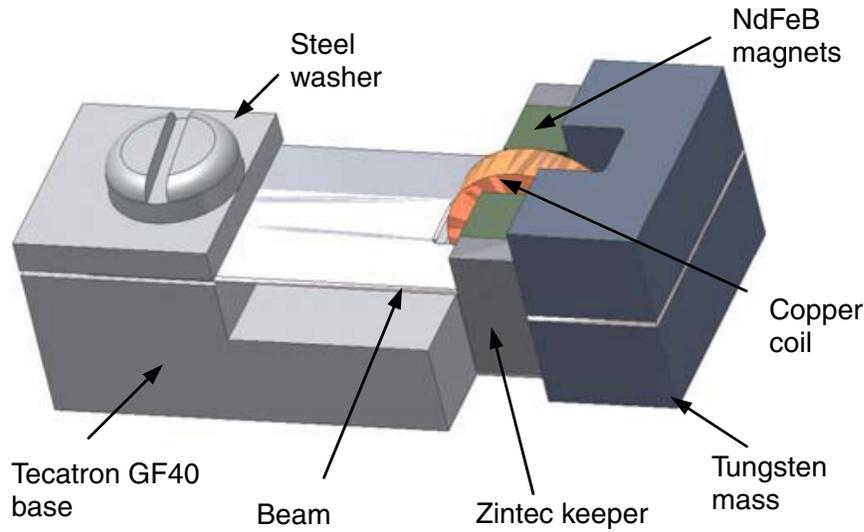
Figure 2.3: Electromagnetic energy harvester example

9.81 m/s^2) across a 110 Ω load. The output voltage was only 428 mV, however when added to a full system with voltage doublers and a PIC microprocessor this harvester can power a simple wireless sensor node for extended periods of time [1]. Electromagnetic harvesters are low impedance sources and as such produce small voltages compared to their output current, requiring that the voltage needs to be stepped up before it can be used in a circuit.

Electrostatic

Electrostatic energy harvesters use vibrations to change the separation distance between two capacitive elements. By placing charge on the plates and then changing the separation distance, the mechanical energy is converted into electrical power. There is a requirement, however, to pre-charge the plates and this can reduce the system efficiency [24] as a long term, reliable, voltage source such as a battery has to be included to provide this pre charge. An alternative is to use a dielectric which creates a charge separation across the plates, these materials are not suitable for use at high temperatures however and so in this project are of little use. Equation 2.1, where ε_0 is the permittivity of free space and in this case also the dielectric given that the plates are separated by air or vacuum, A the area and d the separation distance, describes how the physical properties of the device influence the

capacitance. It shows that C is inversely proportional to d and highlights that if d were to vary periodically with time so would C.

$$C = \frac{\varepsilon_0 A}{d} \tag{2.1}$$

Relating this to equation 2.2 where Q is the charge stored on the plates, V the voltage across them and C the capacitance it is clear that if Q or V is constrained whilst C varies there will be a change in the unconstrained parameter.

$$Q = CV \tag{2.2}$$
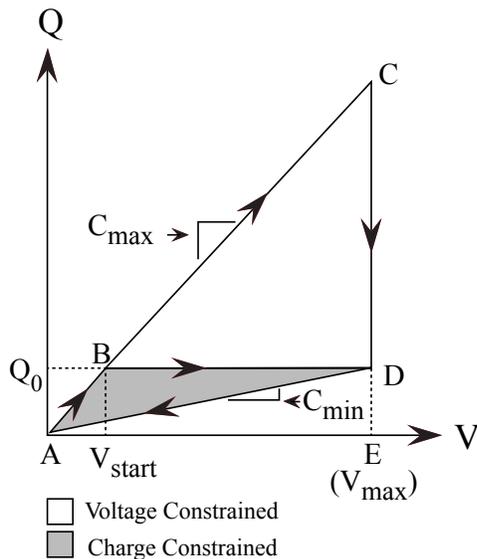
Figure 2.4: Energy conversion cycle comparison for electrostatic energy harvesting

Figure 2.4 highlights the difference between charge and voltage constrained methods, the area contained by the path ACDA shows the net energy produced by the voltage constrained method [25]. The area of path ABDA shows that the energy produced by the charge constrained method is considerably less than that of the voltage constrained method. The benefit of using the charge constrained method is that no secondary voltage level is required and the power electronics are less complex. There has been much work performed in this field

and the main focus has been on reducing the size of the devices from centimetres to small micro harvesters [26]. However, the electronics for such systems remain somewhat more complex than either of the other vibration harvesting methods, these complex electronics render it unsuitable for use at elevated temperatures and any dielectric which could be placed between the plates would be subject to the same temperature limitations.

Piezoelectric

Piezoelectric energy harvesters exploit the piezoelectric effect to convert vibrations into electrical energy. This effect is explained in full in chapter 4 but, in summary, piezoelectric materials produce a voltage when they are strained. The ease of fabrication, and variety of materials exhibiting this property means that a large number of investigations have been undertaken to examine this form of energy harvesting. There are a wide range of devices used and tested including commercially available components [27] (MIDE QuickPak), custom fabricated bulk [28], [29] and thin film devices with CMOS compatible materials [30], [31]. Piezoelectric material has been chosen for the main focus of chapter 3 so detailed discussion of its properties is saved for then however in summary, piezoelectric energy harvesters can be fabricated from one of two bulk materials which can be formed into a device with no moving parts which can be easily designed to operte effectively in a wide range of target environments. The simple construction of such devices is favourable for use hostile environments as it has a reduced number of mechanical failure points.

2.4.2   Resonance

Vibration energy harvesters are mechanical filters which exhibit resonance at a certain frequency. Tuning the harvester resonant frequency to the target environments fundamental vibration frequency is advantageous to maximising the harvested energy from a given environment. One of the primary issues with vibration energy harvesters is the limited bandwidth of their resonance peak leading to systems having to be highly specific to a deployment environment and allowing little margin for error in the manufacturing process.

This is caused by the devices exhibiting high Q factors or, in the case of [23] and [26], they exhibit a non-linear variation in frequency. This limits their deployability to environments where the fundamental environmental vibration frequency does not change and in environments with varying temperature and pressure this can be difficult to guarantee.

$$Q = \frac{f_o}{\delta f} \tag{2.3}$$

The data in figure 2.5 and equation 2.3 describes how the Q-factor of a harvester can be determined. If a system has a Q-factor less than 1/2 it is over damped and will not freely oscillate, a Q-factor of 1/2 represents a system which is critically damped and may over shoot one or two times before settling. Neither of these situations is ideal for vibration energy harvesters as much of the energy in the system is being damped by the mechanical properties. A Q-factor above 1/2 is underdamped and shows a system will freely oscillate for a number of cycles after the driving vibrations terminate.

Systems with a high Q-factor have a narrow bandwidth however they tend to exhibit a greater peak output than systems with lower Q-factor and higher bandwidth. This is because the Q factor is how many times large the free tip displacement is than the input displacement at the base of the cantilever. As the device strain is proportional to the tip displacement so to is the output power. System designers therefore have to make a tradeoff between harvester bandwidth and peak output which can be problematic.

One solution to this is to use multiple harvesters, each tuned to different resonant frequencies, to expand the overall bandwidth of the harvester system. Figure 2.6 shows how such a system can be realised with 3 piezoelectric cantilevers each tuned, with masses m_1, m_2 and m_3, to different frequencies [32]. Such a system does produce an increased bandwidth but whilst one device is operating at resonance the other two are not producing any significant voltage and so are simply taking up space and adding parasitic capacitance to the harvester system.

An alternative solution is an active tuning solution which can dynamically change the
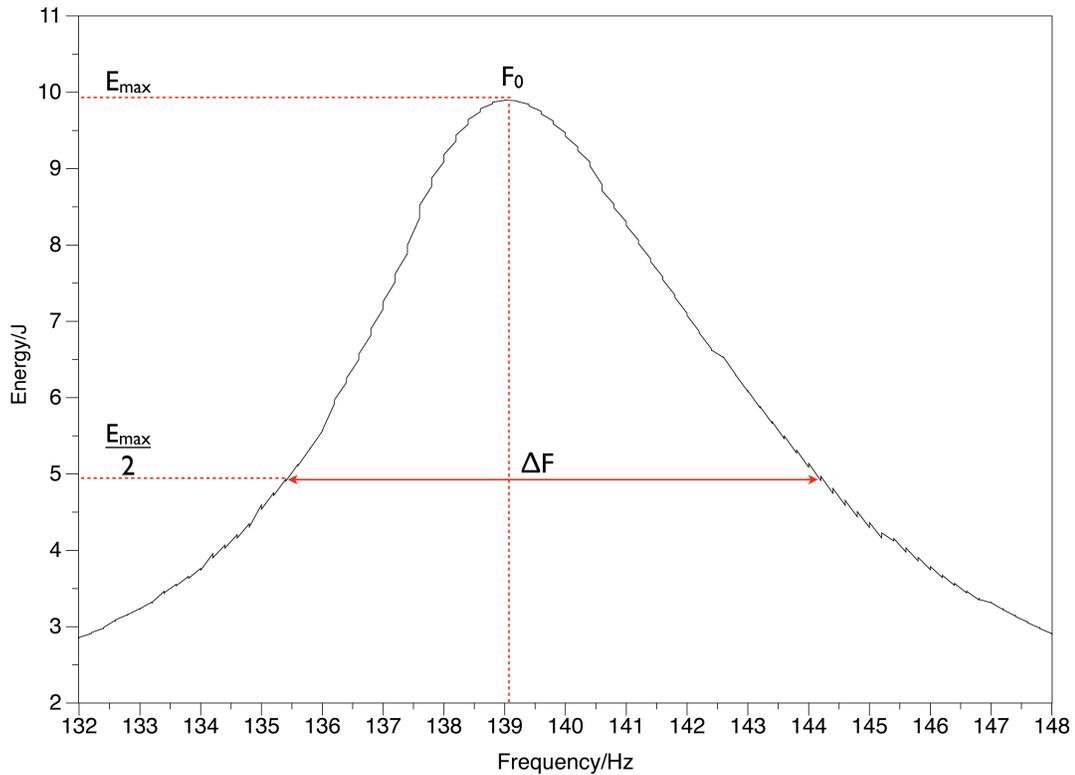
Figure 2.5: Resonance curve from a Piezo Systems cantilever demonstrating Q factor extraction

properties of the energy harvester to tune its resonance. The system proposed by D. Zhu *et al* uses the interaction between two magnets to apply tensile or compressive stress to the cantilever of an electromagnetic inertial energy harvester and so changes its resonant frequency [33]. The schematic for the system is shown in figure 2.7 and shows how the interaction between the tuning magnets will change the cantilever stiffness, and in turn, the resonance. The system is able to tune its resonant frequency to the environmental specta using onboard electronics, although this tuning takes several seconds and uses a considerable amount of energy it still leads to a system which is more effective at harvesting across a range of frequencies than fixed devices. Realistically this device would significantly reduce the installation time for an energy harvester powered wireless sensor network as a large store of initial energy could be used to tune the node when it was first deployed, this would reduce cost and time.
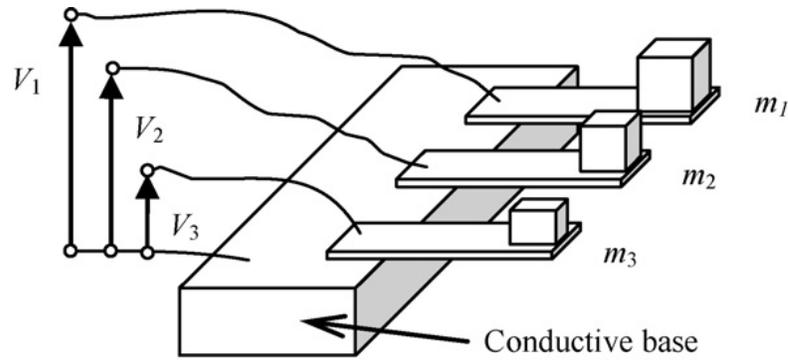
Figure 2.6: Multifrequency piezoelectric array
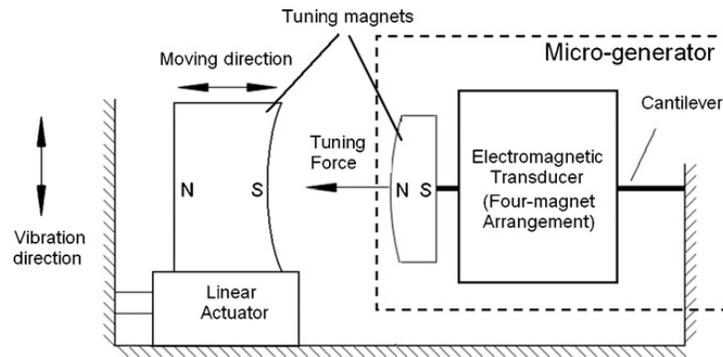
Figure 2.7: Closed loop controlled resonance tuning system

2.4.3 Solar

Photovoltaic devices are well established and have contributed to both large scale and micro power generation. This form of energy harvesting is particularly attractive for powering wireless sensor nodes due to the abundance of light in the built and natural environment. Typical energy densities of $0.1\text{mW}/\text{cm}^2$ in an office environment to $100\text{mW}/\text{cm}^2$ outdoors are not uncommon [34]. Solar cells are made up of a large number of series and parallel connected pn junctions, the requirements of the powered system will determine how the internal junctions are connected. By connecting devices in series the voltage produced by the cell overall is increased and when connected in parallel the current is increased, as such a wide variety of solar cells are available.

Although large crystalline solar cells are commercially available and used extensively in a

wide range of applications there has been much interest in recent years on the potential of thin film solar cells. Thin film technology, such as copper indium gallium selenide (CIGS) and cadmium teluride (CdTe) cells, stand to significantly reduce the cost and weight of solar cells and can act as a lightweight solar cell solution for wireless sensor nodes if the defect density can be reduced [35]. These narrowband gap options are not suitable for hostile environments however and so a silicon carbide photovoltaic energy harvesting is extensively covered in chapter 4 of this thesis. As such, further explanation of the photovoltaic effect in general is saved for then.

2.4.4 Thermal

The most established method for converting thermal energy in to electrical energy is through exploitation of the Seebeck effect. The Seebeck effect states that an electromotive force is generated when the junctions of two different metals are held at different temperatures [36]. A detailed explanation of this effect is presented in [36] and [37], however the fundamental theory is explained here. When two semiconductor materials are placed electrically in series, as shown in figure 2.8, with a temperature gradient across them, there is a generated voltage, and associated current flow, across the external load R_L. This voltage can be determined using equation 2.4.

$$V_L = \alpha_{n,p}(T_H - T_L) - (R_n + R_p)I \tag{2.4}$$

Where $\alpha_{n,p}$ is the summation of the p and n leg Seebeck coefficients, T_H and T_L the temperature of the hot and cold contacts respectively, R the resistance of the p and n type legs and I the current through the junction.

Given that there is a voltage loss due to the internal resistance of the thermoelectric legs it can be observed that a high electrical conductivity is an important design requirement. It can also be seen from equation 2.4 that the temperature difference between the hot and cold electrode is important, from this it is easy to see that materials chosen should have a

very low thermal conductivity to maintain the required temperature gradient. Equation 2.4 highlights that there is a need in thermoelectric materials to exhibit not only a high Seebeck coefficient but also a high conductivity to minimise the ohmic losses in the device.
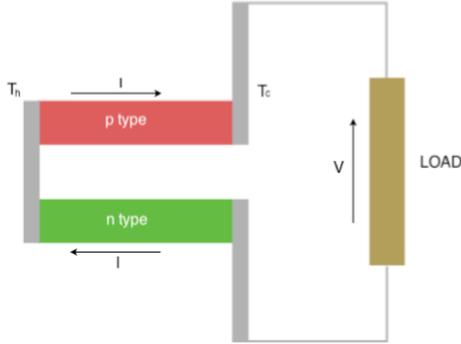
Figure 2.8: Thermal energy harvester principle

The range available in thermal energy harvester is extensive, from relatively simple bulk harvesters such as those provided by Marlow which, with a 60 °C temperature gradient, can produce an optimum output power of 0.92 W at 2.42% efficieny [38], to newer micro scale devices. One such device is manufactured by Micropelt and has the potential to offer higher density energy harvesting due to their increased thermoelectric pair density and reduced device size. Micropelt claim that their processing technique allows for up to 100 thermoelectric leg pairs per mm^2 [39] and can produce higher output power than other thermal methods, around 2.3mW at their peak output. Micropelt technology uses thin film bismuth telluride, Bi$_2$Te$_3$ however its maximum operating temperature, compared to SiGe and PbTe, is limited.

One important factor to consider when comparing materials for use in thermal energy harvesters is the materials figure of merit, ZT, which, as shown in equation 2.5 is dependant on the Seebeck coefficient, α, electrical conductivity, σ, and thermal conductivity, λ, where T is the absolute temperature.

$$ZT = \frac{\alpha^2 \sigma}{\lambda} \tag{2.5}$$

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As the figure of merit increases so to does the device efficiency until it reaches the Carnott efficiency. As can be seen from equation 2.5 this can be maximised with a low thermal conductivity tending toward 0 or with high $\sigma\alpha$ product tending toward infinity.

Bismuth telluride shows high performance around room temperature however its quality figure of merit falls off considerably above 500K [40]. For this reason it is unlikely that bismuth telluride devices will be able to harvest energy from a high temperature hostile environment.
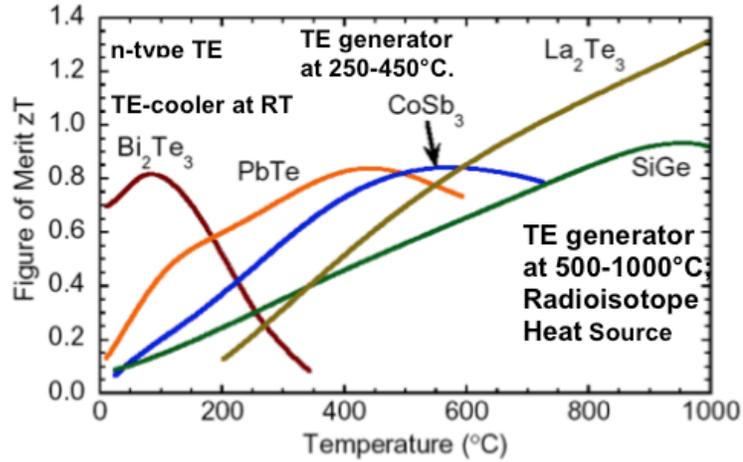
Figure 2.9: Thermoelectric material figure of merit comparisons up to 1000°C

The other two materials mentioned show much more favourable high temperature potential as their figure of merit peak at around 700 K and over 1000 K for PbTe and SiGe respectively [37]. NASA, and other space agencies, have used larger scale thermal energy harvesting to provide long term power to satellites and probes for many years. The NASA Langley Research Centre has details of an investigation in to advanced thermoelectric materials [41] which provides a good comparison between many thermoelectric materials, in particular showing which temperature range each material is most suited. The work also outlines fabrication processes which could produce systems with a figure of merit of over 5, and as such an efficiency of around 30% [41]. Figure 2.9 shows the materials comparison covered in the NASA paper. It shows that a materials figure of merit, the ability to convert a thermal gradient into electrical energy, changes with temperature and highlights the importance of

using a material suitable to the target environment.

Although the materials and methods covered by NASA show potential for high efficiencies and quality factors the mechanically delicate nature of the structures and devices could lower their lifetime in a hostile environment.

2.4.5   Radioisotopic Harvesters

Betavoltaic

The large energy density of radioactive sources makes them attractive for providing the energy for long life batteries [42], converting this stored energy into electrical power is difficult. Of the most novel is a system proposed by Duggirala *et al* [43]. In this work the authors design and build a novel energy harvester which uses a piezoelectric cantilever to generate pulses of electrical energy [43]. The tip of the cantilever is a large silicon area which is exposed to a 2.9 mCi ^{63}Ni β-source. Over time this silicon collector is charged by the emitted β-particles and is attracted toward the source, as shown in figure 2.10. If the initial gap is sufficiently small, then the collector and ^{63}Ni are attracted by electrostatic forces. This results in them making contact and the charge on the collector dissipates, this breaks the electrostatic attraction and the cantilever begins to oscillate at its resonant frequency. This is an impulse response and eventually decays due to the mechanical and electrical damping in the system and so the energy output of each pulse is non uniform. With this system a peak output voltage of 2 V and an overall energy conversion efficiency of 3.97% was demonstrated with an expected life time of several decades limited only by the half life of the radiation source used, in this case 100.3 years. Although this is low compared to other forms of energy harvester [44, 23, 45], it is similar to other devices designed to harvest energy from β radiation decay [46]. This generator has been used to power a ring oscillator light detector demonstrating its effectiveness as an energy harvester [47].

A much simpler approach is that of a betavoltaic converter, this employs the same principles as a photovoltaic device, but electron hole pairs are generated from incident beta particles.
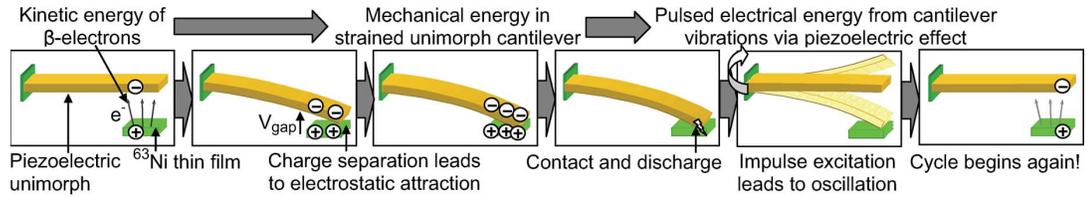
Figure 2.10: Radioisotropic powered piezoelectric generator

The emitted β-particles have more energy than a photon and they also have mass, this mass means that they expend some of their energy kinetically into the lattice and the rest goes to creating electron hole pairs [46]. This is distinct from the photovoltaic effect in which the incident photons are able to make only one electron hole pair and there is no kinetic transfer of energy as photons have no mass.
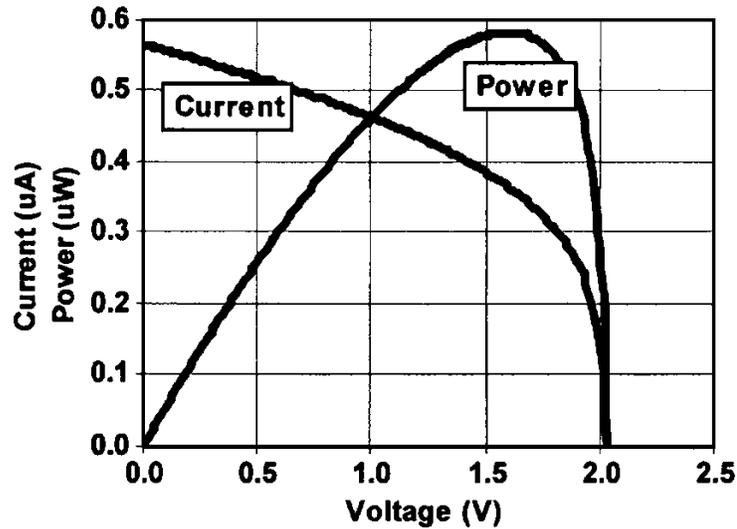
Figure 2.11: Silicon carbide betavoltaic response [46]

Conversion efficiencies for betavoltaics vary considerably in the literature and seem dependant on not only the devices used but the radiation source as well. Eiting et al report efficiencies of 4% from a 4H-SiC pn diode exposed to a 8.5 GBq ^{33}P source. The observed open circuit voltage was 2 V and a short circuit current of 0.55 μA, the data for which is shown in figure 2.11 [46]. The fill factor of their device, a measure of the devices ability to output the energy it generates (covered in more detail in chapter 4), is very low. However,

it is unlikely that the device is suffering from the radiation exposure and given the shape of the illuminated I-V sweep in figure 2.11 it is likely caused by a detrimental shunt resistance [48]. More recent work by Thomas *et al* reports an efficiency of 30% from a SiC betavoltaic exposed to 17 mCi/cm^2 with an open circuit voltage of 2 V and a short circuit current of 1 nA [49]. As with solar cells these devices are still susceptible to temperature changes and the open circuit voltage and short circuit current change accordingly [50].

Alphavoltaic

These are similar in operation to a photovoltaic, but are highly underdeveloped due to radiation damage caused by ^{4}He alpha-particles to standard silicon. Previous experiments show that devices can start with an initial output power of 0.015 μWcm^{-2} with a voltage of 1.613V [51]. After 5 diodes were tested for 100 hours each the output power had fallen to 0.0085 μWcm^{-2}[51]. Using assumptions about the required energy to create an electron hole pair a conversion efficiency of 18% was calculated, a value considerably higher than the efficiency quoted in [46] for a high efficiency betavoltaic cell.

The high output voltage of 1.613V per cell indicates that several cells connected in parallel would increase current output and in turn increase overall power output. However, the 58% [51] power output loss is due the radiation causing deep level traps to develop in the cell. If the effects of these deep level traps could be minimised then an alpha voltaic could be a very useful energy harvesting technique when used in a hostile environment.

2.5 Power Regulation

2.5.1 Rectification

The electrical output from energy harvesters varies and is either AC or DC. The output from a piezoelectric energy harvester, for example, is AC and so requires rectification and smoothing to be of use in the dependant DC circuit. This is added between the storage

capacitor and the energy harvester output.

As the power output from a piezoelectric harvester is generally much less than the average power consumption of a wireless sensor circuit and measured in μW, selecting the correct regulator circuit is important. Typically a four diode full wave rectifier, shown in figure 2.12a, would be used, however this circuit reduces the voltage produced by twice the voltage drop of the diodes. This topology has been used previously to rectify the output from a piezoelectric bimorph for storage on a capacitor [52]. An alternative to this circuit is the voltage doubler, as shown in figure 2.12b, which uses two diodes and a small capacitor to double and rectify the voltage output from the energy harvester. Whilst both circuits are capable of rectifying the output from a piezoelectric energy harvester, the full wave rectifier has a higher current output, while the doubler has a higher voltage output.
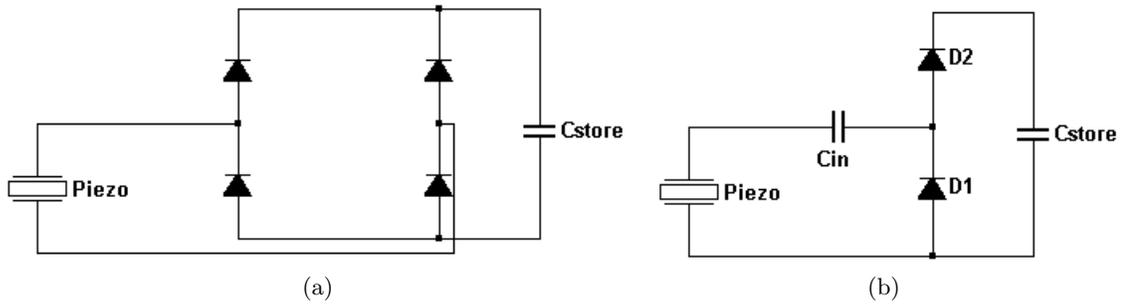
Figure 2.12: Circuit topologies of (a) rectifier and (b) multiplier

The full wave rectifier is well documented [53] but the voltage doubler requires further explanation. With reference to figure 2.12b, D_1 blocks the signal path to ground and so stores the negative half of the signal on the intermediate capacitor C_{in}. When the signal is positive, half a cycle later, the polarity on C_{in} is reversed and the positive signal is summed with the existing voltage on C_{in}. When the addition of these two voltages is greater than $V_{C_{store}}+V_{diode}$, diode D_2 starts conducting and the charge is transferred to C_{store}[54]. It is this stored voltage that will be V_{dd} to the dependent system. Previous modelling by Ferrari *et al.* has shown that the increase in stored voltage for each input cycle is dependant on the ratio of the capacitors C_{store} and C_{in} [32].

A practical investigation into these topologies is undertaken in the following chapter.

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2.5.2 Conversion

The previous section focussed on how to rectify an AC energy harvester output, however many energy harvesters have a DC output. It is unlikely that a solar cell or thermal energy harvester will produce either a stable or useful output voltage, so the challenge is to convert this to another DC voltage which can be used to power a circuit [55]. DC conversion can be used for either stepping up or stepping down voltages. Step up converters require the use of a switching signal typically in the form of a PWM waveform which can add complexity to a system beyond what is capable of operation in a hostile environment. Recently, novel architectures have been demonstrated, such as self oscillating converters [56] which have shown promise for conversion to high temperature operation.

The simplest way to step voltage down is to use a linear regulator, however this is very inefficient. The voltage drop between the input and output is dissipated as heat in a resistor and given the strict energy budget of these systems this is not ideal. Instead, highly efficient buck converters should be used when stepping voltage down, small steps such as this can move conversion efficiencies from less than 50% up to 90% and greater [11].

It is currently possible to construct simple switched converters using SiC components which are suitable for use in a hostile environment. The transistor used can be a SiC JFET which can operate in a stable manner upto 300 °C, the difficulty is in fabricating suitable passive components that can be used in conjuction with the SiC JFET and can withstand the high temperatures, the fast switching frequencies and the noise associated with switched converters. Development of these is crucial to enable a resiient system to operate efficiently.

As discussed by Schemm *et al*, there are benefits to using switched converters, such as dynamic voltage scaling, which can dramatically reduce the energy consumption of systems. In a switched system the output voltage from a transistor, typically a low leakage MOSFET, is smoothed by an inductor or capacitor to provide a new voltage level [57]. Unlike a linear regulator, the lost energy is not dissipated in a resistor and so efficiencies above 90% are not unrealistic [11].

Depending on the type of energy harvester selected different converters will be required, for low voltage sources a step up converter would be the best choice, the stored voltage can be stepped up to match the requirements of the system. This would be particularly useful for solar cells and thermal electric devices with low output voltages. Once rectified and stored the voltages produced by a piezoelectric energy harvester, if the vibration acceleration is great enough, can be larger than 10 V, in this case a step down converter would be useful for reducing this for use in the powered circuit.

2.5.3 Storage

Usually the power requirements of a system are far greater than those available from energy harvester systems. Therefore the energy provided by the harvester is stored before being dissipated into the system electronics. This leads to intermittent operation where the system only performs operations when there is adequate energy to do so. Initially a rechargeable battery appears the most suitable solution, however the energy supplied by an energy harvester is usually measured in the tens of micro watts, this means that the battery would take a very long time to charge. Rechargeable batteries are limited to a few hundered charge cycles before they begin to degrade, and so maintenance is still required on a periodic basis. They also require specific charge profiles to maximise their lifetime which can consume substantial energy to implement.

Table 2.1 compares common primary (non-rechargable) and secondary (rechargeable) batteries and highlights that for that for applciations requiring high temperature operation batteries are not a suitable option. It is clear that the only chemistry which comes close the the target of 300 °C is Lithium Thionyl Chloride and that is still limited to 200 °C, it is also a primary battery and as such would not be useful in an energy harvester powered system as it could not be recharged.

Capacitors provide an alternative to rechargeable batteries, however they have a limited capacity in comparison. They do, however, not need specific charging profiles and can be charged and discharged an infinite number of times due to the materials used in their

Battery type	Self-discharge % per year	Maximum Operating Temperature	Cycle Life
Ni-Cd	15-20	45 °C	300
Ni-MH	20	80 °C	300
Li-ion	5-10	60 °C	500
Lithium Thionyl Chloride	5-10	200 °C	1

Table 2.1: Table comparing common battery types [58, 59]

construction. For these reasons a capacitor is used as the storage medium in the system developed in chapter 3. The size of the capacitor is only 10mF, and whilst it is common to use super capacitors in these types of systems (which can have a capacitance in the range of 1 - 10F) they can take a long time to charge depending on the harvested current [60]. The focus is to make a very efficient and energy intelligent system which can operate on very small amounts of energy, by using a small capacitor the charge time of the system is much reduced and will allow it to operate on a more regular basis.

2.6 System Topologies

With the output current from the energy harvesters typically being less than 100 μA, it is important to maximise the overall system efficiency. For instance, there is little need to have communications circuitry drawing power from the stored energy while the system is sampling a sensor, and in some cases it is worth sacrificing speed of operation for the associated current reduction [61]. Hence, careful consideration of the energy requirements of every operation performed by the sensor system is required.

One method is to design the system around a PIC micro processor that can be placed in a low power sleep mode to allow the stored energy to be replenished. This method relies on the PIC drawing less current in sleep mode than the energy harvester produces, therefore allowing the capacitor to charge, as demonstrated by Torah *et al* [1].

An alternative, comparator approach, presented by Ferrari *et al*, has the benefit of hardware determined voltage thresholds for activating and deactivating the dependant circuitry, and has been shown to provide very stable operation with low "sleep" mode leakage [32]. In the

case of a comparator controlled system the stored voltage is connected to the input of a Schmitt Trigger style comparator which connects the stored voltage to the system electronics when an upper threshold is reaches and disconnects it when the capacitor energy is depleted to a lower level. Although this provides very low leakage in the sleep mode, a trade off to this is a reduced adaptability. As the switching thresholds are set by the hardware they can only be changed by swapping components, as such, a change in the chosen deployment environment would lead to a system redesign for different operating points. One advantage of the PIC approach is that the operating points can be changed dynamically, accounting for environmental changes, component wear and new target deployments, within the embedded software. Hence, circuit elements can be selectively activated and deactivated depending on the desired functionality. Both methods have been successfully implemented and discussed previously [1, 54] so the focus of the work presented in this part of the thesis is on maximising the efficiency during the awake period. Given the complexity of the electronics in a micro controller it is likely that the method most appropriate for resilient systems is the hardware controlled method which could be implemented with simple, discrete components.

One such method could be by using the negative differential resistance effect caused by two bi polar transistors, as shown by Fan in [62]. This piezoelectric powered wireless sensor node is powered by the pressure build up in the cavity an injection mould machine, to realise a simple discharge circuit to control the on and off periods of the system they used the NDR effect found characteristic of the circuit in figure 2.13.

(a) NDR circuit (b) V-I relationship of the NDR circuit
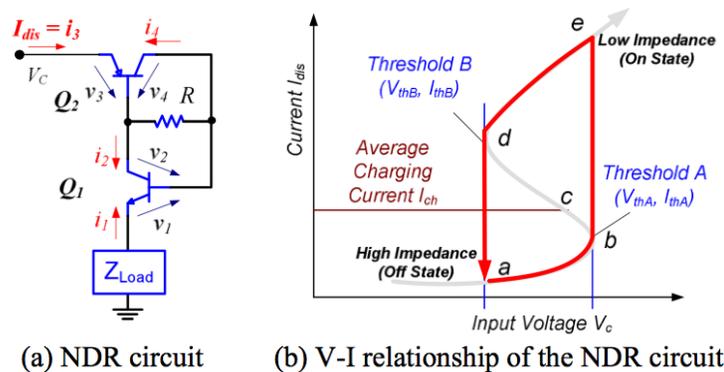
Figure 2.13: System control circuit implemented using BJTs and NDR effect

2.7 Conclusions

The systems discussed so far are designed for relatively benign environments due to either their reliance on silicon electronics or their mechanically delicate construction. The reliance on silicon electronics limits the use of the systems to temperature ranges of -40 °C to 125 °C. Because of this we are unable to monitor some of the most interesting and energy intense processes in the world. Jet engines use huge quantities of fuel and volcanoes are complex systems which we do not fully understand. If we could place simple wireless sensors into the hot areas of these places we could save fuel in the former and save lives in the case of the latter.

The literature review has focussed on the design considerations of energy harvester powered systems and has discussed a wide range of energy harvesting technologies. Taking the research covered into consideration this thesis will focus on the following topics for the experimental sections.

2.7.1 Chapter 2

Given the complexity of energy harvester powered systems it is first thought prudent to develop a room temperature silicon system which can be comprised of commercially available components. The aim of this is to show that a simple, cheap and reliable system can be made with currently available components and to show how simple tweaks can improve a simple system. This system will also help highlight where developments in resilient technologies must occur to realise a resilient energy harvester powered system.

2.7.2 Chapter 3

The literature review and the work in chapter 2 show that for environments with low light levels a piezoelectric vibration harvester is a suitable harvester. This chapter focusses on testing the most popular piezoelectric material, lead zirconate titanate, at elevated tem-

peratures and establishing if this widely used technology is suitable for operation at high temperatures.

2.7.3   Chapter 4

While chapter 3 focusses on testing a well established traditional energy harvester technology at elevated temperatures this chapter instead focussed on taking a well known resilient technology, Silicon Carbide, and testing it as an energy harvester in the form of a photovoltaic harvester. The aim of this is to establish how technologies already suitable for use at elevated temperatures might be developed for this new use.

2.7.4   Chapter 5

One of the key areas of concern highlighted by the work in chapter 2 is the need for a reliable energy storage solution that can temporarily store the energy harvested before periodically dissipating it in to the reliant electronics at a higher current level. Before resilient energy harvester systems can be further developed this is a key area which must be addressed. In this chapter, two capacitor technologies are compared experimentally to establish thier suitability as an energy storeage solution for high temperature environments.

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Chapter 3

Developing a silicon system

3.1 Example System overview

To gain a greater understanding of the requirements and limitations of an energy harvester powered wireless sensor node, a silicon based system comprising commercial off the shelf components was developed. The system is powered by a vibration energy harvester which charges a storage capacitor over a period of time. Once a predetermined voltage level is reached, the system is able to perform a series of tasks culminating in the transmission of several sensor readings to a remote base station. This leads to the system being on and off for varying periods of time, the relationship of which is proportional to the acceleration of the input vibrations. Figure 3.1 shows the schematic for the final system, realised using only commercially available components making it cheap, highly reproducible and, as presented data will show, it operates in a unique and highly energy efficient manner. The system is discussed in more detail and compared to alternatives in the literature throughout this chapter, however a brief overview is given here.

The system uses a piezoelectric energy harvester to convert ambient environmental vibrations into electrical energy, this AC signal is rectified and stored on a 1 mF capacitor. The PIC micro controller is programmed to wake up periodically and decide if there is sufficient stored energy on the capacitor to undertake the required tasks, whilst the PIC is in sleep

mode the current draw is less than the output of the energy harvester and as such the stored energy on the capacitor increases. When there is sufficient stored energy, the PIC wakes up, samples the light sensor reading and then transmits the recording to a remote base station via the 433 MHz AM-RT4-433 transmitter with a current draw of 4 mA. The PIC awake time is maximised by changing the frequency of the onboard clock between high power (500 kHz) and low power (32 kHz) operation. This extends the awake time considerably and above 120 mg acceleration, the system requires no sleep period.
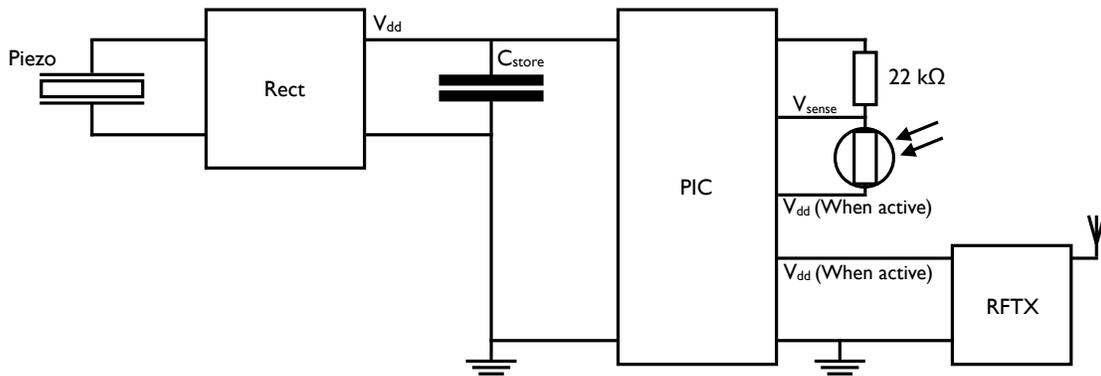
Figure 3.1: Schematic overview of the final system

3.2   Chosen Harvester

A piezoelectric energy harvester was chosen as the power source for an example system because of the ease of implementation and the commercial availability of devices from a number of manufacturers, it is important to reiterate that the chosen device was selected for room temperature system and not a high temperature one. The aim of this wireless node was to use commercially available components to realise an optimised system. Previous systems, such as that published by Colomer-Farrarons [1] and de Villers [2], have shown that a piezoelectric energy harvester is capable of powering a simple wireless sensor node for extended periods of time.

A MIDE V21B Volture energy harvester with a tip mass of 4 g was used as the energy

harvester. The data sheet indicated that this mass would result in a resonant frequency of less than 100 Hz [3], brief experimental validation placed this at 77 Hz. The device is a bi-morph structure with two piezoelectric layers separated by a metallic shim. Both the piezoelectric layers are lead zirconate titanate (PZT), which is one of the most common piezoelectric materials, due to the high piezoelectric constants of d_{31} = -190 x 10^{-12} and d_{33} = 390 x 10^{-12} [3].

Piezoelectric materials rely in the separation of di pole pairs to generate a charge transfer which can be exploited to generation energy. In a freshly formed piece of material these dipoles are randomly ordered and must be aligned, this alignment is called poling and is similar to the principle of aligning the domains in magnetic materials. Once poled the material can be used to make a structure, of which the most common is a bimorph structure, which can come in either a serial or parallel design, as shown by figure 3.2. The device used in this study has two layers which are poled in the same direction and are considered to be in parallel. This means that when one layer experiences tensile strain the other experiences compressive strain and so the metallic shim in the middle acts as an effective ground and the surface electrodes can be combined to produce one signal. If the layers had been poled in opposite directions then they would have been in series and the voltages would have added [4].

Using devices in parallel produces half the voltage for a given strain than the series alternative but generates twice the current. If the target environment for such a system exhibited very low accelerations then the series option would be more suitable as the produced voltage would be more useful. If however, the target environment vibrations are adequate to produce a suitable output voltage then the parallel can be more useful as the increased current output allows the system to harvest energy more rapidly.
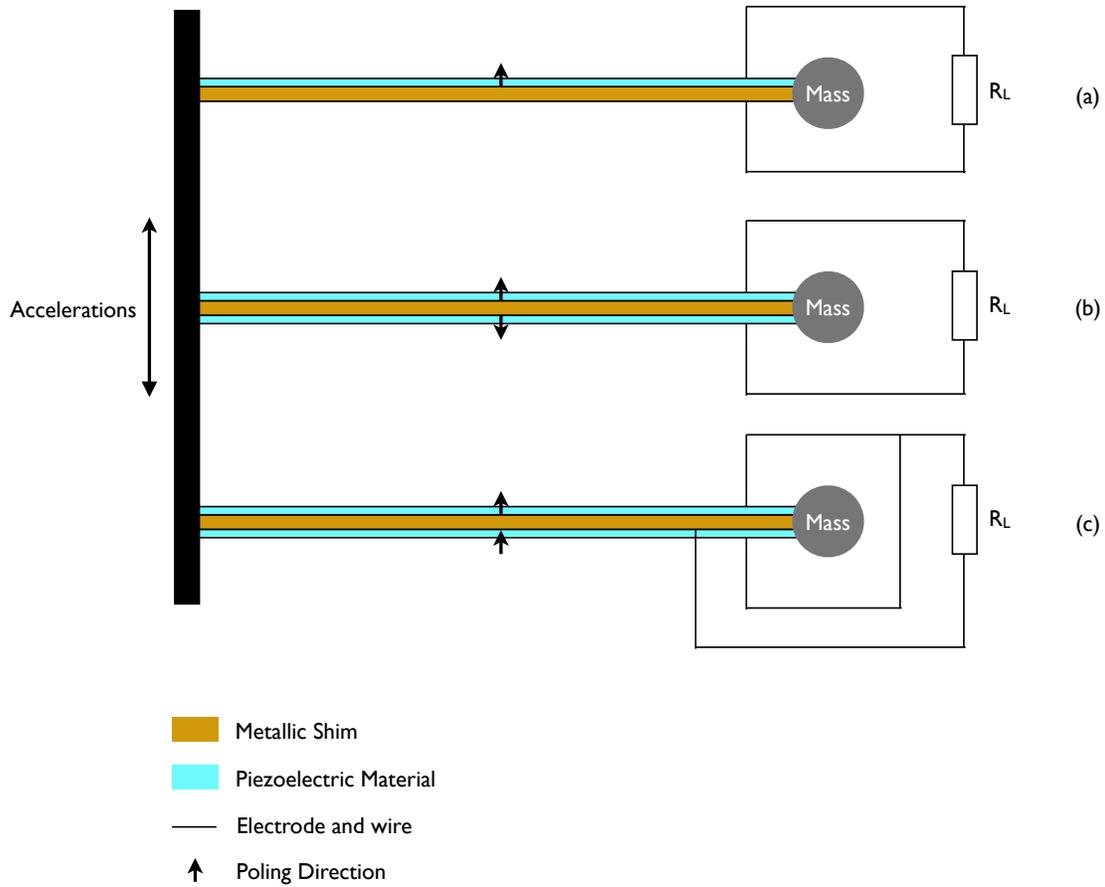
Figure 3.2: Piezoelectric energy harvester cross section showing the differences between how (a) a single layer unimorph is connected compared to, (b) a series connected and (c) a parallel connected bimorph

3.3 Rectification

A voltage double was chosen as the system rectifier and supplies a 1 mF electrolytic storage capacitor. This was chosen for the storage capacitor as it is quick to charge from a low current source, such as the piezoelectric harvester used, and it stores enough energy to full fill the proposed system requirements. The input capacitor was set to 1 μF however, in reality, this capacitor is not necessary as it is in series with the piezoelectric capacitance, C_p, measured with a 200kHz LCR bridge to be 56nF. So the effective capacitance of the input will be similar to that of C_p in accordance with equation 3.1. The capacitor remained

for testing purposes, as when testing the regulator from a function generator, there is no C_p and as such the capacitance provided by C_{in} is required. A 1 μF was selected as for frequencies around line frequency this has been shown to be an adequate value [?]

$$C_{eff} = \frac{1}{\frac{1}{C_{in}} + \frac{1}{C_p}}$$ (3.1)

The voltage doubler was chosen as the system rectifier because of the voltage increase in comparison to the full wave rectifier circuit. For instance, when the acceleration falls to a point where the energy harvester output is less than 1.4V the full wave rectifier will not produce an output, the voltage doubler however could still potentially produce 2.1V, twice the input voltage less one diode drop. This effect could slightly increase the bandwidth of the system allowing it to run at frequencies slightly off resonance, as shown in figure 3.3, where the line at 3.5 V indicates the minimum required output from the piezoelectric harvester to provide a system with 2.1 V.
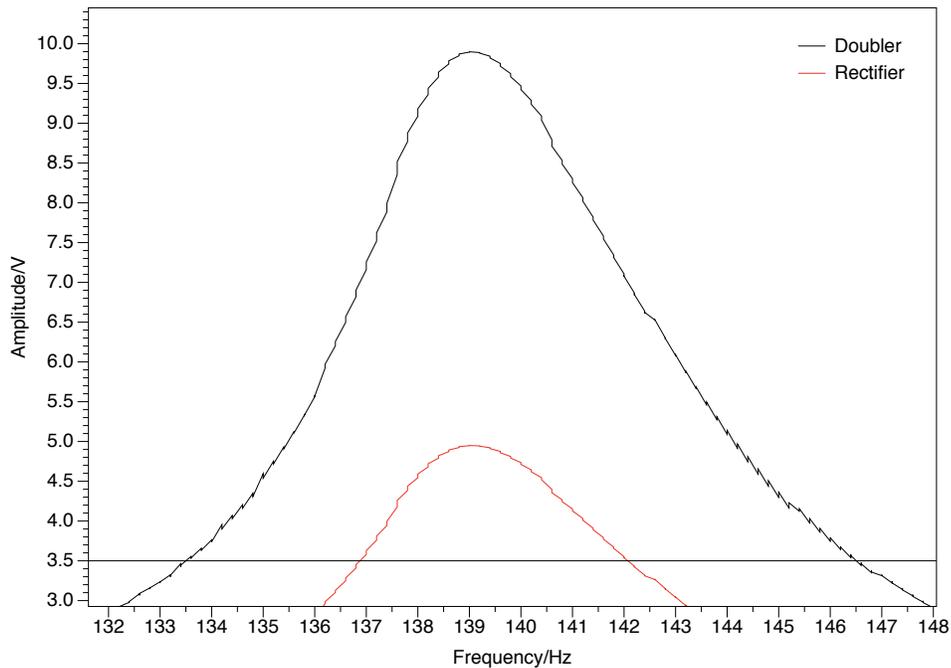
Figure 3.3: Representation of frequency responses highlighting how a voltage doubler can increase the effective bandwidth of the system

Although choosing the correct circuit topology for the system power is important, so is

component selection. With this in mind it was decided to compare the performance of standard silicon pin diodes against silicon carbide Schottky diodes. It has been noted in the literature [5] that the leakage current is as important as having low turn on voltage [6] in order to minimise power loss. Silicon carbide is a wide band gap semiconductor which has a room temperature intrinsic carrier concentration of 8.1×10^{-9} cm^{-3} compared to that of silicon which is 1.45×10^{10}cm^{-3}, which can be calculated using equation 5.7. Hence silicon carbide diodes have a much lower reverse leakage current than silicon devices, however, they also have a larger forward voltage drop [7].

$$n_i = \sqrt{N_C N_V} \left(\exp^{\frac{-E_g}{2k_B T}} \right) \tag{3.2}$$

To test the effect of these diodes on the power rectification, four circuits were built and tested. The circuits comprised both silicon and silicon carbide full wave rectifiers and voltage multipliers. Results from the tests carried out on the diodes and circuits are shown in table 3.1. Figure 3.4 shows a comparison between the I-V characteristics of a silicon carbide Schottky and a silicon diode. It is clear that the silicon device has a lower turn on voltage, but, as the first column in table 3.1 shows, the silicon device has a reverse leakage current 100 times larger than the silicon carbide devices.

Table 3.1: Regulator current and power comparison

	Diode leakage at -5V (nA)	Charge time to 2.5V (s)
Si Rectifier	5	57.9
SiC Rectifier	0.05	65.3
Si Doubler	5	77.9
SiC Doubler	0.05	90.5

Figure 3.5 shows the charge profile of a 1mF capacitor when charged from the rectified output of a Mide piezoelectric energy harvester which is driven with an acceleration of 130mg(1.27ms^{-2}) at resonance. The system was tested with each rectifier circuit and the four charge profiles highlight clear differences between not only the diodes but also the circuits. The full wave rectifier charges the storage capacitor around 1.3 times quicker than either of the multipliers. This is expected because the full wave rectifier doubles the input

43
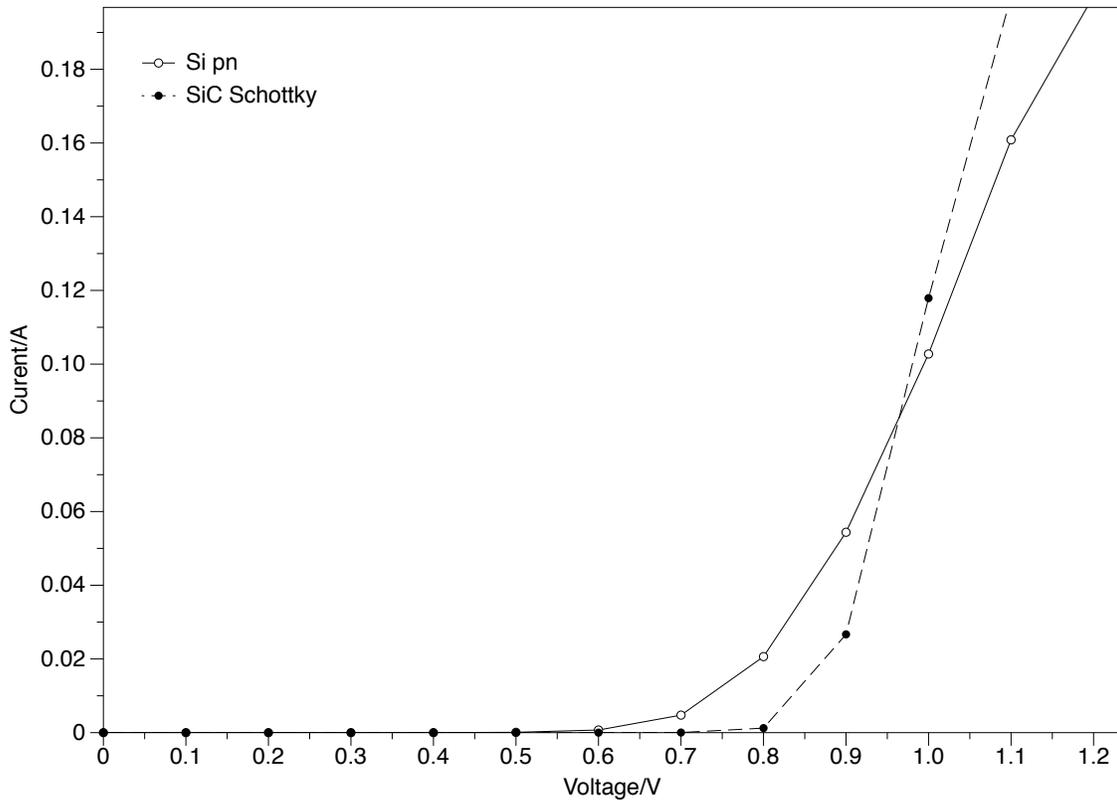
Figure 3.4: Forward IV characteristic comparison between a silicon diode and a silicon carbide Schottky diode

frequency. However the observed charging is not twice as fast, this is likely caused by the difference in diode voltage drop between the topologies. The silicon circuits charge the capacitor faster than the corresponding silicon carbide version, which is likely due to the difference in the diode voltage drops. This voltage drop difference reduces the charging current by 4.4μA for the doubler circuit and 4.8μA for the rectifier. The data in figure 3.5 shows that this has a noticeable effect on the charge rate.

The SiC Schottky diode leakage is 100 times lower than that of the silicon diode. However, the slower charge rate offered by the SiC multiplier shows there is no gain from using the lower leakage SiC diodes in this system. When the system in figure 3.1 is in sleep mode the PIC is still drawing energy from the storage capacitor and as such it is important that the storage element has a net positive input current to stop it being completely depleted, in which case using the silicon diodes is a better option. In a system where the electronics
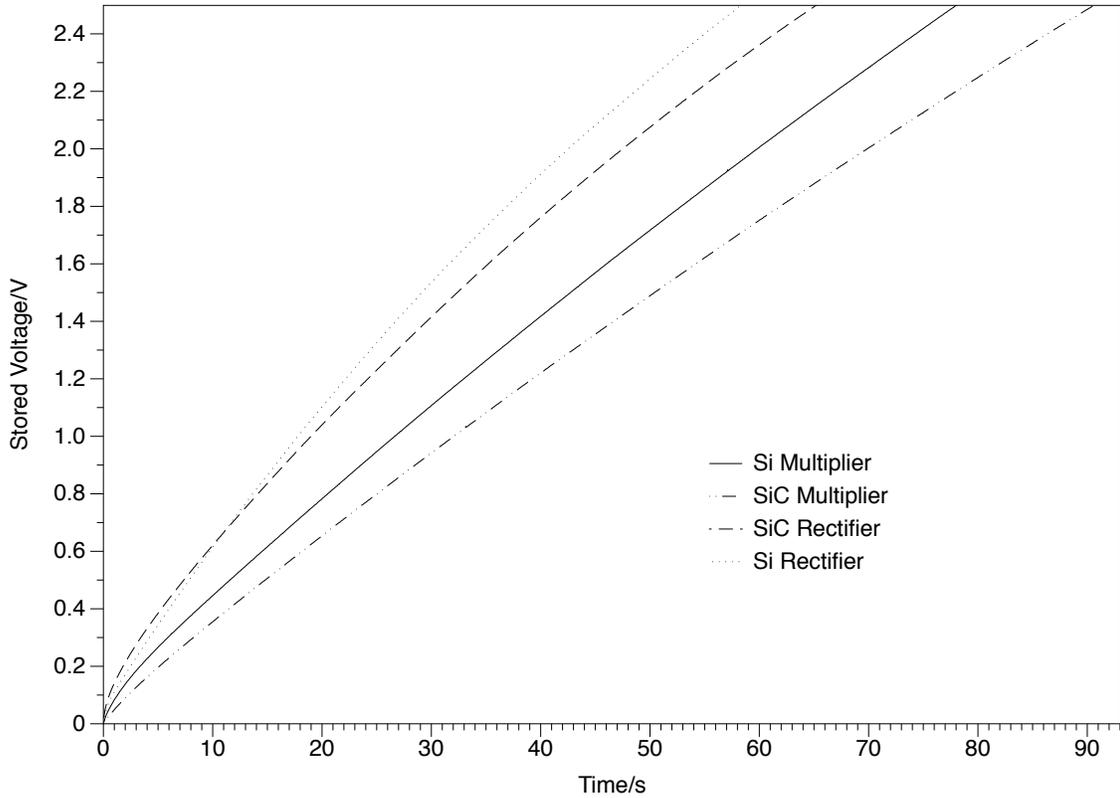
Figure 3.5: Experimentally acquired 1 mF capacitor charge profile at with voltage source provided by piezoelecrtic harvester driven at 130 mg (1.27 ms^{-2}) acceleration comparison for Si and SiC full wave rectifiers and doublers

is isolated from the storage capacitor during the off mode, using diodes with the lowest leakage possible is a more suitable option, as it will minimise the leakage from the storage capacitor back into the energy harvester during times of low energy harvester output.

3.4 Control algorithm

The algorithm shown in figure 3.6 was implemented in the final design using a PIC16F690 for the main system controller as depicted in 3.1. The aim was to minimise the energy burden of the system by using two different clock modes and only activating subsystems when absolutely necessary. There are several internal clock options in the PIC16F690 and each have different current requirements. According to the device data sheet the PIC draws significantly less current than when operating at 31 KHz compared to the full speed 8 MHz.

However, it takes longer to perform operations, resulting in a trade off between the current consumption of a given set of operations and the speed at which they can be executed. The PIC16F690 was chosen as it one of the most widely used PICs, incpororating a serial interface, multiple clock frequencies and a low power sleep mode.
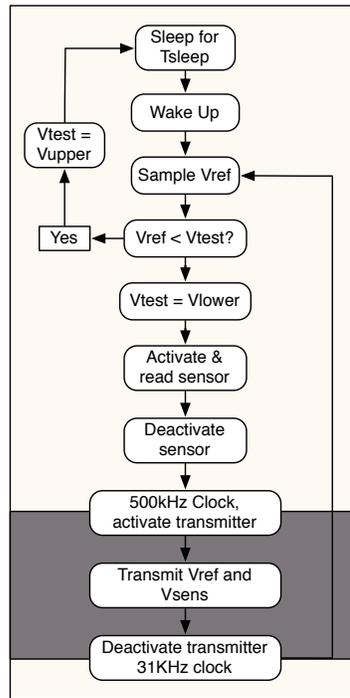
Figure 3.6: Operation algorithm, light area indicates low power 31kHz operation and dark area indicates 500kHz operation

When transmitting data, there is a minimum required clock frequency to obtain an accurate baud rate for wireless transmission of data. The system uses a standard 9600 baud rate for data transmission and on the 16F690, the minimum clock frequency for this to be achieved is 500 kHz. The system needs to switch its internal clock to 500 kHz when transmitting data, faster than this would not speed up the transmission time and would result in a greater number of idle clock cycles as the data is transmitted. The 500 kHz clock frequency increases the current consumption of the PIC above that of the 32 kHz, but it is considerably less than the 8 MHz full speed clock.

To determine if there is sufficient stored energy to perform the required operations, the built in internal voltage reference of the PIC is used to determine the voltage stored on

the capacitor. The stored voltage can not be sampled directly as it is also the system V_{dd} and so will always return the value 1024, independent of the actual V_{dd}. Instead, the PIC's internal voltage reference, V_{ref}, is sampled as a fraction of V_{dd} and used to determine the stored voltage level. According to the specifications, this internal reference is set to 0.6 V. Once activated the reference is sampled with a 10-bit analogue to digital converter and then subtracted from a stored constant. The constants are the upper, V_{upper}, and lower, V_{lower}, operating limits. Prior to subtraction, the two least significant bits are removed from the word, leading to a resolution of 8 bits, so that the PIC can process the data more rapidly and more efficiently.

When V_{dd} is small then the ratio of $\frac{V_{ref}}{V_{dd}}$ will be large. As V_{dd} changes, $V_{refsample}$ will change inversely in accordance with equation 3.3.

$$V_{refsample} = \frac{0.6}{V_{dd}} * 256 \qquad (3.3)$$

Depending on if the PIC is in the awake mode or sleep mode will determine if this sampled value is subtracted from V_{upper} or V_{lower}. If the system is in sleep mode then the PIC will wake up, sample V_{ref} and subtract it from V_{upper}. If the result is negative then the turn on threshold has not been reached as V_{dd} is too low and the PIC will return to sleep. Once the result is positive the system will wake up and perform the required operations.

When the system is in the awake mode, along with data collection and transmission, it will sample V_{ref} once per cycle and subtract it from V_{lower}. When this subtraction returns a negative result the system will go back to sleep because V_{dd} has fallen to a point where V_{ref} is once again a large fraction of V_{dd}. Equation 3.3 has been used to set the values of V_{upper} to 63 and V_{lower} to 75, these equate to 2.43V and 2.04V respectively. For system efficiency and processing speed this system is not programmed to process floating points, and so some accuracy is lost in this conversion process. This is primarily a problem at higher operating voltages where accuracy is of less concern. At around $V_{dd} = 10$ V a one bit change in the the sampled value of V_{ref} equates to 0.5 V of V_{dd}, this is an unlikely operating voltage but not

unrealistic for higher power sensors. Between the operating points of this system, however, the resolution is 25 values per volt, this is sufficient to change the threshold constants to suit a range of environments.

3.5 Operating Characteristics

Energy harvester powered systems have unique operating characteristics caused by their non-deterministic operation. Monitoring the voltage level on the storage capacitor typically shows that there is a large sleep period where the stored energy is allowed to build up followed by a very short discharge of the energy when the system is operating [6, 8, 9, 1].

(a)   (b)   (c)
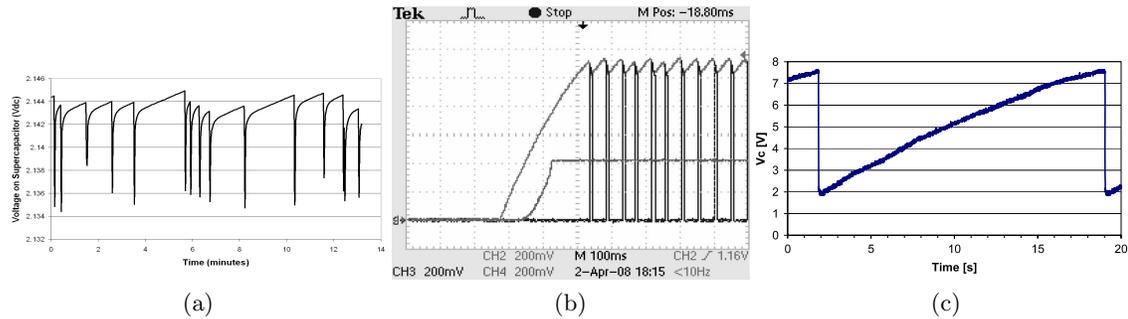
Figure 3.7: Comparison of discharge and change characteristics of vibration energy harvester powered wireless sensor nodes. (a) Torah *et al*, (b) Colomer *et al* and (c) Ferrari *et al*

The time period for the discharge is usually fixed and allows the system to perform a certain number of operations before it returns to sleep. The time the system takes to charge whilst asleep is dependant on the amount of energy produced by the energy harvester. For a vibration based system the output energy is proportional to the acceleration of the input vibrations squared. In the case of a solar cell the current is proportional to the intensity of light incident on the cell. This leads to a simple, predictable relationship between the duration of the sleep periods and the input energy. Examples of this are shown in figures 3.7a - 3.5, it is clear that the time to consume the stored energy is significantly less than the charge time. In figure 3.7a the sharp drops are the time during which the system is

awake and transmitting data, it is clear that the time taken to charge is not consistent and is orders of magnitude lager than the wake time. Similar drops during the awak period are depicted by the data in figures and with the maind differnece being that the sleep and awake time are more comparable in with a period of around 60 ms which is much shorter than the others which are measured in tens of seconds and minutes.

3.5.1 Decay Characteristics

The system was initially operated with an 8 MHz clock and an input acceleration of 100 mg (0.981 ms^{-2}) and the variation in C$_{store}$ monitored with respect to time. The stored voltage on the capacitor C$_{store}$ in figure 3.1 was sampled every 50 ms by an NI DAQ 6033 data acquisition card buffered with a Keithley 6517A electrometer with an input impedance of 200 TΩ. At this operating frequency the system had an awake time of 0.9 s and drew an average current of 0.46 mA. This can be significantly improved using the algorithm shown in figure 3.6. The data in figure 3.8 shows the comparison of these two operating modes and it is clear that using a dual clock frequency uses less energy and allows the system to stay awake for a much longer period of time. The average current draw is now 9.3 μA and the average power reduced to 21 μW.

By using two clock frequencies the system awake time is now 49 times longer than with a constant 8 MHz. Given that the total charge time is 20.84 s, the duty ratio of this system, taken here to be $\frac{t_{on}}{t_{off}}$, has been improved from 0.04 to 3.15.

This large increase in duty cycle is a result of the low current draw of the lower frequency clock operations and selectively activating components. The data in the inset of figure 3.8 shows the stored voltage for a single sleep/awake cycle for the system when the dual clock system is employed. In the awake period it can be seen that the stored voltage periodically increases before a rapid decrease. The increase in stored voltage is a result of the low frequency clock drawing less current than the energy harvester is producing, and so leading to a net positive energy flow into the capacitor. This leads to the creation of two distinct operating modes in the awake period, the low power sample mode and higher power transmit
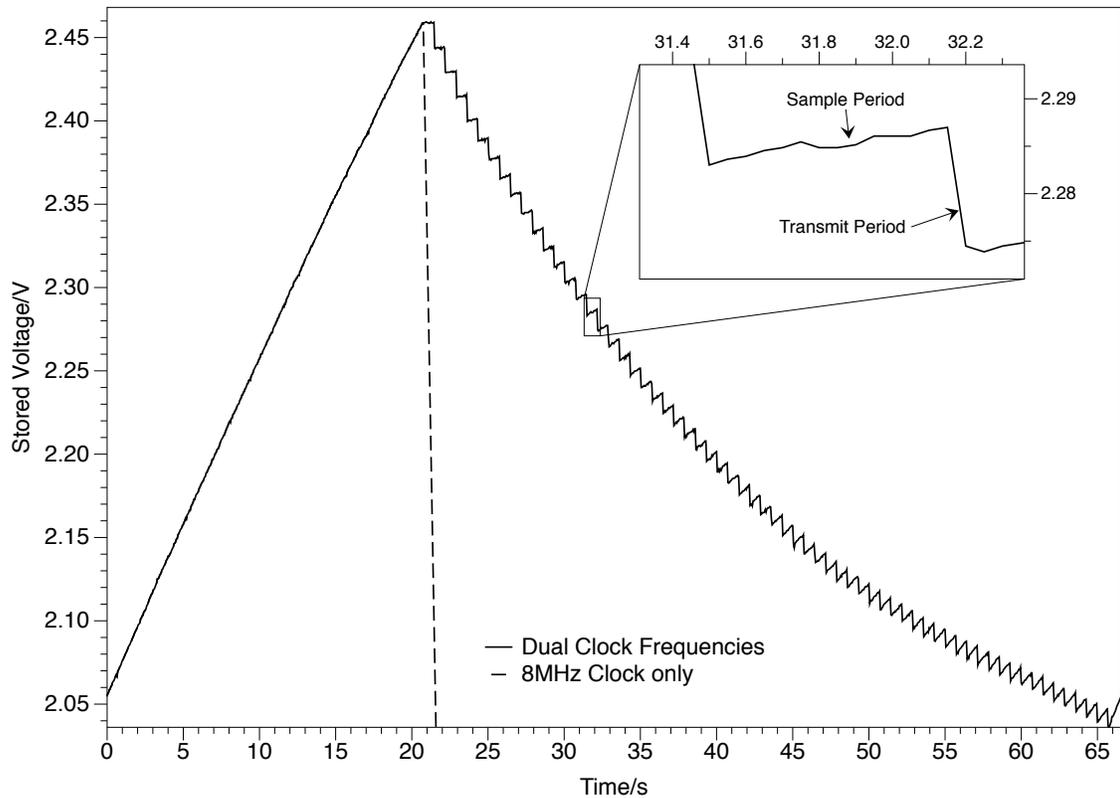
Figure 3.8: Charge/discharge waveform for the stored voltage with dual clock operation at 100mg acceleration

mode.

The data in figure 3.8 shows that the decay in V_{dd} is not linear. To investigage why the change in stored voltage during a sample/transmit pair was normalised to the initial voltage at the start of the sample period. The data shown in figure 3.9 is evaluated from every fifth sample/transmit pair in figure 3.8. The data shows that as V_{dd} decreases during the awake period the amount that V_{dd} increases during the sample period increases. This is caused by the PIC current consumption decreasing proportional to V_{dd} and as such the gross current flowing out of the capacitor is reducing. As the energy harvester is not isolated from the the system electronics during this time there is still some current flow into the capacitor from the piezoeletctric energy harvester. The data in figure 3.9 indicates that eventually the net V_{dd} change during a sample/transmit pair will be 0 V and the system will never need to return to sleep as the energy harvested during the low power sample mode will equal the

energy used in the higher power transmit mode.

In this case, however, V_{dd} still falls below V_{lower} and as such goes back to sleep. To determine the acceleration level at which the system does not require a sleep mode the acceleration used to drive the energy harvester was varied and the system characteristic monitored.
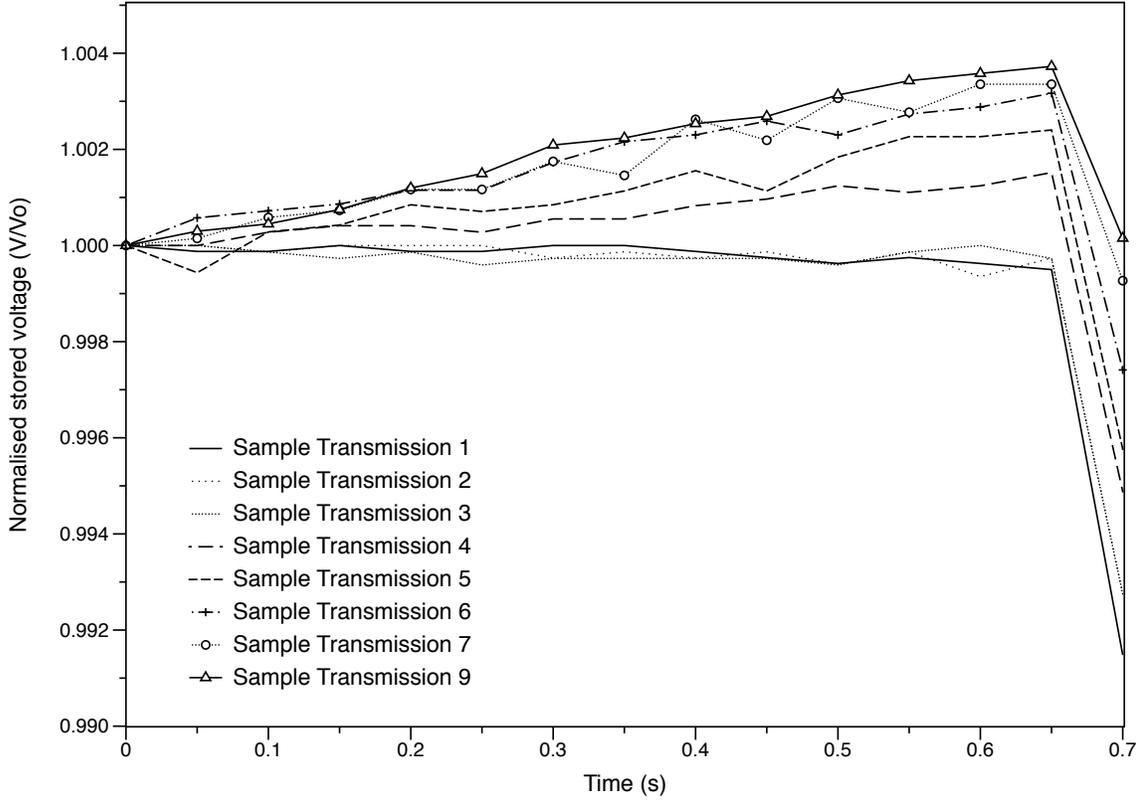
Figure 3.9: Normalised store voltage for sample/transmit cycles

The data in figure 3.10 shows the charge and discharge profile for the storage capacitor at four different accelerations. At 50mg the charge time is longer than the discharge time (duty ratio less than 1), at 100mg the discharge time is longer than the charge time (duty ratio greater than 1), and at 150mg the system operates continuously (duty ratio = ∞).

This data shows that as the acceleration increases, the sleep time decreases and the awake time increases to the point where a sleep period is no longer required. Above 120 mg the energy harvested during the 31 kHz sample period is enough to replenish that used in the transmit mode. This causes the system to settle to an average operating voltage which is
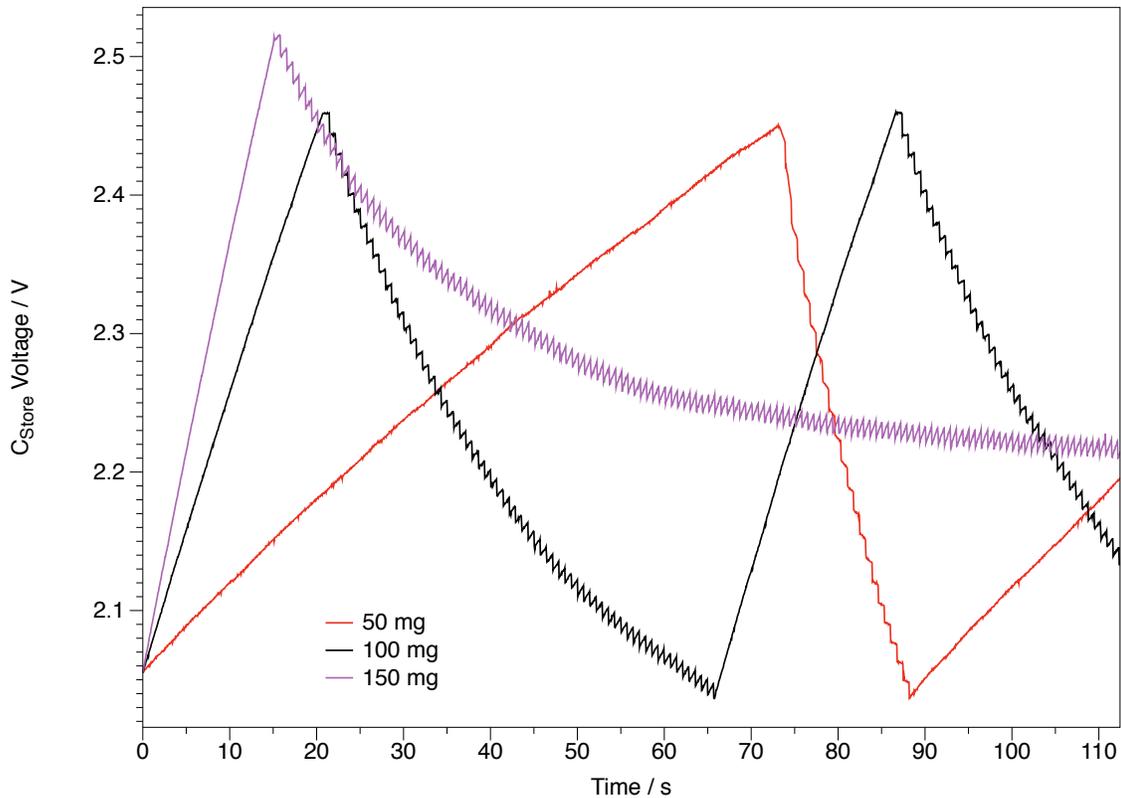
Figure 3.10: Stored voltage characteristic for multiple accelerations

proportional to the driving acceleration. An interesting consequence to this however is that at very high input accelerations the voltage is likely to settle higher than the maximum operating voltage of the PIC. In this case an improvement to the system would be to use a low leakage protective circuit to stop the capacitor charging to that voltage.

The data in figures 3.11a and 3.11b show how the input acceleration affects the stored voltage charge and discharge rate. It is clear from the data in figure 3.11a that an increase in input vibration acceleration increases the rate of charge. However, unique to this system, the input acceleration also has a marked effect on the discharge characteristic, as shown in figure 3.11b. The fit to the data shows that at around 120 mg the total energy in the system will stabilise and there will be no net discharge from the storage capacitor. This is supported by the measured discharge rate at accelerations between 120 mg and 160 mg. At higher accelerations the system does not require a prolonged sleep period and so the voltage stabilises at a balanced operating point, this is also proportional to the input acceleration
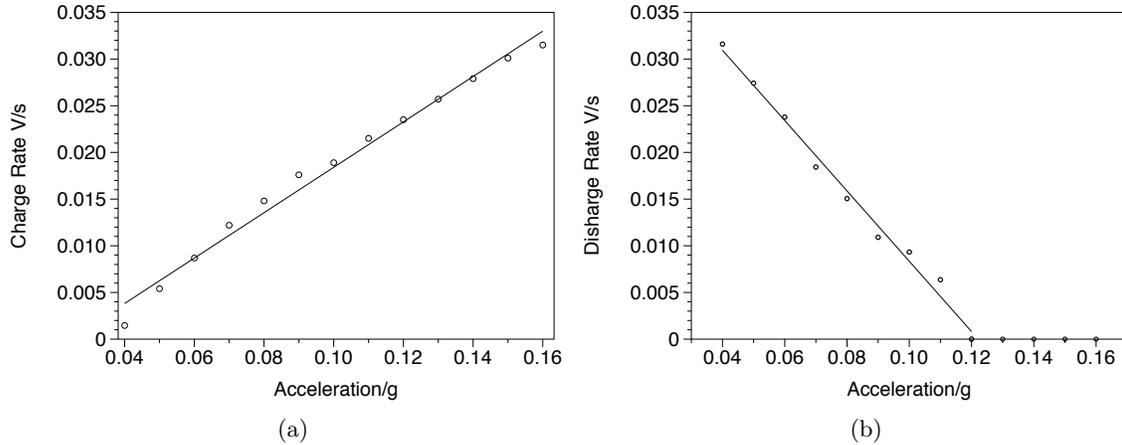
Figure 3.11: a) Charge rate vs acceleration b) discharge rate vs acceleration

as shown by figure 3.12.

Using the dual clock method, there is a measurable gap between packet transmissions, related to the time the system takes to carry out its operations in the 31 kHz clock mode. In this mode the gap between readings is 0.65s and shows no dependence on V_{dd}. This limits the use of this particular system to applications where the measured environmental variable is relatively stable. Changes occurring at a rate comparable or faster than the system sample rate will not be accurately monitored. However, in such situations the sample mode clock frequency can be increased to reduce the sample time and increase the samples per second of the system. This will reduce the overall awake time due to a higher operating current, but the system will be able to feedback measurements more rapidly.

3.5.2 Stability test results

Figure 3.13 shows the results for a 1.1 hour test. In this test four different accelerations were used to drive the energy harvester to determine the system stability. It is clear that the charge and discharge times are dependent on the input acceleration and from this extended test it can be seen that the system operates in a stable manner between V_{upper} and V_{lower}. There appears to be some instability in the upper voltage threshold, however this is caused by the 4 seconds sample delay when in sleep mode. If the PIC were to sample V_{ref} just
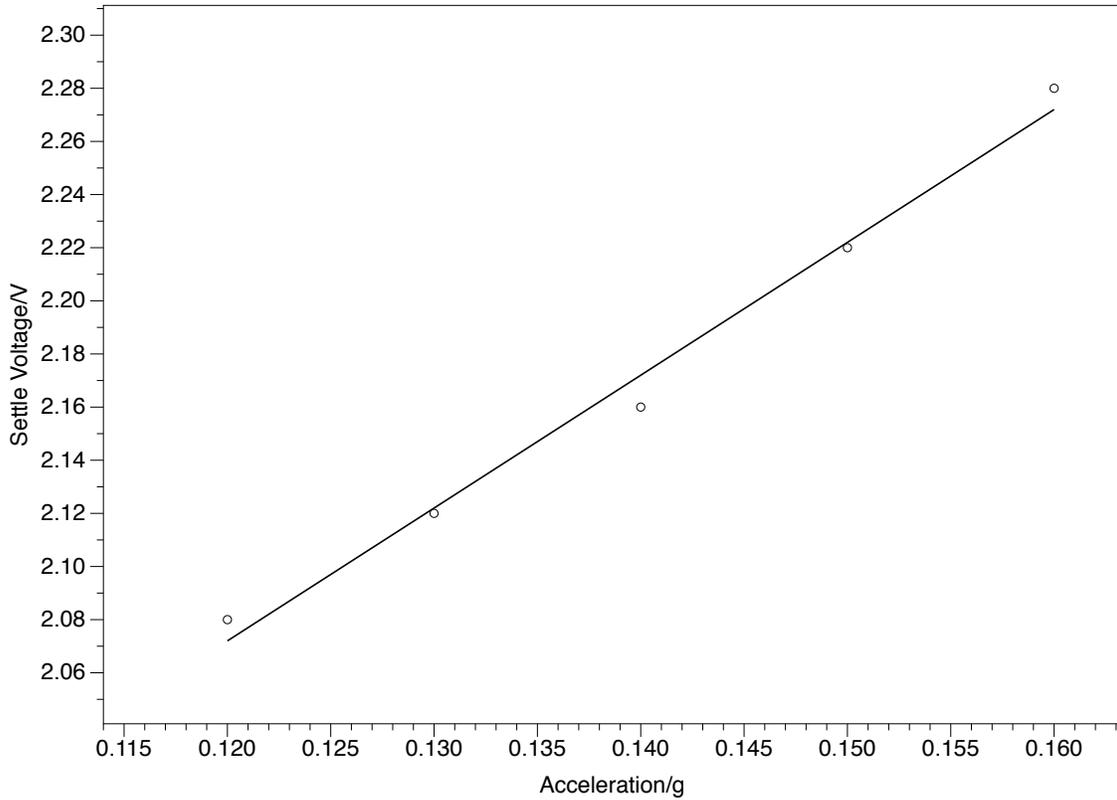
Figure 3.12: Settle voltage during continuous operation

before it crosses V_{upper} then there would be a 4 second delay before the PIC would begin an awake period. During this 4 seconds the stored voltage increases beyond the threshold, this continues until the PIC samples the stored voltage again. There appears to be little difference between 100mg and 80mg because the variation in charge and discharge times for these two accelerations leads to a change of only 3 seconds, in the system time period another unique attribute of this system. The final acceleration tested is 150mg, it is clear that the system begins to operate continuously at this acceleration.

3.5.3 Received data analysis

The receiver software is a command line application that displays the most current reading to a terminal output. If a complete set of data matching the predetermined pattern is received then the value is displayed and saved, otherwise it is discarded. Figure 3.14 shows
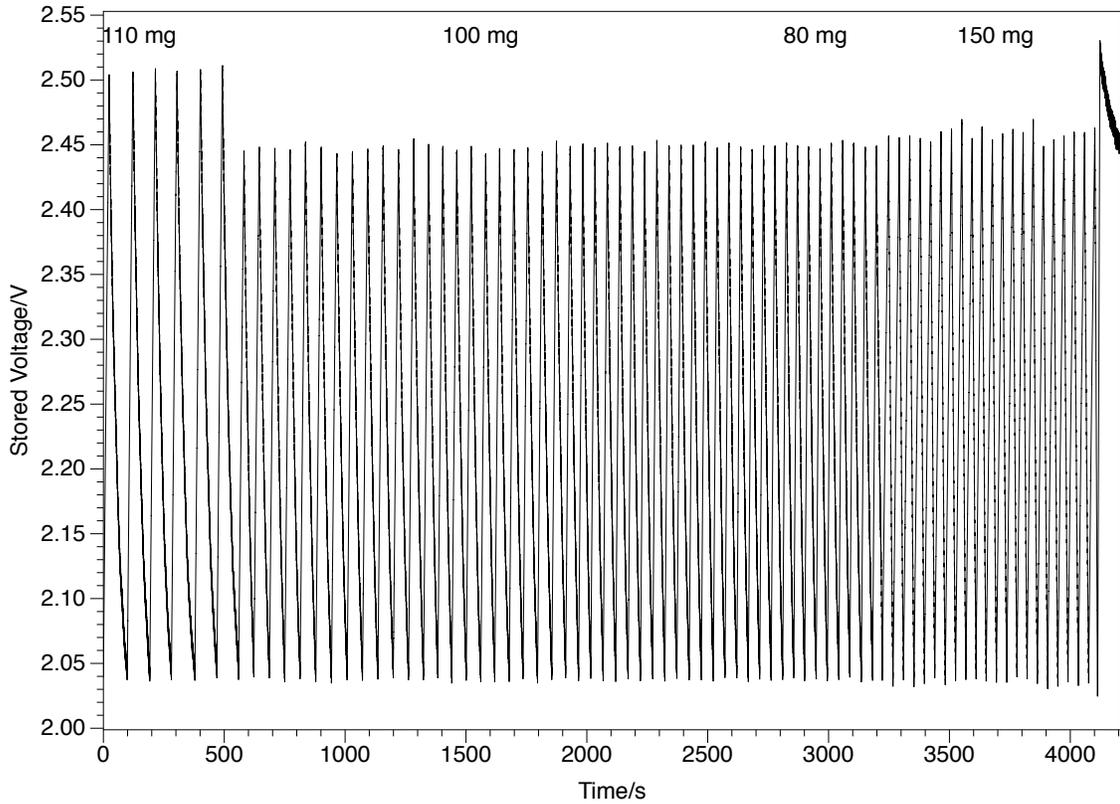
Figure 3.13: Stored voltage change during extended operation

the received data for two discrete test states, in the first period the light dependant resistor is covered and in the second it is illuminated by a halogen desk lamp. The received data shows that the direct voltage reading of the sensor decreases during the sawake period because V_{dd} is also decreasing. However, by compensating for this decrease in V_{dd}, the light level reading, as an intensity, remains constant.

This compensation is acheived by transmitting the sampled internal reference voltage value along with the sensor sample. Therefore, calculating the voltage of V_{dd} from the sample value of V_{ref} and then the voltage of the light sensor, V_{light}, it is possible to obtain a light intensity value from 0 to 1 from the result of $\frac{V_{dd}}{V_{light}}$.

The received data is shown as a function of its received number, rather than time, to clearly show that the data is converted and stabilised.
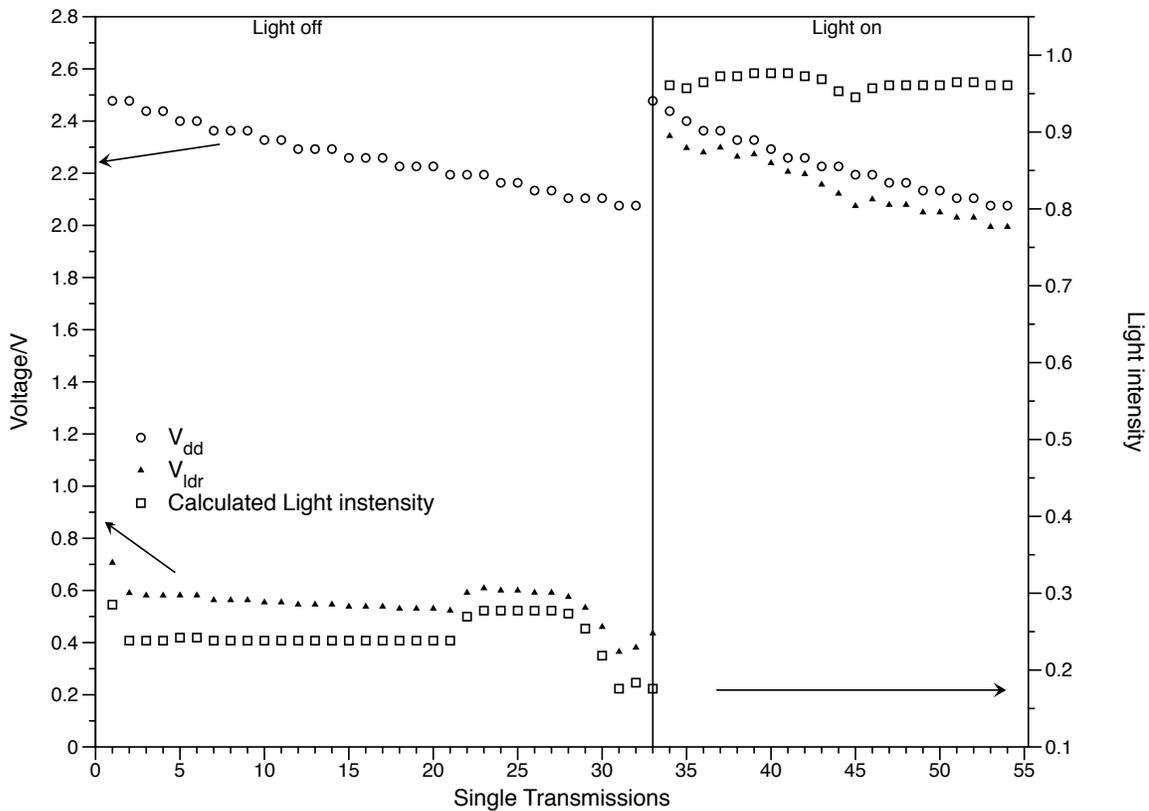
Figure 3.14: Received data from the mote

3.6   Conclusions

The development of this system clearly shows the complexity of designing an energy harvester system. The system developed is capable of intermittent operation at acceleration levels of 40 mg and continuous operation at 120 mg using cheap, simple, off the shelf components. It also highlights that piezoelectric energy harvesters are simple to use as an energy harvester and due to their simplicity are a good candidate to investigate for use at high temperatures.

The importance of selecting the appropriate rectifier and components is clearly highlight by the variation of the storage capacitor charge profiles. For room temperature electronics it is obvious that standard silicon devices is the more suitable approach, however for use at elevated tempera rues silicon carbide devices that are comparable in performance to silicon

diodes would be preferable.

The algorithm implemented to maximise the system efficiency is simple to implement on a microprocessor, however translating this to silicon carbide electronics is currently beyond the state of the art. To replace this, hardware based comparator system would need to be implemented, this is beyond the scope of this work.

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Chapter 4

Piezoelectric Energy Harvesting

Chapter 2 identified that a piezoelectric energy harvester could potentially be deployed in a hostile environment and used as resilient energy harvester to power an electrical system. This is due to its simple mechanical structure, ease of fabrication and simple energy conversion principle. To this end this chapter will focus on characterising a piezoelectric energy harvester at elevated temperatures and identify how the device operation changes with increasing temperature. The characterisation is focussed on determining how the transient temperature variations effect the device and not how long term exposure may affect the materials. An energy harvester composed of lead zirconate titanate, PZT, the most commonly used piezoelectric material, is characterised to 300 °C to determine the limiting factors in using this material in extreme environments.

4.1 Theory

Piezoelectric energy harvesting is a field incorporating aspects of many disciplines, including electrical and mechanical engineering and materials science. Designing piezoelectric systems requires an understanding of the relevant topics in each discipline. With this in mind, the following sections discuss the piezoelectric effect at atomic and bulk material levels and cover both the mechanical and electrical properties.

4.1.1 Background and History

Piezoelectric materials produce a voltage when they experience a strain, and so they have been used extensively in sensing and, more recently, energy harvesting applications [1]. As the power requirements of digital electronics have decreased significantly in recent years this unique family of materials has significantly contributed to energy harvesting technology.

In the late 1800s Pierre and Jacques Curie discovered that, among others, quartz exhibited piezoelectric properties [2], and although its piezoelectric properties are weak compared to more modern materials, it was enough to form the initial research on this unique area. Curie found that when a tensile or compressive strain is applied to a piezoelectric material a proportional voltage is generated, both producing an equal voltage per unit stress but with opposite polarity. They discovered that the inverse was also true, that by applying an electric field, the material would expand or contract by an amount proportional to the applied field, this is now used to great effect in electric buzzers and MEMs transducers [3]. Since the initial discovery many materials have been found to exhibit a piezoelectric response such as AlN, ZnO, BaTi and PZT [4, 5, 6].

4.2 Piezoelectric Material

Piezoelectric characteristics are exhibited by a wide range of materials including single crystals and man made ceramics. PZT is the most common modern piezoelectric ceramic, it is a ferroelectric material with d_{33} and d_{31} piezoelectric coefficients in the ranges of 390×10^{-12} C/N and -190×10^{-12} C/N respectively for bulk materials [7, 6]. Not all piezoelectric materials have the same structure or properties as PZT however. Single crystal materials such as Aluminium Nitride, exhibit a piezoelectric response but is fabricated in a different way [8, 9].

4.2.1 Lead Zirconate Titanate (PZT)

Figure 4.1 shows the structure of a unit cell PZT crystal, it shows that the Lead and Oxygen atoms surround a single Zirconium atom. It shows that when an electric field is applied to the structure the top and bottom bonds do not remain equal in length and so the Zirconium atom moves inside the surrounding structure. This causes a localised charge displacement which, when combined with other unit cells behaving in the same way, will produce an overall charge displacement across the material.
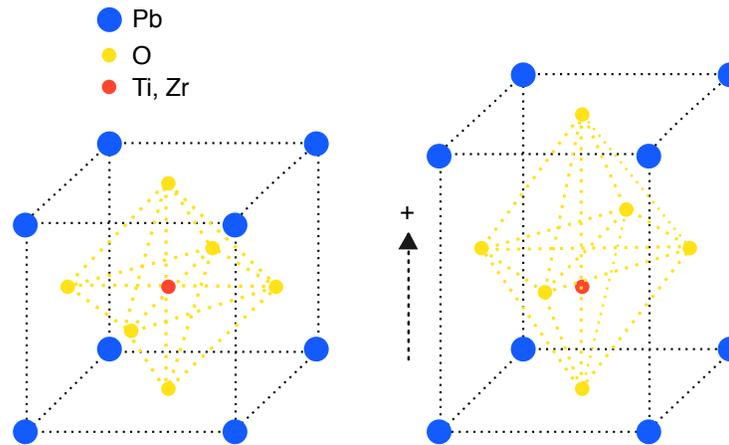
Figure 4.1: PZT atomic structure

The manner in which PZT devices are fabricated means that some areas will respond differently to others when the newly fabricated material is stressed. This non-uniform behaviour can lead to a freshly fabricated PZT layer exhibiting no net piezoelectric response. By applying a large electric field under certain conditions (often at elevated temperatures for an extended period of time) it is possible to pole the device to produce a net piezoelectric response [10, 11]. This is possible as PZT is both ferroelectric and piezoelectric, meaning that it exhibits a spontaneous polaristion of which the direction can be altered with an external field. Not all piezoelectrics however are ferroelectrics. For instance, in the case of AlN, which is piezoelectric, the direction of polarisation can not be altered and as such is not a ferroelectric. Figure 4.2 shows that applying an electric field aligns the randomly ordered ceramic along the axis parallel to the polarisation, when the field is removed the

structure relaxes but remains orientated in the desired direction. When the structure is now stressed the piezoelectric response will be detectable, as all the dipoles respond in the same manner.
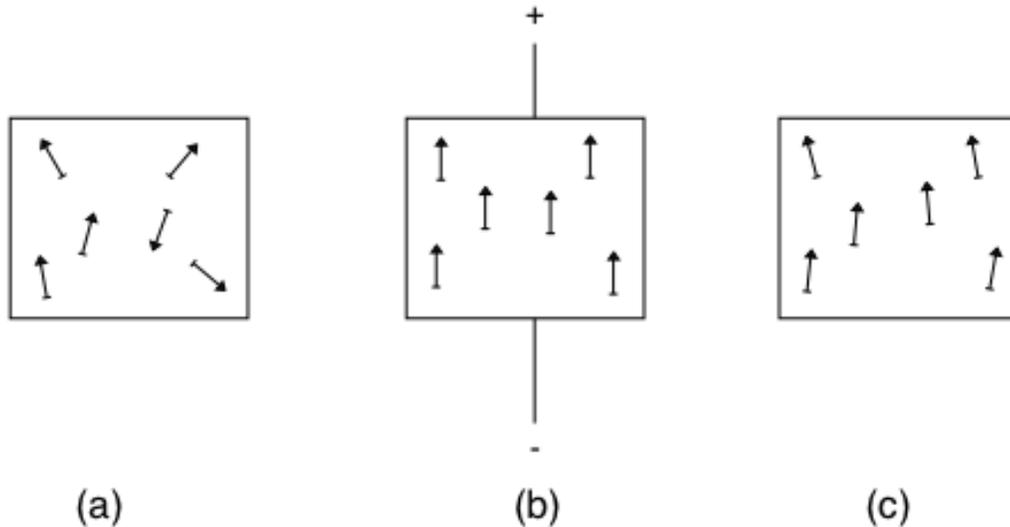
Figure 4.2: Electric dipoles in PZT in (a) as grown material, (b) during poling and (c) latent polarisation once polarising field is removed

Materials such as PZT rely on the latent polarisation that remains once the polarising field is removed. This polarisation can be reversed or weakened by impact, shock and elevated temperatures. The temperature at which the polarisation is no longer effective is called the Curie temperature and is the point at which the dipoles revert back to a random, unordered state where there is no net piezoelectric response [6]. This is problematic when designing and developing energy harvesters for systems deployed in hostile environments as materials need to be resilient to the environment in which they are in.

There are two primary types of PZT which are commonly found in energy harvesting applications, table 4.1 compares the 5A and 5H PZT material to two other common piezoelectric materials, barium titanate, $BaTiO_3$, and Polyvinylidene fluoride, PVDF.

It is clear from this comparison that the most suitable candidate for operation at elevated temperatures is PZT-5A due to the Curie temperature of 350 °C. The compromise made is that the piezoelectric coefficients d_{33} and d_{31} are less than half that of PZT-5H. Although

Property	PZT-5H	PZT-5A	BaTiO$_3$	PVDF
d$_{33}$(10^{-12} C/N)	593	374	149	-33
d$_{31}$(10^{-12} C/N)	-274	-171	78	23
k$_3$3	0.75	0.71	0.48	0.15
k$_3$1	0.39	0.31	0.21	0.12
Curie Temperature (C)	195	365	120	110

Table 4.1: Comparison of popular piezoelectric materials [6]

this high temperature Curie point is suitable for the target temperature of this study, 300 °C, is is further complicated as the application of stress reduces the Curie temperature. This makes high stress and high temperature operation of piezoelectric materials problematic and is one of the reasons why a detailed study of piezoelectric energy harvester operation at elevated temperatures is important and conducted in this chapter.

4.3   Utilisation

4.3.1   Piezoelectric modes

The relationship between the magnitude of the produced voltage and the induced stress is governed by the piezoelectric strain coefficient of the material, which is different for each of the devices operating modes. The two modes most suitable for energy harvesting are the 33 and 31 modes, for which the piezoelectric coefficients are d_{33} and d_{31} respectively [12]. As shown in figure 4.3, the 33 mode is when the stress and voltage act in the same direction, and the 31 mode is when the stress and voltage act perpendicular to each other, this does however assume that the electrodes are connected to the cantilever as depicted in figure 4.4. The d_{33} coefficient is usually considerably higher than d_{31} [13] and so for sensing applications would be favoured because of its larger response to smaller strains. The 33 mode is difficult to implement successfully for energy harvesters contacted in this manner however as the stress and voltage act in the same direction, and although the d_{31} coefficient is lower than the d_{33} it is easier to generate a large amount of strain in the material [13, 14]. It is possible to exploit the d$_{33}$ coefficient using interdigited contacts however and this has

been successfully accomplished and has generated almost twice the maximum open circuit voltage [15].
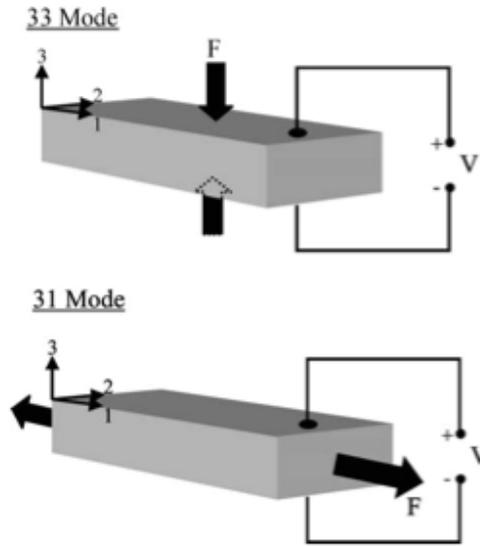
Figure 4.3: Modes of piezoelectric operation [12]

To best utilise piezoelectric energy harvesters, it is desirable to generate the maximum amount of strain for the least input energy, it also needs to be easy to deploy and simple to manufacture. The simplest way to achieve this is to fabricate a piezoelectric cantilever where one end is clamped to a vibrating source and the other is free to oscillate, as shown in figure 4.4.

Once made into this structure the device is used in the 31 mode, where strain is generated across the length of the device and voltage is produced through the y-axis. To use the voltage produced the device is contacted top and bottom across the entire face of the active piezoelectric area with metal electrodes, in this case "active" means that it experiences strain and therefore produces a voltage. An example of an inactive area is that under the clamp which experiences considerably less strain than the rest of the beam however maximum strain is generated at the first part of the cantilever which is not clamped, marked X in figure 4.4. Piezoelectric materials are not conductive and charge will only be collected from areas which are covered by metallic contacts. Their insulating nature means that these devices are also a parallel plate capacitor, so any inactive areas covered by electrodes add
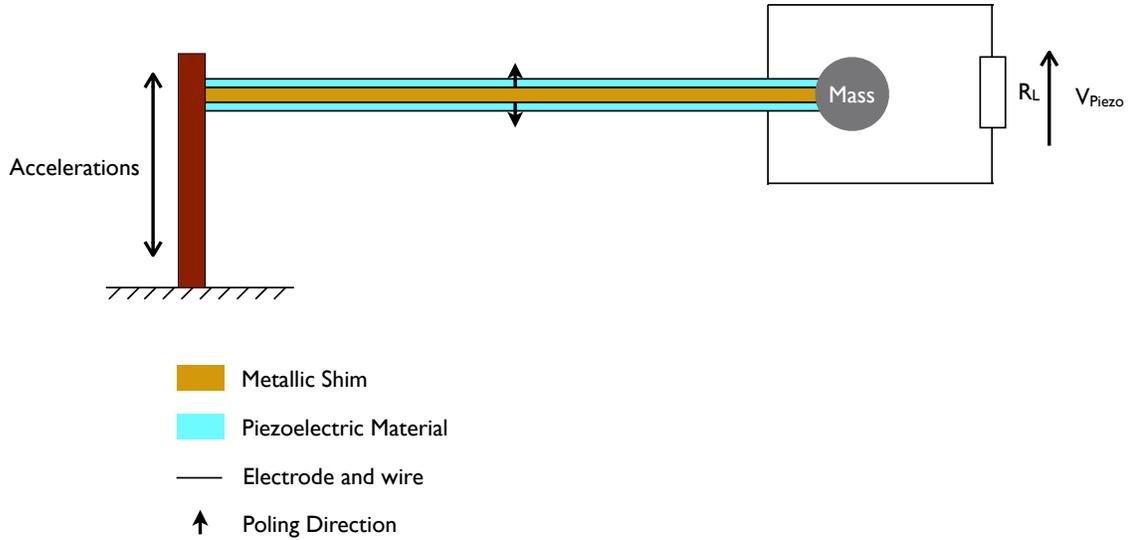
Figure 4.4: Example of a typical rectangular cantilever implementation of a piezoelectric energy harvester operating in the 31 mode with series connection with uniform width and thickness

parasitic capacitance but do not add to the harvesting ability of the device.

The capacitance of the device is one of the properties which determines its matched load and it is therefore is important to take into consideration when designing them and in understanding how they operate at high temperatures. Equation 4.1 is used when calculating the capacitance of a parallel plate capacitor, where ε_r is the dielectric constant of the material, ε_0 is the permittivity of free space, A is the area of the device and d is the separation of the plates, or in this case, the thickness of the cantilever.

$$C = \frac{\varepsilon_r \varepsilon_0 A}{d} \tag{4.1}$$

A high dielectric constant is generally preferred as it leads to a lower source impedance and, as a result, a lower maximum power load. PZT has a high dielectric constant, around 1900 for the device used in this study, and so will have a lower source impedance than a ceramic, single crystal material such as AlN, which has a dielectric constant of around 10 depending on the crystal orientation.

4.3.2 Resonance

The clamped cantilever design has several attributes which make it mechanically ideal for energy harvesting. These are:

- small input vibrations can generate significant displacement at the unclamped end when operated at resonance.

- structure exhibits mechanical resonance and can be tuned to target the environment's vibration spectra and maximise the harvested energy.

- easy to implement due to simple construction in the form of a cantilever.

- simple fabrication process allows for optimisation of the size and shape.

Of these the most beneficial is that the structure exhibits mechanical resonance. When in resonance, a cantilever has a significantly increased tip displacement compared to other frequencies and there is an increase in the strain experienced by the piezoelectric layer. This mechanical resonance, f_0, is a function of the mass of the cantilever, m, and the stiffness, k, as shown in equation 4.2.

$$f_o = \frac{1}{2\pi}\sqrt{\frac{k}{m}} \tag{4.2}$$

The bandwidth of this resonance is limited, so to harvest energy most effectively this resonance needs to be tuned to the target environments frequency spectra. The resonant frequency of the structure is proportional to its mechanical stiffness and is dependant on material properties, as shown in equation 4.3, these are Young's modulus, Y, beam length, l, and the second moment of inertia, I, which is shown in equation 4.4; where, w is the cantilever width and t the thickness.

$$k = \frac{3EI}{l^3} \tag{4.3}$$

$$I = \frac{1}{12}wt^3 \tag{4.4}$$

Combining equations 4.2, 4.3 and 4.4 produces equation 4.5.

$$f_o = \frac{1}{2\pi}\sqrt{\frac{Ewt^3}{4ml^3}} \tag{4.5}$$

Equation 4.5 shows clearly how the structure's resonance is dependant on the width, length, thickness, mass and Young's modulus. However, tuning the cantilever with these properties alone is problematic. Young's modulus is determined by the internal atomic structure of the material used and so it is very difficult to change this without deteriorating or altering the piezoelectric properties of the device. Mass is intrinsically linked to the structural dimensions of the device via the density and so it is difficult to change without affecting at least one of the structural properties.

4.3.3 Tuning

Equations 4.5 and 4.1, and discussion in the previous sections, show how interlinked the devices dimensions and capacitance are. As previously stated, piezoelectric energy harvesters are capacitive sources and so C_p, the devices capacitance, and the operating frequency, f, are the key factors in determining the matched load. Given that the capacitance is determined by the materials dielectric constant tuning the harvester for a set matched load and resonant frequency can be difficult with the properties in equations 4.5 and 4.1.

The solution to this is to use a tuning mass on the tip of the cantilever which reduces the resonant frequency proportional to its mass. This complicates the analysis of the system somewhat as the dominant mass is no longer the cantilever itself but the tip mass instead.

There is still a contribution from the cantilever but, as the m_c term in equation 4.6 shows, it is greatly diminished. Lord Rayleigh's work in to this area in 1894 allows us to use equation

4.6 to determine what tip mass should be added to a cantilever to set the resonant frequency, where m_t is the mass of the attached tip mass and m_c is the mass of the cantilever.

$$f_o = \frac{1}{2\pi} \sqrt{\frac{Ywt^3}{4l^3(m_t + (0.24)m_c)}} \qquad (4.6)$$

Equation 4.6 enables device tuning without the need to change the dimensions of the cantilever, and therefore the capacitance. As m_t tends to 0 there is an increasing divergence between the result of equation 4.6 and the true resonant frequency. As a result equation 4.6 requires that m_t is significantly larger than m_c.

4.3.4 Damping

Figure 4.5 shows the output decay of a piezoelectric energy harvester when the input vibrations are abruptly terminated and allowed to decay to rest. The piezoelectric energy harvester used to produce this data was driven at 140 mg acceleration at resonance into open circuit load.

This structure exhibits both mechanical and electrical damping and, when optimal load resistance is used, these can be assumed to be equal at resonance [16]. The electrical damping is caused by the piezoelectric conversion of the vibration energy into electrical energy and the mechanical damping is caused by the conversion of kinetic energy into thermal energy due to the internal device friction and also air resistance. The mechanical damping ratio can be determined from the decay waveform caused by abruptly ending the driving vibrations into an open circuit load, as shown in figure 4.5.

Using equation 4.7, where x_1 and x_2 are the two values labelled in figure 4.5 which are separated by n cycles, the mechanical damping ratio, ζ_m, can be determined [17].

$$\zeta_m = \frac{1}{2\pi n} ln \left(\frac{x_1}{x_2} \right) \qquad (4.7)$$

The example in figure 4.5 has a mechanical damping ratio of 0.012 which falls within the

69
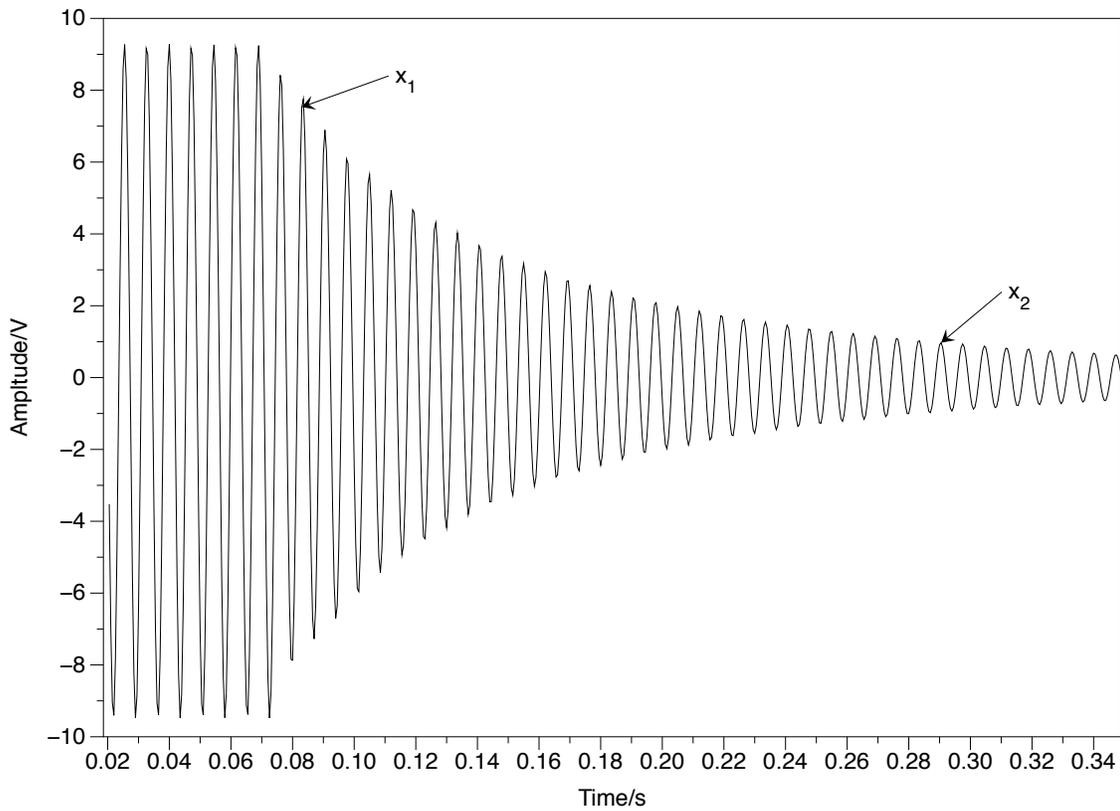
Figure 4.5: Decay of piezoelectric output voltage in open circuit after abrupt termination of driving vibrations

experimentally determined range in the literature [17].

4.3.5 Electrical Power

The magnitude of the output voltage from a piezoelectric energy harvester is controlled by the amount of strain induced in the piezoelectric structure. When the energy harvester is formed in a cantilever structure, the strain is caused by the input vibrations at the clamped end of the device. The induced strain is proportional to the tip displacement, which is in turn related to input vibration displacement. At resonance the tip displacement is the input displacement multiplied by the mechanical Q factor. By tuning the cantilever to the fundamental vibration frequency, the tip displacement is maximised for a given input acceleration. The greater the input acceleration the higher the voltage produced and, hence, the greater the power output from the device [18].

The theory of inertial based generators is well documented and the maximum power harvestable by a given system can be predicted with equation 4.12. A brief outline of the derivation is given here to aid understanding of how this formula can be applied to a system [17, 6].

Assuming the energy harvester is driven by a periodic input displacement of $y(t) = Y sin(\omega t)$ there will be a net displacement between the tip and the base, the dissipated power within this damper is given by:

$$P = \frac{m\zeta_T Y^2 \left(\frac{\omega}{\omega_n}\right)^3 \omega^3}{\left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right]^2 + \left[2\zeta_T \left(\frac{\omega}{\omega_n}\right)\right]^2}$$ (4.8)

where ζ_T is the total damping, m is the mass, and ω is the driving frequency. This equation is only valid for steady state conditions and to the power, P and so is the energy supplied per second by the application vibrations. Peak power occurs when the system is driven at resonance, ω_n and so this can be simplified to equation 4.9.

$$P = \frac{mY^2\omega_n^3}{4\zeta_T}$$ (4.9)

Equation 4.9 indicates that power varies linearly with mass, cubicly with frequency and as the square of the input displacement amplitude. Give that $A = \omega^2 Y$, where A is the acceleration, and the damping factor is related to the damping ratio by $C_T = 2m\omega_n\zeta_T$, equation 4.9 can be written as:

$$P = \frac{(mA)^2}{2C_T}$$ (4.10)

The rules above imply that a target frequency can be chosen simply based on the power output, due to the physical limitations of these systems however this can not be the case. The tip displacement is limited to a maximum, Z_max, which is related to the base displacement by the Q-factor.

Incorporating the electrical and mechanical damping into equation 4.9 gives an average

power generated of:

$$P = \frac{m\zeta_E Y^2 \omega_n^3}{4(\zeta_m + \zeta_E)^2} \tag{4.11}$$

Given that $A = Y\omega^2$ and at peak power and at resonance $\zeta_m = \zeta_E$ this can be represented as:

$$|P| = \frac{m\zeta_e |A|^2}{4\omega\zeta_T^2} \tag{4.12}$$

4.4 Experimental Setup

When testing piezoelectric devices across a wide temperature range there are several characteristic responses to consider, these include changes in:

- piezoelectric coefficient.

- dielectric constant.

- Youngs modulus.

- damping and mechanical Q factor.

Measuring and analysing how these change with temperature will give a clear indication of the devices resilience in a high temperature environment.

4.4.1 Requirements

The experimental set up for testing PZT energy harvesters to high temperature is shown in figure 4.6. The test rig is controlled by a single LabVIEW VI which use an NI DAQ PCI-6035E to produce a sweepable sine wave which controls an LDS V101 shaker stage. This stage is inverted above an oven with a steel shaft used to deliver vibrations to a sample mounted inside the oven. The oven is controlled with a manual control panel and

an internal thermometer. An ADXL203 accelerometer is attached to the base of this shaft and two cooling fans are used to keep the ambient temperature of the accelerometer within operational limits. The NI DAQ reads the analogue output from the accelerometer and the output from the attached sample and stores the data for further analysis.
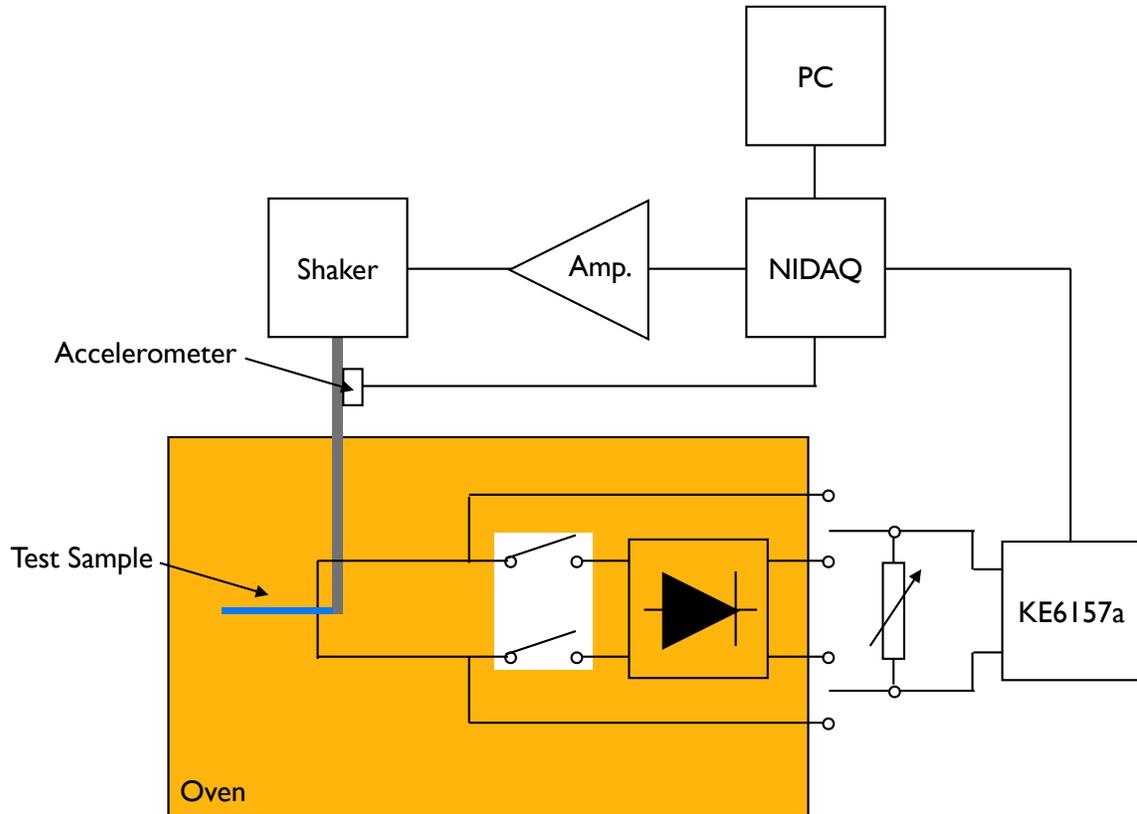
Figure 4.6: Experimental setup for testing piezoelectric energy harvesters at elevated temperatures. Sweeps show how a PID controller system is able to replicate a similar sweep in both directions but a fixed voltage test with no PID control shows deviation.

The LabVIEW VI allows voltage-frequency, sweeps in either direction, to be conducted in either closed loop proportional integral derivative controller (PID controller) mode or an open loop mode with no feedback control. It also allows for direct waveform sampling of the piezoelectric output for damping-temperature tests.
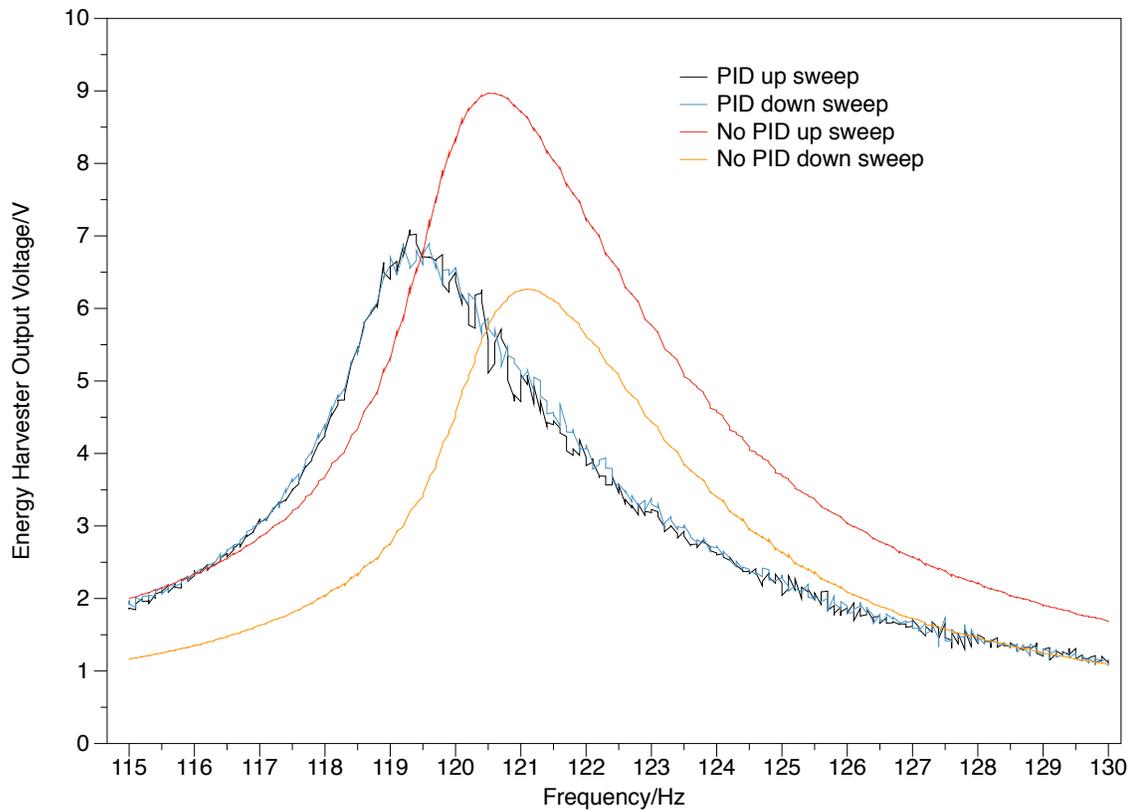
Figure 4.7: Open loop and closed loop voltage-frequency tests

Frequency sweeps

Piezoelectric vibration energy harvesters have a high mechanical Q factor, so accurate control of the driving vibration amplitude is very important for determining the change in peak output voltage at resonance as a function of temperature. The mechanics of this system are very complicated and as such lead to highly dynamic changes in the supplied acceleration if not adequately controlled. The data in figure 4.7 compares the energy harvester output for both a closed loop PID controlled test and an open loop test. All tests were conducted at an initial acceleration of 100 mg (0.981 ms^{-2}) and both frequency-up and frequency-down sweeps were conducted.

It is clear that there is a significant difference in the measured acceleration for the uncontrolled open loop experiment, where the output from the energy harvester matches the closed loop data only at the start of the test. For the closed loop PID tests the data matches

for both up and down tests. The data is however noisier than the open loop test, this is caused by the PID control system taking time to converge on the correct set point.
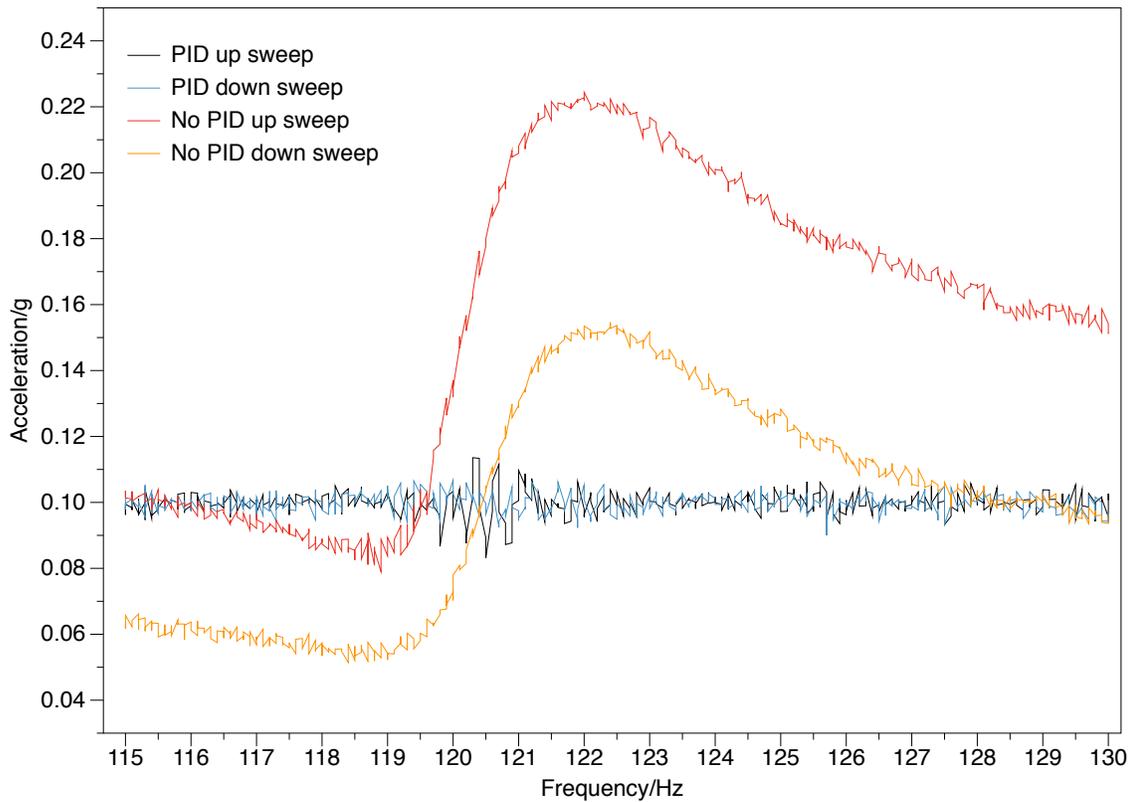
Figure 4.8: Results of open loop and closed loop acceleration-frequency tests highlighting the variation from the initial set point when using an uncontrolled, constant voltage driven input vibration.

The data in figure 4.8 shows the acceleration response for both open and closed loop experiments. The data shows how the acceleration quickly deviates from the set point in both of the uncontrolled tests and shows that for the up sweep the final acceleration is greater than the set point and that for the down sweep the data is below it. This has caused the increased and decreased peak voltage output for the open loop tests in comparison to the closed loop ones.

The variation in driving acceleration is caused by two factors. The first is that acceleration is proportional to the square of frequency as it is the second derivative of displacement. Therefore, should the amplitude of the input signal to the shaker remain constant the

acceleration will naturally increase in a positive frequency sweep and vice versa for a negative sweep. The is highlighted by the derivation of acceleration:

$$
\begin{aligned}
y(t) &= Y sin(\omega t) \\
\frac{dy(t)}{dt} &= Y\omega cos(\omega t) \\
\frac{dy(t)}{dt} &= -Y\omega^2 sin(\omega t)
\end{aligned}
\tag{4.13}
$$

where $y(t)$ is the base displacement as a function of time and ω the frequency of the driving vibrations. Using the uncontrolled up sweep in figure 4.8 however it is possible to determine that this increase does not account for all of the increase observed, if is did then the acceleration would increase from 0.1g (0.981 ms^{-2}) at 115 Hz to 0.127g (1.24 ms^{-2}) at 130 Hz. The remaining acceleration increase, that accounts for both the difference at 130 Hz and the peak at 122 Hz is due to a phase change in the piezoelectric harvester which occurs at resonance. This phase change means that the piezoelectric harvester vibrations superimpose themselves on the driving vibrations and begin adding energy to the system. It is this phase change that also makes PID control of such systems difficult and time consuming and the energy transfers are taking place rapidly and can lead to an unstable system.

Under room temperature testing conditions, the closed loop system would be used as the sweep could be run sufficiently slowly to provide a clean data set and the output of the accelerometer would be consistent as the room would maintain a near constant temperature. In this case, however, the elevated temperatures place a maximum time limit on how long a test can be conducted before the transient temperature variations in the material become less significant than longer term thermal stress effects.

As a result the results presented in the rest of this chapter have been collected on a system which uses a constant fixed voltage driving the shaker stage with no PID control applied. To aid repeatability the sweeps were always carried out with a positive frequency sweep and

the same start acceleration set with a 20 second settle time prior to the commencement of the sweep.

4.4.2 Cantilever Choice

Discussions in the previous section supply the tools necessary to design a piezoelectric cantilever suitable for testing to high temperature. As the stiffness of most materials decreases with temperature, it was assumed the same would occur when testing a PZT energy harvester at elevated temperatures and so the cantilever was designed to have a relatively high room temperature resonant frequency. 140Hz was chosen as it is close to the fundamental frequencies found in industrial environments [12] and, as results will show, accommodated the decrease in resonant frequency across the observed temperature range. 400mg acceleration was chosen up the advice of an industrial adviser to this project and represents a standard acceleration available in their environments.

For the experiments a Piezo Systems T220-A4-303X energy harvester was chosen as the piezoelectric material is PZT-5A and so has a Curie temperature of 325 °C, it has a brass central metallic shim which will not react at the temperatures tested at and it comes as a bare, unpackaged device which can be clamped and used at elevated temperatures.

Given the target frequency of 140 Hz, equation 4.6 was used to determine that with a tip mass of 1.7 g a Piezo Systems T220-A4-303X would have a resonant frequency of 140 Hz.

For the purposes of temperature testing the capacitance of the device is of interest as it gives an indication to the devices piezoelectric condition. The device electrodes were removed from under the clamp so as not to add unnecessary capacitance and allow focus on the active area. Figure 4.9 shows the final assembly mounted in the experimental rig designed for high temperature testing.

Figure 4.9 shows the tip mass attached via a light weight metallic G-clamp and screw. The tip mass is a tungsten weight of 1.7 g and as such is significantly heavier than the cantilever.
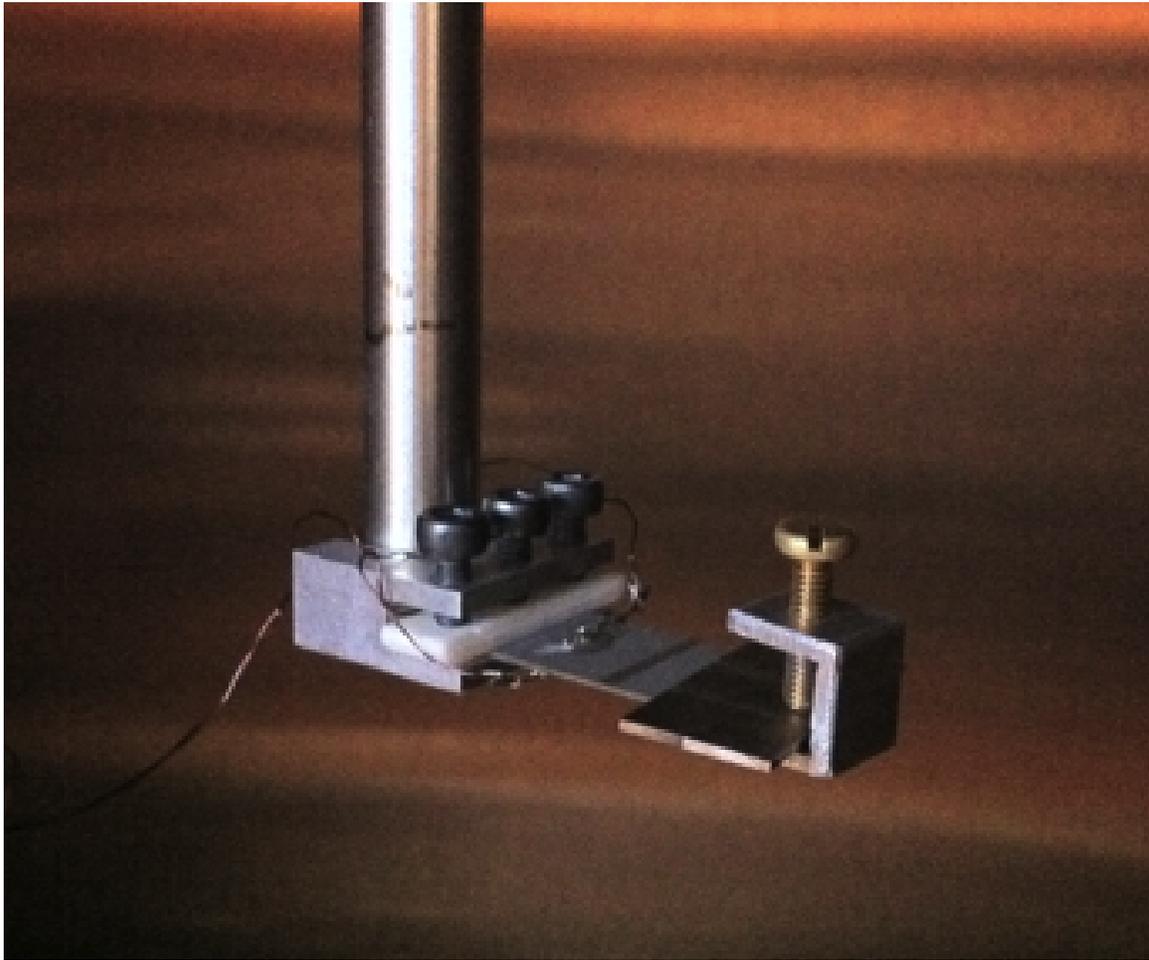
Figure 4.9: Photograph of a PZT energy harvester mounted in the high temperature test rig

It is electrically isolated from the cantilever contacts with a small thin piece of AlN ceramic tile; the weight of which has a negligible effect on the system and can be ignored.

4.5 Temperature Effects

4.5.1 Resonance

To investigate the effects of temperature on the device a series of voltage vs frequency sweeps we conducted from room temperature to 573 K in 25 K increments. The device was held at each temperature for 5 minutes including a 3 minute settle time. At the end of the testing

for a given temperature the oven was set to the next temperature, the increase time between each temperature took between 7 and 10 minutes. Each figure presented is from a single device which shows typical behaviour observed across 7 devices from testing conducted over the course of 18 months from two separate batches of Piezo Systems T220-A4-303X harvesters purchased 12 months apart.
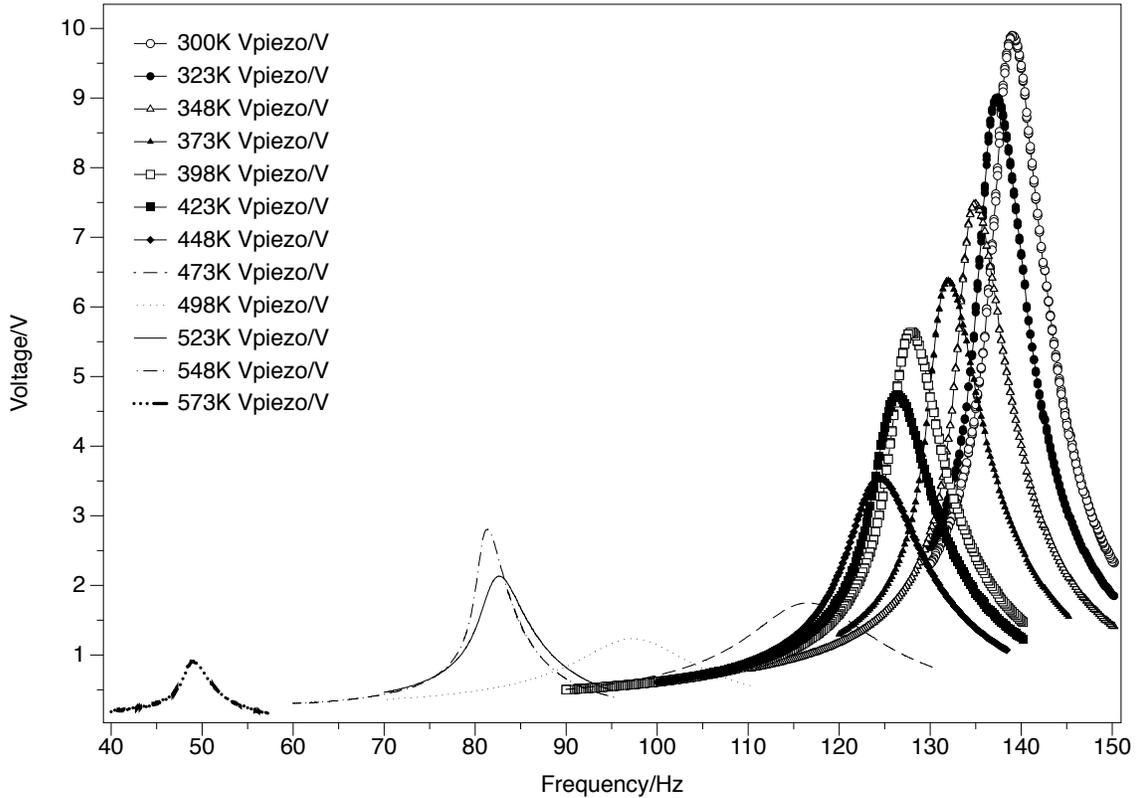
Figure 4.10: Change in resonance and voltage output with temperature of a PZT energy harvester at 400mg vibration acceleration

The data in figure 4.10 shows how the resonance curve changes for a device heated from room temperature to 300 °C. It is clear that the resonant frequency shows a negative temperature coefficient. Analysis of equation 4.14 shows that of the factors controlling resonant frequency only the Young's modulus is likely to change. It is possible to rearrange equation 4.6 to get equation 4.14 and extract the effective Young's modulus of the device.

$$Y = 2\pi f_0^2 \frac{4l^3(m_t + (0.24m_c))}{wt^3} \tag{4.14}$$

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Equation 4.14 allows for the extraction of the device's effective Youngs modulus, this includes the PZT layer and the central brass shim. In this instance it is key to understand how the device responds as a whole to the increased temperature and so by extracting the effective Youngs modulus and plotting as a function of temperature figure 4.11 can be produced. That values in figure 4.11 are consistent with the literature [7, 3, 19]

The data in figure 4.11 shows a clear decrease in Young's modulus with temperature and indicates that there are two linear regions with an inflexion at 450K. This inflexion could indicate that an elastic limit has been reached and that if cooled it will not return to it's original stiffness.
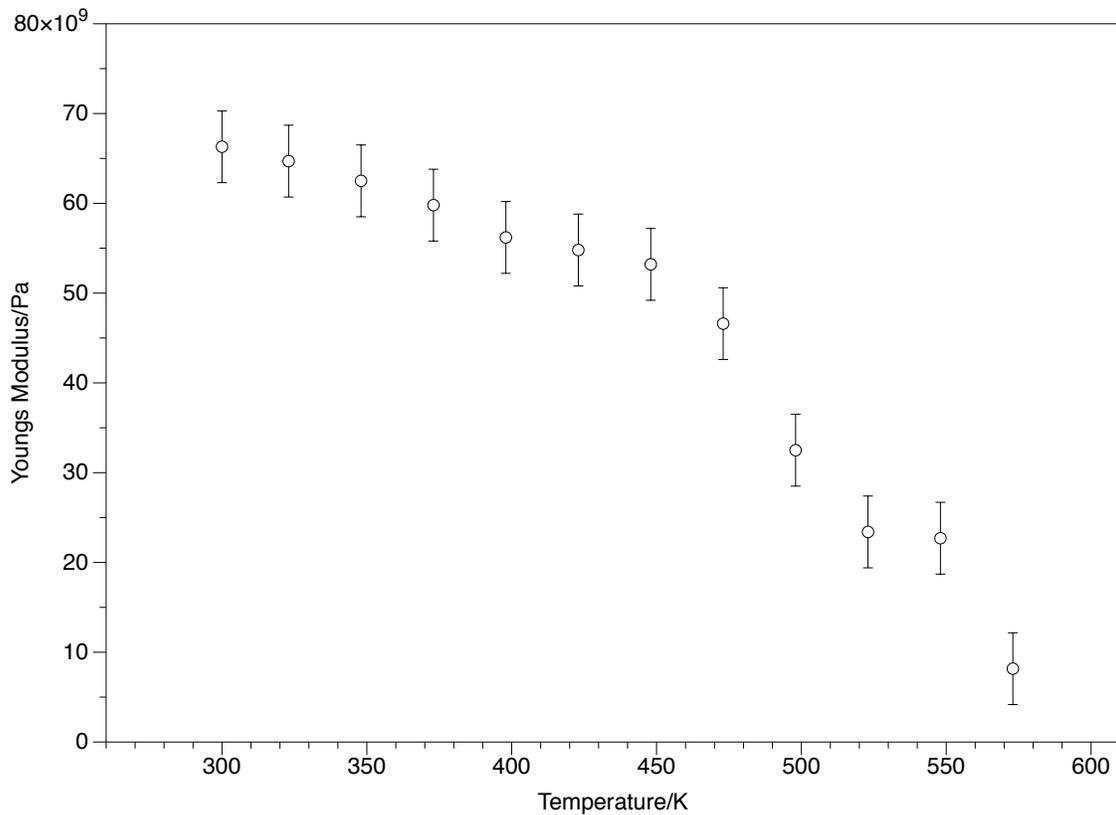

Figure 4.11: Variation in Young's modulus with temperature at 400mg vibration acceleration

It is important to understand if the inflexion point in figure 4.11 represents a permanent change in the resonant frequency or if it is reversible. To test this, a new device was heated to 523 K and tested at 25 K intervals in both directions. The data in figure 4.12 shows how

the resonant frequency changes with temperature during heating and cooling. It is apparent that the resonant frequency recovers to 3.7 Hz less than its initial room temperature value of 144.5 Hz exhibiting hysteresis at the upper temperatures. This indicates a slight decrease in resonance caused by the temperature cycle.
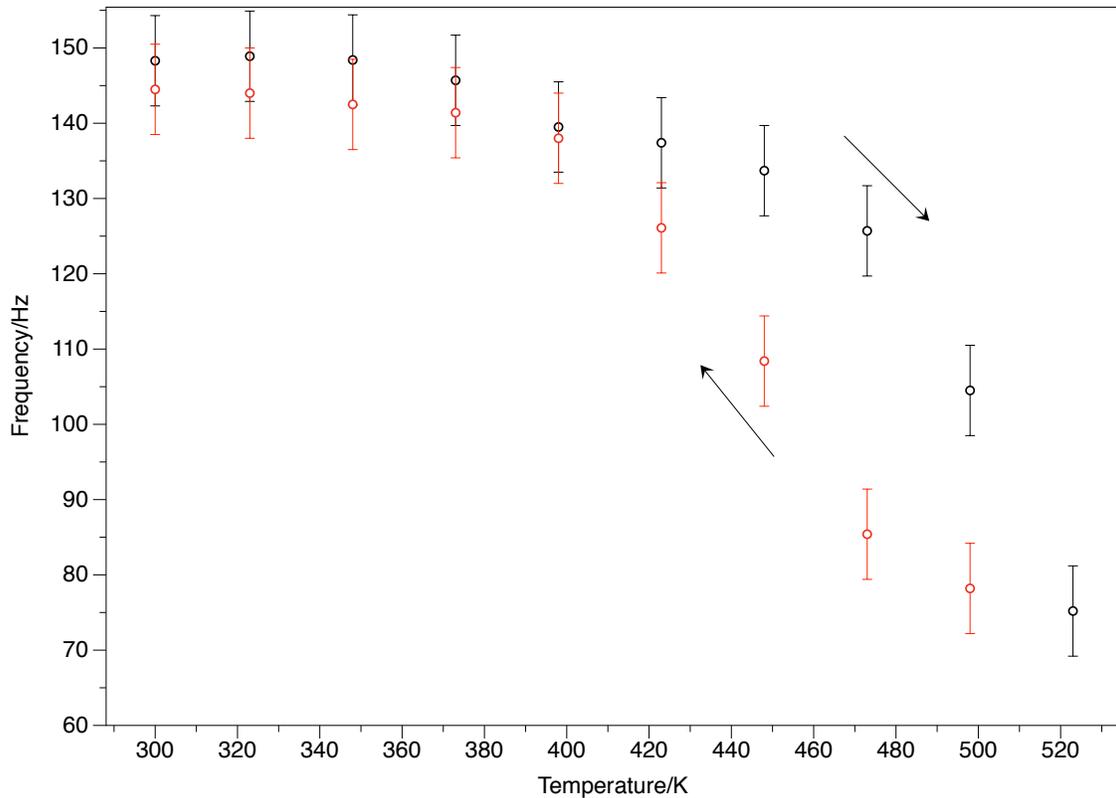
Figure 4.12: Effect of increase and decrease in temperature on resonant frequency

Given that the resonant frequency recovers to near its original value it is unlikely that the inflexion represents an elastic limit, more likely it is due to a change in the piezoelectric properties affecting the resonance caused by temperature.

The data in figure 4.13 shows how the voltage output changes during this test, it is clear that the piezoelectric properties of the device have been changed as the room temperature output is not recovered. The test was not run to the full temperature range as the focus was to investigate the effects of passing the inflexion at 450 K and not to further investigate the effects of heating the device up to, or near, the material curie point.
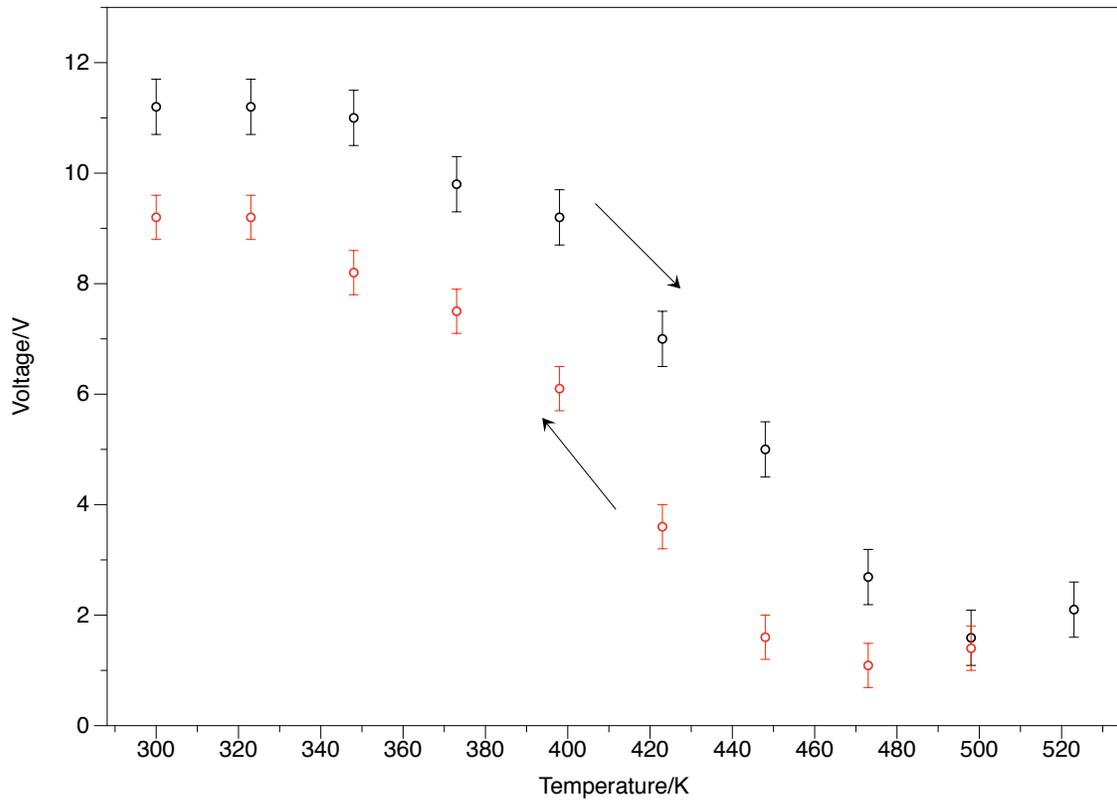
Figure 4.13: Effect of increase and decrease in temperature on resonant output voltage

Besides the decrease in resonant frequency the other notable change occurs in the peak output voltage at resonance. The characteristics shown in figure 4.10 and 4.13 however, indicate that the voltage does not decrease with a single trend and that it recovers around 450K.

As previously discussed, these devices exhibit mechanical damping, the influence of which is determined by their mechanical properties. Young's modulus changes with temperature and it is important to understand the effect this has on the system damping. The data in figure 4.14 demonstrates how this property is affected by the temperature change and the effects it has on the output voltage of the system. The data shows that the mechanical damping ratio changes significantly across the temperature range and peaks at 473K. The high mechanical damping ratio at this temperature is likely to be the reason for the reduced voltage output observed at 473K and 498K. The mechanical damping ratio decreases at temperatures above 473K which causes the output voltage to increase slightly before finally
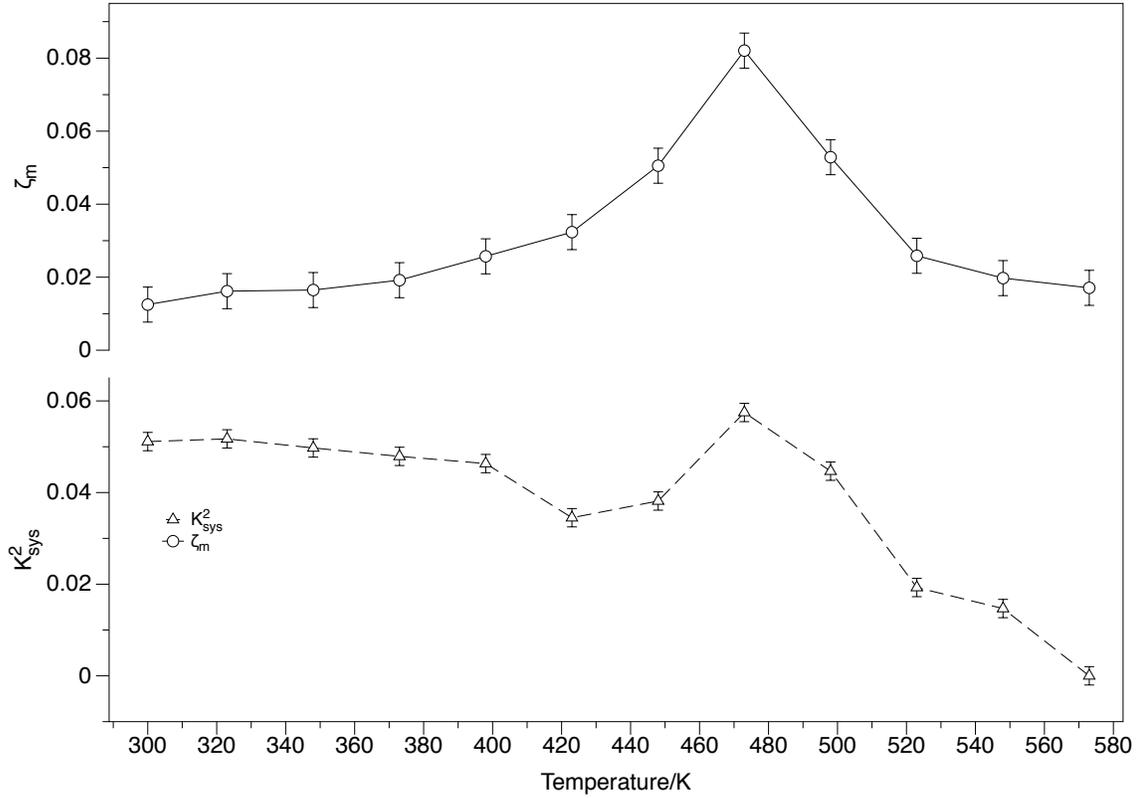
Figure 4.14: Mechanical damping as a function of temperature indicating a peak at 473 K

decreasing significantly around the material curie point.

The data for the mechanical damping ratio presented in figure 4.14 was collected by recording the decay waveform produced from abruptly terminating the input vibrations for a device driven at resonance in open circuit at each temperature. Two points were then chosen, as depicted in figure 4.5, and then equation 4.7 was used to extract the mechanical damping ratio.

The data in figure 4.14 also shows how the system electromechanical coupling coefficient, K_{sys}^2 varies with temperature. K_{sys}^2 give an indication of how effective the system is at converting the kinetic energy in the system into electrical energy and is extracted using equation 4.15, where ω_{sc} and ω_{oc} are the short-circuit and open-circuit resonant frequencies respectively [16, 20].

$$K_{sys}^2 = \frac{(\omega_{oc})^2 - (\omega_{sc})^2}{(\omega_{oc})^2} \tag{4.15}$$

The data shows there is a general decrease in K_{sys}^2 with respect to temperature indicating that the system degrades with temperature. K_{sys}^2 does increase significantly around 473 K, however the output voltage at this temperature remains suppressed due to the increased mechanical damping.

4.5.2 Capacitance

As previously discussed, the energy harvester is a capacitive source and so the change in dielectric properties of the PZT with temperature will affect the capacitance and, therefore, the matched load. Being a capacitive source the matched load can be calculated with equation 4.16 [11].

$$Z = \frac{1}{2\pi f C_p} // R_{sh} \tag{4.16}$$

R_{sh} is the effective parallel resistance of the device and is several orders of magnitude larger than the capacitive reactive component and can therefore be ignored as it has negligible effect on the overall system impedance. The data in figure 4.15 shows the experimental determination of the matched load and the calculated value given the resonant frequency and capacitance at each temperature. The experimental data fits the calculated trend showing that the assumption that R_{sh} is large enough to be ignored is valid and that the change in capacitance and frequency remain the dominant influencing factors. The increase in matched load at 573 K indicates that the capacitance has dropped significantly and that the dielectric is beginning to de-pole and lose the piezoelectric properties, hence the Curie point has almost been reached.
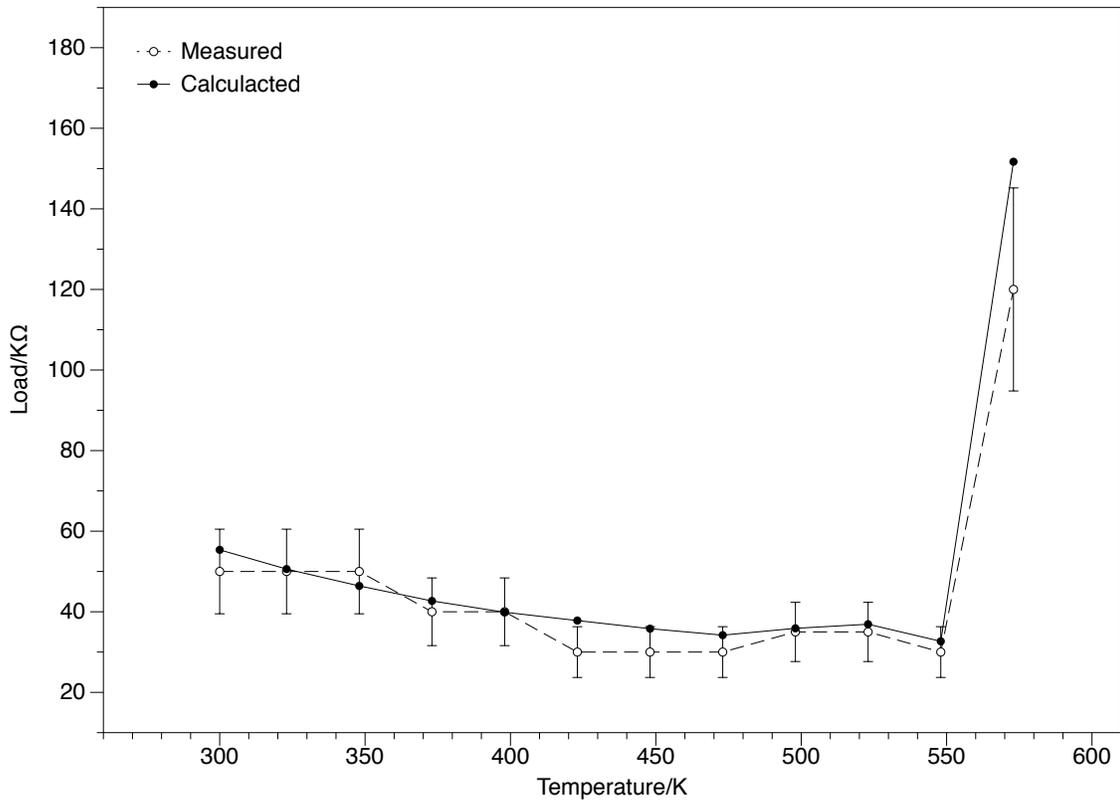
Figure 4.15: Experimentally extracted and theoretically calculated matched load value as a function of temperature with sign of device de poling at 573 K

4.5.3 Voltage Rectification

The electrical output from the piezoelectric energy harvester is an AC signal and requires rectification before it can be used to power a circuit. Given the desired high temperature operation of this system a silicon carbide Schottky diode full wave rectifier was used to rectify the energy harvester output. The data in figure 4.16 shows how the voltage drop of a SiC Schottky diode changes with temperature. The data in figure 4.16 was extracted from 0 A x-axis intercept of IV sweeps carried out with a Keithley 4200 source meter. SiC devices can operate at high temperatures, however as figure 4.16 shows, there is a linear temperature dependant decrease in the diodes built in voltage drop of 2 mV/K.

When configured as a full wave rectifier the total voltage drop will be double that for a single diode as the AC signal must pass through two diodes before reaching the positive
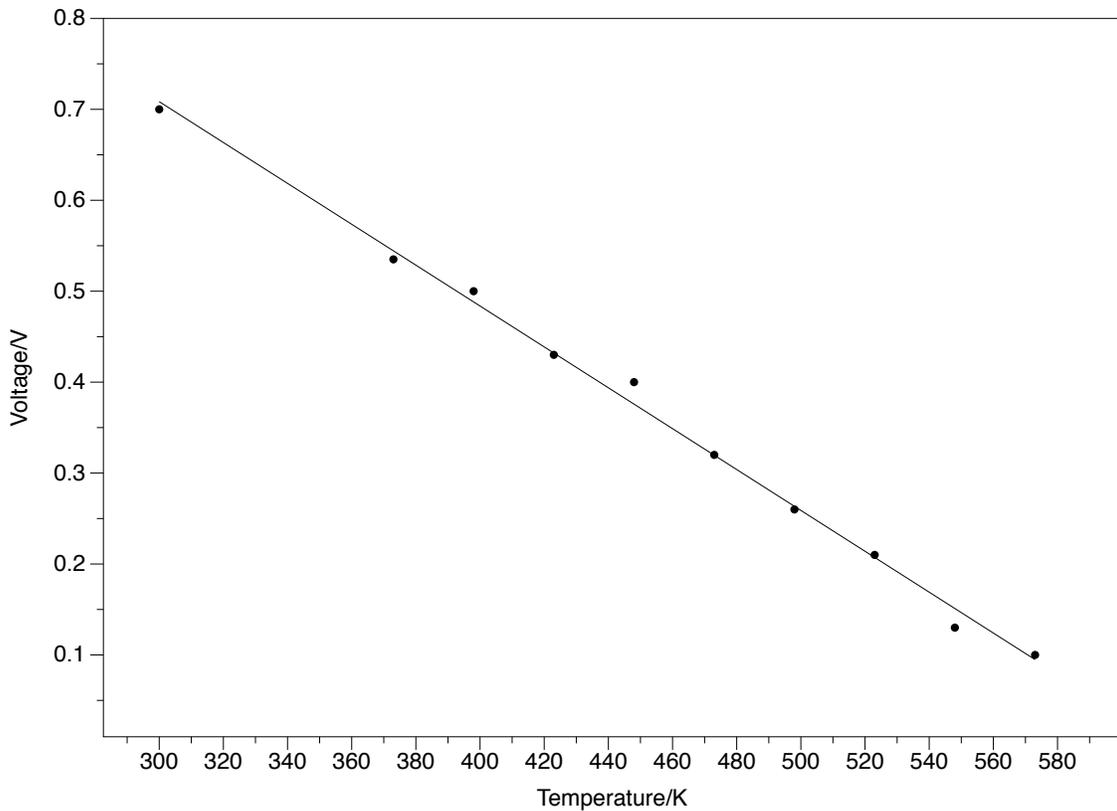
Figure 4.16: Change in Schottky diode voltage drop with temperature

output terminal of the rectifier. At 300 K this voltage drop is 1.4 V, much less than the output of the energy harvester. At 600 K this voltage drop will be 0.2 V which is still less than the energy harvester output at this temperature and so will provide a suitable rectification method.

To investigate the effects on increased temperature on the whole system, the piezoelectric energy harvester was driven at 400 mg and connected to the input of the full wave rectifier. The output power of the rectifier was measured when loaded with a 1 MΩ and with the measured matched loads shown in figure 4.15. Figure 4.17 shows the change in rectified power with temperature, it shows that the power significantly decreases with temperature from 320 μW at room temperature, to 80 μW at 573 K, into the matched load. The reason for the low correlation between the matched load data and the data fit is due to the error in the matched load determination and the high dependance the output power has with temperature, for this reason the test was also run with a 1 MΩ load. At room temperature
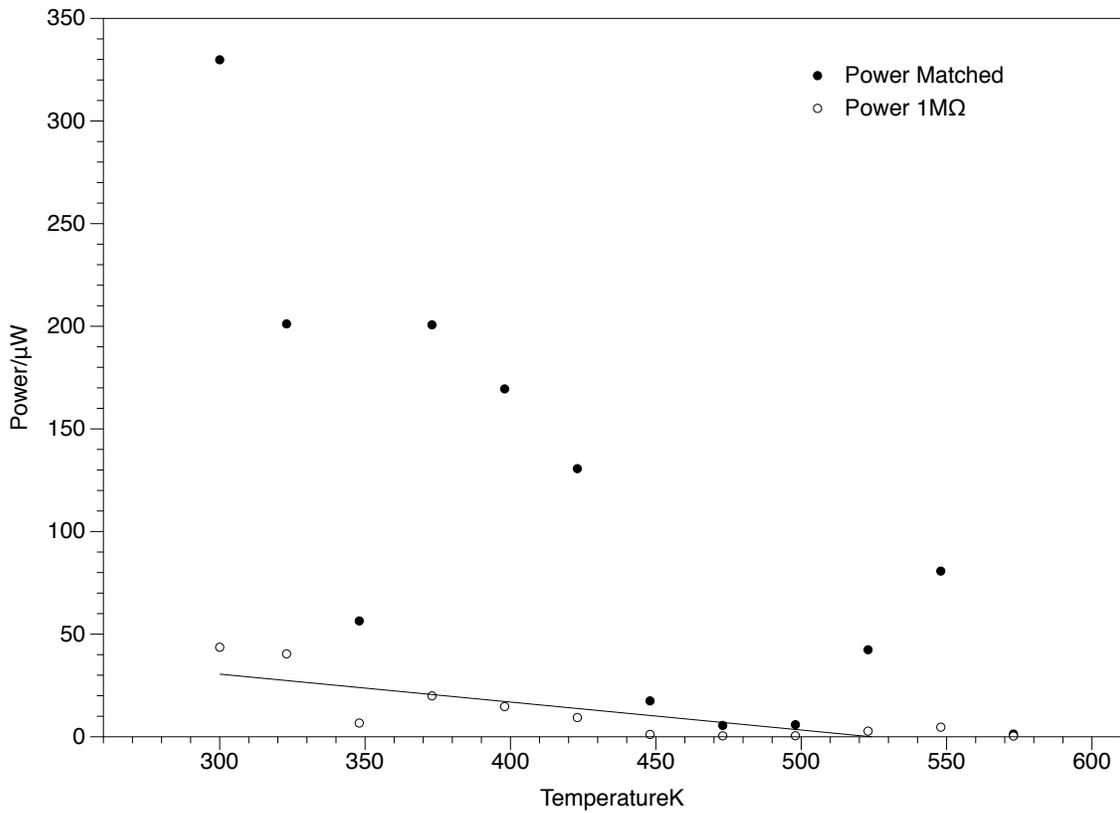
Figure 4.17: Power delivered to both matched and 1 MΩ loads change with temperature

the power delivered to the 1M Ω load is 50 μW, this decreases to 7 μW at 573 K,a decrease by a factor of 7.1 times, which is comparable the matched load scenario decrease of a factor of 4.

To determine if the full wave rectifier is fully operational at the elevated temperatures and not simply acting as a half wave rectifier, the output wave form of the rectifier can be analysed. The un-smoothed output from a full wave rectifier should have a frequency twice that of the input waveform, and no part of the signal below 0 V. Figure 4.18 compares the output from the rectifier at room temperature to 573 K, when the piezoelectric energy harvester is driven at resonance. The output waveform at room temperature has frequency of 285 Hz and at 573 K a frequency of 87 Hz, these are twice the input frequency and show that the rectifier is fully operational.
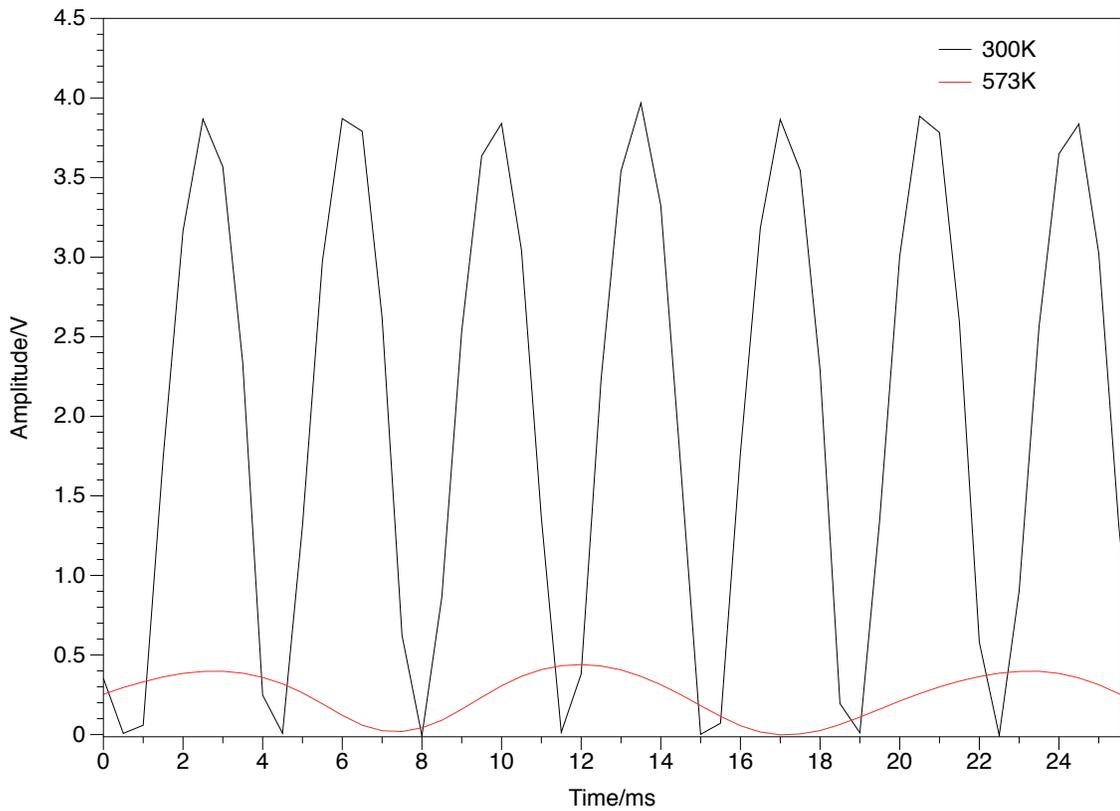
Figure 4.18: Voltage output waveform from rectifier at room temperature and 573 K, waveform at 300 K is running close to the sample rate of the system but clearly is still operating as a full wave rectifier

4.6 Conclusion

This chapter discussed the fundamentals of piezoelectric materials and highlighted where the weaknesses lie in using the most developed material, PZT, in a hostile environment. Experimental tests of a PZT energy harvester showed that as the temperature increases the Youngs modulus of the material decreases as does the output voltage. Interestingly a non-montonic decrease in output voltage is observed, this is likely caused by a change in the mechanical damping coefficient changing the amount of vibration energy which is converted into electrical energy.

Although the results presented in this study show that PZT energy harvesters exhibit significant temperature dependance, with a decrease in peak voltage at resonance from 11.5

V at room temperature to 2.1 V at 523 K, when coupled with a resilient SiC rectifier it is capable of harvesting energy at temperature up to 523 K. Given that the device resonant frequency decreased to 75 Hz at 523 K, from 148 Hz at room temperature, it is clear that the target environment temperature and variation would need to be thoroughly understood and accounted for when designing the system as any self tuning electronics would be too sophisticated to be included in the system.

The device showed good frequency recovery to within 4 Hz of the room temperature resonant frequency however the room temperature peak output voltage decreased by 2V indicating the the piezoelectric constants experienced some degradation with the temperature exposure.

These results indicate that up to 500 K a PZT-5A harvester could be a suitable energy harvester device to deploy in a hostile environment. It is important to note though that further research should be conducted in to a number of aspects. The focus of these experiments was to identify characteristic changes with transient temperature variation and not, as would be the case in a permanent deployment, the long term effects of elevated temperatures and so this would need further investigation.

One area that the work has also not considered is how the Curie temperature varies with increased strain. The literature indicates that high strain applications, which could be caused through sudden shocks, can reduce the Curie temperature. This could be investigated by testing the device at a range of accelerations at a range of elevated temperatures or repeating the tests conducted in this work with a lager number of devices at a range of temperatures.

Finally, testing a cantilever with a different shape that distributes the strain more uniformly along its length would prove useful as it may identify a way in which the maximum operating temperature can be extend as the effect of strain reducing the Curie temperature could be suppressed. Such a design could also make use of the d_{33} coefficient by using an interdigited electrode instead of the parallel plate style ones used in this study. This could further increase the useful operating temperature range as the d_{33} coefficient is twice that of the

d_{31}.

Future work would consider this aspect of device degradation however as likely deployment environments are consistently hot and therefore the long term failure mechanisms of the devices would be critical to understand.

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Chapter 5

Silicon Carbide Photovoltaics for Hostile Environments

As discussed in the introduction, there has been significant development in the field of silicon solar cells over the past several decades - from large scale solar farm installations to milliscale devices for powering sensor nodes. However, the maximum operating temperature of silicon is limited to around 150°C due to the increase in intrinsic carrier concentration with temperature, as such, this renders silicon solar cells unusable in high temperature environments. Also, unlike the internal system electronics, an external solar cell can not be shielded from radiation or noxious gasses and so would eventually fail. Wide band gap semiconductors, such as SiC, can be used to temperatures far beyond that of silicon [1].

This chapter explains the photovoltaic effect and then explores the behaviour of silicon carbide pn junctions at elevated temperatures when exposed to UV light. Results show that silicon carbide is immune to some of the issues which plague silicon devices and it is demonstrated that although fabrication of large area silicon carbide junctions are problematic, there are methods which can be employed to overcome this when necessary. Finally the failure mechanism of thermally stressed SiC devices is explored to determine if long term deployment is possible.

5.1 Photovoltaic Theory

The photovoltaic effect is the conversion of light into electrical energy through the use of a pn junction. The properties of a pn junction mean electrons need to be supplied with energy to promote them into the conduction band, which can be achieved by exposing the junction to light. For the photons irradiated from a light source to be able to create an electron-hole pair, they must have an energy greater than the band gap of the material [2]. This energy promotes an electron to conduction, however, unless the electron is able to successfully cross the depletion region of the junction it will recombine and return to valence.

When an ideal diode is at 0V bias, it is in equilibrium as the drift and diffusion currents balance such that there is no net current flow and the voltage across the device remains 0V. When it is in forward bias there is a measurable increase in current through the device and, so long as the applied voltage is greater than the diodes turn on voltage, it has a constant voltage drop determined by the barrier height. When in reverse bias the device does not conduct and so no net current passes through the device until the reverse breakdown voltage is reached [3].

When operated as a solar cell no external bias is applied to the device. The incident photons absorbed by the junction elevate valence electrons into the conduction band and so a net reverse current flows. This current is called the photocurrent and if the cell has 100% quantum efficiency then it can be calculated using equation 5.1, where I_{ph} is the photocurrent magnitude, N the number of photons incident on the junction with an energy greater than the material band gap and q the elemental charge.

$$I_{ph} = qN \tag{5.1}$$

A real device is not ideal however, so the photocurrent is less than that calculated with equation 5.1. I_{ph} for a given device can be found by measuring the short circuit current,

I_{sc}, which flows when the device is illuminated. I_{sc} is the maximum current the device will produce for a given illumination and, as equation 5.1 shows, it is proportional to the intensity of the light source which is incident on the device.

When in open circuit the photo generated charge collects at the terminals of the device, this generates a bias which effectively forward biases the diode. As more charge collects at the terminals the voltage increases until the forward bias current it generates is equal and opposite to the photo generated current. This is called the open circuit voltage, V_{oc}, and is governed by the turn on voltage of the device. It changes very little with illumination intensity as forward current flow is exponentially proportional to voltage, as shown in equation 5.2 [3].

$$I = I_0 \left(exp \left(\frac{qV}{k_B T} \right) - 1 \right) \tag{5.2}$$

In equation 5.2, I is the forward current, I_o the reverse saturation current, q the elementary charge, n the ideality factor, k_B the Boltzman constant and T the junction temperature. The photocurrent can be simply factored into equation 5.2 as a negative current, I_{ph}, as shown in equation 5.3.

$$I = I_o \left(exp \left(\frac{qV}{n k_B T} \right) - 1 \right) - I_{ph} \tag{5.3}$$

The data in figure 5.1 demonstrates how a photocurrent of 1 mA affects the dark diode IV characteristic and shows that a solar cell generates power in the 4th quadrant and is therefore connected in the reverse orientation compared to a conventional diode. The illuminated curve shows that at 0 V the reverse current is the photocurrent. It also shows that when the illuminated curve is at 0 A the dark curve is at 1 mA, demonstrating the V_{oc} is the point at which forward and reverse currents balance [4].

Equation 5.3 shows that the net photocurrent from a device is what remains once the photo generated current is subtracted from the forward current. The un-illuminated device current
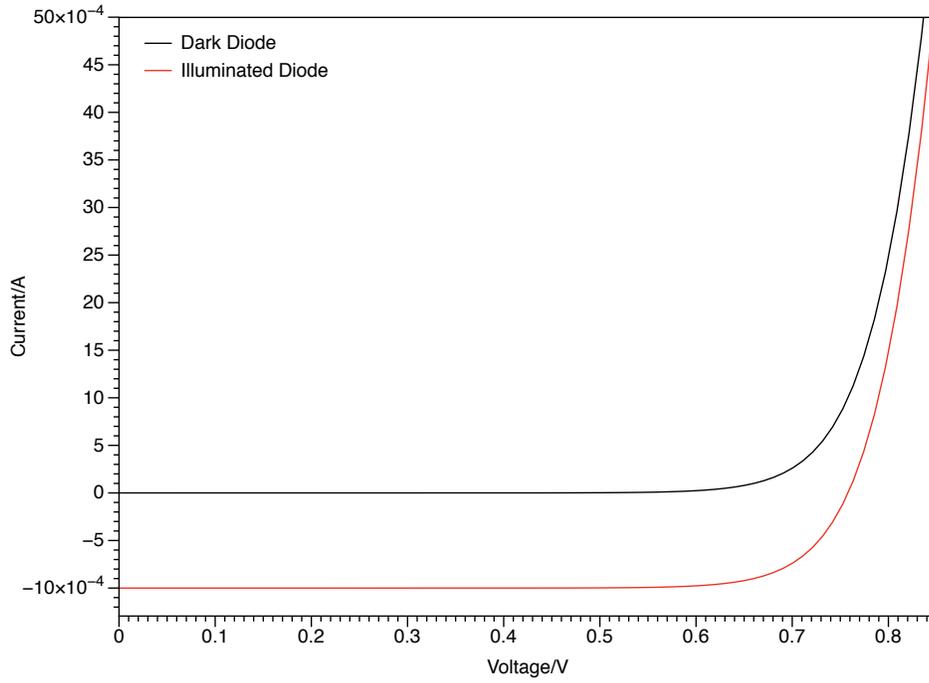
96

Figure 5.1: Simulated dark and illuminated diode I-V response

at 0V is equal to the reverse saturation current, which is governed by device and material properties. As such, minimising the reverse saturation current is beneficial to solar cell operation as it maximises the ratio $\frac{I_{ph}}{I_o}$ and so the device generates a larger short circuit current [3]. Equation 5.4 shows that I_o increases exponentially with temperature.

$$I_o = N_C N_V \left(\frac{1}{N_A} \sqrt{\frac{D_n}{\tau_n}} + \frac{1}{N_D} \sqrt{\frac{D_p}{\tau_p}} \right) exp \left(\frac{-E_g}{k_B T} \right) \tag{5.4}$$

Where N_c and N_v are the density of states at the conduction band and valence band edges respectively, N_A and N_D the p- and n-type impurity concentrations, D_n and D_p the diffusion coefficients of the minority carriers, τ_n and τ_p the minority carrier life times [3].

The reverse saturation current increases monotonically with temperature and will have a detrimental effect on the photovoltaic response of the device. The importance of the $\frac{I_{ph}}{I_o}$ ratio is best demonstrated by equation 5.5 which is a rearrangement of Shockley's equation for $I = 0$A. It shows a low $\frac{I_{ph}}{I_o}$ results in a small V_{oc}.

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$$V_{oc} = \frac{k_B T}{q} ln \left(\frac{I_{ph}}{I_o} + 1 \right) \tag{5.5}$$

There are many other device properties which affect solar cell operation, however discussion of this is saved until experimental data is provided to place the effect of these properties in context.

5.2   SiC for Photovoltaics

Silicon carbide is a wide band gap semiconductor with a band gap of 3.23eV for the 4H-SiC polytype [5]. This wide band gap provides silicon carbide with some unique properties favourable for operating in hostile environments. It is operable to temperatures above 600K [6] [7] [8], inert to noxious gases and chemicals at room temperature [9], radiation tolerant and the second hardest naturally occurring material with a Young's modulus of 424 GPa [10]. These properties make it an ideal candidate for use in a hostile environment, however, its wide band gap does limit its applicability as a solar cell as the incident photons need to have an energy greater than 3.23eV. According to equation 5.6, where h is Planck's constant, c is the velocity of light and E_g is the band gap energy, this equates to a wavelength of 383nm or less.

$$\lambda = \frac{hc}{E_g} \tag{5.6}$$

This makes silicon carbide blind to the majority of the terrestrial solar spectrum, and limits its usage to UV rich environments. This has lead to the development of excellent UV specific high temperature optical detectors [11] but in this instance the focus will be on obtaining the maximum power out at 0 V bias. The operable temperature range at which a silicon device can operate in as solar cell is limited by the exponential increase in reverse saturation current with temperature. This increase in I_o is caused by the increase in intrinsic carrier concentration and because silicon carbide has a very low room temperature intrinsic carrier

concentration it takes a much higher temperature to achieve a high I_o. As such, significantly higher temperatures are needed with silicon carbide devices for the $\frac{I_{ph}}{I_o}$ ratio to decrease to an unacceptable level [2].

The wide band gap of SiC also means that silicon carbide pn junctions usually have a significantly larger turn on than silicon devices [12] [13]. This means that the V_{oc} of a SiC device is larger than V_{oc} for a silicon device, because the voltage at which the forward bias currents equal the photocurrent at a given illumination is greater. This is shown with equations 5.7 and 5.8, showing that an increasing E_g will decrease n_i, which will in turn produce a larger V_{bi}. 4H-SiC has a band gap of around 3.23 eV compared to 1.12 eV for silicon and so depending on the doping concentration, the barrier height of a silicon carbide devices is around 4 times that for an identical silicon device of 0.7 V [3].

$$n_i = (N_C N_V)^{\frac{1}{2}} exp\left(\frac{-E_g}{2k_B T}\right) \tag{5.7}$$

$$V_{bi} = \frac{k_B T}{q} ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{5.8}$$

To determine the effectiveness as a high temperature solar cell, devices were fabricated for high temperature evaluation and long term stress testing. The design of the devices is outlined initially followed by a rigorous analyses of their ability to operate at temperatures from room temperature to 600K. This analysis consists of C-V characterisation for determining device properties and dark and illuminated I-V experiments to characterise the devices performance as a solar cell. Following this an array of devices is made to overcome some of the limitations of current silicon carbide technology and a discussion of optimising this array is pursued. A thermal stress test is presented finally to determine its long term stability.
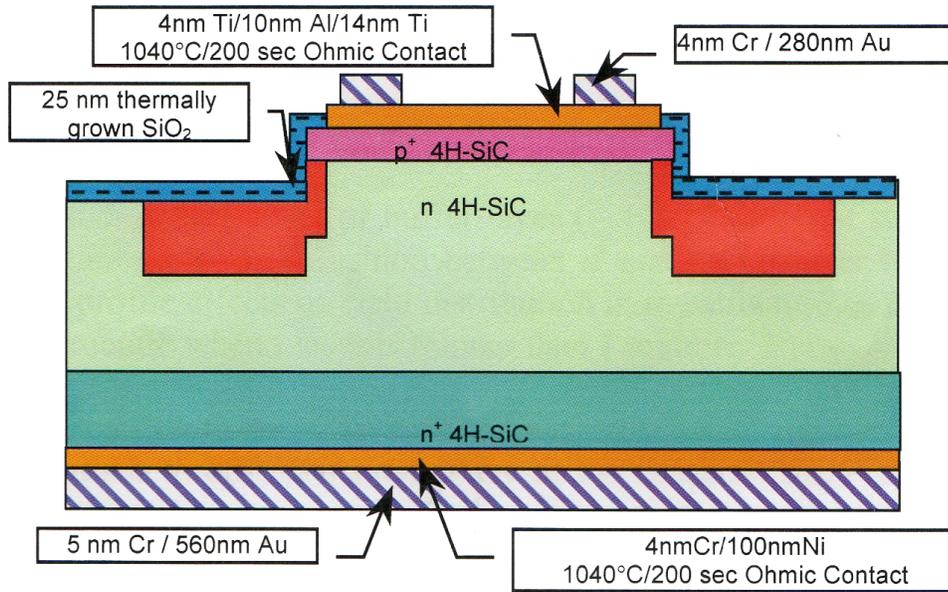
Figure 5.2: Schematic of UVPV cell

5.2.1 Device Design

Once an electron is promoted from the valence band, the electric field across the depletion region will separate the electron hole pair to opposite terminals of the device. For this to work effectively it is best for the electron hole pair to be created inside the depletion region so that they are separated successfully before they recombine. Only a small number of carriers generated outside the depletion region are able to diffuse into the depletion region [14]. It is therefore advantageous to use a device with a large surface area and large depletion region to maximise the number of photons which can successfully create an electron hole pair. For this to occur a pin structure with a thin, heavily doped p^+ region is the most suitable design, however a thick depletion layer means a higher internal device resistance. This higher resistance can negatively impact the solar cell operation of the device and so there is a balance to be made between to two, ideally the depletion region should be much larger than $\frac{1}{\alpha}$, where α is the absorption coefficient. 4H-SiC has a wider band gap than both of the other common polytypes, 6H and 3C [15], which will limit its spectral response but it does have a higher electron mobility which increases the probability of a photon successfully creating an electron hole pair, which then appear at the device terminals.

A pin device creates a large depletion region because the total negative space charge region of the high doped p-side must balance the total positive space charge region in the low doped n-side to maintain the neutrality of this region. Due to the high concentration of N_A compared to N_D, the depletion region in the n type region is large and can be approximated to the same as the n-side space charge region.

The device used in this study is shown schematically in figure 5.2. It has a design which is favourable for operation as a photovoltaic cell. The device comprises of a thin, semi-transparent top metallisation for charge collection, a thin and highly doped p-region and a large, weakly doped n drift region. Although this is not strictly a pin structure it is an abrupt junction with a weakly doped drift region that can be approximated to intrinsic and as such will maximise the length of the depletion region in the device. The doping concentrations for the p and n region were N_A=1x10^{19} cm^{-3} and N_D=3x10^{15} cm^{-3} respectively.

5.3 Dark Properties

Prior to illuminated operation tests it is important to determine how similar the devices are to their initial specification. Typical $\frac{1}{C^2}$-V sweeps for these devices are shown in figure 5.3 as a function of temperature. From this data the device barrier height and bulk carrier concentration can be extracted allowing for a comparison to specification and the physical device [16]. These data were obtained using an Agilent 4284A LCR meter with a DC voltage sweep from -5 V to +5 V with an AC component of 1MHz at 10 mVpp.

Using equations 5.9 and 5.10 it is possible to determine the bulk activated carriers and the depletion region width from the plot of $\frac{1}{C^2}$-V of the room temperature data in figure 5.3. The bulk activated carriers is 2.6x10^{15} cm^{-3} and the depletion region width is 1.18 μm at room temperature and 0V bias. This method for extracting the depletion region only allows us to calculate the length of the portion in the n region, however, as previously stated, the doping concentrations of this device means that this very closely approximates to the length of whole depletion region. The value for N_B is very close to N_D showing that
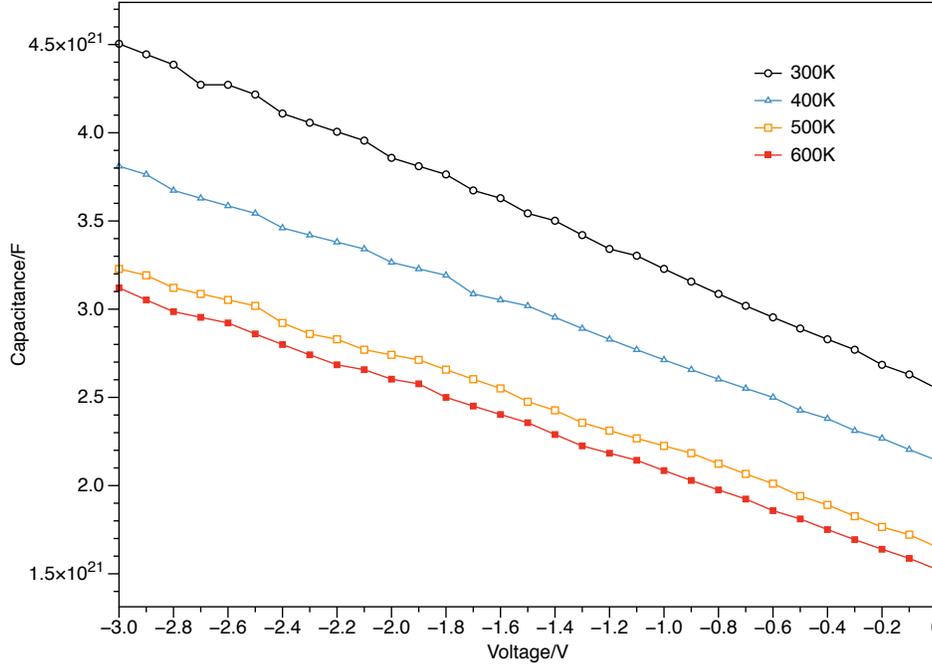
Figure 5.3: $\frac{1}{C^2}$-V sweeps for typical SiC diode at a range of temperatures

the donor impurity concentration is accurate to the intended level of $3\mathrm{x}10^{15}$ cm^{-3}. There is a difference of 13.3% between the intended doping density and the extracted value which could be attributed to either unactivated carriers or processing inaccuracies which can be +/- 25% of the intended value [17].

$$N_B = \frac{2}{q\varepsilon_o\varepsilon_s A^2 \frac{d\left(\frac{1}{C^2}\right)}{dV}} \tag{5.9}$$

$$W \cong x_n = \sqrt{\frac{2\epsilon_s V_{bi}}{qN_B}} \tag{5.10}$$

As previously discussed, the diode's dark properties, such as reverse saturation current, have an important effect on the devices illuminated operation. Dark characterisation of a typical device is presented here which was conducted using a Keithley 6430 Source-Measure Unit controlled with a LabVIEW program to ensure repeatable test conditions. The dark I-V response of a typical silicon device is depicted in figure 5.4 [16] and outlines clearly that
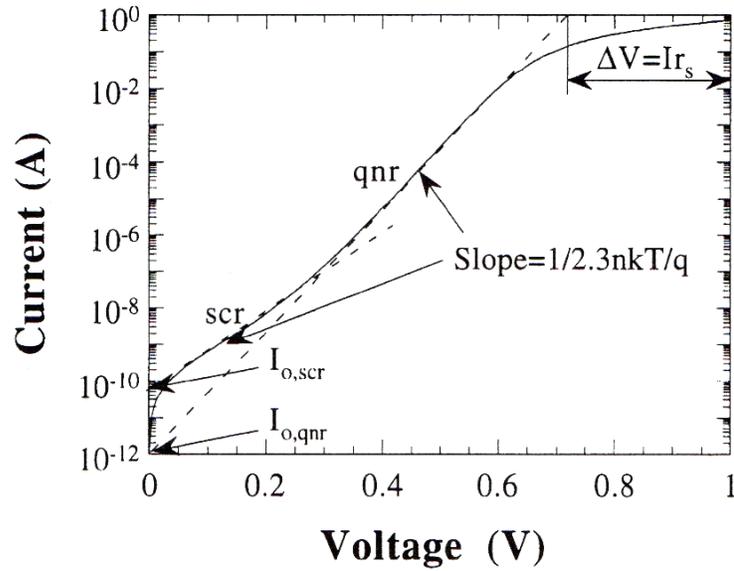
Figure 5.4: I-V sweep analysis for and silicon pn juction [16]

it is possible to extract two reverse saturation currents from the experimental data. For highly accurate current measurements it is possible to see the space charge region current of the I-V characteristic. However, given how small the low bias currents are for silicon carbide devices it is not possible to accurately isolate this region. All presented reverse saturation current values have been found from the y-axis intersect of the linear fit of the quasi neutral region.

Given that the ratio $\frac{I_{ph}}{I_o}$ is very important to solar cell operation, it is useful to understand how temperature effects I_o when the device is not illuminated. The data in figure 5.5 shows that the reverse saturation current increases with temperature but, even at 600K, it is still less than 1 nA for a device 180 μm x 180 μm.

Series resistance is another factor which limits solar cell operation. High series resistance values have a detrimental effect on the illumination curve of a solar cell. The larger the series resistance then the smaller the diode current has to be for it to start having an effect on the photo generated current. This is represented by the data in figure 5.6 and shows how series resistance affects the illumination curve of the diode.

The series resistance of a device is dependant on a number of factors including the bulk
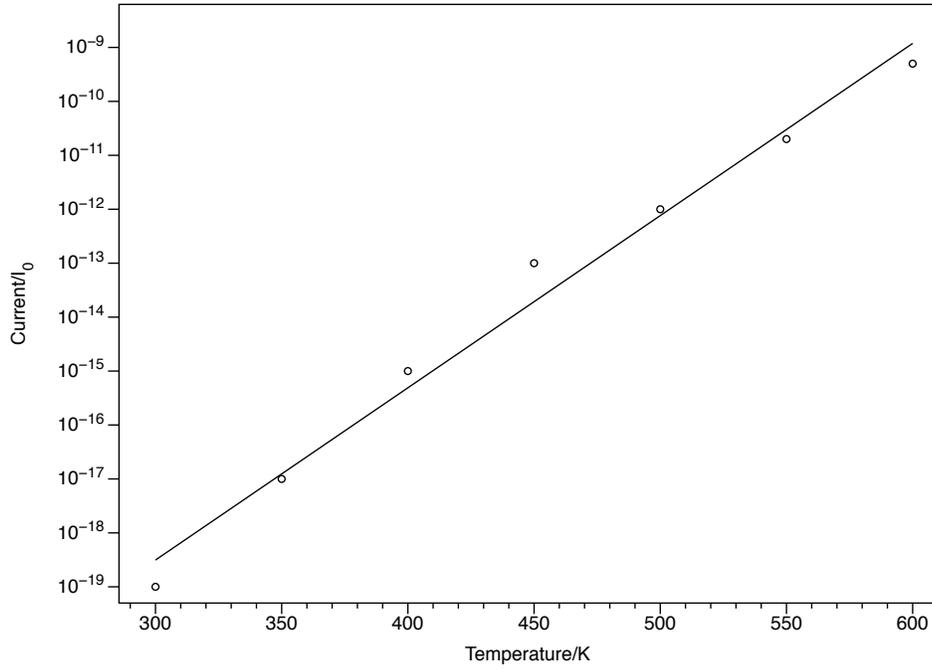
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Figure 5.5: Typical reverse saturation current variation with temperature

semiconductor, contact metallisation and even packaging connections. The series resistance of a device can be factored in to the diode equation with an addition of an IR_s term, as shown in equation 5.11. I_{sc} and V_{oc} do not change with series resistance, as shown in figure 5.6, because at I_{sc} the voltage, and therefore the resistance, is 0; the inverse is true for V_{oc} [16].

$$I = I_o \left(exp \left(\frac{q(V - IR_s)}{nk_BT} \right) - 1 \right) \tag{5.11}$$

The ideal diode equation does not have this term in as it is an Ohmic limit on the how much current a physical device can pass. At very low current levels the voltage loss due to the parasitic resistance is very low, so the diode still exhibits an exponential increase in current proportional to voltage. As the current increases it is limited by the Ohmic resistance and so the increase in current proportional to voltage becomes linear. The data in figure 5.7 shows how the resistance for a typical SiC diode changes with temperature indicating that for this temperature range the resistance decreases with temperature.
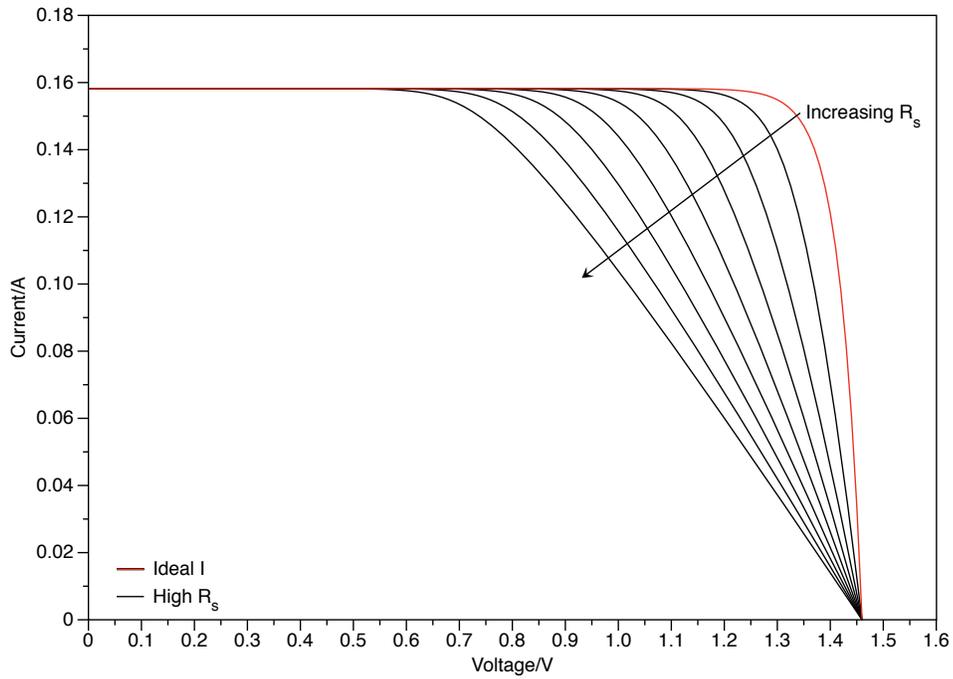
Figure 5.6: Representation of effect increased series resistance on ideal illumination curve

When conductive material is heated there is an increase in resistance due to phonon scattering, this is where the kinetic energy of the material lattice increases and reduces the carrier mobility [18]. However, in semiconductor materials there is also an increase in the intrinsic carrier concentration caused by thermally generated carriers which reduces the materials resistance. The effect these have on the material conductivity are shown in equation 5.12.

$$\sigma = \frac{1}{\rho} = q(\mu_n n + \mu_p p) \tag{5.12}$$

Where σ is the conductivity, ρ the materials resistivity, μ_n and μ_p the minority carrier mobilities and n and p the carrier concentrations.

These two mechanisms, mobility and carrier concentration, dominate the series resistance in different temperature ranges. The increase in carrier concentration initially decreases the series resistance, as shown in figure 5.7, however at higher temperatures the decrease in carrier mobility is the dominant effect [19] and so the resistance should increase at around
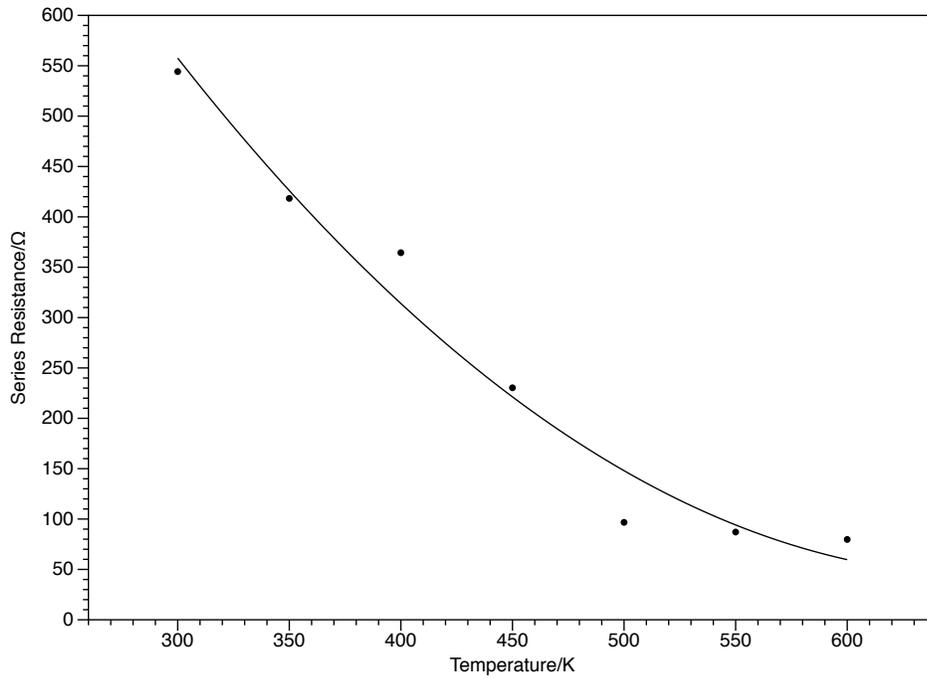
Figure 5.7: Variation in series resistance with temperature extracted from device IV sweep and method detailled in Schroder [16]

450 K. This clearly does not happen with this device which could be due to the very high series resistance compared to other SiC devices in the literature [16, 20]; this is likely due to the large, low doped drift region. Given that silicon carbide has a higher resistivity, higher barrier height and lower reverse saturation current than silicon this increased series resistance is not a big a problem on solar cell operation, as will be shown in the next section.

5.4 Illumination results

As already stated, silicon carbide is blind to the majority of the solar spectrum and testing the device with broad spectrum white light source will not yield useful data. The following illumination data is collected from silicon carbide diodes exposed to light from a XE-175 broad spectrum UV extended light source which is a 5600K-blackbody illuminator designed to mimic the solar spectrum.

This light source has a variable output controlled by a grating which has an increasing number of holes in it toward full exposure. The relationship between the control knob and the intensity of light was non-linear and so to aid repeatability the control knob was set to 0°, 45°, 90°, 135° and 180° which, as shown by table 5.1, relates to 0%, 0.5%, 8%, 18% and 100% of light source intensity. The output current from the calibrated photodetector and the SiC solar cell are shown to vary linearly with the output power, as shown by the data in figure 5.8, and so it is clear that such a set up is reliable for characterising such devices under illumination. The light source data sheet indicates that 5% of the light output has a wavelength less than 300 nm. Assuming that this is the part of the spectrum that the SiC device will respond to the optical power received by the devices can be included in table 5.1. The current response of the photodiode was measured 20 times at each setting across 10 days and the range stated is +1 standard deviation and -1 standard deviation about the mean.

Table 5.1: Intensity as a function of control setting

Control Setting	Photodiode Current (μA)	Optical Power Density (mWcm^{-2}) +/- 10%	Intensity
0°	1.2 - 4.78	0	0%
25°	47 - 78	0.009	0.5%
50°	141 - 167	0.12	8%
75°	225 - 268	0.28	18%
100°	649 - 852	1.6	100%

Figure 5.9 shows how the illumination curve of a typical silicon carbide device changes with illumination power.
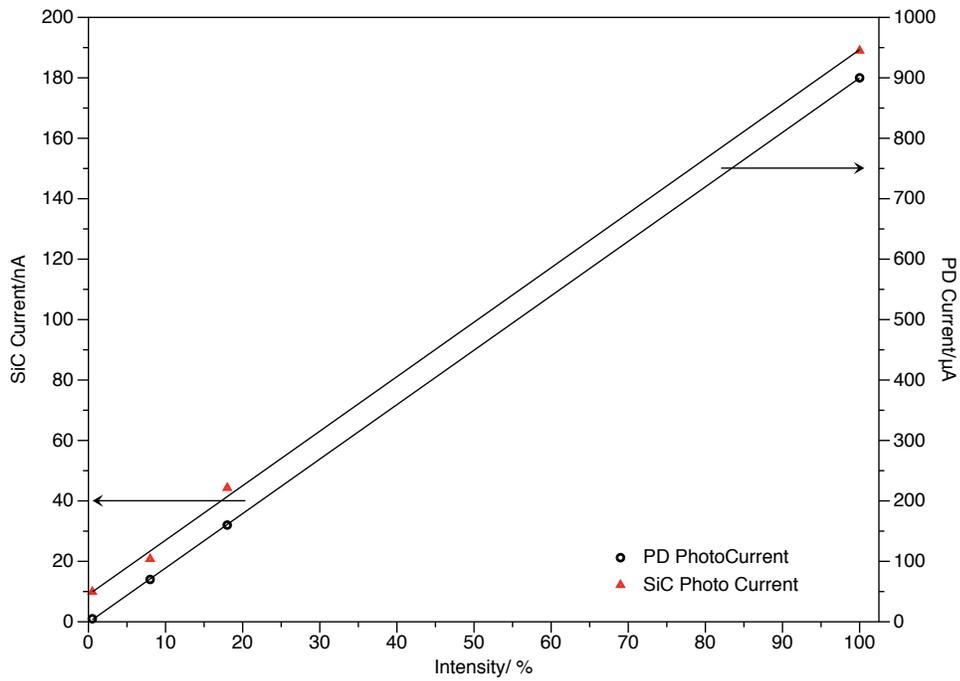
Figure 5.8: Relationship between light intensity and output current from both a calibrated silicon photo detector and a SiC solar cell

The most important data points in figure 5.9 are V_{oc} and I_{sc}, determining how these change with temperature and gives an excellent indication of the devices overall temperature dependance. The V_{oc} is the 0 A x-axis intersect and the I_{sc} is the current at 0V, these are 2.2V and -19 μA at room temperature and 100% illumination respectively. Figure 5.10 shows how V_{oc} and I_{sc} change with temperature for a device exposed to 100% UV illumination. The data clearly shows a increase in magnitude of I_{sc} and a decrease in V_{oc}. The I_{sc} change could be attributed to the increase in diffusion lengths as a direct result of both the carrier lifetime increasing and the diffusion coefficients staying constant or increasing [3]. Although the mobility of the material decreases with temperature the effect of these properties increasing may explain why an overall increase in photocurrent is seen.

Although not stated in the literature as a direct reason, this photocurrent increase could be due to the decrease in the material band gap, E_g. Although the change is minimal, as shown by figure 5.11, any decrease in E_g means that more of the incident photons can be absorbed by the device and used to create electron hole pairs. This was calculated with
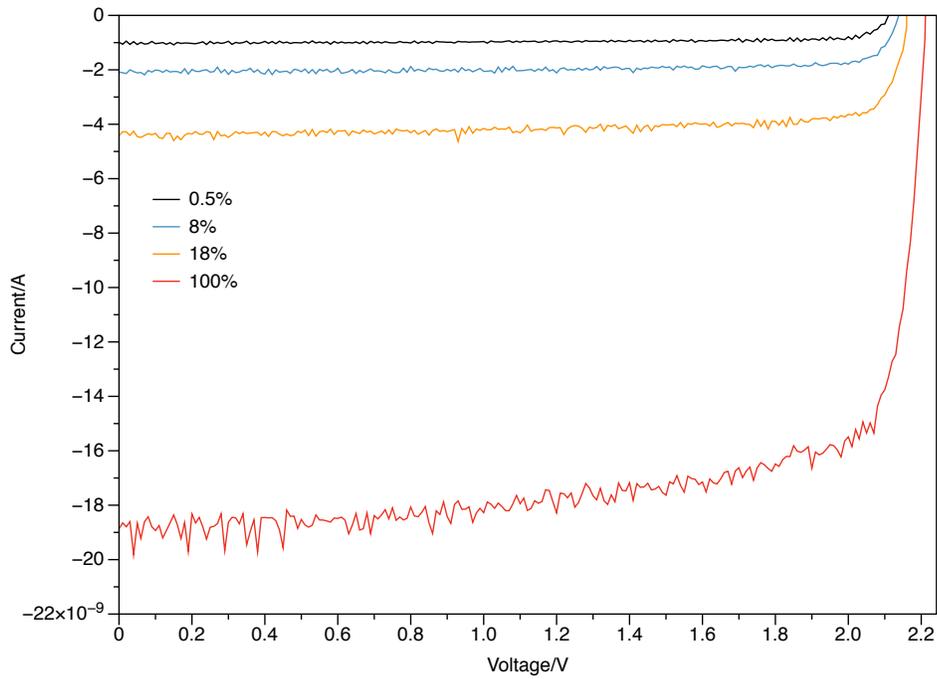
Figure 5.9: Illumination curves for a SiC diode exposed to 4 intensities of UV light

equation 5.13 [5].

$$Eg = Eg(0) - 6.5x10^{-4}x\frac{T^2}{T+1300} \tag{5.13}$$

This is explored further with wavelength absorption tests.

The data in figure 5.9 shows how the device output current changes with load voltage however, this gives little indication as to the optimum operating point of the device. As the power output from energy harvesters is so small it is vital that they are used at, or close to, their maximum operating point where the power transferred from the energy harvester to the load is peak. A typical power curve for these devices, at each illumination intensity, is shown by the date in figure 5.12, this is discussed further in the following section.
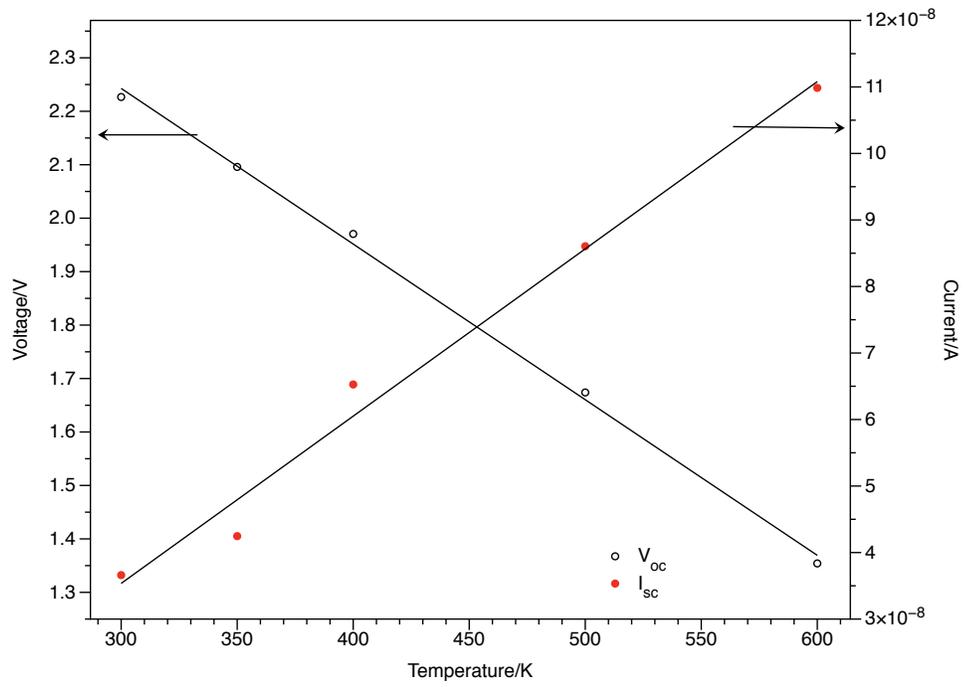
Figure 5.10: Change in V_{oc} and I_{sc} with temperature at 100% illumination
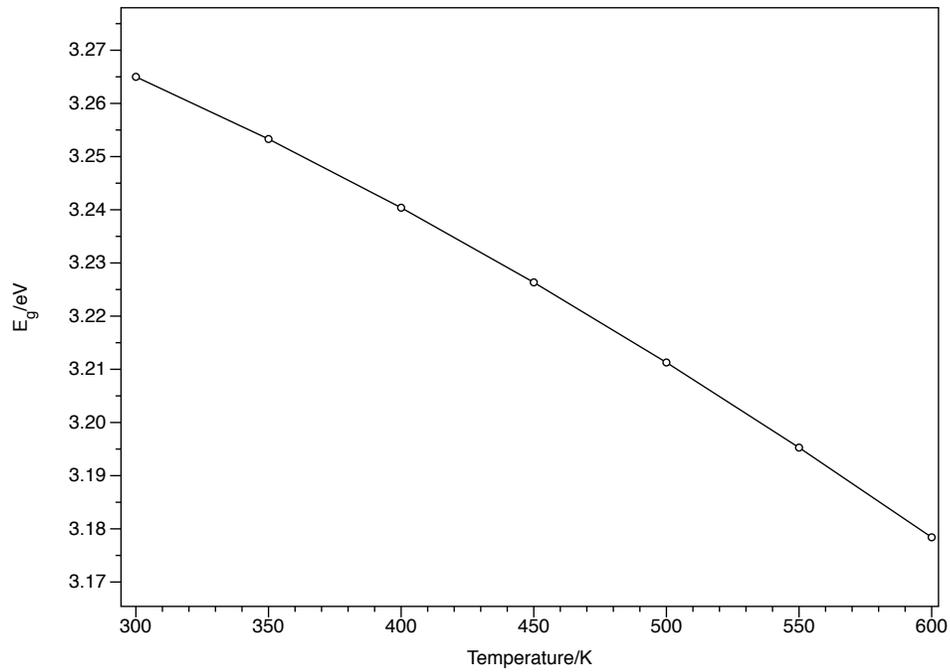

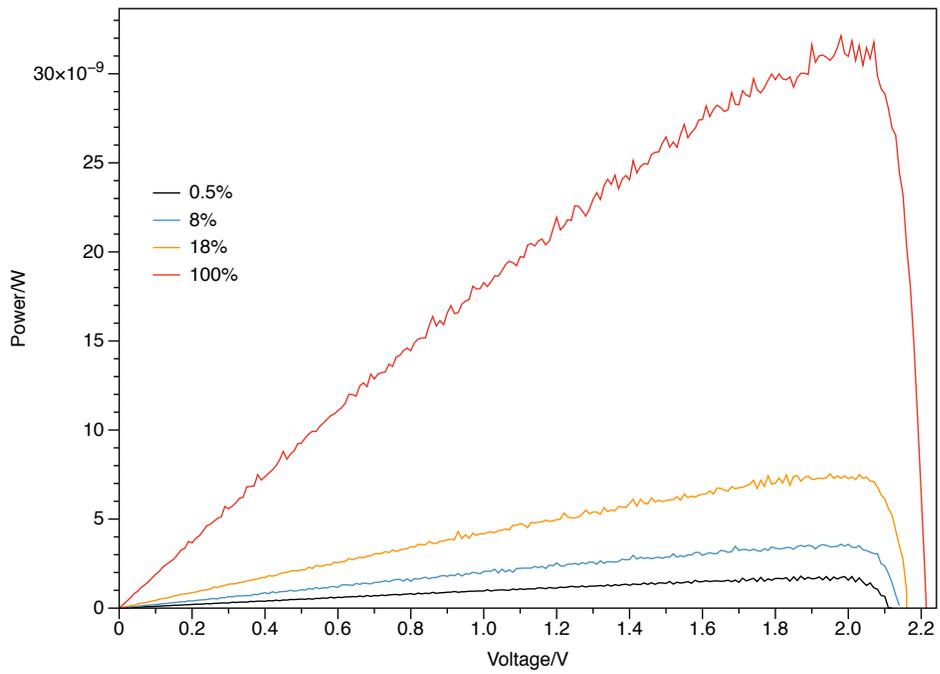Figure 5.11: Calculated temperature induced change in band gap

Figure 5.12: Illuminated power response of pn junction

5.4.1 Maximum Power and Fill Factor

The peak output power from the device characterised in figure 5.12 is 32 nW, given that the area of the device is $0.32\text{x}10^{-3}\text{cm}^{-2}$ and the input UV power is 1.6 mWcm^{-2} +/- 10%, the efficiency of this device can be calculated to be 6.2 %. Compared to modern silicon solar cell this is low, especially given that they are able to harvest energy from the full solar spectrum, however compared to silicon carbide some betavoltaics this is a high efficiency [21].

The I-V and P-V characteristics of the device can be used to determine a number of factors about the photovoltaic response of the device. Figure 5.13 highlights the key parameters where P_{max} is the maximum output power, I_{max} and V_{max} the current and voltage at which P_{max} occurs. Although I_{sc} and V_{oc} are the peak output current and voltage, simply multiplying these together does not equal the devices peak output power as when one is peak the other is at zero.
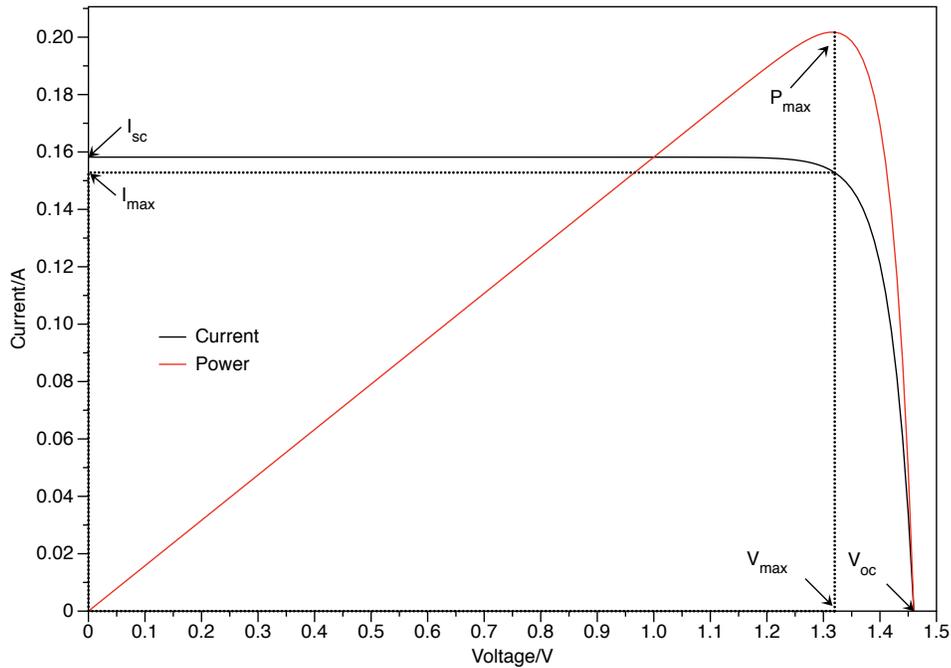

Figure 5.13: Parameter extraction from illuminated device characteristics

This I-V and P-V data enable the extraction of the device fill factor which is the relationship

between V_{oc}, I_{sc} and I_m, V_m and is an indicator of how affected the device is by its non-idealities such as series and shunt resistances and ideality factor. A low fill factor indicates that the device is heavily affected by these which adversely affects photovoltaic operation. This does not necessarily mean that the device has a poor quantum efficiency however, as this is a measure of how effectively the device outputs the power generated.

$$FF = \frac{V_{max} * I_{max}}{V_{oc} * I_{sc}} \tag{5.14}$$

The data in figure 5.12 shows that the output power is proportional to the intensity of light, as would be expected. Of more interest is the data in figure 5.14, as it shows how the peak power, of a typical device at 100% illumination, changes with temperature. It is interesting to note that although V_{oc} decreases with temperature the output power does not. This is because the increase in I_{sc} magnitude is greater than the decrease in V_{oc} and so the output power increases with temperature up to 500 K at which point it decreases again.
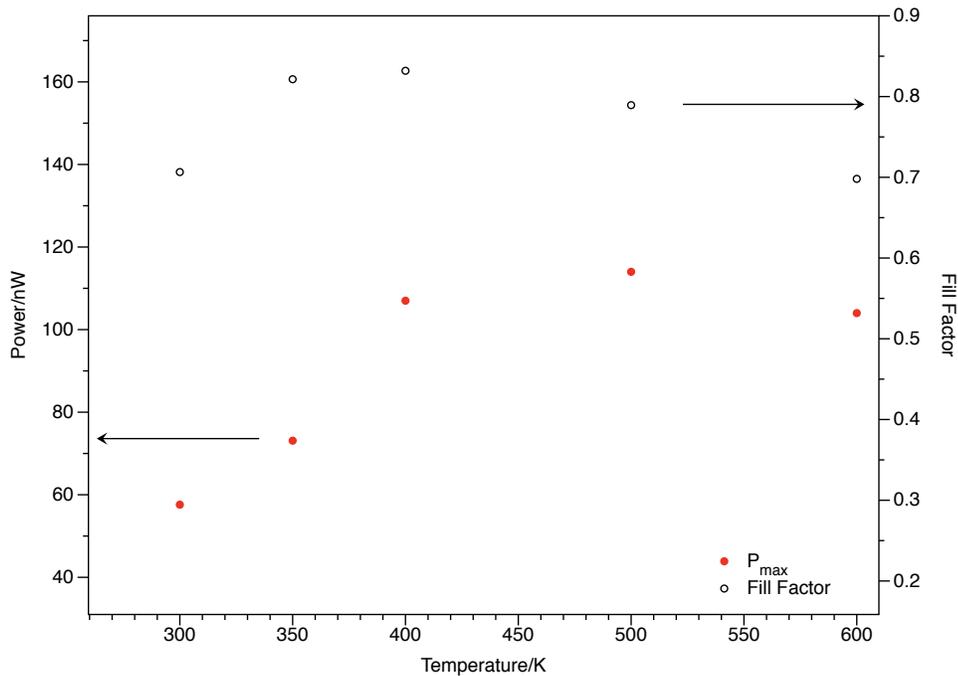

Figure 5.14: Power and Fill Factor variation with temperature for typical SiC pin device exposed to 100% UV illumination

The increase in power shown by the data in figure 5.14 is likely to be due to the observed

decrease in the devices series resistance. The data in figure 5.14 also shows the fill factor variation with temperature. This shows that the fill factor increases with temperature from 300 K to 400 K and then decreases back to the room temperature value by 600K. This supports the hypothesis that the power increases with temperature because the device is less effected by series resistance.

5.5   PV Array

To overcome the technological limitations to silicon carbide large area devices it is possible to connect serval devices in parallel to generate a larger short circuit current.

To facilitate this, a silicon carbide photovoltaic array was made from 8 individual diodes wire bonded, in parallel, into a 40 pin high temperature DIL package. The devices all showed a good photovoltaic response at room temperature with short circuit currents orders of magnitude larger than the dark reverse leakage currents. Figure 5.15 shows their individual illumination curves and the overall response of the array at room temperature.
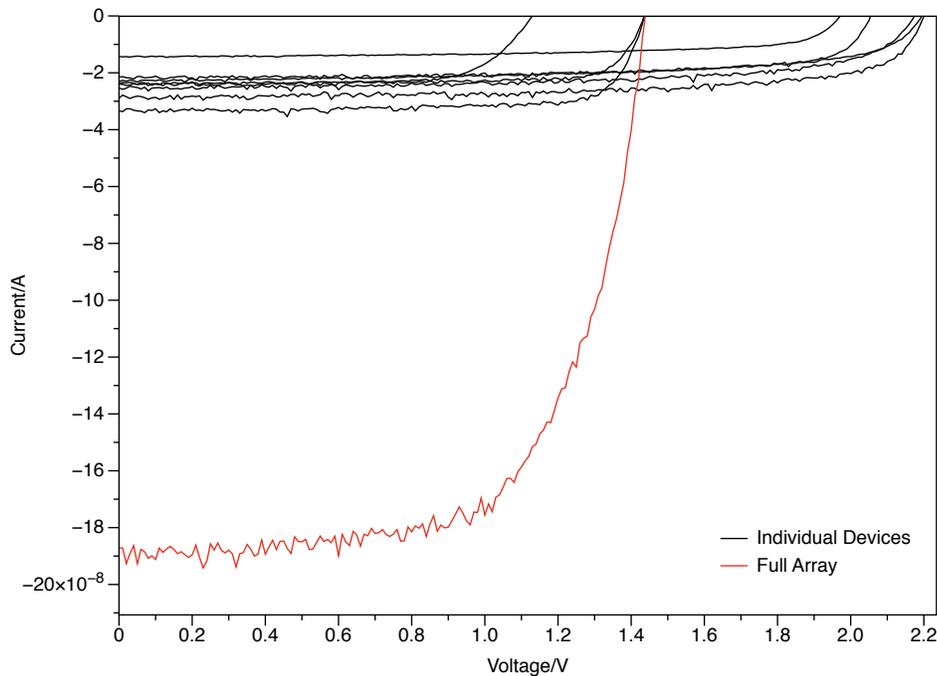

Figure 5.15: Illumination curves for individual devices and the full array

Figure 5.15 clearly shows that by connecting the individual diodes into a parallel array the short circuit current, $I_{sc-array}$, is increased significantly over an individual device and the open circuit voltage, $V_{oc-array}$, is reduced to 1.43V, in between that of the individual devices.

As previously discussed, equation 5.5 shows that the open circuit voltage is the bias at which the internal currents cancel out to produce zero net current. It is reasonable, therefore, that when the devices are connected into a parallel configuration the over all open circuit voltage will be at a bias where the forward currents of the 'on' devices cancel out the reverse currents of the 'off' devices. In this instance the definition of an 'on' device is one in which the forward bias current exceeds the reverse photovoltaic current and as such has a net positive current flow. In this case $V_{oc-array}$ is found to be 1.43V, determined from an IV sweep carried out on the full array.
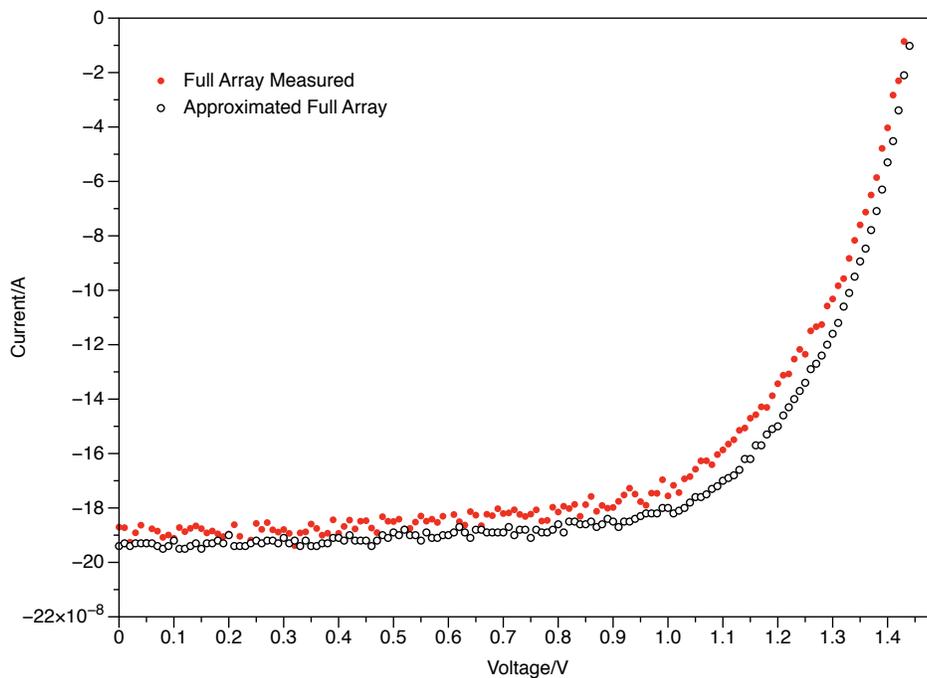

Figure 5.16: Calculated and extracted illumination curve for the full array

As V_{oc} is the bias at which the forward and reverse currents cancel, $V_{oc-array}$ can be accurately determined from the individual IV sweeps of illuminated devices. By summing the currents for each device and plotting the total against voltage, the data depicted in figure

5.16 is produced. It is clear that an accurate $I_{sc-array}$ and $V_{oc-array}$ can be predicted from this calculated curve, and therefore indicates that an optimised array configuration can be determined prior to packaging. The difference between the two illumination curves shown in figure 5.16 is likely caused by experimental variation between the individual device tests and the array test.

5.6 Spectral Response

The data in figure 5.11 shows how the band gap of silicon carbide decreases with temperature, this will in turn decrease the barrier height of a pn junction and so reduce the energy required for an electron to be elevated into conduction. To investigate the effects that this phenomena has on the photovoltaic response an Acton SP2150 monochromator was used to filter the output from the broad spectrum UV source into a monochromatic light source that could be swept across a range of wavelengths. This device allows for a continuous sweep through the spectral range. Figure 5.17 shows how the cut off wavelength from this sweep changes with temperature. As the wavelength approaches cut off there is a linear decrease in output current from the device and, as will be discussed, this can be extended and the 0 A, x-axis intersect is the cut off wavelength.

The data in figure 5.17 was obtained by continually measuring and logging the short circuit current of a pin device whilst the output wavelength of the monochromatic light source was swept from 200 nm to 500 nm. A fit was applied to the decreasing response and its intersection with the x-axis taken as the cut off wavelength. It is clear from the data in figure 5.17 that the cut off wavelength increases with temperature, as would be expected given the band gap narrowing shown by the theoretical data presented in figure 5.11.

Plotting wavelength against band gap produces the data in figure 5.18 which shows a clear relationship between the band gap and the cut off wavelength, the linear decrease in this data shows that they are interlinked and that as the temperature is increased less energy is required to release an electron from the valence band into the conduction band as the gap
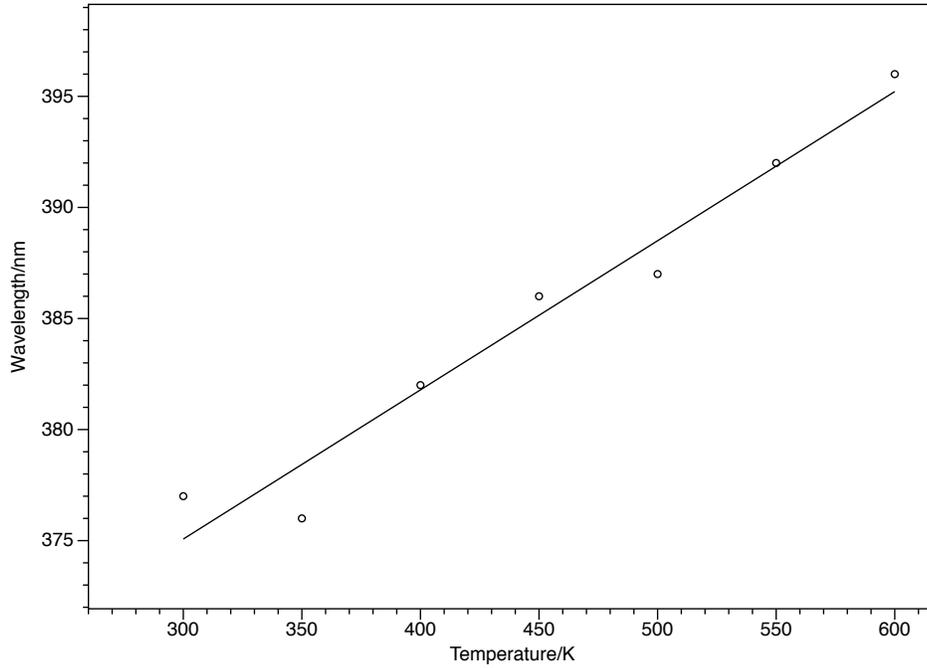
Figure 5.17: Change in cut off wavelength for a typical SiC device as a function of temperature

is reducing.

This experimentally extracted change in band gap, done using equation 5.6 and the data presented in 5.17, represents a 5.5% change in band gap. Given the experimental error of the data, this is comparable to the theoretical decrease of 2.6% represented in figure 5.11. This does however show that the primary driver in both the change in I_{sc} and V_{oc} is not the variation in band gap as the change in these are 168% and 40% respectively. Taking equation 5.5 into account, it is clear that the dominant driver behind the change in V_{oc} is the $\frac{I_{ph}}{I_o}$ ratio. The $\frac{I_{ph}}{I_o}$ change with temperature so far indicates that the V_{oc} will change by approximately 46%, this is similar to the experimentally determined change in V_{oc} which is 40%. This shows that the device is not only operating as expected but that the theory developed with silicon based electronics is also applicable to silicon carbide.
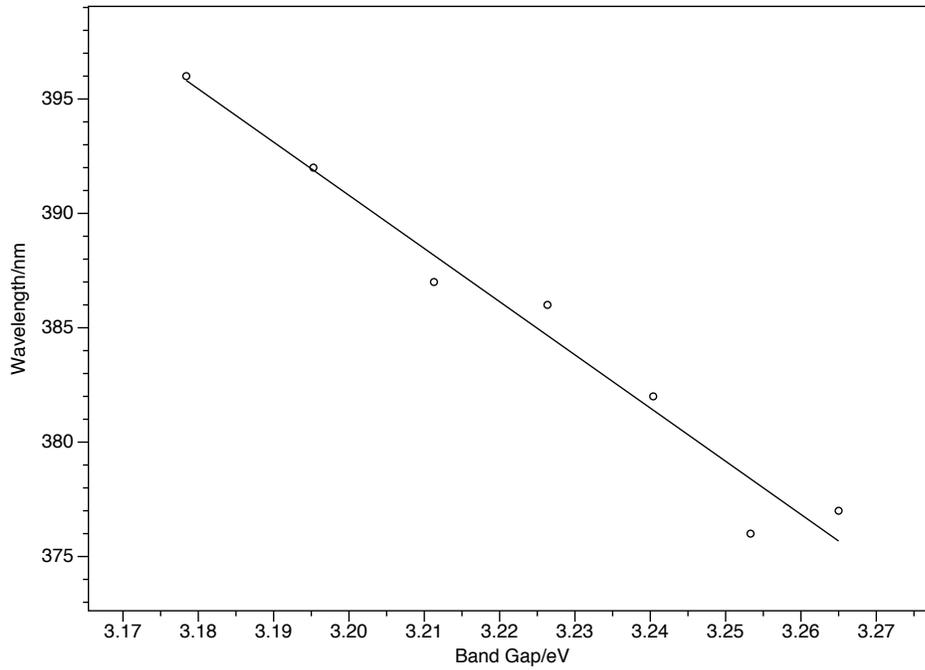
Figure 5.18: Relationship between cut off wavelength and band gap

5.7   Stress Testing

High temperature environments are one of the target deployment environments for silicon carbide systems and as such understanding how high temperatures affect SiC devices over a long period of time is key to developing reliable systems. Although it is well established that long term exposure to temperatures below $500°C$ [22] have little effect on silicon carbide, the effects of long term exposure on the device metallisation is somewhat less explored.

To explore how long term temperature exposure effects the photovoltaic characteristics of silicon carbide a number of devices were stressed at $450°$ for 700 hours in a furnace. At various points during the test the devices were removed from the furnace and characterised as a solar cell and then compared to their pre test results. With long term testing such as this it is important to determine if any change in device performance are real or a systematic error caused by the length of the test. To help determine if any changes are significant each device was tested on 5 different days prior to being placed in the furnace, from this data the standard deviation was calculated and used to calculate the experimental error on each

point. Although removing the devices from the oven to test introduces an element of thermal cycling, this is unlikely to cause a variation in the devices characteristics and all the data presented thus far for temperature testing has caused the devices to be thermally cycled a considerable number of time.
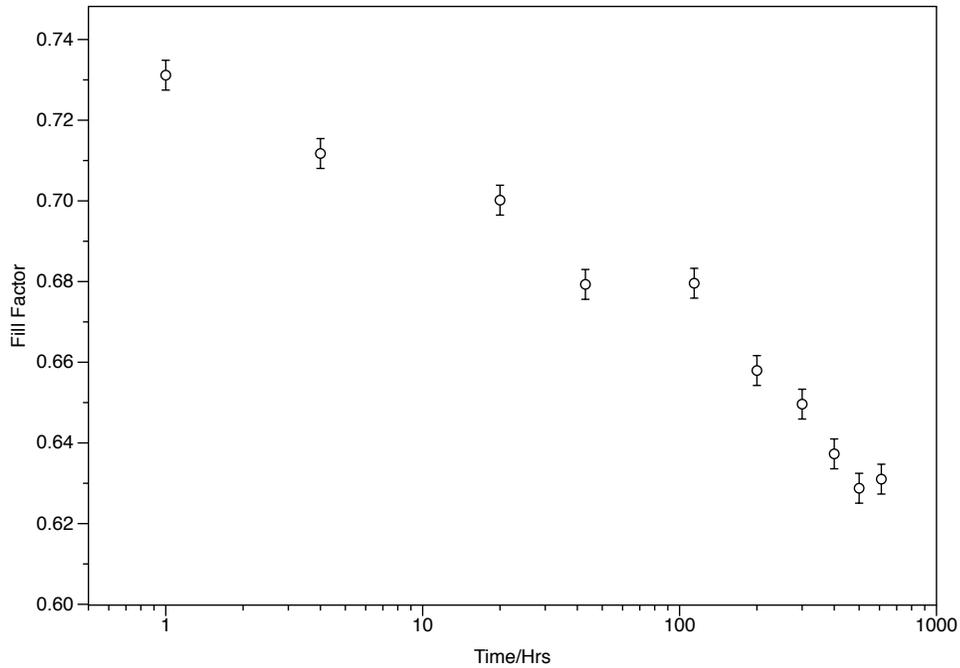
5.7.1 Results

Figure 5.19: Fill factor decrease with stress test at 450°C

The devices were removed from the furnace and characterised at 4, 20, 43, 114, 200, 300, 400, 500, 610 and 700 hours. The final test is not shown in the reported data as the devices failed at this point and were no longer operable as either a diode or solar cell, the cause of this is discussed throughout this section. The only photovoltaic property to change during the stress testing was the fill factor, this was caused by a decrease in I_{max} and V_{mac}. As the data in figure 5.19 shows it decreased during the test. As previously discussed, fill factor is a measure of how affected the device is by its non-idealities so such this change indicates that the device is degrading. This is supported by the data shown in figures 5.21 and 5.20 which show the change in ideality factor and series resistance respectively.
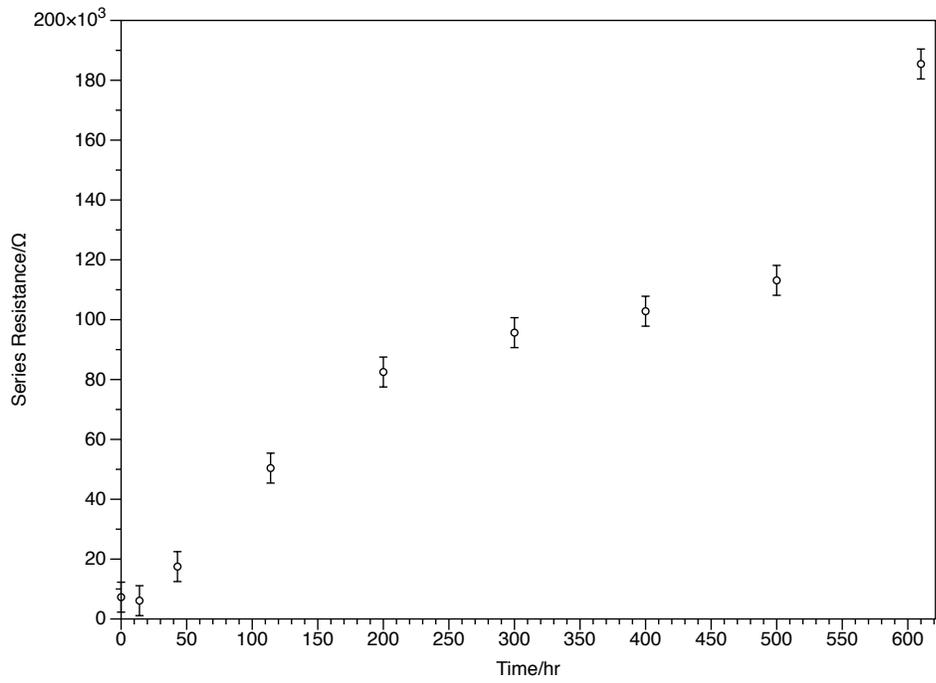
Figure 5.20: Change in series resistance with stress test at 450°C
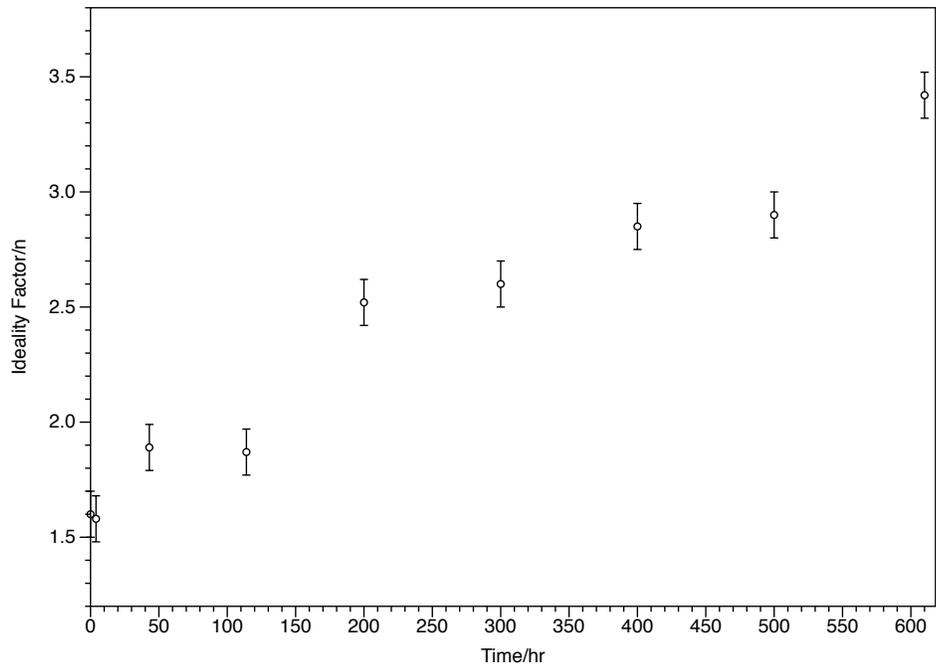

Figure 5.21: Change in ideality factor with stress test at 450°C

The apparent increase in ideality factor is more than likely an artefact of the series resistance increase influencing the I-V characteristic. The ideality factor is extracted from the slope of the quasi neutral region and when the series resistance is very high this region is difficult to isolate accurately as it becomes very small. This is due to the series resistance affecting the current response at much smaller bias than in an unstressed device. With this in mind it is important to realise that ideality factor change indicated by the data in figure 5.21 may not be an accurate representation.

Increase in these properties will have an effect on the fill factor as they have a detrimental effect on the devices performance as a solar cell. Plotting the change in fill factor against series resistance produces the data in figure 5.22, which highlights how interlinked the two properties are. Figure 5.6 showed how series resistance affects the illumination curve so it is clear why fill factor is inversely proportional to series resistance, as fill factor decreases the voltage at which the peak output power is achieved will decrease. For long term deployments of a silicon carbide solar cell maximum power tracking would need to be employed, just as it is for silicon devices, to account for the change in device properties.
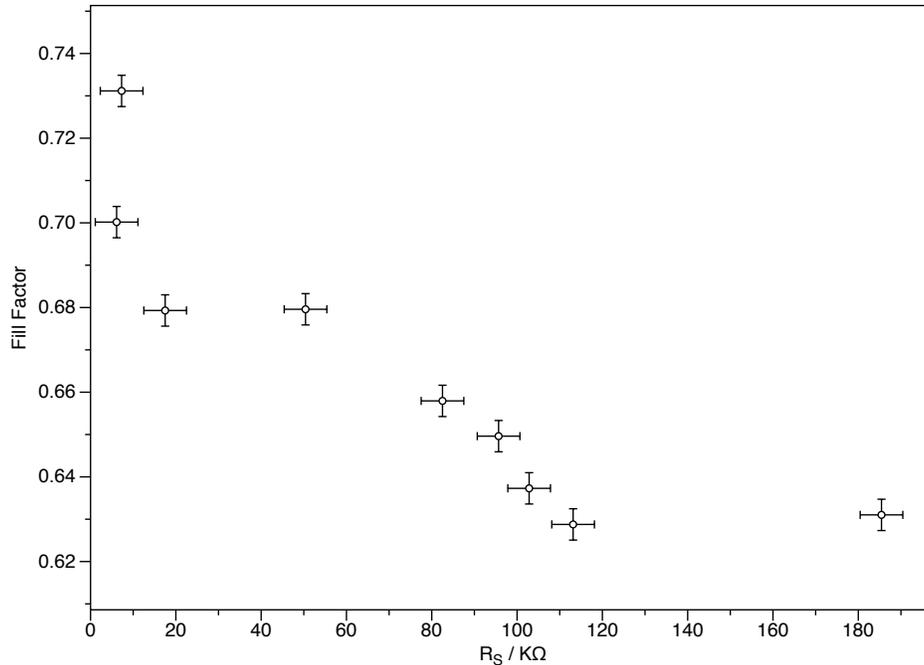

Figure 5.22: Fill factor variation with series resistance

It has been shown in the literature that silicon carbide is unaffected by prolonged exposure to elevated temperatures so it is unlikely that the material is failing [22]. In this case it is important to explore the effects that this test has had on the device metallisation as these are more likely to have failed.

The Scanning Electron Microscope (SEM) images shown in figures 5.23a - 5.23d compare a typical device top contact before and after stressing at 450 °C. Is it clear that the metal has suffered some degradation with small cracks and other visual defects on the surface. As figure 5.2 shows, the top contact is is a Ti/Al/Ti stack with a thick surround of Cr/Au to act as a bonding pad, the Cr/Au pad is the focus of the SEM images.
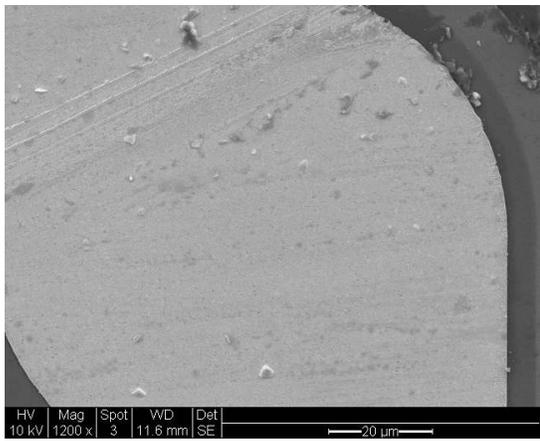
(a) Typical contact before stress test 1200 magnification
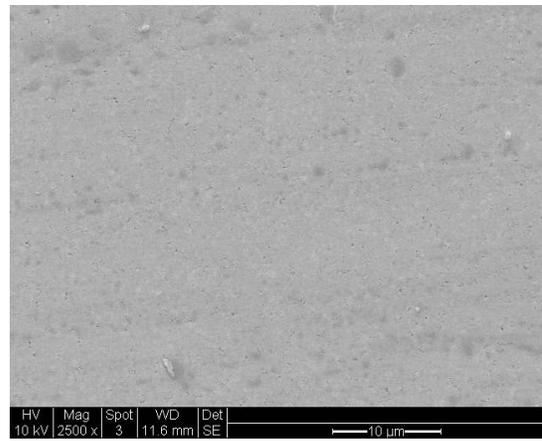
(b) Typical contact before stress test 2500 magnification
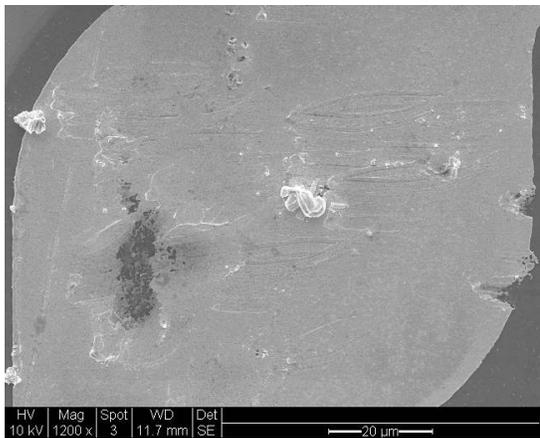
(c) Typical contact after stress test 1200 magnification

(d) Typical contact after stress test 2500 magnification

Figure 5.23: Comparison between thermally stressed and unstressed contacts

Although surrounding the aluminium with titanium is believed to improve its temperature tolerance the temperature and exposure time may have caused the aluminium and titanium to diffuse into the surrounding material. When gold and aluminium come into contact at high temperature an inter metallic is formed which often produces purple, 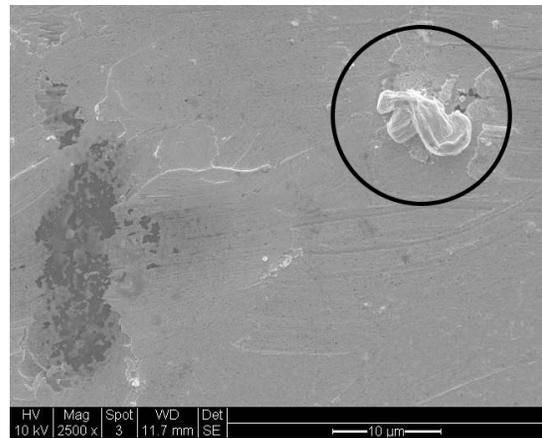shrub like structures which are an indicator of the presence of the AuAl$_2$ compound known as purple plague. This compound leads to an increased series resistance and is mechanically brittle which can make the device difficult to wire bond to. There is evidence of some such structures in figures 5.23c and 5.23d, further evidence of this is supplied by a more detailed material analysis using SIMS. The data for which is shown in figure 5.24.
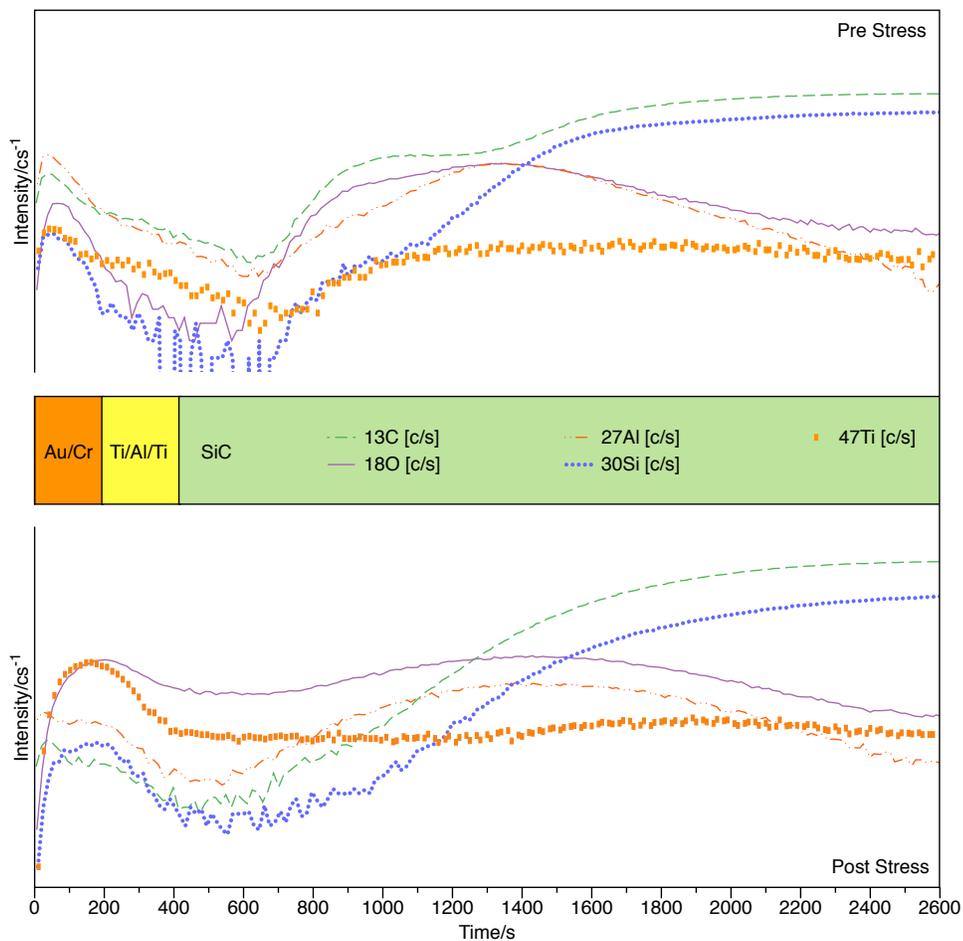

Figure 5.24: SIMS comparison of pre and post stress test device

The Secondary Ion Mass Spectrometry (SIMS) analysis, which provides information about the device elemental composition at different depths, shows not only a broadening of the

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aluminium peak but also a significant increase in oxygen at a shallow depth. This is initially tightly coupled to the titanium peak and indicates that the titanium has oxidised as well as the aluminium. The aluminium peak has broadened indicating that is has indeed diffused into gold layer above it.
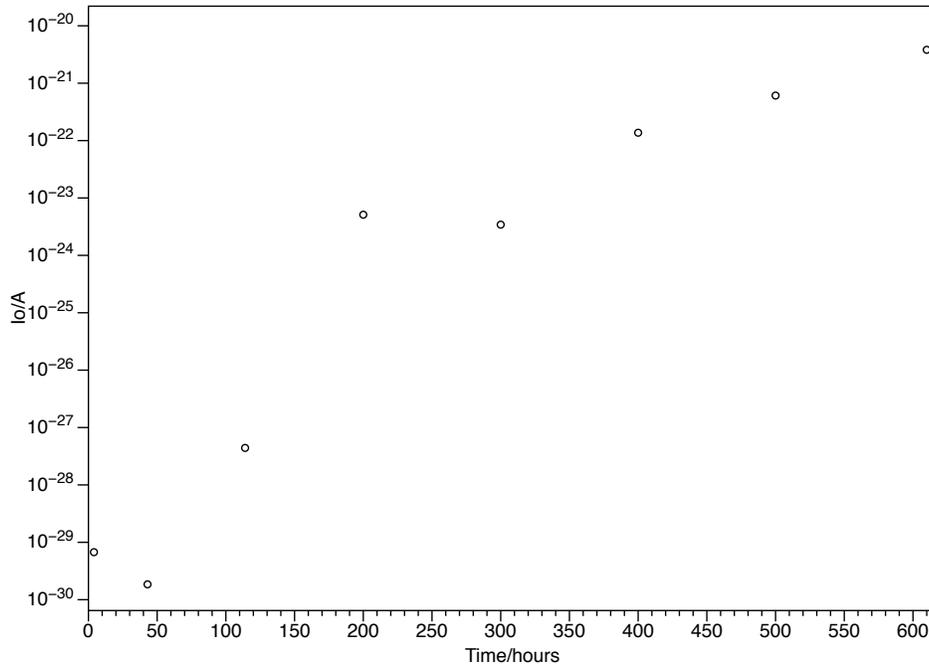
Figure 5.25: Change in reverse saturation current during stress testing

Given the importance of the reverse saturation current on the performance of the device as a solar cell it is worth seeing how this changes as a result of the thermal stress. The data in figure 5.25 shows that there is a significant increase in reverse saturation current and, although significant by 610 hours, it is still smaller than that of an unstressed silicon diode at room temperature. Compared to the series resistance and ideality factor variation the effects of this change are likely to be negligible. There is an anomaly at 210 hours which is most likely caused by variation in where the device was contacted with the test probe. It is important to state however that as the series resistance of the device increases it begins to influence the I-V characteristic at increasingly smaller bias, as this occurs it reduces the size of the quasi neutral region in the I-V data and makes accurate determination of the reverse saturation current increasingly problematic.

5.8 Conclusion

This chapter has shown that silicon carbide is capable of operating as an effective UV energy harvester up to 300°C, exhibiting an increase in power output with temperature and a stable fill factor, indicating that the device is not overly affected by the series resistance or ideality factor. It is shown that the increased temperature decreases the band gap at a rate comparable to theory and that this change has little effect on the power the device is able to harvest.

The devices showed a reasonable level of resilience to long term temperature exposure with catastrophic device failure occurring between 610 and 700 hours at 450°C. The device most likely fails due to a change in the contact stack, whereby the aluminium diffuses into the surrounding material and the titanium, used to stabilise the aluminium, oxidises and increases the contact resistance. This is supported by both experimental I-V characterisation indicating an increase series resistance, from 8 KΩ at the start to 183 KKΩ at 600 hours, and also SIMs analysis showing significant movement of metals in the contact stack. The devices reverse saturation current also increased from 10^{-29} A to 10^{20} A. To improve this the titanium could be removed from the stack and replaced and an alternative diffusion barrier, such as refractory metals like tungsten or tantalum silicide, could be use instead. This is an ongoing area of research and is an issue which has been highlighted by this research.

Overall, silicon carbide can be used as a stable and predictable energy harvester in an extreme UV rich environment. However, the contact metals used would need to be changed for an alternative composition which does not react at elevated temperatures as low as the ones in this study.

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Chapter 6

High Temperature Storage

6.1 Introduction

Previous chapters have explored the temperature response of resilient photovoltaic devices and PZT piezoelectric material. The results have shown that although both are capable of producing power across a wide temperature range, neither can produce the power levels required to operate a sensor node. The harvested energy must, therefore, be temporarily stored and discharged into the dependant circuitry when required, leading to the intermittent operation behaviour discussed in the literature review. To maintain a reasonable system size, this energy storage medium must be integrated into the system and so capable of withstanding the same extreme environment as the rest of the components.

One of the primary causes for device failure at elevated temperatures is the increased leakage current caused by the increased thermal energy of the charge carriers [1]. In some cases, the effect this has on a system or device is not overly detrimental and often means that the system simply runs less efficiently. For devices storing energy however, the increased leakage current can greatly limit the temperature at which they can operate as the little charge stored across the device can very quickly dissipate if the source current is low.

Standard capacitor technology, although limited in energy density potential, can exhibit

good temperature stability depending on the chosen dielectric and technology solution. Figure 6.1 shows the cross section of a parallel capacitor and equations 6.1 and 6.2, where C is the capacitance, V the stored voltage, A the area, w the thickness and ε_0 and ε_r the permittivity of free space and relative permittivity of the dielectric respectively describe how these properties influence the energy that the device is able to store at a given voltage.
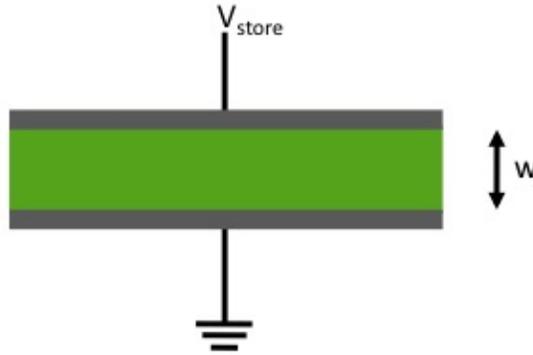

Figure 6.1: Parallel plate capacitor

$$C = \frac{\varepsilon_0 \varepsilon_r A}{w} \tag{6.1}$$

$$E = \frac{1}{2} C V^2 \tag{6.2}$$

It is clear that there are a number of ways in which a high energy storage capacity can be achieved. Ideally the device would be very thin, have a large area, exhibit a high dielectric constant and withstand a high voltage. Realistically however, there are technological limitations on how these properties relate to each other.

This chapter will focus on two potential solutions to obtaining a high energy storage capability at high temperature, the first will be an on chip solution which can be fabricated alongside the SiC components on the same die. The second is a substrate solution which can be integrated with the chip carrier and form part of a hybrid system.

The chapter first introduces the chosen materials and provides a thorough explanation as

to the differences between the proposed techniques and then how they would be deployed in a self powered system. The chapter then outlines the fabrication of the on chip devices and presents I-V and C-V data characterising the devices temperature response and how these changes affect the behaviour of the energy harvesting system. The substrate solution devices are then outlined with the same characterisation and the ramifications for the whole system of the observed behaviour discussed. Finally the issue of scalability is introduced and key issues with each technology highlighted and a solution proposed for a specific system requirement.

6.2 Materials

Ceramic based dielectrics, such as Hafnium Dioxide, HfO_2, and Aluminium Nitride, AlN, have been shown to work at temperatures in excess of 300 °C [2] however reliable fabrication that can be incorporated into complex processes can be difficult due to the constraints imposed. HfO_2 and AlN have shown good temperature stability [3] with extensive research showing that they are able to operate in a at temperatures above 300 °C.

6.2.1 HfO_2

Properties

HfO_2 is a high-k dielectric which has been shown to exhibit excellent resilient properties in a wide range of harsh environments, including those with temperatures in excess of 300 °C [4]. HfO_2 is a so called high-k dielectric as it has a dielectric constant of around 20, five times greater than the 3.9 of silicon dioxide [5]. HfO_2, as well as other high-k dielectrics, has recently received increased research interest as a possible replacement for SiO_2 in highly integrated nano scale systems. In these situations, where MOSFETs have an equivalent oxide thickness of 2 nm, a major contributor to efficiency loss in the transistor is the increased leakage current through these thin gate oxide layers. The use of a high-k dielectric to replace this native oxide will allow for the required gate capacitance without the

limiting leakage currents currently seen [6]. This is because the higher dielectric constant will generate a greater capacitance density that a silicon dioxide film for a given thickness. As such the electric field through the gate oxide is reduced and so a reduced leakage current is observed.

HfO_2 has been shown to withstand higher electric fields and exhibit longer life times than some other high-k dielectrics [7]. As equation 6.1 shows, the high dielectric constant allows devices to be made with a comparable capacitance density to those using SiO_2, but which are much thicker and therefore exhibit a substantially lower leakage current. For example, in the case of Poole-Frenkel emission (a trap mediated conduction mechanism), the leakage current is proportional to the electric field across the device, hence for a given voltage the electric field varies inversely with dielectric thickness and so reducing the leakage current. The trade off to this however is a reduced capacitance density.

HfO_2 can be integrated in to silicon carbide processing and as such devices can be fabricated on the same die as the JFETs and diodes and provide an energy storage solution in very close proximity to where the energy is needed. One drawback to this however is the relatively constrained space on a processed die, this means that device area must be kept small. Hence, the dielectric layer must be thin (less than 100 nm) to increase the capacitance density.

6.2.2 AlN

Properties

AlN is a material with a wide range of applications; its high thermal conductivity makes it an ideal heat dissipater [8], it can be deposited in a Physical Vapour Deposition (PVD) system meaning and be easily incorporated into CMOS fabrication processes [9, 10] and when fabricated under certain conditions it exhibits a highly controllable and detectable piezoelectric response [11]. AlN can be deposited at room temperature in a DC, pulsed-DC or RF PVD system with the resultant film highly dependant on the deposition parameters.

It has a dielectric constant of between 10 and 12, depending on deposition method, and so is greater than that of silicon dioxide but less than HfO_2.

Extensive research has been carried out into controlling the deposition of AlN and the general findings can be summarised using in figure 6.2. This shows how the distance between the target and the substrate and the deposition pressure affect the properties of the resultant film. The {002} orientation occurs at low pressure and short distance as the mean free path for the atoms in the plasma is greater than the distance they have to travel. As a result, the atoms kinetic energy on impact with the substrate is greater, resulting in the high energy {002} crystal structure [11]. It is this structure which is required for a piezoelectric film and allows for the fabrication of SAWs and cantilever MEMS transducers [12]. However, it is difficult to achieve as each PVD system is different and other parameters such as substrate bias, gas concentrations and deposition power play a significant role [13, 11, 14].
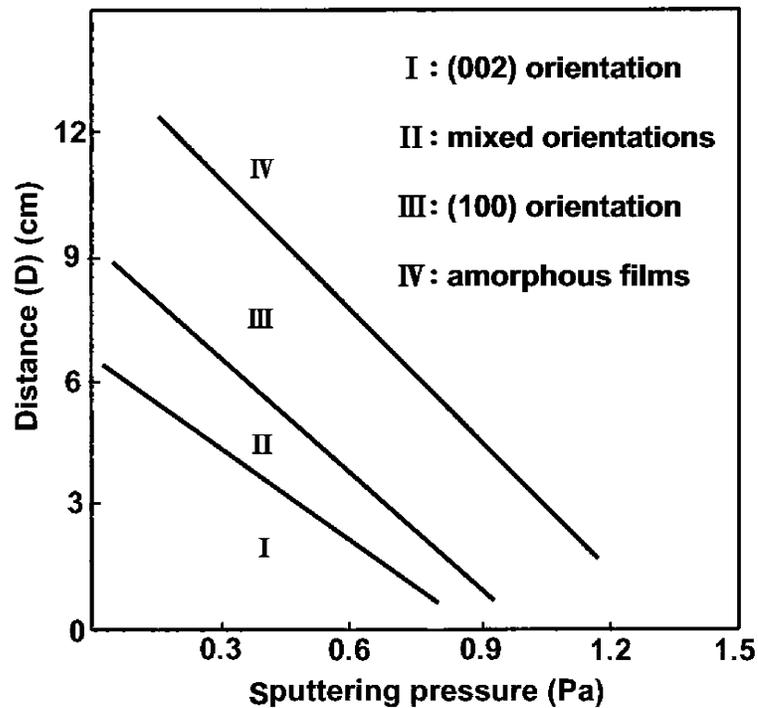

Figure 6.2: Effect of deposition parameters on AlN material [15]

As the distance from the substrate to the target increases, the atoms lose kinetic energy in the plasma and so align in the the energetically favourable {100} orientation and then

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eventually resulting in an amorphous film, which exhibits poor stoichiometry. The properties of the material change considerably across this transition from {002} to amorphous but the most noticeable is the loss of the piezoelectric property. To maintain a reliable charge films fabricated would ideally exhibit a low piezoelectric coefficient and as such exhibit a {100} orientation or be amorphous.

When pressed and sintered into larger tiles AlN makes an ideal high temperature circuit board, operating stably above 300 °C, which is resilient and relatively cheap compared to alternatives such as sapphire. Covering such a tile in a dielectric could lead to thermal expansion rate issues however, by using the same material, albeit in different stoichiometry, for both the circuit board and the dielectric this problem is eased.

The properties of these two materials lend themselves to use as high temperature energy storage mediums. They would be incorporated into a system in different ways with different design considerations and implementation issues to contend with. To this end, the rest of this chapter will focus on comparing the two options; an on chip HfO_2 storage system and a substrate based AlN system.

6.3 On Chip Solution

6.3.1 Why On Chip?

A typical on chip solution is depicted in figure 6.3 and represents the simplest of the two options for system integration and fabrication. The devices can be included into the wider system process flow and then either wire bonded to the relevant system pads or, when silicon carbide processing reaches the required maturity, simply have interconnects running to it.

The close proximity to the devices increases the ease with which hybrid modules incorporating sensor, communications and other devices can be fabricated. This monolithic solution minimises the post fabrication assembly and would speed up manufacturing. It does how-
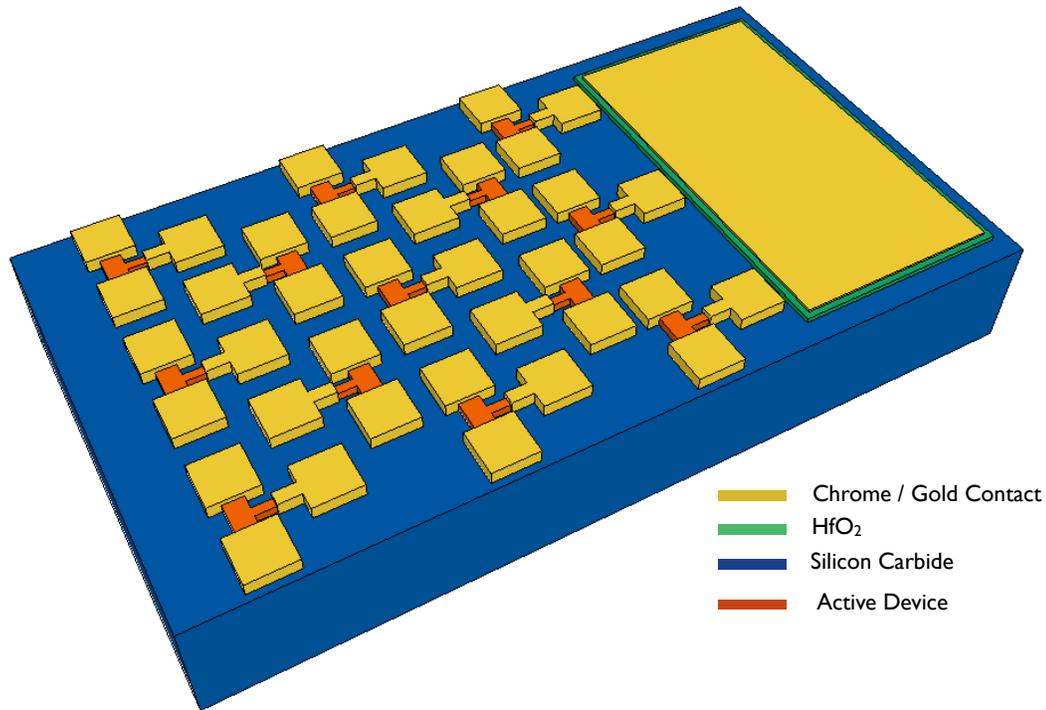
Figure 6.3: Graphical representation of an on chip storage system

ever limit the size of the devices to the processable die size and requires the storage devices to be thin to promote a high capacitance density. The need for high density storage is compounded by the cost of SiC, wafers are still significantly more expensive that silicon ones and as such minimising the size of the required die is beneficial to seeing silicon carbide fully commercialised.

The nature of thin films means that there is a range of leakage mechanisms which can affect the storage potential of the devices and so reduce their storage capabilities. These are further discussed and presented in the results.

6.3.2 Device design

Given the space limitations inherent in this solution, it was decided that small area metal insulator metal (MIM) HfO_2 devices would be fabricated on a semiconductor substrate and investigated for their storage characteristics. Figure 6.4 depicts the mask layout used for

the devices and allows investigation of a range of sizes. Due to the thin nature of the films the probability of defects and pin holes is likely and so producing a range of sizes aids in identifying the optimum size which balances the need for large surface area with the likelihood of a fatal defect. The devices on this mask cover a range of areas and those selected are labelled on figure 6.4, where A has an area of $1.02\text{x}10^{-3}$ cm^2, B $3.14\text{x}10^{-4}$ cm^2, C $6.15\text{x}10^{-4}$ cm^2 and D $0.785\text{x}10^{-4}$ cm^2. These four were selected as they are the closest four in proximity to each other and cover the main area sizes on the mask.
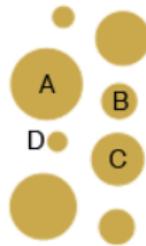

Figure 6.4: Mask design for circular mim capacitors covering a range of areas

To investigate the effects of film thickness the devices were fabricated in two thicknesses of HfO$_2$, 35 nm and 60 nm.

6.3.3 Process Flow

Devices with 35 nm and 60 nm dielectrics were fabricated with the structure shown schematically in figure 6.5.

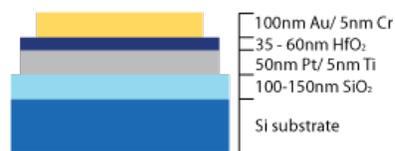Figure 6.5: HfO$_2$ mim capacitor structure

The capacitors were fabricated on a silicon substrate with a thermally grown 100-150nm thick SiO$_2$ isolation layer, as shown in figure 6.6 (a). A Pt layer with a 5nm Ti flash layer was deposited on the SiO$_2$ as a back contact for the devices, figure 6.6 (b). Following this HfO$_2$ films were grown by evaporating a 35nm (or 60nm) Hf metallic layer in an electron-

beam deposition system at 1 x10^{-6} mbar and then oxidising this in an O$_2$ ambient at 500 °C, figure 6.6 (c). Finally, a 100nm Au/5nm Cr top contact was deposited and patterned using photolithography[16], figure 6.6 (e-g). Although silicon is not electrically resilient to high temperatures it is a suitable mechanical substrate material and the temperature induced electrical changes that occur are isolated from the devices by the SiO$_2$ isolation layer.
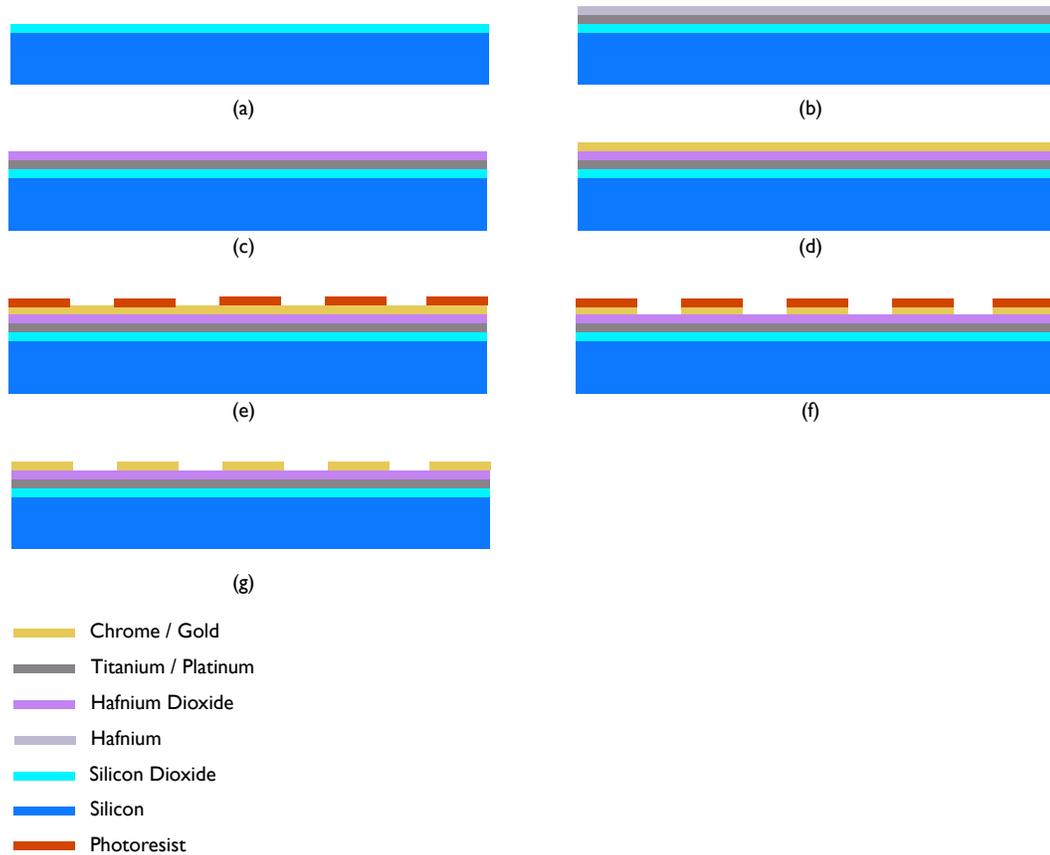

(a)

(b)

(c)

(d)

(e)

(f)

(g)

Chrome / Gold

Titanium / Platinum

Hafnium Dioxide

Hafnium

Silicon Dioxide

Silicon

Photoresist

Figure 6.6: Process flow for HfO$_2$ mim capacitor fabrication

6.3.4 IV Results

The data in figure 6.7 shows the DC leakage through both 35 nm and 60 nm devices at room temperature. These IV sweeps were carried out using a Keithley 4200 source meter. It is clear that the devices exhibit an exponential response with a barrier around 0.7 V, indicating the primary leakage mechanism is driven by the work function difference between the metal

contacts and the dielectric material. Traditionally, leakage current through dielectrics is shown with respect to electric field however, in this instance it is more useful to analyse the data as a function of voltage as it is simpler to correlate the observed response to device operation voltage levels.
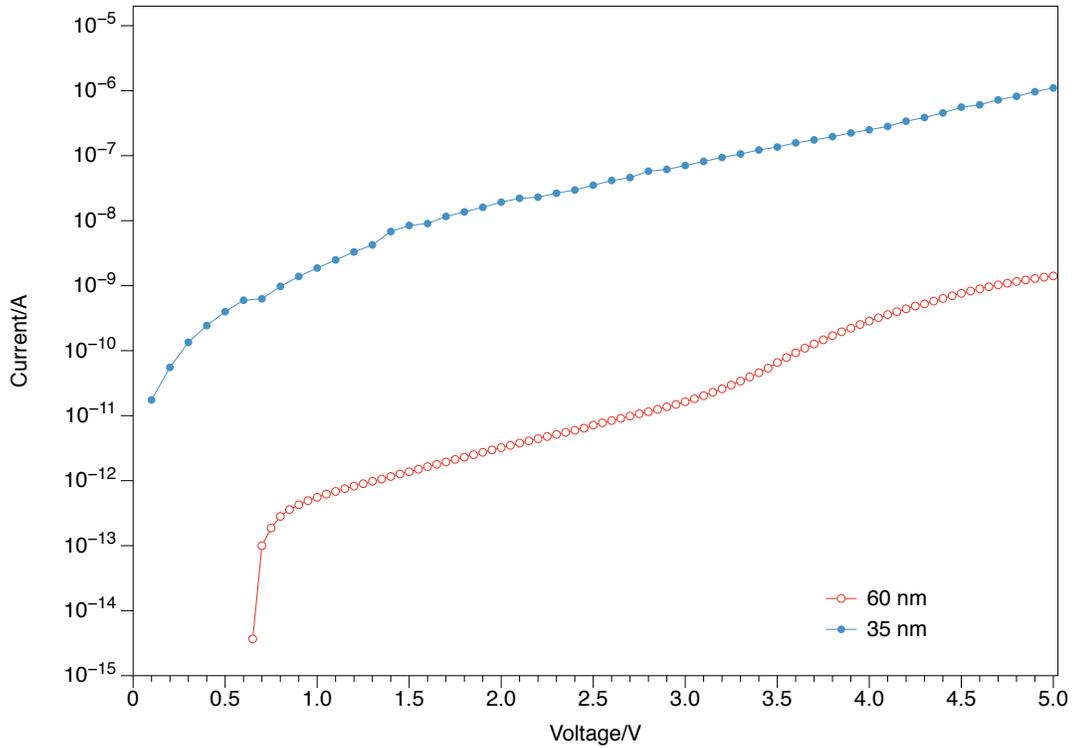

Figure 6.7: Typical IV characteristic of a 60 nm mim capacitor

Given that both Schottky and Poole-Frenkel emission, shown in equations 6.3 [17] and 6.4 [18] respectively, have been shown previously to be drivers of thin film leakage [18, 19] the observed difference between the two data sets in figure 6.7 is likely due to the increased electric field in the 35 nm devices. Equations 6.3 [17] and 6.4 [18] show the same functional form with respect to electric field for both mechanisms, where A^* is the Richardson Constant, ϕ_b the cathode barrier height, E_0 the electric field, σ_0 the conductivity with no external bias, ϕ_t the trap energy barrier, ϵ_0 the permittivity of free space, ϵ_{op} the dynamic high-frequency dielectric constant and J the current density.

$$J = A^* T^2 exp \left[-\frac{q}{kT} \left(\phi_B^0 - \frac{qE_m}{4\pi\varepsilon_0\varepsilon_{op}} \right) \right] \tag{6.3}$$

$$J = \sigma_0 E_0 exp \left[-\frac{q}{KT} \left(\phi_t - \sqrt{\frac{qE_0}{4\pi\varepsilon_0\varepsilon_{op}}} \right) \right] \tag{6.4}$$

Equations 6.3 and 6.4 also highlight that both leakage mechanisms are exponentially dependant on temperature and this is shown by the data in figure 6.8 which, shows a clear exponential increase in current with temperature, up to 500 K.
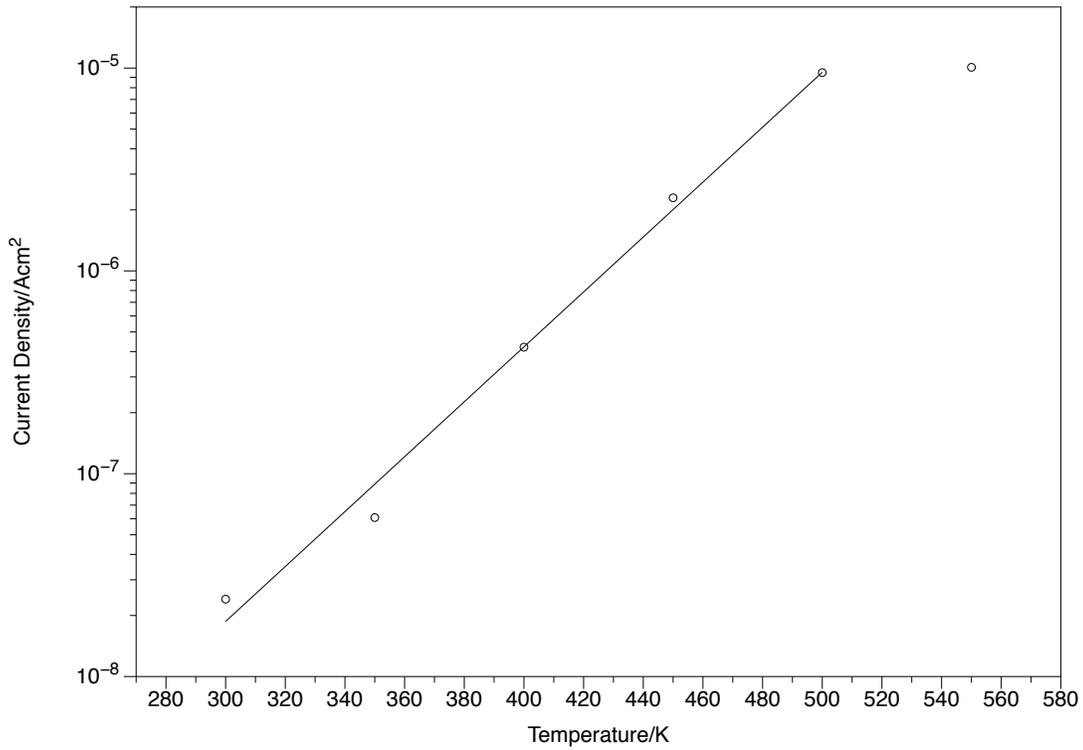

Figure 6.8: DC leakage current at 5 V for 60 nm mim capacitor

The data in figure 6.8 shows that storage ability will be adversely affected by temperature due to the increased dielectric leakage. Given that leakage through the 60 nm film is 10 μA at 573 K and that this is comparable to the outputs of piezoelectric energy harvesters shown in previous chapters, this leakage is too high.

6.3.5 CV Results

Given the increased leakage these devices exhibit at elevated temperatures it is important to investigate changes in capacitance. The CV characteristics as a function of temperature were measured using an Agilent 4284A LCR bridge, to identify capacitors with low temperature and voltage coefficients. A low temperature coefficient is important to provide consistent storage across a wide temperature range. If the capacitance were to change considerably at elevated temperature, this could cause the capacitors to dissipate their stored energy, independent of the leakage mechanisms discussed so far, resulting in a loss of power to the dependant electronics. The results of this testing are shown in figure 6.9 and demonstrate clearly that across a 250K temperature range both capacitors show a low voltage coefficient of capacitance. The exception to this can be seen with the 35nm device at 573K, this increase in capacitance is caused by the increased leakage current through the dielectric.
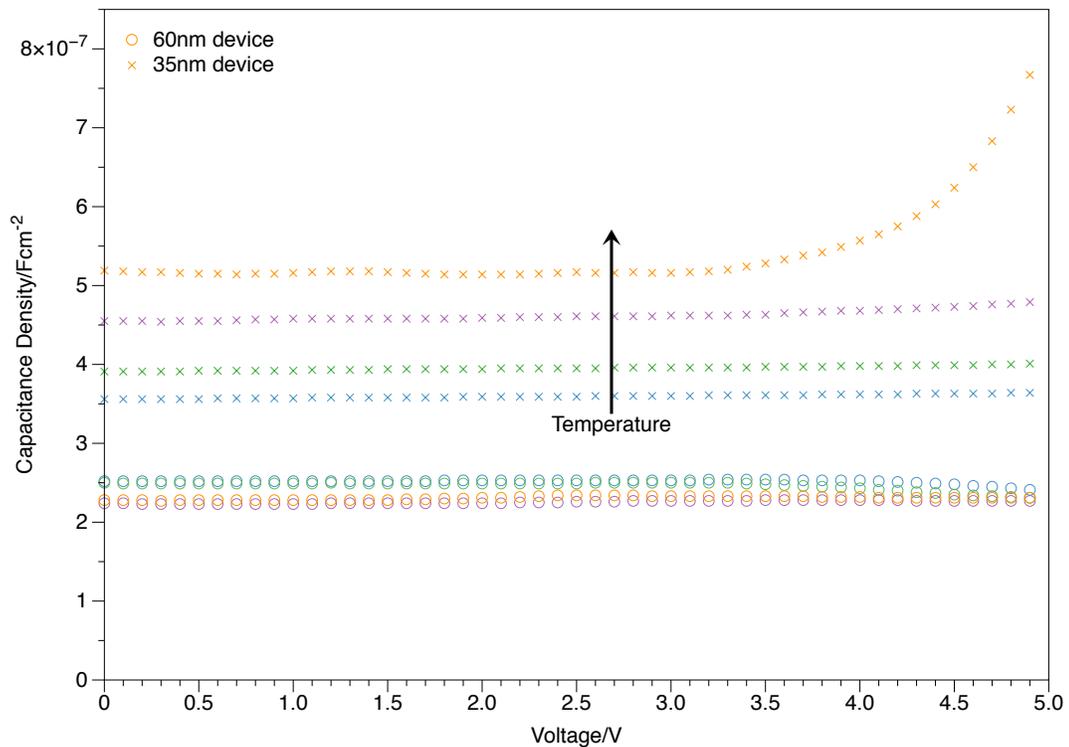

Figure 6.9: 35 nm and 60 nm CV comparison

According to equation 6.5, the capacitance density falls as the reciprocal of dielectric thick-

ness. However, the 60nm device is 1.71 times thicker, but only has a capacitance density 1.43 times smaller than the 35nm device at 300K. In this case there is a 16.4% discrepancy between the expected capacitance densities and the those measured experimentally.

$$C_{density} = \frac{\epsilon_o \epsilon_r}{t} \tag{6.5}$$

Equation 6.5 was used to extract the relative dielectric constant at 300K, these were found to be 17.21 and 14.17 for the 60nm and 35nm dielectrics respectively. This apparent difference is likely due to an accumulation of charge at the cathode, leading to electrode polarisation and therefore a capacitance measurement that is not directly proportional to the dielectric thickness [20].

The data in figure 6.10 shows how the measured capacitance at 0 V for each sized capacitor varies with area. The relationship is found to be linear and varying in accordance with equation 6.1 and shows that the device capacitance is dominated by the surface of the electrodes and not fringing effects.

6.3.6 Summary

A strong variation with temperature was observed in the HfO_2 devices tested, with leakage current increasing exponentially from 22.5 nA at room temperature to 9.86 μA at 550K. This change indicates that although the the 60 nm devices exhibit a low temperature capacitance coefficient they would still be unsuitable individually for high temperature storage. This large increase with temperature is caused by the increase in Poole-Frenkel emission which has been identified as the primary driver of HfO_2 MIM capacitor leakage.
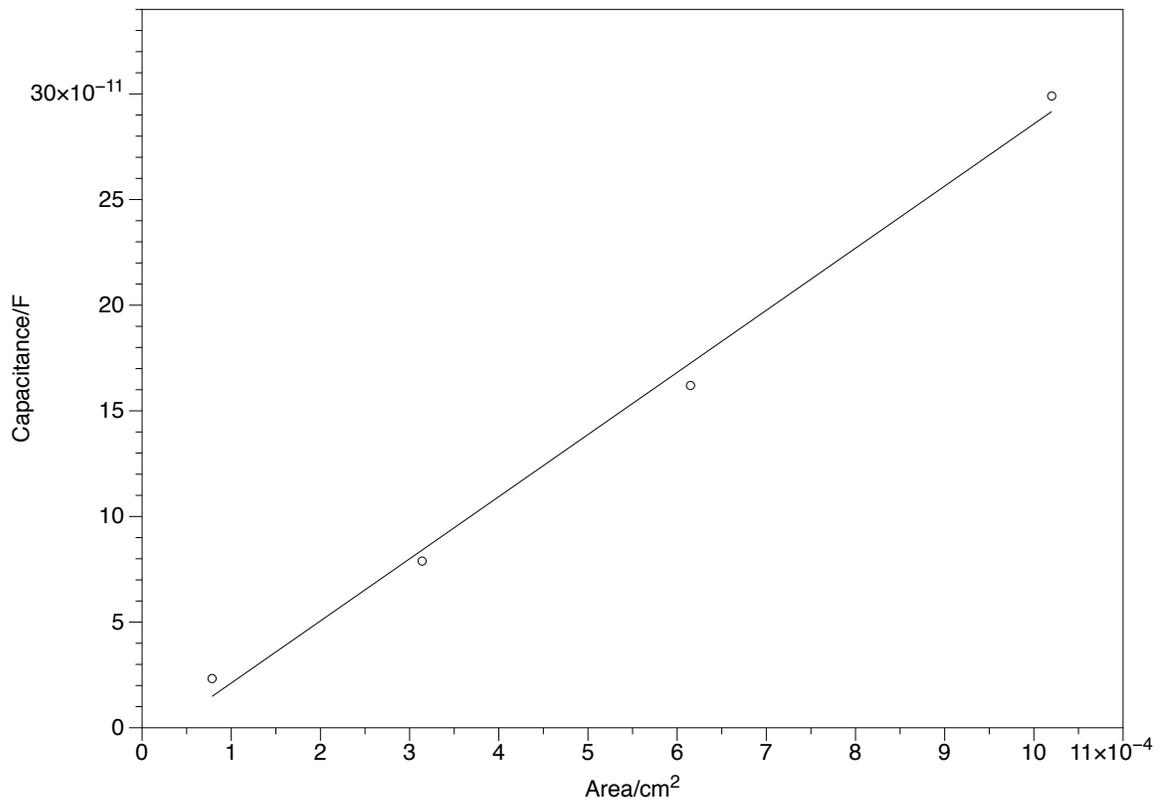
Figure 6.10: HfO$_2$ 60 nm capacitance variation with respect to device area showing a linear dependance

6.4 Substrate Solution

6.4.1 Why Substrate?

Although silicon carbide devices are stable, reproducible and can operate up to 600 °C, supporting technologies such as device packaging are still problematic. One of the most common solutions is to mount discrete devices on a ceramic carrier, such as a small sapphire or larger sintered AlN tile and produce a hybrid module. This enables system designers to reproduce a PCB like system with resilient materials. For instance, rather than copper tracks, gold is used. This does however mean that there are large areas in between components that go largely unused and could be put to better use, especially in the case of the larger AlN tile as seen in [21]. These large unused areas found on such boards can be reduced with

more efficient circuit design however there will always be many orders of magnitude more space available for use as storage, in comparison to the space available with an on chip solution.

In this case, using AlN as the dielectric layer in a storage device is ideal. Figure 6.11 shows how a PVD sputtered AlN layer could be incorporated into a hybrid system at the carrier level and provide energy storage across a large area. Using the large area means that devices do not have to be as thin in order to realise a given capacitance and can therefore be designed to be have a lower leakage current and potentially exhibit more reliable high temperature operation.
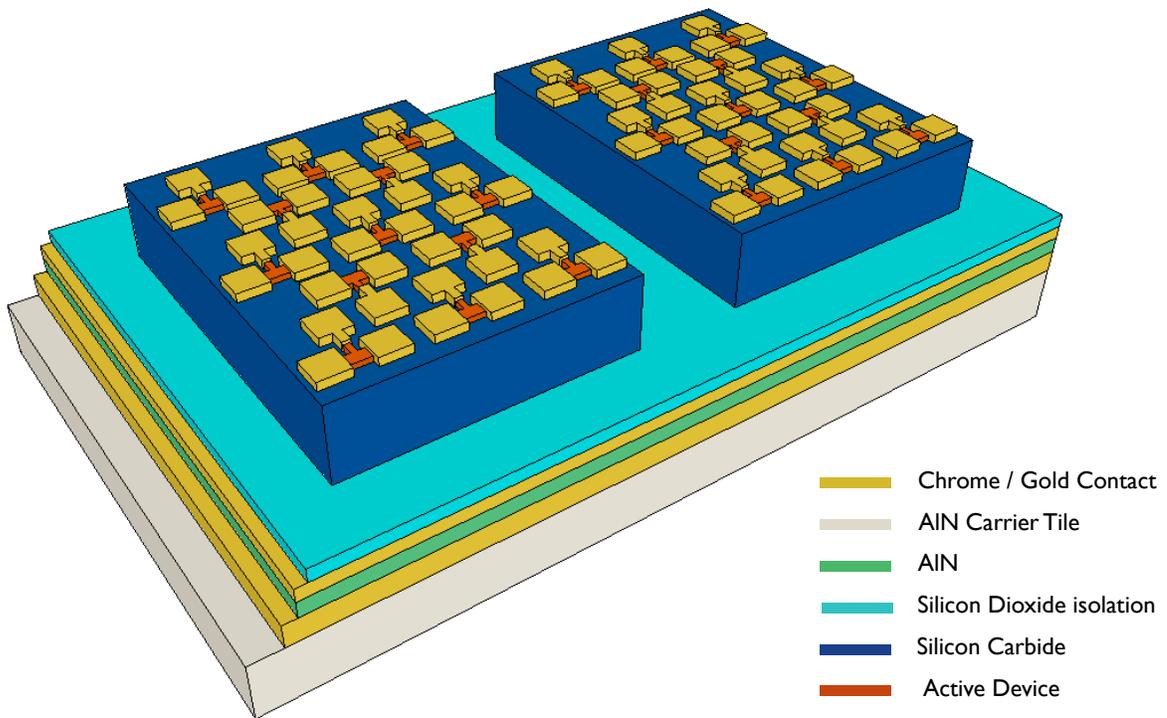

Figure 6.11: Storage integrated into substrate

By using a thicker dielectric the devices should be less affected by the leakage mechanisms seen in the thinner HfO_2 films. Due to the reduced electric field across the dielectric the effect of leakage mechanisms such as Poole-Frenkel or Schottky emission is mush reduced.

6.4.2 Device design

To test larger area, thicker dielectric films, the mask pattern shown in figure 6.12 was used to fabricate AlN MIM capacitors. The area of these devices is 4.9×10^{-3} cm^2 and is a realistic first step into developing MIM storage integrated into the ceramic chip carrier.
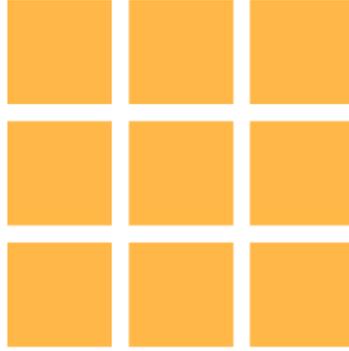

Figure 6.12: Square mask design for AlN MIM capacitors

6.4.3 Process Flow

The capacitors were fabricated on a silicon substrate with a thermally grown 100-150 nm thick SiO$_2$ isolation layer, as shown in figure 6.13 (a). A 100 nm Ti film was deposited using an RF PVD sputter system at 75 W in 100% Argon ambient (40 sccm). This was immediately covered with a reactively DC sputtered AlN layer at 2.5 mTorr chamber pressure, with 50 W power in an ambient of 10 sccm Argon and 20 sccm Nitrogen, 6.13 (b). The AlN was then patterned using photolithography and a 100 nm Au/5nm Cr top contact was formed using lift off in an acetone bath, 6.13 (c-e). The distance between the target and the substrate is 23 cm.

6.4.4 IV

The data in figure 6.14 shows the IV characteristic for 390 nm thick AlN MIM capacitors at elevated temperatures. The data shows that the leakage through the film increases exponentially with temperature, but remains below 50 nA at 600 °C and 15 V. When
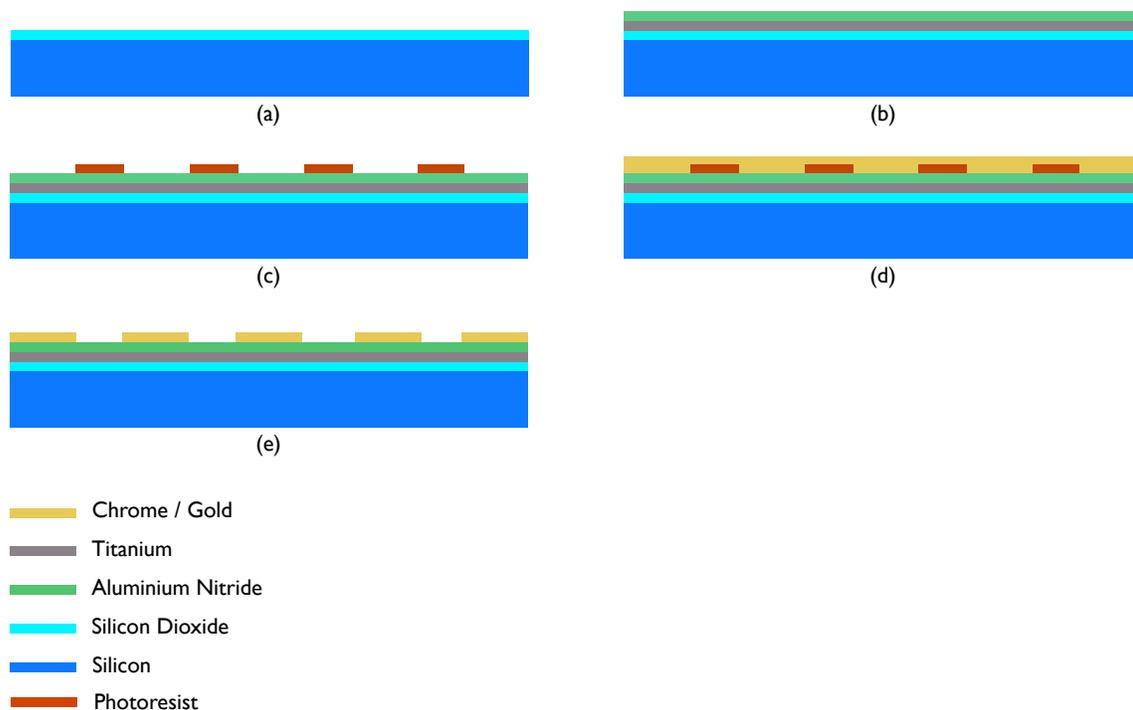
Figure 6.13: Process flow for AlN mim capacitor fabrication

compared to the change in leakage current with temperature shown in figure 6.8 it is clear that the increased thickness has significantly reduced the films leakage. The equipment used for this test has a $1\text{x}10^{-10}$ A measurement limit in the tested range and as such the data is limited to measurements above 500 K. At 500 K the temperature is sufficient to generate a measurable leakage through the film.

Given that these films are considerably thicker than those fabricated using HfO_2 studied in section 5.3, the work function difference between the metal contacts and the dielectric material is less likely to influence the leakage mechanism. This is likely the reason why there is no barrier like that exhibited in figure 6.8.

Figure 6.15 shows the leakage response with temperature and demonstrates that the response is exponential. This indicates that although the leakage mechanisms dominant are not work function difference driven the response is potentially dependant on Poole-Frenkel emission.

To investigate this further Arhenius plots of the leakage current variation with temperature
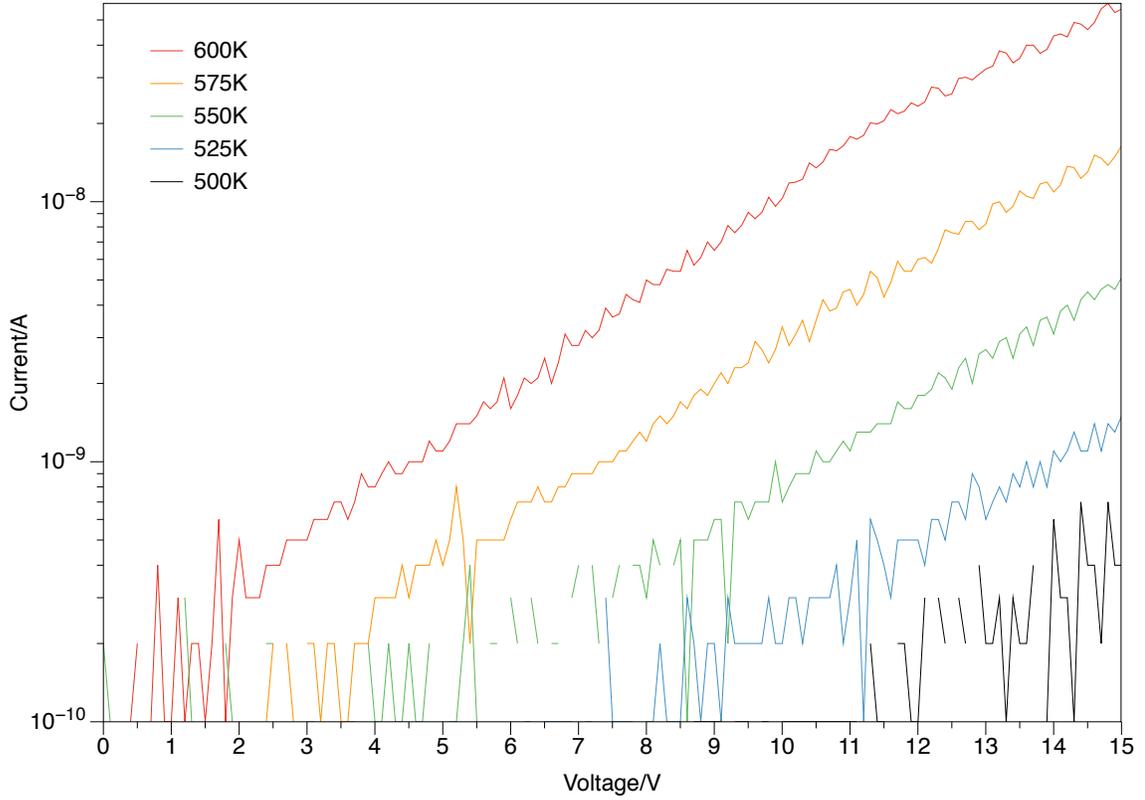
Figure 6.14: AlN MIM capacitor IV characteristics at high temperatures

at 10 V to 15 V, in 1 V intervals, were plotted and the slope of each data set used to extract the trap activation level at each bias. These voltages were chosen as at 500 K, the lowest measurable leakage current was at 10 V. Equation 6.6 shows how this was extracted, where E_a is the activation energy, S the slope of the fit, q the elementary charge and k_B the Boltzmann constant.

$$E_a = \frac{(-S * k_B)}{q} \tag{6.6}$$

The data in figure 6.16 shows that the variation in activation energy demonstrates no discernible positive or negative trend, indicating that the leakage mechanism is trap driven. This suggests that Poole-Frenkel effects are being observed however the data in figure 6.16 is highly dispersed. This dispersion is likely due to the variation in hotplate temperature at elevated temperatures causing a variation in leakage through the IV sweep which is
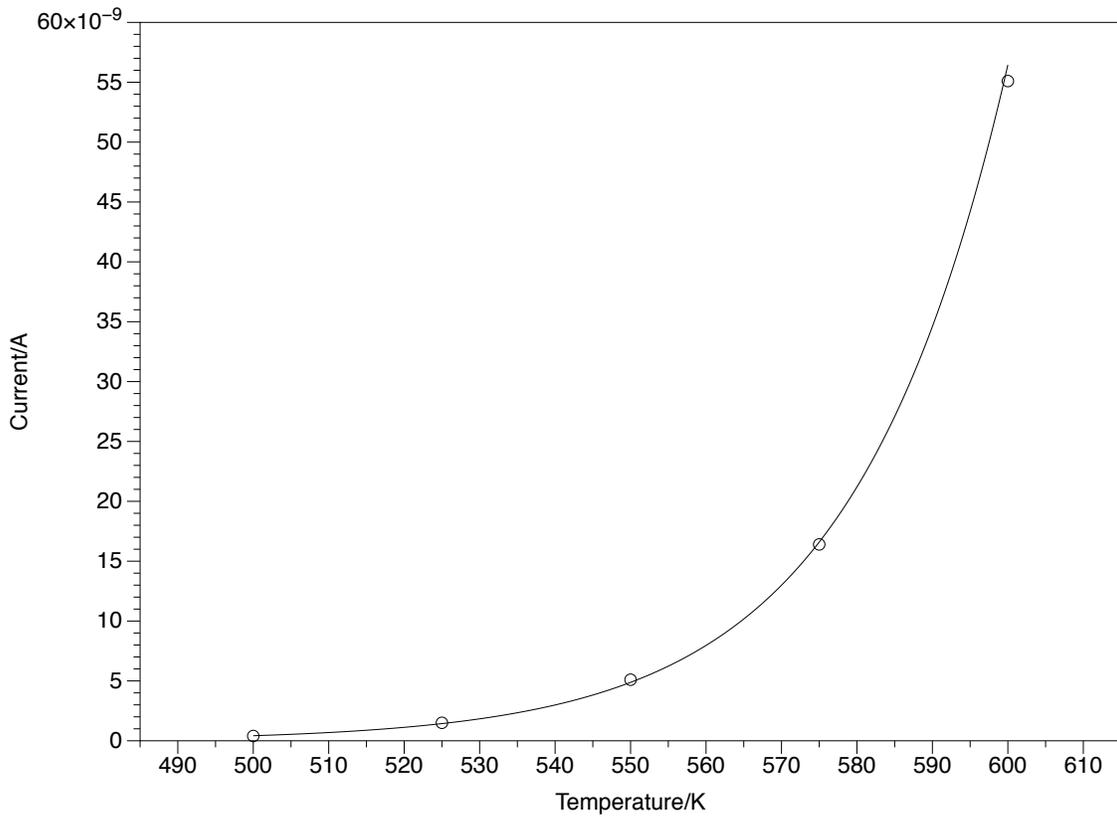
Figure 6.15: Leakage current variation with temperature at 15 V

influencing these data.

The overall leakage current response to temperature shows that these thicker, larger area devices are a potential candidate for high temperature however, as shown in the following section there is a significant trade off in capacitance, and therefore energy, density due to the increased film thickness.

6.4.5   CV

The data in figure figure 6.17 shows the AlN MIM CV sweeps of temperature and demonstrates that these devices exhibit a low voltage capacitance coefficient and are not highly effected by temperature. The device exhibits a 10.8% increase in capacitance from room temperature to 600 K, which is comparable to the stability exhibited by the 60 nm HfO_2 devices discussed previously.
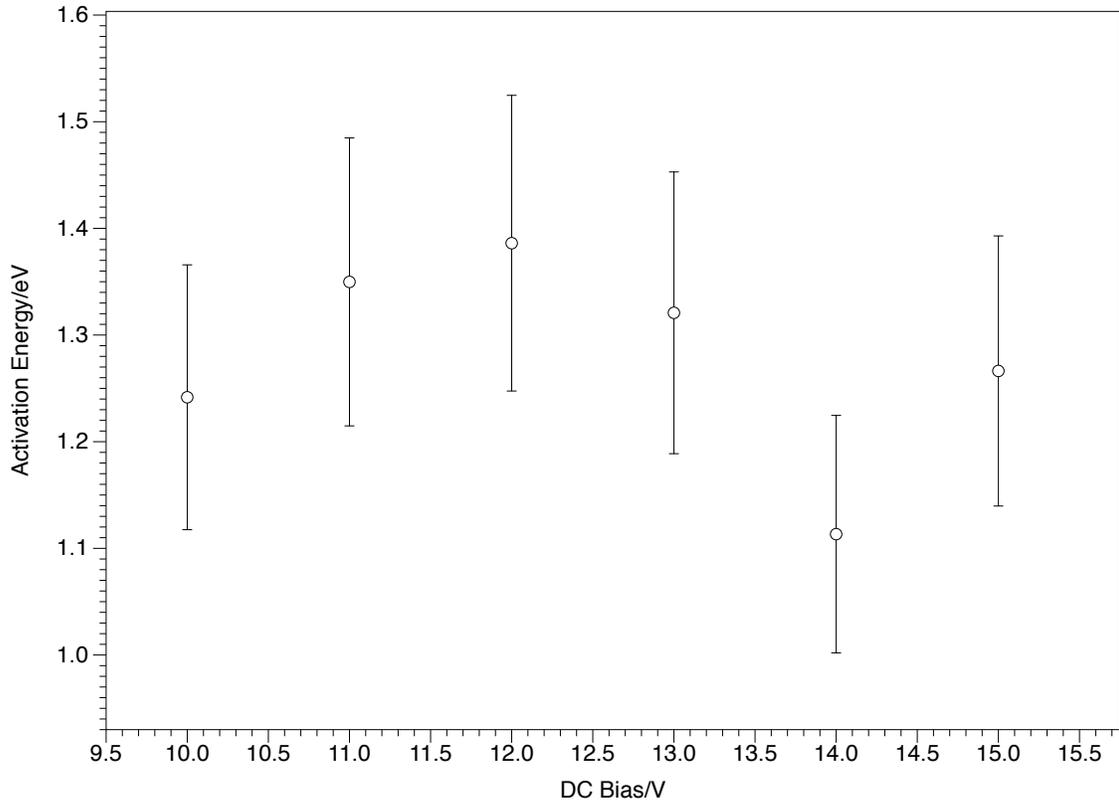
Figure 6.16: Activation energy variation with bias voltage for an AlN mim capacitor

The low capacitance variation with voltage exhibited by these devices is highly beneficial for use as energy storage devices as they maintain a stable storage capacity which is stable for a range of operating voltages. This is vital for use with silicon carbide systems as they operate at voltages significantly greater than that of silicon systems. Previous work has demonstrated SiC circuits operating at 9 - 15 V for the production of a wireless communications system [21].

The data in figure 6.18 show that AlN exhibits a linear dependance to temperature and that the dielectric constant increase from 9.6 to 10.8. This is inline with the literature and within the range for sputtered films [22, 23].

When comparing the suitability of these devices to the HfO_2 ones for the intended application, it is important to understand the effect on the overall capacitance density. Comparing these AlN structures to the 60 nm HfO_2 devices in section 5.3 the dielectric constant is 9.6
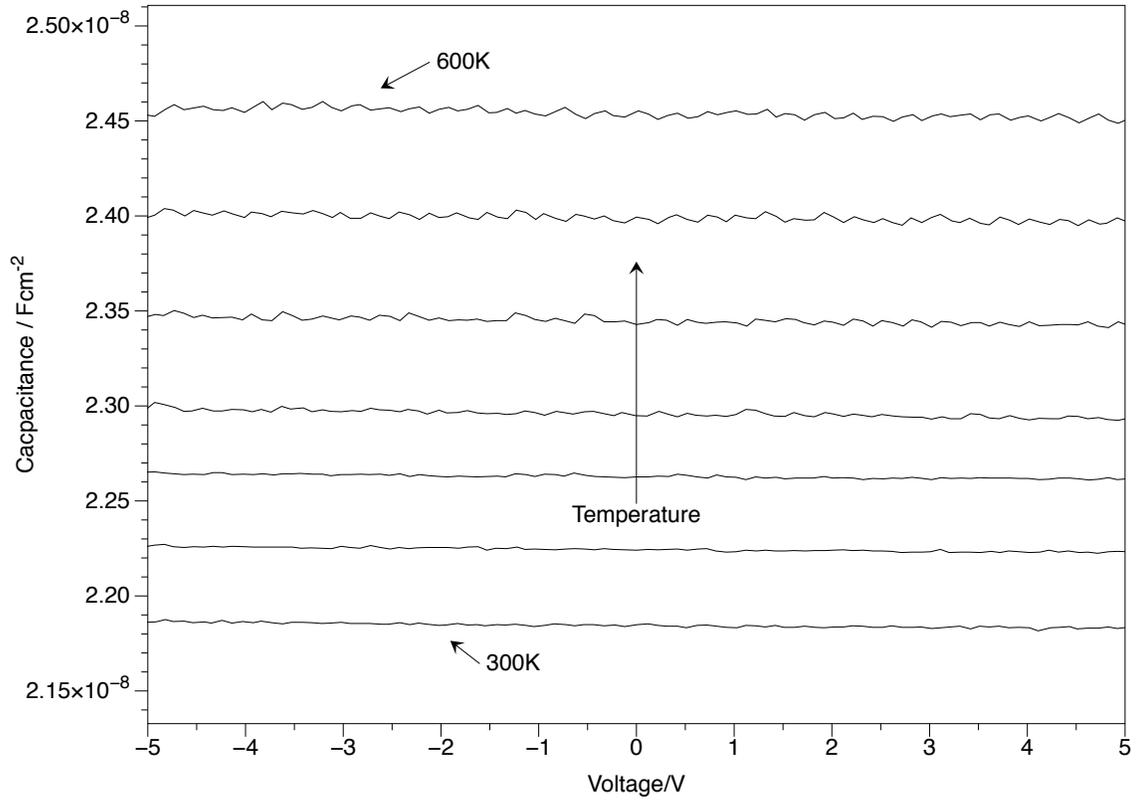
Figure 6.17: CV characteristics for AlN mim capacitor at temperatures from 300 K to 600 K

in comparison to 17.21 at room temperature and the dielectric thickness has been increased from 60 nm to 390 nm. Referring to the parallel plate capacitance equation, repeated here as equation 6.7 for convenience, it is expected that the capacitance density will fall by a factor of 10.5 from that of the HfO$_2$ devices.

$$C = \frac{\varepsilon_0 \varepsilon_r}{d} \tag{6.7}$$

Using the 0 V room temperature capacitance density figures 6.9 and 6.17 there is an observed drop of 10.8 times which is inline with the theoretical value of 10.5. The slight discrepancy is most likely caused by a slight variation in film thickness for the AlN devices across such a large area. Relating this to equation 6.8 it can be seen that although the capacitance density has been reduced by a factor of 10.8 the stored voltage only has to increase by a factor of
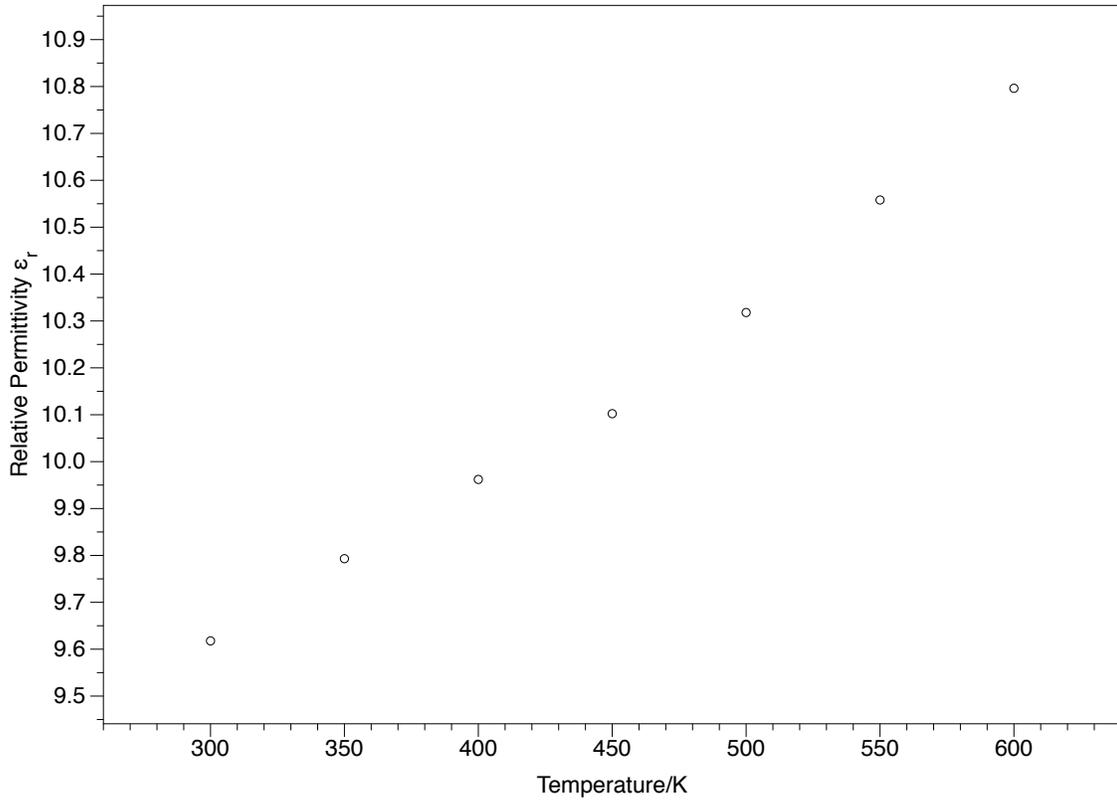
Figure 6.18: Capacitance variation as a function of temperature for AlN MIM capacitor

3.28 to store the same amount of energy. Given that the leakage current of the HfO$_2$ devices at 5V increased significantly with temperature they are likely incapable of reliably storing energy at such a high voltage and so the AlN devices are more suitable.

$$E = \frac{1}{2}CV^2 \qquad (6.8)$$

6.5 Scalability

The physics of energy storage mean that the easiest way to store more energy is to simply increase the contact area of the devices. Due to the increased probability of fatal defects in the film this can significantly reduce the yield of thin film devices. The thick substrate solution presented shows a high device yield, above 90% across 50 devices, and potential for very large area (larger than 1 mm^2) devices fabricated between 2 large electrodes. In

this case, the thick dielectric has significantly reduced the probability of a catastrophic defect. The thinner, on chip devices, however exhibit an unreasonably high leakage current for use as a storage medium. To investigate if this can be improved post fabrication the devices exhibiting the lowest temperature coefficient were packaged and wire bonded such that networks of devices could be realised and tested.

6.5.1 Energy decay rate

Rather than focus on the results of IV and CV tests to analyse the changes due to device networking, the devices open circuit voltage decay, OCVD, was considered as a more realistic metric. The OCVD rate indicates the maximum period a storage device can be left in open circuit before the stored charge is reduced to 37% ($\frac{1}{e}$) of the original value. It is therefore vital to the success of an energy storage device to understand how the OCVD rate can be minimised to provide a stable energy reservoir that can be regulated and dissipated into an electrical circuit.
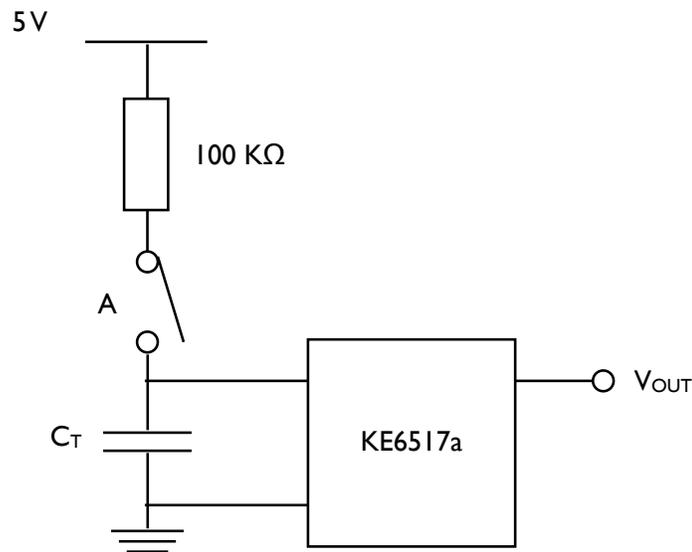

Figure 6.19: Test configuration showing use of Keithley 6517a electrometer used to buffer shunt voltage measurement

The test configuration used in this work, shown in 6.19, comprised of a Keithley 6517a

electrometer, to buffer the shunt voltage measurement across the capacitor by providing a higher impedance than that of the capacitors. The input impedance of the electrometer is $200T\Omega$ and, as the presented results will show, is several orders of magnitude higher than the dielectric impedance. Hence the observed voltage decay will be unaffected. The $100K\Omega$ resistor is used simply to limit the current draw from the power supply if the capacitor were to fail and short circuit. The switch, labelled A, is pressed to charge the capacitor to its maximum storable voltage, when the switch is released the capacitor is in open circuit and the voltage begins to decay. The decay characteristics of typical 35nm and 60nm HfO_2 capacitors are shown in figure 6.20 for 323K and 573K.
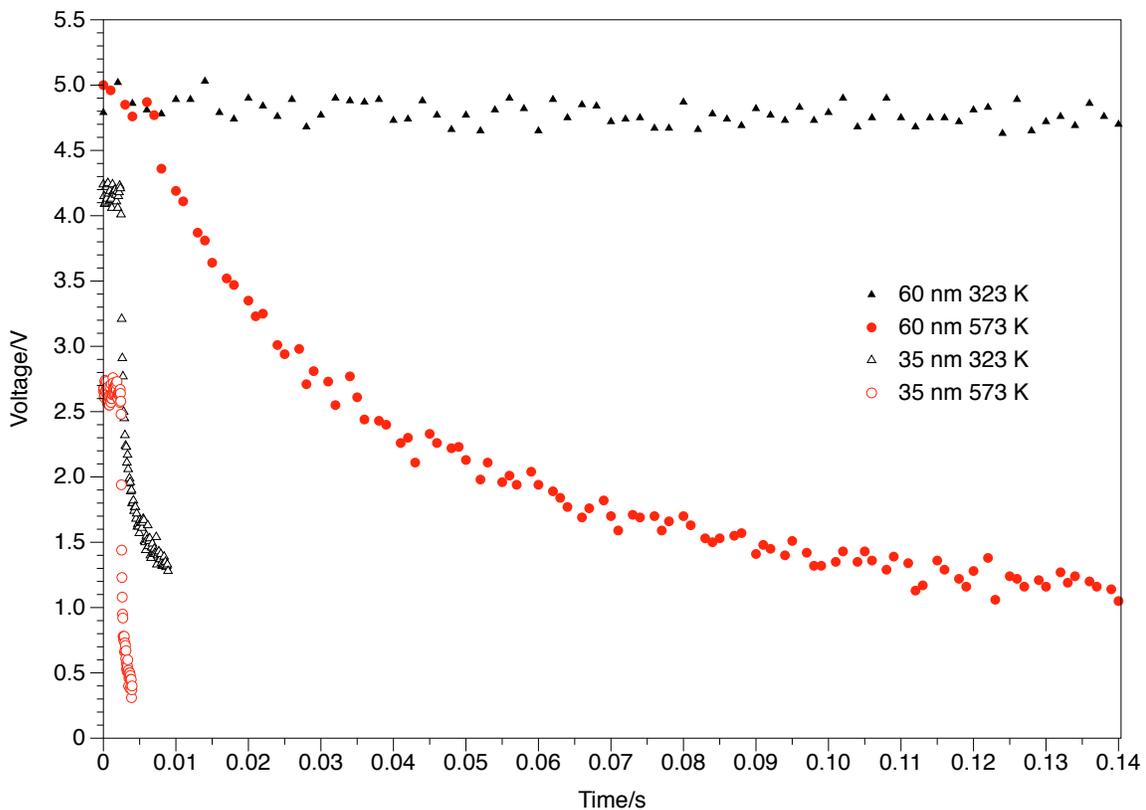
Figure 6.20: OCVD waveforms at 323K and 573K for 35nm and 60nm HfO_2 devices

The data in figure 6.20 shows that there is an increase in OCVD rate with temperature, for both dielectric thicknesses. It is clear that the 60nm device can store charge significantly longer than the 35nm device and that it maintains a full 5V initial charge even at elevated temperatures. This is because the 60nm device exhibits a lower dielectric leakage, therefore

causing a reduction in the OCVD rate and a lower leakage during charging. The 35nm device not only exhibits a similar increase in OCVD rate but it also suffers a large drop in initial stored voltage at elevated temperature due to the increased leakage current.

The high temperature effects on device performance for the HfO_2 dielectric devices is summarised in figure 6.21. The data shows that the 60nm device maintains a full initial charge at 573K compared to the steady fall in initial stored voltage exhibited by the 35nm device. It also shows that the OCVD time is longer for the 60nm device across the temperature range. It can be seen that the OCVD rate has increase by a factor of 20900 for the 35 nm devices, compared to only 13 for the 60 nm devices.
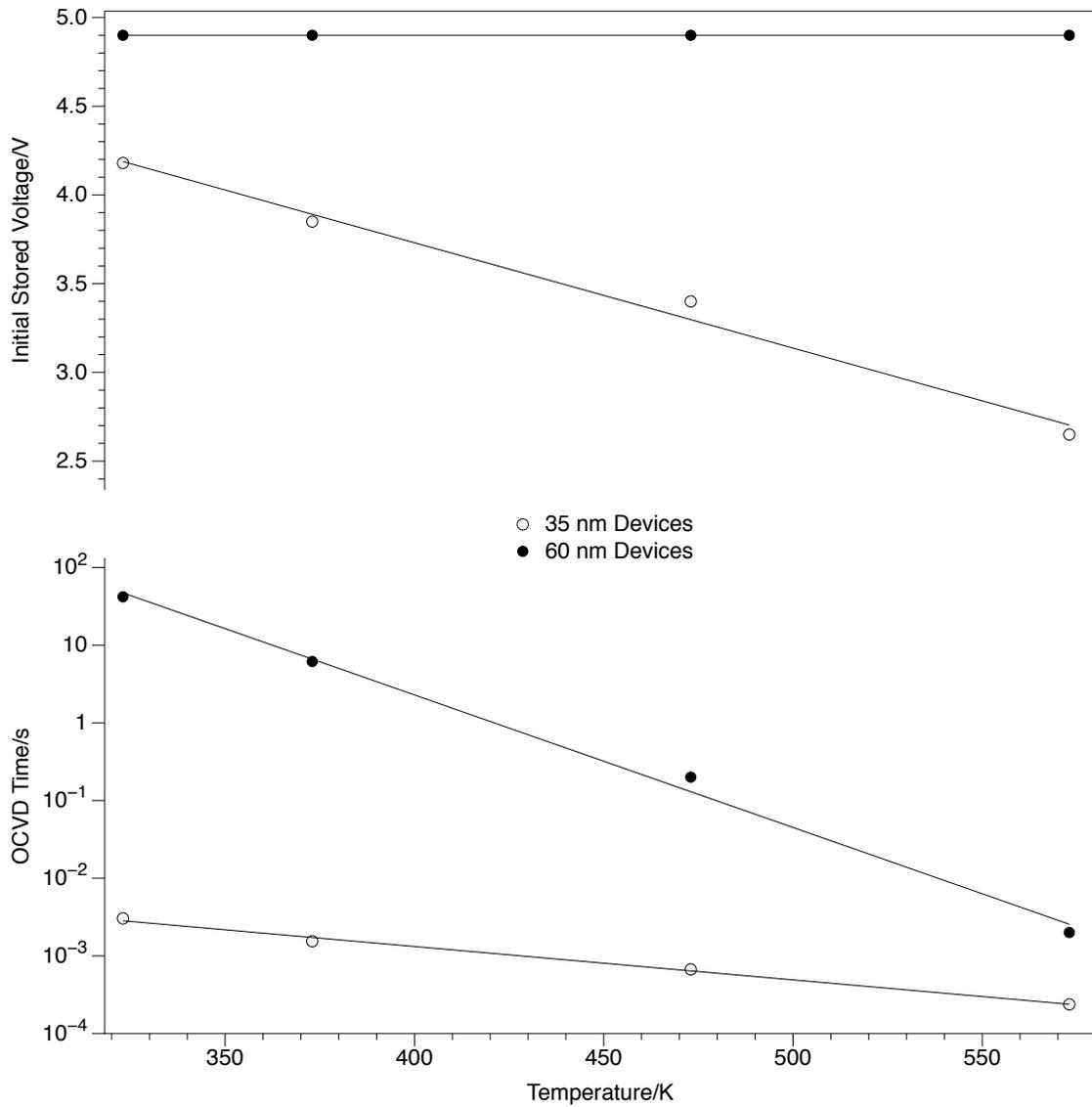
Figure 6.21: Device OCVD time and stored voltage comparison between 323K and 573K, solid fill circles show data for the 60nm HfO_2 device and open circles show data for the 35nm HfO_2 device

This difference, clearly shown in figure 6.21 by the converging OCVD trends for the 35nm and 60nm devices, highlights that the behaviour of the 60nm dielectric exhibits a much stronger temperature dependance than the 35nm dielectric.

The data in figure 6.22 shows the initial electric field for both devices as a function of temperature. It shows that the electric field across the 35nm device decreases with temperature, which reduces the effect of the increased temperature on the leakage mechanism

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and so a lower temperature dependance is exhibited by the 35nm device. In contrast the 60nm device maintains a constant electric field over the temperature range studied and so the temperature increase causes a larger increase in leakage current when compared to the 35nm dielectric.
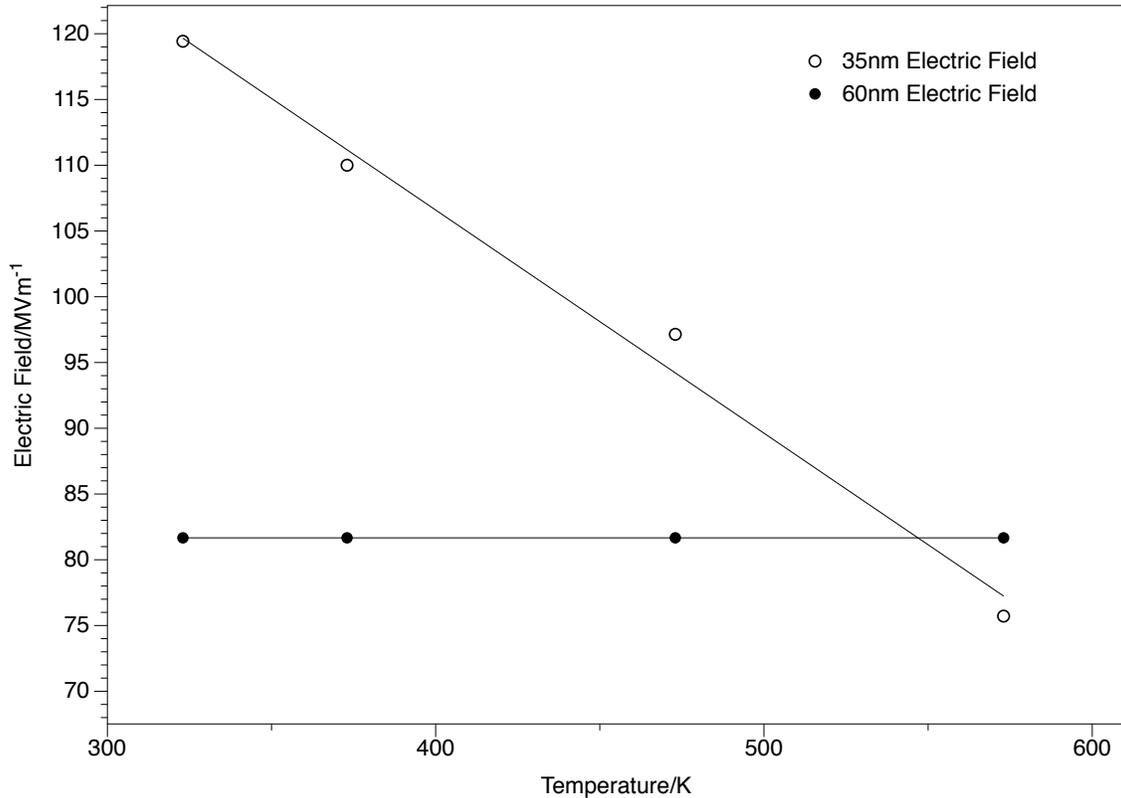
Figure 6.22: Electric field as a function of temperature for 35nm and 60nm devices

The small capacitance of the HfO_2 devices requires a large number to be networked to increase the stored energy. For this to be successful it is necessary to determine the most effective serial/parallel networking of the devices. Given the fundamental formulas governing how capacitance is distributed in capacitor networks, equations 6.9 and 6.11, it can be seen that careful balance is required to obtain a high total capacitance while maintaining a high effective shunt resistance. Parallel connection leads to increased capacitance, but reduces the effective shunt resistance. It is important to bear in mind that although equation 6.11 refers to series resistance it is still a shunt resistance with respect to the leakage path through the dielectric.

$$C_{par} = C_1 + C_2 + ... + C_n \qquad (6.9)$$

$$R_{par} = \left[\frac{1}{R_1} + \frac{1}{R_2} + ... + \frac{1}{R_n} \right]^{-1} \qquad (6.10)$$

$$C_{ser} = \left[\frac{1}{C_1} + \frac{1}{C_2} + ... + \frac{1}{C_n} \right]^{-1} \qquad (6.11)$$

$$R_{ser} = R_1 + R_2 + ... + R_n \qquad (6.12)$$

Figure 6.23 describes how the parallel and series connections of the devices were formed, given that devices has a common cathode the setup for series was limited to just two devices.
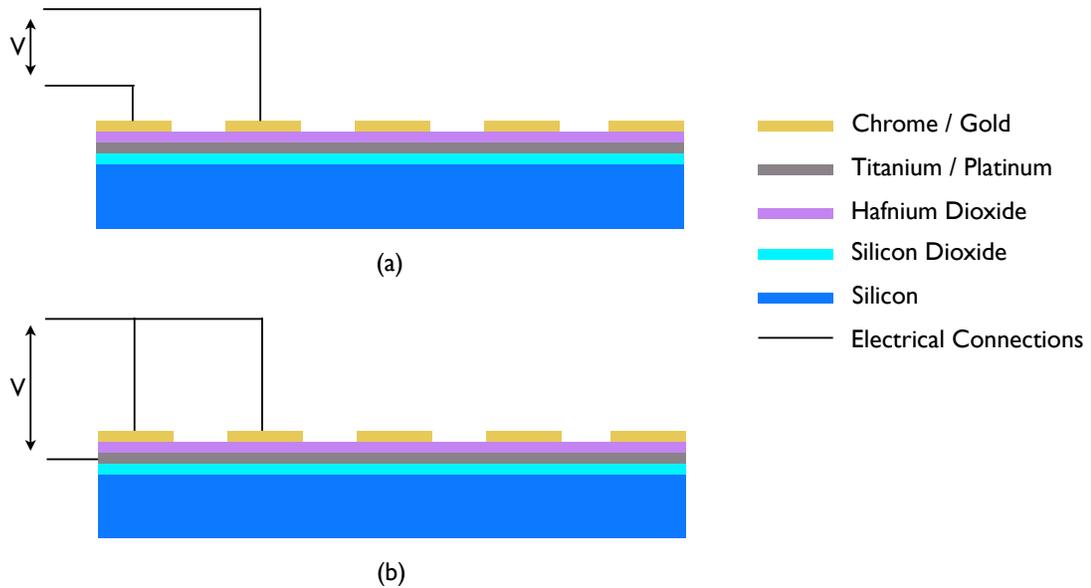

Figure 6.23: (a) Series and (b) parallel connections for HfO$_2$ MIM devices networked together

The data in figure 6.24 demonstrates how the OCVD rate can be reduced by connecting two

similar devices in series where series A and B are the observed changes for the individual devices. It can be seen that the OCVD rate has been reduced by a factor of 8.6 for series connection. Given that the discharge rate of a capacitor is dependent on the RC constant, the observed increase in the OCVD time is unexpected. For a serial connection of two devices, the predicted change in capacitance and resistance should be in accordance with equations 6.11 and 6.12. If both the resistance and capacitance were to change in accordance with these two equations, then the RC constant would be similar to that of the individual devices. However figure 6.24 shows that only the parallel connection behaves as predicted. This result strongly indicates that the serial connection of two devices has a much greater effect on the shunt resistance of the network than it does on the capacitance, this results in a reduced leakage and increased the storage time.
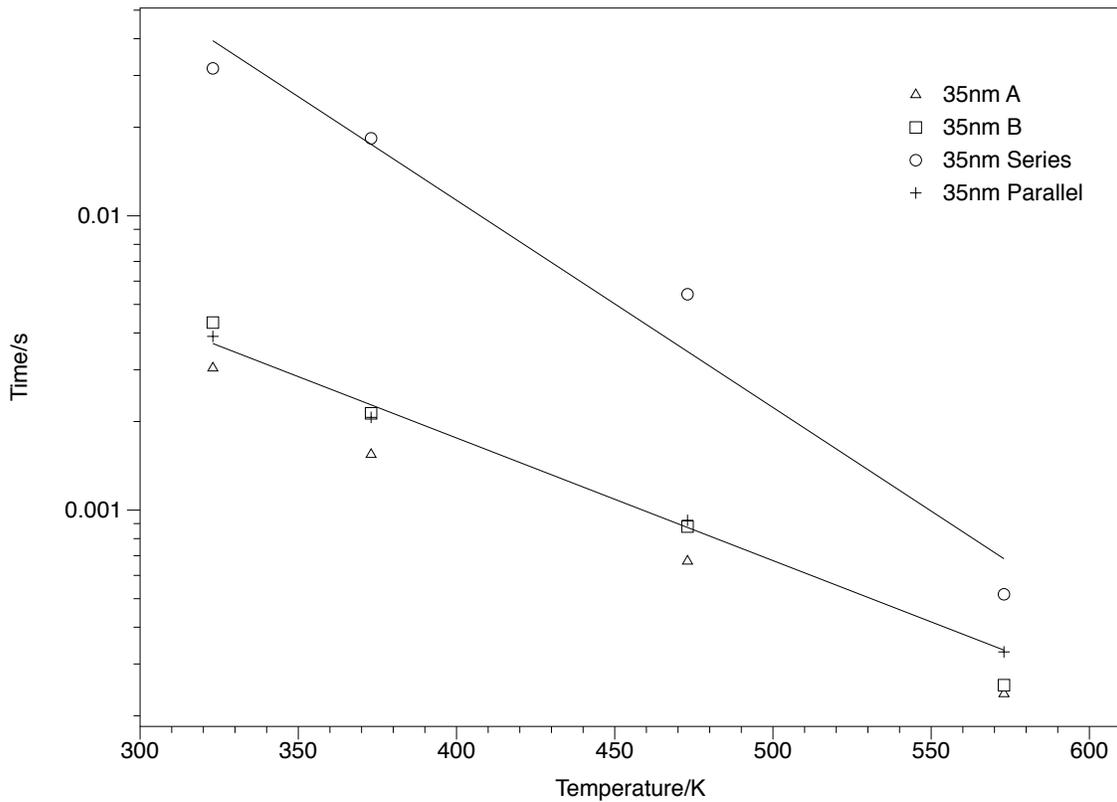

Figure 6.24: Serial and parallel configuration effects on OCVD time of two similar 35nm devices

Previous work has shown that although the devices are operable in both positive and neg-

ative bias conditions, the CV characteristic is asymmetrically parabolic with its minimum capacitance at just under 0V [24]. This is due to the different barrier heights caused by the use of different metal contacts for the anode and cathode. The structure of the devices mean that when in series they are connected in a back to back configuration, as such one device is operating in forward bias and the other is in reverse. This configuration, coupled with the different barrier heights for the two metal-insulator interfaces, may cause the larger than expected decease in OCVD rate for serial connection. Previous work has shown that, alongside Poole-Frenkel emission, Schottky emission also plays a minor role in the leakage mechanism of these devices [16]. The decay characteristics could be effected by the fact that this serial configuration is 4 Schottky diodes in a $m-i-m-i-m$ structure as shown in figure 6.25.
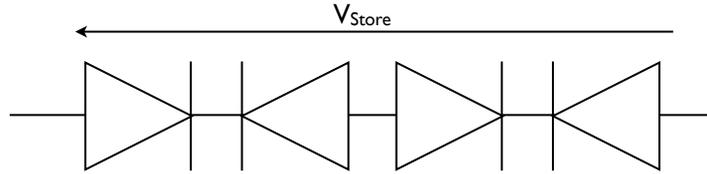

Figure 6.25: Equivalent circuit diagram for series connected HfO$_2$ MIM capacitors

Networking the capacitors also effects the maximum stored voltage. The data in figure 6.26 shows that serial connection reduces the change in stored voltage with temperature compared to that of the individual devices. The improvement can be attributed to the reduced dielectric leakage caused by the serial connection. The test setup placed the capacitor in series with a 100 kΩ resistor and so the effective shunt resistance can be calculated for the devices. For the single capacitor A this is found to be an order of magnitude lower than the serial system at temperatures below 573 K, hence the reduced stored voltage as part of the 5 V is being shared between the resistor and the capacitor. Above 573 K the series connected devices effective shunt resistance falls to 400 KΩ and as such can no longer hold a 5V initial charge and there is the observed voltage decrease seen in figure 6.26.

Compared to capacitor A, the parallel connection reduces the maximum stored voltage of the system by 7.8% at room temperature increasing to 13.2% at 573 K. This change across

temperature is minimal, however the average loss of 10% is much lower than the gain in stored voltage caused by the serial setup. This is most likely due to a balance change in capacitance and resistance for the parallel setup maintaining a similar RC constant. The serial configuration improvement is from the increased shunt resistance, as discussed perviously with the OCVD time results.
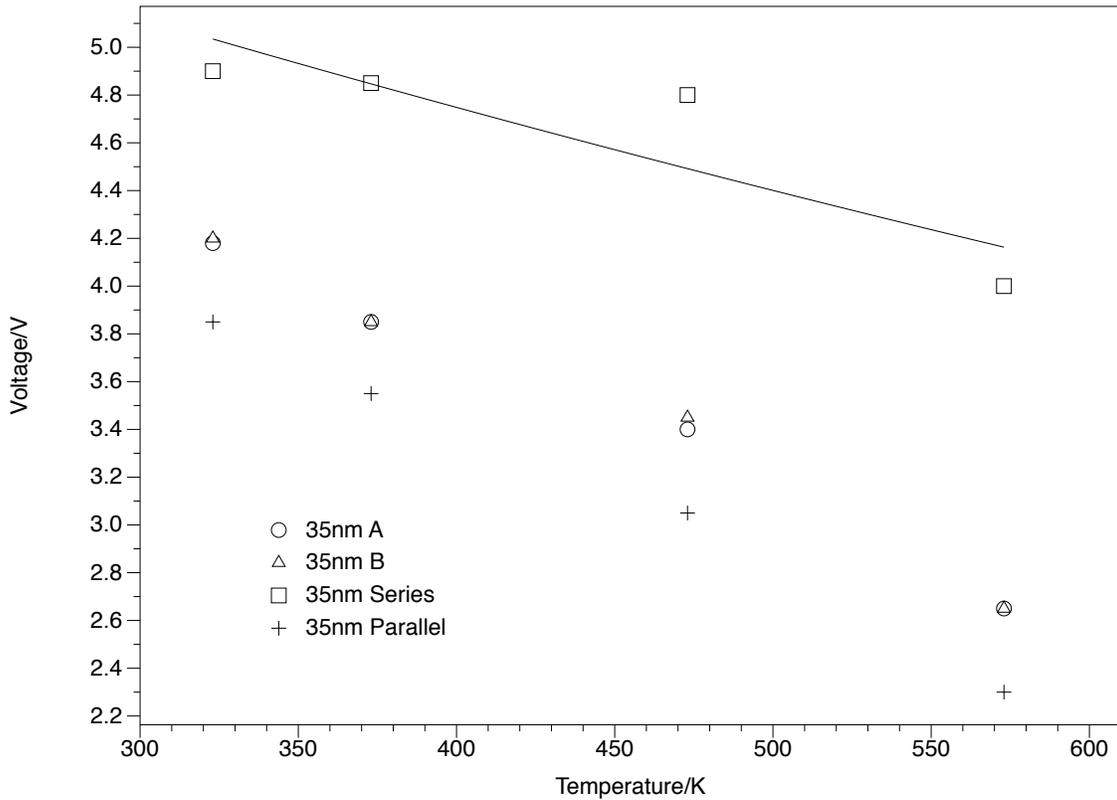
Figure 6.26: Serial and parallel configuration effects on initial stored voltage of two similar 35nm devices

6.6 Conclusion

This chapter investigated the potential use of resilient dielectric materials as an energy storage medium in an energy harvester powered resilient sensor system. Comparing two different solutions and analysing the materials required shows that although temporary energy storage is possible in an on chip solution, the difficulties associated with producing large area thin films which exhibit a low leakage temperature coefficient, makes this solution

difficult to reliably implement. Serial and parallel networking of such devices produces unexpected improvements with regards to the OCVD. However, the substrate based, AlN approach appears to be more feasible. Given that silicon carbide technology currently uses large area circuits with lots of empty substrate space it is a reasonable assumption that the low capacitance density, in comparison to the on chip HfO_2 solution, can be realised through fabrication of large area devices.

Both of these potential solutions show promise as a high temperature energy storage medium and takes steps to address an issue which will severely hinder the development of high temperature, energy harvester powered systems as they mature. At this stage however, it is too early to determine which of these two methods is more suitable or to predict the levels of energy that could realistically be stored by them.

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Chapter 7

Conclusion

The project has focussed on addressing the need of developing a suitable power supply to power resilient electronic systems deployed in hostile environments. Given the ever increasing desire and need to monitor man made and natural processes to determine their impact on the environment it is clear that sensor systems which are capable of operation in the harshest conditions is required. If we wish to reduce our impact on the environment and begin to see positive steps taken toward stemming the flow of green house gasses into the atmosphere then wide band gap technologies such as silicon carbide will need extensive development along with suitable supporting technologies such as energy harvesting and resilient passives.

The literature review of this thesis proposed a resilient sensor system comprising only resilient components whereby the sensing element, power regulation, communications and amplification elements use silicon carbide technology. The rest of this section detailed the areas relevant to energy harvester powered system design and appraising the different forms of energy harvesting which could be used in a hostile environment.

Chapter 3 developed a energy harvester powered wireless sensor system which is capable of autonomous operation from ambient vibration energy. The discussion of this system identified design considerations for not only developing systems which are energy harvester

powered, but also that are capable of high temperature operation. By focussing on current, commercially available components this work avoided the need to develop custom components or electronics and high lighted where resilient technology must be developed to address the issues found in hostile environments.

Addressing this need, chapter 4 details how a currently available material operates at elevated temperatures. The piezoelectric material, PZT, is capable of harvesting energy up to 300 °C with a decrease in output power proportional to temperature governed by variations in output voltage, mechanical damping and Young's modulus. The extracted room temperature effective Young's modulus is found to be 66 GPa which is inline with the literature. The degradation with temperature of the Young's modulus appears is formed by two linear regions with an inflexion point at 448 K. This inflexion is potentially an elastic limit with respect to temperature, however when cooled the resonant frequency returns to within 4% of its initial value however it does exhibit a hysteresis characteristic above 398 K.

The output voltage decreases significantly with temperature, from 11.2 V at room temperature to 1.1 V at 573 K. Although 1.1 V is below the room temperature voltage drop of a SiC full wave rectifier the signal can still be used as the voltage drop of the Schottky diodes used in such a rectifier decreases by 2 mV/K to 0.1 V at 573 K. Given that the full wave rectifier voltage drop is only 0.2 V the output signal from the piezoelectric energy harvester is still capable of producing a useful voltage.

Where chapter 4 discussed the application of a room temperature technology to hostile environment, chapter 5 instead characterised the behaviour of an already resilient technology, in the form of SiC pin diodes, can be used as a resilient energy harvester. The power output of silicon solar cells is heavily temperature dependant and as such they are not suitable for hostile environments. The results in chapter 5 show how silicon carbide, with its wide band gap, can be used as an effective UV energy harvester up to 300 °C. The output power and fill factor remain stable with respect to temperature exhibiting an efficiency of 6% to the harvestable section of the spectrum. a 700 hour thermal stress test at 450 °C identified that although silicon carbide is resilient to long term thermal soaking, the metal contacts used

on the devices are not. SIMS analysis shows significant metallic migration and oxidation of the aluminium layer in the contact stack which increases the series resistance of the devices until they are not useful as either photovoltaic devices or simple diodes. This could be improved with the addition of a diffusion barrier in the contact stack and as such extend the life of the cell.

Chapter 6 identifies two potential solutions to storing harvested energy in a resilient sensor node. The two options each have merit with an on chip option allowing for the possibility for monolithic sensor nodes where all devices, including energy storage, are fabricated on a single SiC die. This is favourable for fabrication purposes as it limits the post fabrication assembly and reduces the mechanical failure points in the system. To overcome the issue of limited space, due in part to the cost of SiC wafers, thin HfO_2 MIM capacitor would have to be incorporated on the chip. 60 nm and 35 nm MIM capacitors were fabricated to test such a solution and it was found that the leakage at elevated temperatures caused a significant reduction in storage capability.

Alternatively, a substrate solution incorporated into the carrier of a hybrid module system could be made significantly thicker as the limitations on space do not apply. AlN DCB tiles have been used as an effective high temperature circuit board and so AlN MIM capacitors with thickness of 390 nm were fabricated to determine the viability of a such a solution. The thicker films exhibited a much reduced leakage and stable operation at elevated temperatures. Given that the reduced capacitance density can be overcome with the large areas available on the carrier this is a more promising solution.

7.1 Future work

The future work which can build upon this thesis can be clearly placed in two categories, first to further address the need for a high temperature energy harvester and second, to create a high temperature energy storage and power regulation system.

Initially a stable high temperature vibration energy harvester must be developed which can

operate for long periods of time in high temperature environment. Piezoelectric materials which do not require poling are required for such a device, there are a range of materials which present themselves for this role however the most advanced and easily incorporated in AlN which, as briefly discussed, can be fabricated to exhibit a piezoelectric response. AlN in a close packed, hexagonal Wurzite film of between 1 - 2 μm has been shown to be an effective room temperature energy harvester. Unlike PZT it requires no poling and therefore exhibits a stable response to very high temperatures. If such a device could be coupled with a SiC rectifier the output power would increase with temperature as the undesirable voltage drop of the rectifier would drop to 0.2 V at 300 °C whilst the energy harvester would maintain a stable output.

Once the energy has been harvested there is a clear need to store and regulate it. Initial work has demonstrated the potential for a high temperature storage system however, the development of a high power regulator remains unaddressed. Once energy has been collected it must be released in to the dependant electronics at a suitable power and voltage level, developing electronics which can do this at high temperatures is currently problematic. The project did consider the use of two bipolar transistors configured to exhibit an S mode negative differential resistance effect however such a system was quickly ruled out due to the lack of p-type SiC bipolar transistors. Instead an automatic switching systems needs to be developed using either SiC JFETs or MOSFETs which can determine when enough energy has been harvested for system operation.

Ideally SiC will continue its current growth and both industry and academia will further realise the potential it has beyond simply high power operation and in years to come simple SiC micro-controllers will allow a system such as that developed in this works literature review to be obtainable.