

Impact of Randomly Distributed Dopants on Ω -Gate Junctionless Silicon Nanowire Transistors

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Abstract—This paper presents experimental and simulation analysis of an Ω -shaped silicon junctionless nanowire field-effect transistor (JL-NWT) with gate lengths of 150 nm and diameter of the Si channel of 8 nm. Our experimental measurements reveal that the ON-currents up to 1.15 mA/ μ m for 1.0 V and 2.52 mA/ μ m for the 1.8-V gate overdrive with an OFF-current set at 100 nA/ μ m. Also, the experiment data reveal more than eight orders of magnitude ON-current to OFF-current ratios and an excellent subthreshold slope of 66 mV/dec recorded at room temperature. The obtained experimental current–voltage characteristics are used as a reference point to calibrate the simulations models used in this paper. Our simulation data show good agreement with the experimental results. All simulations are based on drift-diffusion formalism with activated density gradient quantum corrections. Once the simulations methodology is established, the simulations are calibrated to the experimental data. After this, we have performed statistical numerical experiments of a set of 500 different JL-NWTs. Each device has a unique random distribution of the discrete dopants within the silicon body. From those statistical simulations, we extracted important figures of merit, such as OFF-current and ON-current, subthreshold slope, and voltage threshold. The performed statistical analysis, on samples of those 500 JL-NWTs, shows that the mean I_D – V_{GS} characteristic is in excellent agreement with the experimental measurements. Moreover, the mean I_D – V_{GS} characteristic reproduces better the subthreshold slope data obtained from the experiment in comparison to the continuous model simulation. Finally, performance predictions for the JL transistor with shorter gate lengths and thinner oxide regions are carried out. Among the simulated JL transistors, the configuration with 25-nm gate length and 2-nm oxide thickness shows the most promising characteristics offering scalable designs.

Index Terms—Drift diffusion (DD), electronic transport, junctionless (JL) nanowire field-effect transistors (FETs) (JL-NWTs), random dopants, scattering mechanisms, silicon nanowire, simulations, variability.

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I. INTRODUCTION

SILICON nanowires have a wide spectrum of promising applications such as current field-effect transistors (FETs) [1], ion-selective nanosensors [2], imaging sensor [3], photovoltaics [4], energy conversion and storage [5], and qubits [6]. However, fabricating a nanowire with characteristics required for a specific application can pose some major challenges. For example, as the transistor dimensions are reduced, the ON-current and OFF-current ratio (I_{ON}/I_{OFF}) decreases. Keeping this ratio high is critical, if we want to achieve high-speed operations of the transistors. Also, keeping the I_{OFF} current very low is essential for low-power application systems such as tablets and mobile phones. Hence, the aim for the technology, nowadays, is to provide as low as possible I_{OFF} without comprising the high value of I_{ON} . The low I_{OFF} is one of the major challenges of the planar MOSFETs. Source-to-drain quantum tunnelling [7]–[9] or variability [10]–[12] is much more pronounced and deteriorate the I_{ON}/I_{OFF} ratio in current ultrascaled devices. To overcome this problem, a variety of new architectures, including ultrathin silicon-on-insulator (SOI) [13]–[15], double gate [13], [16], FinFETs [17], [18], trigate [19], Ω -gate [20], junctionless (JL) [21], and gate all-around nanowire FETs [22], have therefore been developed to improve the electrostatic control of the conducting channel. In those architectures, the surface surrounded by the gate is increased in relation to the channel volume, improving the electrostatic control.

In conventional planar MOSFETs, the drain current (I_D) can be improved accordingly to the semiconductor mobility and gate length (μ/L_{CH}) ratio. Specifically, $I_D \propto (\mu/L_{CH})(V_{GS} - V_{TH})^2$, where V_{GS} and V_{TH} are the gate and threshold voltages, respectively. When reducing L_{CH} , I_D is expected to increase. However, I_D is limited by the negative impact on the mobility of the large doping concentrations needed to preserve the electrostatic integrity in the channel. In addition, in ultrathin body MOSFETs, surface roughness (SR) scattering is increased due to the strong electric field necessary to form an electron channel close to the Si–oxide interface [21], thus deteriorating I_D .

Efforts from the device community have been, therefore, devoted on researching new high-mobility materials [23], [24] or novel devices architectures [25]–[27]. Flat-band devices such as JL nanowire FETs (JL-NWTs) have gained substantial attention in recent years [25]–[27]. Contrary to the “standard” p-type or n-type MOSFET devices that operate in an inversion

mode, the JL-NWTs work in a partial depletion mode. As a result, the current is flowing mainly through the body of the transistor creating a 3-D conducting channel far away from the Si–oxide interface. This can explain why the SR scattering is not the limiting mechanism for these nanowire FETs [28].

Being a normally ON device, the JL transistor acts as a gated resistor that pinches off the carrier density by applying a gate voltage or by selecting a gate metal with an appropriate work-function. It becomes a depleted, normally OFF, device. When switched ON, the JL transistor is under flat-band conditions. Due to the resistive behavior of the channel $I_D = I_{ON}$, with $I_{ON} = q\mu N_D A_{\perp} V_D / L_{CH}$, where q is the electronic charge, N_D is the doping concentration, A_{\perp} is the channel conducting cross section area, and V_{DS} is the source–drain applied voltage. From the last expression, one may think that by increasing the doping concentration N_D , I_{ON} would be increased. However, N_D cannot be arbitrarily large, because the semiconductor will become a nearly metallic system, making the channel depletion for a particular cross section very difficult. Larger doping concentrations would also be reflected on a higher number of random distributed dopants, leading to strong variability of I_D – V_{GS} characteristics. Taking into account the position and the number of the random dopant in the Si body is important to investigate the optimal performance of specific JL-NWTs. Indeed, this paper focuses on random distributed dopants and their impact on the current–voltage characteristics of the fabricated Ω -gate Si nanowire FETs reported in [28].

For that purpose, this paper is organized as follows. In Section II, the fabrication procedure of JL Ω -gate transistors is summarized. The simulation methodology is explained in Section III. Statistical analysis performed on samples over 500 JL transistors, including devices with shorter gate lengths and thinner oxide regions, is presented in Section IV. Finally, the conclusion is presented in Section V.

II. FABRICATION

The fabrication process of the JL-NWT considered here is explained in detail in our previous works [28]–[31]. For completeness of this paper, however, we summarize the most relevant steps during the fabrication procedure as follows.

Transistors have been fabricated from 55-nm SOI wafers from SOITEC with a 145-nm buried oxide. The Si channel was implanted with phosphorus at 15 keV to allow majority of dopants to sit at the bottom part of the channel with a dose of $4 \times 10^{15} \text{ cm}^{-2}$ before being annealed at 950 °C for 90 s to provide an implanted doping density of $8 \times 10^{19} \text{ cm}^{-3}$. Temperature-dependent Hall bar measurements on large samples [28] were used to determine that the activated dopant density was $4 \times 10^{19} \text{ cm}^{-3}$. This is well above the Mott criteria for Si:P, implying that the bulk material is strongly metallic in electronic behavior [32] which is confirmed by the temperature dependence of the electronic properties [28]. The top Si was then etched to reduce the thickness for the smallest dimension nanowires before a Vistec VB6 electron beam lithography tool was used to pattern the nanowire using hydrogen silsesquioxane (HSQ) resist. Initially, HSQ resist was used as a mask to etch 55-nm nanowires with 24, 16, and

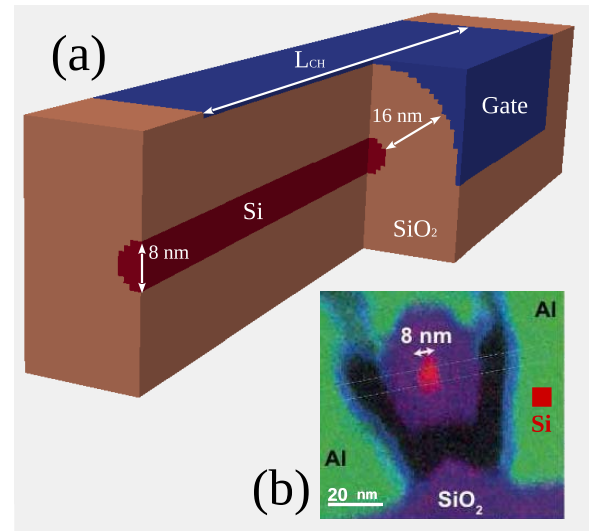


Fig. 1. (a) Sketch of the JL FET, with cuts along and perpendicular to the transport direction, considered in this paper. The gated channel region is designed following the Ω -shaped of (b) fabricated silicon nanowire JL FET. The doping has been experimentally estimated to be 10^{19} cm^{-3} . The silicon nanowire diameter is 8 nm and the oxide thickness is 16 nm within the Ω -gated region with 150 nm long.

8 nm widths, after which via holes were opened in polymethyl methacrylate (PMMA) resist to selectively thin down the Si channel. A low-damage $\text{SF}_6/\text{C}_4\text{F}_8$ inductivity coupled plasma etch [33] was undertaken before the resist was stripped and a thermal oxide grown at 950 °C. Optical lithography was then used to define electrical contacts using 20 nm of Ni and 50 nm of Pt after the oxide had been stripped with HF. An anneal in forming gas at 380 °C for 15 min was used to alloy the contacts forming NiSi Ohmic contacts with a specific contact resistance of 0.8 $\Omega \text{ mm}$. Finally, electron beam lithography was used with 400 nm of PMMA resist to lift-off the Al gate.

The oxidation step resulted in the nanowires being suspended above the buried oxide of the substrate preventing a short gate length being realized later in the fabrication process as reliable lift-off requires resist significantly thicker than any step height. A wide Al gate was, therefore, deposited by lift-off of total length of 2 μm but since the nanowire length was 150 nm, the effective gate length, L_g , is 150 nm. The gate oxide of 16-nm equivalent oxide thickness for the devices has an integrated deep interface trap density, D_{it} below $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ as extracted from measurements on test capacitors fabricated on the same chips. An electron energy loss spectroscopy transmission electron microscope (TEM) image of the smallest nanowire with a diameter of $8 \pm 0.5 \text{ nm}$ is presented in Fig. 1(b). A 3-D sketch of the fabricated and simulated JL-NWT is also shown in Fig. 1(a).

Direct current current–voltage characteristics were measured using an Agilent B1500 semiconductor parameter analyser at room temperature (293 K) with a Cascade Microtech probe station. For the alternating current (ac), lock-in measurements a constant voltage setup was used consisting of a 77-Hz 0.1-V amplitude ac sinusoidal signal from an Agilent 33521A function generator with a voltage

divider (10 M Ω and 1 k Ω resistors) and the current measured using a 1-k Ω resistor with a Stanford Research SR830 lock-in amplifier.

III. SIMULATION METHODOLOGY

The JL transistors were simulated using the commercial TCAD simulator—GARAND which is now part of Synopsys TCAD Sentaurus Simulator. The solution of the transport problem is based on the drift-diffusion (DD) formalism. In this particular case, the DD approximation includes density gradient (DG) quantum confinement corrections [34]. The DG quantum correction is necessary to properly take into account quantum confinements effects within the DD approximation. The Coulomb potentials associated with individual discrete charges are also accurately captured by the DG, being important for the study in this paper. Finally, within this approximation one must solve self-consistently the Poisson and DG equations [35]. Fig. 1(a) represents the device considered in this paper. The silicon diameter is 8 nm, the SiO₂ body thickness is 16 nm, and the gate length is $L_{CH} = 150$ nm, which have been experimentally estimated and shown in Fig. 1(b). The cross section dimensions of the device are measured by a TEM, which clearly distinguishes the Si nanowire core (red) from its SiO₂ (purple) surroundings. For the purpose of this paper, the channel cross section is fixed to 8 nm, where the gate length and SiO₂ are varied for performance predictions purpose. The source, channel, and drain regions are doped accordingly to the experimental value, being $N_D = 10^{19}$ cm⁻³. The contacts, source, and drain are assumed to be semi-infinite. The von Neumann boundary conditions are imposed to allow the potential adjusts the electron injection to preserve charge neutrality in both of them. The device transport is then simulated at room temperature.

Fig. 2 compares the simulated current–voltage ($I_D - V_{GS}$) characteristics with its corresponding experimental measurements for six different devices all with $L_{CH} = 150$ nm and oxide thickness of 16 nm. In this case, the transistor was assumed to be uniformly doped which corresponds to continuous doping concentrations in the silicon. An agreement is achieved between the experimental values and the simulations results. The simulated $I_D - V_{GS}$ curve is within the experimental variability at low- and high-gate voltage biases. The discrepancies in the subthreshold regime arise from the smooth and uniform nature of the doping profile where no imperfections, such as random dopants or oxide traps, have been considered. Also, in our simulations, an ideal Ω -gate covers the Si channel. This is not the case for the fabricated devices, leading to poorer electrostatic integrity.

This agreement is obtained by choosing a combination of the low-field mobility (LFM), perpendicular field-dependent mobility (PFDM), and lateral field-dependent mobility (LFDM) models. Masetti *et al.* [36] doping-dependent model is used for the LFM. Yamaguchi [37] and Caughey and Thomas [38] models are then employed to compute the PFDM and LFDM. Calibration of the critical electric field (F_c) and saturation velocity (v_{sat}), respectively, for the last two models was carried out for the JL transistor

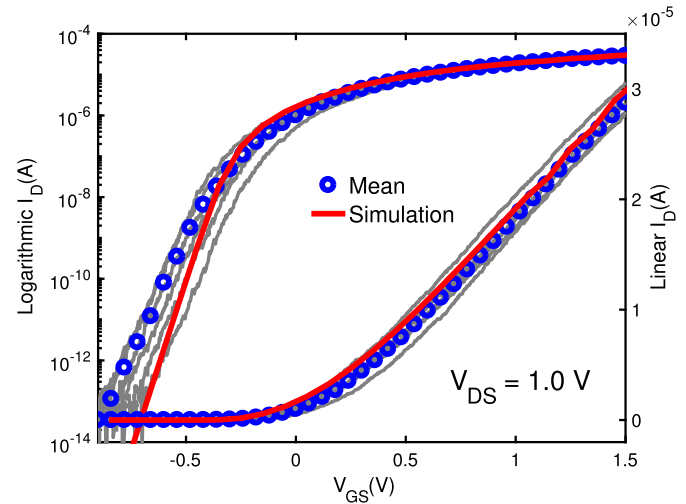


Fig. 2. Comparison of experimental and simulated (red line) $I_D - V_{GS}$ characteristics of the JL transistor shown in Fig. 1. Gray lines: experimental $I_D - V_{GS}$ characteristics from six different devices. Blue dotted curve: corresponding mean value. The gate length and oxide thickness are $L_{CH} = 150$ and 16 nm, respectively. For calibration purpose, the Si region is uniformly doped with $N_D = 10^{19}$ cm⁻³. $I_D - V_{GS}$ characteristics are shown for (a) high $V_{DS} = 1.0$ V and (b) low $V_{DS} = 5$ mV. The calibration procedure is explained in Section III.

at high $V_{DS} = 1.0$ V. It was found that $F_c = 5 \times 10^7$ cm/V, whereas v_{sat} was set to 5×10^8 cm/s. The same values were used to simulate the JL transistor at low $V_{DS} = 5$ mV, resulting in good agreement with the experimental measurement. It is worth mentioning that the values of these parameters are not universal. They might depend, for example, on the device dimensions as well as the doping concentration. They were kept fixed, however, for the simulations of JL transistors with random distributed dopants, presented in Section VI.

IV. RESULTS

Fig. 3 shows the impact of the random dopant distribution (RDD) on current–voltage ($I_D - V_{GS}$) characteristics at high drain bias. For the purpose of this analysis, 500 JL-NWTs with different RDDs were simulated. In all devices, the channel length was kept constant at $L_{CH} = 150$ nm and the oxide thickness is also fixed at 16 nm. The only difference for each device was the position and the number of the RDD in the source, the drain, and the channel. Based on the data presented in the Fig. 3, the following conclusions can be derived.

First, the ratio between the lowest and highest OFF-current (I_{OFF}) is 10^9 or nine orders of magnitude. This variation in the values of the I_{OFF} current can be explained by establishing a correlation between the number and the position of the RDD in the Si region of their corresponding JL-NWTs. However, in case of the device with highest OFF-current, the dopants are equally spread all along the length of the Si body, as shown in Fig. 4(a). However, in the devices with the lowest I_{OFF} current, the dopants are more localized, forming clusters. In Fig. 4(b), one can observe dopants conglomerate in three well-defined groups in the source, in the beginning of the channel, and in the drain regions, leaving two isolated dopants at the channel–drain interface. In this case, the electrons coming

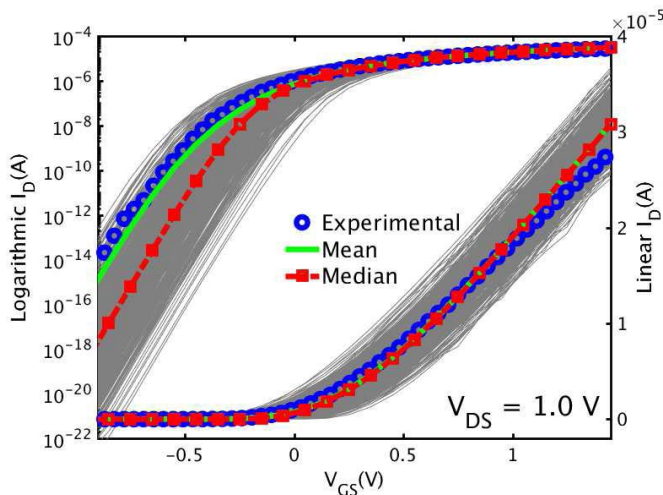


Fig. 3. I_D - V_G characteristics of over 500 JL transistors with random distributed dopants (gray curves). Dotted circle: experimental mean. Green line: statistical mean. Red dashed line: median. The last two are identical in the high gate bias region, e.g., $V_G > 0$ V, and in good agreement with the experimental data. Within the subthreshold regime, the statistical mean current remains closer to the experimental measurements. The gate length is 150 nm whereas the oxide thickness is set to 16 nm in all devices. The doping concentration is as high as $N_D = 10^{19} \text{ cm}^{-3}$.

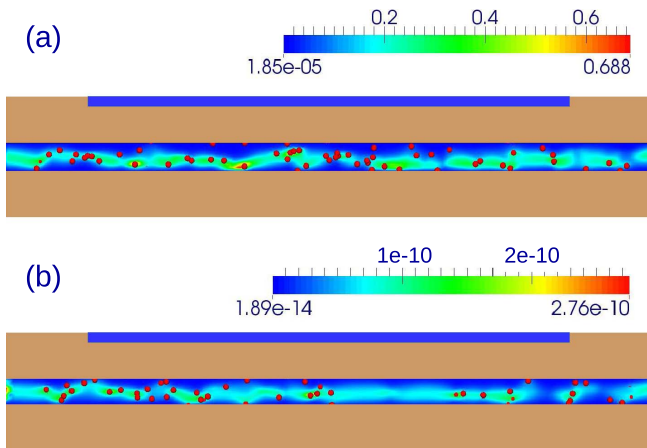


Fig. 4. Simulated 3-D dopant position and current density contours corresponding to JL transistors with (a) highest and (b) low OFF-currents. Current density units are $\text{A}/\mu\text{m}^2$. In case of the device with highest OFF-current, the dopants are more spread all along the Si channel, whereas for its counterpart in (b), dopants conglomerate in three well defined groups in the source, beginning of the channel, and drain regions, leaving two isolated dopants at the channel/drain interface. Such configuration generates less channels for electrons to go through the drain as observed in the current density contours, leading to lower OFF-state currents.

from the source need to overcome a higher potential barrier in this part of the transistor in comparison to the previous devices shown in Fig. 4(a), which is leading to a lower OFF-state current.

The corresponding current density contours shown in Fig. 4 reveal the percolation path which the electrons are kept moving from the source to the drain. Please note that the current flows is localized in the middle of the device which is exactly what is expected as the Fermi wavelength is 18.7 nm [31]. Also, even though the two currents flow look very similar, the difference in the current density between the both devices is almost 10 orders of magnitude. Another difference between the two

JL-NWTs is the total number of the RDD. The transistor with the highest OFF-current has 114 RDD in comparison with 73 RDD in the lowest OFF-current device. The actual number of dopants in each of the 500 JL transistors is chosen randomly from a Poisson distribution, with the mean equal to the experimental doping concentration. The dopants are then placed randomly using a probability rejection technique implemented in the transport tool employed for this paper. The reader can find more details about the approach in [35] and [39]. Moreover, in the highest I_{OFF} nanowire, the dopants are distributed in such a way that they provide an almost continuous percolation path for the electrons from the source to the drain. This leads to enhancement of the I_{OFF} .

Fig. 3 also compares the simulated median and mean and the experimental mean $I_D - V_G$ characteristics. Both simulated median and mean currents are technically identical in the high bias region of the V_G range and in agreement with the experimental mean value of the current. When reaching the subthreshold region, the mean $I_D - V_G$ characteristic deviates from its median counterpart. The mean current, however, remains in good agreement with the experimental data over the entire V_G range shown in Fig. 3. Moreover, compared to the $I_D - V_G$ curve for uniformly doped transistor (Fig. 2), the simulated mean $I_D - V_G$ characteristic reproduces better the experimental mean current within the subthreshold region. Hence, for this specific JL-NWTs, the “smooth” device, which is based on continuous doping, is further away from the experimental mean current in comparison to the mean device. For this reason, all comments and discussions of the results in this section are based only on the mean value of the $I_D - V_G$ characteristics. Moreover, the excellent match between the mean value device and the experimental data proves that statistical simulations are indeed necessary to accurately reproduce the experimental results in such ultrascaled devices.

Performing statistical simulations could help us to extract valuable information about the process and devices variability. For example, Fig. 5 shows probability distribution functions (PDFs) of some of the most important figures of merit (FoM) for those 500 JL-NWTs in Fig. 3. The PDF describes the probability of a particular event or value occurring. Hence, from the PDF distribution of the subthreshold swing (SS), we could conclude that most of the devices would have SS around their theoretical limit at room temperature, i.e., 60 mV/dec. The PDF corresponding to the ON-current (I_{ON}) shows the devices will deliver I_{ON} close to the experimental value of 2.8×10^{-5} A when the JL transistor is at $V_{\text{DS}} = 1$ V. The OFF-diagonal figures in Fig. 5 show the different correlations between FoMs. For example, subthreshold voltage (V_{TH}) and OFF-current (I_{OFF}) are strongly negatively correlated. Such correlation corresponds to decrease in the I_{OFF} value when the V_{TH} increases and vice versa. Note that the I_{OFF} axes are in log scale to highlight its difference between each device. Partial correlation between the I_{ON} and the other FoM can also be observed, except for the SS. Indeed, the correlation between SS and the rest of the FoM was found to be very low, as demonstrated in the last column of Fig. 5.

Next, we will study how the JL transistors would perform when reducing both the gate length and the oxide thickness.

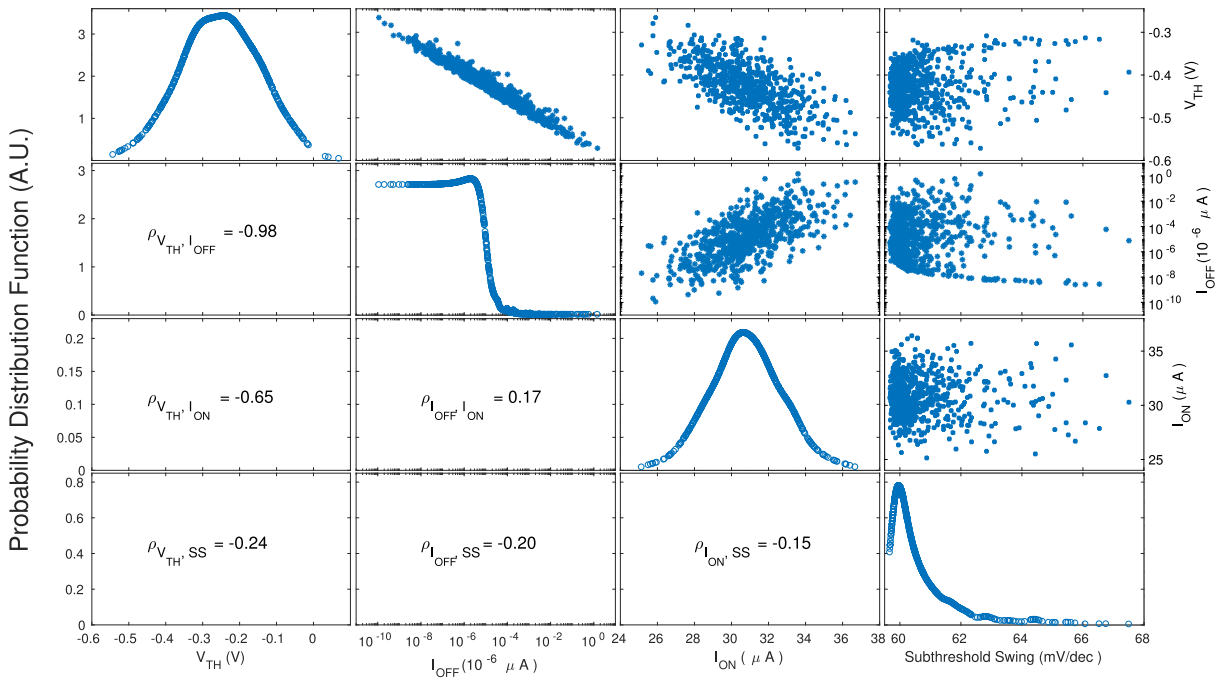


Fig. 5. PDFs and correlation between some of the most important FoM obtained from the simulation of those 500 JL transistors shown in Fig. 3.

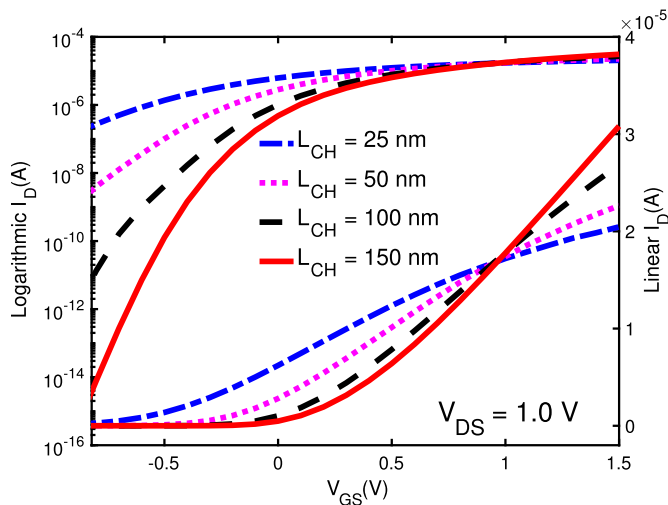


Fig. 6. Mean I_D - V_{GS} characteristics of over 500 JL transistor with different gate lengths varying from $L_{CH} = 150$ to $L_{CH} = 25$ nm. The oxide thickness is fixed to 16 nm.

Over 500 JL transistors with random distributed dopants were simulated for each gate length and oxide thickness. Due to the better agreement with experimental measurements presented for the JL transistor with $L_{CH} = 150$ nm in Fig. 3, only mean $I_D - V_{GS}$ characteristics for the simulated device will be reported from now on.

First, the oxide thickness is fixed to 16 nm, while the gate length is shortened from $L_{CH} = 150$ to $L_{CH} = 25$ nm. The total length of the devices is kept fixed at 200 nm. For example, in the case of the $L_{CH} = 25$ nm device, the gate is exactly in the middle of the channel covering only 25 nm of the 200 nm long nanowire body. The same approach is used for all other gate lengths, where the gate is kept centered in the middle of the device. The corresponding mean $I_D - V_{GS}$ characteristics for four different gate lengths are plotted in Fig. 6. From

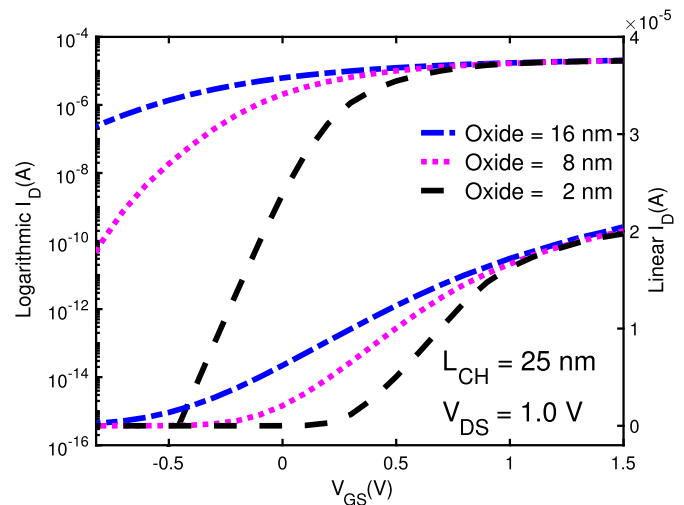


Fig. 7. Mean I_D - V_{GS} characteristics of over 500 JL transistor with different oxide thickness varying from 16 to 2 nm. The gate length is fixed to $L_{CH} = 25$ nm.

the data, it is clear that the JL transistor performance is deteriorated when the gate length is reduced. The main reason is that by reducing the gate length, the electrostatic control is lost, leading to less steep $I_D - V_{GS}$ characteristics with lower ON-current. In the worst case scenario, shown here, the ON-current is reduced by 30%, while the SS increases up to approximately 200 mV/dec for transistors with $L_{CH} = 25$ nm. Second, the crossings of the $I_D - V_{GS}$ curves at around $V_{GS} = 1.0$ V occur due to the fact that when the gate length is decreased the wire behaves as a resistor. This can be compared to adding two resistors on both sides of the gate where the resistance increases with shortening the gate length.

Fig. 7 reports the mean $I_D - V_{GS}$ characteristics of JL transistors with $L_{CH} = 25$ nm and oxide thickness varying from

16 to 2 nm. A performance comparable with the fabricated JL transistor is predicted for the device with the thinnest oxide, showing the steepest slope with SS close to 60 mV/dec and the I_{ON}/I_{OFF} ratio is greater than 10^8 . No improvement of the ON-current is observed. Hence, decreasing in the oxide thickness could indeed improve significantly the device behavior and allow the technology to be scaled down at least $L_{CH} = 25$ gate lengths. Finally, similar qualitatively results for correlations between the FoMs for JL-NWT with different gate lengths and oxide thickness were obtained.

V. CONCLUSION

In this paper, we report an investigation of JL-NWTs from the experimental and computational point of view. The experimental data revealed that JL devices with an 8-nm cross section and a 150-nm gate length demonstrate excellent transistorlike behavior with an SS of 66 mV/dec and a 10^8 I_{ON}/I_{OFF} ratio. All simulations in this paper were carried out using a DD solver, including DG quantum corrections. Agreement with experimental measurements was found after a careful calibration of mobility models.

A simulation study was performed to establish important device parameters and FoMs. This was achieved by simulating an ensemble of 500 JL-NWTs with different RDDs where $I_D - V_{GS}$ characteristics for each device were obtained. Based on those $I_D - V_{GS}$ characteristics, the mean and median values were extracted for each ensemble of devices with a different gate lengths. Our simulations showed that the JL-NWTs start to lose their electrostatic integrity when reducing the gate length below 50 nm, degrading their performance, and that some important FoMs, such as the SS, are also effected. High-performance characteristics, however, could be recovered by significantly decreasing the oxide thickness. For example, if the oxide is scaled down to 2 nm, the devices with the shortest gate length of 25-nm gate length still exhibits an excellent I_{ON}/I_{OFF} ratio. We expect these results to allow optimizing nanowire transistors to improve their performance, which could be used for low-power applications and portable metrology.

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