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DETAILED QUANTITATIVE COMPARISON OF HALF-BRIDGE MODULAR MULTILEVEL CONVERTER MODELLING METHODS

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Abstract

This paper presents a detailed comparison of different modelling methods of the half-bridge modular multilevel converter (HB-MMC), namely, switching function, Thevenin equivalent and averaged, considering both MMC implementations (large and reduced number of cells). The theoretical basis that underpins each modelling method are discussed. Offline PSCAD simulations are used to validate user-defined switching function and averaged MMC models against the Thevenin equivalent model provided in PSCAD library for accuracy, considering steady-state and dc fault conditions. Furthermore, the RTDS based real-time simulation results of the user-defined HB-MMC switching function model are validated against the above mentioned offline models, considering steady-state and dc short circuit fault operations. Simulation speed and efficiency of different offline HB-MMC models being studied in this paper are compared. From comprehensive corroboration of different HB-MMC models presented in this paper, it has been found that the averaged, switching function and Thevenin equivalent models produce practically identical results during steady-state and dc faults. In detailed offline and real-time simulation studies where fundamental and harmonic dynamics are of interest, switching function model is found to be faster and computational efficient compared to the Thevenin equivalent model.

1   Introduction

Many multilevel voltage source converter topologies have been proposed [1-5], and significant efforts have been invested in addressing scalability issue of traditional multilevel converters such as the neutral-point-clamped converter and in the improvement of the quality of the output voltage. The development of the modular multilevel converter (MMC) in [6, 7] has enabled the generation of a true sinusoidal voltage from a dc source, without imposing high voltage gradient (dv/dt) or excessive harmonics on the equipment that will be connected to its ac side. The MMC power circuit structure makes its scalability to high-power and high-voltage levels straightforward and suitable for power transmission application, while still able to provide a similar level of reliability and availability that would be expected from the conventional line commutating HVDC converters.

Compared to traditional voltage source converters such as the conventional two-level and neutral-point clamped converters, MMC offers significant advantages, such as high availability, ease of failure management, short construction time, low ac and dc filtering requirements and low semiconductor losses [8-11].

However, the aforementioned performance improvements and high reliability and availability of the MMC are achieved at the expense of increased complexity of the power circuit and the control system. For example, the use of distributed cell in MMC has facilitated good scalability but has resulted in converter with complex dynamics. Traditionally, power system analysis tools are insufficient to representation non-linear nature of power electronic devices, and this problem has been exacerbated with the introduction of self-commutated power electronic devices such as pulse width modulated voltage source HVDC converters and flexible ac transmission systems (FACTS) devices. A large number of cell capacitors and switching elements in each arm of the MMC presents significant simulation challenges, both computationally and in terms of memory allocation.

This paper discusses the main modelling methods for simulation of the MMC, namely, detailed switching, switching function, Thevenin equivalent and averaged models. The aforementioned MMC models are validated by comparing the results of PSCAD offline simulation models (switching function, averaged and Thevenin equivalent MMC models) and that of the real-time RTDS simulation obtained from the user-defined switching function model. This validation includes both implementations of the MMC (reduced and large number of cells per arm, i.e., 20 and 350 cells), and considers normal steady-steady operation and dc short circuit fault, while assuming identical simulation parameters. These offline and real-time simulation results have demonstrated that the developed MMC models are able to replicate the typical behaviour of the MMC under different operating scenarios.

2   Modular Multilevel Modelling Methods

2.1 Detailed switching model

Fig. 1 shows a three-phase HB-MMC, which consists of six arms, with each arm comprising of a chain link between half-bridge cells and an arm inductor. In detailed switching model, each half-bridge cell is described in detail, where each switching device mimics the conduction pattern and switching characteristics of the physical insulated gate bipolar transistor (IGBT) and its freewheeling diode. With the arm current polarities depicted in Fig. 1 is assumed to be positive, the current i_{armUa} (phase A upper arm current as an example) flows in the switch 'S_{mi}' that bypasses the cell capacitor and in its complementary pair, the switch 'S_{xi}' that inserts the cell capacitor into power path as follows:

- When S_{mi} is on and S_{xi} is off, positive arm current flow through the IGBT part of switch S_{mi}, while the negative arm current flows through its diode part.
- When S_{mi} is off and S_{xi} is on, positive arm current flow through the diode part of switch S_{xi}, while the negative arm current flows through its IGBT part.

The detailed switch representation accounts for the turn-on and turn-off times of the switching devices and their on-state and off-state resistances and voltages. Such detailed representation requires stiff solvers with small time steps in order to simultaneously handle a wide range of time constants associated with different dynamics of the MMC and to enable accurate tracking of the switching voltage edges which are critical for the preservation of different frequency components of the ac and dc side waveforms. However, the main penalties of this modelling method are long simulation times and high computation burden as it creates a large number of electrical nodes (large admittance matrices and their inversion presents a significant computational challenge). In summary, the above discussions highlight the need for the development of accurate and computationally efficient MMC models.
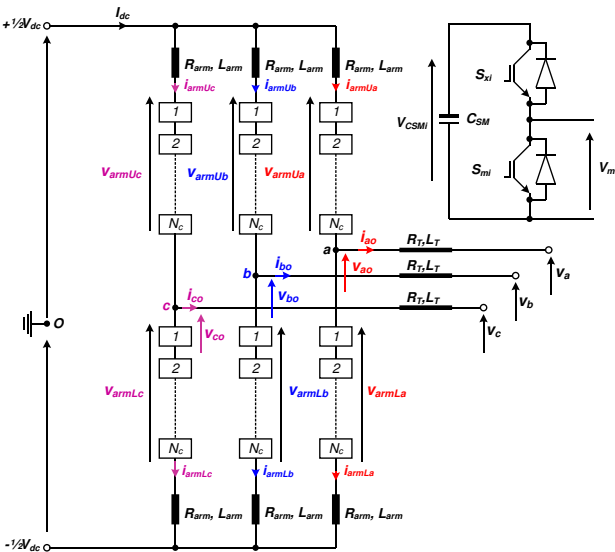

Fig. 1 Basic structure of MMC and detailed model

2.2 Averaged model

The development of the MMC averaged model is driven by the need to have computationally efficient model suitable for a wide range of power system studies. To achieve this objective, the following assumptions are made:

- The switched voltages across the upper and lower arms of each phase are replaced by their average voltages, which can be expressed as:

$$V_{armU} = \sum_{j=1}^{N_{SM}} V_{CSMU} S_{xj} \approx \tfrac{1}{2} V_{carmU} \left[1 - m\sin(\omega t + \delta)\right] \approx V_{carmU} m_U \tag{1}$$

$$V_{armL} = \sum_{j=1}^{N_{SM}} V_{CSML} S_{xj} \approx \tfrac{1}{2} V_{carmL} \left[1 - m\sin(\omega t + \delta)\right] \approx V_{carmL} m_L \tag{2}$$

- The inter-cell dynamics in each arm is neglected; thus, the cell capacitor voltages of each arm oscillate together. So, the upper and lower arms of each phase leg present variable capacitance $C_{armU} = C_{SM}/N_U$ and $C_{armL} = C_{SM}/N_L$; where the number of cell capacitors that the upper(N_U) and lower(N_L) arms insert into power path can be approximated by:

$$N_U \approx \tfrac{1}{2} N_{SM} \left[1 - m\sin(\omega t + \delta)\right] \approx N_{SM} m_{aU} \tag{3}$$

$$N_L \approx \tfrac{1}{2} N_{SM} \left[1 + m\sin(\omega t + \delta)\right] \approx N_{SM} m_{aL} \tag{4}$$

- Using the definitions in (3) and (4), the dynamics of the upper and lower cell capacitors can be approximated as:

$$\frac{C_{SM}}{N_U} \times \frac{d}{dt} V_{carmU} \approx i_{armU1}$$

$$\Rightarrow \frac{C_{SM}}{N_{SM}} \times \frac{d}{dt} V_{carmU} \approx \tfrac{1}{2}\left[1 - m\sin(\omega t + \delta)\right] i_{armU1} \tag{5}$$

$$\Rightarrow C_e \times \frac{d}{dt} V_{carmU} \approx m_U i_{armU1}$$

$$\frac{C_{SM}}{N_L} \times \frac{d}{dt} V_{carmL} \approx i_{armL1}$$

$$\Rightarrow \frac{C_{SM}}{N_{SM}} \times \frac{d}{dt} V_{carmL} \approx \tfrac{1}{2}\left[1 + m\sin(\omega t + \delta)\right] i_{armL1} \tag{6}$$

$$\Rightarrow C_e \times \frac{d}{dt} V_{carmL} \approx m_L i_{armL1}$$

Where, $C_e = C_{SM}/N_{SM}$ represents the equivalent cell capacitance for each arm, C_{SM} is the cell capacitance, N_{SM} is the number of half-bridge cells per arm and total blocking voltage of the half-bridge cell capacitors in each MMC arm is

$$V_{carm} = \sum_{j=1}^{N_{SM}} V_{CSM,j} \geq V_{dc} .$$ From (5) and (6), the upper and lower

arms equivalent capacitor currents are:

$$i_{capU} \approx C_e \times \frac{d}{dt} V_{carmU} \approx m_U i_{armU1} \tag{7}$$

$$i_{capL} \approx C_e \times \frac{d}{dt} V_{carmL} \approx m_L i_{armL1} \tag{8}$$

Equations (5), (6), (7) and (8) that describe averaged MMC dynamics are repackaged in graphical form, which resembles the MMC averaged model in Fig. 2(a). Fig. 2(b) shows detailed conduction path of the modified averaged model, where the added IGBTs and diodes facilitate recreation of the MMC typical behaviour during blocked and de-blocked states.
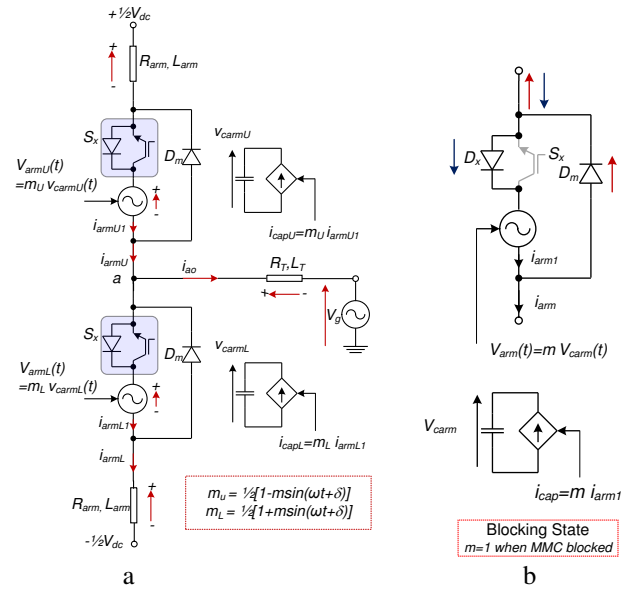
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Fig. 2 MMC averaged model
(a) Depiction based on averaged model for one phase
(b) Blocking state

2.3 Thevenin equivalent model

This modelling method treats HB-MMC switching devices as two-state switched resistors, with on-state and off-state resistances of R_{ON} and R_{OFF} respectively, and where each cell capacitance is replaced by its electromagnetic transient equivalent circuit, see Fig. 3 (a). For a generic cell, the cell capacitor dynamic is expressed as:

$$\frac{dV_{CSMi}(t)}{dt} = \frac{I_{ci}(t)}{C_{SM}} \tag{9}$$
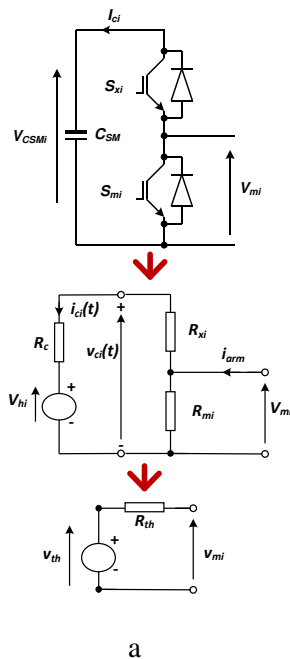
Fundamentally, the electromagnetic transient simulation pre-solves all the differential equations using standard numerical integration methods such as Backward Euler and Trapezoidal. For example, after solving (9) using trapezoidal integration method, the following equation is obtained:

$$\begin{aligned} V_{CSMi}(t) &= V_{CSMi}(t-\Delta t) + \tfrac{1}{2}\frac{\Delta t}{C_{SM}}\left[I_{ci}(t) + I_{ci}(t-\Delta t)\right] \\ &= V_{CSMi}(t-\Delta t) + R_c I_{ci}(t-\Delta t) + R_c I_{ci}(t) \\ &= V_{hi} + R_c I_{ci}(t) \end{aligned} \tag{10}$$

Where, the term that represents the calculations in the previous time step is denoted as history term $V_{hi} = V_{CSMi}(t-\Delta t) + R_c I_{ci}(t-\Delta t)$, and $R_c = \dfrac{\Delta t}{2C_{SM}}$ represents the electromagnetic transient fictitious equivalent resistance of the cell capacitance. Fig. 3(a) depicts equivalent circuit of the half-bridge cell with Backward Euler and Trapezoidal integration methods, and which is further reduced using Thevenin theory, with the Thevenin voltage and resistance per cell are:

$$V_{mi}(t) = \frac{R_{mi}}{R_c + R_{xi} + R_{mi}} \times V_{hi} \tag{11}$$

$$R_{thi} = \frac{R_{mi}(R_c + R_{xi})}{R_c + R_{xi} + R_{mi}} \tag{12}$$

The switched voltage to be developed across each HB-MMC arm can be calculated by:

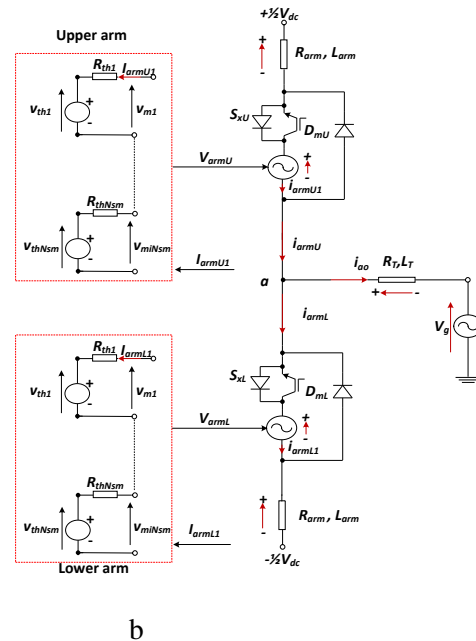$$V_{arm} = \sum_{i=1}^{N_{SM}} V_{mi} \tag{13}$$

Fig. 3 Thevenin equivalent model
(a) Depiction of the HB-MMC model based on Thevenin equivalent circuit of a half-bridge cell
(b) Depiction of the MMC model based on Thevenin equivalent circuit of phase A of the half-bridge cells

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Fig. 3(b) shows the block diagram of one MMC phase-leg, where arms are modelled using the Thevenin equivalent circuit, and modified to be able to mimic the typical MMC behaviour during blocking and de-blocking. Handling of blocking state during dc fault in the Thevenin equivalent HB-MMC model is similar to that of the averaged HB-MMC model described earlier.

2.4 Switching function model of HB-MMC

This modelling method represents the MMC semiconductor switching devices by ideal switches, where their on and off states are denoted by 1 and 0 respectively as shown in Fig. 4(a) [12]. The switched output voltage of a single half-bridge cell can be expressed in terms of its cell capacitor voltage using the state of the switch S_{xi} as:

$$V_{mi}(t) = S_{xi}V_{CSMi}(t) \qquad (14)$$

Similarly, the switched cell capacitor current of each cell can be related to MMC arm current by:

$$i_{ci}(t) = S_{xi}I_{arml}(t) \qquad (15)$$

The cell capacitor voltage can be calculated at each time step as

$$V_{CSMi}(t) = \frac{1}{C_{SM}}\int i_{ci}(t)dt \qquad (16)$$

Equation (16) is transformed into discrete arm voltage similar to Thevenin equivalent model. The total switched voltage across each MMC arm is:

$$V_{arm} = \sum_{i=1}^{N_{SM}}V_{mi} = \sum_{i=1}^{N_{SM}}S_{xi}V_{CSMi} \qquad (17)$$

Fig. 4(b) depicts switching model of the HB-MMC, which is developed from (15), (16) and (17). As the switching function modelling method ignores the conduction pattern and switching characteristics of physical semiconductor switching devices, without the inclusion of the composite switches S_{xU} and S_{xL}, and diodes D_{mU} and D_{mL} shown in Fig. 4(b), it will be unable to simulate the blocking state of the HB-MMC during normal operation and dc faults.

3 Control Systems

Fig. 5 depicts a generic control block diagram of the HB-MMC. Since the d-axis is aligned with the voltage vector at PCC, this means the direct and quadrature currents represent active and reactive power components respectively. Therefore, the outer controllers that set the active power and dc voltage orders are implemented on d-axis. Conventionally, one converter terminal of point-to-point HVDC link controls the dc voltage level, while the other regulates the active power. Similarly, the outer controllers that regulate reactive power or ac voltage are implemented on q-axis. Therefore, the active power/dc voltage and reactive power/ac voltage set the positive sequence direct and quadrature current orders respectively. The negative sequence direct and quadrature current orders are set to zeros (which indicate elimination of any negative sequence currents that may arise during operation under unbalanced grid voltage or asymmetric ac faults).
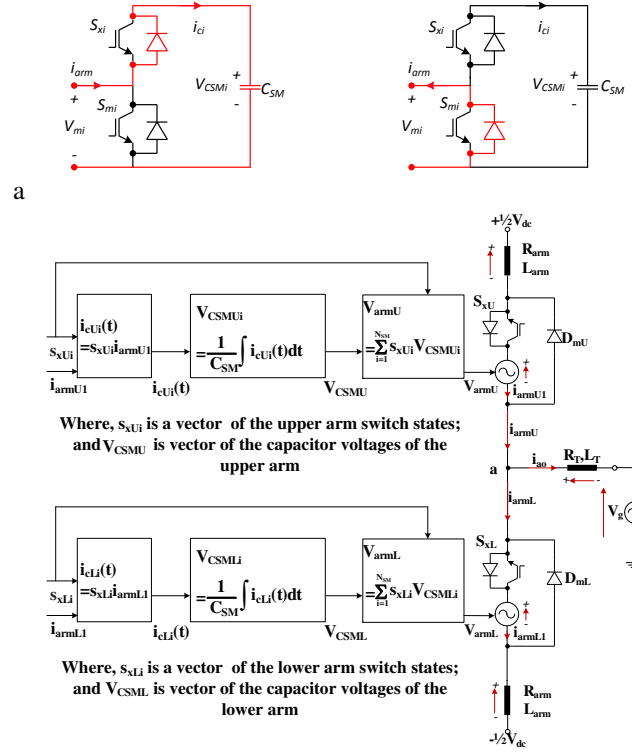

a

b

Fig. 4 Depiction of the HB-MMC switching function model
(a) On and Off states of a cell
(b) Switching function depiction of a single phase

The inner current controllers regulate both positive and negative sequence currents during normal operation and limit the MMC current contribution to ac fault and generate the principle ac modulating signals (phase and magnitude). Active circulating current suppression controller is used to suppress the 2nd order harmonic currents in the MMC arm currents in order to reduce the semiconductor power losses and cell capacitor voltage ripples. This supplementary controller slightly modifies the principle modulating signals. The average cell capacitor voltage controller facilitates regulation of half-bridge cell capacitor voltages independent of the MMC dc link voltage, and this improves MMC dynamic response as a change of the active power or dc voltage orders do not require the changes in the cell capacitors energy levels. This controller introduces a minor modification to the principle modulation signals, particularly, their dc components. The most inner controller is the implementation of the non-distributed cell capacitor voltage balancing and modulator that ensure the total voltage across each MMC arm is equally shared between the cell capacitors of the arm and generate the desired arm and output voltages by selecting appropriate number of cell capacitors to be inserted into power path and bypassed in each instant.
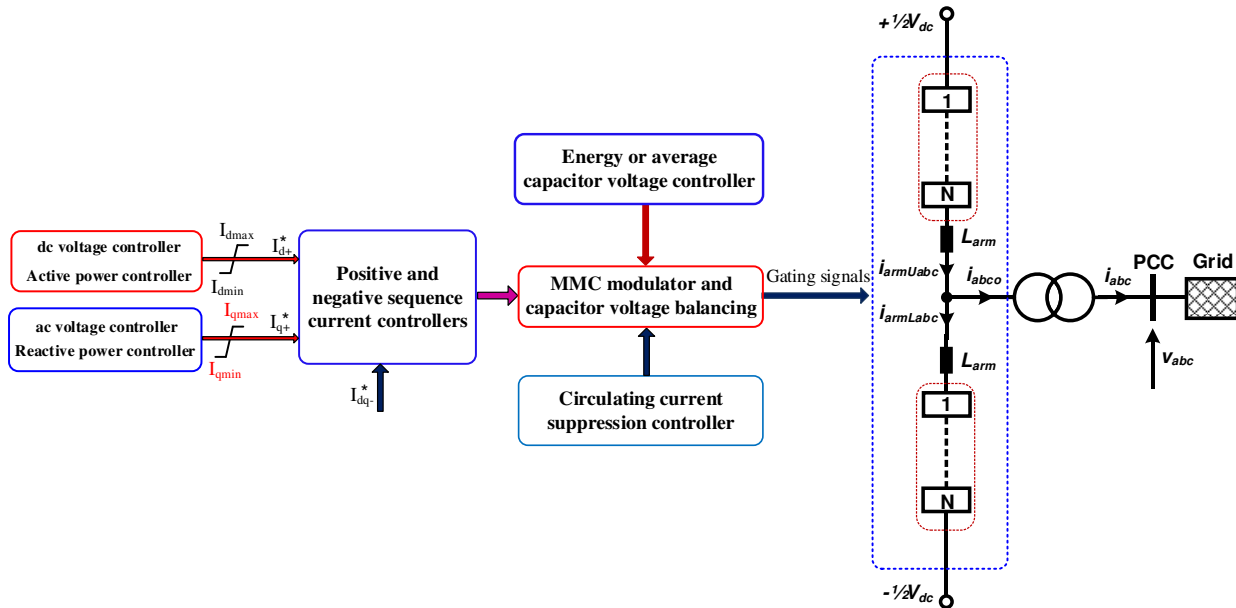
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Fig. 5 Control block diagram of the MMC

4 Test System

This section uses one converter terminal of the MMC based point-to-point HVDC link to validate the offline and real-time HB-MMC models presented earlier, particularly, the averaged, switching function and Thevenin equivalent. The simulated converter station is equipped with the controllers summarized in Fig. 5.

Detailed system parameters are listed in Table 1. The cell capacitances of the 20-cell and 350-cell HB-MMC models and averaged HB-MMC model are calculated, assuming the same minimum inertia constant of 30ms (or 30kJ/MVA) as suggested in [13, 14].

Table 1 Test system parameters

Parameters		Value
MMC rated apparent power (Sn)		1265MVA
MMC rated active power (P)		±1200MW
MMC rated reactive power(Q)		±400MVAr
MMC nominal dc Voltage (V_{dc})		640kV(±320kV)
MMC rated ac output voltage (L-L)		360kV
Arm inductance (L_{arm})		0.13pu
Cell capacitance (C_{SM})	20-cell MMC	628µF
	350-cell MMC	11mF
	Averaged model	31.4µF
Nominal Frequency		50Hz
Transformer rated apparent power		1265MVA
Interfacing transformer voltage ratio		400/360kV
Transformer leakage reactance		0.18pu
Transformer resistance		0.004452pu

On the basis of section 2.4, a 20-cell switching function model based HB-MMC model with parameters listed in Table 1 is built on RSCAD-RTDS simulation platform and validated against the offline HB-MMC averaged, switching function and Thevenin equivalent models developed on PSCAD-EMTDC.

As in PSCAD, the switching function model in RTDS consists of two parts, namely, the power circuit part which includes controllable voltage sources, arm inductors and IGBTs and diodes being used to mimic the HB-MMC blocking state (see Fig. 4); and the calculation part that simulates the HB-MMC cell dynamics and generates the upper and lower arm voltages V_{armU} and V_{armL}. In the RTDS implementation, the power circuit part of the switching function model and its associated components such as the ac grid and interfacing transformer are placed in a dedicated template for small time step provided by RSCAD library, and time-step of 2.5µs is used in this part. While the part that calculates the cell capacitor dynamics and control systems are placed in a dedicated template for large time step that adopts 50µs as the time step. The user-defined components that implement calculations of cell capacitor dynamics and voltage balancing are first realized in MATLAB-SIMULINK and then converted to RSCAD. The real-time simulation model of the whole system described above is implemented on one RTDS rack, with a PB5 card (with 2 PB5 processors) and 2 GPC cards (4 GPC processors). Both processors on the PB5 card are assigned to solve the power circuit that operates at a small time step, and with calculation part of each phase on one GPC processor.

5 Accuracy Validation

5.1 Normal operation.

This section validates the offline and real-time HB-MMC models described above (Thevenin equivalent 'PD', switching function 'SF' and averaged 'Avg' models), considering both HB-MMC implementations (20 cells and 350 cells as representatives for reduced and large number of

cells per arm). The offline PD models which are based on the PSCAD library are assumed to be reference models. The system operation conditions during the validations are summarized as follows.

- The HB-MMC is assumed to operate as an active power controller with unity power factor at the point-of-common-coupling (PCC).
- Initially, HB-MMC maintains its active power output at zero, and at t=1s, it ramps its active power output from 0 to 1200MW.
- The sum of the cell capacitor voltages of each HB-MMC arm is regulated at 640kV.
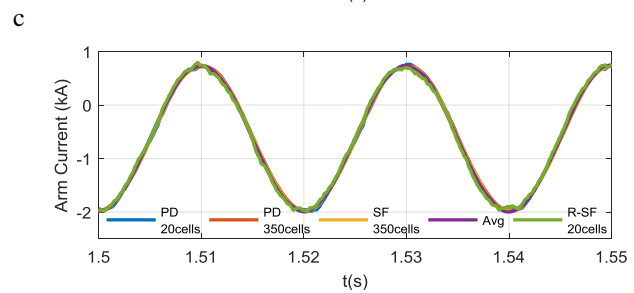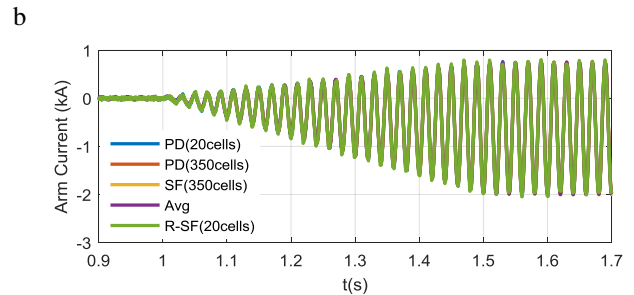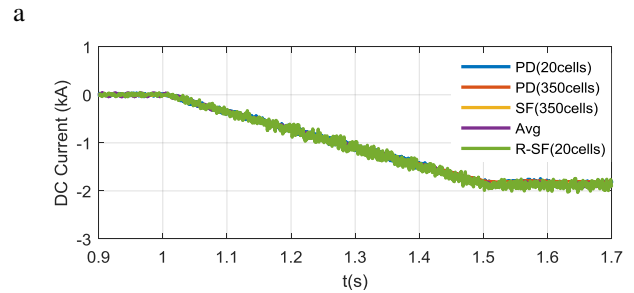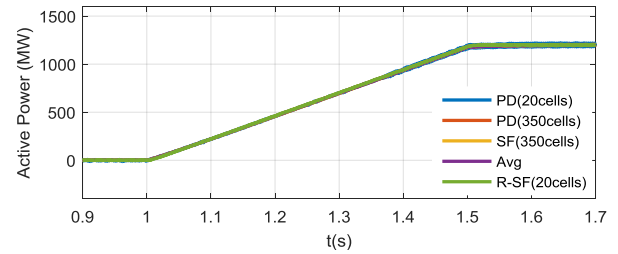
The offline and real-time simulation waveforms during normal operation are displayed in Fig. 6 with the traces of the 'SF' and 'Avg' HB-MMC models superimposed on that of the PD models. Fig. 6(a) and (b) show the active power at PCC (the positive power flow is from ac to dc side) and dc link current (with the dc current corresponding to 1200MW is 1.875kA, and positive dc current direction is from the converter to dc side direction). Phase A upper arm current and its zoomed version are displayed in Fig. 6 (c) and (d). The traces for the phase A upper capacitor voltage sum, and common and differential capacitor voltage sums are shown in Fig. 6 (e), (f) and (g). These offline and real-time waveforms indicate the followings:

- During normal operation, the user-defined HB-MMC averaged and switching function models produce practically identical results as that of the Thevenin equivalent of the PSCAD library (active power, dc link currents and arm currents).
- All the models being compared are able to reproduce the asymmetry of the arm current 'i_{armUa}' and dynamics of its both principal components, i.e., the dc component 'I_d^a' which equals to one third of the dc link current 'I_{dc}' and fundamental current '$\frac{1}{2}i_{ao}$', with circulating current component well suppressed.
- All the models being compared are able to reproduce practically identical capacitor voltage sums, including inter-dynamics between the upper and lower arms of the same phase-leg that introduce fundamental and 2nd harmonics in the differential and common-mode capacitor voltage sums, $V_{carmL} - V_{carmU}$ and $\frac{V_{carmL} + V_{carmU}}{2}$.
- With the same controllers, the HB-MMCs with a reduced and large number of cells per arm produce identical output power, dc link current and arm currents. This conclusion is confirmed by all HB-MMC models being compared.

5.2 Pole-to-pole DC short circuit fault.

This section presents offline and real-time validations of the HB-MMC averaged and switching function MMC models against that of the Thevenin equivalent model of the PSCAD library, considering the dc short circuit scenario, and HB-MMCs with 20 and 350 cells per arm. The system operating conditions during these validations are summarised as follows:

- The HB-MMC operates as a dc voltage controller with dc load equivalent to 1200MW and unity power factor at PCC.
- At t=2s, a permanent pole-to-pole dc short circuit fault is applied, and converter blocking is activated after 50µs from dc fault inception.
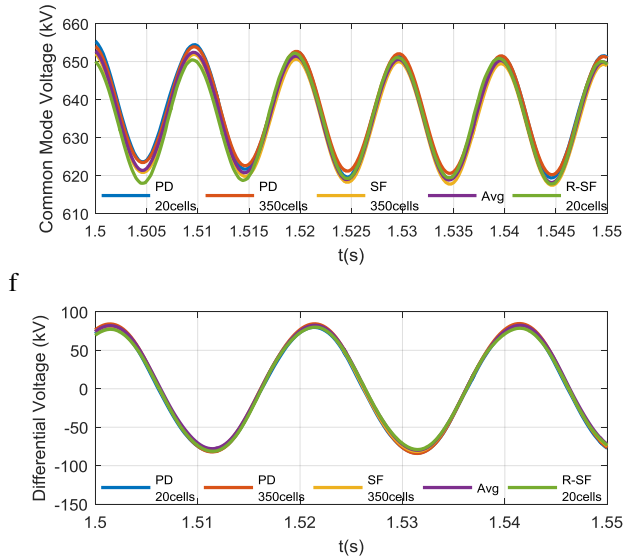

a

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c

d

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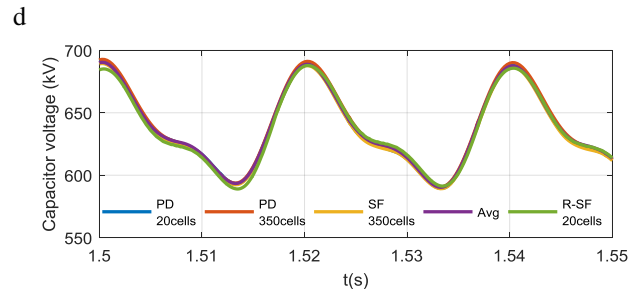
Fig. 6. Normal operation simulation waveforms of the HB-MMC when active power is ramped from 0 to 1200MW within 0.5s, with the results of the offline simulations ('PD' with 20 and 350 cells, 'SF' with 350 cells and 'Avg') superimposed on that of the real-time simulation with 20-cell 'R-SF'.

(a) Active power 'P'

(b) DC current 'I$_{dc}$'

(c) Phase A upper arm current 'i$_{armUa}$'

(d) Snapshot of phase A upper arm current 'i$_{armUa}$'

(e) Snapshot of phase A upper capacitor voltage sum 'V$_{carmUa}$'

(f) Snapshot of phase A common-mode capacitor voltage sum

(g) Snapshot of phase A differential-mode capacitor voltage

Fig. 7 displays the offline and real-time simulation waveforms that illustrate the responses of different HB-MMC models being compared for a solid pole-to-pole dc short circuit fault. The traces of pole-to-pole dc link voltages and currents displayed in Fig. 7(a) and (b) indicate that all the HB-MMC models being compared produce practically identical fall in the dc link voltage and an identical rise in the dc link arm currents, independent of the selection of the number of cells per arm. The plots in Fig. 7(c) show that after converter blocking is activated (50µs from dc fault inception) the upper arm currents become unipolar. This indicates that the two components of arm currents during dc fault period flow through the freewheeling diodes of the switches that bypass the cell capacitors, with the ac current in-feeds flow from the ac grid towards the dc side, and the dc fault current flows from the negative dc pole to positive dc pole through the inner common-mode path that includes the HB-MMC lower and upper arms. These typical HB-MMC behaviours have been reproduced by all MMC models being compared, in offline and real-time, and independent of the number of cells. The plots in Fig. 7 (d) show that the cell capacitor voltages produced by all models being compared are practically similar, with the sum of the cell capacitor voltages of different HB-MMC models exhibit slightly different magnitudes but the same trends during normal operation and

dc fault when the converter is blocked, with worst-case margin of errors remaining less than 2%.
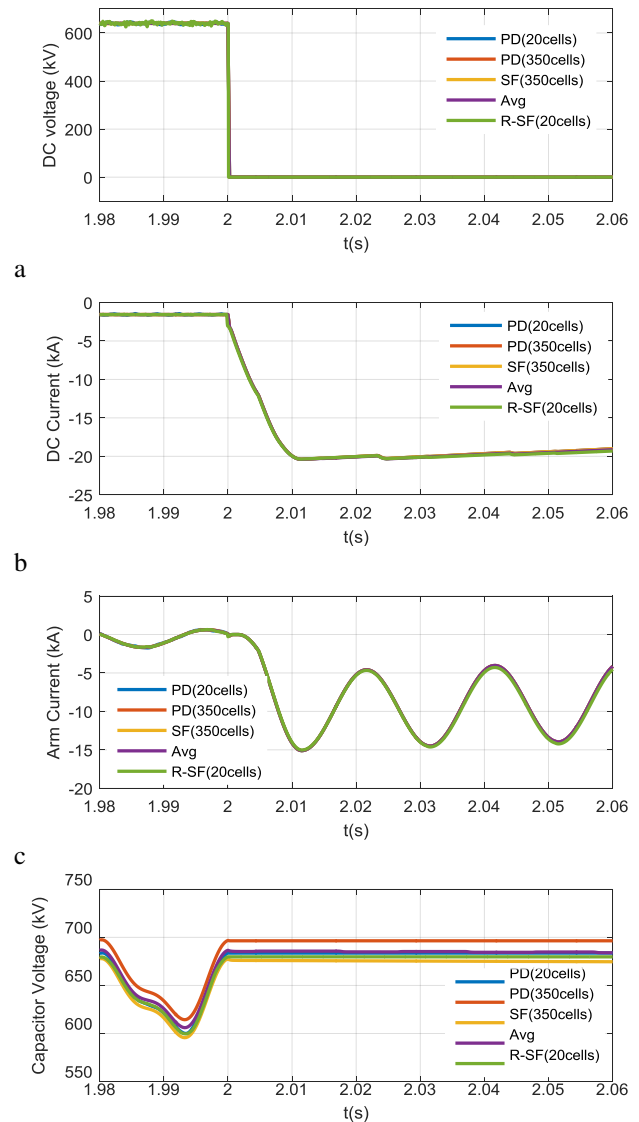

a

b

c

d

Fig. 7. Simulation waveforms that illustrate the behaviours of switching function 'SF' and averaged 'Avg' HB-MMC models against that of the Thevenin equivalent 'PD' HB-MMC model during dc short circuit fault, including effect of number of cells per arm on system performance

(a) DC voltage 'V$_{dc}$'

(b) DC current 'I$_{dc}$'

(c) Phase A upper arm current 'i$_{armUa}$'

(d) Sum of capacitor voltages of phase A upper arm

6   Efficiency Comparison

Simulation efficiencies of different HB-MMC models being compared are summarized in Table 2. Table 2 summarises the simulation time of different HB-MMC models being compared when they are configured as a terminal converter of a point-to-point HVDC link, with all controllers stated earlier are incorporated, for 1-second simulations. These simulations were conducted using PSCAD 4.6 on HP

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computer with Intel(R) Core(TM) i7-6700 CPU @ 3.4GHz, 16GB RAM and 64-bit Windows 10 Enterprise system.

From the results displayed in Table 2 (a) to (f), it is clear that the averaged HB-MMC model is the most efficient and followed by the switching function and then Thevenin equivalent, while detailed switching model is less efficient (the slowest and with the largest number of electrical nodes).

Table 2 Simulation time of different HB-MMC models

Result	Model type	No. of cells	Execution time
(a)	Averaged	256	1.7s
(b)	Switching function	256	3.64s
(c)	Thevenin equivalent	256	5.15s
(d)	Thevenin equivalent	20	2.7s
(e)	Switching function	20	1.84s
(f)	Detailed switching	20	4mins26s

7   Conclusion

This paper has presented a number of modelling methods of the HB-MMC, including the theoretical basis that underpins each modelling method, and basic assumptions made in the development of each method. The comprehensive comparison of the offline and RTDS based real-time simulation waveforms presented in this paper reveal that the averaged and switching function HB-MMC models produce practically the same results as that of the Thevenin equivalent MMC model of the PSCAD MMC library, but with much greater simulation efficiency. This conclusion is valid for a wide range of studies, including normal steady-state operation and faults. Similar voltage and current stresses are observed on the MMC active and passive components.

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