Microelectronics Reliability 84 (2018) 55–65

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Comparison of power cycling reliability of flexible PCB interconnect smaller/thinner and larger/thicker power devices with topside Sn-3.5Ag solder joints

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ARTICLE INFO

Keywords:
Reliability
Planar interconnect
Power semiconductor
Finite element method
Power cycling
Sn-3.5Ag solder alloy
Scanning electronic microscopy

ABSTRACT

The power cycling reliability of flexible printed circuit board (PCB) interconnect smaller/thinner (ST) 9.5 mm × 5.5 mm × 0.07 mm and larger/thicker (LT) 13.5 mm × 13.5 mm × 0.5 mm single Si diode samples have been studied. With the assumption of creep strain accumulation-induced fatigue cracking as the failure mechanism of the Sn-3.5Ag solder joints, finite element (FE) simulations predicted a higher power cycling reliability of soldering the flexible PCB on a ST Si diode than on a LT Si diode under similar power cycling conditions. Then the power cycling test results of 10 samples for each type are reported and discussed. The samples were constructed with commercially available ST Si diodes with 3.2/0.5/0.3 μm thick AlSiCu/NiP/Pd topside metallization and LT Si diodes with 5/0.1/1/1 μm thick Al/Ti/Ni/Ag topside metallization. In contradiction with the FE prediction, most ST Si diode samples were less reliable than those LT Si diode samples. This can be attributed to the fact that the failure of the ST diode samples was associated with the weak bonding and hence the shear-induced local delamination of the topside solder joints from the AlSiCu metallization, while the failure of the LT diode samples was mainly caused by the creep strain accumulation-induced fatigue cracking within the solder joints. Such results can be used to not only provide better understanding of the different failure mechanisms, but also demonstrate the importance of employing an appropriate topside metallization on the power devices.

1. Introduction

The planar interconnect power modules have been promising to replace the conventional Al wire and Cu bus bar interconnect power modules for obtaining dramatic improvements in both thermal and electromagnetic performance due to their better ability to dissipate heat and reduce parasitic inductance [1–4]. However, work in the selection of materials, manufacturability and reliability for the implementation of efficient and low cost planar interconnect technology is still needed for wider acceptance and commercialization. For example, metal/composite bumps and flexible printed circuit boards (PCBs) have been bonded on the topsides of Si or SiC power devices and ceramic-based substrates to form the planar interconnect structures [5–9]. The joints were produced using the conventional Sn-based solder alloys, i.e. eutectic or near eutectic Sn-Ag or Sn-Ag-Cu solder alloys, or the emerging Ag sintering technology. Because of the mismatch in coefficients of thermal expansion (CTEs) between the interconnect materials and the power devices and the substrates, thermal stress and inelastic strain develop in the joints during the assembling process and in the subsequent service environments. As a result, inelastic strain/work accumulation may lead to initiation and propagation of cracks in the joints making them as potentially thermo-mechanical weak points in the assembled planar interconnect power modules.

In the previous work on double side cooled planar power modules [8], Cu/Mo/Cu composite bumps were used to reduce the CTE of the pure Cu bumps soldered on the Si power devices (with Sn-3.5Ag). The improved reliability of the soldered bump interconnects was verified through thermal cycling test between −55 °C and 150 °C. In another work [10], Si_3N_4 ceramic-based structure with through vias designed and filled with brazing alloy was proposed as CTE-constrained planar interconnect solution in planar power modules. The improved reliability in comparison with the flexible PCBs soldered on the similar Si power devices (with Sn-3.5Ag) was demonstrated with power cycling tests with junction temperatures between 40 °C and 120 °C. On the other hand, in the planar SKiN interconnect technology by SEMIKRON [5–7], the micro-silver sintered joints rather than the Sn-based solder joints were used to bond the flexible PCBs on the topsides of the power devices for achieving high power cycling reliability.

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https://doi.org/10.1016/j.microrel.2018.03.013
Received 17 December 2017; Received in revised form 3 March 2018; Accepted 11 March 2018

Flexile PCBs are both cost effective for manufacturing and mature for achieving high resolutions of conductive tracks to match the bond pads on the power devices. Under similar thermal conditions, flexible PCB interconnect smaller/thinner (ST) devices can be expected to have reliability higher than similar flexible PCB interconnect larger/thicker (LT) devices. This is because ST devices have lower total stiffness, and thus are easier to deform than LT devices to reduce the thermo-mechanical stress and/or inelastic strain developments in the solder joints or the sintered joints. Therefore, in some cases, the combination of flexible PCBs with ST devices and the Sn-based solder joints may be more cost-effective to assemble the planar power modules with satisfactory thermo-mechanical reliability. On the other hand, the combination of flexible PCBs with ST devices and the sintered Ag joints can be used for higher thermo-mechanical reliability requirement.

The present work compares the reliability of the flexible PCB interconnect ST and LT power devices under similar power cycling conditions, where the Sn-3.5Ag solder joints were used as the device topside joints. By assuming creep strain accumulation-induced fatigue cracking as the failure mechanism of the solder joints, the finite element (FE) modelling and simulation was first carried out to demonstrate the theory that soldering the flexible PCB on a ST 9.5 mm × 5.5 mm × 0.07 mm Si diode is more reliable than soldering a similar flexible PCB on a LT 13.5 mm × 13.5 mm × 0.5 mm Si diode under similar power cycling conditions. The backsides of both the ST and the LT Si diodes were attached on AlN-based substrates also using the Sn-3.5Ag solder joints. Then the samples were constructed with the corresponding ST diodes with 1/0.3/0.3 μm thick AlTi/Ni/Ag backside metallization and 3.2/0.5/0.3 μm thick AlSiCu/NiP/Pd topside metallization and LT diodes with 1/1/1 μm thick AlTi/Ni/Ag backside metallization and 5/0.1/1/1 μm thick Al/Ti/Ni/Ag topside metallization. The power cycling reliability of 10 samples for each type of the two diodes were tested and compared for revealing the different failure mechanisms.

The main objective of this paper is to understand the advantage and issue for the thermo-mechanical reliability of the above flexible PCB interconnect ST Si diode samples over LT Si diode samples. The specific objectives include: (i) to present the FE simulation results predicting that the topside solder joint on a ST Si diode is more reliable than the topside solder joint on a LT Si diode for bonding similar flexible PCBs; (ii) to compare the tested power cycling lifetimes and failure mechanisms of the flexible PCB interconnect ST and LT Si diode samples; (iii) to report the different evolutions of the cycle times, duty cycles and forward voltage drops for the two types of samples during the power cycling tests and explain them with the observed different failure mechanisms; and (iv) to point out the importance of a modified and appropriate topside metallization system for achieving high thermo-mechanical reliability which may have been overlooked in the selection of commercially available ST power devices.

2. Finite element modelling and simulation

2.1. Description of single Si diode samples

In the previous work [10], Sn-3.5Ag solder joints were used to both bond the Si_3N_4 ceramic-based structures and flexible PCBs on the topsides of 13.5 mm × 13.5 mm × 0.5 mm Si diodes and attach the diodes on the AlN-based substrates for forming planar interconnect samples. The stress and creep strain developments in the solder joints in the samples during both the assembling process and power cycling tests with junction temperatures between 40 °C and 120 °C were simulated. In the present work, similar FE modelling and simulation have been carried out on the flexible PCB interconnect ST 9.5 mm × 5.5 mm × 0.07 mm and LT 13.5 mm × 13.5 mm × 0.5 mm single Si diode samples.

Fig. 1 describes a flexible PCB interconnect ST diode sample, where the diode and a same size Cu post are attached on an AlN-based substrate with 100 μm thick Sn-3.5Ag solder joints. The substrate is 58.2 mm × 49.5 mm × 1 mm thick AlN ceramic tile with 0.3 mm thick Cu tracks on both sides. A flexible PCB is soldered on the topsides of both the diode and the post also with 100 μm thick Sn-3.5Ag solder joints. The flexible PCB consists of 100 μm thick polyimide and 50 μm thick Cu tracks on both sides, and the vias (0.5 mm in diameter) are through the bottom Cu tracks and the polyimide layer, and are filled with Sn-3.5Ag solder alloy.

For matching the sizes of the diodes, in one ST diode sample, the flexible PCB is 22 mm × 9.5 mm in size, and contains two matrixes of 9 × 5 ϕ0.5 mm vias in the two 8.5 mm × 4.5 mm bonding pads on the topsides of the Si diode and the Cu post. By contrast, in one LT diode sample, the flexible PCB is 30 mm × 1.5 mm in size, and contains two matrixes of 8 × 8 ϕ0.5 mm vias in the two 8 mm × 8 mm bonding pads.

2.2. FE models and simulation

As in the previous work [10], thermal models were used to simulate the temperature fields of the single diode samples during 50 power cycles. In each sample, the top one third volume of the diode was considered as the active region generating electrical heat. The latter was the product of 50 current pulses with an amplitude of 90 A multiplied by the voltage drop across the diode during the power cycling test. The on-time and off-time of each current pulse were determined by achieving 40 °C and 120 °C as the lower and upper limits of the average temperatures on the hottest 5 mm × 5 mm top surface area on the sample. A heat exchange coefficient of 575 $W{\cdot}m^{-2}{\cdot}k^{-1}$ was applied on the bottom surface of the AlN-based substrate to match the average temperature profile of 10 diode samples during the early stage of the power cycling tests.

In the thermo-mechanical models, the samples were first subjected to a predefined temperature profile of 192 °C down to 25 °C within 3 min to simulate the reflow process. The initial heating up stage of the reflow process was found to have negligible effects on the simulated stress/strain developments in solder joints [8], and was eliminated from consideration. The solidification of the molten Sn-3.5Ag solder generally occurs at a super-cooling temperature of 192 °C [11]. The temperature fields simulated with the thermal models were then used as inputs to simulate the further stress/strain developments in the samples during the 50 current pulses.

The meshing system similar to that used in the previous work [10] was employed to discretize the present samples. In particular, the sizes of the triangular prism elements used to discretize the critical solder joints whose maximum von Mises stress and creep strain accumulation are used to assess the thermo-mechanical reliability are all 0.25 mm in the plane directions, and 0.025 mm in the through-thickness direction. The thermal and thermo-mechanical properties of all the materials were taken from either the previous work [10] or the existing literature [9,12,13]. This is because the present simulations considered the failure of the solder joints only. In particular, creep strain accumulation-induced fatigue cracking was assumed as the failure mechanism, and Anand's creep model was used to describe the mechanical properties of the solder joints [9,14–16]. Both the thermal and thermo-mechanical simulations have been executed using Abaqus 6.14-1 on a computer with Intel(R) Xeon(R) CPU E5-2699 v3 @ 2.30 GHz processor and 256 GB RAM. The running time for the thermal simulations with 6 cores was 0.7 h and for the thermo-mechanical simulation with 18 cores was 7.1 h.

2.3. FE simulation results

Fig. 2 show the temperature fields in the hottest samples during one power cycle. Fig. 3 present the heating powers (heating sources during the simulations) and the simulated evolutions of the cyclic average temperatures on the hottest 5 mm × 5 mm top surface areas of the samples. The amplitude and duration of the heating power pulse in the

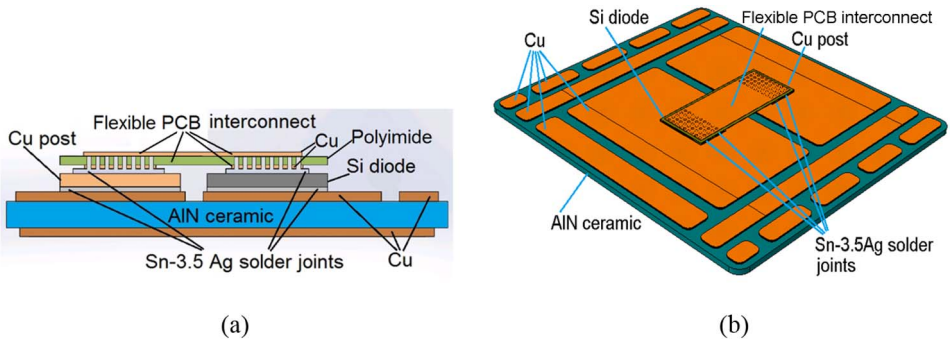

Fig. 1. The flexible PCB interconnect ST Si diode sample with the Sn-3.5Ag solder joints: (a) cross-sectional schematic (not to scale); and (b) three-dimensional ISO view of the design graph.

ST diode are approximately half and double of those in the LT diode to achieve similar cycle time (time per power cycle). During the initial stage of the transient simulation, the low and high limits of the average temperatures on the hottest 5 mm × 5 mm top surface area are somewhat lower and gradually increased with increasing number of power cycles (number of current pulse with an amplitude of 90 A). After about 60 s of the transient simulation, they reach the specified 40 °C and 120 °C during each power cycle.

The thermo-mechanical simulation results indicate that in each as-reflowed sample, the maximum Mises stress and maximum creep strain accumulation occur in the solder joint used to attach the Cu post onto the substrate, as can be ascribed to the mismatch of CTEs between the Cu post and the substrate. During the power cycling, the maximum stress and creep strain accumulation have been moved to the diode topside solder joint, i.e. the solder joint used to bond the flexible PCB on the topside of the diode, especially near the solder/diode interface. This can be explained by the fact that the cyclic high temperatures are encountered by this solder joint as shown in Fig. 2, and the flexible PCB still has higher CTEs than the Si diode. Figs. 4 and 5 present the simulation results comparing the distributions of Mises stress and creep strain accumulation in both the diode topside and backside solder joints in the two samples. In each sample, the diode topside solder joint with the maximum Mises stress and the maximum creep strain accumulation can hence be identified as the weakest solder joint.

Fig. 6 compares the evolutions of the maximum Mises stress and the maximum creep strain accumulation in the diode solder joints in the two types of samples. Here $\Delta\varepsilon_{ca}$ stands for the stable maximum creep strain accumulation per power cycle. In each sample, the cyclic range of the maximum Mises stress in the diode topside solder joint is higher than that in the backside solder joint. This is because the topside solder joint in contact with the active region of the diode experienced with wider cyclic temperatures than the backside solder joint. On the other hand, the cyclic ranges of the maximum Mises stress in the solder joints in the ST diode sample are similar to those in the LT diode sample. This is because the solder joints in the two samples have similar cyclic temperature profiles, while the maximum Mises stresses in the solder joints have been saturated and mainly dependent on the temperatures and the changing rates of the temperatures.

In each sample, the diode topside solder joint has significantly higher maximum creep strain accumulation than the backside solder joint. This can be attributed to both higher temperatures in the topside solder joint than the backside solder joint and higher mismatch of CTEs between the flexible PCB and the diode than between the diode and the AlN-based substrate. For the weakest solder joints, i.e. the topside solder joints, in the two types of samples, the ST diode with lower stiffness can reduce the maximum creep strain accumulation per power cycle from 0.0172 to 0.0142 (21% reduction) when compared with the LT diode. On the other hand, for the backside solder joint in the ST diode sample, the maximum creep strain accumulation per power cycle (0.0030) is somewhat higher than that for the backside solder joint in the LT diode sample (0.0026). This can readily be understood because the former backside solder joint is subjected to higher temperatures than the latter solder joint due to the fact that the 0.07 mm thin ST diode is much thinner than the 0.5 mm thick LT diode while both diodes have similar junction temperature profiles during the power cycling tests.

Thermo-mechanical fatigue lifetimes of soft solder joints, such as the present Sn-3.5Ag solder joints can be described with prediction models based on plastic strain development, creep strain development and inelastic energy density per thermal/power cycle [8–10,14–16]. As in the previous work [8–10], the mechanical property of the present Sn-3.5Ag solder joints was described by the Anand viscoplastic model, and the simulated creep strains include both the creep and plastic deformation developments in the solder joints. Based on the previous work [10], the average lifetimes of the three groups of Sn-3.5Ag solder joints with $\Delta\varepsilon_{ca}$ of 0.0178, 0.0176 and 0.0092 were 62,371, 80,460 and 362,532 power cycles, respectively. These results can be well fitted to the following Engelmaier model for predicting the lifetimes, N_f, of the solder joints [10,14]:

$$N_f = \frac{1}{2}\left(\frac{\Delta\varepsilon_{ca}}{2 \times 1.02}\right)^{-(2.50\pm0.56)} \quad (1)$$

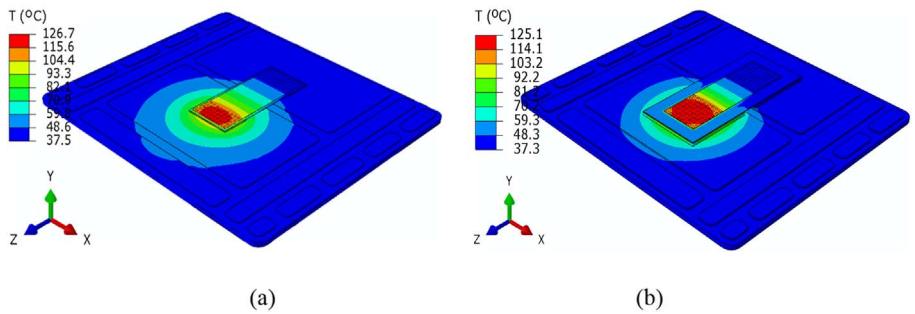

Fig. 2. Thermal simulation results showing the temperature fields in the hottest: (a) ST diode sample; and (b) LT diode sample during one power cycle.

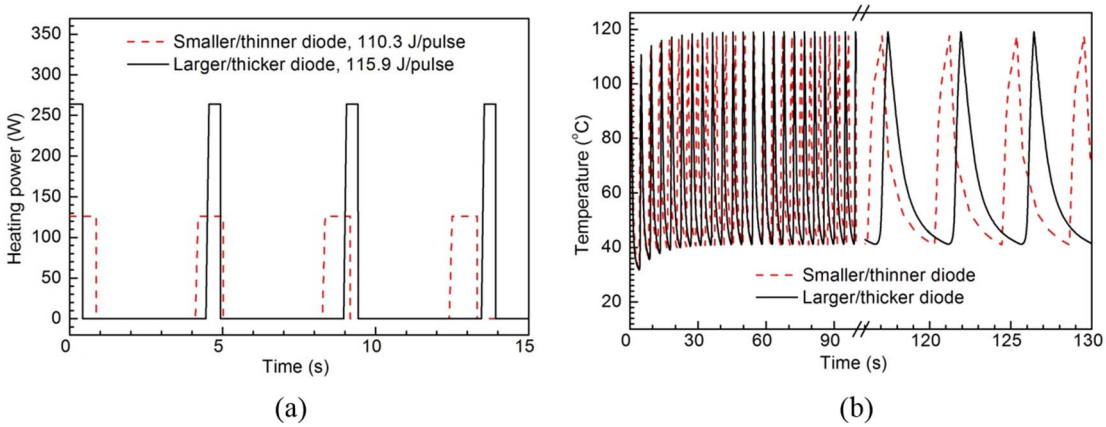

Fig. 3. Thermal simulation results comparing: (a) the heating powers specified during the simulations; and (b) the evolutions of the cyclic average temperatures on the hottest 5 mm × 5 mm top surface areas.

It should be noted that in both the previous work [10] and the present paper, the cyclic temperature conditions and thus the stress/strain rates of the critical Sn-3.5Ag solder joints were similar to each other. It was the $\Delta\varepsilon_{ca}$, the stable maximum creep strain accumulation per power cycle, rather than the maximum creep strain range per power cycle, which has been used to establish Eq. (1). As demonstrated in the existing literature [15], this can better account for the time-domain effect of the different temperatures on the maximum creep development in the solder joints. Applying Eq. (1) to the present results as shown in Fig. 6(b), the creep strain accumulation-induced fatigue lifetimes of the topside solder joints in ST and LT diode samples are respectively 123,687 and 76,599 power cycles. The improvement in the lifetime with ST diode is 61.5%.

3. Power cycling tests

3.1. Materials and methods

9.5 mm × 5.5 mm × 0.07 mm Si diodes, rated at 200 A–600 V, were obtained from Infineon Technologies. The backside (cathode) metallization in the as-received diodes was 1/0.3/0.3 μm thick AlTi/Ni/Ag and topside (anode) metallization was 3.2/0.5/0.3 μm thick AlSiCu/NiP/Pd. 13.5 mm × 13.5 mm × 0.5 mm Si diodes, rated at 50 A–4.5 kV, were obtained from Dynex Semiconductor Ltd (Lincoln, UK). The backside metallization in the as-received Si diodes was ~0.1/1/1 μm thick Ti/Ni/Ag and topside metallization was ~5 μm thick Al. ~0.1/1/1 μm thick Ti/Ni/Ag tri-metal was sputtered on the existing ~5 μm thick Al topside metallization to prepare the flexible PCB interconnect samples.

The flexible PCBs were custom manufactured from Stevenage Circuits Ltd (Stevenage, UK). There was ~4/0.1 μm thick NiP/Au finish on the surfaces of the Cu tracks on the as-received flexible PCBs. The AlN-based substrates with bare Cu finish were custom manufactured from DOWA Metaltech Co., Ltd (Tokyo, Japan). For assembling each single diode sample, 100 μm thick Sn-3.5Ag solder performs were placed between the surfaces to be bonded together as shown in Fig. 1. The Sn-3.5Ag solder joints were formed by reflowing in a vacuum of 500 Pa and at a peak temperature of 260 °C for 5 min.

Power cycling tests were carried out on the prepared single diode samples using a bespoke power cycling rig [10]. 10 samples for both ST (S1 to S10) and LT (L1 to L10) diode samples were tested. During the tests, each sample was heated by inputting current pulses with an amplitude of 90 A through the diode and cooled by mechanically mounting the sample on a cold plate of a water-based heat sink. The temperatures on the diode topsides of all the samples were monitored with infrared sensors. The cyclic temperatures were set between 40 °C and 120 °C, while the switching of the current pulses through each sample was controlled independently. The cycle number, cycle time, duty cycle (ratio of heating time to cycle time) and forward voltage drop across the sample at 40 °C were collected. All the samples were cycled until failure occurred as judged with a failure criterion which was set as a 20% increase in the forward voltage drop or a sudden decrease to nearly zero in the forward voltage drop.

After the power cycling tests, all the samples were visually checked to identify any visible characteristics, and the diodes were tested with multimeter to see whether they were still functional or not. The flexible PCBs in all the tested samples could easily be separated from topsides of the diodes. The microstructures of the as-prepared samples and representative failed samples were further observed using scanning electron microscopy (SEM). This was carried on a Hitachi TM300 desktop SEM integrated with a Quantax 70 energy-dispersive X-ray spectroscopy (EDXS) microanalysis system. For cross-sectional SEM observation, all the samples were first cut using a diamond saw, and then they were mounted within an epoxy resin which was later grinded

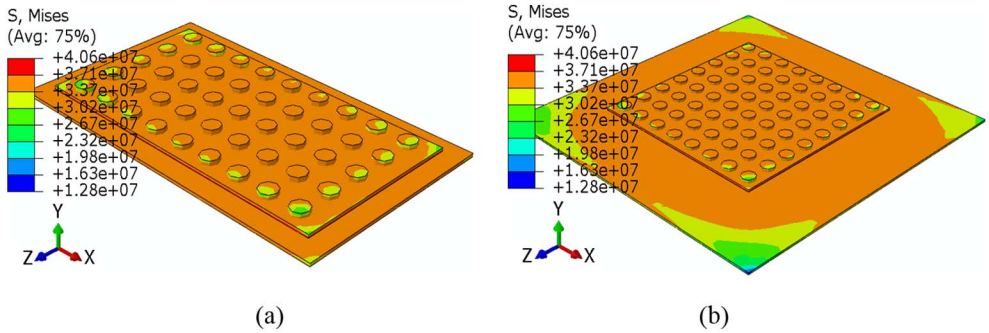

Fig. 4. Thermo-mechanical simulation results comparing the distributions of Mises stress in the diode solder joints in: (a) ST diode sample; and (b) LT diode sample after 50 power cycles.

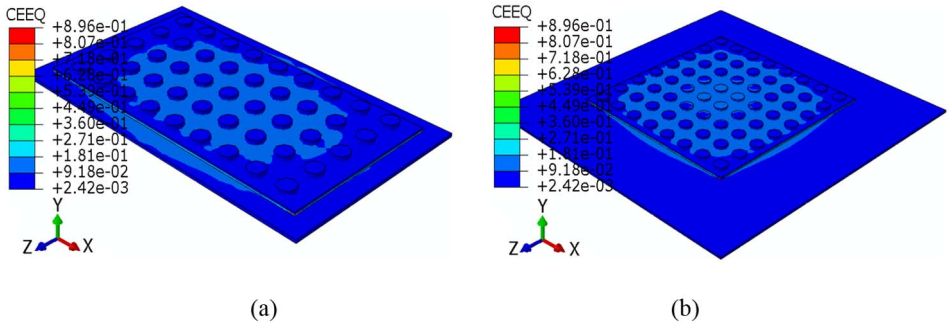

Fig. 5. Thermo-mechanical simulation results comparing the distributions of creep strain accumulation in the diode solder joints in: (a) ST diode sample; and (b) LT diode sample after 50 power cycles.

and polished using first 600 grit size SiC paper down to 1 μm diamond suspension.

3.2. Power cycling parameters and lifetimes

As presented in Figs. 7 and 8, for the majority of the ST diode samples, both the cycle times and duty cycles decreased and the forward voltage drops increased with increasing the numbers of power cycle from the beginning or very early stages of the power cycling tests. Only sample S10 with the longest lifetime had the cycle time and forward voltage drop which were relatively stable and appeared to remarkably fluctuate or increase with increasing the number of power cycle during the late stage. By contrast, for the majority of the LT diode samples, all the cycle times, duty cycles and forward voltage drops were relatively stable until the late stages of the power cycling tests. Then both the cycle times and forward voltage drops increased dramatically with further increase in the numbers of power cycle leading to rapid failure. In addition, the variations in the cycle times among the different LT diode samples were clearly lower than those among the different ST diode samples.

It was the average cycle times of 4.2 s and 4.5 s and average duty cycles of 20% and 9% that were calculated from the collected data of the ST and LT diode samples and had been used to obtain the thermal simulation results as shown in Fig. 3. After the power cycling tests, it is found by using a multimeter that 8 of the 10 ST diodes had nearly zero forward voltage drop, and only the rest 2 were functional (working diodes). By contrast, only 3 of the 10 LT diodes had nearly zero forward voltage drop, and the rest 7 were still working diodes. Here and in what follows, a diode with nearly zero forward voltage is referred to as a "broken diode".

Fig. 9 compares the distributions of cumulative probability for the power cycling lifetimes obtained from the two types of samples. Here the R values stand for the coefficients of correlation for the linear data fittings. The cumulative probability for each data set, $f(i)$, was calculated by placing the data of the lifetimes in ascending order and letting:

$$f(i) = \frac{i - 0.5}{n} \times 100\% \tag{2}$$

where n is the total number of data points for each type, and i is the ith order in ascending data set [10]. The lifetimes of the two types of samples statistically follow both the Logarithm-Normal distribution and the Weibull distribution quite well. The average lifetime of 63,813 power cycles for the LT diode samples is slightly lower than but close to the FE prediction of 76,599 power cycles. However, the average lifetime of 50,016 power cycles for the ST diode samples is significantly lower than the FE prediction of 123,687 power cycles.

3.3. Structure characterization

Figs. 10 and 11 present the SEM images showing the interfacial microstructure in the as-prepared ST and LT diode samples, respectively. In both samples, the Ni_3Sn_4, Cu_6Sn_5 and $(Cu,Ni)_6Sn_5$ intermetallic compounds (IMCs) formed at the interfaces are typical products of the interfacial reactions between the solid NiP, Ni and Cu and the liquid Sn-based solders during reflow processes [17–21]. The 0.3 μm thick Pd and 0.3 μm and 1 μm thick Ag finishes on the topsides and/or backsides of the two types of diodes had rapidly been dissolved into the liquid solders, and thus their involvement in the interfacial reactions was hardly observed. During the solidification of the liquid solders, they precipitated into Ag_3Sn and Pd_3Sn IMCs, and were embedded into the matrix of the solder joints. The 0.5 μm thick NiP and 1 μm thick Ni on the topsides of the two types of diodes had almost been consumed completely, but there were still ~0.2 and 0.8 μm thick Ni residuals under the backsides of the ST diode and the LT diode,

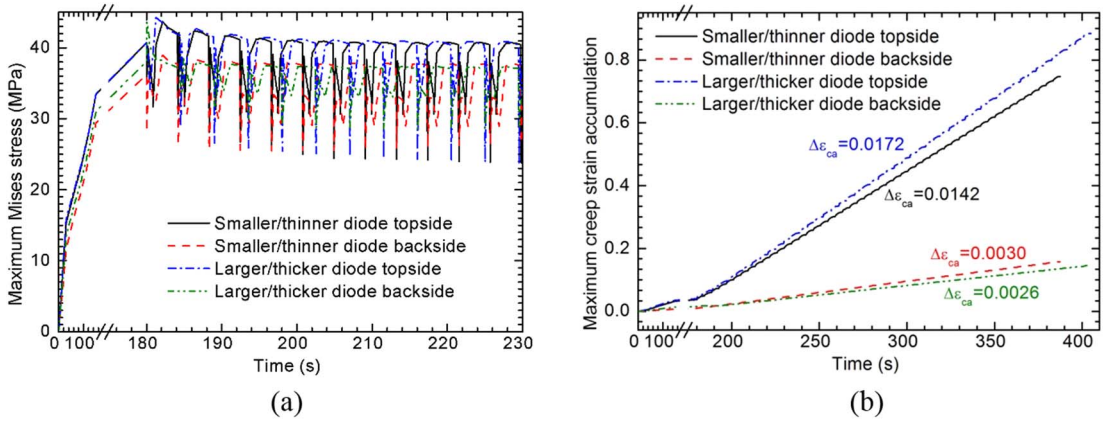

Fig. 6. Thermo-mechanical simulation results comparing the evolutions of: (a) the maximum Mises stress; and (b) the maximum creep strain accumulation in the diode solder joints in both ST and LT diode samples during the reflow process and 50 power cycles.

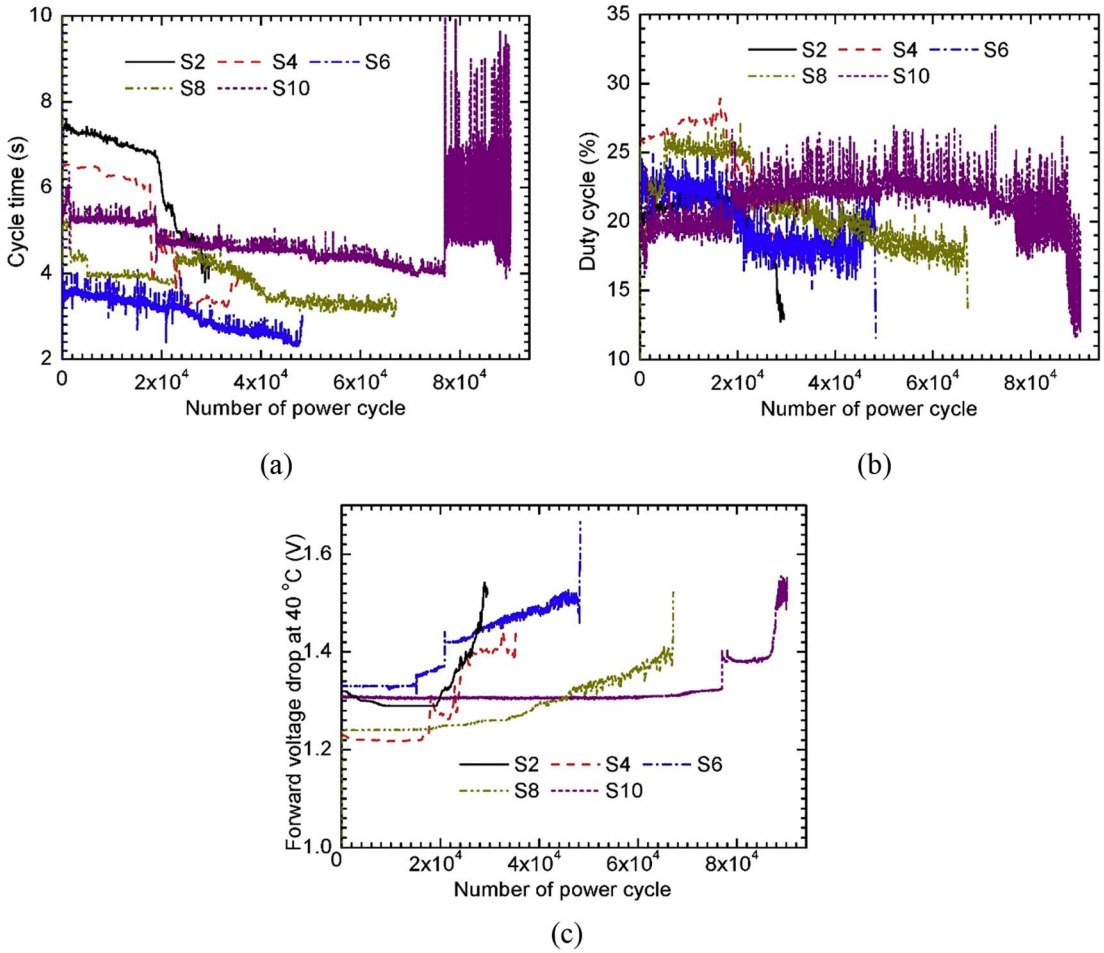

Fig. 7. Representative curves of the collected parameters versus number of power cycle from the ST diode samples during the power cycling tests: (a) cycle time; (b) duty cycle; and (c) forward voltage drop.

respectively. This can be understood because the interfacial reaction between NiP and liquid Sn is quicker than that between pure Ni and the liquid Sn [20]. On the other hand, the supply and migration of Cu atoms from the opposite sides of the Sn-based liquid solder joints could slow down the interfacial reaction between Ni and liquid Sn [21]. It should especially be noted that it was the solder that was in direct contact with the topside AlSiCu in the as-prepared ST diode sample, while there was a layer of Ni_3Sn_4 IMC between the solder and the topside Al in the as-prepared LT diode sample.

Rapid solidification structure can be visually observed from the topsides of the diodes in all the failed samples with broken diodes. Figs. 12 to 15 present the SEM images taken from the diode topsides and the polished cross sections of representative samples after the power cycling tests. The rapid solidification structure consisted of 0.1 to 0.5 mm sized Si dendrites filled with Sn- and Al-enriched phases between the Si branches, which is smaller than but similar to one of those observed in the 50 A–1.7 kV insulated gate bipolar transistor (IGBT) subjected to an overcurrent of ~1100 A within millisecond [22]. This reveals that the local melting of Si and the later rapid solidification occurred in these samples. There were also a few Sn whiskers formed over the Si dendrites.

In the 8 ST diode samples failed with broken diodes, the solder residual was in continuous, and sub-millimeter sized Al (AlSiCu) patches were exposed on the topsides of the diodes. In the 2 ST diode samples failed with working diodes and all the 10 LT diode samples, there was a thin layer of solder residual continuously covering the topsides of the diodes. In particular, in the LT diode samples, the interfacial Ni_3Sn_4 crystals still had good contact with the underneath Al layer, and the primary cracks leading to the de-bonding of the flexible PCBs from the diodes occurred within the solder joints (very close to the interfacial Ni_3Sn_4 crystals). There were also many secondary cracks and broken small particles distributed around the primary cracks or at the grain boundaries, see Figs. 14 and 15.

4. Discussion

In most ST diode samples after the power cycling tests, the observed exposure of sub-millimeter sized Al (AlSiCu) patches on the topsides of the diodes indicates that the solder joints probably had weak bonding strength on the diodes, and shear-induced local delamination of the solder joints from the underneath AlSiCu metallization played an important role in the final failure of the samples. This may be the main reason why the average lifetime of the 10 ST diode samples is significantly lower than the FE prediction based on the creep-induced fatigue cracking as the failure mechanism of the topside solder joint.

To verify the above hypothesis, 6 of 2 mm × 2 mm × 0.5 mm Si dummy diodes with 0.1/1/1 μm thick Ti/Ni/Ag metallization were soldered on the topsides of 3 ST diodes or 2 LT diodes with the same Sn-3.5Ag solder alloy and the same reflow process as those used to assemble the power cycling samples. The shear strengths of the dummy diode solder joints were tested at a constant shear rate of 0.2 mm/s on a Nordson DAGE 4000 plus bond tester (Aylesbury, Buckinghamshire, UK). The failure was found to occur at the solder/AlSiCu interfaces in all the 6 dummy diodes soldered on the ST diodes, while failures were within the solder joints in all the 6 dummy diodes soldered on the LT diodes. The resulting shear strengths are plotted in Fig. 16 where the

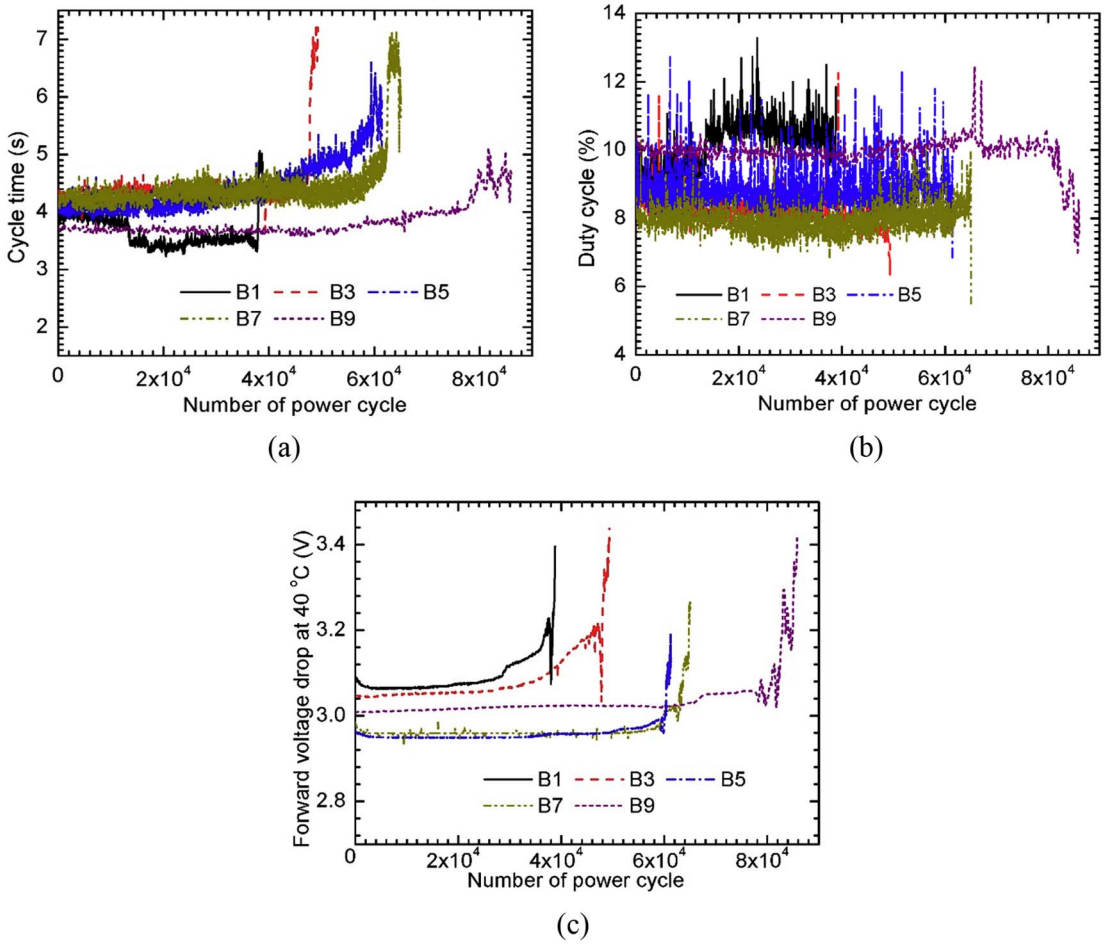

Fig. 8. Representative curves of the collected parameters versus number of power cycle from the LT diode samples during the power cycling tests: (a) cycle time; (b) duty cycle; and (c) forward voltage drop.

cumulative probability values were also calculated with Eq. (2). The FE simulation results indicated that the maximum shear stresses of the solder joints at the solder/diode topsides were 20.7 MPa and 22.3 MPa for the ST and LT diode samples during the power cycling tests. Therefore, the shear-induced local delamination of the solder joints from the AlSiCu metallization should be the main mechanism leading to the power cycling failure of most ST diode samples.

Because of lower shear strengths, shear-induced local delamination of the solder joints from the AlSiCu metallization of the diodes could start quite early. As a result, substantial contact resistances between the solder joints and the diodes increased with increase in the delamination area. Thus increasingly additional heating powers due to the contact resistance were generated during the power cycling tests. The additional heating powers were in so close contact with the active regions of the diodes that they almost directly superposed on current heating powers generated in the diodes. This may be the reason why the collected forward voltage drops increased and both cycle times and duty cycles decreased with increasing the numbers of power cycles from the beginning or very early stages of the power cycling tests with the constant current mode.

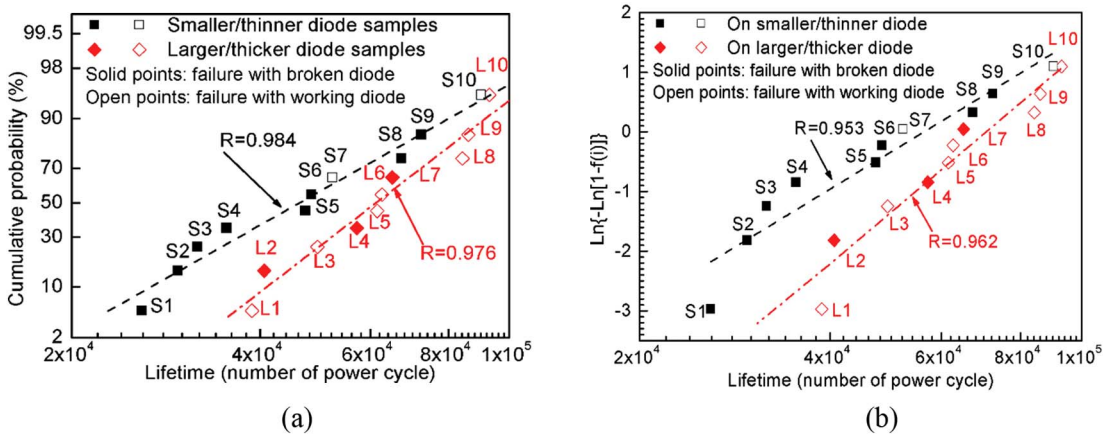

Fig. 9. Distributions of the power cycling lifetimes of the ST and LT diode samples on the: (a) Logarithm-Normal probability coordinate; and (b) Weibull probability coordinate.

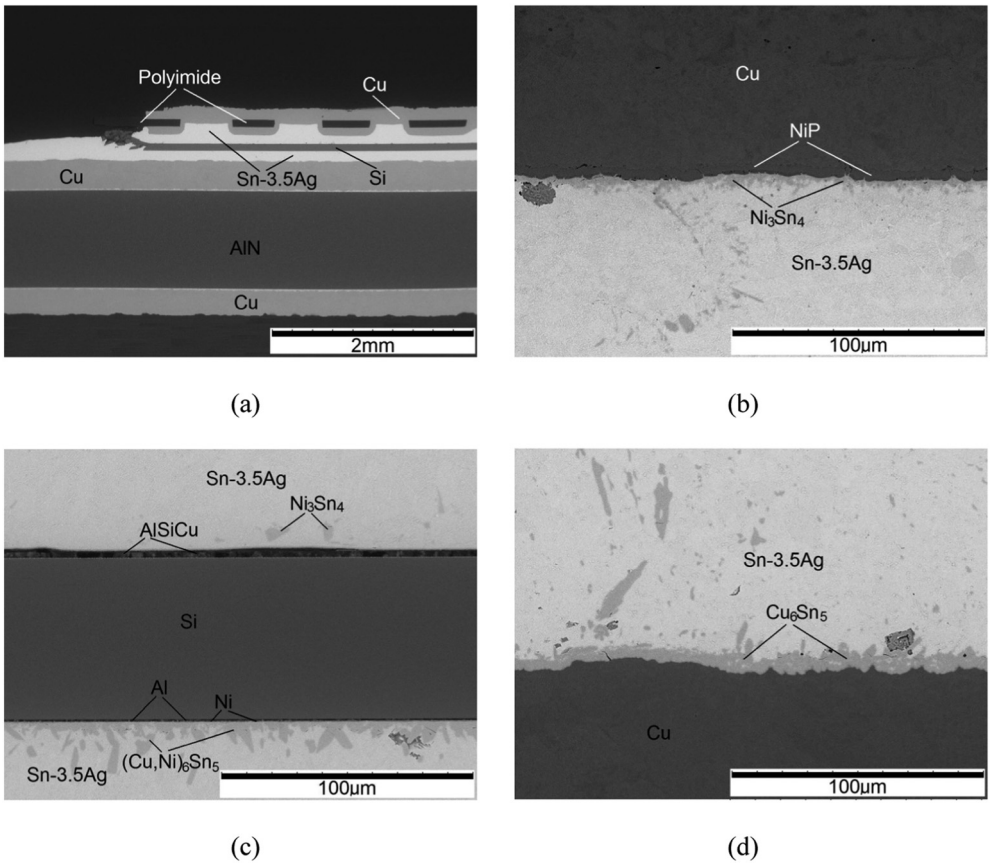

Fig. 10. Cross-sectional SEM images of the as-prepared ST diode sample showing: (a) large field of view; (b) flexible PCB/topside solder interface; (c) topside solder/diode interface and diode/backside solder interfaces; and (d) backside solder/substrate interface.

When the increase in the contact resistance and in the additional heating powers reached certain levels, the heats could not effectively be removed by the heat sink any more leading to the temperatures exceeding the upper limits. As in the failure of diodes due to high power dissipation [23,24], the forward voltage drops across the diodes would further increase with increasing the temperature. Then sudden and high accumulations of the heats led to local melting of the nearby materials, and hence broke the diodes as observed in most of the ST diode samples. The local melting of the nearby materials also resulted in compressive stresses due to expansion of volume which could promote the formation of the Sn whiskers as shown in Fig. 12(b).

In the LT diode samples after the power cycling tests, the observed primary cracks within the solder joints which caused the de-bonding of the flexible PCBs from the diodes are in good agreement with the FE simulation result of the maximum creep strain accumulation near the solder/diode interface (Figs. 5 and 15). The primary cracks accompanied with secondary cracks and broken small particles at the grain boundaries are typical creep-induced fatigue cracks due to grain boundary sliding [14]. Therefore, the average lifetime of the 10 LT diode samples is close to the FE prediction based on the creep-induced fatigue cracking as the failure mechanism of the topside solder joint. It should be noted that the lifetimes of the present LT diode samples are somewhat shorter than those of the conventional Al wire interconnect samples [25]. The emerging sintered Ag joints should be selected to replace the Sn-3.5Ag solder joints to bond the flexible PCBs on the LT diodes or similar other power devices as the alternative to the Al wire bonding technology.

The propagation of the creep-induced fatigue cracks within the topside solder joints in the LT diode samples was slower than the shear-induced delamination of the solder joints from the AlSiCu metallization on the topsides of the diodes in the ST diode samples. This is probably the reason why for the majority of the LT diode samples, all the cycle times, duty cycles and forward voltage drops were relatively stable. During the late stages of the power cycling tests, the creep-induced fatigue cracking also led to increases in the forward voltage drops, and hence caused additional heating powers in the LT diode samples. However, these additional heating powers were ten of micrometers away from the active regions of the diodes (Fig. 15), and hence the total heats generated in the samples could still be effectively removed by the heat sink through automatic increases in the current switching off times. The latter can be justified by the increase in the cycle times and decrease in the duty cycles of most LT diode samples during the late stages of the power cycling tests as shown in Fig. 8. The effective removement of the heats also reduced the probability of breaking the diodes in the LT diode samples as aforementioned.

It is hence the different failure mechanisms of the topside solder joints that led to the results of the power cycling tests in contradiction to the FE predictions for the lifetimes of the two types of diode samples. The shear-induced delamination of the solder joints from the AlSiCu metallization which causes the poor power cycling reliability of the ST diode samples can be related to the lack of a layer of stable Ni_3Sn_4 IMC at the topside solder/diode interface as that was observed in the LT diodes samples. This can be further attributed to the following two facts. On the one hand, the 0.5 μm thick NiP was too thin to provide sufficient amount of Ni to generate a layer of Ni_3Sn_4 IMC at the interface. On the other hand, the NiP layer plated with electroless process in general had relatively poor bonding strength with the underneath AlSiCu [26], and the Ni_3Sn_4 IMC formed through the interfacial reaction between NiP and Sn-3.5Ag solder could not stay at the interface stably. If it was the same 0.1/1/1 μm thick Ti/Ni/Ag topside metallization as that on LT diodes had been used, much longer power cycling lifetimes similar to the FE prediction (123,687 cycles) could be

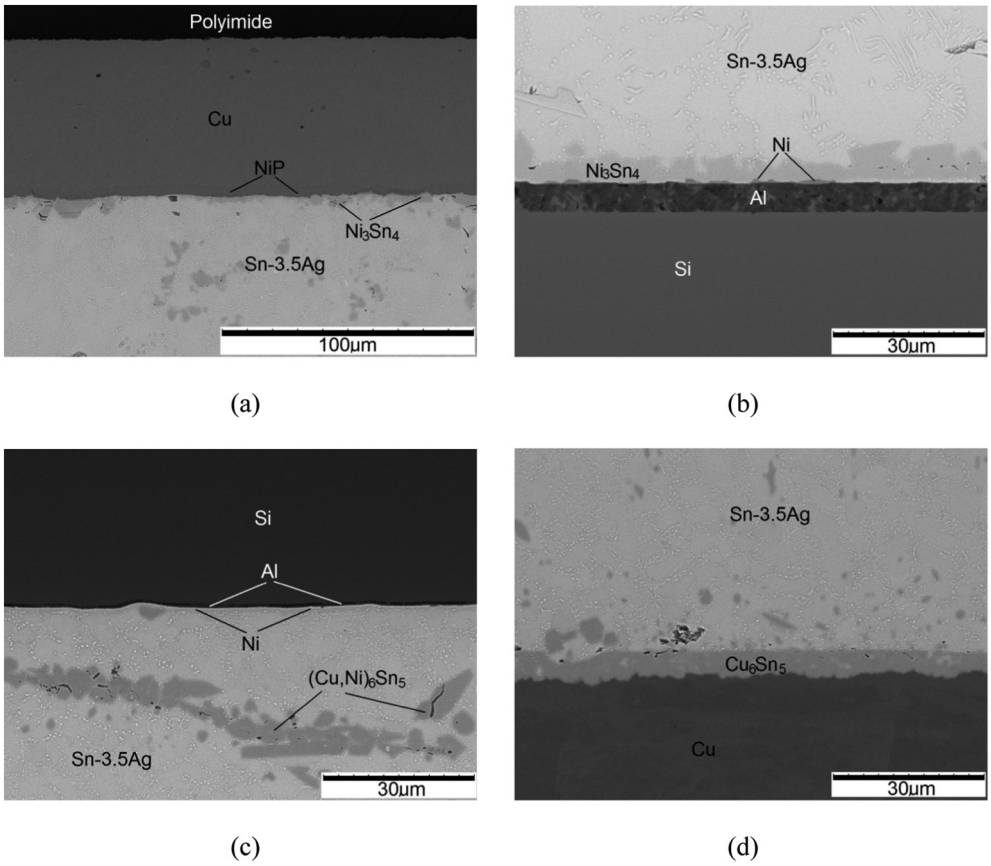

Fig. 11. Cross-sectional SEM images of the as-prepared LT diode sample showing: (a) flexible PCB/topside solder interface; (b) topside solder/diode interface; (c) diode/backside solder interfaces; and (d) backside solder/substrate interface.

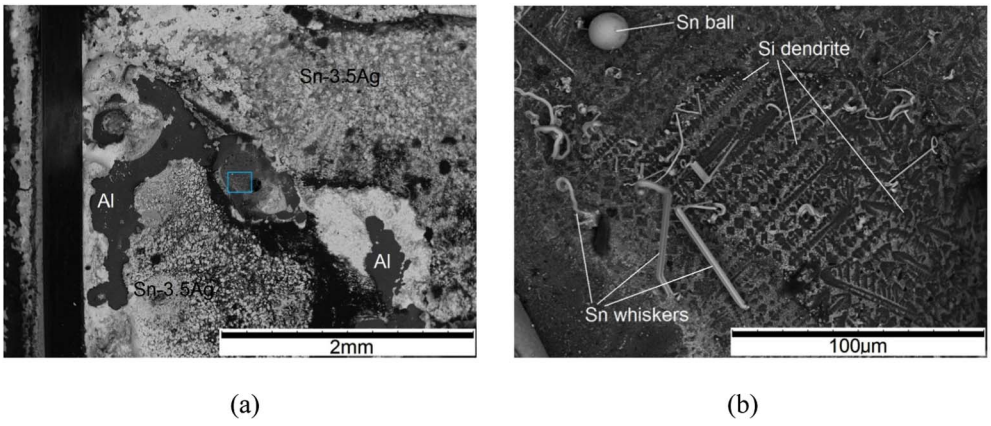

Fig. 12. Diode topside SEM images of ST diode sample S1 after the power cycling test: (a) large field of view; and (b) enlarged view of the blue line boxed area in (a). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

achieved from the ST diode samples. In such a case, even if the Sn-3.5Ag solder joints are used to bond the flexible PCBs on ST power devices for forming the planar interconnects, they could have lifetimes similar to those of the conventional Al wire interconnect samples [25]. Therefore, a modified and more appropriate topside metallization system should be applied on the commercially available ST diodes to obtain the potentially high thermo-mechanical reliability.

5. Conclusions

All the results have been obtained from the flexible PCB interconnect single ST 9.5 mm × 5.5 mm × 0.07 mm and LT 13.5 mm × 13.5 mm × 0.5 mm Si diode samples, but the methods and principles established through this work should be applicable to real power modules assembled with similar planar interconnect technology. Based on the above results and discussion, the following conclusions are drawn:

1) By soldering 0.05/0.1/0.05 mm thick Cu/polyimide/Cu flexible PCBs on single diodes to form planar interconnect samples, the FE simulation results predict that the topside Sn-3.5Ag solder joint on a ST diode has a lifetime 61.5% higher than that on a LT diode due to creep strain accumulation-induced fatigue cracking under similar power cycling conditions.
2) The power cycling lifetimes of the ST diode (with 3.2/0.5/0.3 μm thick AlSiCu/NiP/Pd topside metallization) samples are

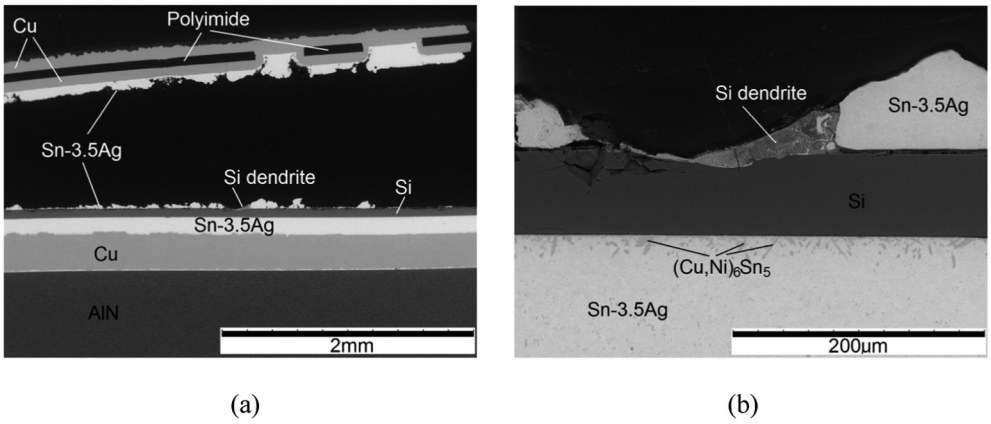

Fig. 13. Cross-sectional SEM images of ST diode sample S9 after the power cycling test: (a) large field of view; and (b) enlarged view.

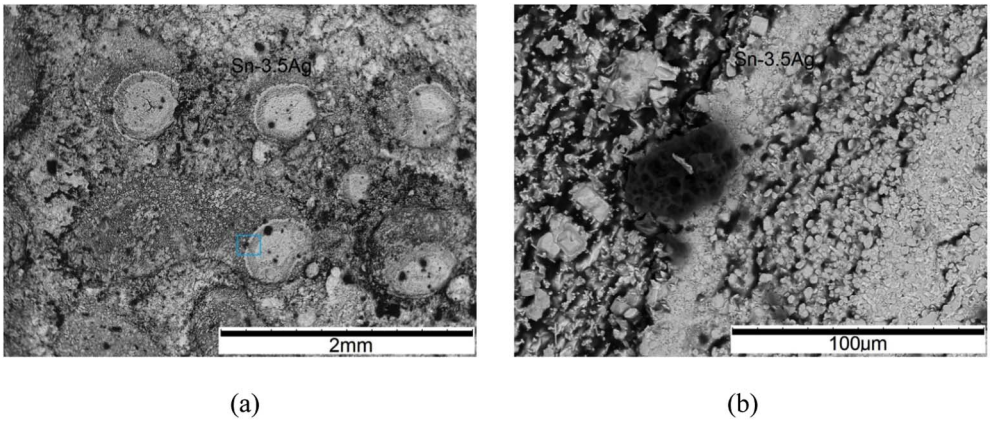

Fig. 14. Diode topside SEM images of LT diode sample L6 after the power cycling test: (a) large field of view; and (b) enlarged view of the blue line boxed area in (a). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

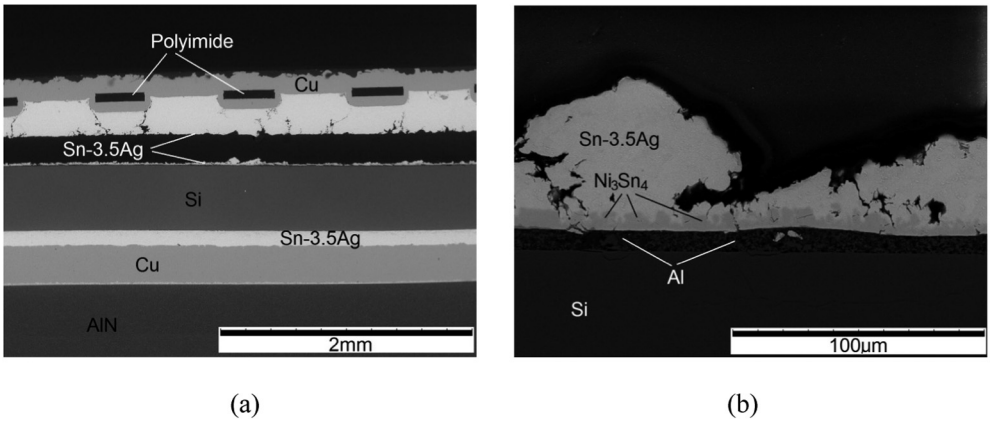

Fig. 15. Cross-sectional SEM images of LT diode sample L10 after the power cycling test: (a) large field of view: and (b) enlarged view.

significantly lower than the FE prediction. This can be attributed to the weak bonding strength of the topside solder joints on the diodes and the shear-induced local delamination of the solder joints from the underneath AlSiCu metallization layer during the power cycling tests.

3) The average value of the tested power cycling lifetimes of the LT diode (with 5/0.1/1/1 μm thick Al/Ti/Ni/Ag topside metallization) samples is reasonably in agreement with the FE prediction. Microstructure characterization reveals that the samples indeed failed through creep-induced fatigue cracking due to grain boundary sliding within the topside solder joints and near the solder/diode interfaces.
4) The different failure mechanisms revealed by microstructure characterization can be used to explain the evolutions of the collected cycle times, duty cycles and forward voltage drops of the ST diode samples which were different from those of the LT diode samples during the power cycling tests.
5) The present results can also be used to demonstrate that a modified and more appropriate top metallization system should be applied on the commercially available ST diodes to achieve potentially high thermo-mechanical reliability of the flexible PCB planar interconnects.

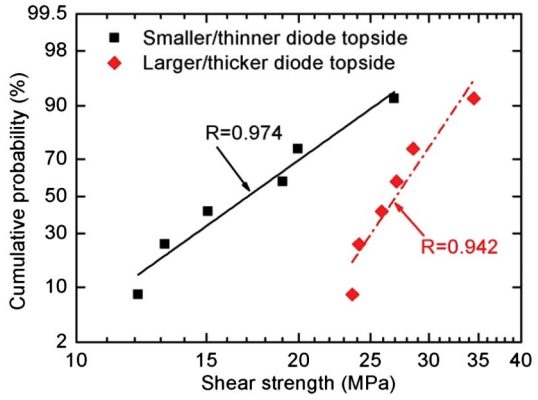

Fig. 16. Comparison of shear strengths of Sn-3.5Ag solder joints on ST and LT diode topsides.

Acknowledgements

This work was supported by the Engineering and Physical Sciences Research Council [grant numbers EP/K035304/1, EP/K034804/1] (EPSRC, UK) through the Centre for Power Electronics (grants for the hub and components theme respectively).

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