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Reducing Peak Current and Energy Dissipation in Hybrid HVDC CBs Using Disconnector Voltage Control

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***Abstract*—Peak fault current and energy dissipation in high voltage direct current (HVDC) circuit breakers (CBs) are very important parameters that impact dc grid protection development. This paper analyses a hybrid DCCB (HCB) control that reduces peak current and energy dissipation, by regulating the voltage across contacts of the ultra-fast disconnector (UFD). This is achieved by manipulating the number of inserted surge arresters while contacts of the UFD are moving apart. The controller is seamlessly integrated with the current controller of HCBs. Analytical model for current and energy calculation is presented, verified, and employed for parametric studies. PSCAD simulation with 320kV, 16kA test circuit confirms that the proposed voltage control reduces the peak current and energy dissipation by around 20-30%. A 900V, 500A HCB laboratory hardware is described and the experimental results are shown to corroborate simulation conclusions.**

***Index Terms*-- Dc meshed grids, HVDC protection, HCB, fault current limiting.**

I. Introduction

INCREASED interest towards realizing HVDC grid, have resulted in substantial recent advances in the HVDC CB technology [1]. Dc grid faults cause very fast current rise, while converters at grid terminals are very sensitive to overcurrent conditions, which leads to stringent requirements for DCCB performance. Unlike ACCBs, DCCBs must dissipate large amounts of energy which is stored in the transmission lines and the series inductor.

Different DCCB technologies (i.e. solid state, mechanical, and hybrid) have been developed and high-voltage prototypes demonstrated in the past few years [2]-[7]. The hybrid IGBT-based DCCB (HCB) is the fastest operating technology, which also provides low-loss operation in closed state [7]. However, high cost and size are the main disadvantages of the HCB.

A number of recent research projects have reported methods to improve performance and reliability of HCBs. Reference [8] describes how low-loss closed-state can be achieved without sacrificing on costs, overcurrent capability or reliability. In [9] authors present modeling methods, demonstrate wide range of functionalities and describe self-protection principles. Fault current rating of HCBs is around 16-19kA which is achieved by the new transistor technology in the main valve [10]. Because of this limited current rating, and considering also component costs and magnitude of prospective dc grid fault current, HCBs will have self-protection function [9]. Authors in [11] present an HCB concept where the IGBTs in the main valve are turned OFF sequentially. This may result in lower fault current, however, the control details on the HCB are not provided.

The peak fault current is of foremost importance in developing dc grid protection. It dictates not only the current rating of the HCB IGBTs but also the surge arresters. The dissipated energy depends on the square of peak current, and it has major influence on HCB size and weight. The same fault current passes through other dc grid components like modular multilevel converter (MMC) terminals, which can tolerate only small overcurrent. If MMC terminal is blocked on overcurrent, this implies loss in transmission capacity and has major consequences for dc grid reliability.

Two methods for limiting peak fault current have been traditionally studied:

- Increasing opening speed of ultrafast disconnector [12]. The reported minimal opening time is around 2ms which is constrained by the physical characteristics of UFD.
- Increasing size of series inductors. These inductors limit the rate of current increase while DCCB contacts are opening, and they will be required with all DCCBs. However large inductors may affect performance of dc grid (energy balancing, overvoltage and stability), and only values below 300mH are discussed in [2].

This article studies an alternative method to limit the peak fault current, based on accurate voltage control across Ultrafast Disconnector (UFD) switch inside HCB.

UFD achieves fast speed by using low weight contacts, high-speed repulsion actuators, and lateral closed-force on contacts, under the assumption of operation at zero current [12]. The traditional approaches consider the UFD as a two position device with its status either open or close. In this paper the UFD is consider to have three positions: open, close, and moving contacts. Furthermore, a voltage control is proposed which is activated while contacts are moving. The study aim is to present theoretical analysis of possible benefit of such control, to develop the control method, and to demonstrate functionality on 320kV, 16kA model in PSCAD. Finally, the proposed method will be evaluated on 900V, 500A HCB prototype at University laboratory.

The paper is organized as follows: Section II explains the conventional operation of the HCB, including analysis of the

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fault current and energy dissipation. The proposed voltage control of the UFD is explained in Section III. Section IV and V deal with PSCAD and experimental verification respectively. The conclusions are provided in Section VI.

II. Hybrid DCCB Conventional Operation

A. Operating principles

Fig. 1 shows a HCB schematic. The normal current path consists of load commutation switch (LCS) T_1, and UFD. The main breaker branch consists of a string of IGBTs. The energy absorber includes appropriately rated bank of surge arresters. An inductor L_{dc} is used to reduce the rate of current rise. The residual circuit breaker (RCB) isolates the HCB from the grid once the current is extinguished. The opening process is summarized as follows [6]:

1- On receiving the trip signal the LCS is turned OFF immediately. The current commutate to the main breaker branch, which is continuously ON.
2- When the UFD current is less than residual current, the UFD is signaled to open. It takes few milliseconds to achieve full contact separation in UFD.
3- When UFD is fully open, the main breaker is commanded to open. This commutates the current to the arrester branch and forces the current to decay to zero.
4- Once the T_2s are OFF and RCB current is less than the residual current then the RCB is commanded to open. Once the RCB is fully open, the CB is open completely.

The closing process is reverse. Fig. 2 shows the current waveform for opening process using 320kV, 16kA test system with parameters from Table I in the Appendix. The PSCAD model includes default surge arrester (SA) characteristic, and the complete HCB model from [8].

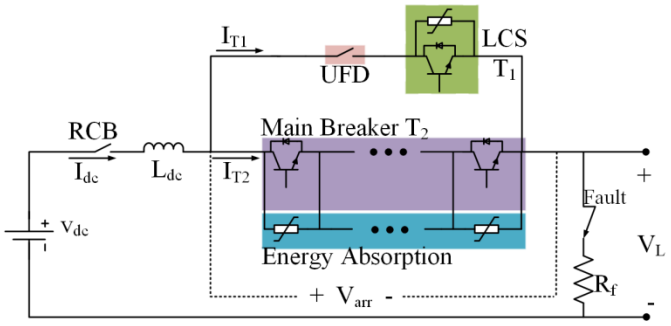


Fig. 1. Schematic of HCB proposed by [7].

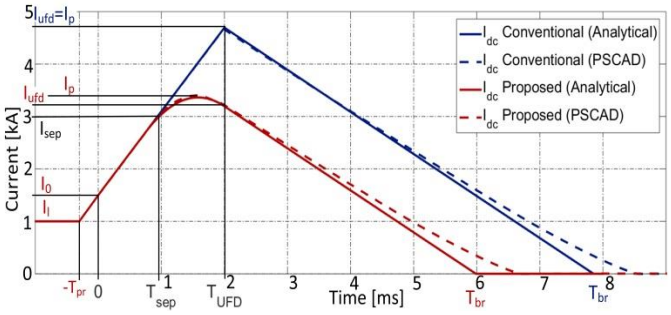


Fig. 2. Analytical and PSCAD results for DC fault current with conventioanl and proposed control.

The analytical modeling is undertaken to derive a closed-form expressions for fault current (I_{dc}), break time (T_{br} time from receiving trip signal until current decays to zero [2]), and energy dissipation in the arresters (E_{arr}). This will enable qualitative evaluation of benefits of new control method.

B. Current rising interval $0<t<T_{ufd}$

It is assumed in Fig. 2 that time starts when HCB receives trip signal. The current value at this instant is I_o, which consists of load current I_l and current increase while protection is making trip decision in interval T_{pr}, as seen in Fig. 2.

$$I_0 = I_l + \frac{V_{dc}}{R_f}\left(1-e^{-\alpha Tpr}\right) + I_l e^{-\alpha Tpr} \tag{1}$$

where, R_f is fault resistance, and $\alpha=R_f/L_{dc}$. The dc voltage V_{dc} is assumed constant, since this represents the worst case current rise, corresponding to a strong dc bus. Also, high dc voltage avoids converter blocking, which is highly desired. Some other value of V_{dc} will not change the main conclusions. The instantaneous fault current in this interval is calculated as:

$$I_{dc} = \frac{V_{dc}}{R_f}\left(1-e^{-\alpha t}\right) + I_0 e^{-\alpha t}. \tag{2}$$

It is assumed that the operating time of UFD (i.e. T_{UFD}) is known. The peak current I_p can be determined by replacing $t=T_p=T_{ufd}$ in (2).The energy dissipation in this interval is zero.

C. Current falling interval $T_{ufd}<t<T_{br}$

Once the UFD is open, the whole energy absorber (bank of surge arresters) is inserted in the circuit. The circuit configuration changes and the dc current can be calculated as:

$$I_{dc} = \frac{V_{dc}-V_{arr}}{R_f}\left(1-e^{-\alpha t}\right) + I_p e^{-\alpha t}. \tag{3}$$

Where I_p is the initial current determined in the previous interval. In all further calculations, it is assumed that the arrester voltage is constant and is equal to $V_{arr}=1.5\times V_{dc}$, which is accurate for the proposed simplified model. The HCB break time (T_{br}) can be calculated by equating (3) to zero:

$$T_{br} - T_{ufd} = \frac{1}{\alpha} Ln\left(\frac{0.5V_{dc} + R_f I_p}{0.5V_{dc}}\right) \tag{4}$$

The energy dissipation in the surge arresters is calculated by integrating the product of the arrester's current and voltage:

$$E_{arr} = \frac{3V_{dc}^2}{4R_f}\left(T_{br} - T_{ufd} + \frac{e^{-\alpha T_{br}+\alpha T_{ufd}}-1}{\alpha}\right) - \frac{3V_{dc}I_0}{2\alpha}\left(e^{-\alpha T_{br}+\alpha T_{ufd}}-1\right) \tag{5}$$

As it is seen in Fig. 2, these analytical expressions give reasonably good accuracy, compared with PSCAD simulation.

III. Proposed Voltage Control Across Disconnector

A. Operating principles

We are proposing to commence inserting surge arresters while contacts are moving. The expected benefit is that resistance in the current path will be larger in the current rising interval which may lead to reduction in the peak fault current. Such control method is based on the two assumptions:

1) It is possible to manipulate the number of inserted cell in the HCB. This is justified since dc current control with HCB has been reported [9], although only 4 cells of 80kV have been assumed. One cell consists of a number of IGBTs in series with a parallel arrester across them. There is no technical difficulty in using larger number of smaller cells, although this may marginally increase costs. Evidently the larger the number of cells (and SAs), the better control resolution will be. In the analyses here 8 cells are considered.
2) It is possible to accurately control the voltage across UFD while contacts are moving. We propose using contact position measurement and close loop feedback control, although it will be shown that open loop may also suffice. It can be reasonably assumed that the UFD voltage withstand is proportional to the distance between UFD contacts, but the coefficient will depend on the insulating medium.

B. Contact separation dynamics

A UFD with two moving contacts and lateral force for closed-position as in [7],[12] is assumed. This design requires some lateral overlap (OL) between contacts in closed position, and the contact separation z, can be expressed using absolute position of one contact x, as:

$$z = 2x - OL. \tag{6}$$

The dynamic force equation of the UFD can be represented as:

$$F - Bv - kx = m\frac{d^2x}{dt^2}. \tag{7}$$

Where, B is the friction coefficient, k is spring constant (of bi-stable assembly), m is the weight of the moving part, and F is the electromagnetic force generated by the Thomson Coils (TC) [13],[14].

A complete UFD dynamic model is developed in PSCAD, which includes detailed TC and also electrical actuation circuit. This model is verified against experimental results on 900V, 500A UFD which is reported in [15], and the parameters are shown in Table II in Appendix. The evolution of the UFD contact position and the contact separation over opening time are shown in Fig. 3, which is in good agreement with curves reported in [14]. The separation time T_{sep} is the time when the contacts of the UFD become separated from each other (z>0). It is seen that the contact position curve is initially non-linear because of high acceleration, but for most of contact travel it increases linearly (velocity is constant).

In the interval of interest, when z>0, it can be assumed that the contact distance increases linearly with time. This approximation is used in the simple analytical model. It also indicates that open loop control may suffice.

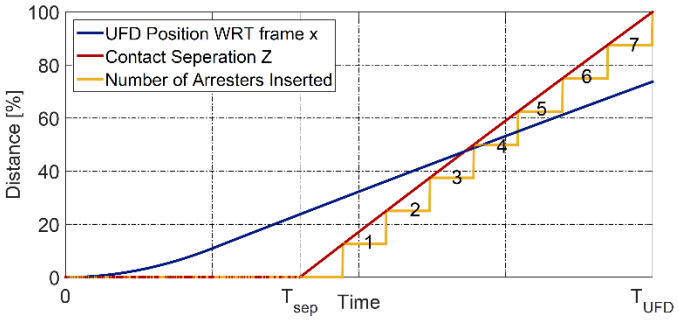


Fig. 3. UFD contact position with respect to the fixed frame, UFD contact separation, and number of inserted arresters.

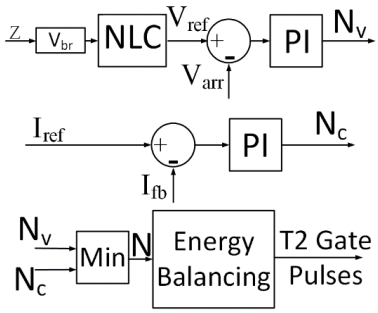


Fig. 4. Voltage controller for opening of HCB.

C. Control method

It is recommended to accurately measure contact position in order to achieve high-precision and robust control. As an example, in our prototype Hall Effect sensors are used. The UFD voltage withstand can be estimated by multiplying the contact separation with medium breakdown voltage per unit distance (V_{br}), with some additional safety margin. In the experimental air UFD we use very conservative 0.5kV/mm.

The UFD instantaneous voltage withstand becomes the linear reference voltage. This signal is then discretized in the nearest level control (NLC) block which considers the available SAs to produce reference signal for the controller. The number of arresters is inserted such that the voltage across arresters V_{arr} (also voltage across contacts of the UFD) is equal to the voltage reference.

The block diagram of the proposed voltage controller based on PI control is shown in Fig. 4 where, N_V is the number of arresters to be inserted during the voltage control. This figure also shows the fault current limiting controller which is discussed in Section F. The final output of the controller are the T_2 gate signals, which indicate arresters to be inserted. The number of inserted arresters is also plotted in Fig. 3.Current rising interval $0<t<T_{sep}$

The time to contact separation T_{sep} can be determined from simulations, or experimentally. In this interval the current rise is governed by the same equation as in (2). The current at the end of this period I_{sep} is determined by replacing T_{sep} in (2). There is no energy dissipation during this period.

D. Current rising interval $T_{sep} <t<T_{ufd}$

Considering analysis in Fig. 3, we represent arrester voltage as a liner function of time as:

$$V_{arr} = K \times t \tag{8}$$

This simplification is based on two assumptions:

1. There is an infinite number of steps,
2. Arrester voltage is constant, and identical for all cells in each step.

By replacing (8) in (3) the current expression is

$$I_{dc} = \frac{V_{dc}}{R_f}\left(1-e^{-\alpha t}\right) + I_{sep}e^{-\alpha t} - \frac{K}{L\alpha^2}\left(\alpha t + e^{-\alpha t} - 1\right). \tag{9}$$

The time when peak fault current occurs T_p, can be calculated by equating first derivative of (9) with zero:

$$T_p = -\left(Ln\,A\right)/\alpha \tag{10}$$

where, $A = K/\left(\alpha V_{dc} - R_f \alpha I_{sep} + K\right)$. By replacing (10) into (9) the peak fault current can be calculated as:

$$I_p = \frac{V_{dc}}{R_f}\left(1-A\right) + I_{sep}A - \frac{K}{L_{dc}\alpha^2}\left(-LnA + A - 1\right). \tag{11}$$

The current value at the end of contact opening interval I_{ufd} is lower than peak value I_p with the proposed control. It is determined by replacing T_{ufd} in (9). The energy dissipation in this interval is obtained as:

$$E_{arr1} = B\left(\frac{KV_{dc}}{R_f} - I_{sep}K - \frac{K^2}{L_{dc}\alpha^2}\right) + \frac{\left(T_{ufd}-T_{sep}\right)^2}{2}\left(\frac{KV_{dc}}{R_f} - \frac{K^2}{L_{dc}\alpha^2} + 1\right) + \frac{K^2\left(T_{ufd}-T_{sep}\right)^3}{3L_{dc}\alpha} \tag{12}$$

where, $B = \frac{1}{\alpha^2}(\alpha T_{ufd} - \alpha T_{sep} + 1)e^{-\alpha(T_{ufd}-T_{sep})}$.

E. Current falling interval $T_{ufd} < t < T_{br}$

In this interval, current decreases from I_{ufd} to zero, while all surge arresters are inserted. Therefore using the same method as in (4) the time to current zero is:

$$T_{br} - T_{ufd} = \frac{1}{\alpha} Ln\left(\frac{0.5V_{dc} + R_f I_{ufd}}{0.5V_{dc}}\right) \tag{13}$$

The energy dissipation can be calculated as in (5):

$$E_{arr2} = \frac{3V_{dc}^2}{4R_f}\left(T_{br} - T_{ufd} + \frac{e^{-\alpha T_{br} + \alpha T_{ufd}} - 1}{\alpha}\right) - \frac{3V_{dc}I_0}{2\alpha}\left(e^{-\alpha T_{br} + \alpha T_{ufd}} - 1\right) \tag{14}$$

The above expressions are verified by comparing with PSCAD measured values, and responses are shown in Fig. 2. The PSCAD results are plotted with dotted lines, while the analytical results are plotted with solid lines. It is seen that accuracy is good. The discrepancies occur at lower currents, which is a consequence of approximating arrester voltage with a fixed voltage in (8). At lower currents, the arrester voltage may not reach saturation values.

F. Coordination of voltage control and current control

One of the advantages of the HCB is the current controlling mode [7], [9]. The current control mode is also implemented in this study. A seamless transition between voltage and current control mode can be achieved by selecting minimum number of arresters between the two controllers as shown in Fig. 4. This ensures that once the trip signal is received the controller begins in voltage control and once all the arresters are inserted it moves to current control mode. The current control mode lasts until the temperature exceeds threshold. A temperature estimation is implemented in controller for both: surge arresters and IGBTs in the main breaker, and HCB moves to open state when either temperature approaches threshold. If no current regulation is needed (just HCB tripping), then user sets $I_{ref} = 0$.

IV. PSCAD Simulation Results

A 320kV, 16kA HCB is modeled in PSCAD with firm dc source representing dc bus. We have selected 8 cells (each has its own SA) of 40kV each. This represents a difficult control case because of coarse voltage adjustment, while it is likely that in practice many more cells will be used.

The short circuit tests have been carried out on the model with conventional control and with the proposed voltage control. The results are shown in Fig. 5. The fault is initiated at time t=0. With conventional control, the main breaker T_2 turns OFF once the UFD is fully open, which occurs at 3ms. At this time all the arresters are inserted in the circuit and the peak current reaches 9.5kA.

In the case of proposed voltage control the arresters are inserted earlier, based on the contact separation of the UFD. The current reduction therefore starts earlier, and the peak current in this case reaches 6.8kA. The energy dissipation in the arresters reduces from conventional 14MJ to 8.5MJ with the proposed control. The total breaking time is also better with the proposed control. The stepped voltage waveform indicates the quality of contact voltage control.

Fig. 6 shows the simulation of the proposed control, when coordinated with current limiting mode. It is seen in Fig. 6 (a) that firstly the controller works in voltage control mode and then it moves to current control by inserting all arresters (since current is high). Once current drops below current reference (2kA), the controller inserts different number of cells to keep current at the reference. The current is regulated until the energy dissipation in the arresters reaches the pre-set limit. At this time all the arresters are inserted and the controller proceeds to open the RCB.

During the voltage control, the arrester voltage increases in steps, which however are not uniform. The update rate of the controller is every 100μs, and at each instant the number of inserted arresters is rounded depending on the estimated voltage of inserted arresters using NLC method. This rounding results that steps can be shortened or widen.

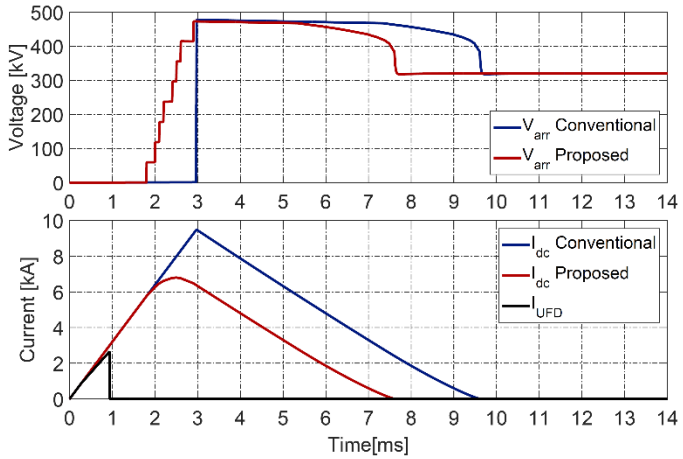
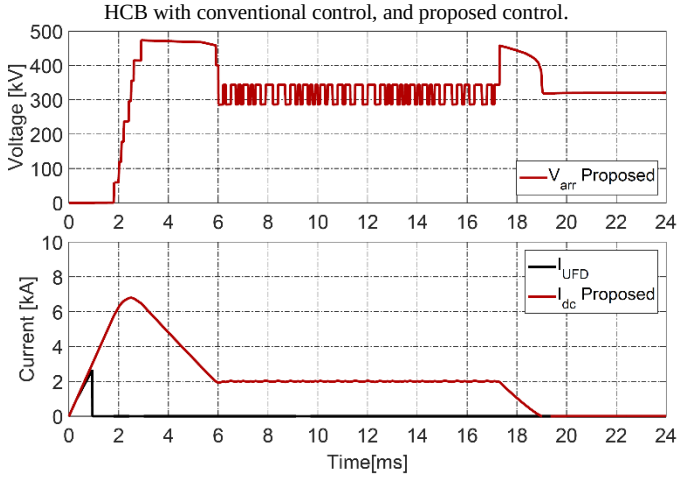
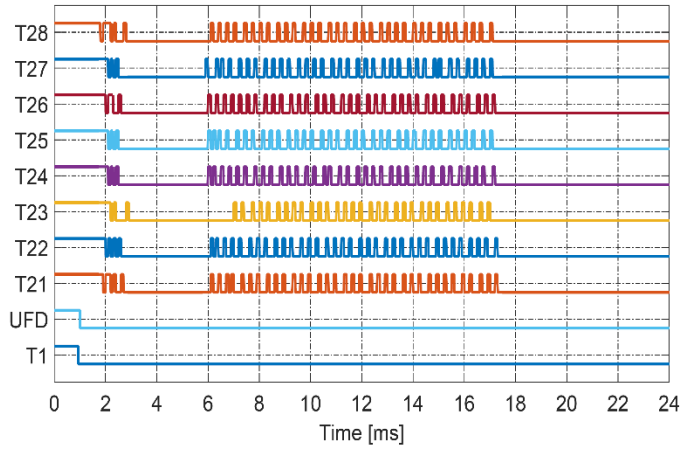


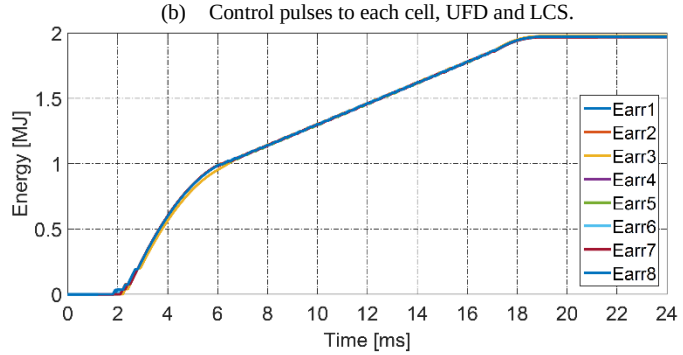
Fig. 5. PSCAD simulation results of UFD voltage and dc current of the HCB with conventional control, and proposed control.



(a) HCB Voltage and current,



(b) Control pulses to each cell, UFD and LCS.



(c) Energy dissipation in each arrester,

Fig. 6. Simulation of voltage control coordinated with current limiting.

The gating signals for the IGBTs in T2, the IGBTs in LCS T1, and the UFD command are shown in Fig. 6(b), where the voltage control mode is present from 2ms to 4ms, while the current control is depicted from 6ms to 17ms.

In the proposed control method a number of arresters are inserted depending on the required contact voltage. This means that the energy dissipations in different arresters are different. To ensure that all the arresters equally share energy and temperature increase, an energy balancing control is developed. The method is explained in [9] and [16]. The energy dissipation in arresters is shown in Fig. 6 (c). It is seen that the individual energies are very close to each other except during the voltage control (2-4ms). In this interval there are limited number of rotations available for balancing, because of time restriction, switching rate and small number of arresters.

A. Effect of the proposed method on reducing the size of current limiting inductor L_{dc}

It was shown in the previous sections that the proposed control reduces the peak fault current and energy dissipation in the surge arresters. Alternatively, it is possible to reduce the size of the current limiting inductor (L_{dc}) such that the same peak current as in the conventional control is obtained.

Firstly, the influence of inductor size is analyzed, based on parametric study using the analytical model. Fig. 7 shows the peak current and energy dissipation for a range of inductance values for the considered test case. The peak current and the total dissipated energy reduce as the inductance is increased (for same HCB operating time) as expected. It is seen that the relative current reduction is similar for all inductances.

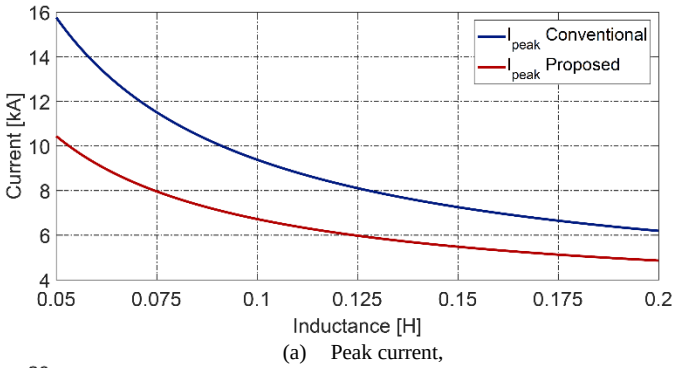
It can be seen from Fig. 7(a) that with the proposed method and the inductance of *58mH* it is possible to obtain the same peak current as in the conventional control with *100mH*.

Fig. 7(b) shows the total energy dissipation in the arresters which is compared against the results obtained from PSCAD. It can be seen that the accuracy of analytical model for energy dissipated is lower, but within 5% and 14% in conventional and proposed methods respectively. Fig. 7(b) enables comparison of energy dissipation. Considering the same case that *100mH* is replaced with *58mH* in the proposed control (to obtain the same peak current), the proposed method further reduces the energy dissipation by more than 29%.

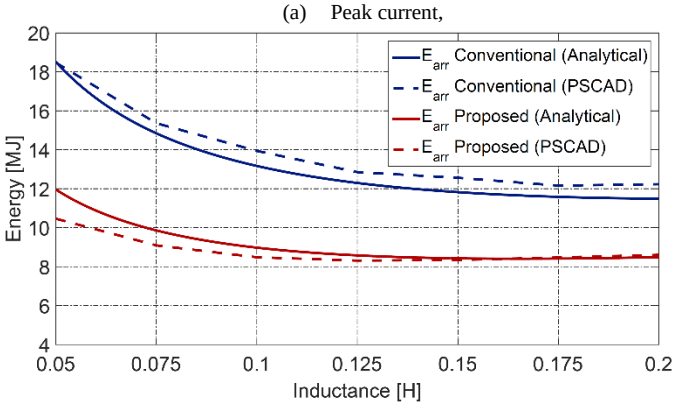
V. Experimental Verification

A. Hardware test circuit

The HCB 320kV chopper-based test circuit is discussed in [17], but some further modifications are made for the laboratory low-voltage demonstrator and the circuit diagram is illustrated in Fig. 8. Fig. 9 shows the picture while the parameters are given in Table III. It consists of a 900V, 30A AC-DC power converter with a 7mF capacitor bank which can supply a fault current up to 1kA. The HCB configuration is the same as given in Fig. 1 and the peak fault current is 500A. The number of IGBTs in T2 is 8. The IGBT switches, arresters and the UFD are shown in Fig. 10, where Fig. 10(a) shows four IGBTs (in white) and arresters (in blue), while another 4-cell module is not shown. The UFD is shown in Fig. 10(b), while the UFD design is discussed in more detail in [15].



(a) Peak current,



(b) Energy dissipation,

Fig. 7. Improvements with proposed control for different series inductance.

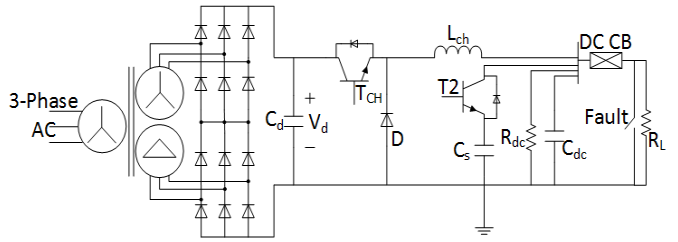


Fig. 8. Chopper-based HCB test circuit in the laboratory.

B. Energy balancing implementation

The energy balancing keeps track of all the energy dissipations in the arresters and tries to insert the arrester with least energy dissipation. This is done every 100μs (f_s=10kHz).

To implement the energy balancing, the measurement of current through and voltage across each of the arresters are needed. The number of required voltage and current sensors is high, and a simpler method is used here which needs only the available current sensor I_{dc} and voltage sensor V_{arr}. Based on the number of arresters inserted (N), and the gating signal of each IGBTs (G_{T2i}) the voltage and the current of each arrester are calculated as:

$$I_{arri} = I_{dc}\left(1-G_{T2i}\right), \qquad V_{arri} = \frac{V_{arr}}{N}\left(1-G_{T2i}\right)$$
$$P_{arri} = V_{arri} I_{arri}, \qquad E_{arri} = \int_0^t P_{arri}\,dt \tag{15}$$

where i denotes the i^{th} arrester. This method is valid with the assumption that all the arresters are identical and have the same thermal characteristics. In our hardware testing, the accuracy of this method has been verified by measuring temperature on individual arresters, although the method may not be sufficiently reliable on high voltage systems.

C. Testing voltage control

Fig. 11(a) shows the arresters voltages and dc current for the cases with conventional and proposed control. It can be seen that the peak current is reduced from 500A to 366A. Additionally, the arresters' voltage magnitude and break time are reduced with the proposed control. The measured UFD

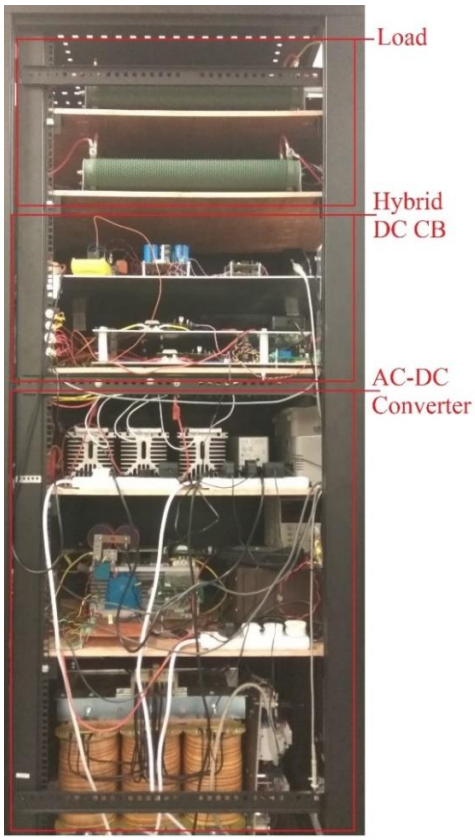
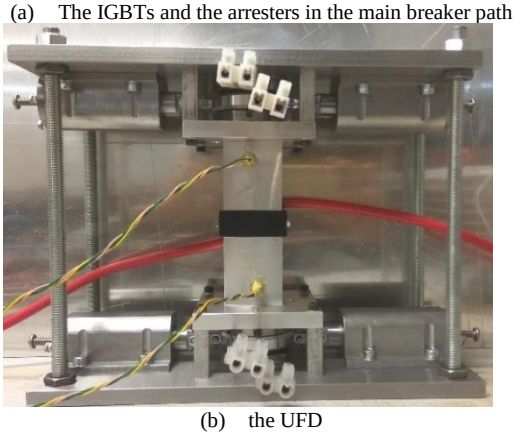


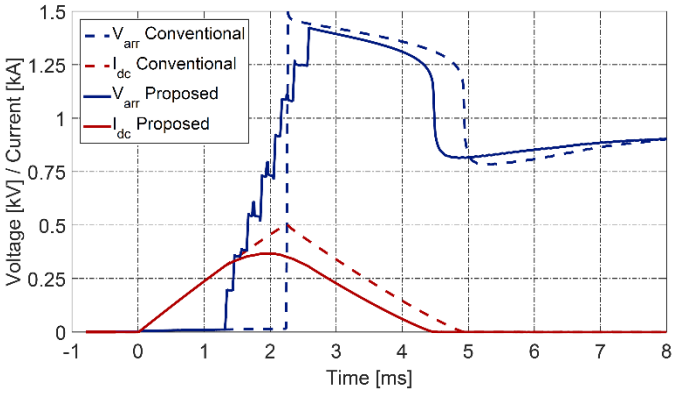
Fig. 9. Experimental HCB test circuit, with HCB and resistor load.

(a) The IGBTs and the arresters in the main breaker path

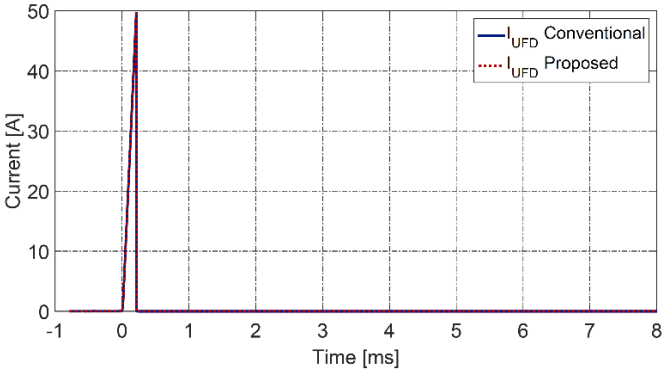


(b) the UFD

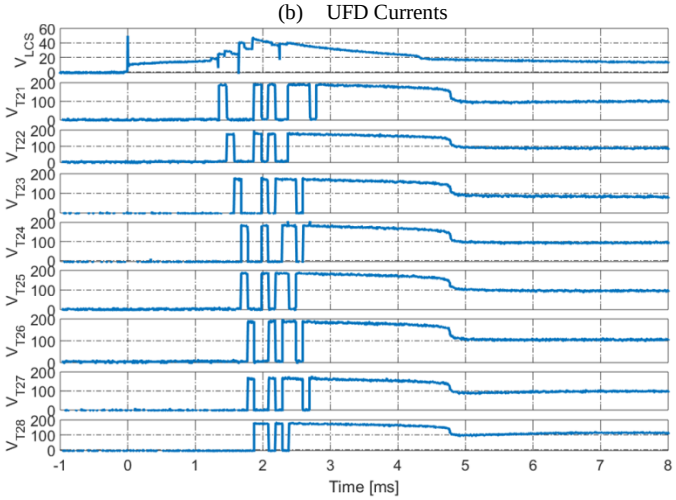
Fig. 10. Components of the experimental HCB.



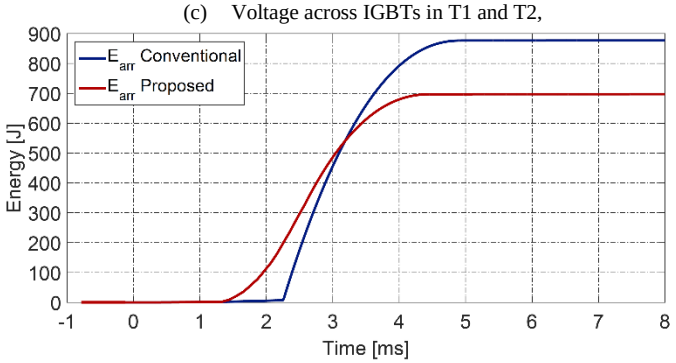
(a) Arrester voltage and dc current



(b) UFD Currents



(c) Voltage across IGBTs in T1 and T2,



(d) Total energy in surge arresters,

Fig. 11. HCB experimental results with conventional and proposed controls.

current is shown in Fig. 11(b), which confirms that there is no arcing or re-striking in UFD. The voltage across the IGBTs in LCS and the main breaker T_2 are shown in Fig. 11(c). It can be seen that the LCS voltage has spikes because of parasitic inductances, but it is limited to 50V by the LCS arrester. The voltages across each T2 arrester are limited to around 180V.

Fig. 11(d) shows that the energy dissipation starts earlier with the proposed control and the overall dissipation is smaller compared with conventional control. The overall energy dissipations are 869J and 694J for the conventional and proposed controls respectively.

D. Testing the combined voltage and current controls

The combined voltage and current control from Fig. 4 is also implemented on hardware. The test results are shown in Fig. 12. This test is carried out at loading condition and fault is applied at t=0. It can be seen that the voltage controller inserts a proper number of the arresters in the current rising period. Once all the arresters are inserted, the current controller is activated and controls the current to the reference value (30A). Once the energy dissipation reaches the preset limit, the controller inserts all the arresters and proceeds to open state.

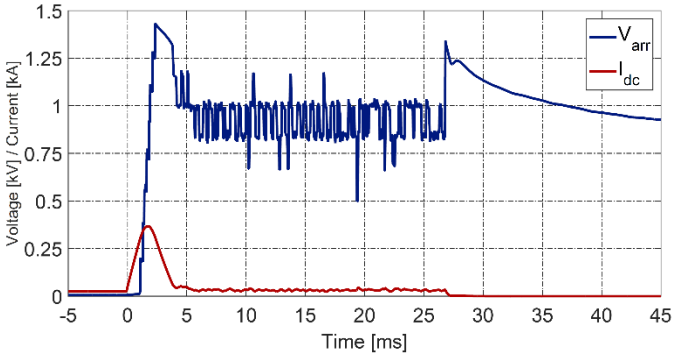


Fig. 12. Experimental results of integrated UFD voltage and dc current control.

VI. Conclusion

It is emphasized in this study that peak fault current and energy dissipation play significant role in dc grid protection development. A voltage control method for HCB is proposed as an effective method of reducing peak current. The proposed control measures the UFD contact separation while contacts are moving and regulates the voltage across contacts at the required withstand capability. This is achieved by inserting different number of surge arresters. The proposed control is verified using PSCAD simulation and also on 900V, 500A experimental hardware. The analytical model is also presented and by comparing with PSCAD results, it is concluded that accuracy is good. The experimental results showed that the proposed control is able to reduce the peak fault current by 28.8% and reduces the energy dissipation in the arresters by 20%. The PSCAD simulation results also confirm that the proposed method can reduce the size of the current limiting inductor by 42%.

VII. Appendix. 320kV, and 900V test systems

Table I Parameters of the 320kV, 16kA HCB.

SL.NO.	PARAMETER	VALUE
1	Voltage rating	320kV
2	Current rating	2kA
3	Maximum Breaking current	16kA
4	UFD operation time	2ms
5	Number of IGBT modules in T_2	8
6	Conventional breaking operation time	2ms
7	Limiting inductor L_{dc}	100mH

Table II Parameters of the 900V, 500A UFD in experimental DCCB.

SL.NO.	PARAMETER	VALUE
1	Thomson coil inductance	3.5µH
2	Number of turns in Thomson coil	8.5
3	Contact distance	3mm
4	Mutual inductance per m	40µH/m
5	Friction coefficient	20Ns/m
6	Mass of contacts	0.1kg
7	Bistable spring	29N/mm
8	UFD supply voltage	100V
9	UFD peak current	3.5kA
10	UFD driver capacitance	7.29mF

Table III. Parameters of the 900V, 500A experimental test circuit.

SL.NO.	PARAMETER	VALUE
1	Input Transformer	415V, 3phase-Y/Δ
2	Chopper Input dc voltage	V_d = 1170V
3	Chopper inductor	L_{ch} = 3.5mH
4	DC capacitor bank	C_{dc} = 7mF
5	Carrier frequency	f_s = 10kHz
6	Chopper output voltage	V_{dc} = 900V
7	Load current rating	I_l = 25A
8	Rate fault current	If=500A
9	Resistor load	R_l = 35Ω
10	Input capacitor	C_d = 20µF
11	DC Capacitor	C_s = 40µF
12	DC Resistor	R_{dc} = 1kΩ

VIII. Acknowledgment

The authors are thankful to Mr R. Osborne for help with the experimental studies.

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X. Biographies

Mohammadhassan Hedayati (S'14-M'16) He received his B.Tech. degree in electrical engineering from the Islamic Azad University, Kazeroon, Iran, in 2006. He received his ME and PhD. degrees from Indian Institute of Science (IISc) Bangalore, India in 2010 and 2015 respectively. He is currently a research fellow at University of Aberdeen, Aberdeen, UK. His primary areas of interests are in Hybrid DCCB, power electronics, motor drives, active damping, common mode and EMI filters and high-power converters.

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