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ΚΑΙ ΜΗΧΑΝΙΚΩΝ Η/Υ

Σχεδιασμός διαφορικού ταλαντωτή στα 16GHz σε FinFET τεχνολογία 16nm

Design of a 16nm FinFET 16GHz differential LC-VCO

Μεταπτυχιακή Διατριβή

Ιωάννης Φ. Ζωγραφόπουλος

Επιβλέποντες Καθηγητές: Πλέσσας Φώτιος
Επίκουρος Καθηγητής

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Ευμορφόπουλος Νέστωρ
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Βόλος, Οκτώβριος 2015

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Μεταπτυχιακή Διατριβή για την απόκτηση του Μεταπτυχιακού Διπλώματος Ειδίκευσης «Επιστήμη και Τεχνολογία Υπολογιστών, Τηλεπικοινωνιών και Δικτύων» του Πανεπιστημίου Θεσσαλίας, στα πλαίσια του Προγράμματος Μεταπτυχιακών Σπουδών του Τμήματος Μηχανικών Η/Υ, Τηλεπικοινωνιών και Δικτύων του Πανεπιστημίου Θεσσαλίας.

……..

Ιωάννης Φ. Ζωγραφόπουλος

Διπλωματούχος Μηχανικός Ηλεκτρονικών Υπολογιστών, Τηλεπικοινωνιών και Δικτύων, Πανεπιστημίου Θεσσαλίας

Στον αγαπημένο μου πατέρα,

Ευχαριστίες

Με την ολοκλήρωση αυτής της μεταπτυχιακής εργασίας, θα ήθελα να ευχαριστήσω ιδιαίτερα τον επιβλέποντα καθηγητή μου, **κ. Πλέσσα Φώτιο**, για την άψογη συνεργασία που είχαμε τα τελευταία 3 χρόνια των σπουδών μου, για τις γνώσεις που μου μετέδωσε αλλά και για την εμπιστοσύνη που έδειξε στο πρόσωπό μου. Είναι βέβαιο πως χωρίς την καθοδήγησή του και τις σημαντικές υποδείξεις του αυτή η εργασία δεν θα μπορούσε να περατωθεί.

Επίσης, θα ήθελα να ευχαριστήσω θερμά τους επιβλέποντες της μεταπτυχιακής μου **κ. Σταμούλη Γεώργιο** και **κ. Ευμορφόπουλο Νέστωρ**.

Επιπρόσθετα, θέλω να ευχαριστήσω του φίλους μου για την υποστήριξη και βοήθειά τους σε όλη την διάρκεια των σπουδών μου.

Τέλος, δεν θα μπορούσα να παραλείψω την οικογένεια μου, η οποία δεν έπαψε στιγμή να με στηρίζει και να εμπιστεύεται τις ικανότητές μου. Φρόντισε να μου εξασφαλίσει όλα τα απαραίτητα εφόδια για να μπορέσω, από μέρους μου, να αφιερώσω όλο το χρόνο στις σπουδές μου. Είναι βέβαιο, πως χωρίς την αμέριστη κατανόηση και βοήθειά της δεν θα τα είχα καταφέρει.

Ιωάννης Φ. Ζωγραφόπουλος

Βόλος, 2015

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Acronyms

pMos	Positive-Channel Metal Oxide Semiconductor
nMos	Negative-Channel Metal Oxide Semiconductor
cMos	Complementary Metal Oxide Semiconductor
FinFET	Fin-Shaped Field Effect Transistor
MosFET	Metal Oxide Semiconductor Field Effect Transistor
MG	Multi-gate
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration
IC	Integrated Circuits
DC	Direct Current
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
PTM	Predictive Technology Model
SNR	Signal to Noise Ratio
Q	Quality Factor
Dbc	Decibels relative to the carrier
PLL	Phase Locked Loop
HB	Harmonic Balance
RD	Resistively Degenerated

Περίληψη

Στην παρούσα μεταπτυχιακή διατριβή παρουσιάζεται ο σχεδιασμός και η προσομοίωση ενός διαφορικού FinFET LC-tank ταλαντωτή με συχνότητα λειτουργίας τα 16GHz. Τα κυκλώματα που θα παρουσιαστούν μελετήθηκαν ως προς τα βασικά τους χαρακτηριστικά (κατανάλωση ισχύος, απόκριση συχνότητας, απόκριση θορύβου) και έγινε προσπάθεια βελτίωσης της συνολικής τους απόδοσης, όπου αυτό ήταν δυνατόν.

Η υλοποίηση και προσομοίωση των κυκλωμάτων γίνεται με χρήση του λογισμικού Keysight ADS(Advanced Design System) και η τεχνολογία που θα χρησιμοποιήσουμε για τον σχεδιασμό των κυκλωμάτων έχει μήκος καναλιού(L) 16nm και προκαθορισμένη τάση τροφοδοσίας τα 0.85V. Δυστυχώς, επειδή κατά την περίοδο συγγραφής της διατριβής βιβλιοθήκες για τόσο μικρές τεχνολογίες ολοκλήρωσης δεν υπήρχαν διαθέσιμες, όλη η μελέτη θα βασιστεί σε μοντέλα πρόβλεψης της συμπεριφοράς των τρανζίστορ(PTMs) [1] τα οποία είναι διαθέσιμα στο σύνδεσμο **ptm.asu.edu/.**

Λέξεις Κλειδιά:

Ταλαντωτής, διαφορικός ταλαντωτής, cross-coupled LC-tank, FinFET 16nm, καθρέφτης ρεύματος, θόρυβος φάσης, φιλτράρισμα θορύβου, αρμονικές συχνότητες

Abstract

In this master thesis, the design and simulation of a 16GHz FinFET differential LC-tank Voltage Controlled Oscillator(VCO) is presented. The featured designs' evaluation is based on their most important characteristics (ie. power consumption, frequency response, phase noise performance) and we will attempt to improve their overall performance where it is feasible.

For the implementation and simulation of the previously mentioned designs, Keysight Technologies ADS(Advanced Design System) was used. Furthermore, the integration technology used for the simulations presents a 16nm Channel Length(L) while the predetermined voltage supply is set at 0.85V. Unfortunately, at the time this thesis tool place, library files for such integration technologies where not available, thus the overall study will be based on Predictive Technology Models(PTMs) [1] which are online available at **ptm.asu.edu/.**

Keywords:

Oscillator, Differential Oscillator, cross-coupled LC-tank, FinFET 16nm, current mirror, phase noise, phase noise filtering, harmonic frequencies

Chapter 1
Introduction

1.1 Problem Formulation

In recent days, due to the immense growth of both wireless and optical telecommunications systems, low-phase noise high Frequency oscillator units have become a necessity. Local Oscillators with as low as possible phase noise are useful to Radio Frequency(RF) transceivers' design, where the information signal is modulated or demodulated. During this process the bit-error-rate(BER) characteristic is highly dependent on the phase noise added by the VCO.

Oscillators are electronic circuits that produce periodical signals, usually sinusoidal or pulses. The frequency of these signals is solely determined by the discrete values of the components constituting the oscillator without the need for any other input to the circuit. Additionally, we could say that oscillator circuits convert the DC current which supplies the circuit into the power of the alternating signal.

Furthermore, oscillators are widely used in many electronic devices, some applications are in radio and TV signal transmitters, as clock references for digital and analog ICs, in biomedical devices such as pacemakers, in waveform generators which are an irreplaceable instruments of every electronics lab, in Quartz watch mechanisms, in musical instruments and other.

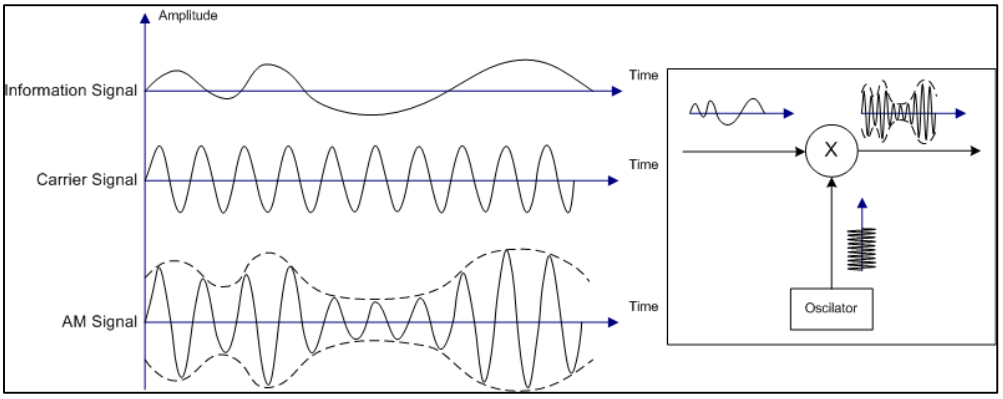


Figure 1.1 Oscillator Contribution at **AM-Modulation** of an information signal

1.2 Related Work and Contribution

In this work, apart from designing and simulating our circuit we will implement and evaluate different methods to improve some of the most critical characteristics which govern a VCO's performance. Although, some of these methods are well-known and provide noticeable enhancements for integration technologies above 65nm, for smaller dimensions these optimizations are not widely adapted due to the complexity they introduce to the design .

Having in mind the constraints induced by 16nm technology and the specifications for a low-phase noise 16GHz differential LC-VCO, we will outline and measure the improvement these optimizations provided to our circuit design and compare it with similar works. In this process, harmonic filtering and transistor-sizing possess significant roles and emphasis will be given towards this direction.

Furthermore, the factors that directly affect phase noise will be discussed and methods to lessen their affect, as well as metrics to measure the improvement will be introduced in order to have a reference for comparison with other similar state-of-the- art designs.

1.3 Outline

In ***Chapter 2***, some oscillator fundamentals are provided such as the categories in which we can separate them and the main differences of each topology. Further, some really important VCO working principles are mentioned, regarding the initiation of the oscillation, how and under which circumstances the amplitude is stabilized. Moreover, the variables regarding the oscillation frequency and their effects are presented.

In ***Chapter 3***, the 16nm FinFET transistor evaluation, under certain biasing circumstances, takes place. Also some basic information on FinFET transistors which will be of great importance for the simulations that will take place afterwards will be given. Different LC-tank configurations will be evaluated and a current source consisting of transistors of the previously mentioned technology will substitute the ideal current source we used in the first stages of the simulations.

In ***Chapter 4***, the concept of phase noise is introduced and what effect it has on the overall circuit performance. The variables that directly affect phase noise are stated and different methods to alleviate their impact are used in conjunction with the simulation results they yielded.

In ***Chapter 5***, the conclusions gathered from all the previous simulations are discussed and the overall performance improvements are noted. Further, a comparison with other similar works is provided.

In ***Chapter 6***, we wrap up all the steps we followed in this thesis and report some aspects of the design that future work could provide even better performance depending on the application the VCO is intended for.

Chapter 2

VCO Overview

2.1 Introduction

Oscillators are some of the most principal circuits in electronics. They are mainly used in telecommunications systems both in the transmitters and the receivers. Their frequency range is vast as we can find oscillators with frequencies varying from some Hz to even tens of GHz. Depending on the circuit implementation, an oscillator will operate in a very narrow range around its center frequency, although ideally we would like it to operate only on this specific frequency(f_o).

Some of the main components consisting any oscillator topology under review are the following:

- The power supply of the circuit
- An amplification stageΈνα κύκλωμα ενισχυτή
- A resonant circuit(in our case the LC-tank)
- A **positive** feedback

Fundamental working principle for initiation of oscillations is a positive feedback loop, which in turn means that a proportion of our output signal is fed back to the input of our oscillator. However, this is not enough since the signal proportion that is fed back needs to be in-phase with the input signal (phase difference 0^o or 360^o). Additionally, closed loop gain should be equal to unity in order to preserve oscillation.

Note: As we have mentioned in order to preserve oscillation a zero-phase positive feedback with unity gain around the loop is a prerequisite. However, in order for the oscillations to start and be sustained, gain should be even greater than unity in order for the output signal to reach a desired amplitude (resonator non-idealities should also be taken into account). Once the signal reaches this state, the oscillator is now self-resonating.

Barkhausen Stability Criterion

The condition to preserve oscillation is **|β.A|=1**

A= gain of the amplification stage

β= the portion of the signal that is returned through the positive feedback loop

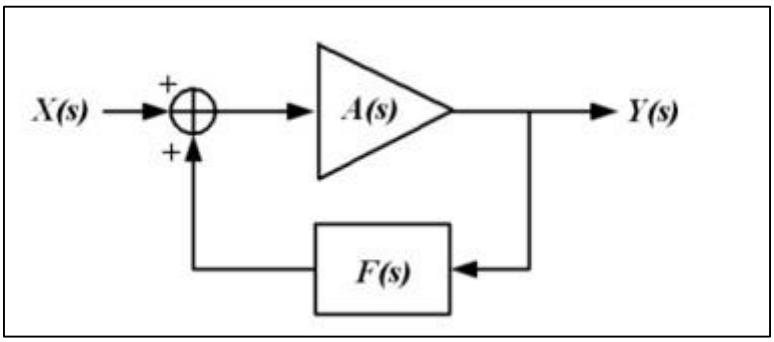


Figure 2.1 Positive Feedback Loop with Frequency selection network F(s)

Two main oscillator topologies are presented in the next two sections VCO:

- Resonant Oscillators
- Waveform Oscillators

The advantages and disadvantages of each one of these mentioned topologies will be outlined, and should be a guide when selecting the appropriate circuit block to meet the design specifications.

2.2 Resonant Oscillator Topologies

- **Resonant Amplifier**

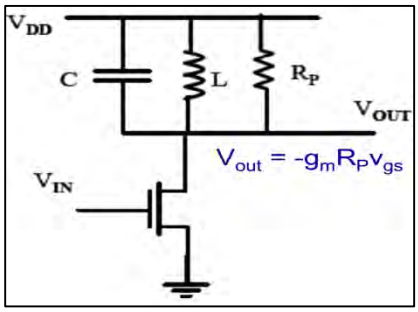


Figure 2.2 Resonant Amplifier

The impedance of the resonant circuit (LC) reaches its maximum, which is equal to Rp and the phase difference is 0^o or 360^o at the resonant frequency. Additionally, at resonance the imaginary parts of the conductance, induced by the LC components, are equal to zero.

- **In-Series Resonant Amplifiers(with Feedback loop)**

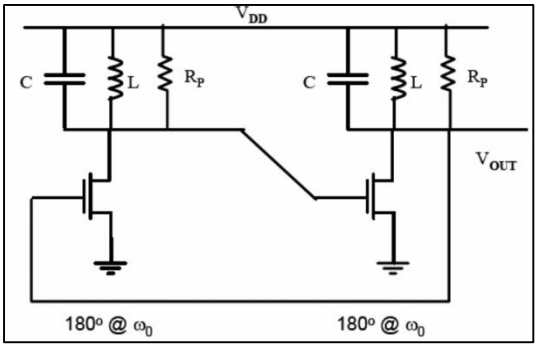


Figure 2.3 In-Series Resonant Amplifiers

Placing two of the previously mentioned amplifiers in series we arrive at the topology presented in Figure 2.3, which in order to oscillate we must have a unity gain amplification(even greater than unity in the beginning) and an in-phase positive feedback loop. Of course, our circuit can only oscillate at ω_0, since the condition for 0^o phase difference can only be satisfied around this frequency. Furthermore, the feedback "going through" the amplification stage constitutes the oscillation generator. The amplitude of the oscillations will gradually start to grow (as we can easily observe in the upcoming transient

simulations) until it will saturate due to the finite value of the current source (in theory it would built up to infinity).

- **Cross-Coupled Oscillator**

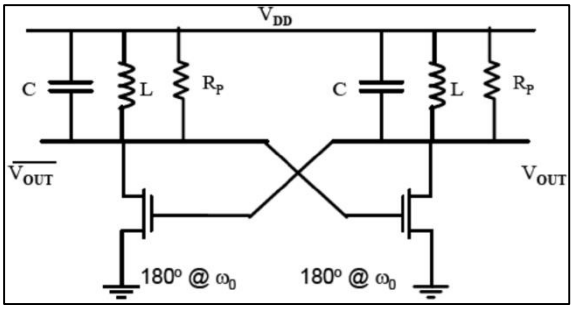


Figure 2.4 Cross-Coupled Oscillator

With few changes to the previous topology, with the resonant amplifiers, we can end up with the above cross-coupled oscillator. The cross-coupled oscillator topology will be examined in detail in this work.

The main differences we can observe in this topology have to do with the differential nature it presents. Since we mentioned differential Oscillator, it is reasonable to have two outputs, one complementary to the other, or more simply put with an 180^0 phase difference. The advantages of such topologies are well known and in our case we decided to examine this circuit due to the low phase noise, high CMRR (Common Mode Rejection Ratio) as well as high PSRR(Power Supply Rejection Ratio) it produces, which are critical characteristics for high performance circuits.

- **Crystal Oscillator**

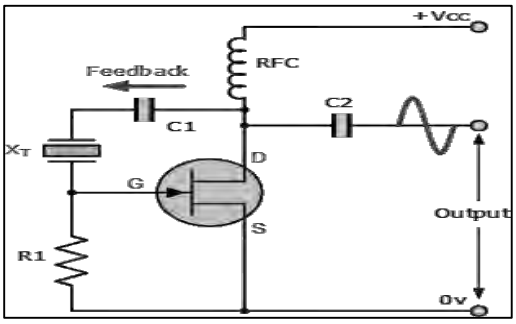


Figure 2.5 Crystal Oscillator

Crystal Oscillators are the most stable topology of all the previously mentioned and are therefore use in telecommunications systems where high stability is required. These oscillators use a piezo-electric crystal, usually quartz, and present inductive resistance over a very narrow frequency band. We can replace the LC resonator implemented in the previously proposed topologies with the crystal having a well-defined resonating frequency as a result. Due to the fact that quartz crystals present a really high quality factor (Q), when used as a frequency selection network it exhibits stable frequency response indifferent to temperature variations.

However, the usage of quartz crystal, which are discrete components and operate on a *fixed frequency*, has its drawbacks. In most applications, where we need a varying operating frequency, crystal oscillators cannot provide a viable solution.

2.3 Waveform Oscillator Topologies

- **Ring Oscillator**

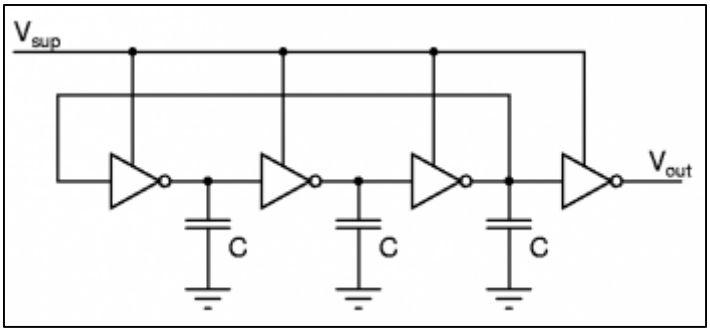


Figure 2.6 Ring Oscillator

Ring oscillators(RO) are the most popular topology used to produce pure digital output signals(pulses). ROs have been implemented in many applications, some having operating frequencies in the range of several GHz, due to their simplicity and ease of integration with other digital circuits.

Integration technology advances rapidly and high performance circuits are demanded, therefore ROs have started to take an ever-growing share in the oscillator market. They can provide high operating frequencies, crucial for wireless high data rate communications, with a very simple topology. Their simplicity in addition to the fact that no external components i.e. inductors are needed, proves to be their greatest asset. Their architecture is purely based on transistors, thus leaving a smaller footprint on the silicon than any other oscillator topology.

Inspecting closely a RO, we can understand that in fact it consists of an **odd** number of series inverters forming a feedback loop. A high input signal is propagated through the several stages of inverters, and after the delay they induced, a low signal is provided at the output of our circuit. This low signal is fed back to the input through the loop connecting the first and last inverters of the chain having as a result a pulse waveform at the output. All the preceding, summarize the operation principle of this topology.

- **Relaxation Oscillator**

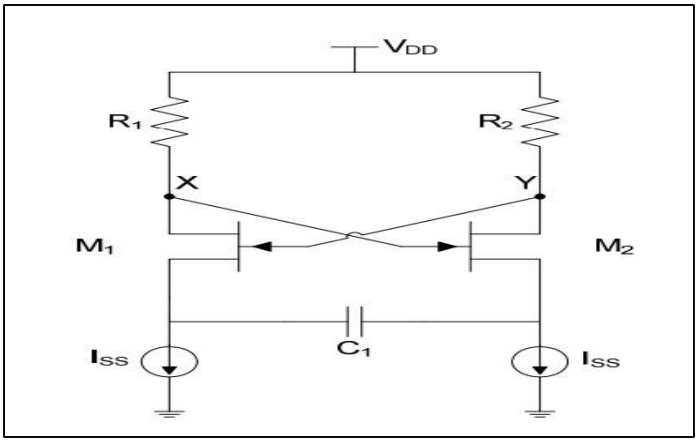


Figure 2.7 Relaxation Oscillator

Another widely used circuit to realize a digital output oscillator is the relaxation oscillator. In this topology, a capacitor or inductor, with defined time constant, is charged gradually and then is abruptly discharged forming the output signal. Varying the capacitor's time constant, using a current source for example, we can set the oscillation frequency. The most common outputs of a relaxation oscillator are pulses or ramps (saw tooth outputs).

2.4 Resonant Oscillators VS Waveform Oscillators

Ideally any of the previously mentioned VCO topologies could be used in any application. However, knowing the key assets of each circuit can help us select the best topology which will meet or even exceed the design specifications. When selecting the *best* topology for our design constraints, some features we should take into account are the following:

- Low phase noise or jitter
- Low power consumption
- Wide tuning range
- Integration simplicity
- Small die area foot print
- High operation frequency(GHz)

Depending on the application where our design will be implemented the previous features receive different priorities. However, we proceed with the circuit knowing that in order to meet our goals some features will be sacrificed so others can be optimized (trade off).

Additionally, before designing or simulating our circuit, knowing if a waveform or resonant oscillator will be used, can help us have a first insight on the performance of our circuit as far as the previous metrics are concerned.

In the following table, some of the most obvious advantages and disadvantages of the mentioned oscillator categories are presented.

Note: In the following table the comparison is held between LC-tank and Ring oscillators in purpose. We don't mention neither Crystal Oscillators nor Relaxation oscillators due to the fact that, the first can operate on a fixed frequency (poor tuning range performance) and the second proves to have very poor phase noise performance. Therefore, we avoid, whenever it is possible, these two topologies.

Ring VCO	LC-tank VCO
Advantages	
Integration simplicity (VLSI circuits)	Best phase noise or jitter performance
Low power consumption	High operating frequency
Wider tuning range	
Small die area	
Disadvantages	
Poor phase noise or jitter performance	Bigger die footprint(due to L,C)
Low operating frequency	Difficult integration(VLSI circuits)
	Higher power consumption

Table 1 Advantages/Disadvantages of LC and Ring oscillators

Despite the above categorization with regard to the advantages and disadvantages of each topology, proper design can help suffiently improve the performance of our circuits in every aspect.

Furthermore, from all the presented information we can easily assume that Ring oscillators are the most suitable topology for low power-small die area applications, while LC oscillators are irreplaceable in telecommunications where low phase noise is the determining design specification.

In this thesis, all the attention is drawn towards designing, simulating and improving the overall performance of an **LC-tank Cross-coupled** architecture, knowing in advance where this topology lacks and having made any possible tweak to minimize this effects.

Chapter 3

Circuit Design

3.1 Basics of FinFET Technology

FinFET technology has recently seen a major increase in adoption for use within integrated circuits. The FinFET technology promises to provide and deliver superior levels of scalability needed to ensure that the current progress with increased levels of integration within integrated circuits can be maintained.

FinFET technology has been born as a result of the relentless increase in the levels of integration. The basic tenet of Moore's law has held true for many years from the earliest years of integrated circuit technology. Essentially it states that the number of transistors on a given area of silicon doubles every two years. Some of the landmark chips of the relatively early integrated circuit era had a low transistor count even though they were advanced for the time. The 6800 microprocessor for example had just 5000 transistors. Todays have many orders of magnitude more.

To achieve the large increases in levels of integration, many parameters have changed. Fundamentally the feature sizes have reduced to enable more devices to be fabricated within a given area. However other Figures such as power dissipation, and line voltage have reduced along with increased frequency performance. There are limits to the scalability of the individual devices and as process technologies continued to shrink below 20 nm, it became impossible to achieve the proper scaling of various device parameters. Those like the power supply voltage, which is the dominant factor in determining dynamic power were particularly affected. It was found that optimizing for one variable such as performance resulted in unwanted compromises in other areas like power. It was therefore necessary to look at other more revolutionary options like a change in transistor structure from the traditional **planar** transistor.

FinFET technology takes its name from the fact that the FET structure used looks like a set of *fins* when viewed. The main characteristic of the FinFET is that it has a conducting channel wrapped by a thin silicon "fin" from which it gains its name. The thickness of the fin determines the effective channel length of the device. In terms of its structure, it typically has a vertical fin on a substrate which runs between a larger drain and source area. This protrudes vertically above the substrate as a fin.

The gate orientation is at right angles to the vertical fin. And to traverse from one side of the fin to the other it wraps over the fin, enabling it to interface with three side of the fin or channel. This form of gate structure provides improved electrical control over the channel conduction and it helps reduce leakage current levels and overcomes some other short-channel effects.

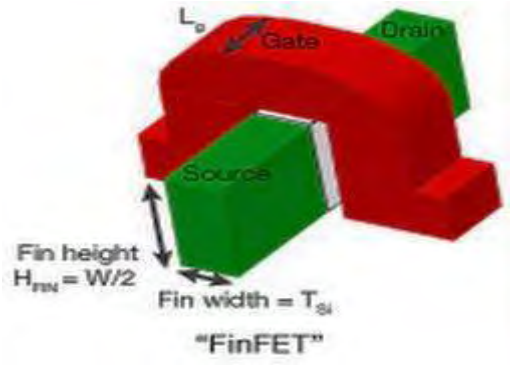


Figure 3.1 FinFET transistor structure

The term FinFET is used somewhat generically. Sometimes it is used to describe any fin-based, multigate transistor architecture regardless of number of gates.

There are many advantages to IC manufacturers of using FinFETs. The most important are listed in the following table.

PARAMETER	DETAILS
Power	Much lower power consumption allows high integration levels. Early adopters reported 150% improvements.
Operating voltage	FinFETs operate at a lower voltage as a result of their lower threshold voltage.
Feature sizes	Possible to pass through the 20nm barrier previously thought as an end point.
Static leakage current	Typically reduced by up to 90%
Operating speed	Often in excess of 30% faster than the non-FinFET versions.

Table 2 FinFET Advantages

The FinFET is a technology that is used within ICs. FinFETs are not available as discrete devices. However FinFET technology is becoming more widespread as feature sizes within integrated circuits fall and there is a growing need to provide very much higher levels of integration with less power consumption within integrated circuits.

As we have mentioned previously, our simulations were performed using Keysight ADS2014 (Advanced Design System), the channel length (L) of the integration technology was set to 16nm and voltage supply was 0.85V. Furthermore, this whole work is based on Predictive Technology Models (PTMs) which are available online at **ptm.asu.edu/.**

Before we start designing our circuit it is critical to explore our transistor's characteristics. We will perform a DC analysis to benchmark their performance, measure their threshold voltage, drain current Id versus gate-source and drain-source voltages and calculate the DC operating point which yields best results.

The following Figures present the DC biasing circuit for an nMOS transistor and its output characteristic graph. In our analysis we used the software tool FET Curve Tracer, which provides us with all the possible combinations of Id vs Vgs and Id vs Vds. In the first Figure we can also see the model card where all the variables of the integration technology are imported.

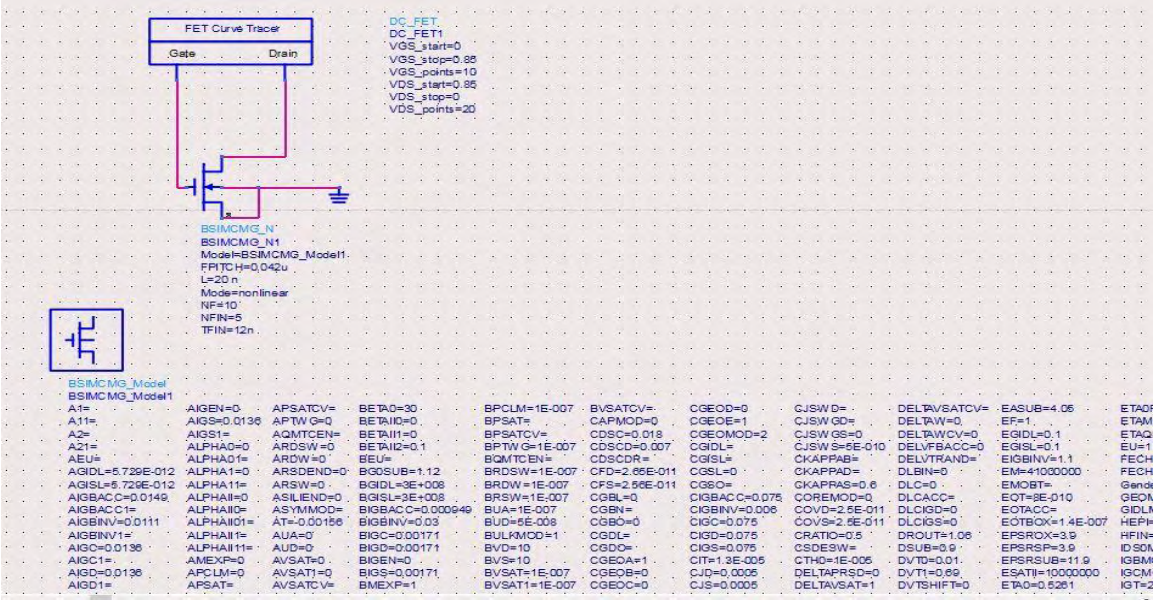


Figure 3.2 nMOS biasing circuit

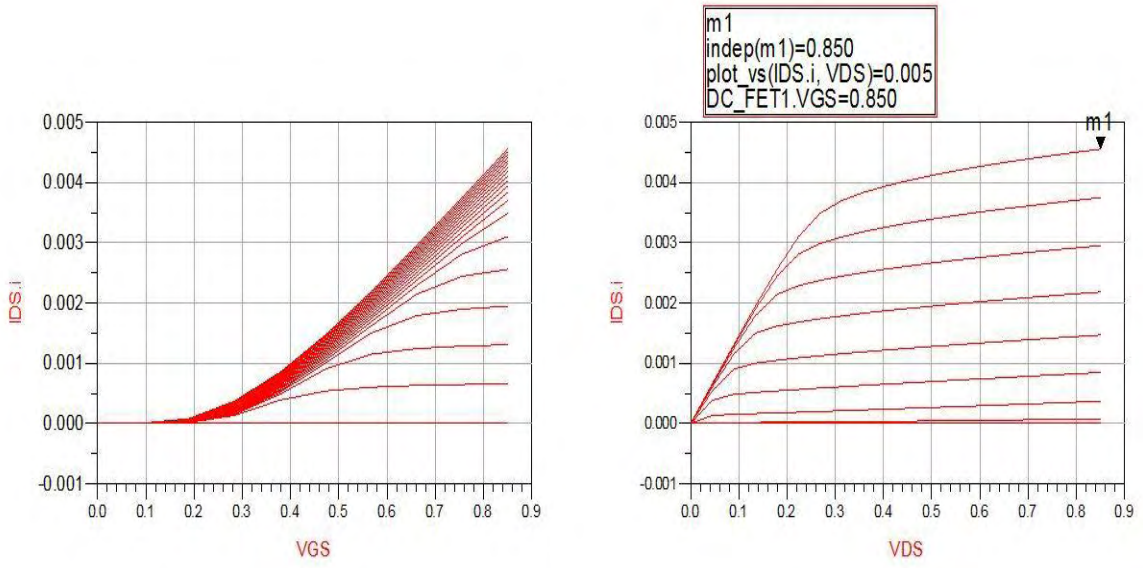


Figure 3.3 **Id-Vds** and **Id-Vgs** graphs for nMOS

3.2 Circuit Design

In this section, we will present the circuit schematic of the FinFET nMOS differential LC-VCO. The presented Figure implements an ideal current source and ideal inductors and varactors. We used this design as a reference for the simulations held afterwards, where replaced all the previous ideal components with equivalent non-ideal.

- **nMOS differential cross-coupled LC-tank VCO(with footer)**

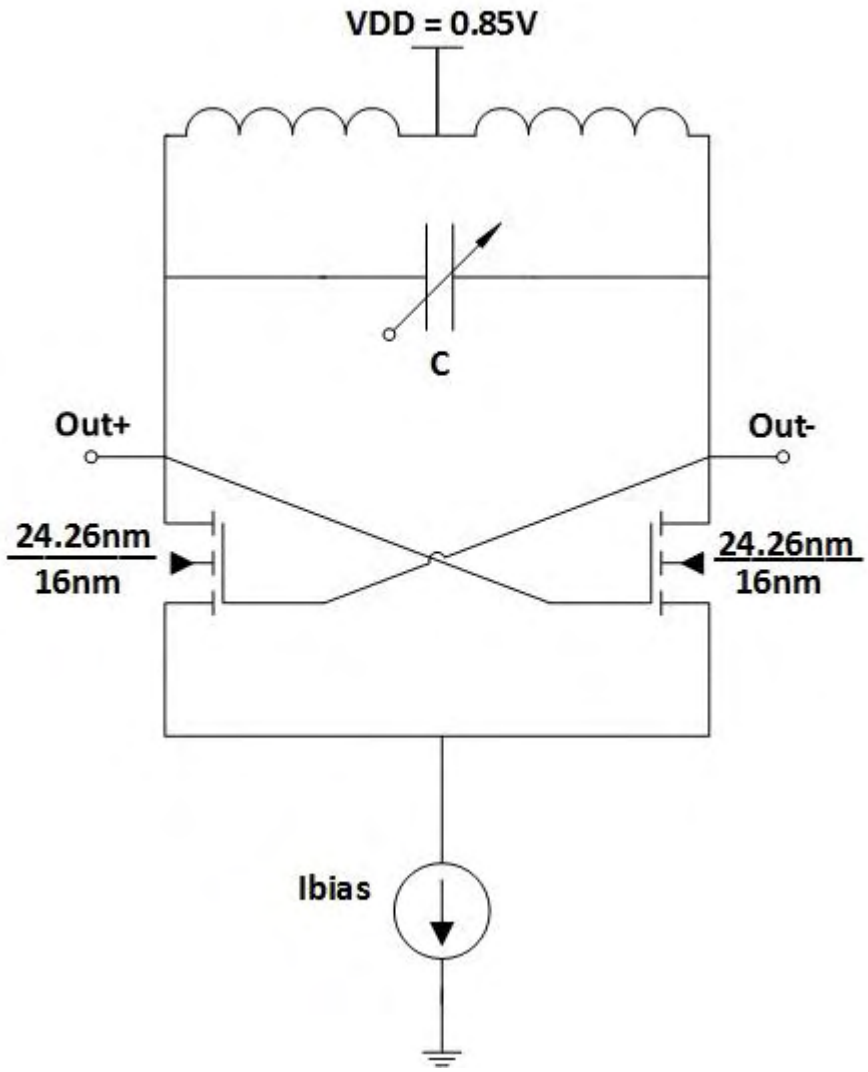


Figure 3.4 nMOS cross-coupled LC-tank VCO topology

- **ADS Circuit**

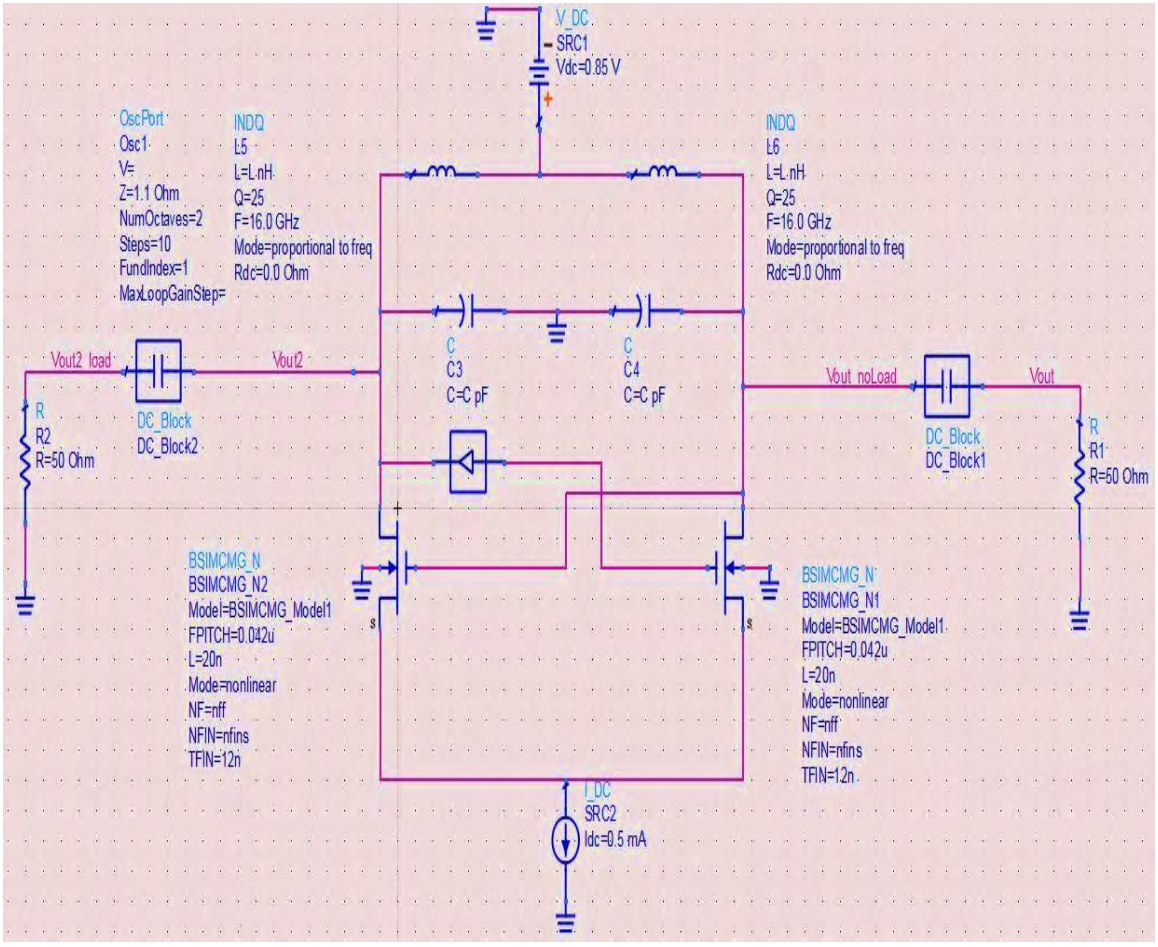


Figure 3.5 ADS implementation of nMOS cross-coupled LC-tank VCO

Note:

In this ADS implementation the circuit is biased by an ideal current source and all its passive components (inductors, capacitors) are ideal. In the next steps of our work, we will replace the ideal current source with a current mirror consisting of transistors at 16nm FinFET technology. Furthermore, the inductors and the varactor will be replaced with equivalent, non-ideal, at 16nm. More information about these components are outlined in the following sections.

3.3 Simulations for varying LC-tank configurations

As we have mentioned previously oscillators are electronic circuits that produce periodic signals, usually sinusoidal or square pulses, *the frequency of which is determined by the discrete values of the components constituting the oscillator*, without any other input.

The LC-tank, i.e. pair of inductance and capacitance, is the dominant factor in frequency determination. The direct independence of the oscillation frequency to the LC product is easily observed in the following norm.

$$\boldsymbol{f_{osc} = \frac{1}{2\pi * \sqrt{LC}}}$$

Therefore, we can have the exact same oscillation frequency with a great number of LC-value combinations. However, getting the same frequency does not necessarily mean that we have the exact same performance from the circuit indifferently.

In the following Figures, we present the simulation results of two transient simulations for different LC values to prove our point. The oscillation frequency remains set at 16GHz. It is also important to mention that the following simulations where performed using *only* ideal components, thus when performed with non-ideal components yielded slightly worse results.

In the end, we gathered some notes regarding the variations in the LC tank and the overall circuit performance deduced from the oscillations performed. Since, the LC combinations giving a 16GHz oscillation frequency is practically infinite, our assumptions are based on the results provided by the simulation vectors provided to the ADS software and the output results returned.

- nMOS Cross-coupled LC-tank VCO
  - **L = 0.23nH – C = 0.34pF – I_{bias} = 12mA**

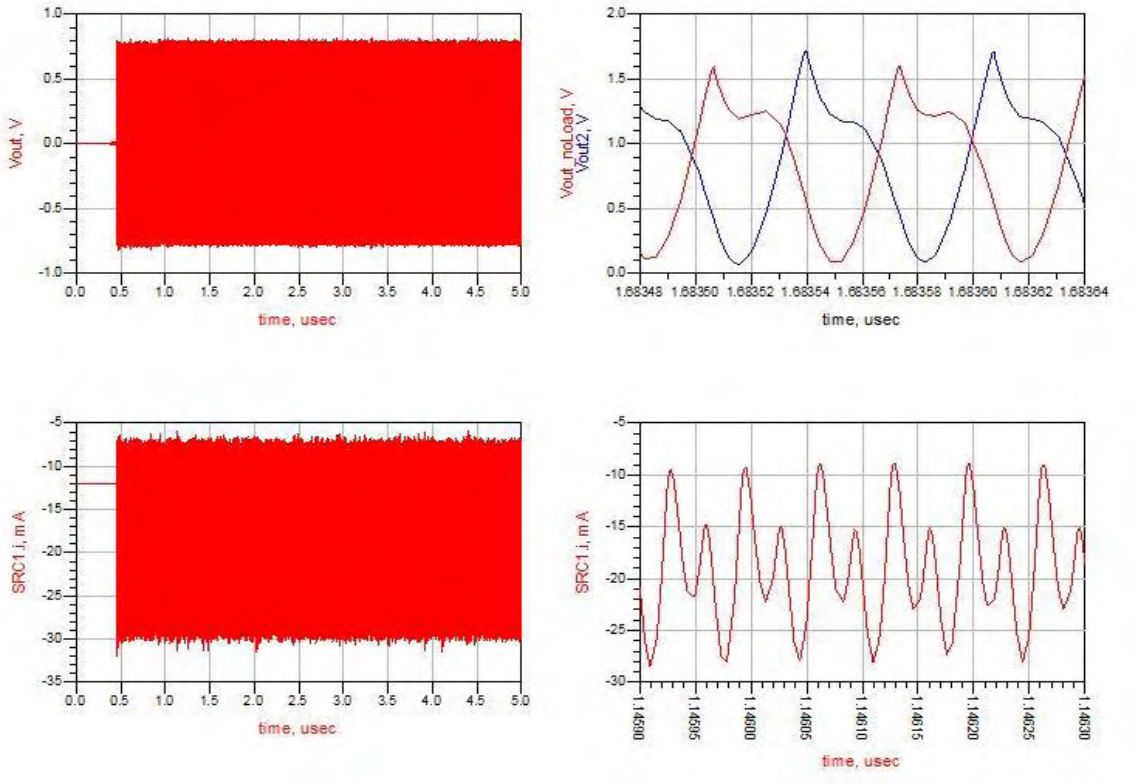


Figure 3.6 nMOS Simulation for L = 0.23nH – C = 0.34pF – I_{bias} = 12mA

- **L = 0.44nH – C = 0.11pF – I_{bias} = 12mA**

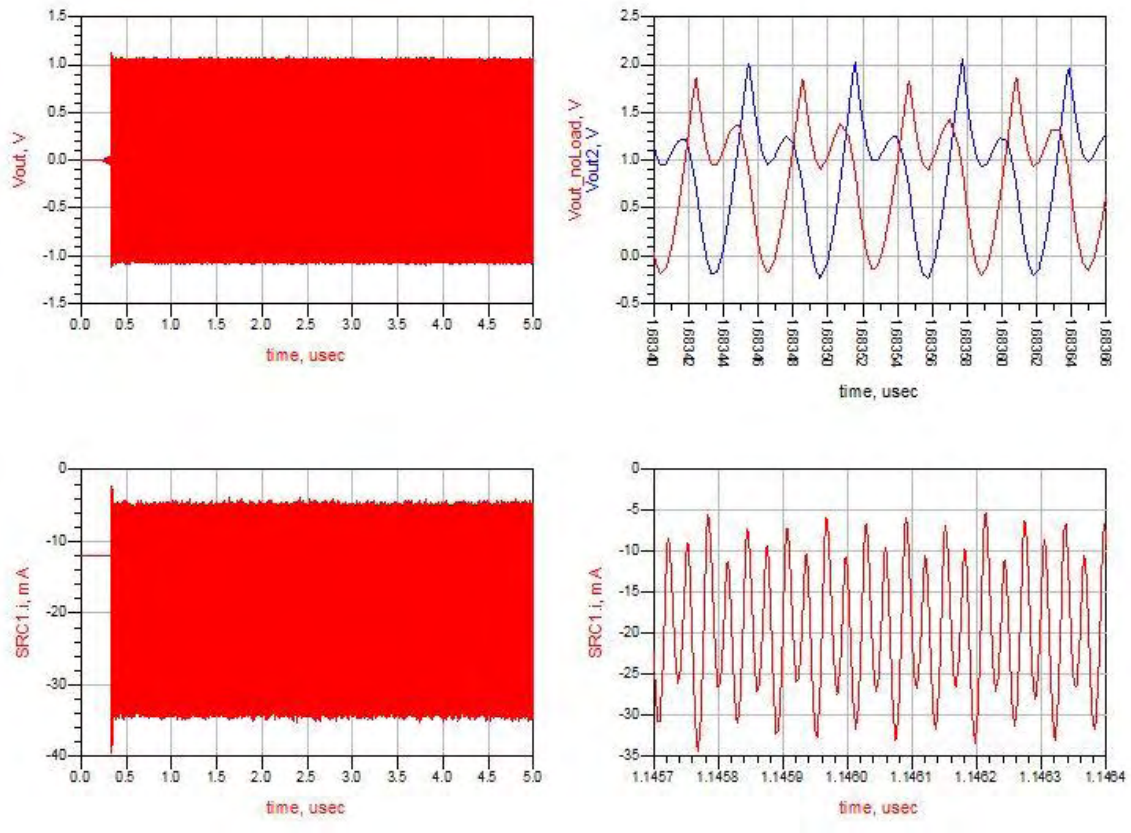


Figure 3.7 nMOS Simulation for L = 0.44nH – C = 0.11pF – I_{bias} = 12mA

Notes:

- For all the previous simulations the LC product produces an oscillation frequency of 16GHz, which is the most important specification for our circuit.
- Inspecting closely the results of our simulations, we observe that while we increase the inductance, reducing the capacitance at the same time to keep the product constant, our circuit stabilizes and starts oscillations faster. Furthermore, with the increase in inductance the output signal tends to become an ideal sine waveform.
- In addition increasing L, gives even greater output voltage (Vpp), which is one defining circuit specification.
- However, 12mA of current give great power consumption. For this reason in the following simulations we use much smaller bias currents to supply our circuit, sacrificing performance to meet the low power specifications needed.

In the following table, results from more transient simulations are presented to verify the observations we mentioned before as well as the norm used to calculate the oscillation frequency.

I_{bias}(mA)	Inductance(nH)	Capacitance(pF)	Freq(GHz)	V_{pp}^{out} (mV)
12	0.23	0.33	16.11	1493.8
12	0.23	0.34	15.92	1475.9
12	0.25	0.3	15.99	1537.3
12	0.44	0.11	16.22	2278.1

Table 3 Results for varying LC configurations

3.4 Quality Factor (Q) and non-linearities of inductors - capacitors

As we have mentioned in the introduction, at the time this thesis took place libraries for passive components, like inductors and capacitors, were not available at 16nm making the circuit design fairly difficult.

For a better design, knowing the quality factor of inductors and capacitors/varactors is critical. Since, we did not have these information at our disposal, we found ways round this problem without sacrificing the precision of our simulation results. But before we continue with the simulations it is important to give the definition of quality factor in order to have a better understanding of its role in circuit designs.

As quality factor (Q) we define the ratio of the energy stored in the oscillating resonator - in our case inductors and varactors - to the energy dissipated per cycle by damping processes. The losses appear as a result of the non-idealities the components used in the design exhibit.

$$Q = 2\pi * \frac{Energy\ stored}{Dissipated\ Energy\ per\ cycle} = 2\pi f * \frac{Energy\ stored}{Power\ Loss}$$

Ideally, both the inductors and the varactor should not dissipate any energy, and all the energy stored in them should be returned back to the circuit in every cycle. However, due to the resistance present at the materials consisting the varactor and the wire resistance of the inductor, equations to approximate these losses as well as the quality factor of each component are used.

$$Q_C = \frac{1}{\omega C R_C}$$

where ω is the frequency, C is the capacitance and R_C is the capacitor's series resistance.

As far as the inductor is concerned we have,

$$Q_L = \frac{\omega L}{R_L}$$

where ω is the frequency, L is the inductance and R_L is the inductor's series resistance.

Since capacitors always present smaller losses (higher Q) compared to inductors, the resonator's quality factor is dominated by the inductor, thus we neglect the varactor's Q. In order to have a precise overview of the inductor's behavior we should characterize it. In more detail, the exact inductance, series resistance and parasitics of the inductors in our setup should be calculated beforehand. Afterwards using all the previous information and the equations provided above the quality factor can be calculated. There are several way to measure the quality factor of an inductor, although usually models taking into account the geometric characteristics, such as the number of coils, the metal thickness and the inductor topology, are more accurate. Several topologies of on-chip inductors are presented below, all with the main goal of achieving minimum losses, higher Q and higher resonating frequencies.

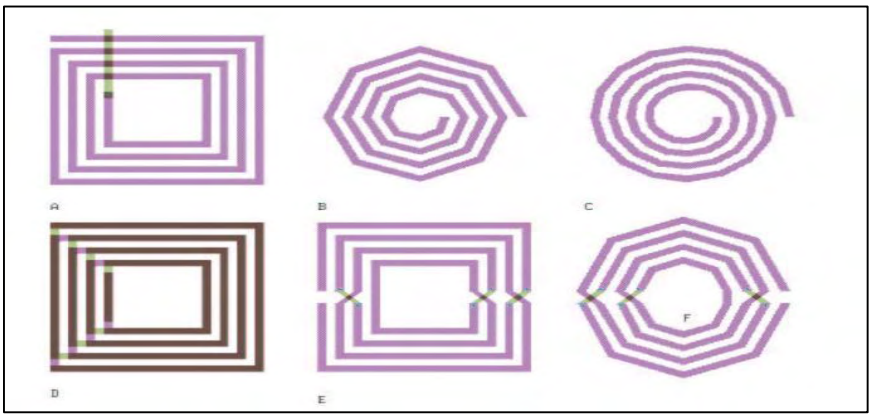


Figure 3.8 On-chip inductor topologies

Wheeler's formula can give as an approximation of the inductance based on inductor's layout

$$L = \frac{K_1 \mu_0 n^2 d_{avg}}{1 + K_2 FR}$$

where $K_1 = 2.34, K_2 = 2.75$ for square spirals (Figure 3.8 A) and $K_1 = 2.25, K_2 = 3.55$ octagonal spirals (Figure 3.8 B), $\mu_0 = 4\pi * 10^{-7}$ vacuum permittivity, n is the number of coils and

$$d_{avg} = \frac{d_{out} - d_{in}}{2}$$

$$FR = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}$$

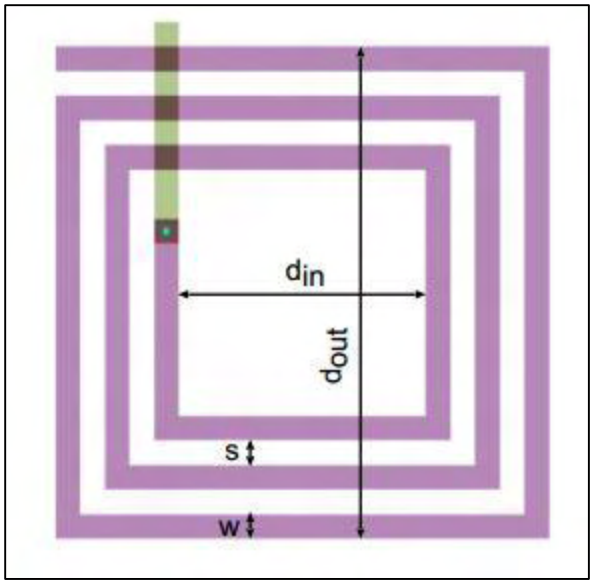


Figure 3.9 Dimensions of a square spiral inductor

In our case inductors have been synthesized using VeloceRF™ inductor synthesis EDA tool which provides rapid modeling and synthesis of integrated inductors and transformers, with signoff accuracy for electromagnetic effects such as mutual inductance, skin effect and substrate losses. Details about the inductor are shown below. It consists of 2.6um thick Redistribution Layer (RDL) stacked with 3.2um thick copper stacked with 1.05um thick copper. Q is 29.38, L is 0.43 nH, MaxQ frequency is 16 GHz, Self-Resonance Frequency (SRF) is higher than 48 GHz, area is 248 um x 248 um, track width is 10.38 um, and track distance is 2.01 um.

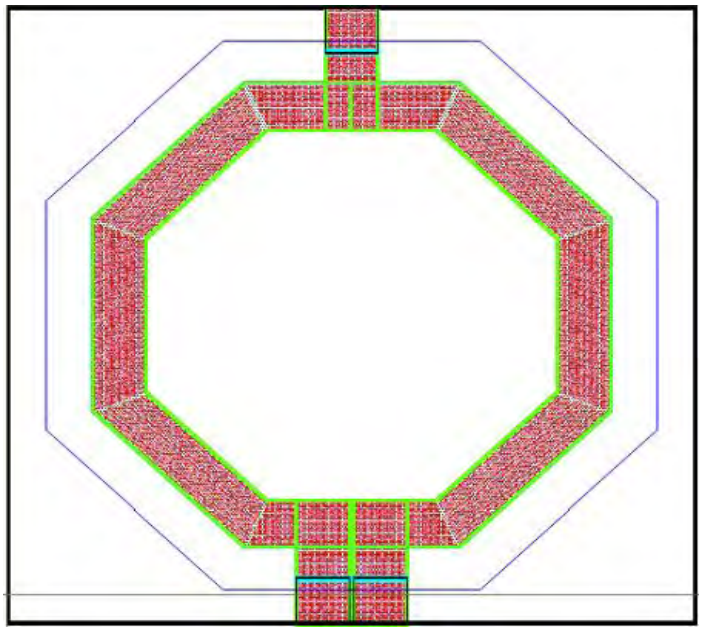


Figure 3.10 Inductor layout

In order to provide the desirable frequency fine-tuning in our design varactors are used. MOS-based Inversion type varactors were used due to their high *Q*-factor, wide tuning range, which improve with every new process generation, and implementation simplicity. A pMOS-varactor has the same structure as a pMOS transistor, with its gate as the first terminal and drain-source as the second, while the bulk is connected directly to V_{DD}. In Figure. 3.11, we present the exact connection and the capacitance over the tuning range characteristic follows in Figure. 3.12.

Furthermore, several stages of the previously mentioned structure in parallel can be utilized in order to provide the specific capacitance needed (i.e. 0.15pF) for our center oscillation frequency.

Further, the C-V characteristics of a pMOS varactor could not be easily modeled, although we know the oscillation frequency is computed using the following equation:

$$f_{osc} = \frac{1}{2\pi\sqrt{L \cdot C(V)}}$$

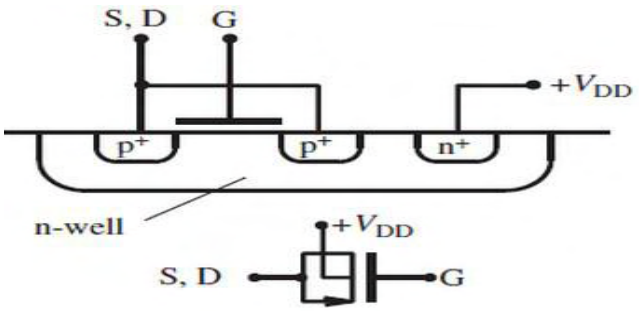


Fig. 3.11 MOS Inversion Type Varactor Cross-section & Connection

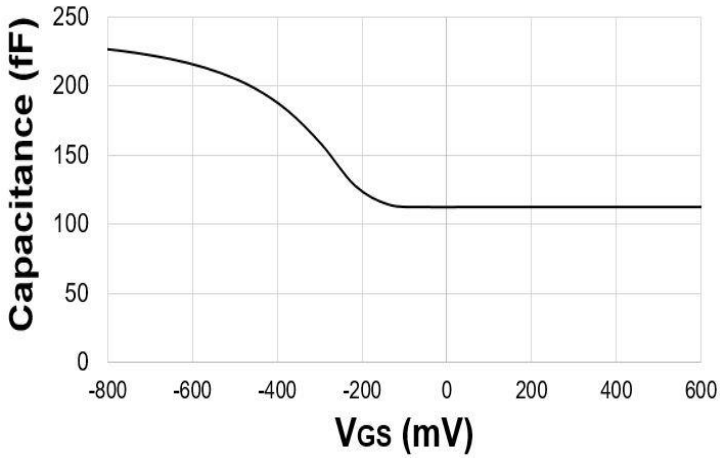


Fig. 3.12 Capacitance – V_{GS} Curve

where L is the inductance and $C(V)$ is the equivalent capacitance at a given biasing point.

Simply solving equation, we could get the norm to model $C(V)$ given a certain oscillation frequency and inductance as follows:

$$\boldsymbol{C(V) = \frac{1}{4\pi^2 \cdot f_{osc}^2 \cdot L}}$$

Apart from all the preceding, it is critical to take into account that capacitance is dependent not only on the signal swing of the output but also on the contribution of the center frequency harmonics.

3.5 Current source implementation

After the transient analysis simulations, which helped us verify that our circuit starts and preserves oscillations at the predefined frequency and also gives us a usable voltage output, it is time to start removing any idealities remain. Knowing the demanded current for our design to operate we will start by removing the ideal current source and replace it with a current mirror built from 16nm transistors

Of course, as we will discuss in detail in the next chapter, the replacement of the ideal current source with a current mirror will severely degrade the phase noise performance of our design, however techniques to reduce this effect will be implemented.

We will use a simple current mirror (current copier topology), due to its simplicity and small count of transistors needed to operate. Other more sophisticated current sources could be implemented but as the transistor count - consisting the non-ideal source - increases so does power consumption and the degradation of phase noise performance. In addition, varying the transistor width, number of fins and number of fins per finger we can ensure that the needed current in the copier stage will be provided to the circuit for correct operation. In the following Figure we can see the implemented current copier providing the circuit with the required power to ensure oscillation.

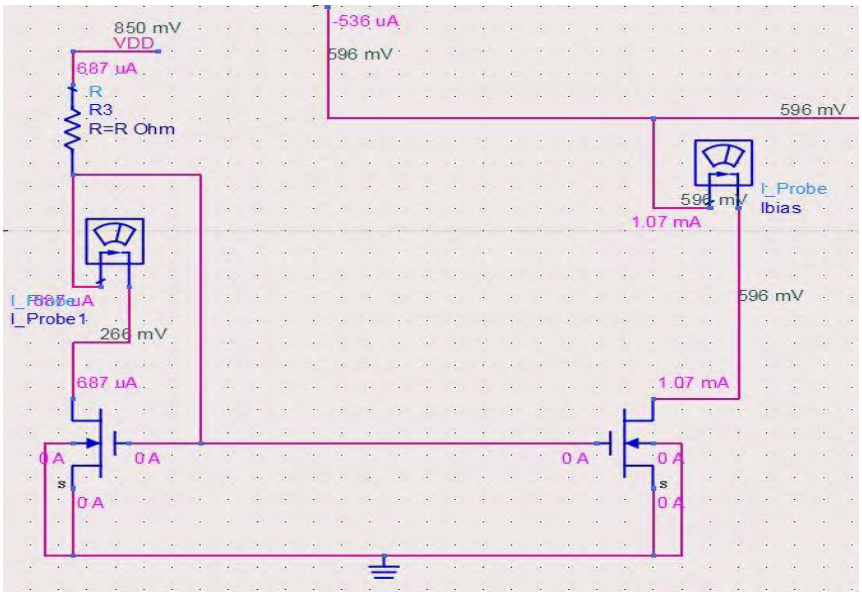


Figure 3.13 Simple current mirror with nMOS transistors at 16nm

Notes:

- Our initial circuit with the ideal current source could oscillate with less than 1mA of current supplied. However, when we implemented the current mirror we increased this current slightly in order to counterbalance the phase noise introduced by the non-idealities of the mirror.
- We also know that for planar transistors the output current is dependent on the reference current of the mirror with the following equation.

$$\boldsymbol{I_{out}} = \frac{\left(\frac{\boldsymbol{W_2}}{\boldsymbol{L_2}}\right)}{\left(\frac{\boldsymbol{W_1}}{\boldsymbol{L_1}}\right)} * \boldsymbol{I_{ref}}$$

where W_2, L_2 the channel width and length of the transistor providing I_{out} and W_1, L_1 the channel width and length of the transistor providing I_{ref}. In FinFET devices we can vary the output current, modifying the number of fins and number of fins per finger.

Chapter 4

Phase Noise Analysis

4.1 Introduction to Phase Noise (PN)

Phase noise or phase jitter is a key element in many RF and radio communications systems as it can significantly affect the performance of systems. While it is possible in an ideal world to look at perfect signals with no phase noise, that are a single frequency, this is not the case. Instead, all signals have some phase noise or phase jitter in them. In many cases this may not have a significant effect, but for others it is particularly important and needs to be considered.

For radio receivers, phase noise on the local oscillators within the system can affect specifications such as reciprocal mixing and the noise floor. For transmitters, it can affect the wideband noise levels that are transmitted. Additionally, it can affect the bit error rate on systems using phase modulation as the phase sitter may just cause individual bits of data represented by the phase at the time to be misread.

4.2 Frequency Stability (Harmonic Balance Simulation)

Phase noise is aggregated in an oscillator due to the non-linearities presented from both the passive (inductors, capacitors) and the active elements (transistors). The higher the quality factor of our LC-tank the less fluctuations in phase noise we can observe in our circuit. Phase noise affects not only the frequency but also the amplitude of the oscillations. However, the variations in amplitude are easily taken care for since the transistors are saturated, therefore we can neglect them. On the other side, the frequency instabilities presented are a major component of the overall phase noise performance and not only we cannot neglect them but finding ways to lessen their effects proves to be challenging.

High phase noise components introduce significant divergence in oscillation frequency which in time domain can be interpreted as a random shift –either forward or backwards in time- of the signal's waveform, where it crosses the time axis.

In Figure 4.1, is presented the frequency response of an ideal (a) and a real (b) oscillator, while in Figure 4.2 we can observe the effect phase noise introduces in a sine waveform both in the Time Domain(shift) and in the Frequency Domain where more unwanted frequency components are present.

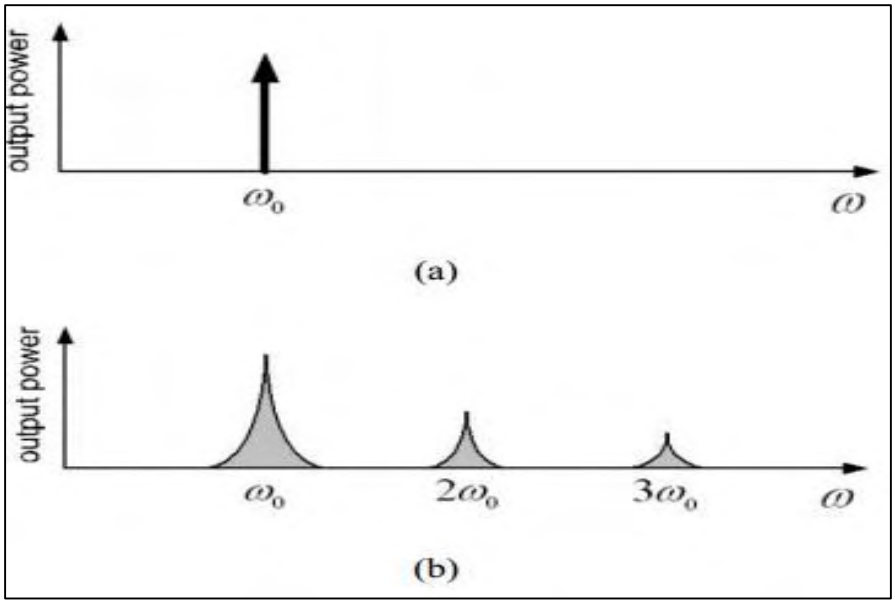


Figure 4.1 Frequency Response of an (a) Ideal and a (b) Real oscillator with Harmonic frequencies

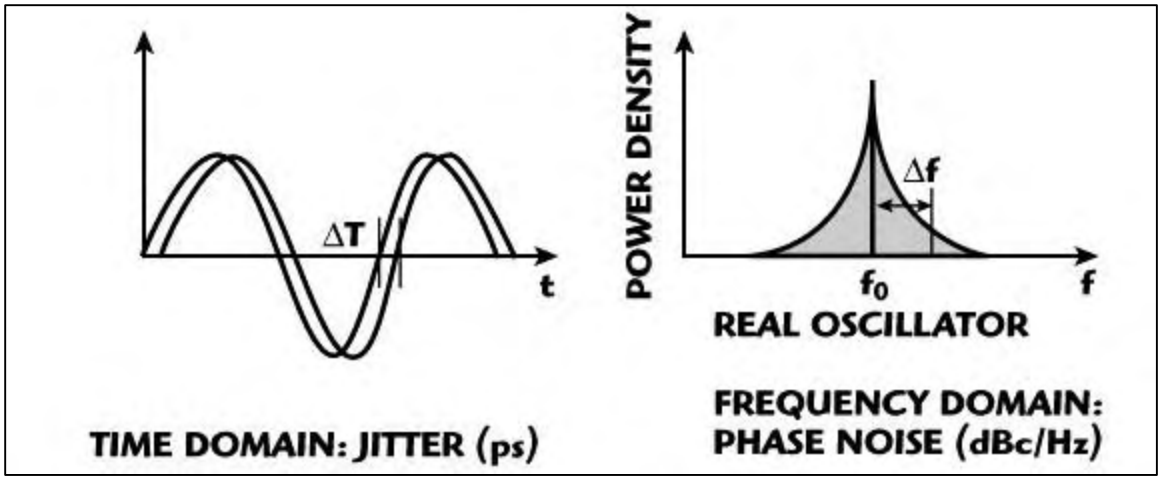


Figure 4.2 Time Domain and Frequency Domain representation of phase noise

As phase noise can become the most critical specification of an oscillator it is really important to study and measure the quality of our circuit topology with regard to this metric.

Phase noise computation is conducted in a predefined (bandwidth) Δω away from the center frequency. We calculate the power of the phase components in this frequency spectrum and divide it by the output power of our carrier signal. The measurement unit for phase noise is dBc/Hz, and since it is always negative, it reflects the attenuation of phase noise power (in logarithmic scale) as we move away from our center frequency of our carrier. An example of a phase noise specification is the GSM protocol, where -128dBc/Hz at 600KHz away from the carrier signal's center frequency is demanded.

$$L(\Delta\omega) = 10\,log\left[\frac{phase\ noise\ power\ in\ a\ 1Hz\ bandwidth\ at\ frequency\ \omega_0 + \Delta\omega}{carrier\ signal's\ power}\right]$$

where ω_0 is the VCO's center oscillation frequency

Additionally, in Figure 4.3 the attenuation of phase noise's power is depicted as we move further away from the center frequency, and more specific, Δω Hz away from f_{osc}.

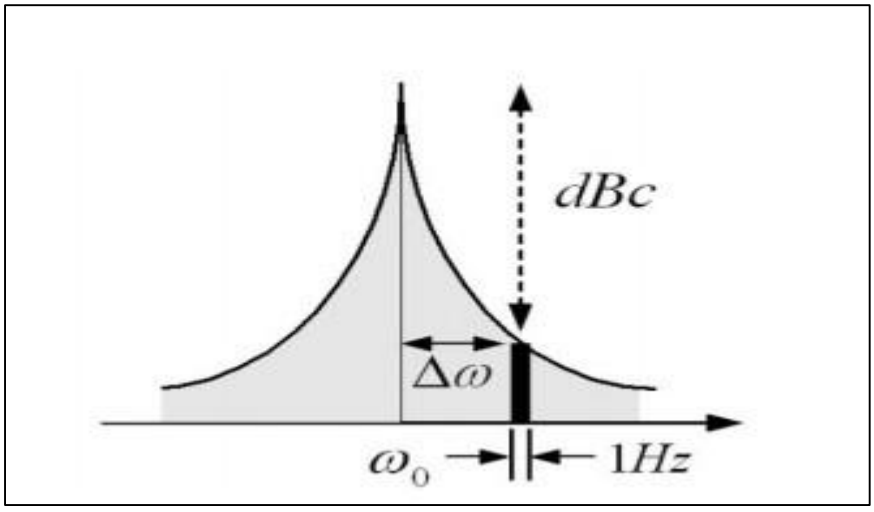


Figure 4.3 Phase noise at Δω Hz away from ω_0 in dBc/Hz

Having sufficiently discussed phase noise, its effects on oscillator performance and conducted transient analysis simulations to verify the proper functionality of our circuit, the only thing remaining is to run Harmonic Balance simulations to evaluate the circuit's frequency response and the purity of the oscillation frequency.

The Harmonic Balance simulation, provided by the ADS software, can present and evaluate the circuit's performance in the Frequency domain. However, a transient analysis have to precede the HB simulation, since we have to confirm the oscillation center frequency, in our case 16GHz, and afterwards conduct the HB simulation around at the correct bandwidth. Furthermore, HB simulation calculates the phase noise of our circuit and also the output power in dB, dBm of the oscillation frequency and its harmonics, constituting an irreplaceable tool in oscillator design.

In the following Figure, we can observe the output of the HB simulation and in the next table we have gathered results from several simulations where different LC configurations were tested. It is important to note that, in these previously mentioned simulations we used non-ideal inductor models provided by ADS with proportional to frequency response and a set Q at 20. We were really conservative at our selection since we already know that increasing the Quality factor of our inductors would yield much better results and nearly ideal circuit behavior (Dirac's Delta response).

- nMOS Cross-coupled LC-tank VCO

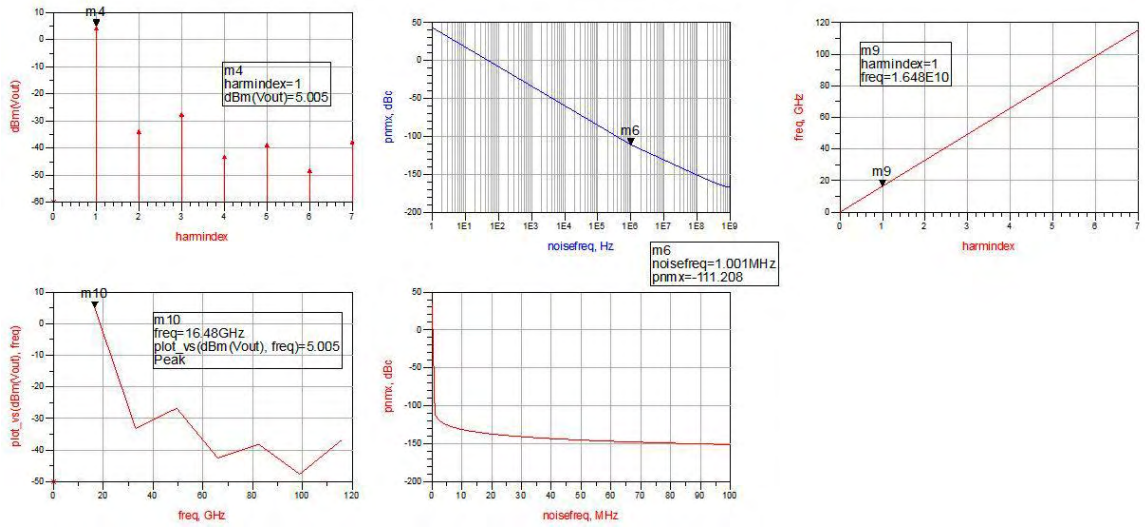


Figure 4.4 HB-Simulation for L = 0.43nH – C = 0.17pF – I_{bias} = 2mA

Inductance (nH)	**Capacitance (pF)**	**Freq (GHz)**	**I_{bias} (mA)**	**PN@1MHz (dBc/Hz)**	**V_{pp}^{out} (mV)**	**V_{out} (dBm)**	**V_{out} (dB)**
0.43	0.16	16.43	3	-110.807	1263.7	5.617	-4.383
0.43	0.17	16.06	3	-111.126	1247.2	5.6	-4.4
0.43	0.18	15.72	3	-111.426	1253.3	5.584	-4.416
0.43	0.17	16.32	1	-113.696	1118	5.201	-4.799
0.43	0.18	15.96	1	-114.086	1120.8	5.192	-4.808
0.43	0.17	16.63	0.5	-103.853	600.6	0.154	-9.846
0.43	0.18	16.25	0.5	-104.435	596.1	0.177	-9.823
0.44	0.19	15.89	0.5	-104.992	604.4	0.2	-9.8

Table 4 Harmonic Balance Simulation Results

4.3 Phase Noise Correlation with LC-tank characteristics and power dissipation

Low phase noise performance is the single most important specification for any device in telecommunications systems. In this direction, we always make sure that the elements constituting our designs, be it active or passive, should introduce as low as possible noise to our circuit.

We should not neglect the noise introduced to our design by the transistors implemented in our topology. However, this problem is easily addressed with better biasing circuits or by increasing their size respectively. An example could be the thermal noise introduced between the Gate and Drain of the transistors, we could deal with it by either increasing their size or decrease their bias current. Increasing the size of the transistors increases also the parasitics, while decreasing the bias current decreases the output voltage swing. This way we are faced with a trade-off where in order to optimize one specification another specification's performance is degraded. Not to mention that in some cases, the design specifications could limit the degrees of freedom we have in designing our circuit, by setting specific values for supplied power, transistor size, phase noise floor, output power, voltage swing, tuning range etc.

Further, by increasing the LC-tank's value we can obtain a much higher quality factor (Q), with all the mentioned advantages i.e. greater voltage swing, less phase noise, fastest initiation and more stable oscillations. Although, bearing in mind that integrated inductors and capacitors tend to occupy space on the wafer, when minimum area is a design constraint, there are few things a designer can do towards this direction.

Another design constrain that aroused with the advances in integration technology and all the new devices should exhibit – mobile phones, laptops etc. – is long standby time. In order to meet this specification, designing circuits consuming as low as possible power is imperative. However, as we mentioned previously, low power consumption, which in turn means lower biasing currents, results in poor phase noise performance. Again, we are dealing with a trade-off, this time between power consumption and phase noise.

4.4 Transistor sizing impact on Phase Noise

Phase noise is the measure of purity of a local oscillator and its most critical specification. Since it is calculated as the ratio of noise power to output signal power in a 1Hz bandwidth at a given offset from the carrier signal, providing a larger signal to our circuit would improve phase noise. The easiest way to achieve a greater signal is by providing the circuit with higher tail current.

In the context of this work, and since the voltage provided to our circuit is predefined at 0.85V the only way to increase the biasing current of our circuit is by varying some of the transistor values we have at our disposal. The two most important values defining the overall output current of the mirror are the number of fins and the fins per each finger of our FinFET transistors, also proper biasing is a prerequisite in order to secure the best performance at their operating point.

However, better phase noise due to increased tail current comes at the expense of higher power dissipation, which is not always feasible. Furthermore, if the cross-coupled transistors have reached their saturation limit, no matter how much current is provided to the circuit, its output will remain unaffected. These are the main reasons this technique should be implemented with caution, bearing in mind that increased tail current induces further noise to the circuit, due to the non-ideal current source, and greater power consumption. In Table 6, we have gathered some simulation results with regard to tail current and it is easily concluded that small increases in the current supplying our circuit can result to much better overall phase noise performance. Notably, the results regarding phase noise in Table 6 are worse as compared to Table 5, because the following results were extracted from a circuit design where a non-ideal current mirror was implemented.

I_{tail}(mA)	Freq(GHz)	PN@1MHz(dBc/Hz)
0.731	16.11	-99.871
0.960	15.99	-100.761
1.055	15.95	-101.126
1.530	16.08	-102.646
1.947	15.97	-104.22
2.849	16.15	-107.357

Table 5 Tail Current Contribution to Phase Noise

4.5 Phase Noise Enhancement (Biasing Filtering)

A current source with almost ideal, noiseless, behavior is not easily achieved and all the non-linearities that stem from this phenomenon are converted in phase noise. In an effort to reduce these contributions a large capacitor is connected in parallel with the current source and shunts the high-frequency noise to the ground. In addition, to provide high impedance and at the same time resonate the parasitic of the current source at the second harmonic ($2f_o$) a source inductor is implemented connecting the current source with the cross-coupled transistors. The simulation results provided in Table 7 show that for the exact same design and power consumption source filtering exhibits much better phase noise characteristics and should be therefore implemented wherever design constraints permit it.

Source Filtering	Freq (GHz)	I_{tail} (mA)	PN@1MHz (dBc/Hz)
Without	15.89	1.071	-103.398
With	15.93	1.071	-106.553
Without	16.2	1.071	-102.941
With	16.03	1.071	-105.007

Table 6 Current Source Filtering Contribution to Phase Noise

In the following Figure we can see the two most frequently used ways to filter a current source, with an inductor (inductively degenerated) or a resistance (resistively degenerated). In our case we used the inductively degenerated topology that yielded better result and dissipated less power compared to the resistive. Further, a large capacitor was connected in parallel to shunt high frequency noise. The overall topology, with the inductive degeneration and the capacitor is presented in Figure 4.6.

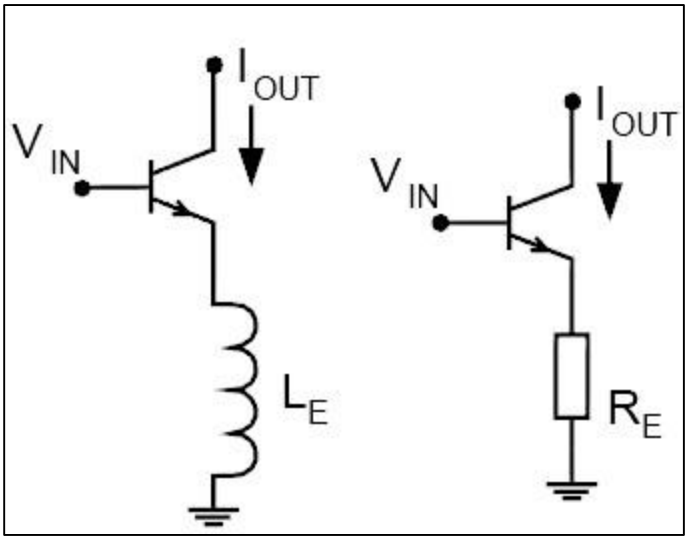


Figure 4.5 Inductive and Resistive degeneration of a current source

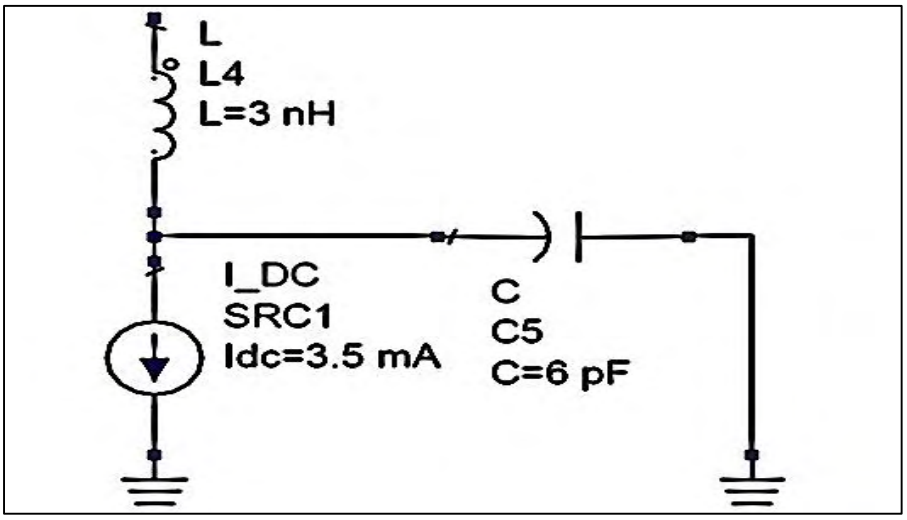


Figure 4.6 LC filtering to attenuate 2nd harmonic noise

In the following circuit schematic we can get a glimpse of the design and how it has changed compared to the one we had previously presented. Also LC-filtering is used in the current mirror and output buffers (Common Drain Stage) to effectively drive our loads.

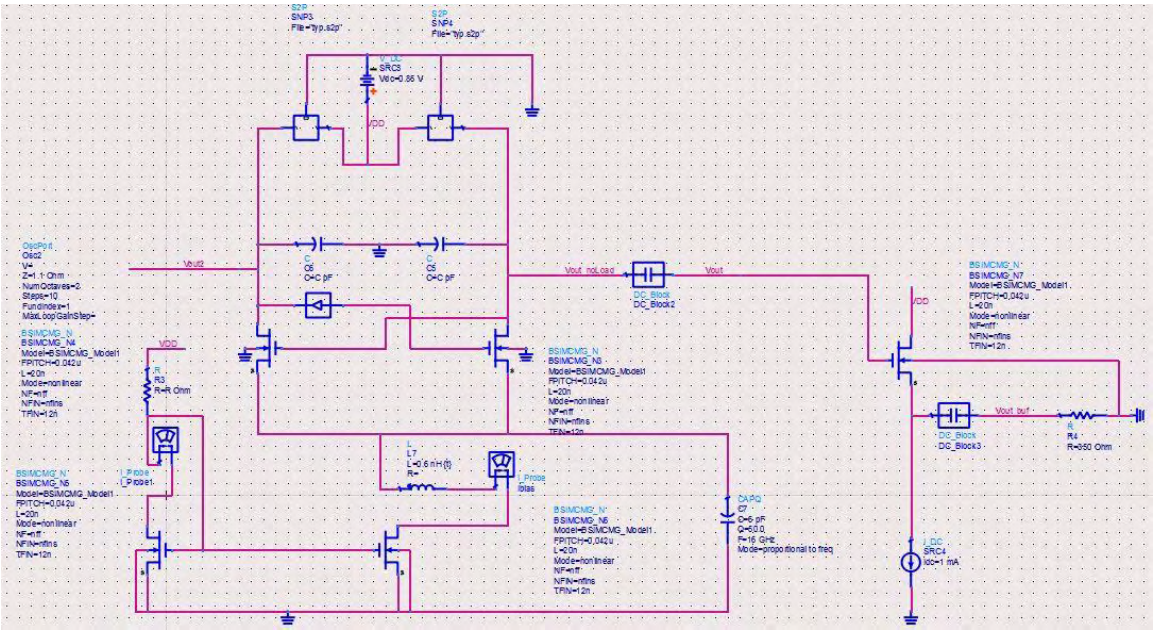


Figure 4.7 Circuit Schematic with LC-filtering

Chapter 5
Design Evaluation

5.1 VCO simulation results and performance evaluation

The improvement current source filtering provided to our circuit is not negligible and can be observed in Figure 5.1. Since the phase-noise performance at 1MHz offset from f_o is -106.553dBc/Hz for the source-filtered implementation while only -103.398dBc/Hz for the current source without inductive filtering.

Furthermore, the output frequency ranges from 14.31 to 17.06 GHz with control voltages varying from 0.2 to 0.8V. The center frequency of the implemented VCO, f_o, is 16GHz and the differential output is 3.259 dBm driving 350Ω loads at its output. It is also critical to observe the severe attenuation at the second harmonic due to $2f_o$ filtering, as presented in Figure 5.2, which also improved phase noise.

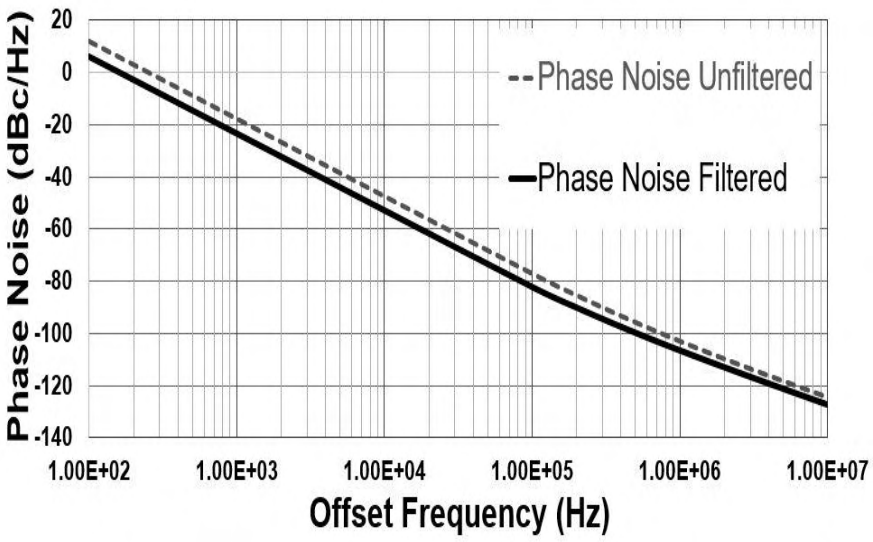


Figure 5.1 Phase Noise performance, with and without Source Filtering

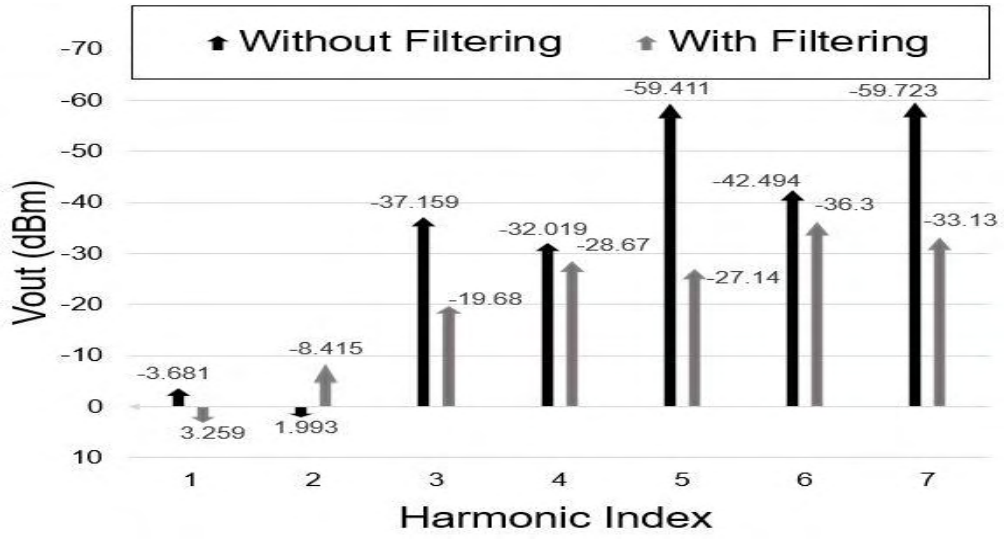


Figure 5.2 Harmonic Amplitude in dBm, with and without Source Filtering

In order to evaluate different VCO designs apart from their Phase Noise, power dissipation and output power characteristics, which can be misleading at different implementations, other metrics are also used. Figure of Merit (FoM), can determine the efficiency of an oscillator taking into account both the Phase Noise at a specific offset frequency and the power consumption. The calculated FoM value provides the necessary abstraction to compare circuit topologies that might even have different oscillation frequencies and other process variations. In Table 8, other similar designs are presented and their performance parameters are outlined for comparison. FOM is calculated by the following equation:

$$FOM = 10log_{10}\left(\left(\frac{f_o}{\Delta f}\right)^2 * \left(\frac{1}{P * 10^{\frac{L(\Delta f)}{10}}}\right)\right)$$

where f_o is the oscillation frequency, Δf is the offset frequency from the carrier (1MHz in our case), P is the power consumption in mW and $L(\Delta f)$ is the Phase Noise at the mentioned offset frequency

Ref	Process	Freq (GHz)	PN@1MHz (dBc/Hz)	Power (mW)	FoM (dB)
This Work	FinFET 16nm (PTM)	16	-106.553	0.91	191
[7]	FinFET 80nm	15.3	-94	7.5	169
[8]	32nm SOI CMOS	23.5	-96	13.5	172
[9]	28nm FDSOI CMOS	42.2	-98	6	183

Table 7 VCO Figure of Merit Performance

Due to the immense growth of wireless technology, oscillators with wide tuning range are demanded. However, the conventional FoM does not consider the frequency tuning range, which degrades the phase noise drastically.

In Table 9, a variation of the traditional FoM is used which takes into account the tuning range provided by the design for benchmarking purposes. The proposed work compares favorably against similar VCOs, exhibiting decent results for FoM and the tuning aware FoM formula mentioned below:

$$FOM_T = 10log_{10}\left(\left(\frac{f_o * tuning\%}{10\Delta f}\right)^2 * \left(\frac{1}{P * 10^{\frac{L(\Delta f)}{10}}}\right)\right)$$

where f_o is the oscillation frequency, *tuning%* is the tuning percentage (in our case 2.75GHz/16GHz = 17.2%), Δf is the offset frequency from the carrier (1MHz in our case), P is the power consumption in mW and $L(\Delta f)$ is the Phase Noise at the mentioned offset frequency

Ref	Process	Freq (GHz)	PN@1MHz (dBc/Hz)	Tuning Range (%)	FoM_T (dB)
This Work	FinFET 16nm (PTM)	16	-106.553	17.2	195.8
[7]	FinFET 80nm	15.3	-94	5	162.9
[8]	32nm SOI CMOS	23.5	-96	30	181.6
[9]	28nm FDSOI CMOS	42.2	-98	18.5	188

Table 8 VCO Tuning Range aware FOM Performance

Chapter 6
Conclusion

6.1 Future Work

In this work, a 16GHz differential LC VCO using an inversion-type varactor has been implemented in 16nm FinFET technology. The simulated tuning range of the oscillator is 17.2%. A number of phase noise reduction techniques have been evaluated. Good phase noise performance is achieved over the entire tuning range, reaching -106.553dBc/Hz at 1 MHz offset from f_o. The power consumption of the proposed core design is 0.91mW, since 1.071mA is drawn from a 0.85V supply under typical conditions. All the preceding, lead to a Phase Noise Figure of Merit (FoM) of 191dB, which when tuning range is also accounted for (FoM_T), reaches 195.8dB.

A VCO is a simple circuit block of the overall circuit found in a transmitter or a receiver. As we have already mentioned, it is responsible to provide a very stable oscillation at a predefined frequency which will be later used to modulate/demodulate an information signal. Thus, it could be implemented in a PLL (Phase Locked Loop) for better oscillation stability and even better phase noise performance. A simplified circuit diagram of a PLL is presented in the following Figure 6.1 where we can see how a VCO is embedded in the overall architecture.

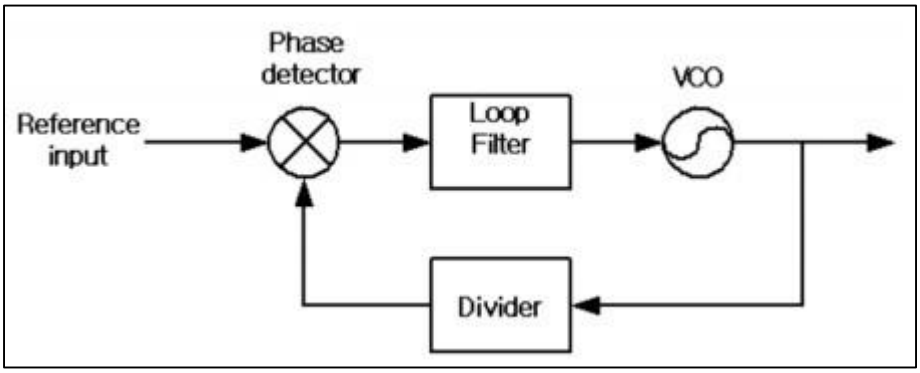
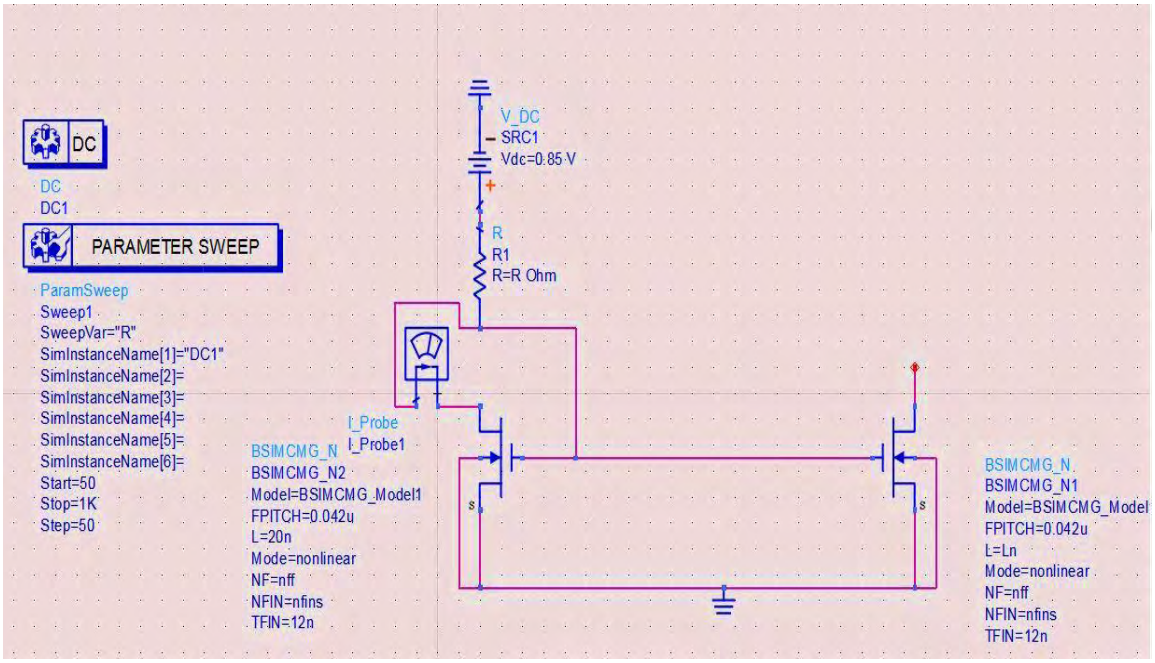


Figure 6.1 Simplified PLL Circuit

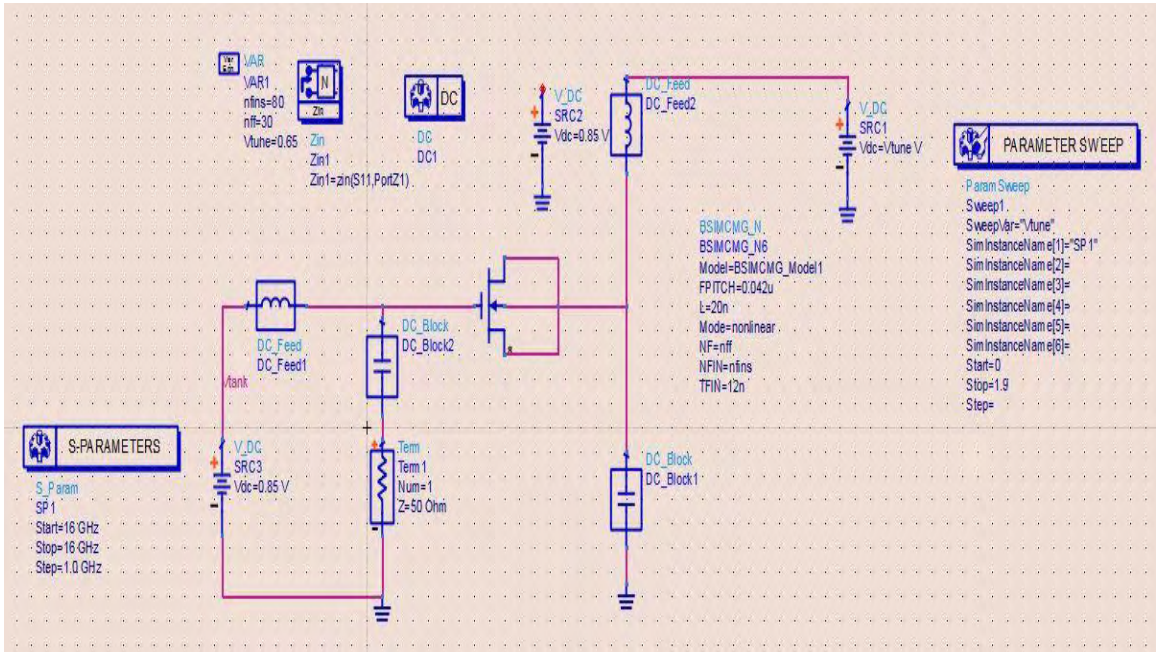
In a phase locked loop, the output of a voltage controlled oscillator is divided by a frequency divider circuit to a much lower frequency in which a crystal oscillator is operating. The main reason a frequency divider is used, is to transform the local oscillator's output frequency f_{LO} – usually in the MHz or GHz range – in a much lower one so that it can be compared to the frequency of the crystal oscillator used as referencef_{ref}. This division is performed most of the times with a particularly great number as crystal oscillators operate in really low frequency ranges (up to some MHz) due to their mechanical structure and the constrains it applies. Since recent telecommunications systems operate at frequencies of tens to hundreds of GHz, several stages of frequency dividers are used to lower the f_{LO} so it can be comparable to f_{ref} , as a result most of the power is consumed at these stages. In the next steps, the divided signal and the signal provided by the crystal oscillator are supplied as inputs to a phase detectors, in order to be compared and the difference in frequency is used afterwards to regulate the oscillation frequency of the VCO. When the frequency difference is lower than a certain threshold our PLL is locked, the time needed for our oscillation to stabilize and the PLL to lock is one of the most critical specification in PLL circuit design.

Appendix

- Current Mirror Simulation circuit



- Varactor Simulation circuit



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