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Transport Scaling Limits of Ovonic Devices: a Simulative Approach

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Abstract. The transport scaling limits of Ovonic devices are studied by means of a numerical solution of a time- and space-dependent transport model based on a set of equations that provide a good physical grasp of the microscopic process in hand. The predictivity of the approach has been confirmed through the comparison with recent experimental results where the parasitic effects have been reduced by the use of top-technology measuring equipments. The present analysis is performed for the AgInSbTe chalcogenide, since this material exhibits a steep threshold-switching dynamics which makes it promising for high-speed, non-volatile memory applications.

1. Introduction

The Ovonic threshold switch (OTS) is a characteristic electrical feature of many chalcogenide semiconductor materials. The process is very complex and still under analysis after about fifty years from its discovery [1]. Charge transport in Ovonic semiconductor materials is heavily influenced by the presence of trap states in the energy gap, which is confirmed by many structural analyses. This fact supports the applicability of a trap-limited transport scheme [2]–[7]. Recent experiments, performed with advanced testing equipments, focused on time-resolved electric response of nanometer chalcogenide layers [8], [9]. In fact, OTS has recently been exploited by the electronic industry as key physical mechanism of high-speed nano selectors for non-volatile memory (NVM) arrays [10]–[12]. Presently the scaling down of NVMs is reaching the 10-nm size [12], and the single memory selectors are scaled accordingly. Many experimental features can consistently be interpreted assuming that hot-carrier phenomena are dominant in the operating range of testing experiments and foreseen technological applications [7], [13].

Recently some Authors [14] suggested that scaling below 4 nm could induce structural changes in the electron states, thus spoiling the electric response of the device. In the present paper, we show that scaling below about 5 nm can prevent the setup of the microscopic non-equilibrium conditions that produce the electric switch. Our results were obtained using a numerical solution of a time- and space-dependent model described in [13] with the purpose of analysing transient transport regimes in Ovonic materials for the case of spatially non-homogenous electric fields. Here we focus our study on AgInSbTe (AIST) devices in view of the fact that AIST exhibits high-speed Ovonic switch when parasitic effects are engineered down to their minimum.

2. Theoretical framework and computational approach

The transport framework used in the present analysis is briefly summarized in this section; the details are provided in [13]. The model is of the hydrodynamic type and considers two levels for the carriers with energy difference Δ; the lowest level refers to trapped electrons, while the upper level refers to electrons in the band with mobility μ. Furthermore, a Maxwellian distribution of carriers at temperature T_e is assumed. Three equations are included for the particle continuity, local particle redistribution, and power balance, namely,

$$\frac{\partial n}{\partial t} = -\frac{\partial j}{\partial x}, \qquad \frac{\partial n_B}{\partial t} = \frac{\partial n}{\partial t} - \frac{n_B - \tilde{n}_B}{\tau_n}, \qquad n\frac{k_B T_e - k_B T_\circ}{\tau_T} = q\,j\,F + \Delta\,\frac{n_B - \tilde{n}_B}{\tau_n}, \quad (1)$$

where k_B is the Boltzmann constant, n_B and j the concentration and flux of carriers, $T_\circ$ the equilibrium temperature, n the total concentration (sum of band and trap concentrations), F the electric field, τ_n the recombination lifetime, and τ_T the temperature-relaxation time. Furthermore, $\tilde{n}_B$ is "tendential value" of the mobile-carrier concentration after a time variation of the electric field, and the following equality holds: $n/\tilde{n}_B = 1 + (g_T/g_B)\exp[\Delta'/(k_B T_e)]$, with g_T (g_B) the density of states of the traps (band), where the modified exponent $\Delta' = \Delta - \gamma\,|F|$ accounts for the fact that the excitation energy necessary to reach the band level is reduced by the field according to the Poole model. The model assumes that neither the lattice temperature nor the relaxation time τ_T vary within the operating time scale of the device [7]; finally, the electric field is obtained from the Poisson equation

$$\frac{\partial F}{\partial x} = \frac{q}{\epsilon}\,(n_\circ - n), \qquad (2)$$

with ϵ the material permittivity and $n_\circ$ the background charge.

The model's equations are solved numerically for the unknowns n, F, n_B, and T_e, assuming the following constraints at $t = 0$: $F = 0$, $n(x,0) = n_\circ$, and $T_e(x,0) = T_\circ$ anywhere in the device. Furthermore, $n(0,t) = n(L,t) = n_\circ$ (with L the device length) at any time t; this implies $\partial n(x,t)/\partial t = 0$ and, from the Poisson equation, $\partial F(x,t)/\partial x = 0$ at $x = 0$ and $x = L$. Finally, the integral condition $V(t) = -\int_0^L F(x,t)\,\mathrm{d}x$ is imposed on F by the applied bias $V(t)$. The sensitivity of the results obtained with the above-described approach on both the physical parameters of the Ovonic material at hand and the device length have been reported in [13] for a "reference" case. The sensitivity on the crystal temperature has been analysed in [7] for the homogeneous case.

3. Results

The set of the four equations in (1)–(2) has been solved focusing on the AIST chalcogenide. The model has initially been fitted to the experimental data of [9], where the dynamics of the threshold switching is investigated for a 80 nm-long device at the picosecond time scale, and the effect of the measuring circuit is reduced to the minimum allowed by the present electronic technology. The parameters used for the calculations are listed in table 1, and the results are reported in figure 1. The model well interprets the results up to the threshold voltage. Just above threshold AIST crystallizes [9] (see the upper kink in the $j(V)$ curve), and the model cannot be applied since no thermal effects are included at present.

The potential technological interest of AIST is related to the rapid OTS switching (sub 50 ps delay time for the device tested in [9]), and the effect of the device length on the transport features is quite a relevant issue for the exploitation of this material for nanoelectronic applications. The present theoretical framework allows for a space-dependent analysis of the transport process, and this has been carried out here for three devices of 20, 40 and 80 nm. Some results enlightening the role of carrier heating on the onset of OTS are reported in figures 2 and 3.

Table 1. Parameters used for fitting the AIST current vs. voltage characteristic.

| Symbol	Definition	Value	Units
Δ	Energy of mobile states from the trap level	0.315	eV
Γ	g_T/g_B	$1.4 \cdot 10^{-3}$	
γ	Coefficient of Poole effect	$5.0 \cdot 10^{-29}$	C m
ϵ	Relative permittivity	15	
μ	Mobility of mobile electrons	$6.0 \cdot 10^{-4}$	$m^2/(Vs)$
$n_\circ$	Equilibrium electron concentration	$1.45 \cdot 10^{27}$	m^{-3}
τ_T	Temperature relaxation time	$8.3 \cdot 10^{-13}$	s
τ_n	Recombination time	$1.0 \cdot 10^{-13}$	s
L	Device length	$80 \cdot 10^{-9}$	m
$T_\circ$	Room temperature	300	K
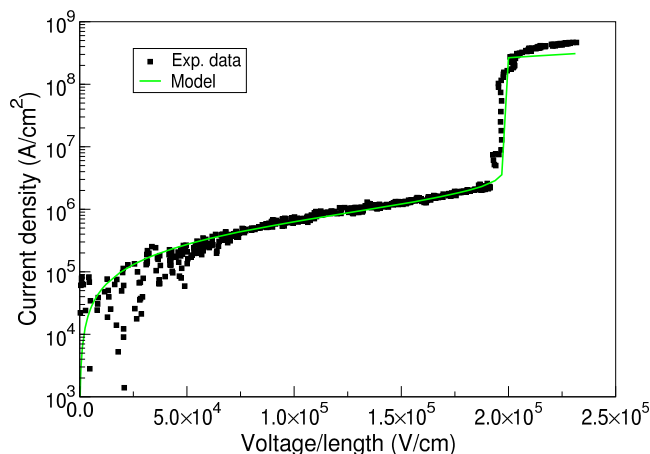
Figure 1. Experimental (black dots) and simulated (green line) current density vs. mean electric field for AIST. Experimental data are from [9].

Figure 2 confirms that the transport features of devices of different lengths depend only on the internal field and not on the applied voltage (see inset); in particular, the threshold voltage for the OTS in AIST devices is determined by a mean field of 2×10^5 V/cm. Finally, figure 3 shows the profiles of the internal field and relative concentration of mobile carriers at different voltages along the device for the $L = 20$ nm case. All the considered microscopic quantities show a significant variation within the first few nm from the injecting contact, then slowly reach constant values within 5 nm from the same contact. Below threshold the field is almost uniform in the device, while at and above threshold it reaches very high values just inside the device near the injecting contact. This process, fulfilling the energy balance included in the model, transfers enough energy to the electrons to sustain the necessary concentration of mobile carriers in the rest of the device. We can then conclude that the ultimate limitation to scaling, as far as the material properties are concerned, is the one related the the heating process. Scaling down to few nm is nowadays well outside the technological range. In order to go further down the nm scale, chalcogenides tailored to show more efficient heating effects must be explored.

4. Conclusions

The transient transport in OTS AIST-based devices has been analysed, assuming a trap-limited transport model, by means of a theoretical framework based on the solution of the three balance equations in (1), each encoding a basic physical principle, together with the Poisson equation (2). The limited computational burden of the model makes it possible to test a variety of conditions and, possibly, to incorporate it into more complex device-simulation tools.

A good comparison with available experiments is achieved for a 80 nm-long device. Moreover
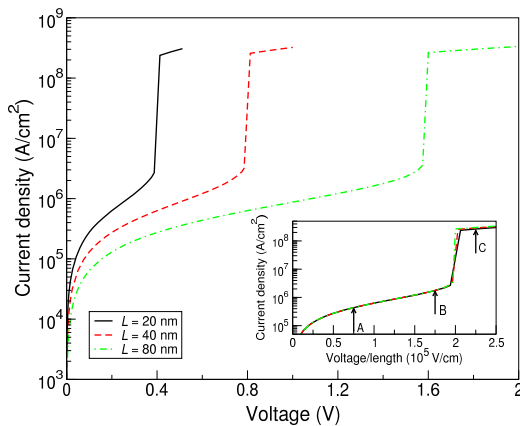
Figure 2. (top) $j(V)$ characteristic for AIST devices of different lengths. The inset shows the same result as a function of the mean field. A, B, and C show the cases considered in figure 3.

Figure 3. (right) Profiles of the electric field and fraction of electrons in the mobile states as functions of the position inside the device for a 20-nm layer of AIST at different values of the applied bias.
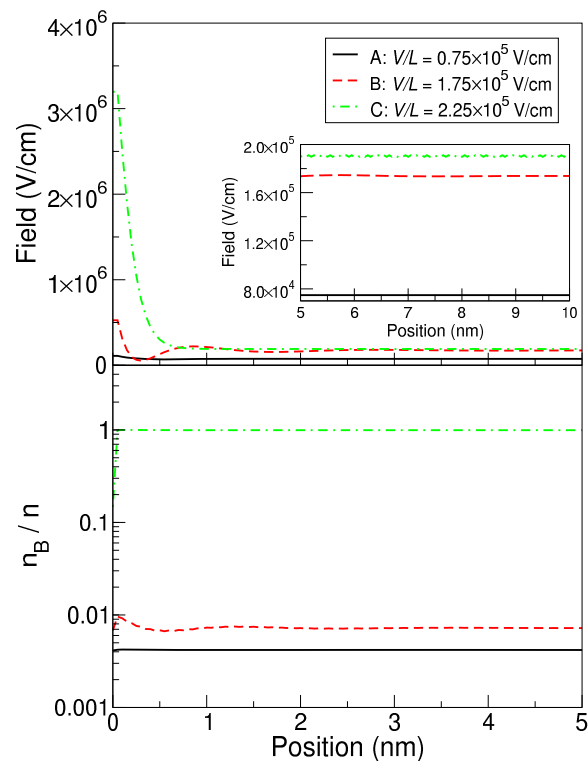
the analysis has been extended to shorter devices with the purpose of establishing the transport scaling limits of the OTS process in this material. As already obtained for other chalcogenides [13], the most significant spatial variability of the relevant quantities takes place within about few nm from the injecting contact. This suggests that the carrier heating process responsible for the OTS imposes a lower limit to the scaling down of OTS devices for nanoelectronic implementation.

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