UNIVERSITÀ DEGLI STUDI DI NAPOLI
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UNIVERSITÀ DEGLI STUDI DI NAPOLI FEDERICO II

PH.D. THESIS IN

INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING

ADVANCED TERMINATION STRUCTURES FOR HV POWER SEMICONDUCTOR DEVICES

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“Don’t ever let someone tell you
that you can’t do something.
You got a dream, you gotta protect it.
You want something, go get it”
(Chris Gardner)

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Chapter 1

Introduction

Power semiconductor devices constitute the main components of power electronic systems playing a key role in term of cost and efficiency. Due to the widespread use of electronics in consumer, industrial, medical, and transportation sectors, power devices have great impact on world economy. Nowadays the conversion systems are even more efficient, greatly reducing the amount of lost energy. Most attention is paid on power electronic devices that often are the main responsible of power dissipation.
As regards the power dissipation, it is a problem not only related to the energy lost during a conversion process, but for power devices it is also related to Joule effect that can produce a local destructive increasing of temperature. The latter becomes particularly important for devices working in harsh environment conditions, like often happens in automotive or railway fields. This leads to industrial manufacturer to require restricted standard of ruggedness and reliability of power components. Hence, a power device must guarantee its correct functioning well beyond the nominal specifics of a given application. Different tests have been introduced by industry to qualify their product like Unclamped Inductive Switching (UIS) test, Short-circuit test, etc. able to overstress the device in different operative conditions. The actual trend of power system in reducing the size as well as increasing the power capacity, leads to power device to operate at even higher power density. While the nominal current depends on the active area design, the voltage rate depends on the design of the periphery (termination) area. For a side there is the demand of increasing the voltage rate, but on the other side, this would require larger termination in contrast with the necessity of reduce the global dimension of the device. New terminations design are recently developed to guarantee the voltage rate with a lower consumption of area but they still need of reliability improvements.

In this scenario, the ruggedness and reliability analysis of a power device is mandatory. It can be lead in first instance by means of simulations before to proceed to the experimental validation using specific tests. This thesis mainly deal on the development of new termination design with particularly attention on analyzing the design parameters the mainly affect the reliability and ruggedness.

Thesis Contents

The thesis is divided in three chapters and one appendix.

First chapter briefly recalls of the Silicon power devices history. Particular attention is paid on two power devices which are analyzed in the rest of the work, namely P-i-N Diode and IGBT. The description of the working principles, as well as, the physical properties occurring inside the devices are provided. Static and dynamic electrical behavior are qualitatively recalled.
The Avalanche Breakdown physical mechanisms taking place within a P/N junction and a P/NP structure are treated. The necessity of adopting a dedicated design to solve the problems occurring in avalanche conditions at the periphery area of a Power device is discussed. The operative working of the main Termination designs are described. A brief recall on the technological fabrication process of a Power device Termination is provided.

Second chapter is about the analysis of the optimization, reliability and ruggedness of Termination design. In particular, two innovative JTE-based terminations are presented providing a well precise optimization methodology. Their performance are compared with that achieved with an advanced Floating Field Ring structure. Termination ruggedness has been evaluated by means of Unclamped Inductive Switching simulations. Therefore, current crowding phenomena occurring in avalanche condition are deeply analyzed together with its relation with the Negative Differential Resistance branch on the I-V avalanche curve.
The emulation process flow for a Floating Field Ring termination of a IGBT 600V rated active area has been provided.

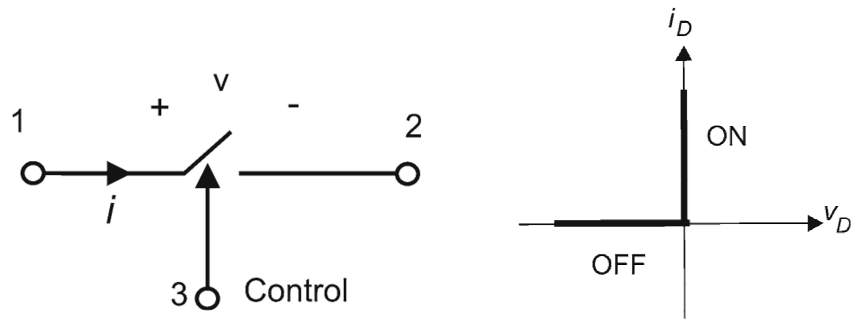
Third chapter is analyzed the influence of design parameters on the Short-Circuit capability of a FS-IGBT device. The device has been experimentally characterized by means of static curves tracker, Inductive Load Switching test and Short-Circuit test. A simulative approach has been used to evaluate innovative design solutions able to increase the Short-Circuit capability.

Appendix A is focused on the state-of-art of Reverse Conducting IGBT devices. Benefits and drawbacks of this modern technology have been discussed. Analytical and simulation approach have been provided to analyze the Snap-back phenomenon.

1.1 Fundamentals of silicon power devices

Modern power electronic began in 1957 when the first commercial thyristor, or Silicon Controlled Rectifier (SCR), was introduced by General Electric Company. Power rating and switching frequency increment led to develop other solutions, including Bipolar Junction Transistor (BJT). In 1978, Metal Oxide Semiconductor Field Effect (MOSFET) was introduced. Due to its high impedance and fast switching speed, it replaced BJT in low voltage (< 100V) and high frequencies (> 100kHz) switching applications. Insulated Gate Bipolar Transistor (IGBT) took place in 1983 by merging MOS and bipolar physics in unique block. It is used in applications from low to medium frequencies. From 1997, the Integrated Gate Commuted Thyristor (IGCT) is used in applications from medium to high power and from low to medium frequencies [1].
Energy conversion system in power electronic exploits electronic switches capable to handle high voltage (HV) and current operations at high frequency (HF) [1]-[3]. An ideal power electronic switch can be seen as a three terminals device (see Figure 1.1), where the input, the output, and a control terminal allow to impose the ON/OFF condition. The ideality condition expects that when the switch is open, it can handle an infinite voltage with a null current passage. On the other hand, when the switch is closed, it can carry in fine current and

the voltage on it is null. In an ideal switch the transient times ON-to-OFF or OFF-to-ON are nulls, for this reason, it exhibits zero-power dissipation. Additionally it allows a bidirectional current passage, and can support bidirectional voltage.



(a) (b)

Figure 1.1. (a) Ideal switch; (b) Idealized characteristic.

Actually, a real switch presents limitations in all of the fields explained in an ideal case. In On-state, a voltage drop occurs on it and it carries a finite current. Also in Off-state, it may carry a small current (leakage current) and a finite voltage can be supported. A finite transition time needs during the switching from ON-to-OFF and vice versa. For each switching devices it can define some characteristic times as the delay, rise, storage, and fall times.

As above mentioned, voltage and current are always present in a real switch during its operating, which will results in two types of losses. The first one defined as “conduction loss” occurs during the on and off-states; the second one called ‘‘switching loss’’ takes place during the transitions ON to OFF or OFF to ON of the device. During this phase high values of current and voltage can be contemporary acting on the device resulting in the overall increment of the switch temperature.

The classification of power switches passes through the concept of “ideal switch”, which allows evaluating the different topologies. Considering the characteristics of an ideal switch three class of power switch can be defined:

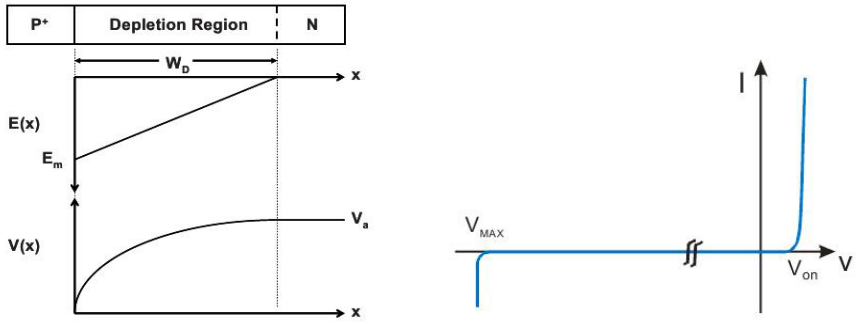
a) *Uncontrolled switch*, which has no controlling terminal. The external current or voltage determine the condition state of the switch, as in case of diode.

b) *Semi-controlled switch,* whose state is conditioned by an external circuit. For example, Thyristor or SCR have a terminal that determines the turn-on of the device but turn-off state needs of an auxiliary circuit.

c) *Fully controlled switch,* which can be turn-on and turn-off by terminal controlling. Close in the category there are BJT, MOSFET, GTO and IGBT.

1.2 Breakdown voltage

One of the main power devices requirements is the capability to withstand high voltages. The desire to control high power in motor system and power distribution system has encouraged in developing power devices with even higher BV. Avalanche multiplication phenomenon is responsible in semiconductor voltage limiting and depends on the electric field distribution inside the structure [4].
High electric field can generate either in active-area or in periphery-area depending on the structure design. This last have to be realized considering a right trade-off between an elevate BV and a low on-state drop in order to reduce the losses. The depletion region at the P/N junction, or Schottky barrier or at the Metal-Oxide-Semiconductor (MOS) interface, sustains the high voltage (Figure 1.2).



(a) (b)

Figure 1.2. (a) Electric field and electrostatic potential distributions in a P/N junction. (b) P/N junction I-V characteristic.

Avalanche breakdown is strictly related to generation-recombination processes. They represent a physical phenomenon of great importance, in particular for bipolar devices, and consist in the carriers exchange between conduction band and valence band. A continuous balancing between generation and recombination of electron-hole pairs occurs at the thermal equilibrium. The equilibrium can be broken by applying an external stimulation, which creates carriers excess. When the perturbation leaves off, the equilibrium condition starts to return with a recovery rate depending on minority carriers lifetime.

1.2.1 Impact ionization

Impact ionization effect is a generation mechanism that can occur in semiconductors in particular polarization conditions. Electrons and holes entering into the depletion region, due to the space charge generation or for diffusion from the adjacent quasi-neutral regions, are led outside under the effect of a high electric field depending on the applied voltage. With the increasing of this last the electric field grows too, by accelerating the mobile charges until to reach their saturation velocity ($1x10^7$ $cm \cdot s^{-1}$) in correspondence of which the electric field overcome the value of $1x10^5$ $V \cdot cm^{-1}$. In such case, the kinetic energy of the mobile charge is sufficiently higher than the semiconductor energy bandgap E_G. This permits in the interaction with crystal lattice atoms, to excite the electrons from the valence band to the conduction band, generating electron-hole couples (Figure 1.3).

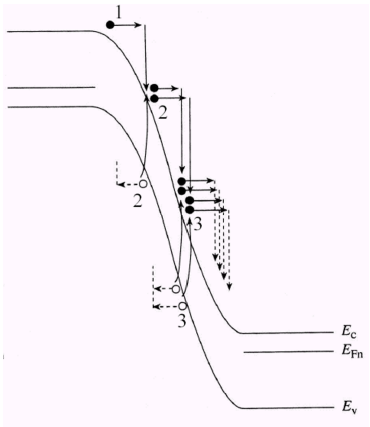


Figure 1.3. Impact ionization effect

Since electron-hole couple generation takes place inside the depletion region, it is subjected to the electric field acceleration, contributing in turn to generate further electron-hole couples. As consequence, the impact ionization is an avalanche multiplicative phenomenon able to significantly increase the amount of mobile charge, and hence, of current flow. As the matter of fact, the avalanche multiplication represent a limitation to the maximum voltage rate, since the fast current growing does not allow to the device to sustain too much elevated voltages.

In the avalanche breakdown phenomenon, it is possible to define an *impact ionization coefficient* for electrons and holes. It is defined as the amount of electron-hole couples generated by on electron and by one hole, respectively, in 1 cm through the depletion region along the electric field direction [5], [6]:

$$\alpha = ae^{-\frac{b}{E}} \tag{1.1}$$

The coefficient is strictly related to the electric field magnitude, as shown in Figure 1.4.

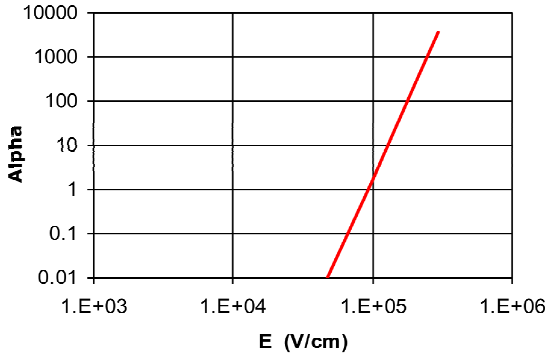


Figure 1.4. Impact ionization coefficient dependence on electric field in silicon.

Breakdown occurs when the impact ionization rate tends to infinite. It is considered the case of a mono-dimensional N^+/P junction, for which the depletion region mainly extends into the P region. If an electron-hole couple is created at a distance x from the junction, then the holes will be push to the P region contact while the electron toward the N^+ region. Considering the above mentioned relation (1.1), one hole will generate $\alpha_p \cdot dx$ couples at distance x from the depletion region, at the

same way, one electron will generate $\alpha_n \cdot dx$ couples. The total number of the created electron-hole couples at distance x from the junction is [7], [8]:

$$M(x) = 1 + \int_0^x \alpha_n M(x) dx + \int_x^W \alpha_p M(x) dx \tag{1.2}$$

where W is the depletion region thickness.

$$M(x) = \frac{\exp[\int_0^x (\alpha_n - \alpha_p) dx]}{1 - \int_0^W \alpha_p \cdot \exp[\int_0^x (\alpha_n - \alpha_p) dx] dx} \tag{1.3}$$

With the last equation, the *multiplication coefficient* is defined. Breakdown condition takes place when the total number of generated pairs tends to infinite, namely when M tends to infinite. Observing (formula *M*) this happens when the *ionization integral* is equal to unity:

$$\int_0^W \alpha_p \exp[\int_0^x (\alpha_n - \alpha_p) dx] dx = 1 \tag{1.4}$$

The avalanche effect produces a current that can be expressed as:

$$I = M \cdot I_0 \tag{1.5}$$

Considering now a P/N junction like in Figure 1.2, the ionization integral can be manipulated to be dependent on the electric field, by transforming dx into the dE variable. In such case:

$$\frac{dx}{dE} \int_0^{E_{CR}} \alpha(E) dE = 1 \tag{1.6}$$

The ratio dx/dE can be provided by Poisson equation for constant doping in drift region [9]:

$$\frac{d^2V}{d^2x} = -\frac{dE}{dex} = -\frac{Q(x)}{\varepsilon} = -\frac{qN_D}{\varepsilon} \tag{1.7}$$

The maximum electric field at the junction with which avalanche breakdown occurs is referred as *critical electric field* (E_{CR}). Its dependence on doping concentration of low-doped region is shown in Figure 1.5.

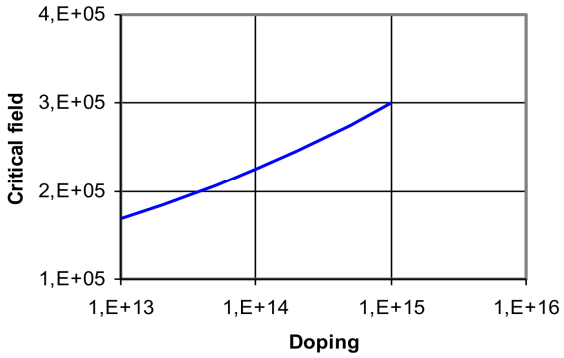


Figure 1.5. Critical electric field for avalanche breakdown in silicon p-n junction.

In more complex structures like IGBTs, which are made with more P/N junctions, the *open-base breakdown voltage* limits the maximum sustainable voltage by the device. Because of the bipolar transistor gain amplifies the current generated by the impact ionization [10]. More in details, the case of P/N/P transistor (Figure 1.6) is analyzed.

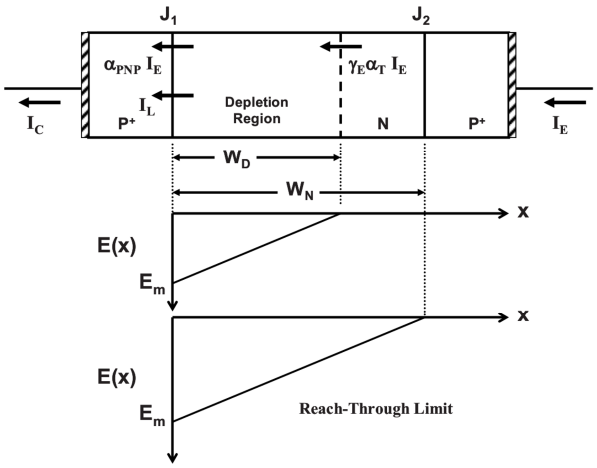


Figure 1.6.Open-base transistor analysis.

By applying a positive voltage to the emitter (right side), J_2 junction becomes directly polarized, while J_1 is in reverse polarization. The depletion region sustains the reverse polarization, which mainly develops into the low-doped N region. If the depletion region completely extends into the N region then the breakdown takes place when the electric field reaches its critical value. The holes injection from J_2 junction produces as effect the current flow amplification due to P/N/P gain, generating the open-base breakdown. The additional current contribution to due the generated carriers into the depletion region and in neutral region is indicated with I_{CB0}. Applying the Kirchhoff's low results:

$$I_C = \alpha_{PNP} \cdot I_E + I_{cB0} = I_E \tag{1.8}$$

or:

$$I_{CB0} = \alpha_{PNP} \cdot I_{CE0} + I_{cB0} \tag{1.9}$$

or:

$$I_{CB0} = M(\alpha_{PNP} \cdot I_{CE0} + I_{cB0}) \tag{1.10}$$

or:

$$I_{CB0} = \frac{M \cdot I_{CB0}}{1 - \alpha_{PNP} \cdot M} \tag{1.11}$$

Empirical equation of multiplication coefficient is [11]:

$$M = \frac{1}{1 - \left(\frac{BV_{CE0}}{BV_{CB}} \right)^6} \tag{1.12}$$

where BV_{CB0} is the BV of base-collector junction.
Equaling $M=1/\gamma\alpha_T$ results:

$$\frac{BV_{CE0}}{BV_{CB0}} = (1 - \gamma\alpha_T)^{\frac{1}{n}} \simeq (1 - \alpha_T)^{\frac{1}{n}} \tag{1.13}$$

if $\gamma=1$.
where it has been considered the relation:

$$\alpha_{PNP} = \gamma_E \cdot \alpha_T \tag{1.14}$$

γ_E is the emitter injection factor and α_T is the base transport factor.
For asymmetric devices [12]:

$$\gamma_E = \frac{D_{p,NB} L_{nE} N_{AE}}{D_{p,NB} L_{nE} N_{AE} + D_{nE} W_{nB} N_{DNB}}, \quad \alpha_T = \frac{1}{\cosh(W_{NB} / L_{p,NB})} \tag{1.15}$$

where $D_{p,nB}$ and D_{nE} are the minority carriers diffusion coefficients within buffer and collector region, respectively; N_{AE} and L_{nE} are the doping concentration and minority diffusion length into the collector region, respectively; N_{DNB}, W_{NB} and $L_{p,NB}$ are the holes doping concentration, width and diffusion length within buffer layer.

1.2.2 Leakage current

Inside the depletion region generation-recombination effects may occur, which add further current components to that of an ideal P/N junction. Even when the device is in off-state, it always exhibit a finite current, referred to as the *leakage current*. Such current contributes in power dissipation during the blocking state of a power device. The leakage current consists of two contributions, the first one due to the diffusion of free minority carriers; while the second one, is represented by carriers generated within the depletion region. In silicon devices, the diffusion current is negligible at room temperature, and only at high temperature, it becomes comparable to the generation current.
The current density generated within the space charge is given by [13]:

$$J_{SCG} = \frac{q W_D n_i}{\tau_{SC}} \sqrt{\frac{2 q \varepsilon_S V_C}{N_D}} \tag{1.16}$$

where n_i is the intrinsic carriers concentration and V_C is the voltage applied across the junction.
At the denominator of this expression appears the *space-charge generation lifetime* (τ_{sc}). Such term incorporates the generation mechanisms inside the space-charge. To reduce the space-charge generation current, a large value of τ_{sc} is desirable.

For IGBTs, the generation-recombination processes take place within both the base-emitter and base-collector junctions. In particular, the asymmetric IGBT works in forward blocking and space-charge current generation at the J_2 junction (see Figure 1.6) is amplified by the p-n-p transistor gain:

$$J_L = \frac{J_{SCG}}{1-\alpha_{PNP}} \tag{1.17}$$

1.2.3 Recombination processes

Carrier recombination is a fundamental process in any bipolar device since it influences both the static and the dynamic behavior. The recombination takes place when an electron within the conduction band passes into the valence band, when an electron in conduction band and a hole in valence band recombine them inside the semiconductor bandgap. Another possibility occurs when both, an electron in conduction band and a hole in valence band, drop in superficial trap (Figure 1.7).

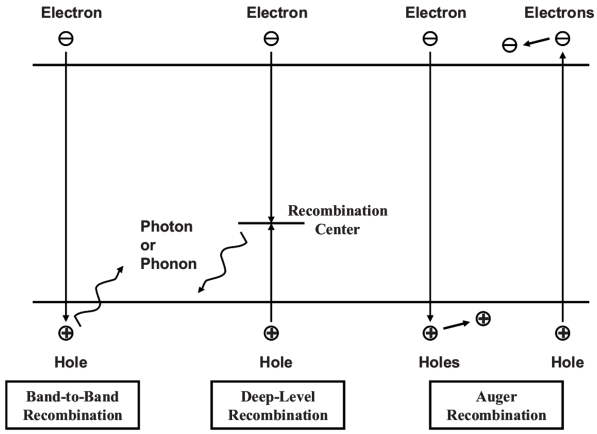


Figure 1.7. Semiconductor recombination.

In semiconductors, the possibility of direct transition (band to band) are highly unlikely, while the indirect transition mechanisms Shockley-Read-Hall (SRH) [14][15], whom exploit the charge passage through the middle recombination centers generated by lattice

impurities, are dominant. Auger recombination [16][17] become important in highly doped region or at high injection levels in drift region for bipolar devices. It consists in energy and momentum transferring to a third carrier and requires a triple collision.
The recombination rate U can be described by the following general expression:

$$U = \frac{pn - n_i^2}{\tau_{n0}\left(p + p_i \exp\left(\frac{E_i - E_T}{kT}\right)\right) + \tau_{p0}\left(n + n_i \exp\left(\frac{E_T - E_i}{kT}\right)\right)} \quad (1.18)$$

with the minority carriers lifetime $\tau_{n0,p0}$:

$$\tau_{n0,p0} = \frac{1}{\sigma_{n,p} v_{th} N_T} \quad (1.19)$$

Eq.(1.19) highlights the dependence of the lifetime on the thermal carrier velocity v_{th} and on cross section $\sigma_{n,p}$ and trap density N_T of electrons and holes.
The lifetime can be generally expressed as:

$$\tau = \frac{\Delta n}{U} \quad \left(or \frac{\Delta p}{U}\right) \quad (1.20)$$

where $\Delta p, \Delta n$ is an excess of injected carriers. In case of N-type silicon, the electron density n_0 is much larger than the hole density p_0. In such case: $p = p_0 + \Delta p, \quad n = N_D + \Delta n, \quad p_0 N_D = n_i^2, \quad p_0 << N_D$, substituting in eq.(1.18) the resulting expression is:

$$\tau = \frac{\tau_{n0}\left(p_0 + \Delta p + p_i \exp\left(\frac{E_i - E_T}{kT}\right)\right)}{N_D + \Delta n} + \frac{\tau_{p0}\left(N_D + \Delta n + n_i \exp\left(\frac{E_T - E_i}{kT}\right)\right)}{N_D + \Delta n} \quad (1.21)$$

At this point, it is possible dividing the discussion considering the two limit cases of *low* and *high* carriers injection. With low injection, the donor concentration is much higher than the excess of carriers

generated by external stimulations $\Delta p,\Delta n << N_D$ and the eq.(1.21) becomes:

$$\tau_L = \tau_{p0}\left(1+\frac{n_i}{N_D}\exp\left(\frac{E_T - E_i}{kT}\right)\right) \tag{1.22}$$

The low injection lifetime τ_L is only dependent on the recombination level position and minority carrier lifetime τ_{p0}.
At high injection, the donor concentration is much lower than the excess of carriers $\Delta p,\Delta n >> N_D$ and the high lifetime τ_H is given by:

$$\tau_H = \tau_{p0} + \tau_{n0} \tag{1.23}$$

Lifetime control techniques were developed in order to optimize the average carriers lifetime [18][19]. In order to generate middle energy levels, they are based on:

a) Impurity introduction by means of thermal diffusion of elements like gold or platinum, before of the active area realizing.

b) Electrons high energy irradiation.

The irradiation has the advantage of being realized after the active area since the accelerated ions are cabled to pass through both metal and oxide. Furthermore, recombination centers can be localized with the lifetime depending on the energy provided by ions. It points out that a higher lifetime is desirable from the static point of view to reduce the conductivity modulation resistance; on the other hand, a lower lifetime allows a faster charge redistribution during the transitory. Lifetime control techniques are used to balance these two aspects.

1.3 P-i-N diode

The P-i-N diode differs by the conventional P/N for the presence of intrinsic region (N-Drift) able to support the device reverse blocking (Figure 1.8). When the high-level injection of minority carriers occurs

into the drift region, the resistance of this thick layer is greatly reduce. Consequently, a low on-state voltage is achieved.

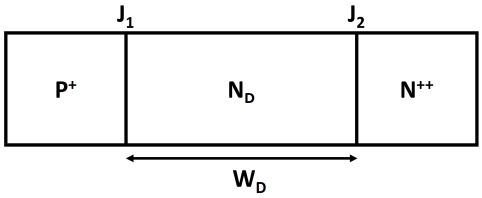


Figure 1.8. Basic geometry of a P-i-N diode.

The structure presents two junctions, J_1 and J_2. The P^+ Anode region and the N-Drift region form the first one, while the N-Drift layer and the N^+ Cathode region form the second one. Due to its low doping, the depletion region extends almost exclusively into the drift region until reaching the N^+ region. For this reason, its thickness must be designed to sustain the reverse breakdown voltage. The on-state voltage drop across the structure strongly depends upon the voltage drop across this drift region in addition to the voltage drop across the P/N junction. The holes injected by the P^+ region are minority carriers into the drift layer. However, if the doping N_D of this region is quite low, with the increasing of the current density, the injected holes density can reach a higher value respect to the one of electrons, which at ambient temperature is properly equal to N_D as depicted in Figure 1.9.

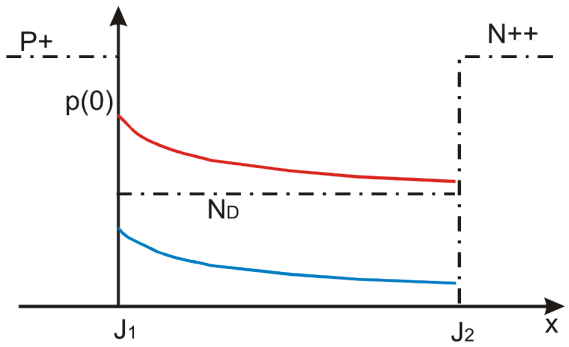


Figure 1.9. N-Drift holes distribution in low injection regime (blue line) and high injection regime (red line).

Considering the situation just described, it is possible to distinguish three transport mechanism that govern the current flow during the on-state condition:

a) Low current levels, where the *diffusion* of minority current dominates the transport within the drift region.
b) High current levels, where the high concentration of both carriers types dominates the transport within the drift region, referred also as *high injection current*.
c) At very low current levels, the recombination within the space charge determines the current transport.

At low injection regime, the profile of minority carriers into the neutral region is illustrated by the blue line in Figure 1.9. Applying the low of the junction, the holes concentration at the boundary of the depletion region is given by:

$$P_N(0) = P_{0N} e^{qV_a/kT} \tag{1.24}$$

where V_a is the voltage applied across the diode, P_{0N} represents the hole concentration at the equilibrium on the N side of the junction. The excess of minority carrier density at the depletion region boundary is described by:

$$\Delta P_N = P_N(0) - P_{0N} = P_{0N}(e^{qV_a/kt} - 1) \tag{1.25}$$

The total current flow at the depletion region boundary due to the diffusion current is given by:

$$J_{TN} = J_P(0) = qD_P \Delta p_N = \frac{qD_P p_{0N}}{L_P}(e^{qV_a/kT} - 1) \tag{1.26}$$

where D_P and L_P are the diffusion coefficient and the diffusion length for holes, respectively.
Assuming that for low minority injection:

$$P_{0N} = \frac{n_i^2}{N_D} >> n_{0P} = \frac{n_i^2}{N_A} \tag{1.27}$$

Considering that, the current J_{TP} given by the injection into the P side of the junction is negligible, the total current flowing through the P-N junction is described by the eq.(1.26).
At high injection regime, with the increasing of the voltage applied across the diode, the injected minority concentration rises in accordance to (1.24) until the profile of both electrons and holes becomes equal into the neutral region as illustrated by the red line in

Figure 1.9. In such condition, the minority carriers exceed the drift doping concentration N_D:

$$p_n = n_n >> n_{n0} = N_D \tag{1.28}$$

Considering the boundary low of the space-charge region:

$$pn = \frac{n_i^2}{n_n} e^{\frac{qV_a}{kT}} \tag{1.29}$$

Substituting eq.(1.28) into eq.(1.29) the new boundary condition for n side is achieved:

$$p_n(x_n) = n_i e^{\frac{qV_a}{2kT}} \tag{1.30}$$

The formula of $n_p(x_p)$ in the p side is the same because of they does not depend on doping level.
The electron current in the Drift region is zero at N^- side of the junction:

$$J_n = q\mu_n n_n E + qD_n \frac{dn_n}{dx} \cong 0 \tag{1.31}$$

Drift-diffusion equilibrium for electron is reached if:

$$q\mu_n n_n E = -qD_n \frac{dn_n}{dx} \tag{1.32}$$

The hole current is given by:

$$J_p = q\mu_p n_p E - qD_p \frac{dn_p}{dx} = -qD_p \left(1 + \frac{p_n}{n_n}\right) \frac{dp_n}{dx} \tag{1.33}$$

Since in the Drift region $n_n \approx p_n$:

$$J_p = -2qD_p \frac{dp_n}{dx} \tag{1.34}$$

$$p_n(x) = p_{n0} + n_i e^{\frac{qV_a}{2kT}} e^{-\frac{x-x_n}{L_p}} \tag{1.35}$$

with a constant length diffusion $L_p = \sqrt{2D_p \tau_p}$.

The current flow at high injection is given by:

$$J = \frac{2qD_p}{L_p} p_n(\mathrm{x_n}) = \frac{\sqrt{2}qD_p}{L_p} n_i e^{\frac{qV_a}{2kT}} \tag{1.36}$$

At high injection, the presence of a high concentration of free carriers strongly reduce the resistivity of the Drift region. Such phenomenon takes the name of *conductivity modulation*. It has a beneficial effect since it reduces the on-state voltage drop across the Drift region.
Since the diffusion gradient is negligible, the total current in the drift region can be written as:

$$J = q(\mu_n n + \mu_p p)E = q(\mu_n + \mu_p)n_a E = q\mu_a n_a E \tag{1.37}$$

where μ_a and n_a are the ambipolar mobility and concentration, respectively. In presence of ambipolar transport the time dependent diffusion equation is given by:

$$D_a \frac{\partial^2(\delta n)}{\partial x^2} + \mu_a E \frac{\partial(\delta n)}{\partial x} + G - R = \frac{\partial(\delta n)}{\partial t} \tag{1.38}$$

where *D'* is the ambipolar diffusion:

$$D_a = \frac{\mu_n n D_p + \mu_p p D_n}{\mu_n n + \mu_p p} \tag{1.39}$$

and

$$\mu_a = \frac{\mu_n \mu_p (p - n)}{\mu_n n + \mu_p p} \tag{1.40}$$

It is now considered the case of a very small current flowing across the P-N junction. The current transport is dominated by a recombination phenomenon governed by the SRH theory in accordance to eq.(1.18). As written in §1.2.2 the recombination current can be described in accordance to the eq.(1.16).
The forward conduction characteristic that indicates the relation between the current density and the voltage drop is dependent on the injection level of the carriers as in Figure 1.10. At very low current it is related to the space-charge generation phenomenon. At low injection the current flow is proportional to (qV_a/KT), while, with a

further increase of current density, it becomes proportional to $(qV_a/2KT)$. Finally, a larger current density in the drift layer generates a rapid increase of the voltage drop due to the recombination that reduces the injected carrier density.

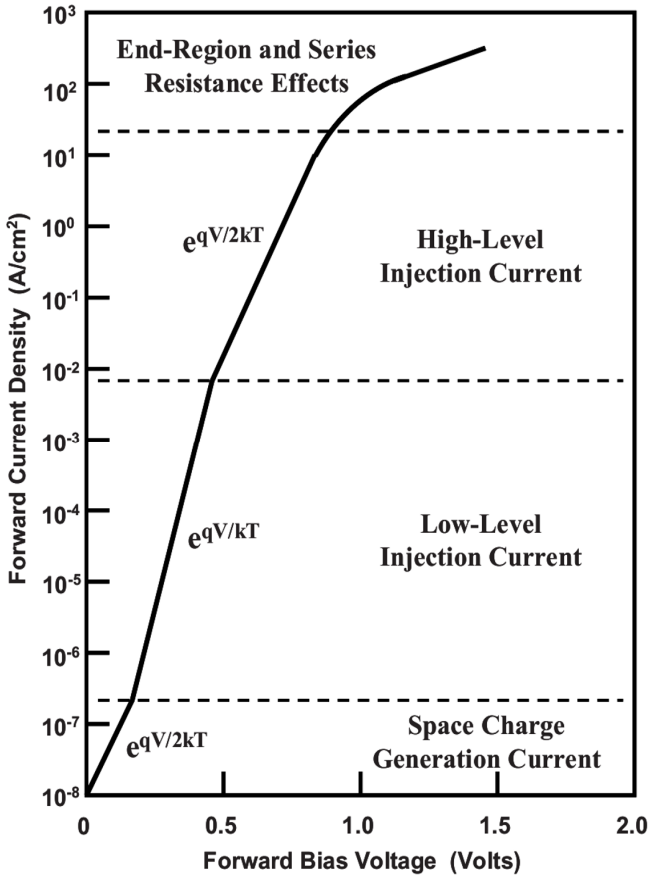


Figure 1.10. On-state forward characteristic for a P-i-N diode.

- **Transient characteristic**

The simplest power switching circuit of Figure 1.11 is adopted to describe the switching behavior of the device.

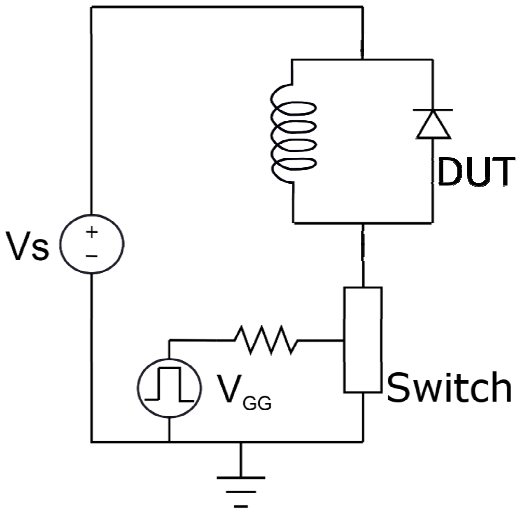


Figure 1.11. Simplest P-i-N diode switching circuit.

If the diode is operating as free-wheeling diode on inductive load, the turn-on phase takes place when forced by an external current source. The holes injected within the drift region do not reach in short time the high injection regime, and hence the conductivity modulation. This produces as effect an initial raising of the voltage across the junction (Figure 1.12). During the time, the injection of holes produces a decreasing of the voltage drop until to stabilize at the Von value due to the conductivity modulation.

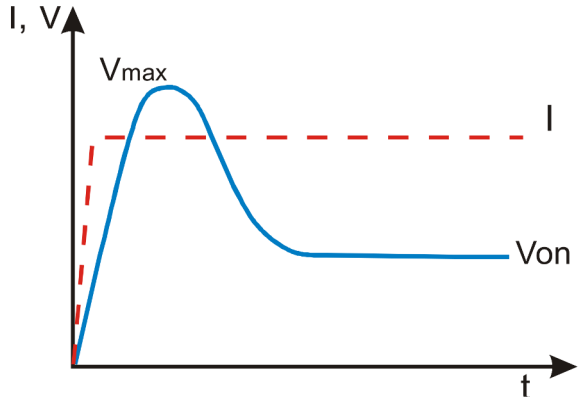


Figure 1.12. Diode current and voltage during the turn-on.

- **Turn-off transitory**

The *reverse recovery* is fundamental specification for P-i-N rectifier. It refers to switching process needed to bring the device from the on-state to the blocking state and governed by the free charge excess removing. When the switch (MOSFET for example) closes on the circuit, its current linearly increases from the times t* to t_0. The diode starts to turn-off and its current linearly decreases. Due to the presence of the stored charge within the drift layer, the diode is still conducting even after t_0 and the current is negative. Only after the time t1 two depletion regions at the junction P^+-N Drift and N Drift-N^+ start to developing toward the drift layer center. From the time t_0 to t_5 the product of the I_{RR} reverse recovery current and the growing reverse voltage of the diode gives an important contribution of power dissipation. Figure 1.13 shows the turn-off transitory waveforms together with a one-dimensional cross section of the currier distribution within the drift layer.

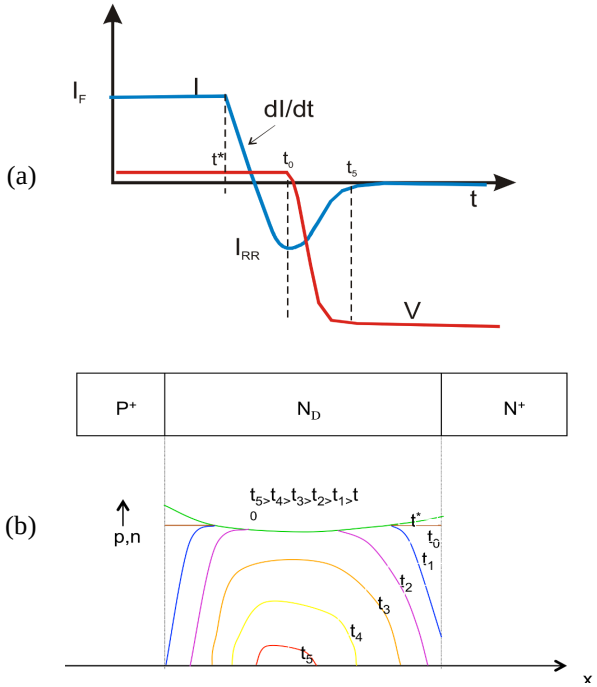


Figure 1.13. P-i-N rectifier turn-off waveforms (a) and free carriers distribution (b).

t_{RR} reverse recovery is time employed by the diode to remove the exceeded charge and approaching to a non-conduction condition. The charge stored into the drift layer and then removed is Q_{RR}. Under the assumption of a triangular shape of the current curve, geometrical consideration leads to:

$$Q_{RR} \cong \frac{I_{RR} t_{RR}}{2} \tag{1.41}$$

$$I_{RR} \cong \frac{di}{dt} \frac{t_{RR}}{2} \tag{1.42}$$

Since Q_{RR} must be the same stored in forward conduction, it can be related to the lifetime as:

$$Q_{RR} = Q_F = I_F \tau \tag{1.43}$$

Substituting eq.(1.41) and eq.(1.42) into eq.(1.43), I_{RR} can be described by:

$$I_{RR} \cong \frac{2\tau I_F}{t_{RR}} = \frac{\tau I_F}{I_{RR}} \frac{di}{dt} \cong \sqrt{\tau I_F \frac{di}{dt}} \tag{1.44}$$

From the eq.(1.44) the following expression for t_{RR} can be provided:

$$t_{RR} = \frac{2\tau I_F}{t_{RR} \frac{di}{dt}} = \sqrt{\frac{2\tau I_F}{\frac{di}{dt}}} \tag{1.45}$$

Considering the relation of the lifetime τ with I_{RR} and t_{RR}, it points out as a fast turn-off switching needs of a low carriers lifetime. Lifetime killing techniques are adopted to realize *fast recovery diodes* without compromising their on-voltage drop.

1.4 Insulated Gate Bipolar Transistor (IGBT)

The IGBT is a semiconductor device constitutes by four alternating layers (P/N/P/N) with a metal-oxide-semiconductor (MOS) gate structure operating as controlling terminal without regenerative action. Nowadays, IGBT has become the most important power devices for medium and high power applications.

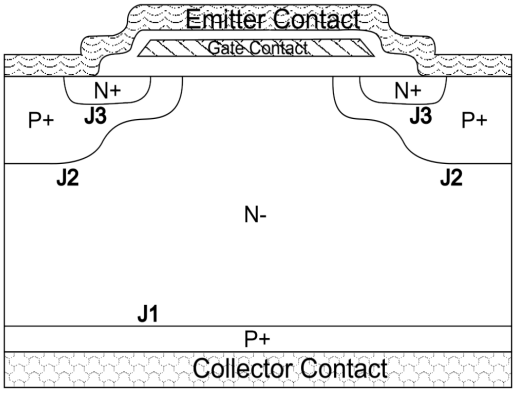


Figure 1.14. IGBT basic structure.

The geometry of a basic IGBT structure for a Planar Non-Punch-Through IGBT (NPT-IGBT) is depicted in Figure 1.14, but during the years, many different structures have realized. The device is composed by paralleling thousands elementary cells each of them with a common design. For the IGBT, as for the Power MOSFET, the multicellular approach poses no problems because it has an intrinsic thermal stability. A P/N/P/N is a thyristor structure, which can be activated by applying a voltage on the gate terminal. More in detail, the N^+ region is the emitter diffusion and represents the source of the MOSFET part of the device; while the P-body region is both the body of the MOSFET part of the device and the collector of the vertical PNP structure of the IGBT. The threshold voltage of the MOSFET part of the device is defined by the doping concentration of the P-body region at the Silicon/Oxide interface. The low-doped region is designed thick enough to sustain the high voltage when the device is

in the blocking state. In the IGBT, this region represents either the low-doped drain of the MOSFET and the n-base of the vertical PNP. The collector of the IGBT is the P+ region (the emitter of the vertical PNP), also called “hole-injecting layer”. The back part of the structure is achieved by doping diffusion up to the junction J1 and requires special laser treatments. As regards the top design, channel is realized by the difference in lateral extension of the P-base and N^+ source regions. Both regions are self-aligned to the gate region sides during ion implantation used to introduce the respective dopants; while polysilicon is used as gate terminal.

- **Device operation**

P^+ collector layer play a fundamental rule in the IGBTs since it allows the conductivity modulation into the drift-layer in on state condition. The device operates in blocking state when the gate-emitter voltage is kept to zero. In this situation, applying a positive voltage to the collector, the collector-drift junction (J1) becomes forward biased, while the P-body-drift junction (J2) is reversely biased and the leakage current of this junction is the only current flowing into the device. This condition, called *forward blocking*, is limited by the breakdown of J2 that is the open base breakdown voltage of the PNP. If a negative voltage is applied to the collector terminal, still keeping the gate-emitter voltage to zero, the junction J1 is reversely biased while J2 is directly biased. This is the *reverse blocking* condition. For a NPT structure, the forward blocking capability is equal to the reverse blocking capability, due to symmetric with respect to the drift layer. To achieve the on-state condition, a gate-emitter voltage higher than the threshold voltage have to be applied. In such condition, a positive collector-emitter voltage allows the electrons flowing across the MOSFET channel under the gate and then across the drift region. On the other hand, holes are also injected from the collector into the drift region, due to directly biased collector-drift junction, recombining with electrons injected by the channel and a double injection of carriers occurs into the drift layer. The collector of the PNP collects the exceeding holes. With the increasing of the current density, the density of the mobile charges becomes higher than the doping concentration of the drift layer. Since it is needed to keep the

neutrality of the charge in the drift layer, high concentrations of both electrons and holes are reached with the voltage drop consequently reduced. This bipolar effect is called “conductivity modulation”. Because of the P-body/drift junction cannot be directly biased in on-state, therefore, the vertical PNP never enters in saturation mode. However, when the gate voltage is slightly above the threshold voltage the MOSFET enters in pinch-off condition, limiting the electron current delivered to the drift region, and consequently the overall current as well. The conductivity modulation has the advantage in reducing the on voltage drop, but also the drawback in accumulating a high amount of charges. Indeed, when the device is switched off, the channel of electrons is fastly removed but the remaining charge stored in the drift region can be removed only by recombination mechanisms. During the charge removal time the device exhibits a classical collector “current tail”. For this reason, there exists a conflictual condition between forward voltage drop and turn-off switching times: by increasing the exciding charge in the drift layer, the forward voltages is reduce but producing an increment of the effective turn-off time for the device.

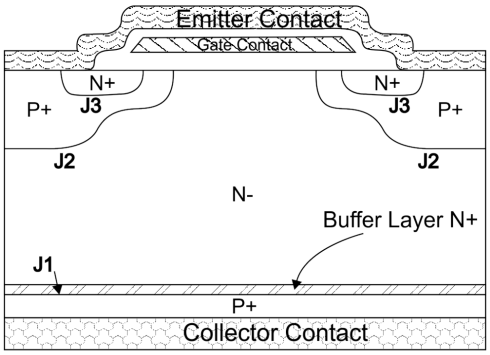


Figure 1.15. Geometry of a Punch-Through IGBT.

A structure able to reduce the off switching time, but keeping a large on state voltage drop is shown is presented in Figure 1.15 [20].The structure, named Punch-Through IGBT (PT-IGBT), presents an additional N doped buffer layer between the collector and drift region having higher doping respect this last layer. The higher electron density in the Buffer layer favors a partial recombination of holes injected from the collector within the buffer reducing the collector

junction efficiency. Since the minority carrier lifetime in the base region is also reduced, a lower charge concentration in the drift layer is generated producing a higher voltage drop in the on-state. Moreover, it leads to a faster recombination of excess charges during the turn-off, resulting in a shorter turn-off time. The doping profile and electric field distribution of a symmetric and asymmetric IGBT can be compared observing Figure 1.16 and Figure 1.17, respectively. Symmetric structure presents a triangular field profile that approach to zero before reaching the opposite junction. This happens in both forward and reverse blocking, which have the same $V_{CE,MAX}$, This because BV_{CE0} and BV_{CB0} are very similar due to the low value of α_{pnp} being the large width of the epy-layer. Asymmetric structure has a trapezoidal field profile in forward blocking that allows to reach a larger $V_{CE,MAX}$ in forward blocking. The buffer layer must be thin enough to guarantee that depletion region of J_2 does not reach the J_1 junction. At the same time, its doping concentration is imposed to reduce the injection efficiency of the junction J_1 able to degrade the forward conduction characteristic.

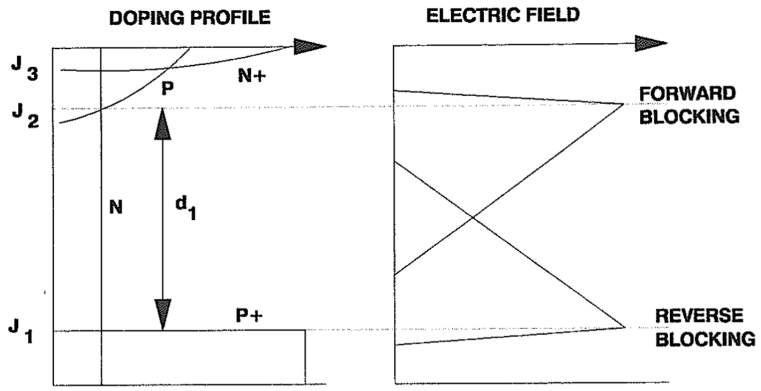


Figure 1.16. Doping profile and electric field distribution of a symmetric IGBT structure.

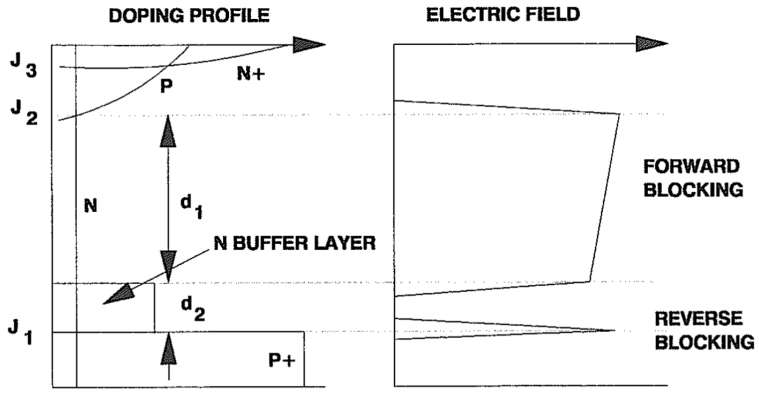


Figure 1.17. Doping profile and electric field distribution of a symmetric IGBT structure.

- **Static characteristic**

The analysis of the forward conduction characteristics of an IGBT can be described by means of two equivalent circuit as illustrated in Figure 1.18.

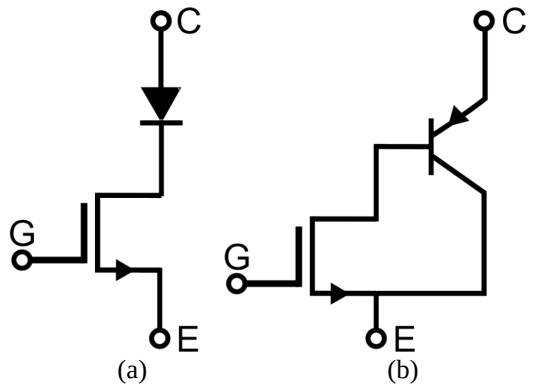
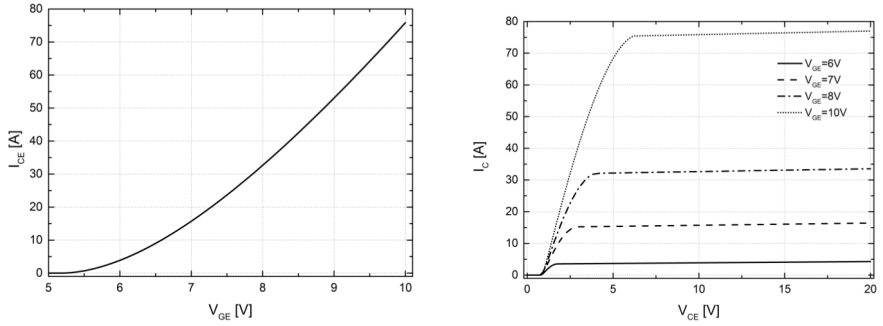


Figure 1.18. Equivalent model of an IGBT: a) Power MOSFET and diode; b) Power MOSFET and PNP transistor in Darlington configuration

The first equivalent circuit is based on a PiN-rectifier in series with a MOSFET. It provides only an approximation of the device behavior in the forward state, since this model does not consider the current produced by the holes flowing within the P-base region. The junction formed by P-base and drift region is reversely biased during forward

mode and the free charge density must be zero as reaching the junction. As effect, the conductivity modulation of the IGBT in the drift region is identical to the PiN diode near the collector junction, but lower than a PiN diode near the P-base junction [21]. The second circuit is based on a Darlington configuration. The Power MOSFET current supplies the base current of a PNP transistor, providing a deeper and more precise description of the conduction characteristics. Both circuits shows that IGBT has the same voltage drop of a Power diode. If the collector-emitter voltage is lower than the diode built-in voltage, a negligible current flowing into the device. As above mentioned, the gate-emitter voltage creates the electron channel between the emitter and the drift region with the electrons injection that increases with growing the applied voltage. The static characteristics of an IGBT are depicted in Figure 1.19.



(a) (b)

Figure 1.19. Simulated IGBT static characteristics: (a) I_C-V_{GE} for V_{CE} = 10V; (b) I_C-V_{CE} for different gate-emitter voltages.

With the second model an important effect is considered. In fact, due to the large thickness and low doping concentration of the drift region, the PNP transistor provides low current gain factor, consequently the Power MOSFET in the equivalent circuit carries a major contribution to the total collector current. Therefore, the on-state voltage of the IGBT includes also a significant drop across the MOSFET portion. In particular, near the P-base junction the conductivity modulation has a minor effect resulting in a considerable drop across the JFET resistance of the MOSFET in addition to the voltage drop across the channel resistance and the accumulation layer resistance as reported in [22]. A solution able to remove the JFET resistance of the MOSFET

current path is *trench* design, whose structure is depicted in Figure 1.20.

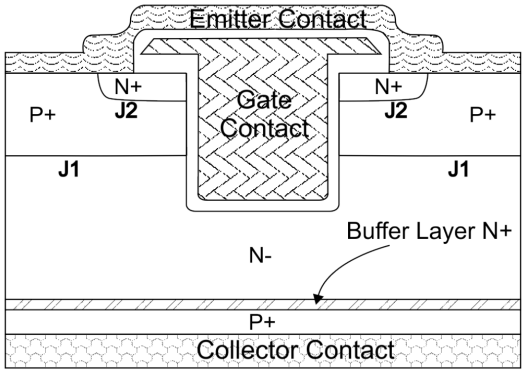


Figure 1.20. Trench IGBT structure.

In addition, the Trench structure provides a robustness improvement to the latching because it reduces the resistive path in the P-base region. Assuming a pinch-off condition of the Trench (T)-IGBT, the collector current results:

$$I_C = \frac{\mu_n C_{OX} W_{CH}}{2L_{CH}(1-\alpha_{\mathrm{PNP}})}(\mathrm{V_{GE}} - \mathrm{V_{th}})^2 \tag{1.46}$$

where W_{CH} and L_{CH} are the width and the length of the MOSFET channel, respectively.
For this structure the on-state voltage drop can be seen as the sum of three contributions:

$$V_{ON} = V_{PN} + V_{NB} + V_{MOSFET} \tag{1.47}$$

where V_{PN} is the drop on the forward biased Collector/Buffer junction, V_{NB} is voltage across Drift region and V_{MOSFET} is the component due to the MOSFET structure. More in detail, V_{PN} contribution can be calculated as:

$$V_{PN} = \frac{kT}{q}\ln\left(\frac{p_0 N_{D,NB}}{n_i^2}\right) \tag{1.48}$$

where p0 is the hole concentration at Collector/Buffer junction, and ND,NB is the Buffer doping concentration. The MOSFET voltage contribution is given by:

$$V_{MOSFET} = \frac{J_C L_{CH} P}{2\mu_n C_{OX}(V_G - V_{th})} \tag{1.49}$$

where P is the cell pitch. As regards the contribution across the Buffer, it can considered composed by two parts:

$$V_{NB} = V_{NB1} + V_{NB2} \tag{1.50}$$

$$V_{NB1} = \frac{2L_a J_C \sinh(W_N / L_a)}{qp_0(\mu_n + \mu_p)} \cdot \cdot \left\{ \tanh^{-1}\left[\exp(W_{ON} / L_a)\right] - \tanh^{-1}\left[\exp(W_N / L_a)\right] \right\} \tag{1.51}$$

$$V_{NB2} = \frac{kT}{q}\left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right) \ln\left[\frac{\tanh(W_{ON} / L_a)\cosh(W_{ON} / L_a)}{\tanh(W_N / L_a)\cosh(W_N / L_a)}\right] \tag{1.52}$$

where $L_a = \sqrt{D_a \tau_{HL}}$ is the ambipolar diffusion length, W_{ON} is the depletion region, W_N is the part of the Drift not reached by the depletion. Both contributions are very affected by the high injection lifetime of the Drift layer.
Finally, it is considered the I_C-V_{GE} characteristic in sub-threshold region, which depends on the Gate Oxide/P-body interface. The sub-threshold can be calculated considering the expression of the surface potential as follows [23]:

$$S_{S-th} = \left[\ln(10)\frac{\mathrm{kT}}{q}\left(1 + \frac{C_D}{C_{Ox}}\right)\right]^{-1} \tag{1.53}$$

- **Transient characteristic**

As done for the analysis of the PiN diode, even in this case a simplest power switching circuit is considered (see Figure 1.21). The inductor load, which presents a free-wheeling diode in parallel, can be considered as a constant current source during the on- and off-switching of the device.

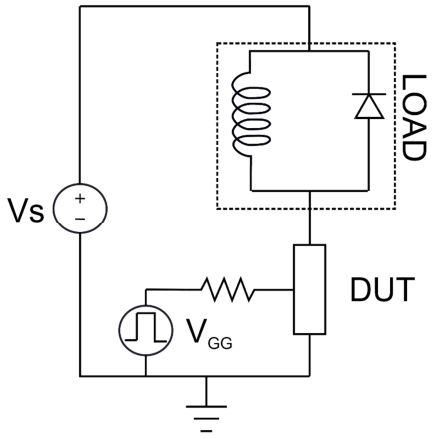


Figure 1.21. Simplest power switching circuit.

Turn-on characteristics The MOS structure governs the turn-on switching performance of the IGBT. The IGBT turn-on waveforms are illustrated in Figure 1.22. The turn-on starts when a voltage V_{GG} is applied by the driving circuit. During the time interval t0-t1 the voltage values is lower than the MOSFET threshold voltage, which remains in the blocking region. During this interval a gate current flows charging the gate-source capacitance and the V_{GS} grows exponentially governed by the input capacitance and resistance. When V_{GS} approaches the threshold voltage the device starts to conduct with a current proportional to the applied gate-source voltage. During the interval t1-t2 V_{GS} keeps on rising exponentially until the drain current reaches the load current at the time t2. At t2 the load current completely flows though the IGBT with the diode that starts to switching off. In this phase the device is in pinch-off regime due to the high value of V_{DS} (the collector potential is assumed as the drain potential for the MOSFET). At time t3 the device enters in the triode regime since the V_{DS} has almost reached the forward voltage drop with the gate voltage that starts to rise again. The power dissipation is significant only during the interval t1-t3 where the voltage-current product is large.

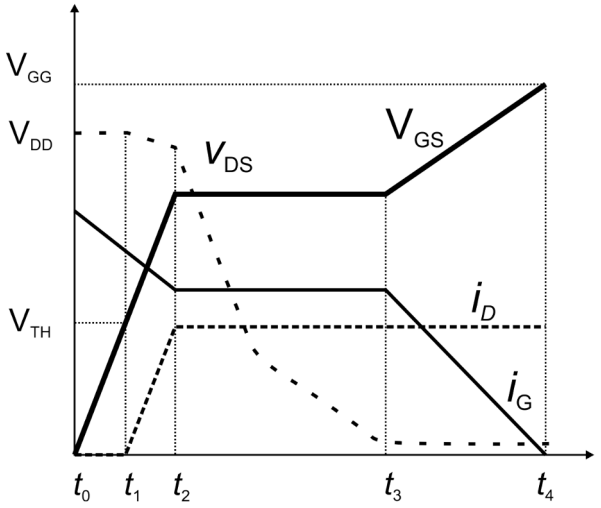


Figure 1.22. IGBT turn-on waveforms.

Turn-off characteristics Turn-off waveforms are depicted in Figure 1.23.

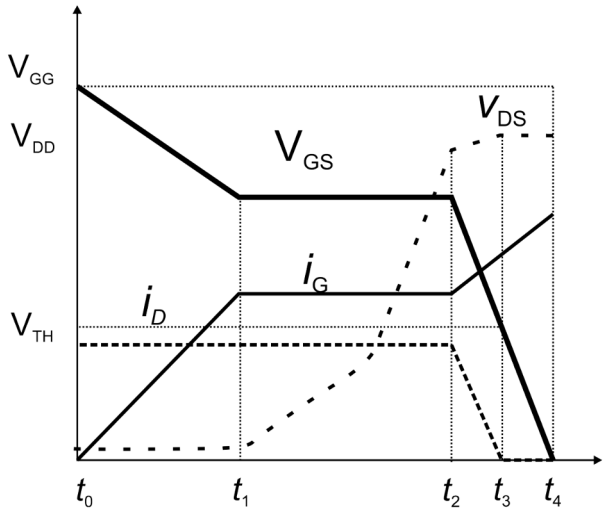


Figure 1.23. IGBT turn-off waveforms.

Turn-off transient starts when the external gate terminal drives V_{GG} to zero. This leads to an exponential lowering of the gate-emitter voltage to the value for which the device is in saturation regime. Collector

voltage and current keep constant during this phase. At time t1, the collector voltage rises, but the current is still constant. With the increasing of the collector voltage, the current flows into the Miller capacitance towards the driving circuit, across the gate resistance. This last governs the current in the Miller capacitance and, for this reason, the collector voltage rate of rise becomes critical project parameter. When the collector voltage is high enough, the free-wheeling diode starts to conduct its current increases. As a consequence, the IGBT current decreases until to reach to a finite value due to the stored charge within the drift region. Recombination mechanisms allow a gradual decreasing of the minority carriers resulting a *current tail*. During this phase the collector voltage is at its maximum value and current tail produces a significant power dissipation in the device. The duration of the current tail limits the IGBT operating frequency and trade-off between on-state losses and switching times is therefore needed. A method to partially overtake this drawback consists on localized control of the lifetime in order to reduce the recombination time of the free carriers within the drift region.

- **Latch-up of Parasitic Thyristor**

One of the most significant problem in IGBT structures is the presence of a parasitic N-P-N structure. When the minority carriers injected by the collector flow toward the emitter terminal, they tend to pass in a narrowed area near the gate terminal. This current path develops a spreading resistance of the P-base region. If this current is significantly high, the base-emitter junction of the NPN-parasitic BJT can become forward biased. The NPN current drives the PNP-transistor to the on-state, and therefore the parasitic thyristor will latch up and the gate loses control over the collector current. Reducing the gain of the NPN- or PNP-transistors can prevent the parasitic thyristor to latch-up. However, this means to increase the IGBT on-state voltage drop. Different solution can be adopted to contrast the letch-up phenomenon like the reduction of carrier lifetime, the use of Buffer layer, and the use of deep P^+-body diffusion. This last solution allows reducing the spreading resistance but requires a fine control of the P^+ region extension. It has to be adequate to prevent the device from

latch-up, but it cannot extend into the MOS channel because this would cause an increase in the MOS threshold voltage.

- **Safe operating area**

The Safe Operating Area is defined as the values of current and voltage for which the device can safety operate. For IGBT it must be separately considered the case of forward operations, that is when the gate-emitter voltage is positive, and reverse operations, when the gate-emitter voltage is zero or negative.

Forward Biased Safe Operating Area (FBSOA) The FBSOA is represented of the safe operations conditions when the gate bias is applied and both electrons and holes flows in the IGBT and the collector voltage is still at high values. Different phenomena regulate this condition. In particular, the breakdown phenomenon limits the maximum sustainable voltage, while for lower voltage the limit depends on the maximum power dissipation. Finally, for very low voltage, the letch-up phenomenon limits the maximum current. As regards the breakdown, it is regulated by gain of the *pnp* as discussed in the previous section.

Reverse Biased Safe Operating Area (RBSOA) When the IGBT is reversely biased, no electrons flow in the device and only a holes current component is present. The RBSOA is therefore limited only by the avalanche phenomenon occurring to the junction formed by P-base and drift region. The electric field depends on the net charge in the drift region and with the increasing of the hole concentration the breakdown voltage becomes lower than the one determined by the only background donor concentration and it reduces with the increasing of the current. It is also lower than the correspondent FBSOA breakdown voltage because hole concentration is not compensate by the electrons. As for FBSOA, also the RBSOA is limited by latch up phenomenon for lower voltage. When an IGBT turns off the device current is determined only by the holes current. If the P-base parasitic resistance is high enough for turns on the NPN transistor, the parasitic thyristor turns on and latch up occurs. This phenomenon limits the maximum current owing in the structure for low voltage values.

1.5 Terminations

Semiconductor power device are made in appropriate packages realized for specific application. Their cutting require the use of special diamond blades, which inevitably provoke a damage at the crystalline lattice. If the cut reaches a device zone designated to sustain high voltages, the generated damage produce as effect a leakage current increasing able to reduce the breakdown capability and its stability during the time. For this reason, the periphery area of power devices, usually named as termination, is made with special design. In reverse polarization at high voltage, to the depletion region at the termination should not intersect the damaged zones. In vertical power devices, another problem is related to the BV due to the curvature of the electrostatic potential at the periphery area. Planer junction in modern devices are achieved by using appropriated dioxide masks lied on semiconductor surface. Creating an open window through the mask it is possible to diffuse the impurity by means of either thermal diffusion or ionic implantation (Figure 1.24).

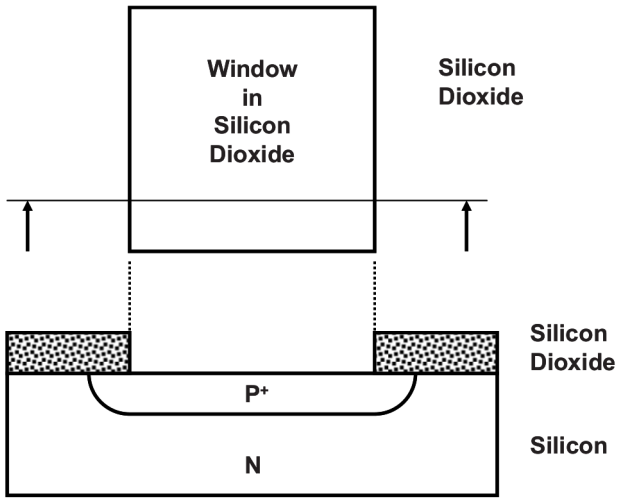


Figure 1.24. Planar diffusion mask in silicon devices.

During the drive-in process, the impurity diffusion takes place in both vertical and lateral directions. Lateral diffusion is about the 85% of the

vertical one depending on the oxidation type, crystalline orientation and segregation. If the open window within the mask is rectangular, there is an accumulation of impurities in correspondence of the window corners (Figure 1.25).

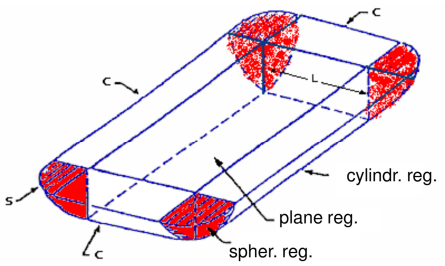


Figure 1.25. 3D diffusion effects with a rectangular window in dioxide mask.

Such impurities are distributed in tridimensional space comparable to slice of sphere, which introduce electric field curvature effects modifying the BV [24]. For the same applied voltage, the electric field will result to have more intensity around the curve region producing a premature breakdown. To explain this effect it can be refer to Figure 1.26, where is shown a section of the planar diffusion.

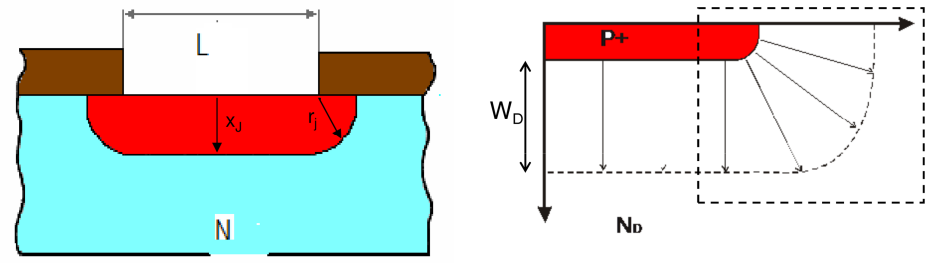


Figure 1.26. Planar junction section.

Assuming an isotropic diffusion: $r_j = x_j$ and approximating L >> r_j, the cylindrical region can be analyzed within the (E,r) plan by considering the Poisson's equations in radial coordinates :

$$\frac{1}{r}=\frac{d}{r}(rE)=\frac{Q(r)}{\varepsilon}=\frac{-qN_D(r)}{\varepsilon} \qquad (1.54)$$

Integrating the first term between r and r_D (in correspondence of which E = 0) it achieves the radial electric field [25]:

$$E(r) = -\frac{qN_D(r)}{\varepsilon}\left[\frac{r_D^2 - r_J^2}{r}\right] \tag{1.55}$$

The electric field at the abscissa r_j assumes its maximum value:

$$\left|E_M\right|_{CIL} = \frac{qN_D}{2\varepsilon}\left[\frac{r_D^3 - r_J^3}{r_J}\right] \tag{1.56}$$

Since N-region is low doped, with a low value of ND there is a large depletion region resulting in $r_D >> r_j$:

$$\left|E_M\right|_{CIL} \sim \frac{qN_D}{2\varepsilon}\left(\frac{r_D^2}{r_J}\right) \tag{1.57}$$

For the planar junction $W_D = r_D - r_j$ and always for $r_D >> r_j$:

$$\left|E_M\right|_{PL} = \frac{qN_D W_D}{\varepsilon} = \frac{qN_D r_D}{\varepsilon} \tag{1.58}$$

The ratio between planar and cylindrical electric field results:

$$\frac{\left|E_M\right|_{CIL}}{\left|E_M\right|_{PL}} \sim \frac{r_D}{2r_J} >> 1 \tag{1.59}$$

Poisson's equation in spherical coordinates is:

$$\frac{1}{r^2} = \frac{d}{r}(r^2 E) = \frac{Q(r)}{\varepsilon} = \frac{-qN_D}{\varepsilon} \tag{1.60}$$

Integrating the first term between r and r_D:

$$E(\mathrm{r}) = \frac{-qN_D(r)}{3\varepsilon}\left[\frac{r_D^3 - r_J^3}{r^2}\right] \tag{1.61}$$

The maximum spherical electric field is:

$$\left|E_M\right|_{SF} = \frac{qN_D}{3\varepsilon}\left[\frac{r_D^3 - r_J^3}{r_J^2}\right] \tag{1.62}$$

for $r_D >> r_j$:

$$\left|E_M\right|_{CIL} \sim \frac{qN_D}{3\varepsilon}\left(\frac{r_D^3}{r_J^2}\right) \tag{1.63}$$

The ratio between cylindrical and spherical electric field results:

$$\frac{\left|E_M\right|_{SF}}{\left|E_M\right|_{CIL}} \sim \frac{2r_D}{3r_J} >> 1 \tag{1.64}$$

Eq.(1.59) and eq.(1.64) highlight as $|E_M|_{SF} >> |E_M|_{CIL} >> |E_M|_{PL}$, the critical electric field E_{CR} at the breakdown will be higher respect to the planar case. Electric field curvature effect of the bidimensional case, and even more in tridimensional case, reduce the voltage at which the breakdown occurs at the junction. Firstly, tridimensional case can be avoided by acting on the mask design. In particular, the corners of the open window should be rounded with an adequate curvature radius. This solution permits to reduce the problem to the alone bidimensional case. Different techniques have been developed during the years with the scope, not only to contrast the damage effect, but also to maximize the BV with a lower consumption of periphery area.

1.5.1 Floating field ring technique

A simple approach able to increase the BV near a value of the planar junction consists in surrounding the diffusion window of the active area with Floating Field Ring (FFR) [26] as in Figure 1.27. Since the ring is floating, it is not electrically connected with any terminal, depending on the distance W_s by the active area, its potential is at a value in the between respect to the applied voltage.

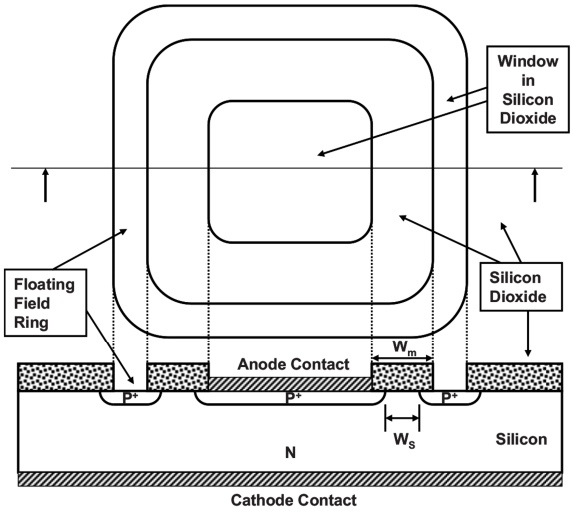


Figure 1.27. Planar junction with a single field ring

It is possible to use the same diffusion process of the main junction without increasing the technological steps. Hence, doping peak concentration and diffusion depth will be equal for both main junction and field ring. The distance W_s is a fundamental parameter for this technique. If the ring is too close to the main junction its beneficial effect will be weak, and the ring simply behaves as prolong of the active area. On contrary, a too elevate distance will not permit to the ring potential of coupling with that of the active area. In other word, if W_s is too small the electric field remains that of cylindrical one, while a W_s too large mitigates the ring effect resulting in a premature breakdown.

Applying the Poisson's equation to the structure in Figure 1.27 results [27]:

$$\frac{d^2V}{dy^2} = -\frac{dE}{dy} = V_R - \frac{qN_D}{\varepsilon} \qquad (1.65)$$

where V_R is the reverse voltage applied at the cathode terminal. Considering the following boundary conditions

$$\begin{cases} V = 0, & per \quad y = 0 \\ V = V_R, & per \quad y = W_D \end{cases} \qquad (1.66)$$

It achieves

$$|V(y)| = V_R - \frac{q}{\varepsilon} N_D \left(W_D y - \frac{y^2}{2} \right) \tag{1.67}$$

Eq.(1.67) highlights that by increasing the cathode voltage V_R the depletion region extends along y-direction reaching the floating ring, and the breakdown will be premature if $W_S < W_{BV}$. W_{BV} is the value of the depletion region at which the breakdown occurs.
For y = W_S

$$|V|_{FR} = V_R - \frac{q}{\varepsilon} N_D \left(W_D W_S - \frac{W_S^{\,2}}{2} \right) \tag{1.68}$$

From eq.(1.68) two limit cases are pointed out:

$$\begin{cases} V_{FR} = V_R, & per \quad y = 0 \\ V_{FR} = 0, & per \quad W_S \to W_{BR} \end{cases} \tag{1.69}$$

Not only the distance Ws is important to maximize the BV but also the width of the ring. Figure 1.28 shows the modification occurring to the depletion region boundary depending on the floating ring width. A largest ring width produces as effect an enlarging of the depletion space with consequent increasing of BV, since this last results from integrating the electric field on the depletion region.

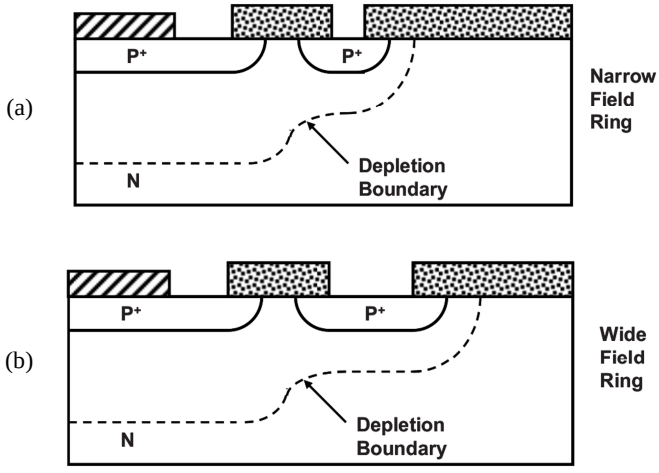


Figure 1.28. Depletion region boundary in dependence on the floating ring

width.

Another design solution able to reduce the electric field cylindrical effect consists in the using of a Field Plate (FP) [28]. It is a prolongation of the metal layer of the main junction contact lying on top of dioxide layer and extends for a length LFP (Figure 1.29).

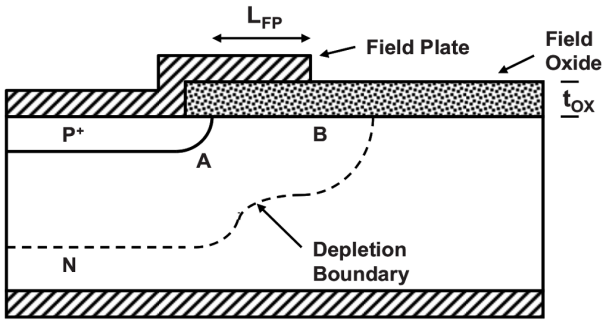


Figure 1.29. Field plate effect on planar junction

Since the electrostatic potential is constant along the whole metal layer, this last produces the same effect of a negative charge at the oxide layer, allowing a lateral extension of the depletion region. FP is able to mitigate the cylindrical field at the point A increasing the BV. On the other hand, the cylindrical field is generated at the FP edge (point B). Regarding the electric field at the edge of the FP it is related to oxide thickness following dependence described by Gauss' low:

$$x_j = \frac{\varepsilon_{Si}}{\varepsilon_{Ox}} \approx 3 \cdot t_{Ox} \tag{1.70}$$

If the main junction has a depth of 6 µm the breakdown at the field plate will be that of cylindrical for an oxide thickness of about 2 µm. The oxide thickness, together with the FP length, can be optimized in order to maximize BV by appropriate balancing the two peaks at the points A and B.

More in general, with the increasing of BV rate it is needed to use more complex structures, which exploit the action of several floating rings often surrounded by field plates. To understand the effect of multi guard rings structure on the electrostatic potential it can be considered the following theoretical discussion [29]. The multi-FFR

structure having two rings P2 and P3 and the main junction P1 illustrated in Figure 1.30 is analyzed.

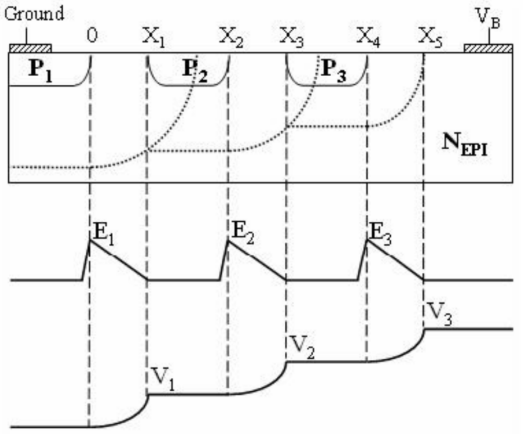


Figure 1.30. Cross section of FFR structure with theoretical one-dimensional electric field and potential distributions at the surface.

Integrating the Poisson equation of (1.7) the one-dimensional electric field and the potential at the junction P1 can be written as:

$$E_1(x) = \frac{qN_{EPI}}{\varepsilon}(x_1 - x) \tag{1.71}$$

$$V_1 = \frac{qN_{EPI}}{\varepsilon}x_1^2 \tag{1.72}$$

where x_1 is the distance between the junctions P_1 and P_2.
Iterating for each junction:

$$E_2(x) = \frac{qN_{EPI}}{\varepsilon}(x_3 - x_2) \tag{1.73}$$

$$V_2 = \frac{qN_{EPI}}{2\varepsilon}(x_3 - x_2)^2 + V_1 \tag{1.74}$$

$$E_3(x) = \frac{qN_{EPI}}{\varepsilon}(x_5 - x_4) \tag{1.75}$$

$$V_3 = \frac{qN_{EPI}}{2\varepsilon}(x_5 - x_4)^2 + V_2 = V_{BR} \tag{1.76}$$

To maximize the BV the surface electric field peak on each junction must be equalized, in other word:

$$V_1 = V_2 - V_1 = V_3 - V_2 \tag{1.77}$$

Largely diffused is the adoption of a termination design realized combining both FFR and FP techniques. Any single FP modifies the potential distribution of the ring reducing electric field at the ring edge. To optimize this structure needs acting on both the rings geometries and field plates extensions, since this last the FP also introduce a further field peak. The presence of the a metal layer having the same potential of the contacted ring is able to prevent the entering of mobile ions, which can produce instabilities effect like walkout.

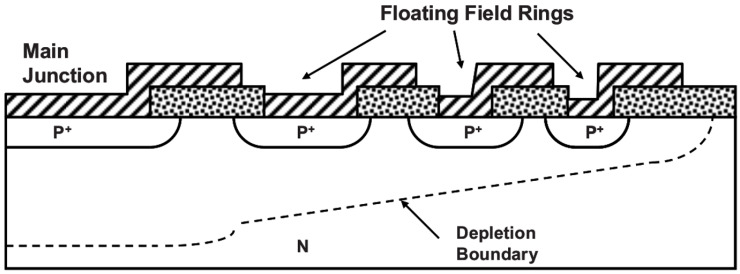


Figure 1.31. Multiple FFR termination assisted by field plates.

1.5.2 Junction termination extension technique

JTE design was introduced for the first time by Temple in 1977 for planar and plane p-n junctions [30]. A manipulation of the surface electric field is realized by controlling the implant dose of a low doped P region, which extends from the main junction toward the device periphery (Figure 1.32).

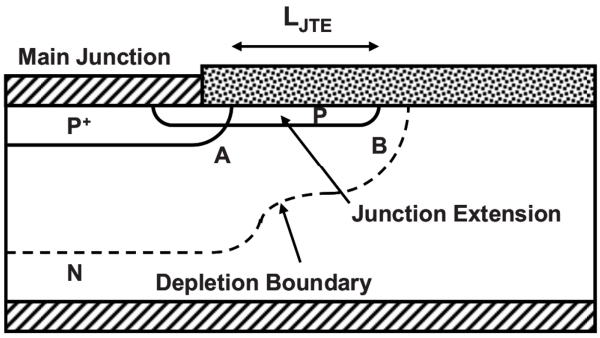


Figure 1.32. Geometry of a classical JTE termination.

P diffusion has the same dopant type of the active area, but its dose Q_1 is only a fraction of that of the ideal junction Q_0. Indeed, to reduce the cylindrical electric field effect it is necessary to balance both peaks at the edge of the main junction and at the edge of the JTE region, namely point *A* and *B*, respectively. As shown in Figure 1.33, if Q_1 is too low, the effect of the P diffusion is too weak and a high peak occurs at the point *A*; on the other hand, if Q_1 is too high, the potential of the main junction is simply translated resulting in a peak occurring at the point *B*.

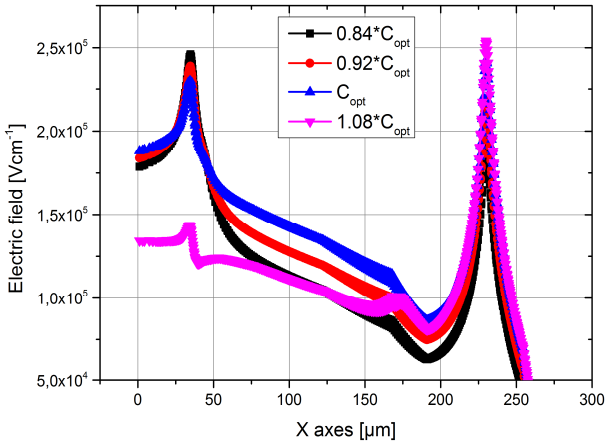


Figure 1.33. Simulated surface electric field distribution for different peak doping concentrations of P diffusion.

The dose Q_1 of the P diffusion can be calculated considering the critical electric field E_{CR} of the ideal junction multiplied for the dielectric constant ε_S as following:

$$Q_1 = \int_0^W qN_A dex = qN_A W_D = E_{\max}\varepsilon_S \qquad (1.78)$$

A further reduction of the peak at the point *A* can be achieved extending the contact metal layer in order to realize a field plate. Indeed, noted the epi-layer doping concentration and thickness, only a well precise peak concentration will guarantee a fully depleted P region. The main drawback of this technique is the high breakdown instability in case of fluctuations of the P doping profile as visible in Figure 1.34.

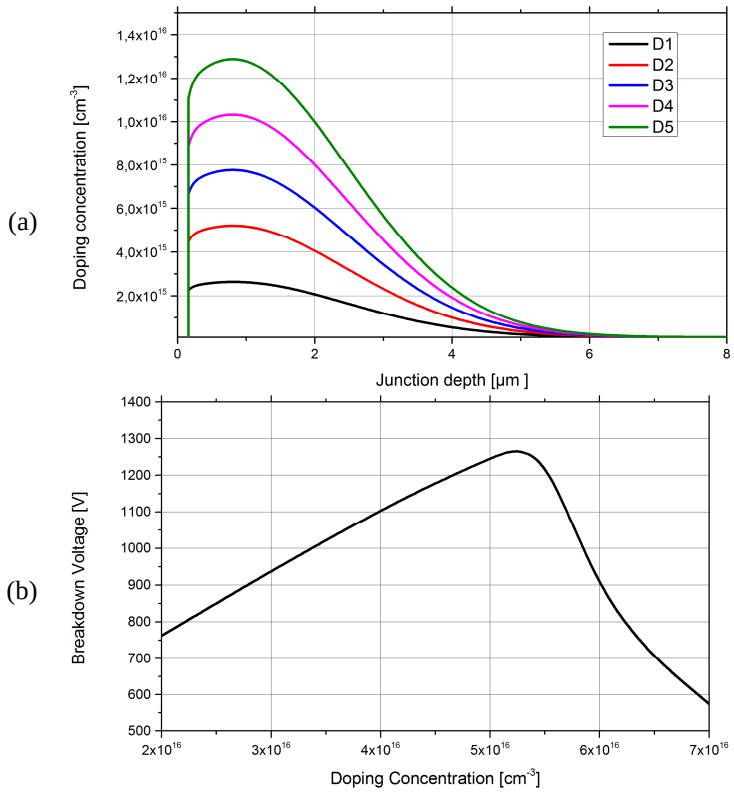


Figure 1.34. (a) Simulation P doping profile for different doses, D1=1x10^{12} cm^{-2}, D2=2x10^{12} cm^{-2} , D3=3x10^{12} cm^{-2} , D4=4x10^{12} cm^{-2} D5=5x10^{12} cm^{-2} (b) Simulation BV dependence on P region peak concentration.

Two solution are possible to improve the performance of the termination by using a JTE multi-masking approach. A first approach [31] consists of dividing the P region in more diffusions, for example three as illustrated in Figure 1.35.

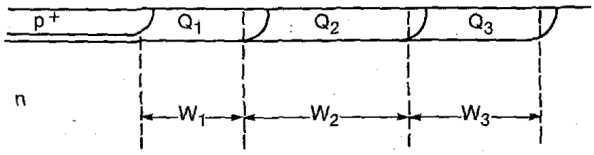


Figure 1.35. Geometry of a three masking JTE termination.

Each diffusion is realized with its own mask (*W* is the diffusion extension) and implant dose *Q*. In particular, the combination of W_1, W_2, W_3 and the ratio Q_1/Q_2 and Q_3/Q_2 determine the maximum efficiency of the structure.
The second approach [32] results less expensive since it allow using a single dose implantation just modifying the window size of each diffusion. The window size must be gradually enlarged going from the main junction to the extern part. In addition, appropriately designing the distance among each mask it is possible to favor the diffusions overlapping generating a similar effect realized by the previous approach. A simplest geometry of the described approach is shown in Figure 1.36.

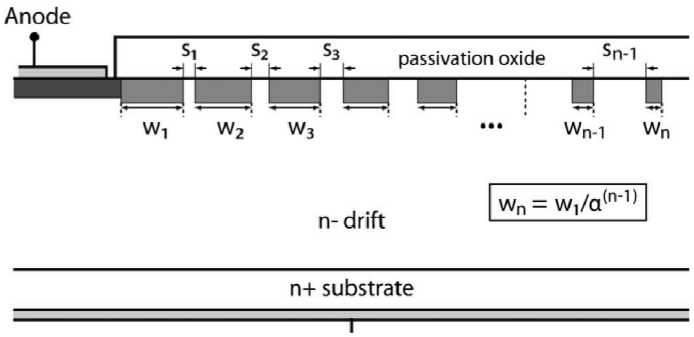


Figure 1.36. Cross section of a Multiple Zone JTE termination

1.5.3 Surface passivation and SIPOS layer

Breakdown instability, like so, the leakage current can be greatly improved by the surface passivation. During the various technological steps, the mobile charge can remain entrapped close to the semiconductor surface. As consequence, an alteration of the superficial electric field can occur leading to a different breakdown voltage. An adequate passivation is able also to reduce the quantity of defects at the surface, like dislocations, which directly affect the leakage current due to presence of traps levels in the band gap. The passivation in planar device is commonly realized with silicon dioxide. However, because of sodium and potassium are able to pass through the dioxide layer, this last is preventively covered by silicon nitride or oxynitride by means of plasma-enhance chemical vapor deposition. Another approach consists in using a layer of Semi-Insulating Polycrystalline Silicon (SIPOS) [33]. This latter is an electrical material doped with oxygen. It is realized by chemical vapor deposition [34], at low pressure (LPCVD) or atmospheric pressure (APCVD), at temperature in the range of 600-700 °C. Used as passivation layer, it does not exhibit walkout phenomena degradation of the α_{pnp} or breakdown voltage. Oxygen dopant allows reducing the density of surface states that contribute to the surface generation current, thus reducing the leakage current [35]. Leakage current in dependence on oxygen concentration in SIPOS passivation of a P^+-n diode is shown in Figure 1.37. The leakage current decreases with increasing the oxygen concentration. After about 15% of oxygen content no further reduction of surface density states takes place. This happens with contemporary increasing of SIPOS resistivity. On the other hand, the BV also decreases with increasing the oxygen percentage as visible in Figure 1.38. In particular, an oxygen content beyond the 8% increases the resistivity of SIPOS lowering the field relaxation effect.

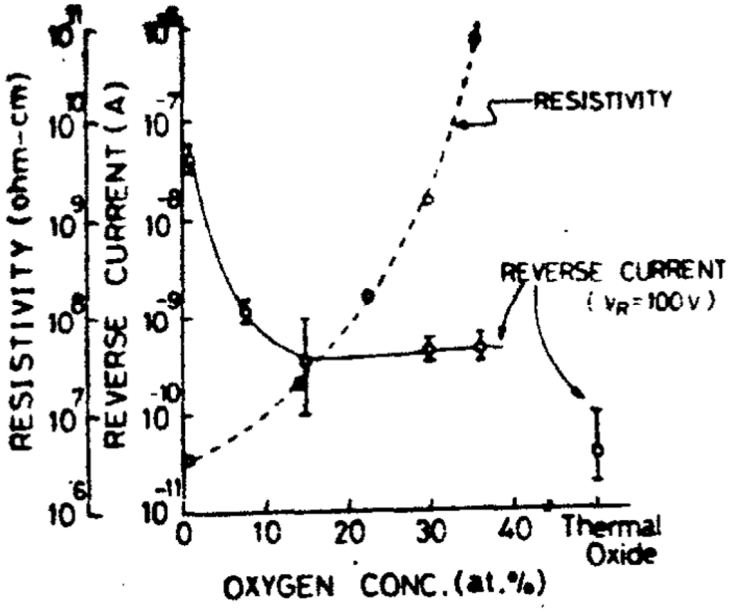


Figure 1.37. Leakage current and SIPOS resistivity as a function of oxygen concentration.

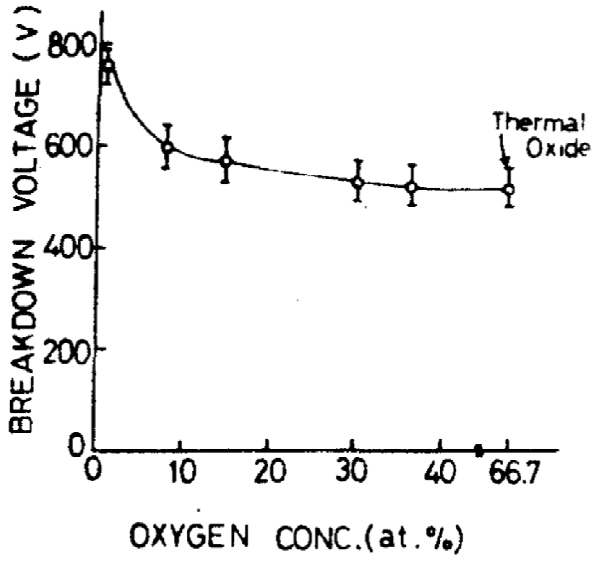
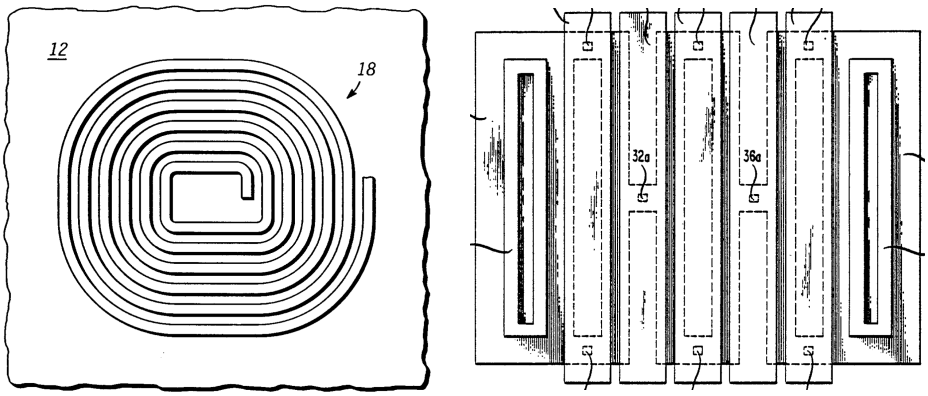


Figure 1.38. P^+-n diode BV as a function of SIPOS oxygen concentration.

Another way to increase the SIPOS layer resistivity without acting on oxygen doping consists in designing the layer geometry. Two examples of design are illustrated in Figure 1.39. In one case SIPOS layer is realized in spiral shape [36], in the other has an interdigitated form [37].



(a) (b)

Figure 1.39. Patent SIPOS layer geometries realized to reduce the layer resistivity.

1.6 TCAD simulations

The use of device numerical modeling and simulation is essential in the world of industry in order to analyze and develop semiconductor power devices. Technology Computer Aided (TCAD) consists in using of computer simulations for designing and optimizing semiconductor processing technologies and devices. TCAD simulations instruments allow reducing time and costs of a production process helping the comprehension on the influence of the design parameters and predicting the electrical behavior.
Synopsys Sentaurus TCAD suite [38] is the simulator used in this work. It operates in Linux environment and it is used to work on 2D and 3D structures simulating optical, thermal and electrical characteristics. Sentaurus TCAD tools solve fundamental, physical, partial differential equations (e.g. diffusion and transport equations)

by discretizing the device domain in finite elements, whom are associated the respective physical equation and parameters. Figure 1.40 shows the typical flow-chart to run a simulation in Sentaurus TCAD.

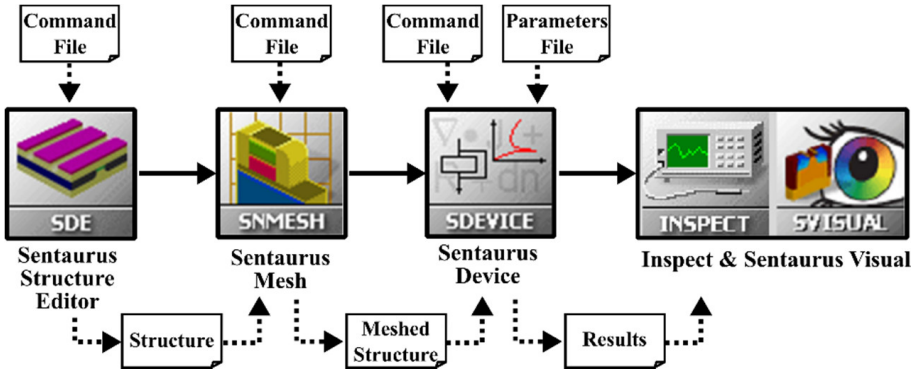


Figure 1.40. Sentaurus tool flow.

In first place, it is needed to define the geometry and doping profiles of the virtual structure. Process simulations can be performed considering each technological step like etching, ion implantation, thermal annealing and oxidation. In this work, process simulations are used to show both the technological steps of FFR termination and the difficulty in generating a real doping profile of a JTE process.
An easier alternative consists in reconstructing the structure knowing the geometrical dimensions from SEM section, creating the doping profiles as superposition of elementary analytical expression (e.g. Gaussian or Error-function). The latter approach has been mainly adopted in this work, using the software Sentaurus Structure Editor. With this tool is possible to define geometry, materials and doping profiles, both for 2D and 3D structures.
The domain of the realized structure is discretized onto a non-uniform grid (or mesh) of nodes. In this way, the device is represented as a meshed finite-element structure, at which every nodes of the device have physical properties associated with them. Physical equations are solved for each node and the carrier concentration, current densities, electric field, generation and recombination rates, and so on, are computed. Thus, an efficient mesh is necessary to obtain realistic results, and therefore the number of points has to be carefully chosen

as compromise between results accuracy and simulation time. A valid mesh can be obtained by trial and by observing the error during the computation, even though some practical rules can be applied. The number of nodes should be increased in zones where some physical parameters could have a significant spatial gradient. It means, for example, that the number of nodes should be increased where it is expected to have high current density or high electric field. For a Power MOSFET, critical sections usually are the channel, the body/drift depletion region, the interface oxide/semiconductor, the JFET region. In avalanche breakdown analysis, critical sections are located in parts of device where the ionization takes place. Another possibility to discretize the structure consists in using Sentaurus MESH. It is the tool provided with Sentaurus TCAD dedicated to discretize spatial domains and to generate doping profiles. Its axis-aligned mesh generator engine produces triangles in the case of 2D devices and tetrahedra in the case of 3D devices. Such tool is provided of exclusive sections able to manage either the mesh grid at the materials interface and/or the angolation of each triangle/tetrahedra to improve the simulation convergence.

Once a proper mesh has been completed, the device can be simulated with Sentaurus Device. As visible in Figure 1.40 different sections in the command file have to be specified to deal a simulation. The adopted physical models able to describe the physical device behavior are listed in a *physics* section. Solver configuration and settings helping convergence are defined in a *math* section. Different type of simulations can be computed and specified in the *solve* section. Each of them as quasistationary, transient, etc. uses the boundary conditions specified in the *electrode* statement. An external parameters file **.par* provides the activated models associated to each adopted material. Output data such as terminal characteristics, physical quantities (specified in a plot section) can be then visualized through visualization tools like Sentaurus Visual or Inspect.

The simulation of a device implies the computation of terminal currents and voltages using a set of physical equations that describes the carrier distribution and conduction mechanisms [39].

The primary step to simulate a device is to solve the Poisson’s equation and the continuity equation based on the Boltzmann carrier transport theory for the electrostatic potential, electrons and holes:

$$\varepsilon \cdot \nabla^2 \psi = -q \cdot (p - n + N_D^+ - N_A^-) - \rho_S \tag{1.79}$$

where ε is the electrical permittivity, q is the electronic charge, n and p are the electron and hole densities, N_D is the concentration of ionized donors, N_A the concentration of ionized acceptors and ρ_S is the surface charge density due to traps and fixed charges. Considering the Boltzmann statistic and given the quasi-Fermi potentials, the electron and hole densities can be expressed as:

$$n = N_C \exp\left(\frac{E_{F,n} - E_C}{kT}\right) \tag{1.80}$$

$$p = N_V \exp\left(\frac{E_V - E_{F,p}}{kT}\right) \tag{1.81}$$

where N_C and N_V are the effective density-of-state, $E_{F,n}$ and $E_{F,p}$ the quasi-Fermi energy levels for electron and hole, E_C and E_V the conduction and valence band edges.
The continuity equation for electrons and holes are given by:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \cdot \vec{\nabla} \vec{J}_n - U_n \tag{1.82}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \cdot \vec{\nabla} \vec{J}_p - U_p \tag{1.83}$$

where J_n and J_p are the electron and hole current densities, while U_n and U_p are recombination rates of electrons and holes, respectively. The analytical expressions of J_n and J_p depending on the transport model used to compute them. Different models are available in Sentaurus, considering that even the simple use of *drift-diffusion model* and the *thermodynamic model* provides an accurate describing of power devices behavior.

- **Drift-diffusion model**

It is the default transport model in Sentaurus. The general expressions for electron and hole current densities, valid for both Fermi and Boltzmann statistics, are:

$$J_n = \mu_n (n\nabla E_C - 1.5nkT\nabla \ln m_n) + D_n(\nabla n - n\nabla \ln \gamma_n) \quad (1.84)$$

$$J_p = \mu_p (p\nabla E_V - 1.5pkT\nabla \ln m_p) - D_p(\nabla p - p\nabla \ln \gamma_p) \quad (1.85)$$

The first term takes into account the contribution related to the spatial variations of the electrostatic potential, the electron affinity, and the band gap. The remaining terms are related to the contribution due to the gradient of concentration, and the spatial variation of the effective masses. Considering valid the Boltzmann statistic, $\gamma_n = \gamma_p = 1$. The Einstein's relation permits to calculate the diffusivity coefficients through the mobilities:

$$\frac{D_{n,p}}{\mu_{n,p}} = \frac{kT}{q} \quad (1.86)$$

Equations 1.38 and 1.39 can be simplified as:

$$J_n = -nq\mu_n \nabla \Phi_n \quad (1.87)$$

$$J_p = -pq\mu_p \nabla \Phi_p \quad (1.88)$$

where Φ_n and Φ_p are the electron and hole quasi-Fermi potentials.

- **Thermodynamic model**

Thermodynamic model [40] considers the temperature gradient as driving term included in current densities equations 1.41 and 1.42:

$$J_n = -nq\mu_n(\nabla \Phi_n + P_n \nabla T) \quad (1.89)$$

$$J_p = -pq\mu_p(\nabla \Phi_p + P_p \nabla T) \quad (1.90)$$

where $P_{n,p}$ are the absolute thermoelectric powers [41] and T is the lattice temperature.

- **Boundary conditions**

To correctly solve differential equations it is necessary defining the boundary conditions at the borders of a domain. By default, each contact on semiconductor, if connected to a circuit node, assumes an Ohmic value of 1mΩ. Assuming also charge neutrality and equilibrium, it can be written:

$$n_0 - p_0 = N_D - N_A \tag{1.91}$$

$$n_0 p_0 = n_{i,eff}^2 \tag{1.92}$$

Assuming Boltzmann statistics:

$$\phi = \phi_F + \frac{kT}{q} \operatorname{arcsin} h\left(\frac{N_D - N_A}{2n_{i,eff}} \right) \tag{1.93}$$

$$n_0 = \sqrt{\frac{(N_D - N_A)^2}{4} + n_{i,eff}^2} + \frac{(N_D - N_A)}{2} \tag{1.94}$$

$$p_0 = \sqrt{\frac{(N_D - N_A)^2}{4} + n_{i,eff}^2} - \frac{(N_D - N_A)}{2} \tag{1.95}$$

where n_0 and p_0 are the electron and hole concentration at equilibrium and ϕ_F the Fermi potential. In the case of gate contacts, the metal contact lies on the insulator layer and the electron potential is expressed as:

$$\phi = \phi_F - \phi_{MS} \tag{1.96}$$

where Φ_{MS} is the work function difference between the metal and the intrinsic level in the semiconductor.
For all boundaries that are not contacted Neumann condition is applied:

$$\varepsilon \nabla \phi = 0 \tag{1.97}$$

$$J_{n,p} \cdot \hat{n} = 0 \tag{1.98}$$

As regards the thermal problem, in case of thermally insulated surfaces the following condition is applied:

$$k\hat{n} \cdot \nabla T = 0 \tag{1.99}$$

On the other hand, at thermally conducting interfaces the boundary condition become:

$$k\hat{n} \cdot \nabla T = \frac{T_{ext} - T}{R_{th}} \tag{1.100}$$

with R_{th} external thermal resistance characterizing the thermal contact between semiconductor and adjacent material.

- **Band structure**

Structure band is fundamental property for semiconductor device simulations. Band gap and density-of-states are summarized in the intrinsic density for the undoped semiconductor:

$$n_i(T) = \sqrt{N_C(T)N_V(T)}\exp\left(-\frac{E_g(T)}{2kT}\right) \tag{1.101}$$

while the dependence of the band gap by the temperature is modeled as:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \tag{1.102}$$

where $E_g(0)$ is the band gap at T = 0K while α and β are values material dependent.
The electron affinity, i.e. the energy separation between the conduction band and that of valence is represented as:

$$\chi(T) = \chi_0 + \frac{(\alpha+\alpha_2)T^2}{2(T+\beta+\beta_2)} + Bgn2Chi \cdot E_{bgn} \tag{1.103}$$

where χ_0, *Bgn2Chi* (0.5 is default value) are adjustable values and E_{bgn} includes the band gap narrowing effect.

- **Band gap narrowing**

Heavy doping influences the density producing an effect called "bandgap narrowing". Sentaurus supports different bandgap model: *BennettWilson, delAlamo, OldSlotboom and Slotboom, JainRipulston* and *TableBGN*. In this work, the *OldSlotboom* model has been adopted and the following relation describes the bandgap modification:

$$\Delta E_g^0 = E_{ref}\left[\ln\left(\frac{N_{tot}}{N_{ref}}\right) + \sqrt{\left(\ln\left(\frac{N_{tot}}{N_{ref}}\right)\right)^2 + 0.5}\right] \tag{1.104}$$

The model is based on measurement of $\mu_n n_i^2$ in PNP transistors. E_{ref} and N_{ref} are fitting parameters.

- **Mobility models**

The carrier mobilities can be dependent on several physical phenomena such as *phonon scattering, doping, high electric field, etc.* [42].Sentaurus uses a modular approach for the description of the carrier mobilities following for each contribution the Matthiessen'n rule:

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + ... \tag{1.105}$$

If the model for high electric field is activated, as in this work, the final mobility is calculated in two steps. The first one, μ_{low} is determined according to eq. (1.105) for low electric field; while the second one, is function of a driving force F_{hfs}.
Phonon scattering model is only dependent on lattice temperature [43]:

$$\mu_{Ph} = \mu_L \left(\frac{T}{300K} \right)^{-\xi} \tag{1.106}$$

where μ_L and ξ are accessible parameters.
The doping dependence can be described though several relations. Arora model has been adopted in this work due to its immediate comprehension and its eventual easy modification [44].

$$\mu_{dop} = \mu_{\min} + \frac{\mu_d}{1 + ((N_{A,0} + N_{D,0}) / N_0)^{A^*}} \tag{1.107}$$

with:

$$\mu_{\min} = A_{\min} \cdot \left(\frac{T}{300K} \right)^{\alpha_m}, \mu_d = A_d \cdot \left(\frac{T}{300K} \right)^{\alpha_d} \tag{1.108}$$

and:

$$N_0 = A_N \cdot \left(\frac{T}{300K} \right)^{\alpha_N}, A^* = A_a \cdot \left(\frac{T}{300K} \right)^{\alpha_a} \tag{1.109}$$

Each parameter is accessible in the parameters file list.

Mobility degradation at interface is important in MOSFETs or IGBTs to describe the influence of the transverse electric field in the channel region. The free carriers in the channel are confined close to the surface in a thin layer. At the semiconductor/insulator interface, carriers are subjected to scattering by surface phonon due to lattice vibrations, interface state and fixed charge and surface roughness. Scattering surface contribution can be modeled using Lombardi model [43]:

$$\mu_{ac} = \frac{B}{F_{\perp}} + \frac{C((N_{A,0} + N_{D,0} + N_2)/N_0)^{\lambda}}{F_{\perp}^{1/3}(T/300K)^{k}} \tag{1.110}$$

$$\mu_{sr} = \left(\frac{(F_{\perp}/F_{ref})^{A^*}}{\delta} + \frac{F_{\perp}^3}{\eta} \right)^{-1} \tag{1.111}$$

where A^*, B, C, N_0, N_2 are fitting parameters and $F_{\perp}$ is the electric field normal to the semiconductor/insulator interface. The acoustic phonon scattering contribution μ_{ac} and the surface roughness scattering contribution μ_{sr} are combined with bulk contribution according to Matthiessen's rule eq.(1.105).

When a high electric field prevail, the carrier drift velocity is no longer proportional to the field, resulting in a saturation of carriers velocity:

$$v = \mu \cdot E \tag{1.112}$$

The model adopted in this work is Canali model [45], which originates by Caughey-Thomas formula [46]:

$$\mu(F) = \frac{(\alpha+1)\mu_{low}}{\alpha + \left[1 + \left(\frac{(\alpha+1)\mu_{low}F_{hfs}}{v_{sat}} \right)^{\beta} \right]^{1/\beta}} \tag{1.113}$$

by default α=0 while the exponent β is temperature dependent. Saturation velocity is part of Canali model and is given by:

$$v_{sat} = v_{sat,0}\left(\frac{300K}{T} \right)^{v_{sat,\exp}} \tag{1.114}$$

where $v_{sat,0}$ and $v_{sat,exp}$ are accessible parameters. F_{hfst} represents the driving force, which supported in Sentaurus by five different models.

Whit the first model, *Eparallel*, the driving field for electrons is the electric field parallel to the electron current:

$$F_{hfs,n} = \vec{F} \cdot \frac{\vec{J}_n}{J_n} \tag{1.115}$$

Even if physically correct to describe both mobility and avalanche generation, this kind of driving suffers of numeric instability for small current J_n. The second model, *GradQuasiFermi*, is an alternative with improved numeric stability:

$$F_{hfs,n} = \left|\nabla \Phi_n\right| \tag{1.116}$$

In this latter, the driving field follows the gradient of quasi-Fermi potential. In general, eq.(1.115) and (1.116) provide the same results. The remaining models are not here discussed.

- **Recombination and generation models**

Recombination-generation processes occur in semiconductor, operating under thermal equilibrium, to balance the exchanging of carriers between conduction and valence bands. As discussed in the previous paragraph, the most relevant recombination mechanism in silicon semiconductor is the SRH, whose model in Sentaurus is in according with eq.(1.18). The electron and hole lifetimes are expressed as function of doping concentration, electric field and temperature:

$$\tau_c = \tau_{dop} \frac{f(T)}{1+g(T)} \tag{1.117}$$

As regards the doping dependence of the SRH lifetime, it is modeled according to the Scharfetter relation [47][48][49]:

$$\tau_{dop}(N_{A0}+N_{D0}) = \tau_{\min} + \frac{\tau_{\max}-\tau_{\min}}{1+\left(\frac{N_{A0}+N_{D0}}{N_{ref}}\right)^{\gamma}} \tag{1.118}$$

where N_{ref} is a fitting parameter.
The temperature dependence of the SRH lifetime can be expressed either by a power low or by an exponential expression:

$$\tau(T) = \tau_0 \left(\frac{T}{300K}\right)^{\alpha}, \quad \tau(T) = \tau_0 \, \mathrm{e}^{C\left(\frac{T}{300K}-1\right)} \tag{1.119}$$

Experimental measurements show a positive dependence of the excess of carriers with the temperature (α, C >1), but its behavior is, in general, strongly dependent on the nature of the recombination centers and difficult to predict.
The effect of the electric field on SRH lifetime becomes relevant in when a P/N junction is reverse biased under a strong electric field ($3x10^5$ V/cm).
In the heavily doped regions, another recombination mechanism of the injected minority carriers is the Auger recombination [50][51][52]. It can be described by the following recombination rate:

$$R_{net}^{A} = \left(C_n n + C_p p\right)\left(np - n_{i,eff}^2\right) \tag{1.120}$$

where the Auger coefficients $C_n(T)$, $C_p(T)$ are temperature dependent.
The avalanche generation is governed by the following generation rate:

$$G_{Av} = \alpha_n n v_n + \alpha_p p v_p \tag{1.121}$$

where α_n and α_p are the ionization coefficients defined in eq(1.1). Sentaurus implements different models for the impact ionization coefficients: *van Overstraeten-de Man, Okuto-Crowell, Lackner, University of Bologna,* new version *University of Bologna* and *Hatakeyama.*

Van Overstraeten-de Man model Based on the Chynoweth low [5]:

$$\alpha(\mathrm{F_{ava}}) = \gamma a \exp\left(-\frac{\gamma b}{F_{ava}}\right) \tag{1.122}$$

with:

$$\gamma = \frac{\tanh\left(\frac{\hbar\omega_{op}}{2kT_0}\right)}{\tanh\left(\frac{\hbar\omega_{op}}{2kT}\right)} \tag{1.123}$$

Eq.(1.123) expresses the temperature dependence of the phonon gas against which carriers are accelerated. a, b and ω are fitting parameters calculated by van Overstraeten-de Man.

New University of Bologna Model It is calibrated with special impact ionization measurements and covers a wide range of electric field [53][54][55].

$$\alpha(\mathrm{F_{ava}},\mathrm{T}) = \frac{F_{ava}}{a(\mathrm{T}) + \mathrm{b}(\mathrm{T})\exp\left[\dfrac{d(\mathrm{T})}{F_{ava} + c(\mathrm{T})}\right]} \qquad (1.124)$$

where *a, b, c, d* are polynomial coefficient of T.

1.7 Process emulation of a FFR termination

In this section a process flow of a FFR termination is simulated by means of Synopsys simulation tool Sentaurus Process. The process flow has been realized by the research group of Fraunhofer Institute ISIT. The FFR structure is termination of PT-IGBT 600V rated.
Sentaurus Process is an advanced 1D, 2D, and 3D process simulator suitable for silicon and semiconductor semiconductors. It features modern software architecture and state-of-the-art models to address current and future process technologies. Sentaurus Process simulates all standard process simulation steps, diffusion, implantation, Monte Carlo (MC) implantation, oxidation, etching, deposition, and silicidation [56] .
The process flow consists of the following steps:

- Oxide growing on the epitaxial layer
- Boron implantation and diffusion
- Gate oxidation thermal budget
- Active area implantations and diffusions

The following theory on process fabrication has been referred to [57]-[59]. The first step, after the epitaxial growing, an oxide layer is realized by means of thermal oxidation. The oxide layer will operate as protection mask during the boron implantation for the rings realization. Two thermal oxidation mechanisms are possible: 1)

Oxidation of silicon in oxygen (dry oxidation); 2) Oxidation of silicon in water vapor (wet oxidation).

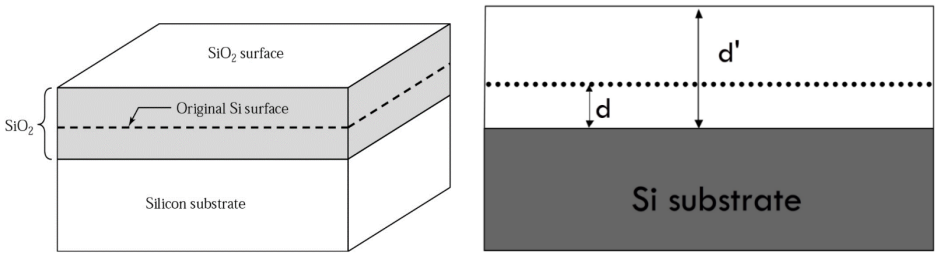
Dry oxidation: Silicon reacts with O_2 to form SiO_2:

$$Si(s)+O_2(s)\rightarrow SiO_2(s) \tag{1.125}$$

Wet oxidation: Silicon reacts with water to form SiO_2:

$$Si(s)+2H_2O(g)\rightarrow SiO_2(s)+2H_2(g) \tag{1.126}$$

During the thermal oxidation, the silicon surface is consumed with the Si/SiO_2 interface moving into the wafer as shown in Figure 1.41.



(a) (b)

Figure 1.41. (a) Movement of silicon/oxide interface during the SiO_2 growing. (b) Cross section of silicon/oxide interface.

The cross sectional image of Figure 1.41 (b) shows as to generate an oxide layer with a thickness *d'*, a silicon layer of *d* thickness is also consumed. The relation between *d* and *d'* can be achieved by applying the molar conservancy low:

$$\frac{dA\rho_{Si}}{Z_{Si}}=\frac{d'A\rho_{SiO_2}}{Z_{SiO_2}} \tag{1.127}$$

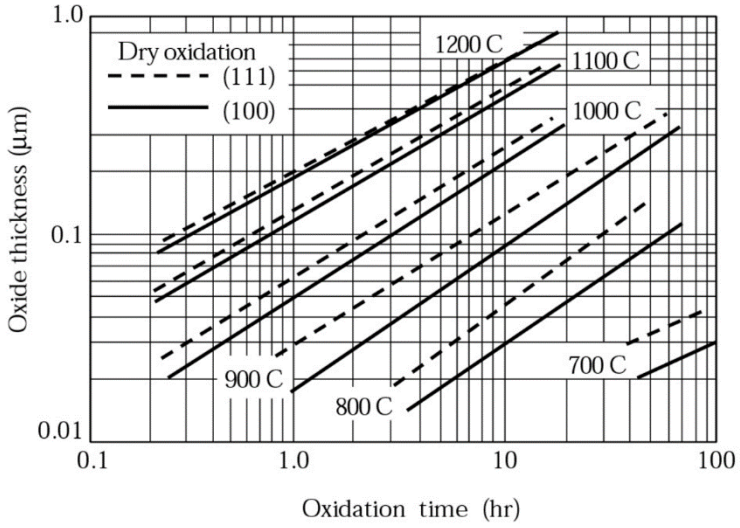
where *A* is cross section area equal for the two materials, ρ_{Si}, Z_{Si}, ρ_{SiO2} and Z_{SiO2} are the density and atomic weight of silicon and oxide, respectively.
From eq. (1.127) the relation between *d* and *d'* results:

$$d'\simeq 1.88d \tag{1.128}$$

This means that to grow 1000 nm of oxide by thermal oxidation, 532 nm of silicon are consumed in the reaction. To control the oxide layer

growing it is need acting on the temperature and duration time of the wafer within the furnace as visible in Figure 1.42.

(a)



(b)

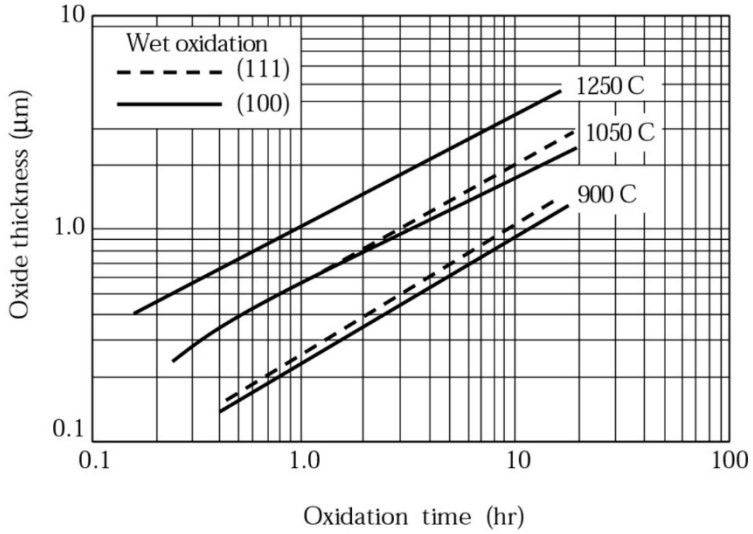


Figure 1.42. Oxide thickness for Si (100) and Si (111) at different temperature for dry (a) wet (b) oxidations.

The rings masks can be realized by means of chemical attaching. Before to proceed with doping deposition a “screening” oxide layer is

grown. As demonstrated in [60], a deeper Boron penetration is achieved as thinner as the screen oxide layer, especially with increasing the implantation energy (see **Figure 1.43**). In addition, in the screen oxide allows light scattering of the ion beam during ion implantation, which prevent the generation of ions channel.

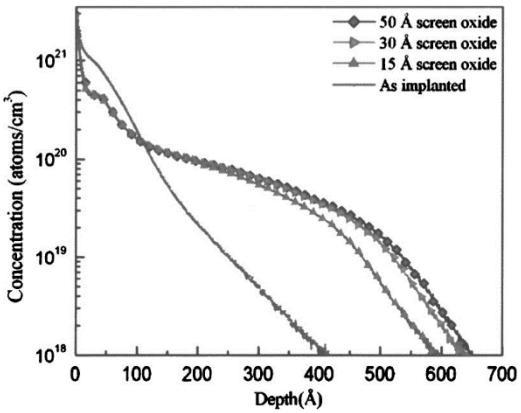
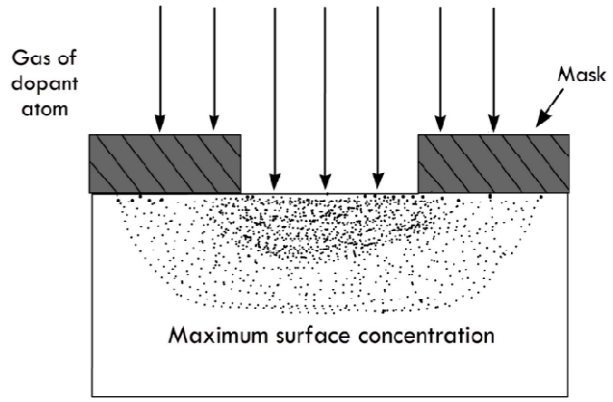


Figure 1.43. Boron SIMS profiles in Si. Thicker oxide during annealing gives deeper junction.

The doping phase, i.e. the introduction of specific impurity within the semiconductor, can be basically realized with two method: 1) Thermal diffusion (Figure 1.44(a)); 2) Ion implantation (Figure 1.44(b)).

(a)



(b)

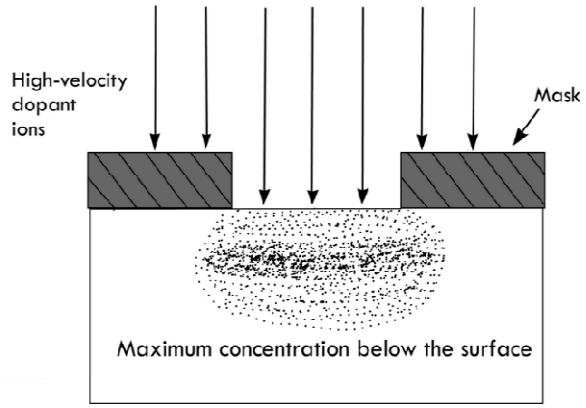


Figure 1.44. (a) Thermal diffusion. (b) Ion implantation.

In analogy with thermal oxidation, thermal diffusion consists in two step process. The first one, the deposition is the introduction of dopant atoms at the wafer surface; the second one, the drive-in is the diffusion of the dopant into the wafer to create the required gradient profile. During the thermal diffusion, the dopant moves vertically but it also spread laterally reducing the effective distance between two adjacent junctions. The dopant source can be in different states solid, liquid or gaseous. This determine a different shape of doping profile within the wafer. The drive-in operation can be realized using dry oxidation or wet oxidation. The diffusion of impurity into the crystalline can be either for vacancy diffusion or for interstitial substitution. The impurity distribution depends on several the crystalline properties, impurity atoms and temperature. During the oxidation there is a dopant redistribution phenomenon called *segregation*. When two solid phases are in contact, an impurity can move in one or another solid until it reaches equilibrium. The segregation coefficient K is defined as the ratio between concentration of impurity in one material and the other at the equilibrium; in this case the two materials are silicon and dioxide:

$$K = \frac{C_{Si}}{C_{SiO_2}} \tag{1.129}$$

Hence, K is related to how fast the dopant may diffuse through the silicon or dioxide material. This acts as a mask against dopant for

most of the dopant species. For instance, the Boron has a segregation coefficient less than one but the diffusion within the dioxide is slow and remains quite constant for a considerable distance. This generates a sort of concentration depletion at the Si-SiO2 interface (Figure 1.45). If the Boron is working oxidation ambient its diffusion on the dioxide side is slow while it would be fast in case of hydrogen ambient. In some cases the dopant can segregate at the Si-SiO_2 interface remaining not activated, bringing to a consumption up to the 50% of the implanted dose.

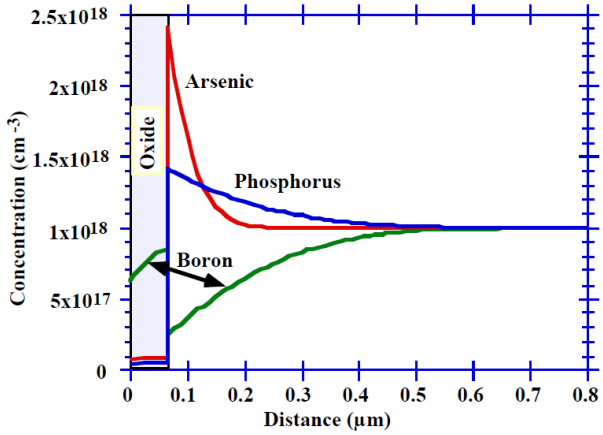


Figure 1.45. Segregation affect in oxidation ambient for three dopant species B, P, and As.

Assuming that the impurity flux J is constant respect to the time, it can be calculated using the Flick's first low as:

$$J = -D\frac{\partial C(x,t)}{\partial x} \tag{1.130}$$

where C is the concentration, x is the distance from the surface, t the time. The diffusion coefficient D is expressed as:

$$D = D_0 \exp\left(-\frac{E_a}{K_B t}\right) \tag{1.131}$$

where E_a is the activation energy for diffusion.

One of the main drawbacks of the thermal diffusion is due to the isotropic diffusion of atoms, which lead to a too high lateral spreading

with increasing of the diffusion depth. For this reason, the ion implantation method is widely adopted. It operates at low temperature by means of chemical reaction. The schematic of an ion implanter is illustrated in Figure 1.46. The ionization system operates at high voltage ionizing the dopant atoms in gas phase. Than the ions selected with a mass spectrometer pass through an accelerator, which add energy to beam up to 5MeV. Finally, a scanning system is used to appropriately deflect the beam across the wafer producing a uniform implantation.

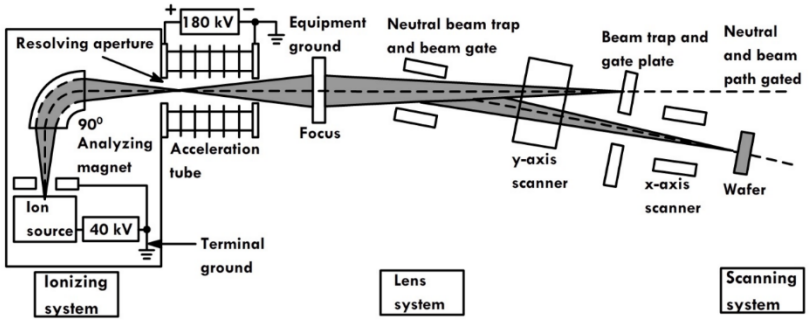
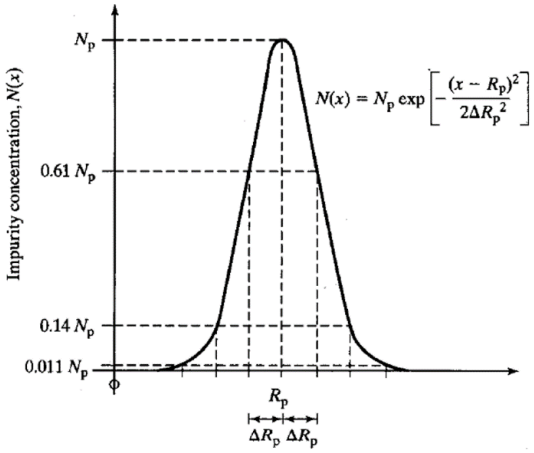
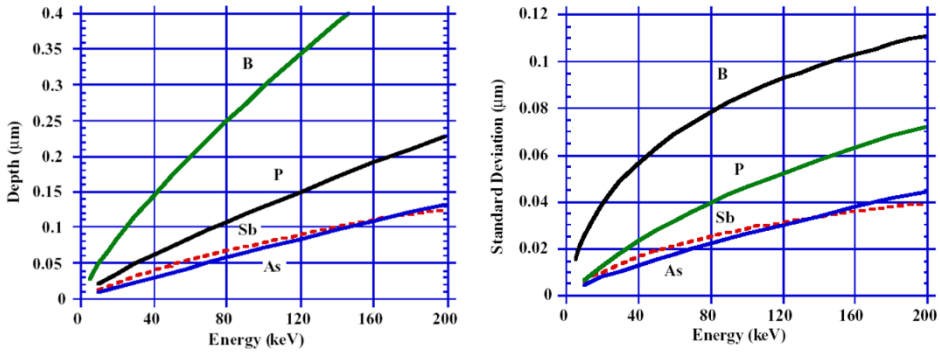


Figure 1.46. Schematic of the ion implantation process.

The implantation energy acts on the penetration depth of the ions, whose concentration can be described by means of a Gaussian function (see Figure 1.47).



(a)



(b) (c)

Figure 1.47. (a) Concentration profile of ion implantation. (b) Depth range vs. ion energy for four different dopant, i.e. B, P, Sb, As. (c) Standard deviation range vs. ion energy for four different dopant, i.e. B, P, Sb, As.

The high energy implantation generates structural crystalline damages. As consequence, a special treatment able to repair the damages is adopted. Such thermal treatment is called annealing and can be realized with two method: 1) with a tube furnace at low temperature (600-1000 ℃) to minimize the lateral dopant spreading; 2) on rapid thermal annealing, realized at high temperature but for a short time.

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Chapter 2

Termination structures

2.1 Introduction

The tendency of modern power devices is to reduce the overall size to favor the integration of several component on a single chip. Power devices employed in applications for motor drive or power distribution systems need to withstand high voltages, which are limited by the avalanche breakdown phenomenon. This last is governed by the electric field distribution within the semiconductor. Depending on the device design, the avalanche generation can occur either in active area or in termination area. The termination is designed to overcome the premature breakdown due to the curvature of the electrostatic potential and sustain the voltage rate of the device. With the increasing of the voltage rate, classical termination like FFR require a too large consumption of area leading to the necessity of developing new design solutions. Reliability and ruggedness are essential requirements for a termination, especially in application with high current rate. A deep compression of avalanche mechanisms occurring at the termination are needed to prevent premature causes of failure during the nominal condition. In this chapter two innovative termination design are presented and compared with a classical FFR one. The relation between the Negative Differential Resistance (NDR) branch on avalanche I-V curve and filamentary current is investigated in the interaction between active area and termination during Unclamped Inductive Switching test.

2.2 Edge termination techniques

In §1.5 the breakdown limitations occurring at the device periphery have been discussed. The influence of termination design like FFR, FP and JTE on the cylindrical electric field was also analyzed. Even if largely diffused, FFR structures assisted by FPs are difficult to fabricate and need of a too high occupation of area respect to the modern power devices requirements. On the other hand, JTE termination is demonstrated to be a good candidate in reducing the consumption of area but its main drawback is being too sensitive to process fluctuations. In this Chapter, advanced termination structures are presented for a power diode 1.2 kV rated provided for a leader company in the field of power semiconductor devices. In particular, two innovative JTE-based design are presented providing a well precise optimization strategy able to guarantee the correct operating even in presence of process fluctuations. Their performances are then compared with that of a FFR structure constitutes by seven guard-rings supported FPs. It will be demonstrated as the two JTE-based design can reach the same BV of a FFR structure with a reducing the occupation of area of over the 40%. Each structure is designed and analyzed by means of 2D TCAD simulations. The parameters optimization is led to maximize the BV at low current generation. Terminations ruggedness is evaluated by means of 2D electro-thermal simulations of UIS, deeply analyzing the problems associated to uneven current distribution. As regards the structures, in Figure 2.1 is shown the doping profile adopted for the simulations along the vertical dimension from Anode to Cathode.

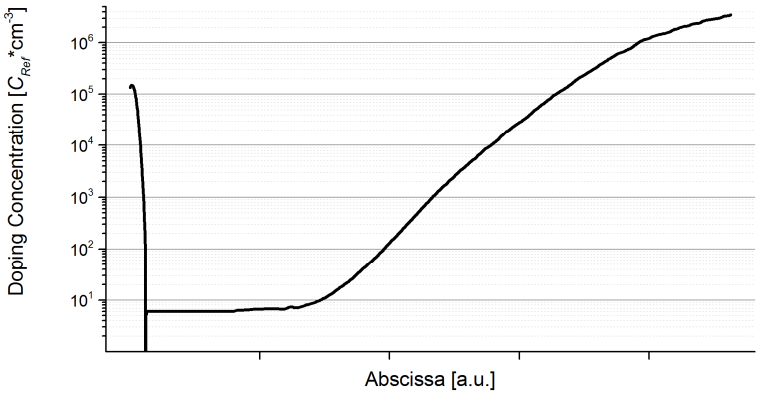


Figure 2.1. Doping profile of the overall structure.

Prior to proceed with the simulations, a preliminary calibration of the physical parameters has been made. In Table 2.1 are reported all the parameters modified by the calibration.

Table 2.1. List of calibrated model parameters.

Model	***Symbol***	***Default Value***	***Calibrated Value***
Dielectric constant	ε	11.7	11.8
Bandgap	*Chi0*	4.05	4.17
	Eg0	1.6964	1.8
	dEg0	-1.5958	0
Canali	*vsat0*	1.07×10^7	2.4×10^7
	vsat,exp,n	0.87	0.8
	vsat,exp,p	0.52	0.8
Scharfetter	τ_n	1×10^{-5} [s]	1×10^{-7} [s]
	τ_p	3×10^{-6} [s]	1×10^{-7} [s]
	N_{Ref}	5×10^{16} [cm^{-3}]	1×10^{16} [cm^{-3}]

In this work, it will refer at the “main junction” as a portion of the active area. As regards the design rules, two aspects must be taken into account. The first one regards the target on the maximum voltage. It is required to obtain a breakdown voltage capability higher than the 15% of the nominal one, hence, a value of about 1350V. The second one regards the space between the last diffusion of the termination and

the field stopper. Such distance (*S*) must guarantee a safety condition for which the depletion region cannot reach eventual cracks of the crystalline.

Finally, as avalanche generation model *Van Overstreaten-De Mann* has been adopted, and an oxide charge density of $3x10^{11}$ cm^{-2} at the Silicon/Oxide interface has been considered.

2.2.1 Floating field ring termination

The theory on FFR technique has been introduced in §1.5.1. During the years several approach for the design dimensioning have been developed [1]-[4]. The FPs to support the FFR design allows both to increase the BV and to improve the breakdown stability against the oxide contamination. The optimization of a structure FFR assisted by FPs can be uneasy since the dimensioning of a single guard ring or FP modifies the electric field distribution on each other element of the structure. In general, the employment of 5 guard-rings would be sufficient to reach the required voltage but two supplementary rings are here used to prevent eventual process fluctuations (Figure 2.2). The main junction and the floating rings are realized with the same process and both present a peak concentration of $1x10^{17}$ cm^{-3} with a junction depth of 6µm.

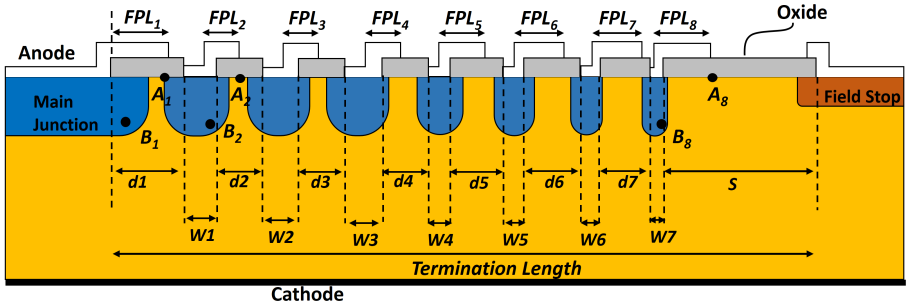


Figure 2.2. Sketch of FFR termination.

Referring to Figure 2.2, when the FPs are used the superficial electric field peaks on each guard ring is mitigated moving at the positions B-th. The FP itself introduces a peak at the point A-th. To optimize the geometries of the structure it is necessary to balance of the electric field peaks at the points A-th and B-th. In this work, a

particular optimization strategy has been adopted in order to prevent a lowering of the maximum BV in case of process variations, which has led to the superficial electric field peaks distribution depicted in Figure 2.3. It forms a sort of bell distribution with maximum peak in the center. This allows compensating eventual distribution variations due to process fluctuations. Its beneficial effect can be appreciate observing the relation between the oxide charge density and the BV reported in Figure 2.4. The redistribution of the electric field due to the lowering of the charge density brings to an increase of the BV.

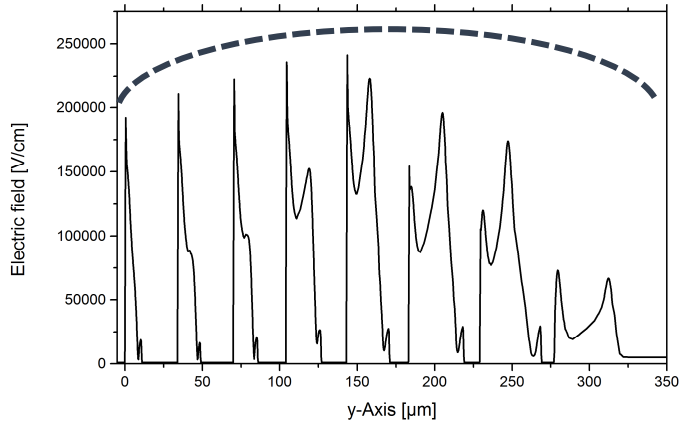


Figure 2.3. Superficial electric field distribution of the optimized FFR termination.

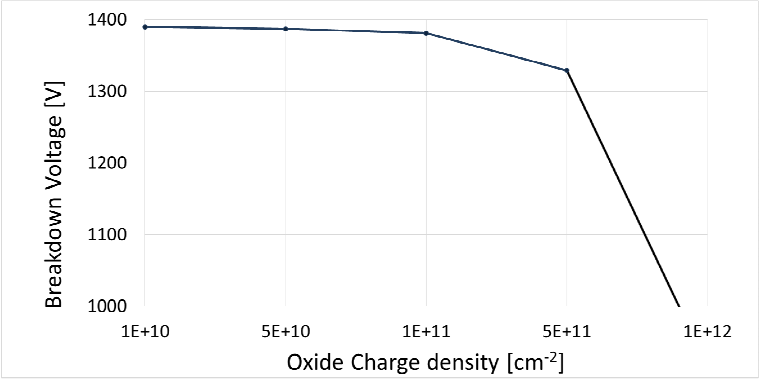


Figure 2.4. BV dependence on Si/Ox interface charge density for the optimized FFR termination.

2.2.2 JTE-based terminations

JTE technique has been discussed in §1.5.2. It pointed out as the main drawback was its breakdown instability in presence of process fluctuations. In this section two new design are proposed both thought to enlarge the range of peak doping of the P-diffusion (*JTE diffusion*) at which the breakdown stability is guaranteed. Such range is called in this work as *stability window*. The first one design is called SIPOS-JTE [31]-[9], and combines the action of the low doped P-diffusion and a high-resistive layer to linearize the potential along the termination; while the second one named Outer Guard-Assisted (OGA)-JTE [10] [11], exploits the actions of supplementary guard-rings to redistribute the electric field peak occurring at the low doped P-diffusion.

2.2.3 SIPOS-JTE termination

SIPOS-JTE structure is shown in Figure 2.5. The high-resistive layer has the dual role, on one hand reducing the superficial electric field peaks, and on the other hand screening the surface against external impurities.

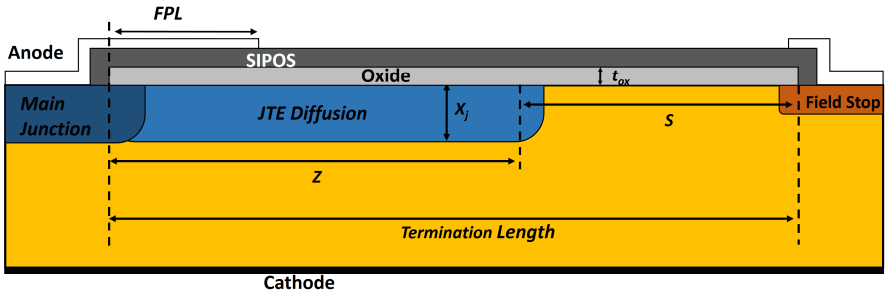


Figure 2.5. SIPOS-JTE geometry.

- **Design optimization**

In this section, the optimization procedure of SIPOS-JTE termination is presented for two values of JTE junction depths X_j at 6 and 8 µm.

Table 2.2 shows the list of parameters with respective range of values (imposed by design rules) needed to optimize the SIPOS-JTE structure.

Table 2.2. SIPOS-JTE parameters list and design rules.

Parameter	***Symbol***	***Range***
JTE Diffusion Length	*Z*	40-220 [µm]
Distance between JTE diffusions and field stop	*X*	0-5[µm]
Distance between JTE diffusions and field stop	*S*	100-280 [µm]
Oxide thickness	t_{ox}	1200-22000 [Å]
Field plate length	*FPL*	- [µm]
SIPOS Resistivity	ρ	$1x10^3$-$1x10^7$ [Ω·cm]
Termination length	*L*	250-300 [µm]

As first step, the dependence of BV on JTE diffusion extension *L* is evaluated for both junction depths (Figure 2.6). Such preliminary curves are achieved considering a distance *X* at 4 µm, t_{ox} at 1200 Å and in absence of the FP. In this phase, the influence of the JTE junction depth seems to be determinant in maximizing the BV, while the effect of *L* on BV tends to saturate after about 100 µm. The choice of *L* depends on three factor: the global termination length, the extension of the safety zone *S* and the distance *X* between the main junction and the JTE diffusion. Hence, the termination length can also be seen as the sum of three contributions *Z+X+S.*

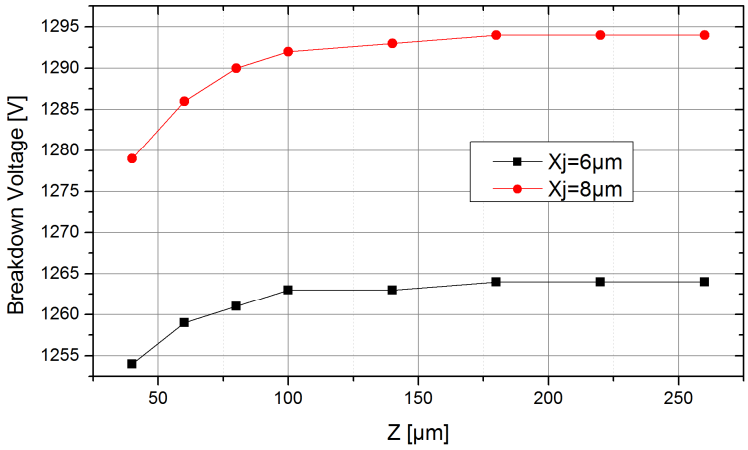
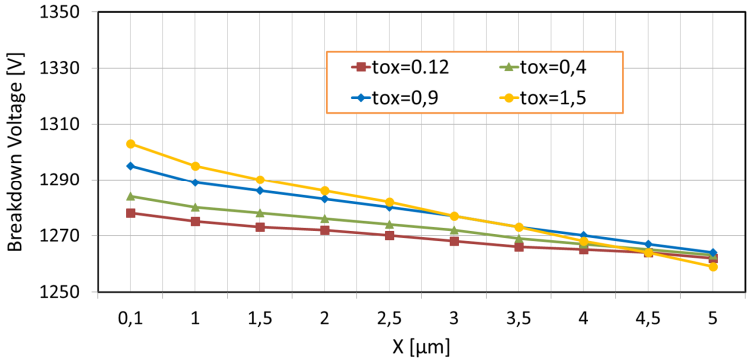


Figure 2.6. BV dependence on termination length Z for X_j at 6 and 8 µm, respectively.

The dependence of BV on X is now considered for different values of t_{ox} (Figure 2.7). X is the effective distance between the two junction edges including the lateral diffusion, which is adopted as the 85% of the vertical one. The BV is maximum when the JTE diffusion completely overlaps the main junction edge, in particular with the increasing of the oxide thickness. The action of the SIPOS layer in lowering the superficial electric field peaks is more effectiveness if the oxide thickness is reduced.

(a)



(b)

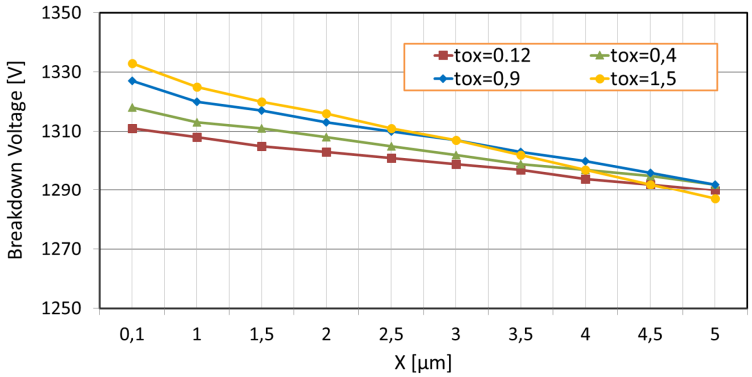
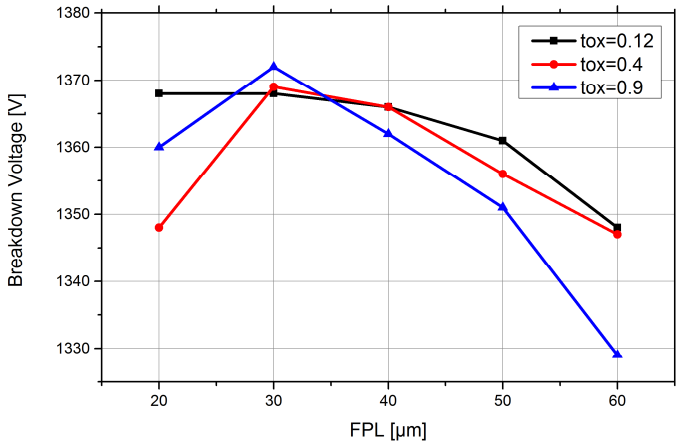


Figure 2.7. BV dependence on the distance *X* between the diffusions for different t_{ox}.

To lower the electric field peak occurring at the edge of the main junction the field plate is introduced extending the anode metallization along the termination for a length *FPL*. This last is dimensioned in dependence on the oxide thickness t_{ox}, JTE diffusion X_j junction depth and *L*. This latter will be chosen according to design rules to be as greater as possible. The effect of *FPL* on the BV is depicted in Figure 2.8 for different values of t_{ox}, fixing *L*=100 µm and *X*=0 µm.

(a)



(b)

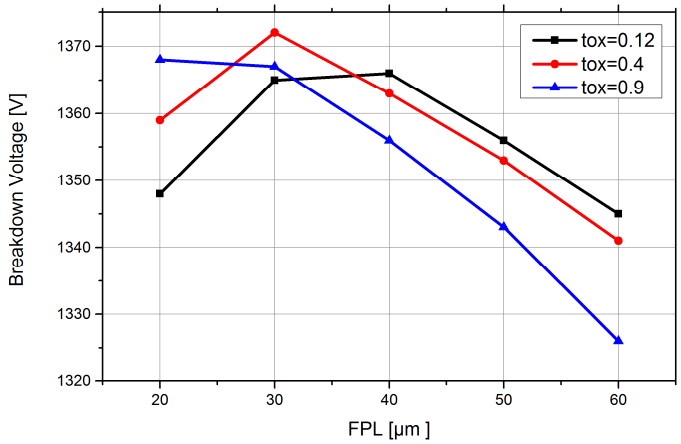
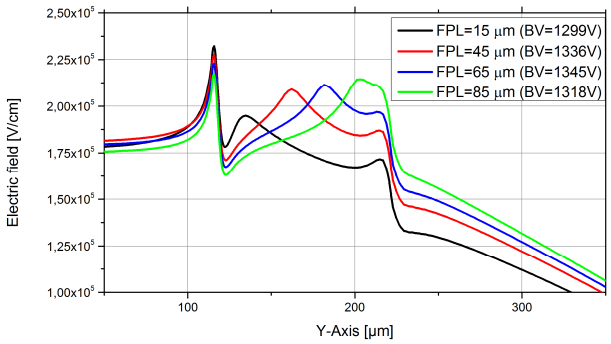


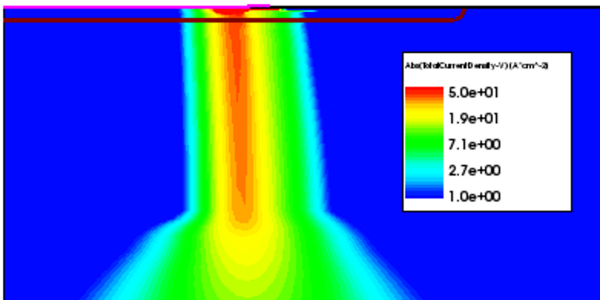
Figure 2.8. BV dependence on field plate length *FPL* for different t_{ox} with X_j = 6 µm (a) and X_j = 8 µm (b).

In Figure 2.9 the effect of the *FPL* on the electric field distribution along the termination is analyzed. It reveals the presence of two peaks placed at the edges of the main junction and the FP, respectively. With increasing of *FPL* the peak occurring at the FP becomes even more higher. It is interesting to note as the FP length (65 µm) that produces the maximum BV, also generates a main current path at the edge of the same FP Figure 2.9(c). Its effect on termination ruggedness will be treated in electro-thermal analysis.

(a)



(b)



(c)

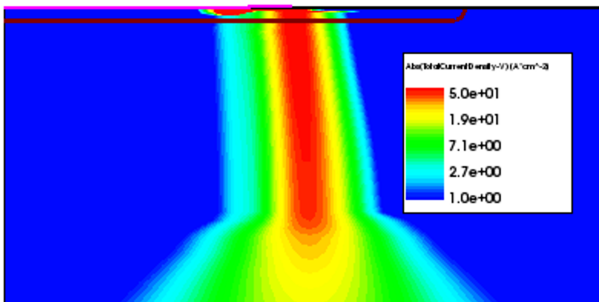
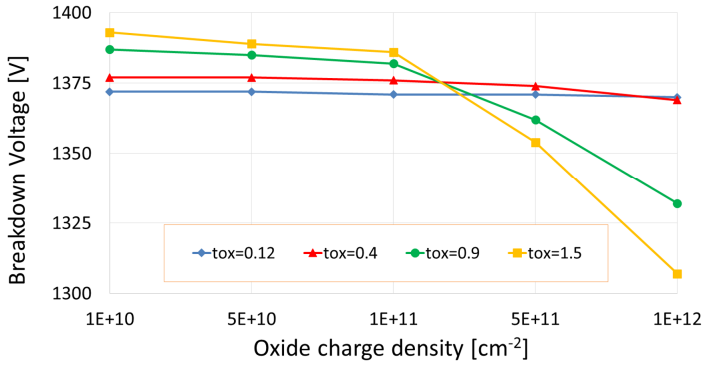


Figure 2.9. (a) Electric field distributions extracted at 5 μm from the surface for different lengths of the FP. Ionization distribution at I=1mA achieved with *FPL*=15 μm (b) and *FPL*=25 μm (c), respectively.

As introduced in §1.5.3, SIPOS layer has a beneficial influence against impurity entrapped in the oxide layer. This aspect is investigated evaluating the relation between oxide charge densities and BV for different values of t_{ox} as illustrated in Figure 2.10. It highlights as a thinner t_{ox} favors a higher rejection to the impurity. It points out as a good balance between a high enough BV and impurity rejection efficiency determines the choice of t_{ox} value. It is interesting to note as the increment of BV due to the t_{ox} growing produces its maximum effect with lowering the JTE junction depth.

(a)



(b)

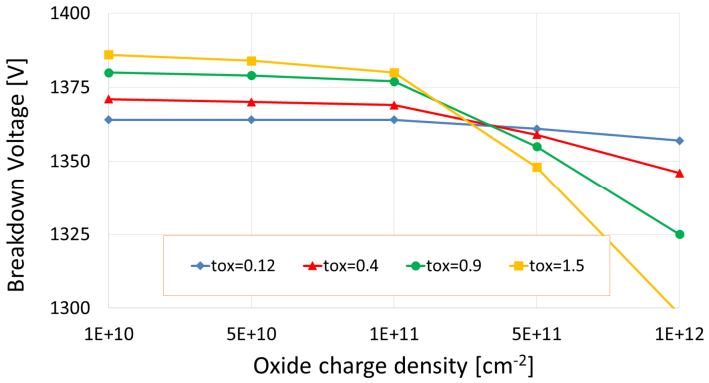


Figure 2.10. BV dependence on oxide charge density for X_j = 6µm (a) and 8µm (b).

One of the crucial aspect regarding the SIPOS layer is the control of its resistivity. A layer not adequately resistive will introduce an excess of leakage component, on the other hand, its screening effect on undesired charge is proportional to its conductivity. The effect of the layer resistivity on the leakage current is depicted in Figure 2.11. It is remembered that the resistivity of the SIPOS layer is managed acting on with both introducing dopant and controlling its dimension.

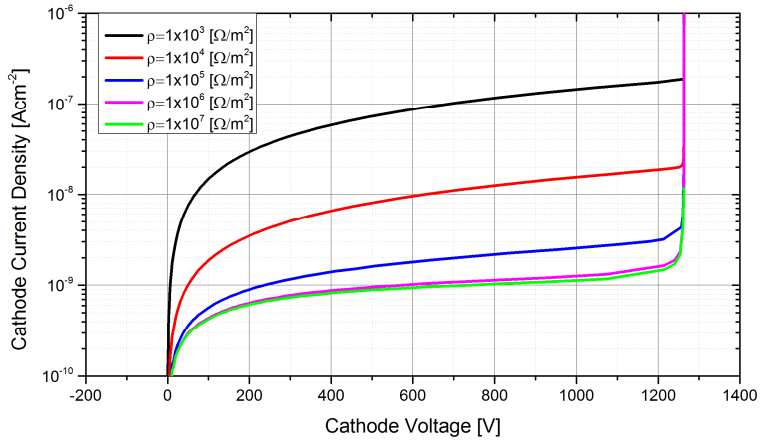


Figure 2.11. Termination leakage current dependence on SIPOS resistivity.

The *stability window* achieved at the end of the design optimization is reported in Figure 2.12. It is considerably enlarged respect to the case of a classical JTE structure.

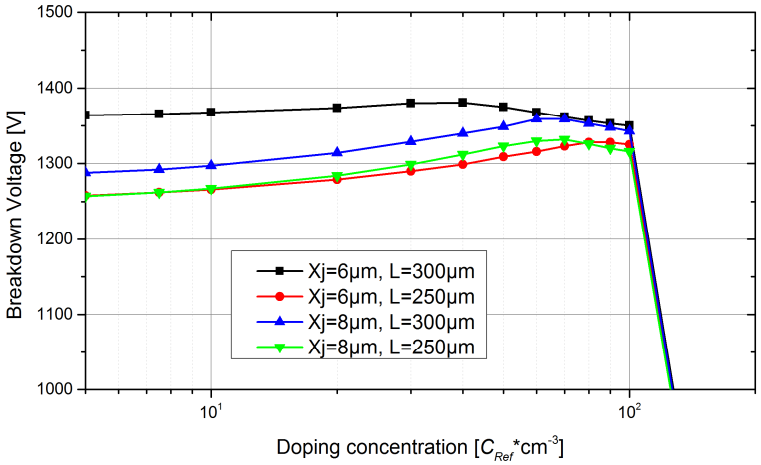


Figure 2.12. Stability windows of the SIPOS-JTE termination for X_j at 6 µm and 8 µm and for L of 250 µm and 300 µm.

The avalanche breakdown curves of the optimized SIPOS-JTE structure are shown in Figure 2.13. The cases of a termination length of 250 µm and 300 µm, as well as, the junction depths at 6 µm and 8 µm are considered. The difference on junction depth not introduces

significant effects in term of BV; while increasing the termination length of 50 µm generates an increment of about 30 V of the BV.

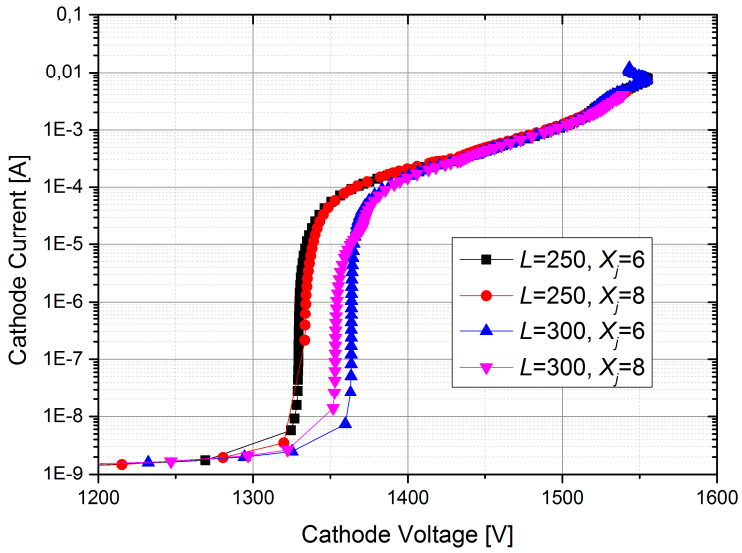


Figure 2.13. Avalanche I-V curve of the optimized SIPOS-JTE termination in different combination of the parameters termination length and junction depth.

2.2.4 OGA-JTE termination

The sketch of OGA-JTE termination is shown in Figure 2.14. The work of the JTE diffusion to sustain the high electric field is helped by a series of guard-rings located in the outer part of the structure. In this structure the outer rings have the same role performed for the FFR termination, with the difference that here they contribute to redistribute the electric field peak at the edge of JTE diffusion instead of the main junction. If the implantation and diffusion process produce a JTE peak doping too high respect to the expected value, the high electric field is located at the edge of the JTE diffusion. In this case, the outer rings help redistributing such peak increasing the BV. On the other hand, when the JTE doping concentration is too low the electric field peak at the edge of the main junction is aided by the FP action. As regards the outer rings width, a unique value of 10µm has been chosen for each ring; while for the optimization of their distances the

methodology reported in art. [4] has been adopted. The latter is based on an iterative approach able to balance, at each step, the electric field peak occurring on each junction. At the start, every ring distance is kept at the minimum, so that the high electric field just occurs on outer ring. Moving the distance between the last ring and the previous one, it is possible balancing the two peaks at the rings edge. The potential of the internal rings is coupled with that of the main junction and does not affect the external rings since it is kept constant. Iterating the procedure for every distance, the electric field peak will be evenly distributed between each ring and the main junction.

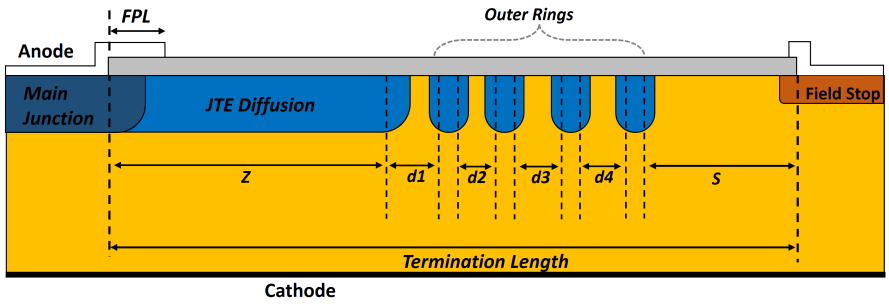


Figure 2.14. Geometry of GA-JTE termination.

In order to reduce the number of masks (hence the costs), it is possible to realize the outer ring diffusions by using the same technological process of the anode junction (*Case1*) or the same of the JTE diffusion (*Case2*). The results of both approaches are reported in **Figure 2.15**. *Case1* allows a wider *stability window* and offering also a further benefit since it results less sensible respect to eventual variations of the ring distances.

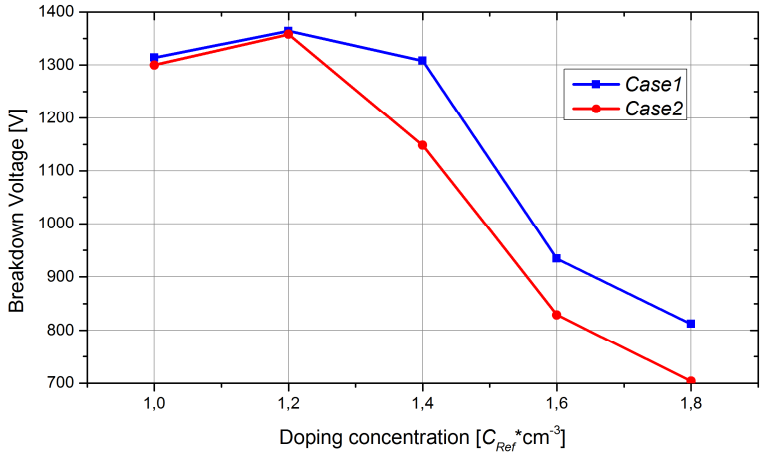
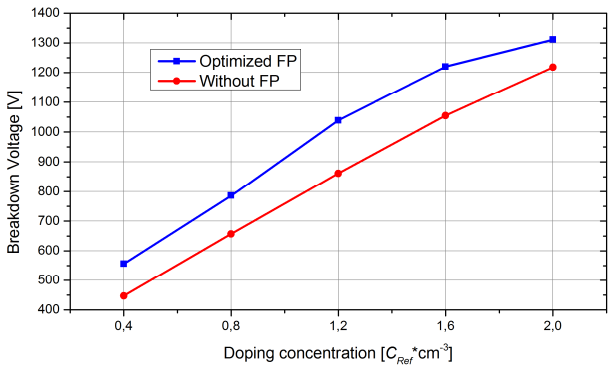


Figure 2.15. BV as a function of JTE peak concentration when the outer rings have the same technology of the JTE diffusion (*Case1*) or the same of Anode diffusion (*Case2*).

- ***Design optimization***

FP optimization contributes to improve the *stability window* in the range of low values of *JTE diffusion* peak doping (see **Figure 2.16**(a)). An eventual fluctuation respect to the optimal length would not significantly impacts on BV capability as visible in **Figure 2.16**(b). The example refers to a case with X_j = 6µm, but analogous results are achieved for X_j = 8µm.
As regards the rings optimization, it is led following the procedure described in [4]. It needs a prior knowing of the electrostatic potential at the main junction side. For this reason, the field plate length (*FPL*) optimization must be the first step to perform. *FPL* dimensioning modifies the potential distribution at the edge between the JTE diffusion and the main junction contributing to lower the electric field peak.

(a)



(b)

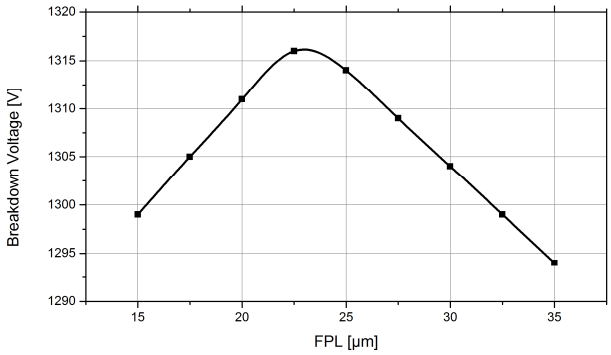


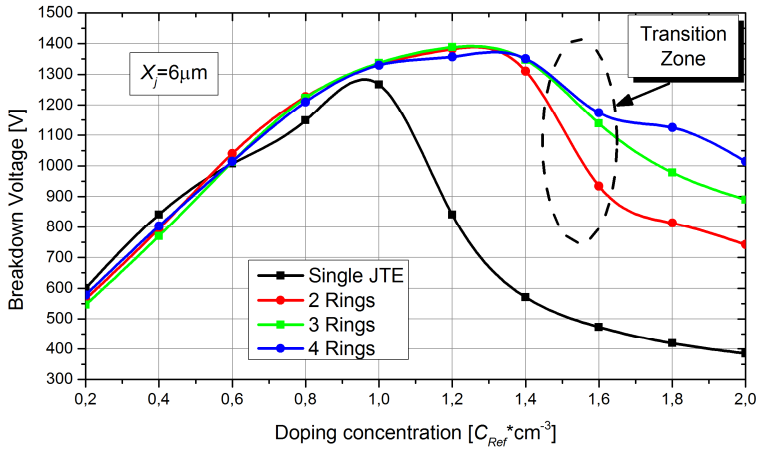
Figure 2.16. (a) Stability window for low values of the JTE doping peak in OGA-JTE termination with an optimized FP (red line) and without FP (blue line); (b) BV dependence on field plate length.

The extension of the JTE diffusion (*Z)* is kept as larger as possible taking into account the space occupied by the outer ring (depending on their number) and the minimum length *S* of safety zone. The design rule on *S* imposes a dimension not lower than 100 µm.

It is now considered the influence of the number of outer rings on the *stability window* (see Figure 2.17) for the optimized termination. The effect of two, three or four outer rings have been considered and compared to the case of the classical JTE. Observing the results achieved for X_j at 6µm and 8µm, this latter shows a narrower *stability window*. In addition, the termination working is more effectiveness with increasing the number of outer rings. Nevertheless, for both junction depths, the stability window appears limited by “transition zone” where the BV drops of over 100V independently of the amount

of rings adopted. Such lessening of the BV is due to an abrupt changing in electric field distribution. It can be comprehended observing Figure 2.18 where the superficial electric field distributions are depicted when *JTE diffusion* peak concentration is optimal, too low, or too high for an optimized termination having four outer rings. With a too low peak, the distribution (green-line) is completely unbalanced close to the main junction and the electric field peak is placed in correspondence of the FP edge. If the peak doping is too high, the JTE diffusion edge and the outer rings (red-line) sustain the high electric field. Finally, with an optimal peak doping, the whole termination is working to sustain the electric field peaks (blue-line). It is clear that when the peak concentration exceeds from its optimal value the electric field peaks tend to be prevalently sustained by external part of the termination. The "transition zone" takes place due to an abrupt passage of the electric field distribution occurring at the optimal case (blue-line) to that of a too high peak doping (red line).

(a)



(b)

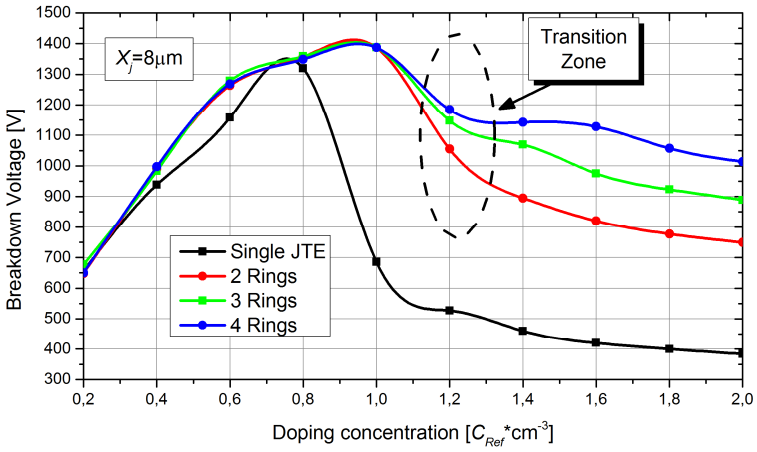


Figure 2.17. Stability window of OGA-JTE termination when 2 (green line), 3 (blue line) or 4 (red line) outer rings are adopted compared to that of simple JTE termination for *Xj*= 6 µm (a) and *Xj*= 8 (b) µm, respectively.

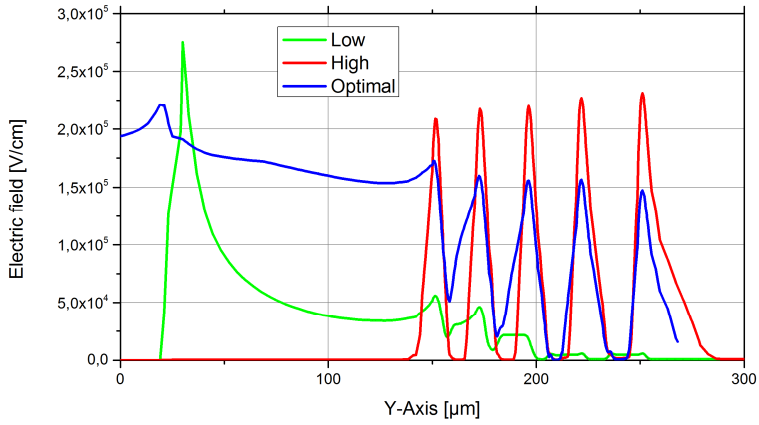
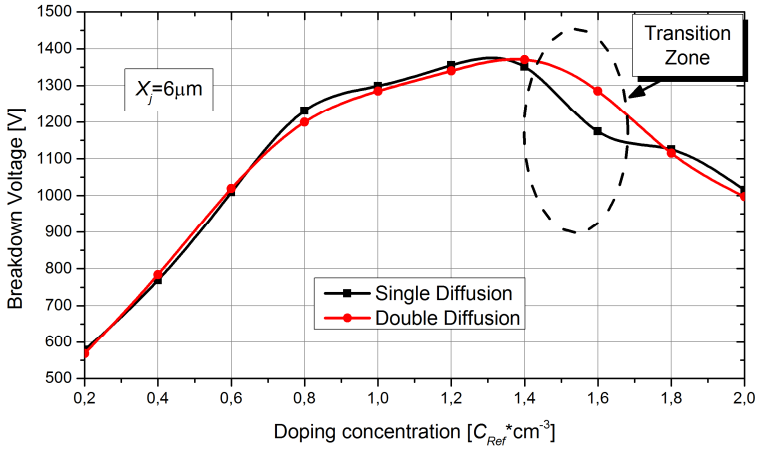


Figure 2.18. The surface electric field distribution when the JTE peak profile is too low (green line), optimal (red line) and too high (blue line).

To favor a more gradual passage of the high electric field toward the external place the multi-mask approach [31] discussed in §1.5.1 is adopted. Just dividing the JTE diffusion in two diffusions having length of L1 = 90µm and L2 = 50µm, respectively, and peak concentration of C1= C_{opt} and C2= 0.95·C_{opt}, respectively, a wider stability widow can be achieved (Figure 2.19).

(a)



(b)

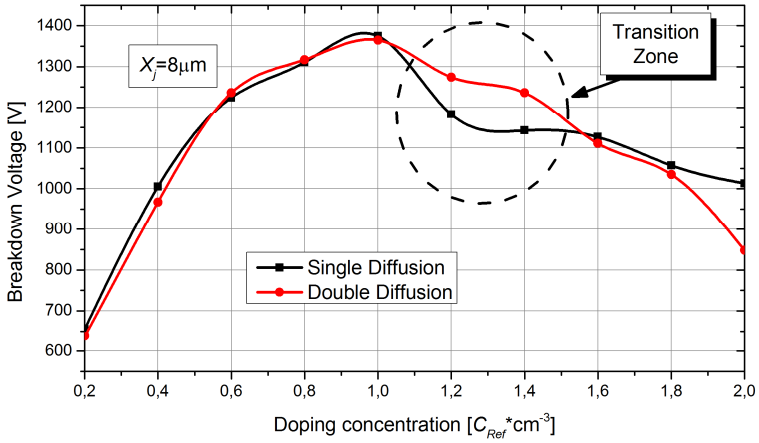


Figure 2.19. Stability window of OGA-JTE termination realized with a unique JTE diffusion (circle markers) and two JTE diffusions (triangle markers) for X_j = 6 µm (a) and X_j = 8µm (b), respectively.

The rejection capacitance against Si/Ox interface impurity is now analyzed. Figure 2.20 shows the BV of the optimized termination as function of oxide charge density variations. For X_j = 6µm the BV is always over the voltage rate, keeping a high values in a wide range oxide charge densities. On the other hand, a strong degradation of BV occurs for X_j=8 µm.

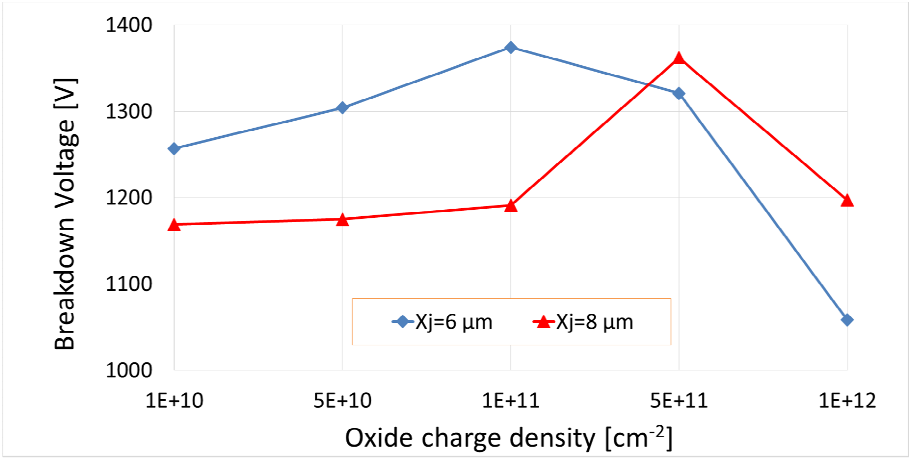


Figure 2.20. BV dependence on oxide charge density of an optimized OGA-JTE termination for X_j = 6µm (blue line) and X_j = 8µm (red line).

As highlighted in Figure 2.21, lowering the oxide charge density has the analogous effect of increasing the JTE peak doping, with unbalancing the electric field distribution toward the external area of the termination. This effect is particularly sensitive for deeper junction depths compromising the correct operating of the termination.

(a)

(b)

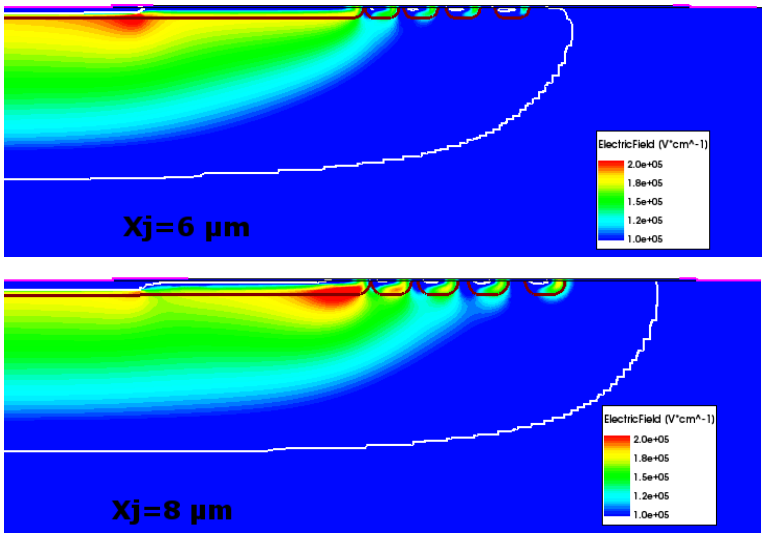


Figure 2.21. Electric field distribution in avalanche condition at I = 1mA with an oxide charge density of 1x10^{10} cm^{-2} for X_j=6 µm (a) and X_j=8 µm

(b), respectively.

The structure realized with junction depth of 8 µm exhibits limitations in term of both stability window and impurity rejection. This suggests of adopting doping profiles with junction depth at 6 µm. On the other hand, the implantation and diffusion process of low-doped junction is easier to realize in case of reduced junction depth.

- ***High current analysis***

Avalanche breakdown analysis is here performed comparing the current density distribution at low (I=1mA) and high (I=10A) value of generated current with isothermal simulations, in particular, considering the three cases for *JTE diffusion* peak doping: optimal, too low and too high. The structure is optimized with three rings but analogous behaviors can be achieved for two or four outer rings. Figure 2.22 shows the avalanche breakdown curves referring to the three cases highlighting as at high current the structure operates in Positive Differential Region (PDR).

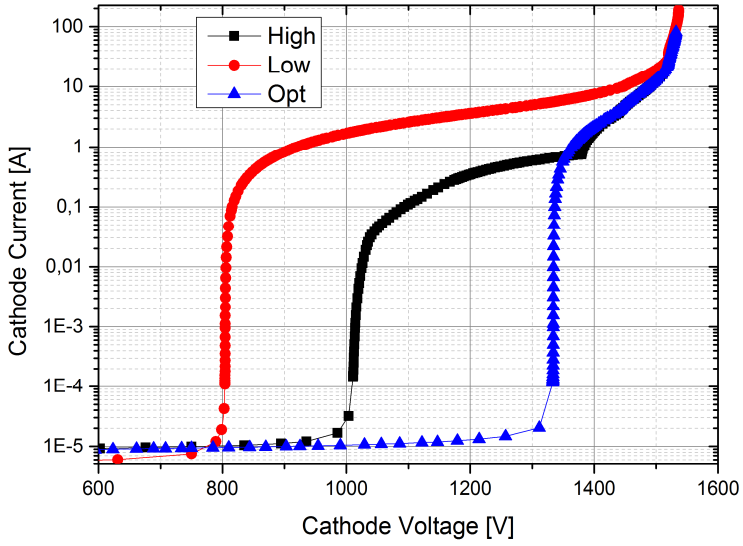


Figure 2.22. Avalanche breakdown curves of OGA-JTE termination for "optimal" (blue line), too "low" (red line) and too "high" (black line) JTE doping concentration.

Starting from the optimal case, a dominant current contribution appears in Figure 2.23 due to ionization occurring at both the edge of the main junction and the edge of the FP. At high current, the contribution at the main junction becomes dominant and second path in active area is generating.

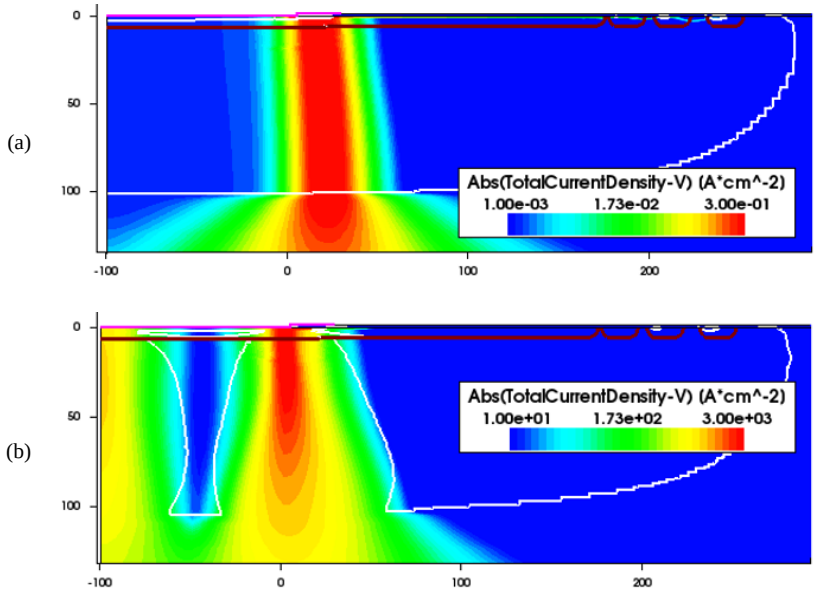


Figure 2.23. Avalanche breakdown current density distribution for I=1mA (a) and for I= 10A (b) for the structure having **optimal** peak doping.

When the peak doping is too low (Figure 2.24), the depletion region is not well extended along the whole termination and the main ionization contribution, at low current, starts from the edge of the FP. Even at high current, the generated contribution continues of being essentially located between main junction and FP edges.

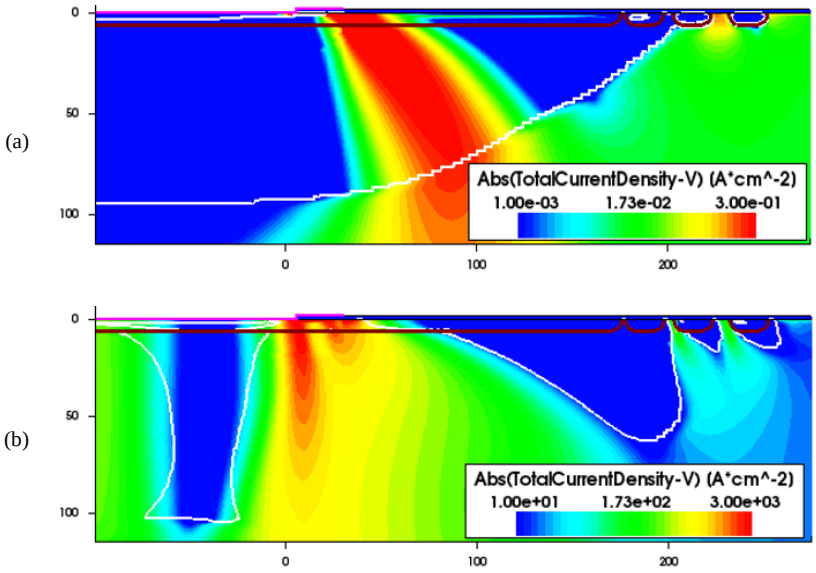
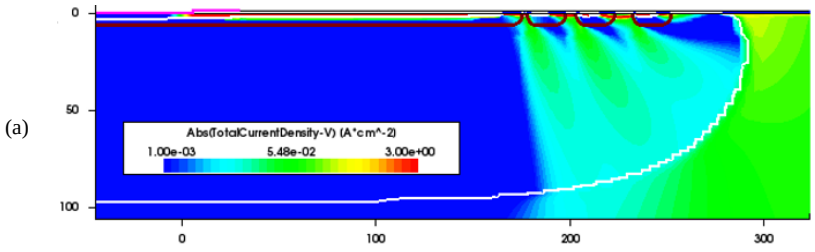


Figure 2.24. Avalanche breakdown current density distribution for I=1mA (a) and for I= 10A (b) for the structure having too **low** peak doping.

Finally, the too high peak case is considered (Figure 2.25). At low current different paths are generated between the JTE diffusion edge and the outer rings. Such paths continue to be present also at high current, even if they are generated a main contribution at the main junction edge and second contribution in active area. The generation of several current paths should favor a better thermal distribution, but this aspect will be treated in the section regarding the electro-thermal analysis.



(b)

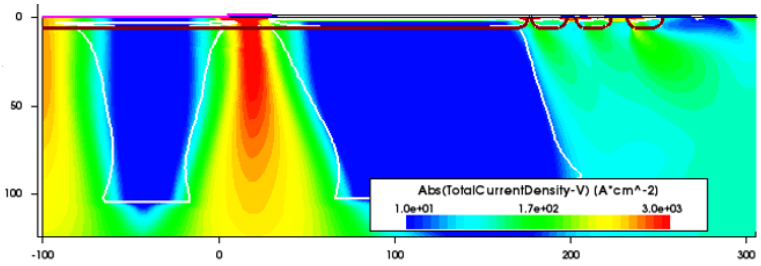


Figure 2.25. Avalanche breakdown current density distribution for I=1mA (a) and for I= 10A (b) for the structure having too **high** peak doping.

2.2.5 Termination performances comparison

In Table 2.3 are compared both the avalanche breakdown capabilities and the oxide charge rejection capacitances of each termination. It points out as the two JTE-based terminations are capable to reach the required BV with strong reduction in term of consumption of area respect to the FFR one. No particular benefits deriving from adopting a deeper junction depth. SIPOS-JTE technology guarantees better performances both in term occupation of area and in term of stability respect to process fluctuations.

Table 2.3. Termination performances comparison

Design	***Length* [µm]**	***Xj* [µm]**	***Oxide charge rejection***	***BV* [V]**
FFR	500	6	↗	1358
FFR	500	8	↗	1401
SIPOS-JTE	250	6	↑	1328
SIPOS-JTE	250	8	↑	1332
SIPOS-JTE	300	6	↑	1381
SIPOS-JTE	300	8	↑	1359
OGA-JTE	400	6	→	1371
OGA-JTE	400	8	→	1360

2.3 Unclamped Inductive Switching test

One of the important characterization tool used in avalanche ruggedness validation of power devices is the Unclamped Inductive Switching (UIS) test [12]-[16]. It allows determining the maximum amount of avalanche energy sustainable by a device when an inverse current is forced through it. In general, the concept of ruggedness for a device is associated to the amount of energy that can be absorbed prior to device failure [17]. The limit imposed by the maximum energy is related to physical and structural device parameters, furthermore, it is strictly affected by electro-thermal effects within the device [18]. The interaction of all these elements can lead to inhomogeneous current distributions on the device area, and in case of positive feedback, a consequent filamentary current [19], [20].

A simplest circuit useful to describe how performing the UIS test is depicted in **Figure 2.26**. An inductive load L is unclamped due to the absence of a free-wheeling diode. The driver signal of the DUT is pulsed for a duration of T_{ON}, during the which, the current through the device increases linearly with a slope given by:

$$\frac{di_C}{dt} = \frac{V_{CC}}{L} \tag{2.1}$$

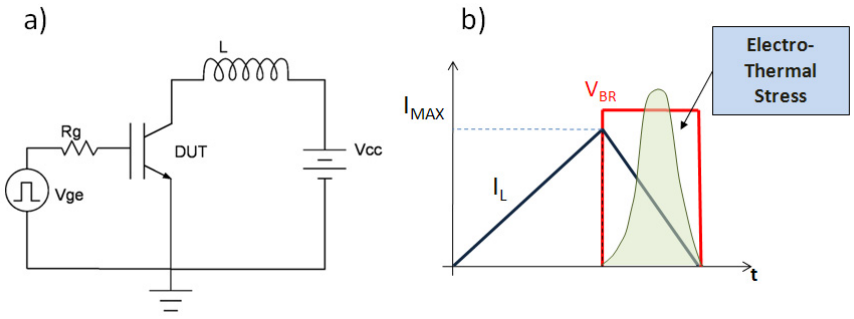


Figure 2.26. (a) UIS simplest test circuit. (b) Typical UIS waveforms.

After the pulse time T_{ON} the current reaches its maximum value I_{MAX} and the device is turned-off, forced by the inductor in breakdown

condition. In this phase, the current decreases linearly but with a different slope given by:

$$\frac{di_C}{dt} = \frac{(V_{BR} - V_{CC})}{L} \tag{2.2}$$

where V_{BR} is the dynamic BV. Since the whole energy stored in the inductor must be dissipated on the active device, neglecting the Joule effect dissipation on all parasitic resistance, such energy can be described as:

$$E = \frac{1}{2} L I_{MAX}^2 \frac{V_{BR}}{V_{BR} - V_{CC}} \tag{2.3}$$

During the inductor discharging time, the power dissipation reaches its maximum value when the avalanche transient starts arriving to zero when it finish. On the other hand, the junction temperature reaches its maximum value somewhere during the UIS time and the two peaks do not overlap making impossible determining the instant of maximum stress. However, since the electro-thermal stress strongly depends on the inductor value, if a thin inductance value is used, the discharge phase rapidly leads to a high electrical stress while the temperature does not approach a critical value. Otherwise, if a high inductance value is employed, the time to discharge all the energy is too long causing a critical rise of the device temperature and a subsequent high thermal stress.

T_{ON} and T_{OFF} can be extracted assuming the triangular shape of the current.

During the turn-on:

$$\frac{di_C}{dt} = \frac{V_{DD}}{L} \Rightarrow I_{C,\max} = \frac{V_{DD}}{L} T_{ON} \tag{2.4}$$

During the turn-off:

$$\frac{di_C}{dt} = -\frac{V_{BR} - V_{DD}}{L} \Rightarrow T_{OFF} = \frac{L I_{C,\max}}{V_{BR} - V_{DD}} \tag{2.5}$$

2.3.1 UIS simulation strategy

To evaluate the avalanche ruggedness of the two terminations optimized in §2.2, 2D TCAD electro-thermal simulations of UIS have been performed under different operative conditions. In addition, the influence of the main design parameters on the avalanche energy capability has been evaluated. During such overstress condition, the interaction between a portion of active area and the termination is also analyzed.

Electro-thermal simulations usually require a considerable computational time, especially for structures having a great amount of mesh nodes as for the terminations. To reduce the time of simulation, a simplified version of the UIS test circuit has been adopted. Referring to a real case, the UIS T_{ON} time is needed to charge the inductor at a desired current value, which will flow into the DUT during the T_{OFF} period. Since the DUT is in off condition during the T_{ON} period and electro-thermal phenomena are negligible, from the simulative point of view, the T_{ON} phase can be simplified. Therefore, the UIS turn-off dynamic of the DUT can be simulated using the equivalent circuit of Figure 2.27. The DUT is connected in mixed-mode to a "current source" appropriately set to replicate the decreasing triangular shape of the current flowing from the inductor.

During the UIS transitory a continuous interplay between active area and termination can occur. Because of the scope of this analysis is to investigate on eventual problem that can affect the termination ruggedness, the avalanche behavior at only two time instants are considered (see Figure 2.28): the first one **t1**, at the starting of T_{OFF} (when collector voltage is stabilized); while the second one **t2**, when the failure occurs. During the UIS a certain amount of energy is transferred by the inductor to the DUT with consequent temperature increasing of this last. Self-heating effects can produce the generation of electron-hole pairs with a generation rate potentially uncontrollable if the local temperature overcomes a threshold of 700K [21][22]. Such temperature has been considered as the threshold value to determine the failure condition during the simulation.

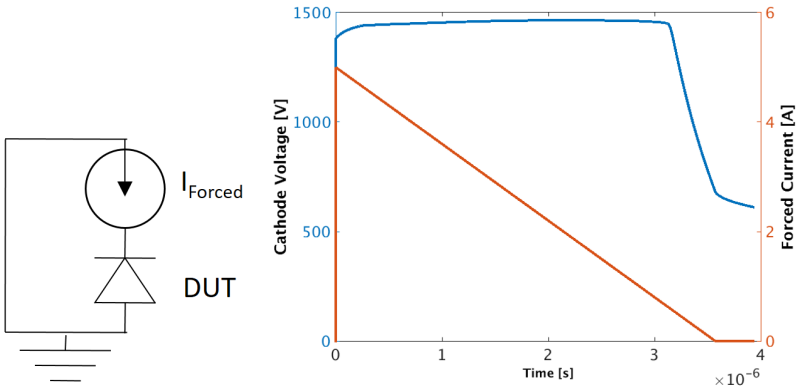


Figure 2.27. Equivalent circuit and deriving waveforms used to perform UIS simulations.

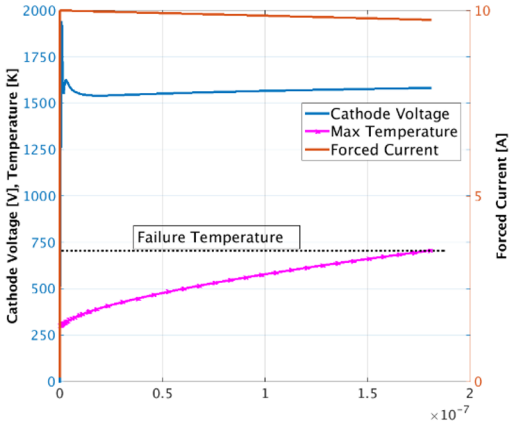


Figure 2.28. Waveforms example during the UIS turn-off. The waveforms are only partial due to the overcoming of the failure condition at time t2. At t1 the voltage oscillation are already terminated and the current is still at low levels.

The simulation T_{OFF} time is regulated to generate a maximum current of 10 and 25 A, respectively, according to eq.(2.5). Three inductance values at 1, 40 and 100 mH, respectively, are adopted. These values of current and inductance will be also used for the experimental analysis.

2.3.2 SIPOS-JTE UIS simulations

Simulation results of SIPOS-JTE termination are resumed in Table 2.4. Avalanche energy capability is evaluated for two values of Anode peak doping at $1x10^{17}$ and $1x10^{16}$ cm^{-3}, respectively. This latter is adopted as worst case to evaluate the possibility that the metal-silicon contact not is completely resistive. Also the termination is evaluated in two optimized configurations having length of 250 and 300 µm, respectively, as well as, two values of doping depths at 6 and 8 µm, respectively. Results highlight values of avalanche energy capability particularly lower for some design configurations. The device behavior during such operative conditions have been analyzed resulting in two types of criticalities: the first one (marked on table with red color) related to current crowding problems depending on the field plate dimensioning; while the second one (green marked) is associated to a reach-through phenomenon occurring at the anode contact.

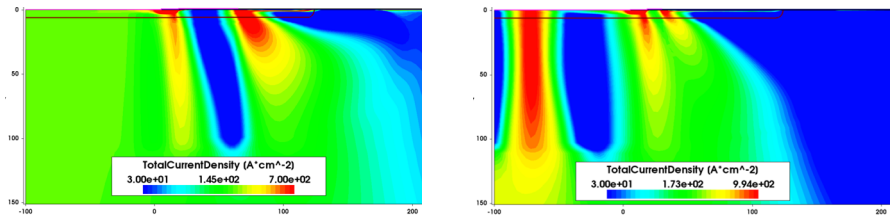
Table 2.4. UIS simulations results for the SIPOS-JTE termination.

Anode Peak [cm^{-3}]	Terminanation Length [µm]	X_j [µm]	Ipeak = 10A			Ipeak = 25A		
			L = 1mH [mJ]	L =40mH [mJ]	L = 100mH [mJ]	L = 1mH [mJ]	L =40mH [mJ]	L = 100mH [mJ]
$1x10^{16}$	250	6	8,5	7,7	7,5	0,65	0,64	0,64
		8	7,2	6,5	6,5	0,65	0,65	0,65
	300	6	5,2	4,8	4,8	0,7	0,7	0,7
		8	13,1	10,8	10,7	0,7	0,7	0,7
$1x10^{17}$	250	6	53,4	49,7	49,7	39,5	39,4	39,5
		8	59,3*	55,8	55,9	41,3	41,8	41,9
	300	6	3,8	3,1	3,8	5,8	5,9	5,9
		8	59,6*	57,3	57,5	37,6	37,6	37,5

* Failure condition NOT occurred

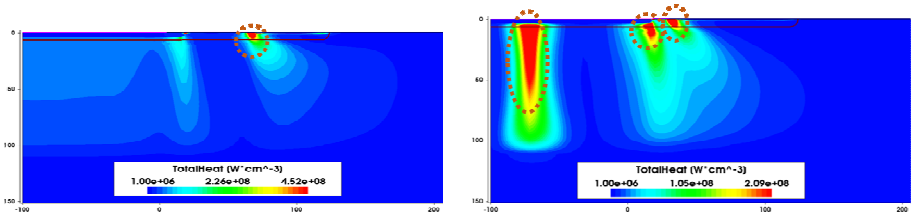
To understand the criticality related the extension of the FP, the current density distributions at the failure moment are considered for two different values of *FPL* at 45 µm and 15 µm (Figure 2.29). Both structures have the same design except for the field plate length. The example refers to a UIS simulation realized with I_{max}=5A, L=100mH, for a termination of length 300 µm with X_j=6 µm. As anticipated in §2.2.2.1 by isothermal simulations, the electric field peak at the FP edge becomes even more dominant with the increasing of *FPL*. In

particular, the value of *FPL* able to produce the higher breakdown capability also generated a dominant current contribution at the FP edge. As depicted in Figure 2.29(a), during the UIS transitory the thermal dynamic is too slow respect to the electrical one, and the failure condition takes place before the ionization contribution can move from its location. With a reduced *FPL*, the two electric field peaks at the main junction and at the FP are evenly distributed. In this condition, the electro-thermal interaction allows the movement of the generated current toward the active area favoring a better distribution of the power dissipation (Figure 2.30).



(a) (b)

Figure 2.29. Current density distribution during UIS simulation at the failure condition for two optimized structure having FPL of 45 µm (a) and 15 µm (b), respectively.



(c) (d)

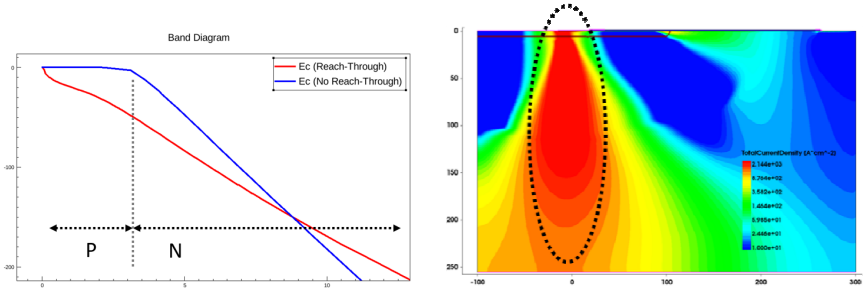
Figure 2.30. Total heat flow distribution during UIS simulation at the failure condition for two optimized structure having FPL of 45 µm (a) and 15 µm (b), respectively.

The optimized structure with *FPL*=15 µm allows solving the analyzed criticality resulting in a considerable increment of the UIS energy capability. Results are reported in Table 2.5, the improved design presents diminution of the BV of 40V, which is still in the range of the acceptable values.

Table 2.5. UIS simulation results of the improved SIPOS-JTE structure.

	Anode Peak [cm-3]	Terminanation Length [µm]	Xj [µm]	Ipeak = 10A			Ipeak = 25A		
				L = 1mH [mJ]	L =40mH [mJ]	L = 100mH [mJ]	L = 1mH [mJ]	L =40mH [mJ]	L = 100mH [mJ]
NEW	$1x10^{17}$	300	6	60,5*	52,9	52,8	41,5	41,8	41,8
OLD	$1x10^{17}$	300	6	3,8	3,1	3,8	5,8	5,9	5,9

It is now analyzed the second criticality underlined in Table 2.4. It is related to reach-through phenomenon occurring at the anode contact under high current levels. If the anode peak doping is too low (in this case $1x10^{16}$ cm^{-3}), the carriers concentration can dramatically modify the band structure (see Figure 2.31a), bringing to a sort of short-circuit condition, as visible in Figure 2.31b.



(a) (b)

Figure 2.31. (a) Conduction bands at the P-Anode N-Drift junction when a reach-through phenomenon occurs (red line) and not occurs (blue line). (b) Total current density distribution in presence of reach-through phenomenon.

2.3.3 OGA-JTE simulations

UIS 2D electro-thermal simulations are performed on OGA-JTE termination evaluating, in analogy with isothermal studies, the behavior when the peak doping of JTE diffusion is *optimal* or too *low* or too *high*. Results are listed in Table 2.6, where red marks are highlighted two critical case in term of energy capability. They are related to reach-through phenomenon, as already discussed in the previous section.

Table 2.6. UIS simulation results for the optimized OGA-JTE termination with four rings.

Anode Peak [cm^{-3}]	JTE Peak [cm^{-3}]	X_j [µm]	Ipeak = 10A		Ipeak = 25A	
			L = 1mH	L = 100mH	L = 1mH	L = 100mH
$1x10^{16}$	$6x10^{15}$	6	En = **35,7** [mJ]	En = **31,0** [mJ]	En = **4,5** [mJ]	En = **4,5** [mJ]
	$5x10^{15}$	8	En = **44,9** [mJ]	En = **42,1** [mJ]	En = **34,7** [mJ]	En = **35,7** [mJ]
$1x10^{17}$	$6x10^{15}$	6	En = **43,6** [mJ]	En = **49,8** [mJ]	En = **45,6** [mJ]	En = **47,4** [mJ]
	$5x10^{15}$	8	En = **52,8** [mJ]	En = **51,6** [mJ]	En = **54,0** [mJ]	En = **44,2** [mJ]
$1x10^{16}$	$2x10^{15}$	6	En = **10,1** [mJ]	En = **9,1** [mJ]	En = **4,5** [mJ]	En = **4,5** [mJ]
	$2x10^{15}$	8	En = **27,7** [mJ]	En = **22,1** [mJ]	En = **48,2** [mJ]	En = **47,8** [mJ]
$1x10^{17}$	$2x10^{15}$	6	En = **8,8** [mJ]	En = **8,6** [mJ]	En = **14,7** [mJ]	En = **14,8** [mJ]
	$2x10^{15}$	8	En = **18,7** [mJ]	En = **19,0** [mJ]	En = **25,4** [mJ]	En = **25,6** [mJ]
$1x10^{16}$	$1x10^{16}$	6	En = **45,9** [mJ]	En = **39,9** [mJ]	En = **29,3** [mJ]	En = **29,9** [mJ]
	$1x10^{16}$	8	En = **62,9*** [mJ]	En = **49,3** [mJ]	En = **44,4** [mJ]	En = **44,9** [mJ]
$1x10^{17}$	$1x10^{16}$	6	En = **59,3** [mJ]	En = **60,4** [mJ]	En = **29,8** [mJ]	En = **37,3** [mJ]
	$1x10^{16}$	8	En = **63,3*** [mJ]	En = **68,1** [mJ]	En = **50,7** [mJ]	En = **51,9** [mJ]

* Failure condition NOT occurred

Starting from the *optimal* JTE peak doping, the current density distributions at the times t1 and t2 are shown in Figure 2.32. At t1 it is visible as several current paths are generated, even if the main contribution is located at the main junction edge. During the transient there is a continuous movement of current between active area and termination. Because of the self-heating effect, the generation of current tends to stabilize at the edge of the main junction bringing to the device failure (Figure 2.32(b)).

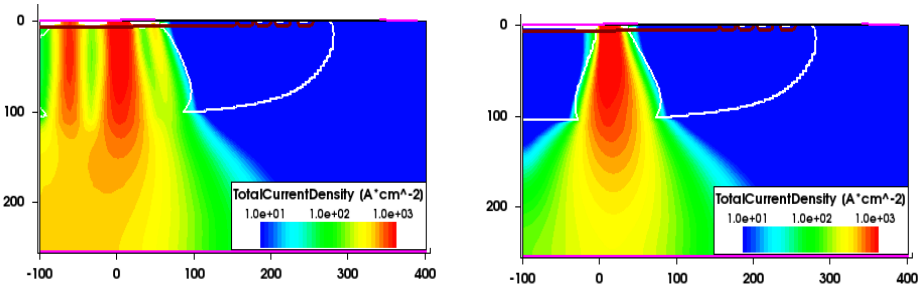
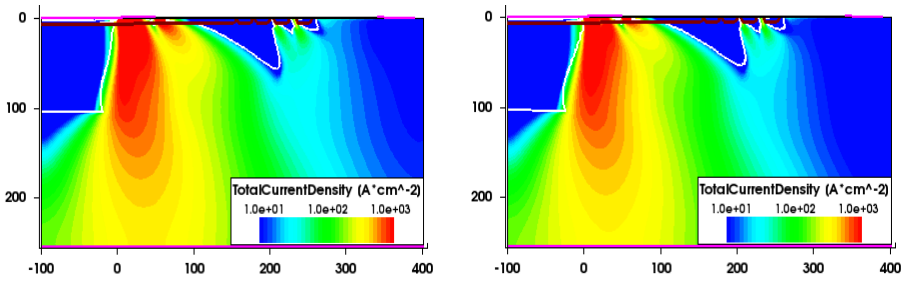


Figure 2.32. Current density distributions at the time t1 (a) and t2 (b) when the JTE peak doping is **optimal**.

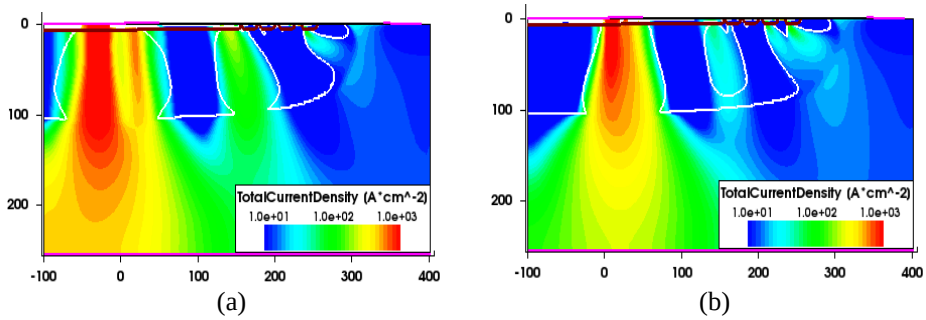
The case of a too *low* peak doping (Figure 2.33) is very critical for the device ruggedness. This because the electric field peak at the edge of the main junction is the only contribution to the ionization generation during the whole UIS transitory. The produced current path (the current distribution results identical a t1 and t2) brings to a fast increment of the local temperature, which leads a reduced UIS energy capability.



(a) (b)

Figure 2.33. Current density distributions at the time t1 (a) and t2 (b) when the JTE peak doping is too **low**.

Table 2.6 indicates as an increment of the avalanche energy capability can be achieved if the JTE peak doping is high. In this case, a better thermal distribution is due to the generation of several current paths. At the time t1 (Figure 2.34(a)) a main current contribution is located in active area, situation particularly advantageous in term of power dissipation. Figure 2.34(b) shows as, even in this case, the failure condition is due to the current crowding occurring at the edge of the main junction.



(a) (b)

Figure 2.34. Current density distributions at the time t1 (a) and t2 (b) when the JTE peak doping is too **high**.

2.4 Failure in termination and relation with NDR branch

In this section, the failure condition at the termination area due to filamentation problem is analyzed and correlated to the NDR branch on avalanche I-V curve. Depending on the overall device design the avalanche breakdown can occur either in active area or in termination area. This last can reveal particularly critical since the actual trend for the design of power semiconductor devices is the demand of high current density to reduce the overall die area. Electro-thermal UIS simulation on 2D structures are carried out to perform such analysis since it is commonly used in power devices validation in term of avalanche ruggedness [12]. During UIS transient unevenly current distribution can take place reducing the avalanche energy capability [23]- [29].

For this analysis a 2D FFR termination designed for a 600V punch-through IGBT is considered. FFR geometry is realized following two different techniques able to produce, with a similar breakdown capability, two different set of distances between the rings. The avalanche behavior at low current level is different for the two structures, permitting a better comprehension of the dynamic that occurs passing from low to high current level. In the latter condition the interaction between local electric field and charge, as well as, the presence of a NDR region in the forward blocking I-V curve are investigated with preliminary isothermal simulations. The self-heating effect on the termination region is evaluated by means of transient electro-thermal TCAD simulations by applying an idealized UIS test to the structures. Firstly, the influence of thermal effects on the current paths distribution is analyzed in PDR conditions. Finally, an analysis on the maximum sustainable energy in NDR condition are performed for different design solutions. Experimental proof of the theoretical results and current filamentation evidences are finally reported, by means of infrared thermal analysis.

Figure 2.35 shows the geometry of the adopted FFR termination. Both structures have the rings widths fixed at 10μm, since it represents a good trade-off to minimize the overall dimensions, and use three rings. Such number allows reaching a BV well beyond the

rate voltage of 600V, and a higher amount of it is not useful for scope of this analysis. The structures are realized adopting the optimization methodologies proposed in [4] and [8], here called *M1* and *M2*, respectively. Both of them are aimed to maximize the BV by appropriately spacing the distances among the rings (d1, d2 and d3).

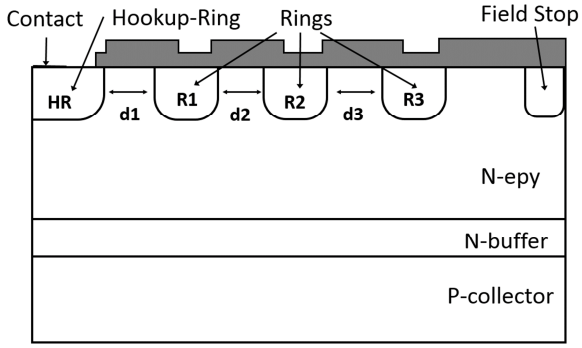


Figure 2.35. Sketch of FFR adopted for 600V PT-IGBT

It is important to note as in this analysis the active area is not directly connected to the termination, since hook-up ring is considered. The hook-up is an interface region appropriately designed to connect the active area with the termination [30].

The Epy-layer has doping concentration of $1x10^{14}$ cm^{-3} and thickness of 56μm. The Buffer region has doping concentration and thickness of $1x10^{17}$ cm^{-3} and 15μm, respectively, while the collector concentration is $5x10^{18}$ cm^{-3}. Finally, the results refer to terminations designed for a square active device of 1 cm^2. The physical models are same discussed in the Chapter 1, where the model *New University of Bologna* has been adopted for the avalanche generation. All parameters are kept at their default values, except the recombination lifetime of the Scharfetter model. Usually, lifetime killing techniques are adopted in the PT-IGBT technology and this was kept into account with a reduction of the lifetime in the structure with an electron lifetime and hole lifetime of 1μs and 300 ns, respectively. The two set of distances generated for M1 and M2 are listed in

Table 2.7.

Table 2.7. Rings spacing of M1 and M2.

Technique	***d1* [µm]**	***d2* [µm]**	***d3* [µm]**
M1	17	21	26
M2	18	21.5	27.5

The avalanche I-V curves of the two optimized terminations are reported in Figure 2.36 for a temperature of 300K. It is visible that for a current level of 10 µA the *M1* structure reaches a BV 15V higher than *M2* case; while for I > 10A they exhibit similar NDR branches with ΔV and ΔI of 180V and 950A, respectively.

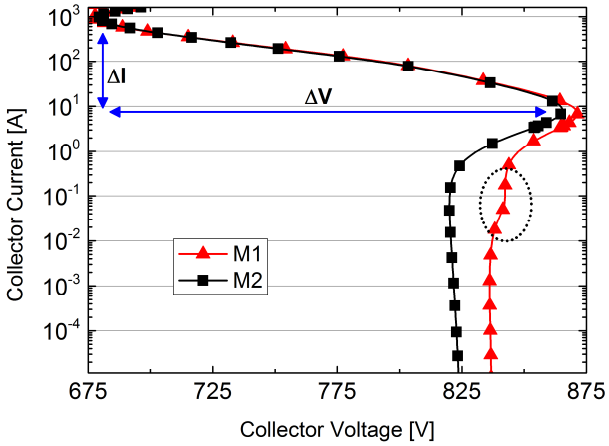
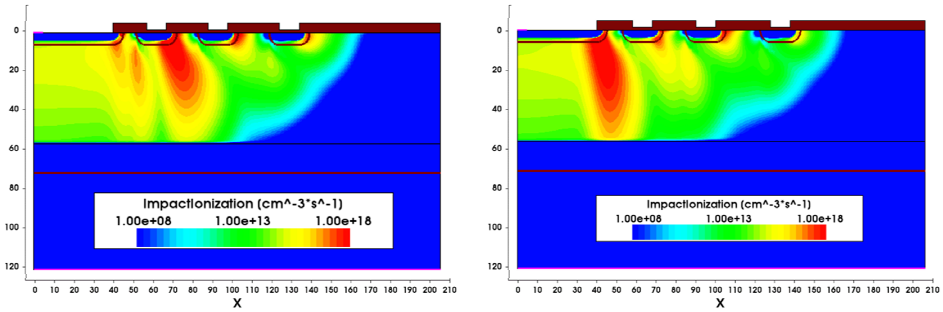


Figure 2.36. Avalanche I-V curves of the optimized *M1* and *M2* structures.

The weak difference between the two sets of ring distances does not significantly influences the maximum BV achievement; however it affects the electric field distribution which generates different local impact ionization rates. Contrary [4] and [8] where the optimization techniques leaded to a uniform electric field peaks on each ring junction and a consequent uniform distribution of current density at low current level, in this analysis, the electric field peaks are unevenly distributed. This is because in [4] and [8] a simple P/N junction (Diode structure) was analyzed, while in the PT-IGBT structure the current gain of the vertical *pnp* regulates the carriers flows ratio

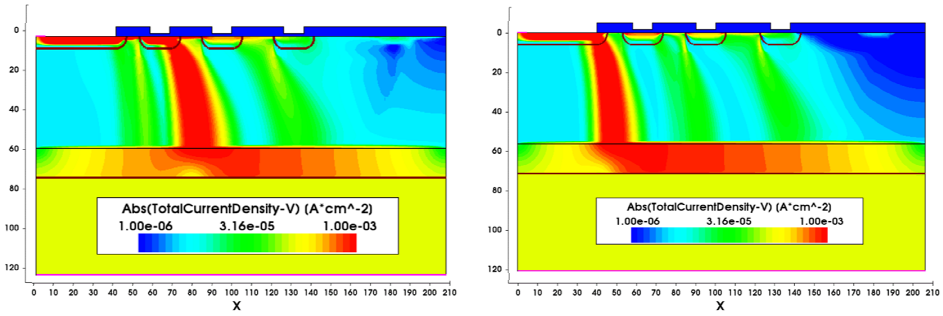
together with the impact generation rate in a more complex distribution. Non-uniformity of the generated carriers are reported at I=10µA in Figure 2.37. *M1* geometry produces a main contribution on the edge of the first ring, while *M2* has a main contribution on the edge of the hook-up ring.



(a) (b)

Figure 2.37. Impact ionization distributions at I=10 µA for M1 (a) and M2 (b).

It is more clear observing Figure 2.38 where the current density distributions of the two structures are depicted.



(a) (b)

Figure 2.38. Current density distributions at I=10 µA for M1 (a) and M2 (b).

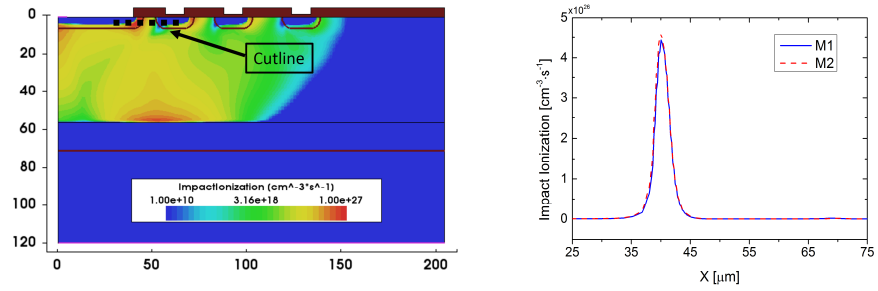
At this point, the behavior at high current levels is analyzed. The passage from low to high current level is defined in the following. The electric field can be redistributed according to Poisson law:

$$\frac{dE}{dx} = \frac{q(N_D + p - n)}{\varepsilon} \tag{2.6}$$

From (2.6) it is possible to define a threshold current density J_{Th}:

$$J_{Th} = qN_D v_{sat} \tag{2.7}$$

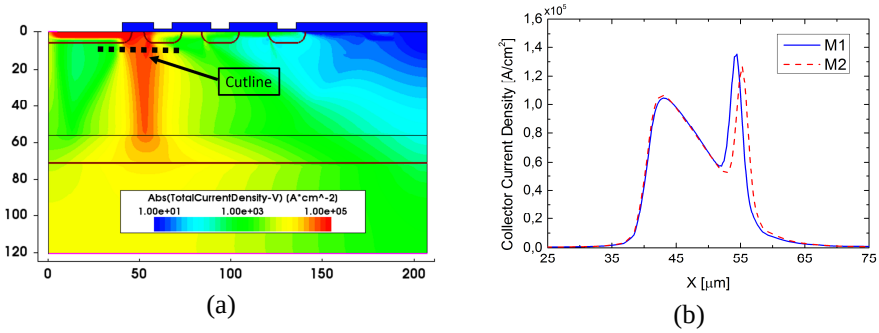
The doping concentration of the analyzed structure gives a $J_{Th} \approx 10^2$ A/cm^2 and the device operates in high current levels when the local current density exceeds this value. Because of the complexity of the phenomena that regulate termination behavior, it can happen that the condition is verified locally in a portion of the structure, even if the overall forced current density is lower than the J_{Th} current density level. In the investigated structures, the local high current level condition is reached for I>80mA and over this current level both *M1* and *M2* show the same current distributions (Figure 2.39).



(a) (b)

Figure 2.39. Impact ionization distribution at high current level (I=500A) for M1 (a). A very similar behavior occurs at M2 as visible in (b).

Figure 2.40 shows the current density distribution at high current levels (I=500A) of both structures. The high holes injection from the P-Collector into the depletion region warps the electric field distribution and an electric field peak E_{peak}=3.37x10^5 [V·cm^{-1}] is achieved at the edge of the hook-up ring, where the impact ionization shows a peak.



(a) (b)

Figure 2.40. Current density distribution at high current level (I=500A) for M1 (a). A very similar behavior occurs at M2 as visible in (b).

In such condition, the current crowds at the edge of the hookup ring, and this effect is the same in both the analyzed structures. In principle, the current collected by each ring should be the same, however, at high current levels the higher resistive current path for the carriers, coming from the floating filed rings, leads to a current crowding at the junction directly connected to ground. Finally, it can be observed in Figure 2.36 that the passage from low to high current level for M1 HCL is characterized by a fast variation in shape of the avalanche IV curve.

2.4.1 Electro-thermal analysis

The aim of this section is the investigation of the current paths in the termination area when electro-thermal effects occurs during the UIS test, up to high current levels. UIS test is used to investigate the effect of the temperature in avalanche conditions. During the test, the load current reaches a maximum value $I_{max,}$ than, linearly decreasing down to zero value, forcing the device to conduct in avalanche conditions. UIS test leads the device in electro-thermal overstress conditions, because of the contemporary high current and high voltage values, and both electrical and thermal effects are strictly correlated to each other and depend on the inductance value L (Figure 2.41). The slope depends on the inductance value and the BV in accordance to eq.(2.5).

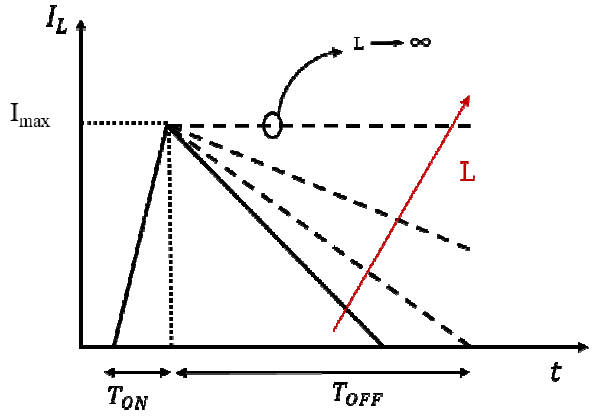
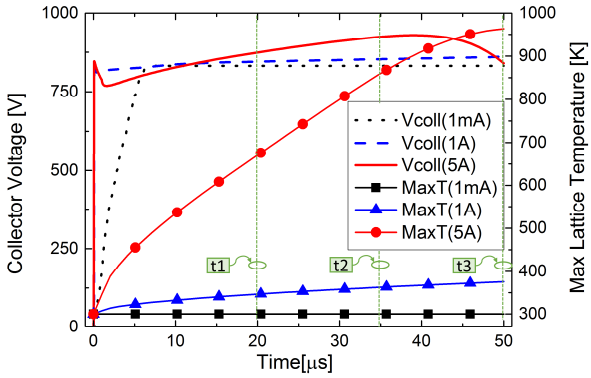


Figure 2.41. Inductive current trend under UIS test for different value of

inductance L.

To a better understanding of the thermal effects, the electrical dynamics is reduced supposing that the test is performed with an inductance whose value tends to infinite, therefore at constant current level. This is of course a worst-case condition and it investigates the lower boundary of the avalanche ruggedness of the structure. Three current levels are investigated to analyze the behavior at different levels of the I-V avalanche curve: I=1mA, I=1A and I=5A. Figure 2.42 shows the Voltage, the Current and the maximum temperature for the three current levels during a current pulse with a duration of 50µs.

(a)



(b)

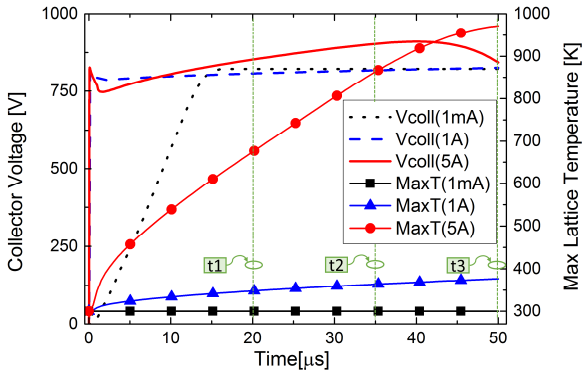


Figure 2.42.Collector voltage and maximum lattice temperature curves for the structures *M1* (a) and *M2* (b) during the current pulses at 1mA, 1A, 5A. The 2D current density distribution and temperature of the devices are taken

at times t1 = 20µs, t2 = 35µs and t3 = 50µs.

For I=1mA, at low current level, an electro-thermal equilibrium is achieved after a transient, therefore the maximum temperature and the BV are constant during the current pulse. It has to be highlighted that the current flow is so low, that the Collector voltage exhibits a ramp, due to the charge of the depletion region capacitance. This aspect is clear in Figure 2.43 where the current density and lattice temperature distributions for M1 and M2 at t1= 20µs, t2= 35µs, t3= 50µs are reported. Current waveforms perfectly overlap for both structures, while the temperature variation is negligible. Low current level electro-thermal simulations exhibit a terminations behavior similar to isothermal case in terms of current distribution.

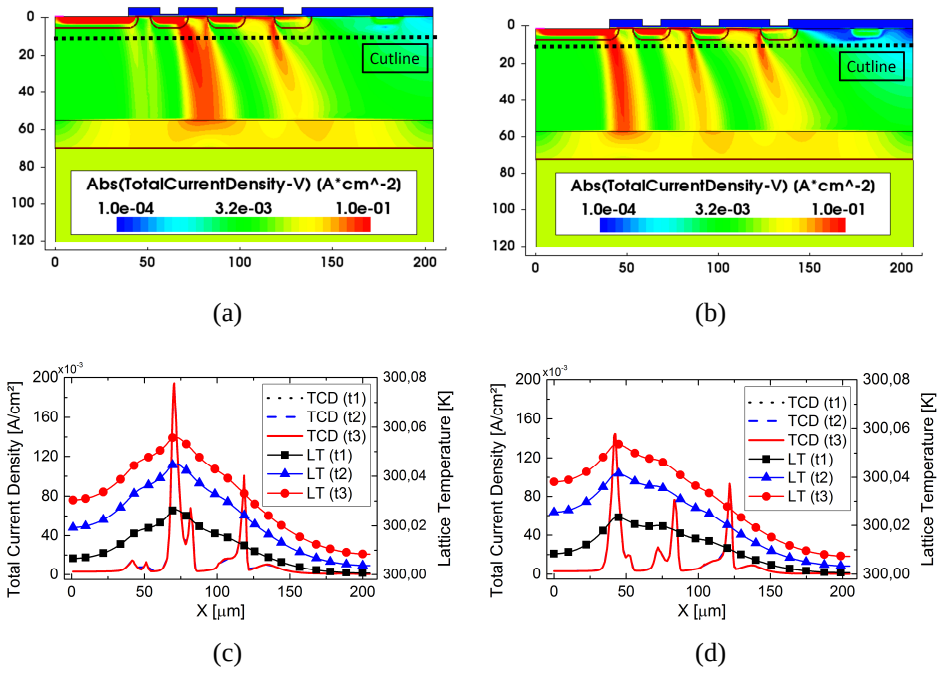


Figure 2.43. Current distributions in *M1* (a) and *M2* (b) when a current of **1mA** is forced in avalanche conditions. In (c) and (d) are depicted the section profiles of the total current density (*TCD*) and maximum lattice temperature (*LT*) extracted at 8µm from the surface for *M1* and *M2*, respectively. They show the steady-state behavior at the times t1, t2 and t3.

A different behavior rises when the forced current is in the range of the high current levels. With a pulse of 1A, the collector voltage of

both structures is approximately constant during the pulse and the maximum temperature reaches about 360K (). Because of the HCL achievement, thermal effects produce a variation of electric field distribution, and a consequent migration of the peak current from the first ring to the hookup ring of M1.

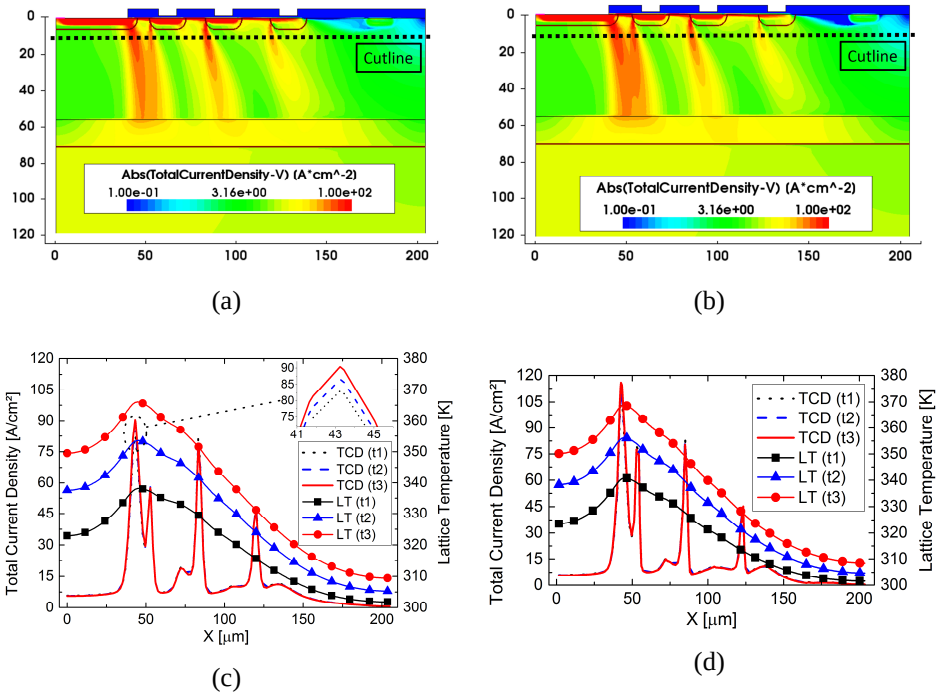


Figure 2.44. Current distributions in *M1* (a) and *M2* (b) when a current of **1A** is forced in avalanche conditions are shown. In (c) and (d) are depicted the section profiles of the *TCD* and *LT* extracted at 8µm from the surface for *M1* and *M2*, respectively. From t1 to t3 a temperature rises due to the carrier movement from the first ring to the hook-up ring.

This effect is emphasized at I_C=5A. The temperature rises and, locally, the impact ionization rate reduces. Even if current density peak decreases at the hook-up junction, the integral of current density in such area grows leading to a stronger temperature increase because of the higher dissipated power (Figure 2.45).

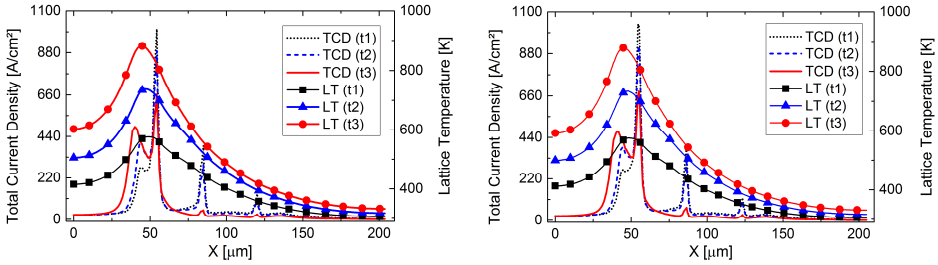


Figure 2.45. The section profiles of current density and max temperature for *M1* (a) and *M2* (b) for three time t1, t2 and t3 are shown when the structures are triggered in avalanche condition with a current pulse of I=**5A**.

This effect reduces drastically the reliability in avalanche condition because of power dissipation occurs in a restricted area of the device (termination area). Therefore, thermal dynamic shows a worsening of the behavior respect to the isothermal case. Critical thermal effects appearing already below (I_{max}=5A) the NDR branch, hence, are not linked to the filamentation problem. Actually, the current crowding observed in the previous analysis does not depend on the current filamentation in the longitudinal direction due to the NDR branch of the overall I-V curve in avalanche condition, but rather to the transverse complexity of the termination area. Finally, the thermal generation electron-hole pairs due to the temperature increment leads to the rising of the intrinsic carrier concentration and when the leakage current reaches the donor concentration N_D of epitaxial layer, the *pnp* junctions does not regulate the current flux and the device fails. Typically, the short-circuit condition in Silicon material occurs when the device temperature crosses 700K. This temperature limit can be used to estimate the thermal failure of the termination area as well.

2.4.2 Current crowding analysis in presence of NDR

In this section, through 2D TCAD simulations, the thermal effects of the crowding current on the termination behavior in avalanche condition and in presence of an NDR branch in the I-V blocking curve of the termination area is analyzed. The aim is the comprehension of the impact of the local increasing temperature, due to the filament, on

the device avalanche ruggedness. In detail, the analysis estimates the thermal dynamics occurring in the device during a UIS test and the amount of energy dissipated, making a comparison from two structure that exhibit different NDR branch on I-V curve.

Since the interaction between active area and termination strongly affects the device ruggedness in avalanche condition (it is not possible to know in advance if the avalanche current flows in one region or another), for the analysis, active area and termination are appropriately connected (Figure 2.46).

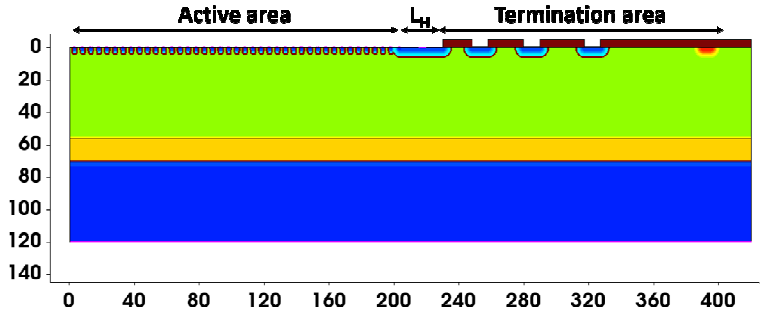


Figure 2.46. TCAD model of the analyzed structure.

In detail, 200μm of active area is connected to the termination area through a hook-up ring that has the same depth of the floating field rings and a width named L_H. The termination area is optimized by means of the technique coming from [4]. In order to achieve two devices that exhibit different NDR branch, it was chosen to act on the hook-up width. Indeed, the hook-up ring adds a resistive path to the current collected by the floating rings and its effect is increased by increasing its width. This reduces both ΔI and ΔV values of the NDR branch. In particular, the two structures have a L_H is 30μm (*Case1*) and 70μm (*Case2*), respectively. In Figure 2.47 avalanche curve of *Case1* and *Case2* are shown and compared with that of the active area. The first one present a valley point at I_{v1}=1615A, while a second one a valley point at I_{v2}=863A. It can be assumed that the avalanche current flows in termination area due to the lower BV of this last.

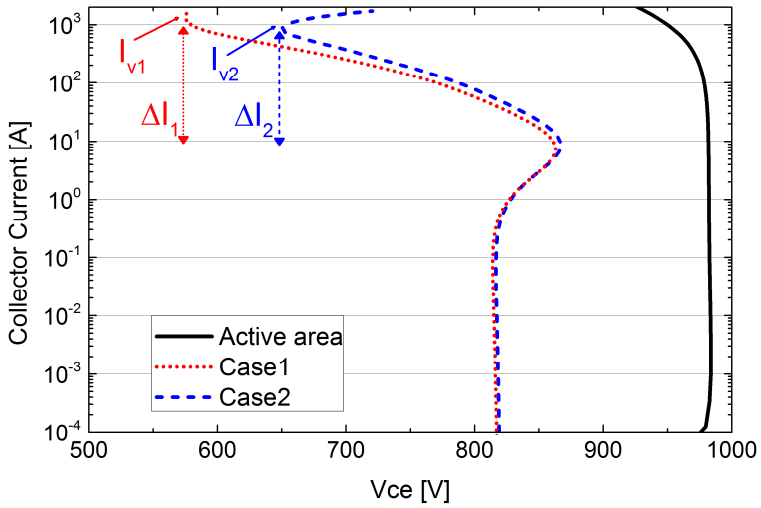


Figure 2.47. I-V avalanche curves of *Case1*, *Case2* structures and active area. For *Case1* the filament area is proportional to $\Delta I1 = I_{v1} - I_{Forced}$, while for *Case2* is proportional to $\Delta I2 = I_{v2} - I_{Forced}$.

In [25] the correlation between the NDR branch and the filament area is analyzed. In particular, it is found that the area of the filament is proportional to the ratio between the current at the valley point and the triggered current. Since the filament is focused in a small portion of the termination, in order to analyze the thermal effects produced by this phenomenon through 2D simulation, it is needed to consider a structure whose transverse dimensions are proportional to the filament area. The filament area is estimated by the relation (2.8):

$$A_{Filament} = I_{Force} / J_{Valley} \tag{2.8}$$

As predicted, the filament generation occurring at the termination region during the UIS simulation. In both, *Case1* and *Case2*, the filament is localized at the hook-up junction edge, remaining stable in that place during the pulse. In Figure 2.48 the filament thermal effects of the two terminations whose dimensions are determined by eq.(2.8) are shown. The devices are triggered in avalanche condition by applying a current pulse with peak of 10A, a current value that lies on the NDR branch.

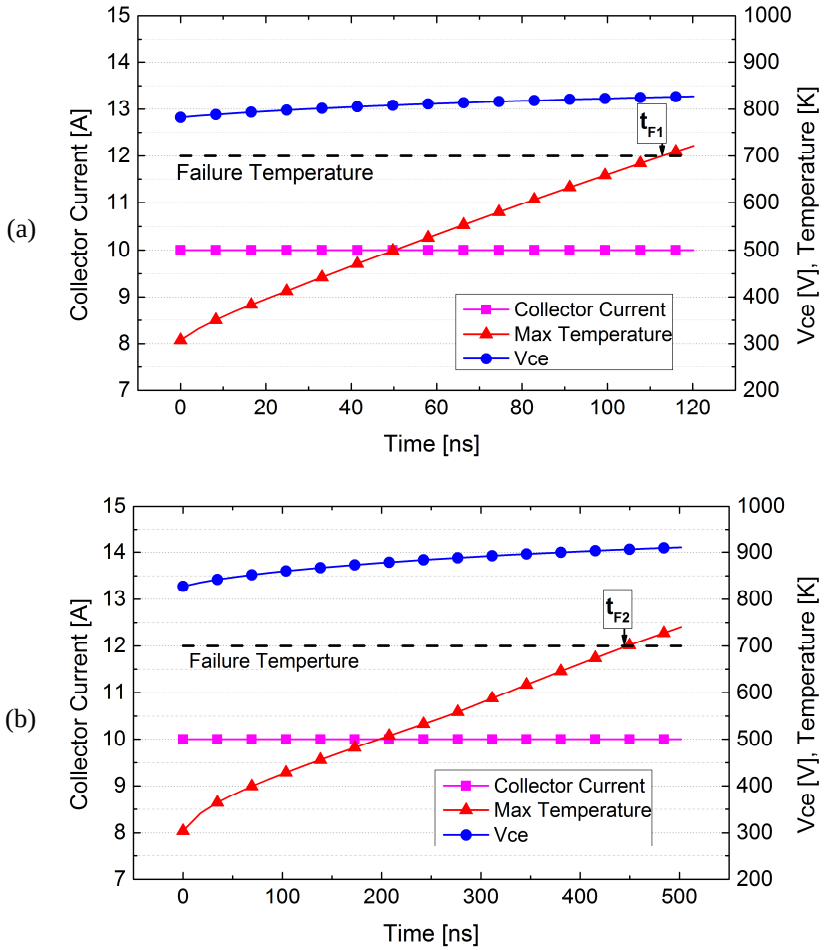


Figure 2.48. Collector current, Collector Voltage and Maximum temperature curves during the UIS test for *Case1* (a) and *Case2* (b), with a triggered current of 10A in filamentation condition.

Both terminations show a fast increment of the maximum temperature with the *Case1* that reaches the temperature threshold of 700 K in t_{F1} = 114 ns while the *Case2* in t_{F2} = 450 ns. The rapid temperature threshold achievement is caused by the stability of filament at the edge of the main junction. As expected, *Case2* design allows to dissipate a higher energy amount, corresponding to 3.94 mJ, respect to 950 μJ of the other structure.

2.4.3 Experimental results

The previous numerical analysis and theoretical approach is supported by an experimental case study discussed in this section. A 600V–200A rated commercial IGBT with trench-gate structure is used as device under test for dynamic thermal analysis in avalanche condition. This aspect is investigated by both UIS test and infrared thermography. In Figure 2.49 is shown the device behavior under UIS test at a peak current of 1 A.

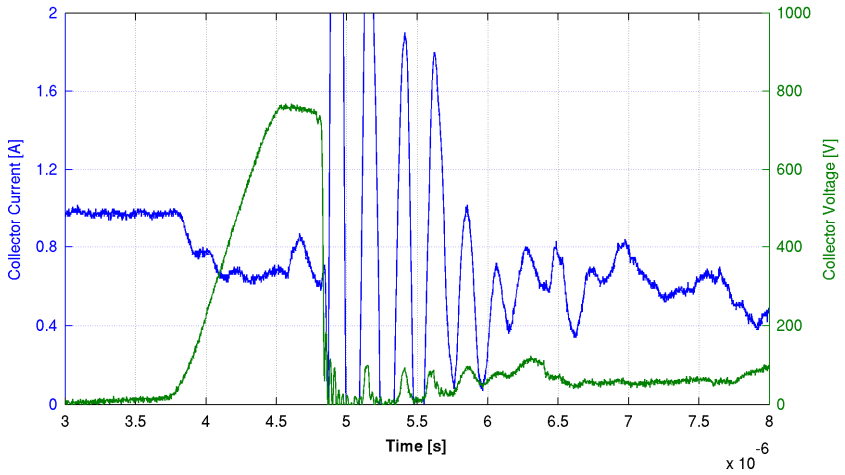
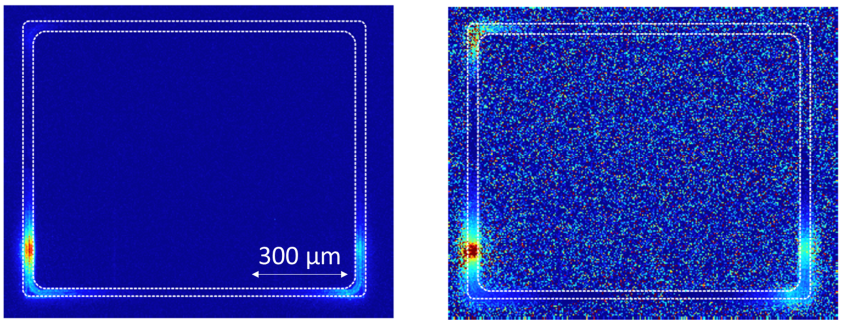


Figure 2.49. UIS current and voltage waveforms with I_{max}=1A on a DUT.

The curves show the device failure at low dissipated energy after about 200 ns, confirming the results achieved in previous section. To investigate the current distribution on the device area, a state-of-art infrared thermography system [31] is employed to perform transient lock-in measurements [32] in UIS operation. This technique is demanded for measuring transient operation within short time interval, resulting in a weak temperature increase on the device top-surface. (The principle is based on the periodically repetition of the transient and detect the temperature distribution in lock-in mode [33]). The resultant thermal map shows the mean value of the temperature distribution over the repetition time. As in the numerical analysis, the power is applied to the DUT only for a Δt time and the temperature

distribution detected is basically the mean temperature distribution during this time.

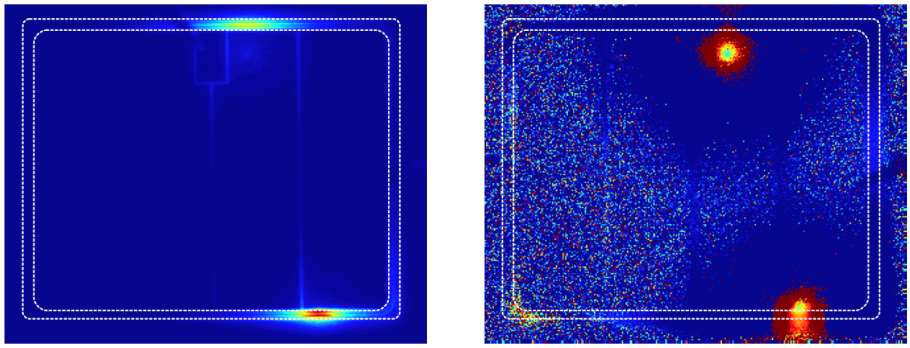
Experiments are carried-out at different current levels during avalanche operation, and thermal maps show the presence of a current filamentation phenomenon on the device periphery as demonstrated in the numerical analysis. In the following two relevant cases are reported. In Figure 2.50 (a) the resultant amplitude thermal map of the lock-in algorithm is shown for a total current of 0.5mA.



(a) (b)

Figure 2.50. Amplitude thermal map for a transient lock-in measure in avalanche condition at 0.5mA; (b) Related power distribution after emissivity correction algorithm application.

A hot spot is visible on the termination region, however to recover the real power distribution it is mandatory to compensate the emissivity contrast effect [33]. Using the in-phase and the out-phase output images of the lock-in procedure the correct estimation of the power distribution was revealed [34] as depicted Figure 2.50 (b). This last picture confirms a filament presence on the termination region, with some other weak current conduction on the periphery. The second presented result is obtained for a current level of 2mA. Figure 2.51 (a) show again the presence of hot spots on the device periphery; on the other Figure 2.51 (b) clearly shows two current filaments inside the device.



(a) (b)

Figure 2.51. Amplitude thermal map for a transient lock-in measure in avalanche condition at 2mA; (b) Related power distribution after emissivity correction algorithm application.

The first one located across the termination region and the device active area, while the second one insists on the active area. The meaning is that increasing the external current, more filaments can coexists and an interplay between the two regions arises.

Summarizing the work presented in this section, study of the current path at high current levels in avalanche conditions was carried out for the termination of a PT IGBT structure, with a 600V voltage rate by means of 2D TCAD simulations. Two termination designs were presented with two different methodology of optimization in order to maximize the breakdown voltage. The analysis of current paths was extended up to high current levels by studying the phenomena occurring both in static and dynamic conditions. The static avalanche I-V curve shows different behavior of the two structures with current paths generated at low current level distributed in different locations. Nevertheless, the field-charge interaction at high current level produces as effect a current crowding at the main junction and the current distribution of both terminations tends to uniform. Electro-thermal simulations were performed to evaluate the thermal dynamics occurring in the structures during the UIS test at different current values. They confirm the results achieved in isothermal analysis, which highlight analogous crowding current problems at high current level due the movement (in both cases) of the current density toward the hookup junction. Although it cannot talks of filamentation problem, the current crowding occurring at high current level leads as

consequence an increment of power dissipation in a restricted portion of the device that severely affecting the reliability. An in-depth filament analysis in 2D simulations was presented. The results highlight times and dynamics of failure in accordance with experimental cases. These last were studied by means of infrared thermography with lock-in measurements. The thermal maps reveal the filament generations at the periphery of the device that are responsible for the eventual device failure.

2.5 Process emulation of a FFR termination

The predictive emulation of a real technological process by means of TCAD simulations permits to reduce the time-consumption and costs of fabrication process. Simulation process usually involves deposition, etching, planarization and implantation of different species. The models development related to each process phase is constituted of separate field of research [35].

In this section, a FFR termination process is emulated. The final FFR structure is the same adopted in the previous analysis for a PT-IGBT 600V rated.

The process flow expects the following steps:

- Epitaxial growing
- Oxide growing on the epitaxial layer
- Boron implantation and diffusion
- Trench Gate generation process
- Active area implantations and diffusions

The option *Advanced Calibration* has been activated. It provides advanced process models for an accurate definition of the doping profile.

As starting point, the domain of the Collector layer is defined together with a grid mesh by the command:

```
line x location= 0.0        spacing=50<nm>   tag=SiTop
line x location= 0.5<um>  spacing=100<nm>
line x location= 3<um>  spacing=500<nm>
line x location=$ysub<um>  spacing= 3.0<um>  tag=SiBottom
line y location=0.0        spacing=2.5<um>  tag=Mid
line y location=$xsi<um>  spacing=2.5<um>  tag=Right
region Silicon xlo=SiTop xhi=SiBottom ylo=Mid yhi=Right
init concentration=5e18 field=Phosphorus  !DelayFull
```

Phosphorus is used as dopant with a concentration of $5x10^{18}$ cm^{-3}. The mesh in proximity of the surface has been made very tight, as visible in Figure 2.52. Because of improving the accuracy and the convergence of the following *epitaxial growing* step. The following command have been used:

```
mgoals on min.normal.size= 0.01<um> normal.growth.ratio= 1.41 \
     accuracy= 1e-6<um> minedge= 2e-5<um> max.box.angle= 90
refinebox name= Interface1 #  min.normal.size= 0.05 \
     interface.materials= "Silicon"
```

where *mgoals* instances change the default parameters, while *refinebox* defines the interface refinements.

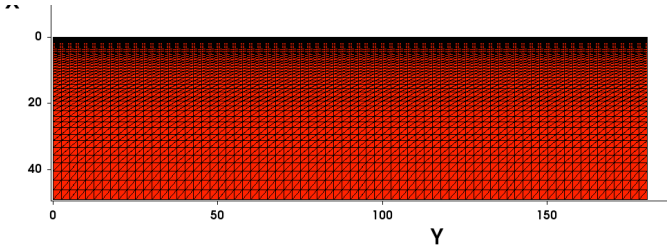


Figure 2.52. Mesh grid at the surface of the epitaxial layer.

Both Buffer layer and Drift layer are realized for epitaxial growing with the command:

```
diffuse thick= TK <um> temperature= 900 <C> time TIME <min> \
   epi epi_doping= {Phosphorous = DopingConcentration } \
      epi_layers= N info= $diff_info
```

In particular, *TK*, *TIME* and *N* are set to determine the number of horizontal lines composing the grid. The epitaxial layer is grown at the temperature of 900K. The doping concentration is $1x10^{17}$ cm^{-3} for the

Buffer and $1x10^{14}$ cm^{-3} for Drift. Figure 2.53 shows the whole termination area after the epitaxial growing. It is well visible as the back side is a PT structure.

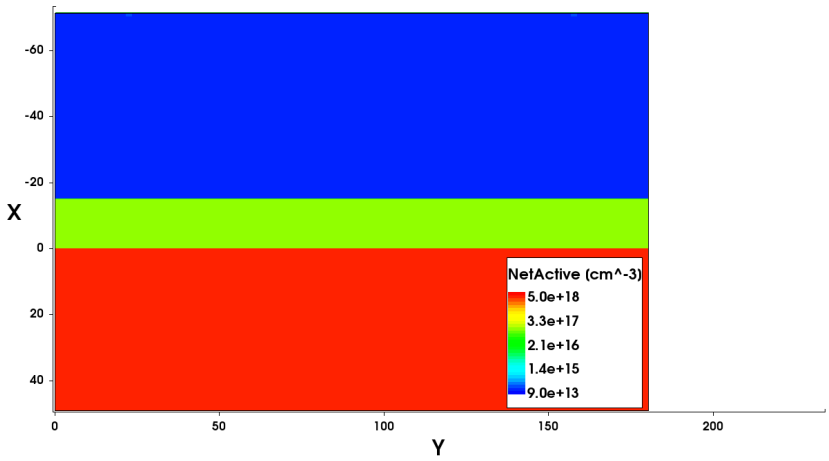


Figure 2.53. FFR structure after the epitaxial growing.

The mesh grid of the bulk has been made recurring to the *adaptive meshing*. It enhances the evolution of the doping profile during the process. This permits to reduce the simulation time due to its direct action on the operating areas. The re-mesh can be provided for any process step: etching, deposition, implantation, etc.. Furthermore, a specific interval time can be set to make an evaluation control on the re-mesh necessity. The adaptive meshing is activated with the command:

```
pdbSet Grid Adaptive 1
```

In this project three adaptive *refineboxes* have been adopted:

```
refinebox name= Buttom adaptive Silicon \
    min= "-0.1 -0.1" max= "50 180.1" \
    refine.min.edge= ".5 .5" refine.max.edge= "5.0 5.0" \
    def.abs.error= "2.5e18" def.rel.error= "0.5"

refinebox name= Epi adaptive Silicon \
    min= "0 -0.1" max= "-75 180.1" \
    refine.min.edge= "0.2 .5" refine.max.edge= "2.0 2.0" \
    def.abs.error= "2.5e14" def.rel.error= "0.5"
```

```
refinebox name= Active adaptive Silicon\
    min= "-75.0 -0.1" max= "50 180" \
    refine.min.edge= "0.2 0.5" refine.max.edge= "5.0 5.0" \
    abs.error= "Phosphorus= 5e14 Boron= 5e14 Arsenic= 5e16"
    def.rel.error= "1.0"  max.dose.error= "Phosphorus= 1e8 Boron= 1e9
    Arsenic= 1e11"
```

def.abs.error and *def.rel.error* are the absolute and relative error, respectively. The minimum length edge is set by means of *refine.min.edge*. This last if too small can introduce a too large number of nodes. The first refinebox (named “Bottom”) is applied to the PT structure, the second (named “Epi”) is applied to the Epi-layer, and the third (named “Active”) is applied to the whole structure exerting a control action respect to doping concentrations.

It is important that the top of the structure has a very thin mesh the favor the accuracy and convergence during the *thermal oxidation*. During such process step, part of the silicon surface is consumed since its reaction with the oxide atoms. Thermal oxidation is realize with the following command:

```
grid set.min.normal.size=3<nm> set.normal.growth.ratio.2d=1.6
diffuse temperature=110<C>  time=80<min> H2O
```

The mesh oxide generation during the oxidation is set by means of the command *grid,* specifying the minimum grid size and aspect ratio. The oxidation is made in Wet Ambient at a temperature of 110°C for a time of 80 minutes. It allows generating an Oxide layer of 800 nm with a consumption of surface of about 345 nm (Figure 2.54).

Figure 2.54. Structure surface after thermal oxidation.

An anisotropic etching has been used to generate the mask windows for the Boron implantation (Figure 2.55). A “screening”

oxide of 20nm is deposited on the surface to favor the penetration capacitance of the implantation and, furthermore, reducing the surface damage.

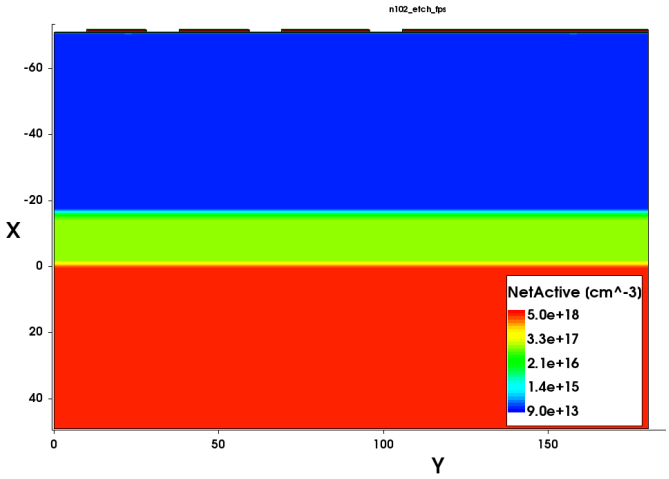


Figure 2.55. Mask etching to realize the main junction and rings implantations.

To realize the implantation and diffusion of the Boron an appropriate re-meshing is needed to achieve an accurate definition of the generated doping profile as in Figure 2.56.

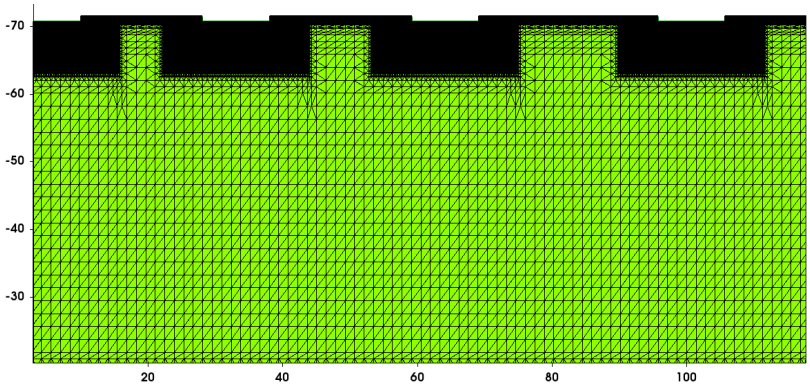


Figure 2.56. Mesh grid improvement for drive-in step.

The Boron implantation and diffusion have been generated with the command:

```
implant  Boron  dose=5e14  energy=150 tilt=0 rotation=0
diffuse temperature=1150<C>  time=20<min> H2O
```

A Boron dose of $5x10^{14}$ cm^{-2} with energy of 150eV has been implanted with angulation of zero degrees. It is followed by dopant diffusion by means of thermal oxidation in Wet Ambient at temperature of 1150°C for a time of 20 minutes. The latter his been realized selecting the *React* model for the thermal diffusion as:

```
pdbSet Silicon Boron DiffModel React
```

React model allows an advanced description of the dopant transport. It solves a set of differential equations that describe both the substitutional and defects of the flux dopant. The silicon surface at the end of the thermal oxidation results deeply modified as visible in Figure 2.57. It can be seen as the oxide has consumed a further portion of silicon in correspondence of the mask window. In this phase the junction depth of the Boron is lower than 4µm.

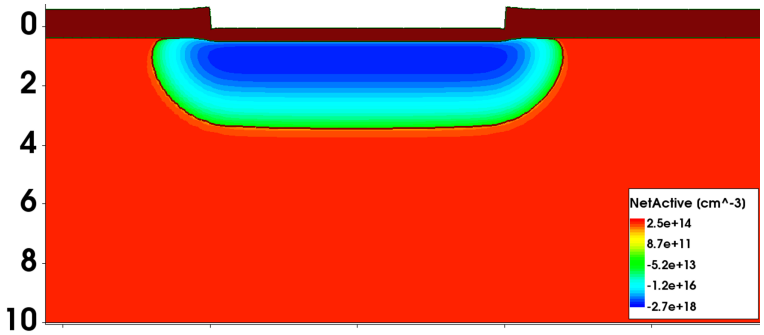


Figure 2.57. Surface view after Boron diffusion.

The structure is then subjected to a Nitridation process realized at temperature = 1150°C and time = 80'. Only at this point the Trench Gate and P-body are realized. Taking into account the thermal budget due to these last two process steps, the final structure results as in Figure 2.60, where the Boron junction depth has reached 6 µm.

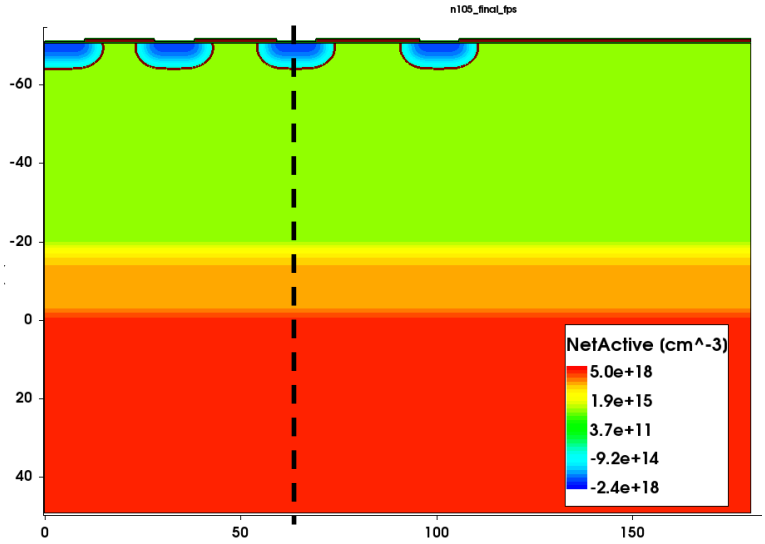


Figure 2.58. End process FFR structure.

In is interesting to see as the doping profile of the whole structure (extracted along the vertical black line) changing at any step process (see Figure 2.59).

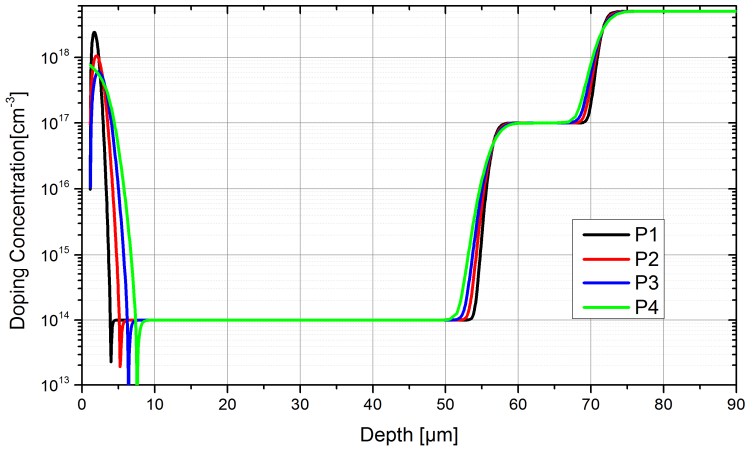
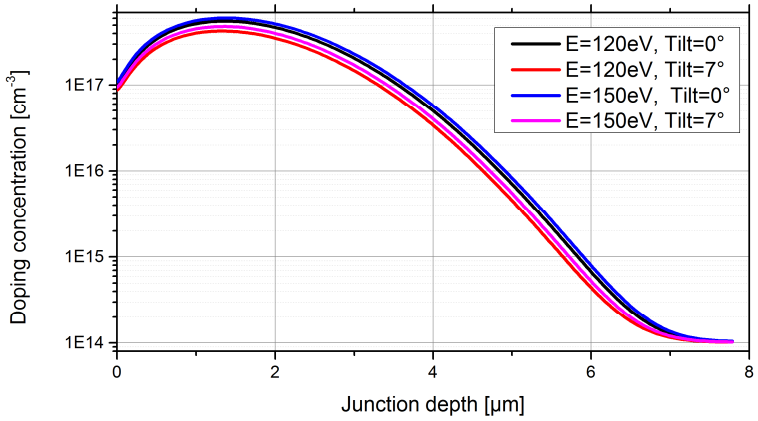


Figure 2.59. Vertical doping profile extracted at the end of each step process: P1 = Boron implantation diffusion; P2 = Nitridation; P3 = Trench Gate; P4 = P-body implant diffusion.

The influence of the process parameters on the Boron doping profile are reported in Figure 2.60.

(a)



(b)

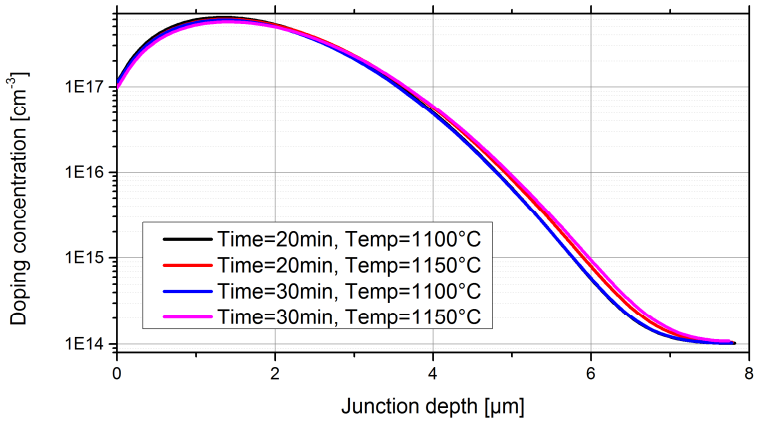


Figure 2.60. Boron doping profile for: (a) different combinations of Energies and Tilt angulations with Temperature = 1150 °C and Time = 20'; (b) different combination of Temperatures and Times with Energy = 150eV and Tilt=0°.

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Chapter 3

Short-Circuit capability analysis on a new design of FS-IGBT device.

Today is always more growing the demand of high reliability for power semiconductor devices. In particular, in fields like automotive or high power converters a comprehension of the failure mechanisms is needed to prevent the device premature destruction during its nominal condition. The Short-Circuit is one of the most critical condition for a semiconductor device which is subjected to a contemporary action of high current and high voltage that lead to a quick increase of temperature due to the Joule effect. In this condition, the current is only limited by the internal device resistance and could be several times higher than the nominal rated one leading to a fault condition. In this scenario the reliability of an IGBT 600V rated, realized in Field-Stop (FS) technology, is analyzed under Short-Circuit over-stress condition. The involved device is provided by a leader company in the field of power semiconductor devices. The IGBT Short-Circuit failure mechanisms can be essentially distinguished in three main modes as depicted in Figure 3.1 [1]:

A) The failure occurs near the peak current [2]. It can be named as “Power limited failure”.
B) The failure occurs during the steady state due to the high energy dissipation which produces a local increase of temperature [3]. It can be called “Energy limit failure”.
C) The device fails at the turn-off, definable as “Inhomogeneous operation failure” [4].

In this work only the failure mode *B* is considered.

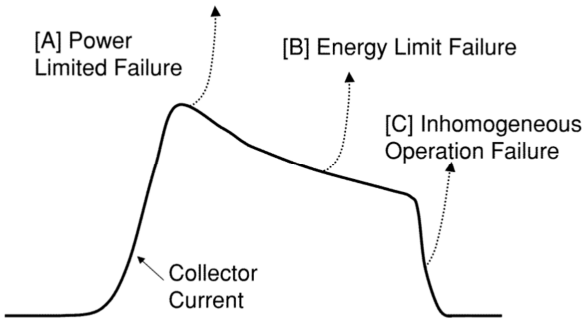


Figure 3.1. Short-Circuit failure mechanisms.

The aim of this analysis is to evaluate the influence of the device design on the Short-Circuit capability by means of 3D TCAD simulations. This requires an experimental characterization of the DUT in order to calibrate the physical models of the TCAD elementary cell. Finally, several design proposed in order to increase the Short-Circuit capability.

3.1 Structure definition and calibration

A correct description of the elementary cell physical models is needed due to the strong dependence between the dynamic during the Short-Circuit and device design. It also requires of coupling both electrical and thermal equations. Since the elementary cell geometries and doping profiles directly affect the Short-Circuit capability, its accurate calibration and description is mandatory for a quantitative evolution of the device operations.

3.1.1 Structure definition

In this section the definition of the elementary cell is presented. Prior to proceed with the calibration phase, the reconstruction of realistic doping profiles and geometries is necessary. In order to extrapolate

the information both Scanning Electron Microscopy (SEM) and Spreading Resistance Profiling (SRP) techniques have been used.
A SEM image of the device top view is shown in Figure 3.2, where the section of the elementary cell that needs of the definition is highlighted. The active area can be achieved for symmetry of the elementary cell, replicating it along the longitudinal direction and extruding it along the transversal direction. With TCAD simulation is more convenient working on the half pitch cell to reduce the number of nodes constituting the mesh. The overhead structure is known as Self Aligned Structure [5].

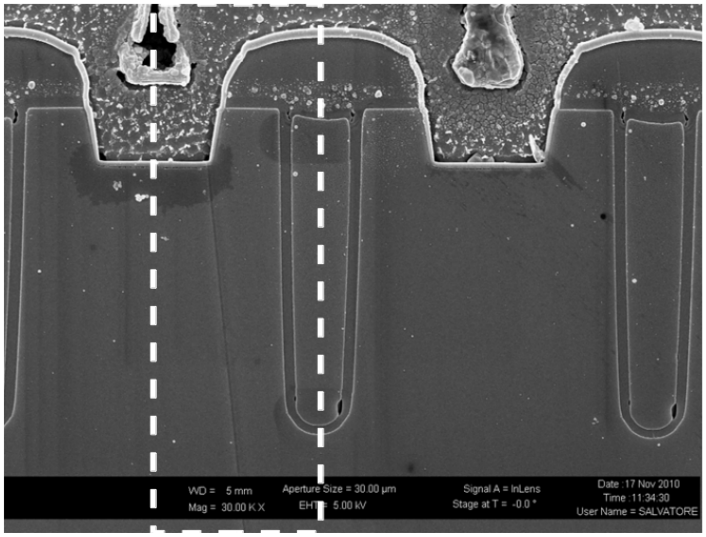
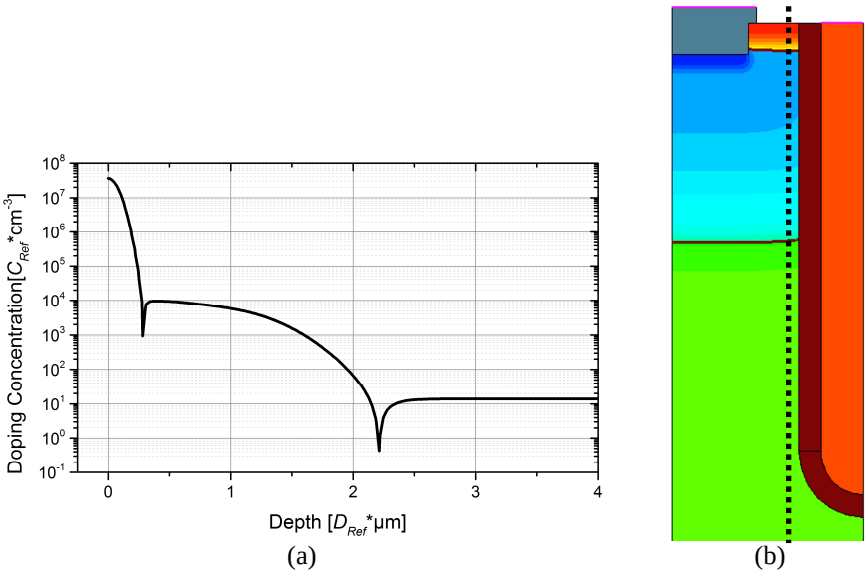


Figure 3.2. SEM section of the analyzed structure.

The Gate Trench and the Contact Trench can be considered geometrically separated. In particular, the former lies on the right side of the rectangle, while the latter is on the opposite side. By measuring such dimensions is possible to determine the geometries of the elementary cell. The Contact Trench has the main role of suppressing the letch-up phenomenon [6]. It allows reducing for the holes that passing below Emitter diffusion coming from the Emitter contact. In absence of Contact Trench, the path travelled by holes to approach the silicon/metal junction interface generates a higher voltage drop at the P-body/Emitter junction. The Contact Trench has further advantage, since the metal/silicon interface increases the recombination rate of

carriers reducing the holes flow. However, as it will be illustrated in the next section, this solution a part to increase the latch-up immunity, also reduces the device reliability during the avalanche condition.
The doping profile are achieved by means of both SRP measurements and by process emulation. The latter, realized with emulation process tool of ATHENA® Silvaco, has provided the most of the information. The P-body diffusion is realized before the Trench Gate structure, and doping profile in proximity of the Silicon/Oxide interface presents a curvature, due to the Boron segregation [60] within the oxide, which reduces the concentration close to the interface.
Emulation process data together with SRP measurements have provided the doping profile of the P-body region and the back of the device. In Figure 3.3(a) illustrates the SRP profile of the P-body diffusion. In general, the SRP measurements are affect by uncertainty, this leads to recreate the doping profiles used in for the simulations mainly by means of process emulation. The SRP profile are used to verity the coherence of the achieved results. The doping profile of the elementary cell are recreated by superimposition of Gaussian functions.



(a) (b)

Figure 3.3. (a) SRP profile of the P-body region. (b) 2D TCAD elementary cell of the FS-IGBT.

Figure 3.3(b) offers a geometrical point of view of the reconstructed TCAD structure. It points out as the main difference respect to the real one is the vertical slope of the trench. The former presents light shrinkage from the top to the bottom, while the reconstructed trench has a vertical slope. Anyway, this detail has not relevant effects on both on-state and avalanche conditions. Figure 3.4 shows the absolute doping profile extracted in correspondence of the black line of Figure 3.3(b).

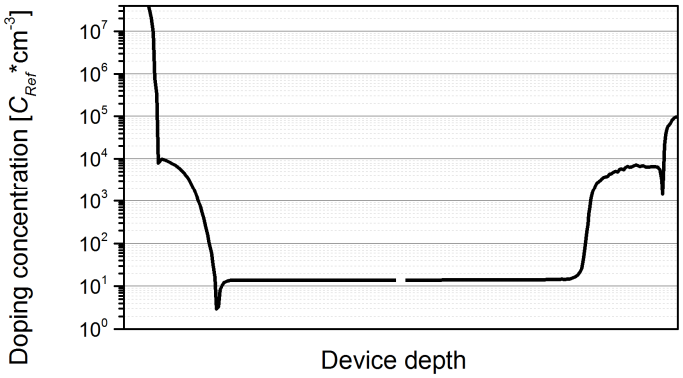


Figure 3.4. Doping profile of the overall structure.

3.1.2 Emitter diffusion modulation

As previously discussed, during the Short-Circuit mode the device is forced under high voltage and high current, which can generate high power dissipation due to the local increment of the temperature. Since a larger Short-Circuit current produces a larger thermal loss, the device has to be design to produce an adequate saturation current. The Short-Circuit capability can be essentially addressed on two factor:

1) Saturation current of the device. The Short-Circuit capability decreases when the saturation current increases due to the rising of the local temperature.
2) Carriers lifetime. The Short-Circuit capability increases when the lifetime of the device decreases. The lifetime (through the diffusion length) is related to the gain of the parasitic PNP of the structure in accordance to equations (1.14) and (1.15). Since the saturation Emitter current can be expressed as:

$$I_E = \frac{I_n}{1-\alpha_{PNP}} \tag{3.1}$$

Eq.(3.1) highlights as the injection efficiency of the IGBT reduces the Short-Circuit capability.

To reduce the saturation current, it is possible to optimize the surface structure as reported in [8], [9]. Another possible solution consists in the modulation of the Emitter diffusion region (N^+) [10], [11]. The Self-Aligned process is modified to control the extension of the Emitter diffusion along the orthogonal plan to the section in Figure 3.3(b). The Emitter modulation can be defined as the ratio between N^+-Emitter diffusion length along the z-axis and the elementary cell length along the z-axis expressed in percentage. The 3D cell and layout of the structure in which the Emitter modulation is applied is depicted in Figure 3.5. In Table 3.1 are reported the simulated V_{ON} and I_{SAT} values of the calibrated structure for different Emitter modulations. In particular, *M25*, *M50* and *M75* refer to a structures having the Emitter diffusion modulated of 25%, 50% and 75%, respectively.

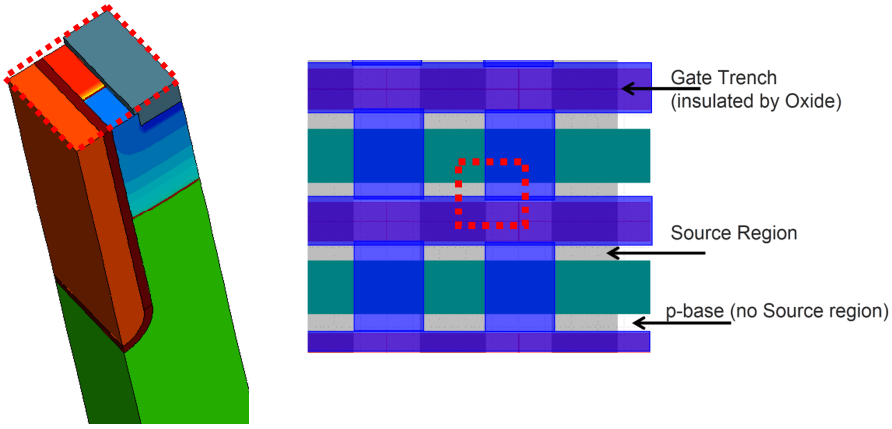


Figure 3.5. (a) 3D structure. (b) Top view layout of the structure.

Table 3.1. V_{ON} and I_{sat} for different Emitter modulations of the analyzed structure.

Design	V_{on} **[V] at** J_C **= 100A/cm²**	I_{SAT} **[A] at** V_{CE} **= 10V**
M 25	1.246	11.62
M 50	1.288	11.30
M 75	1.247	11.42

3.2 Experimental calibration

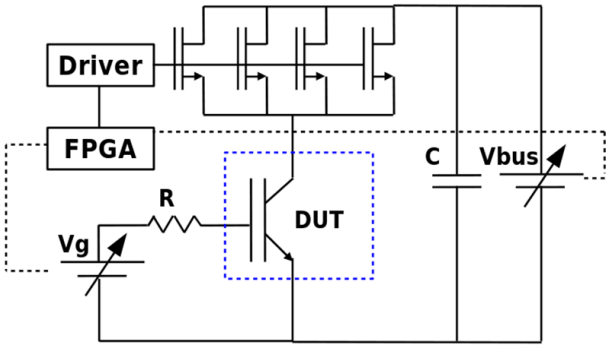


Figure 3.6. Experimental set-up of the pulsed curve-tracer

Figure 3.6 illustrates the setup adopted to trace the I_C-V_{CE} and I_C-V_{GE} curves of the DUT. The measurements are led under pulsed regime in way to not affect the results by self-heating effects. The setup operates providing a fixed Gate voltage by means of the generator V_g, while V_{bus} fixes the Collector voltage. Four Power MOSFET in parallel control V_{bus}. The FPGA manages the timing and operates a feedback control to stabilize both Gate and Collector voltages, and it is configurable. Terminal characteristics have been measured at three temperatures 25, 100 and 150 °C. The output characteristic is traced imposing a Gate voltage of 15V, while the I_C-V_{GE} curve is traced for V_{CE} = 10V.

To evaluate the lifetime dependence of the device by the temperature Inductive Load Switching (ILS) measurements have been carried out. The ILS test is an industrial test used for quality control of power semiconductor devices [12]-[15]. During the test a considerable energy can be dissipated by the DUT determining its failure. The aim

of this test is to identify the failure starting point, hence, the amount of energy dissipated before the catastrophic event.
The set-up circuit for the ILS measurements is analogous to that depicted in Figure 1.21. During the turn-off the current decreases, in a first time linearly, then due to stored charge, recombination mechanisms overcome. The carriers lifetime can be evaluated observing the current tail of the device (see Figure 3.7). It provides a global information since it is not possible distinguishing the lifetime associated to the Drift region and the Buffer region, due to the tight length of the Field Stop buffer. A detailed evaluation of the buffer lifetime is not possible because of the oscillations occurring for V_{CE} = 400V at ambient temperature. Iterating the procedure for different temperatures, it is possible to determine the trend on the temperature dependence of the lifetime. This allows estimating the parameter *C* of the eq. 1.112.

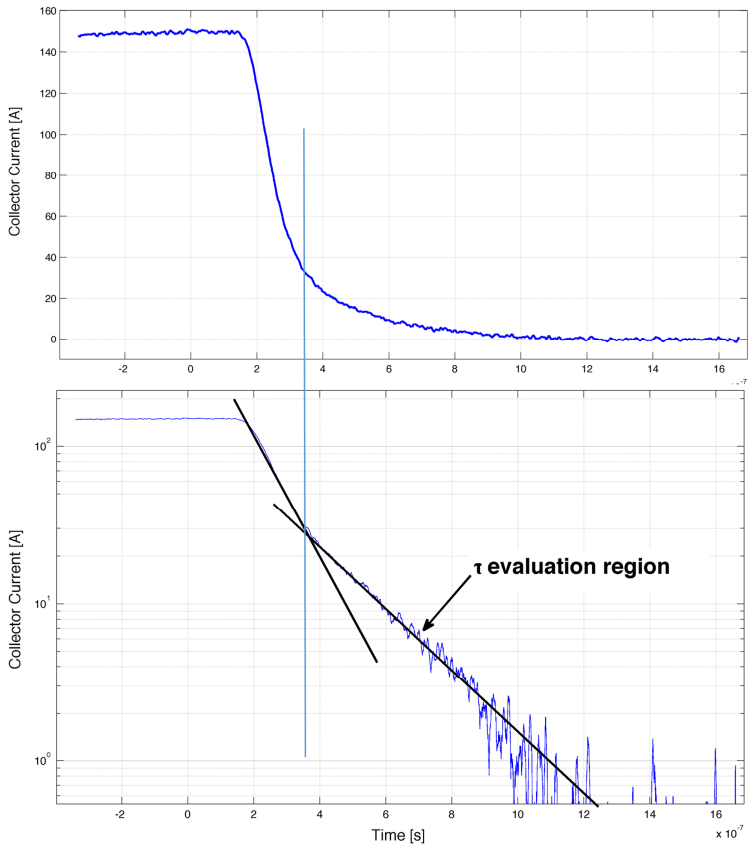


Figure 3.7. ILS waveforms evaluation for the lifetime extrapolation.

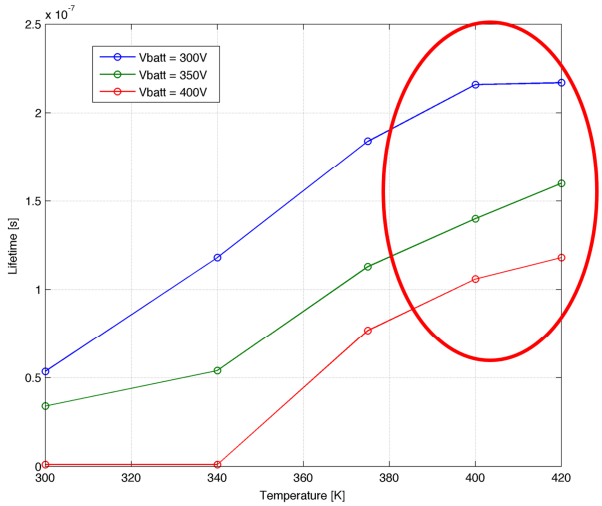


Figure 3.8. Extrapolated lifetime in dependence on temperature extrapolated at different battery voltages.

The calibration produce expects to match both the simulated I_C-V_{GE} and I_C-V_{CE} characteristics on the experimental ones. The curve fitting of the I_C-V_{GE} characteristic is constituted by two parts: the fitting of the sub-threshold region and the fitting at high current level. The calibration is realized at three temperatures: 25, 100and 150 °C. The parameters of the physical models considered to fit the experimental curves are reported in Table 3.2.

Table 3.2. Parameters details

Model	***Symbol***	***Default Value***	***Calibrated Value***
Scharfetter	τ_n	$1x10^{-5}$ [s]	$6.921x10^{-7}$ [s]
	τ_p	$3x10^{-6}$ [s]	$2.078x10^{-7}$ [s]
	N_{Ref}	$1x10^{16}$ [cm^{-3}]	$8x10^{15}$ [cm^{-3}]
	T_α	-1.5	3.5
	E_{trap}	0.33 [eV]	-0.2 [eV]
Arora	$\mu_{max,n}$	1252 [cm^2/V·s]	1001.6 [cm^2/V·s]
	$\mu_{min,n}$	88 [cm^2/V·s]	70.4 [cm^2/V·s]

As visible from eq.(1.53) the sub-threshold current slope depends on the ratio between the oxide capacitance and the depletion region capacitance. The oxide capacitance is related to the values of both oxide permittivity and thickness. Since this last has been extracted from SEM images, the former is varied in order to fit the sub-threshold curve in semi-logarithmic scale. A first check can be provided observing the slope of the characteristic, which exclusively depends on the oxide thickness. To determine the threshold voltage an iterative procedure is adopted where the Silicon/Oxide interface charge density is varied. Eq.(1.46) highlights as the collector current, in pinch-off region, is mainly governed by the electron mobility in the channel and the gain of vertical PNP structure, the latter mainly dependent on minority carriers lifetime. For this reason, the holes value of each parameter has been kept at its default value. To fit the experimental the I_C-V_{GE} characteristic, only the electron value of the following parameters have been changed: N_0 in the eq.(1.102) and β in eq.(1.106) have been considered to calibrate the temperature dependence. In [68] has been pointed out as a dominant energy level (E_{trap}) regulates the recombination rate, because of the power silicon devices mainly work at high injection levels of the minority carriers. Equations (1.47), (1.51) and (1.52) show as the on-state voltage drop are strongly governed by the minority carriers lifetime. Therefore, τ_{p0} and τ_{n0} in eq.(1.118) are chosen to regulate the voltage drop of the Drift layer (V_{NB}), but it also affects the threshold voltage. From the literature [54] the ratio between τ_{p0} and τ_{n0} is regulated by capture cross section σ_n and σ_p. The doping dependence of the minority carrier lifetime is calibrated through the parameter N_{Ref} in eq.(1.118) To estimate the global lifetime of the structure and evaluate the temperature dependence of the lifetime (parameter in C in eq.(1.119)), experimental measurements of ILS have been led on the device. This approach will be treated in the following. As reported in eq.(1.50), the on-state voltage drop can be considered formed by three contributions. The contribution due to the Collector/Buffer junction affects the voltage drop at low current (low injection). Even if the doping profile of the back part of the device are extracted by SRP data and process emulation, a further calibration of the Collector peak concentration and junction depth has been needed to fit the experimental curves. The leakage current at V_{GE} = 0V is achieved considering $E_{trap} = (E_t - E_i) =$

= -0.2 eV. E_{trap} is the distance between the intrinsic Fermi level and the trap level within the bandgap [59]. The threshold voltage has been calibrated by means of a Silicon/Oxide interface charge density of $1.7x10^{11}$ cm^{-2}. The calibrated and experimental characteristics are reported in Figure 3.9. To fit the measured chrematistics a contact resistance of 0.75 mΩ has been taken into account.

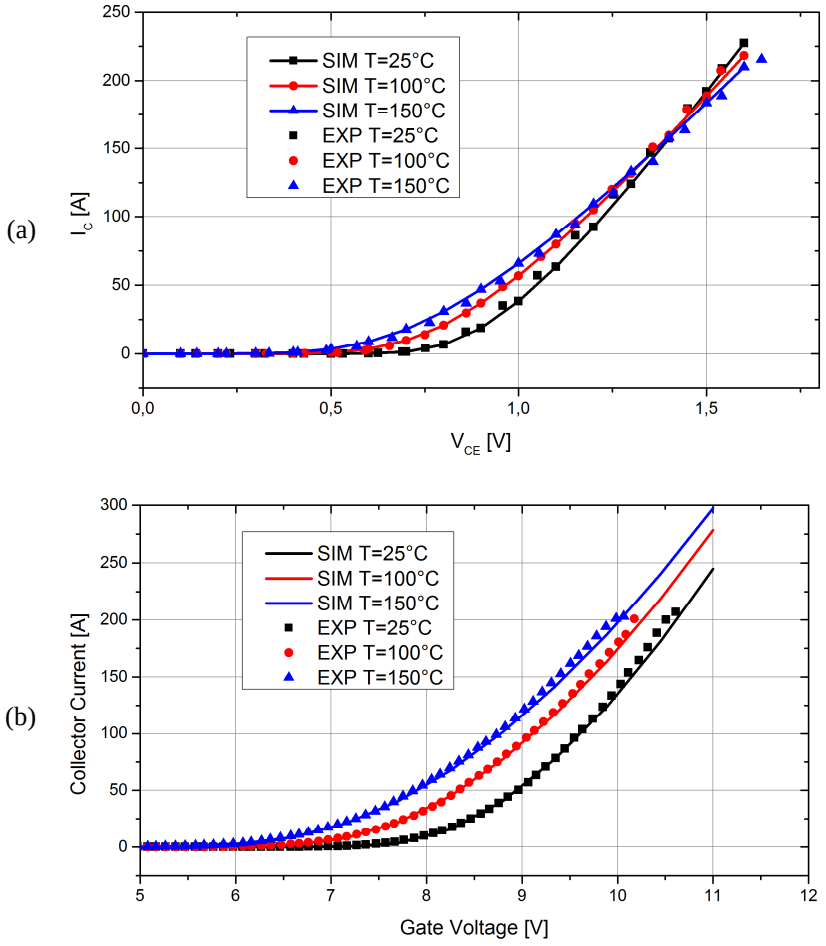


Figure 3.9. Simulated and measured terminal curves after calibration for the FS-IGBT: (a) I_C-V_{CE} characteristic; (b) I_G-V_{CE} characteristic.

The Short-Circuit condition takes place when the device is turned-on in absence of a Load and the whole battery voltage insists across the

device. When the device turn-on, the current through the device reaches its saturation value and a great amount of energy is dissipated within the device during the pulse duration T_W:

$$E_{SC} = \int_0^{T_W} I_C \cdot V_{CE} dt \tag{3.2}$$

The Short-Circuit capability t_{ON} can be defined as temporal time occurring from the Gate pulse starting time to the failure moment. In Figure 3.10 are depicted the typical Short-Circuit waveforms for an IGBT device. During the t_{ON}, the Collector current exhibits a negative slope due to mobility reduction into the channel. Prior to reach the failure moment at the t_{ON} time, the current tends to rise because of the thermal latch-up.

Experimental measurements under Short-Circuit condition have been carried out on the analyzed device. A reduced Collector voltage has been applied in order to evaluate the saturation current without triggering the failure. A first measure realized with V V_{GE} = 13V and V_{CE} = 150V has provided more accurate results as visible in Figure 3.11(a). The saturation current remains quite constant between 15 µm and 20 µm, and can be estimated as about 680A. The second measure is led at higher saturation current with V_{GE} = 15V and V_{CE} = 150V (Figure 3.11(b)). Nevertheless, a lower accuracy is achieved due to the saturation of the current probe. The saturation current seems to be around 1100A. Even if not destructive, the two measures serve to comprehend if the elementary cell is well calibrated. In Figure 3.12 are shown the Short-Circuit simulation waveforms of the calibrated structure. An acceptable agreement with the experimental ones is achieved since the main focus of the work is on evaluating the influence of design on the Short-Circuit capability.

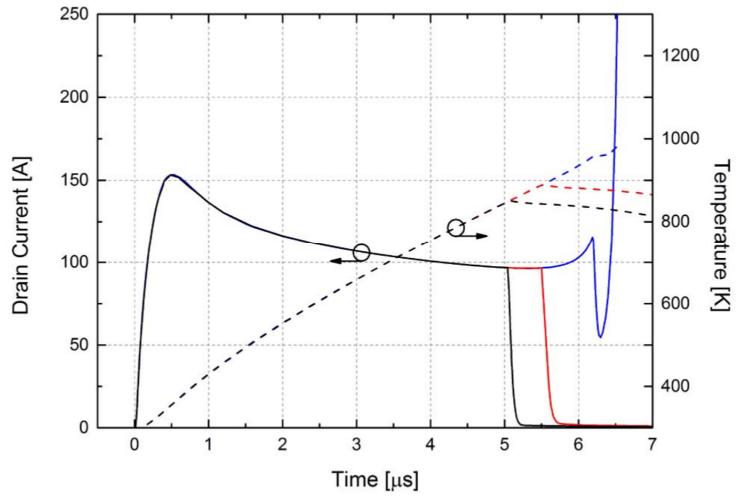
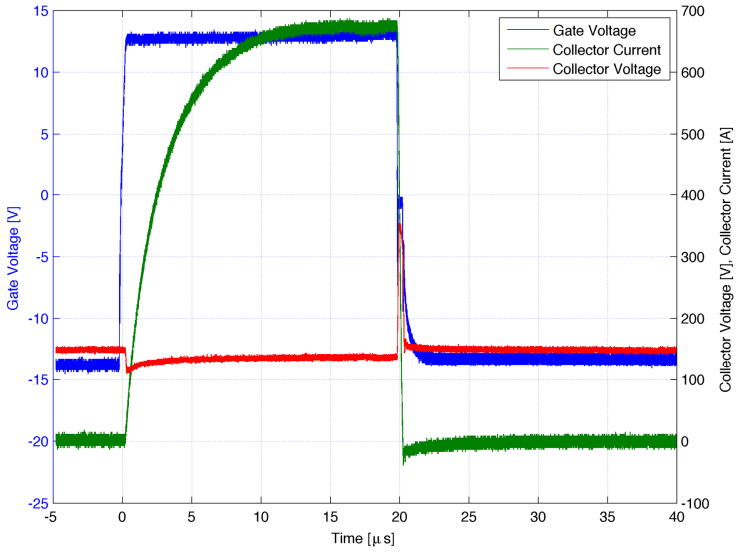


Figure 3.10. Simulation of typical Collector current and surface temperature during the Short-Circuit at different duration times.

(a)



(b)

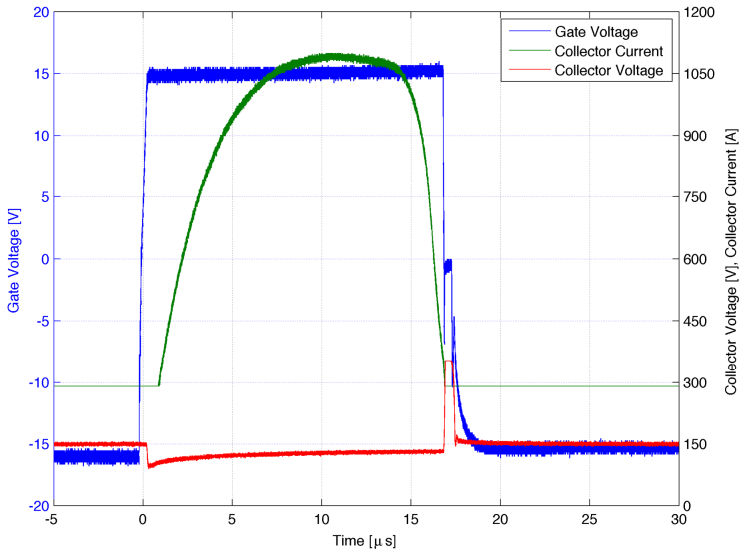


Figure 3.11. No fail Short-Circuit measures on the analyzed device for: (a) V_{GE}=13V and V_{CE}=150; (b) V_{GE}=15V and V_{CE}=150V.

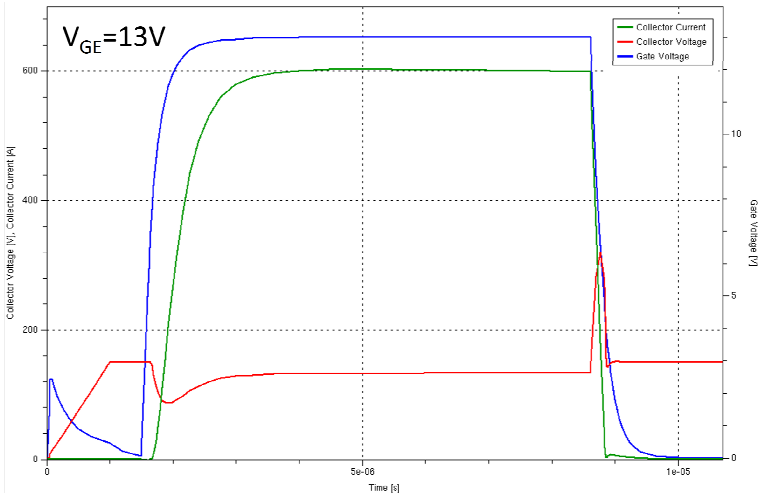


Figure 3.12. Simulation Short-Circuit waveforms of the calibrated elementary cell.

3.3 Design proposals

From the previous analysis it has pointed out as the Short-Circuit capability can be mainly addressed to the saturation current of the device. The Emitter diffusion modulation has been presented as possible improvement to reduce the saturation current. With the same scope, a further design modification is proposed in this section. It is based on the control of the spatial distribution of the elementary cells along the Emitter modulation direction. The saturation of the device can be essentially addressed to current contribution of the MOSFET channel. As visible in Figure 3.13, in presence of the Emitter modulation the physical channel is not confined below N^+-Emitter diffusion because of the lateral spreading of the electrons. The latter has a finite size, since the diffusion length of the carriers governs the phenomenon. Actually, if the not modulated P-body portion (L_{NM}) is too tight, the lateral spread of the electron tends to completely fill this area and the saturation current is insensitive to the variations of L_{NM}.

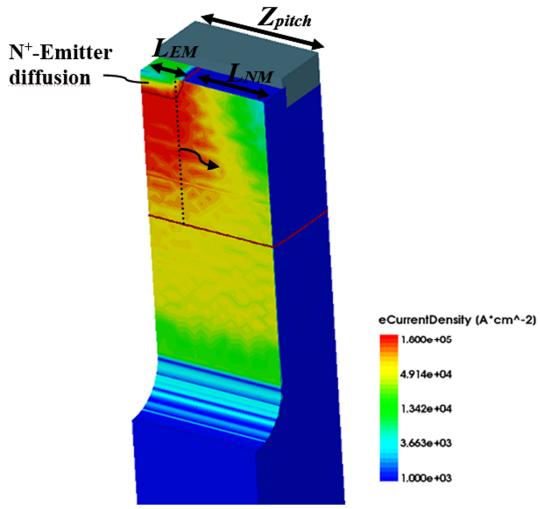


Figure 3.13. Electron current density distribution along the Emitter modulation direction of the elementary cell.

The idea is to evaluate the influence of the spatial separation (Z_{pitch}) between the cells along the z-axis on the saturation current. Defining L_{EM} as the length of the Emitter diffusion along the z-axis, the analysis is led considering an Emitter modulation at 50%, i.e. for $L_{NM} = L_{EM}$.. The proposed structures are illustrated in Figure 3.14. The aspect ratio along the z-axis is increased as follows $Z_{p1} : 0.5 \cdot Z_{p2} : 0.25 \cdot Z_{p3}$.

- **STR1** is the actual calibrated elementary cell.
- **STR2** has Z_{pitch} double respect to STR1.
- **STR3** has Z_{pitch} quadruple respect to STR1.

The Area Factor of the elementary cell is scaled inversely proportional respect to the aspect ratio. The same grid mesh is adopted for each structure in order to guarantee the results are not affected by numerical errors. This can be demonstrated considering the static characteristics in Figure 3.15, which show, as the threshold voltage remains equal for three structures.

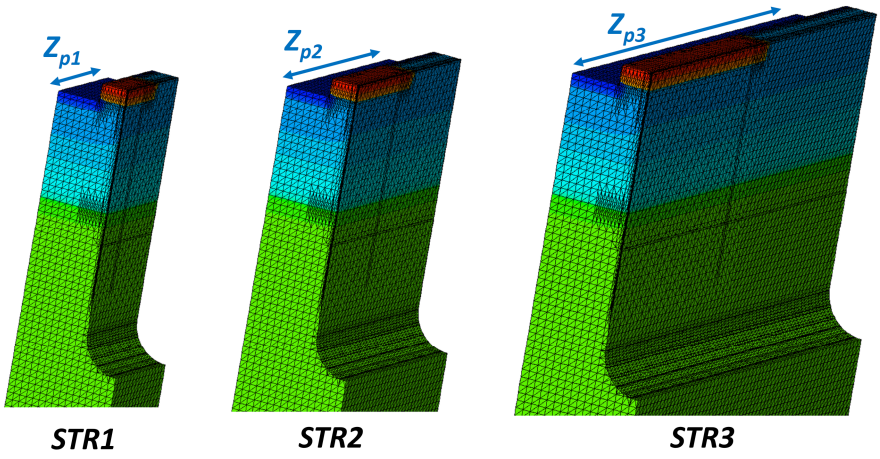
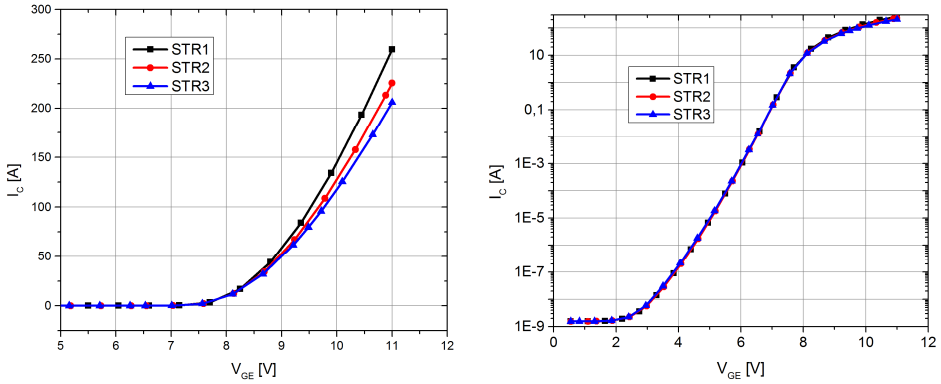


Figure 3.14. 3D proposed design.



(a) (b)

Figure 3.15. (a) I_C-V_{GE} characteristic and (b) sub-threshold curves of the proposed structures.

Short-Circuit simulations have been performed for the proposed structures at both ambient temperature and T=150°C (Figure 3.16). The results confirm a great reduction of the collector current with increasing of the Z_{pitch}, which produces as effect an increase of the Short-Circuit capability. It can be noted as the collector current diminution is not proportional to the incremental factor of the cell dimension. Because of the lateral spreading of the electron tends to saturate its effect. Remembering that the modulation has been kept at the 50%, it can deduce as strong control of the saturation current can be practiced by controlling both the Emitter diffusion modulation and the spatial transversal distance among the cells.

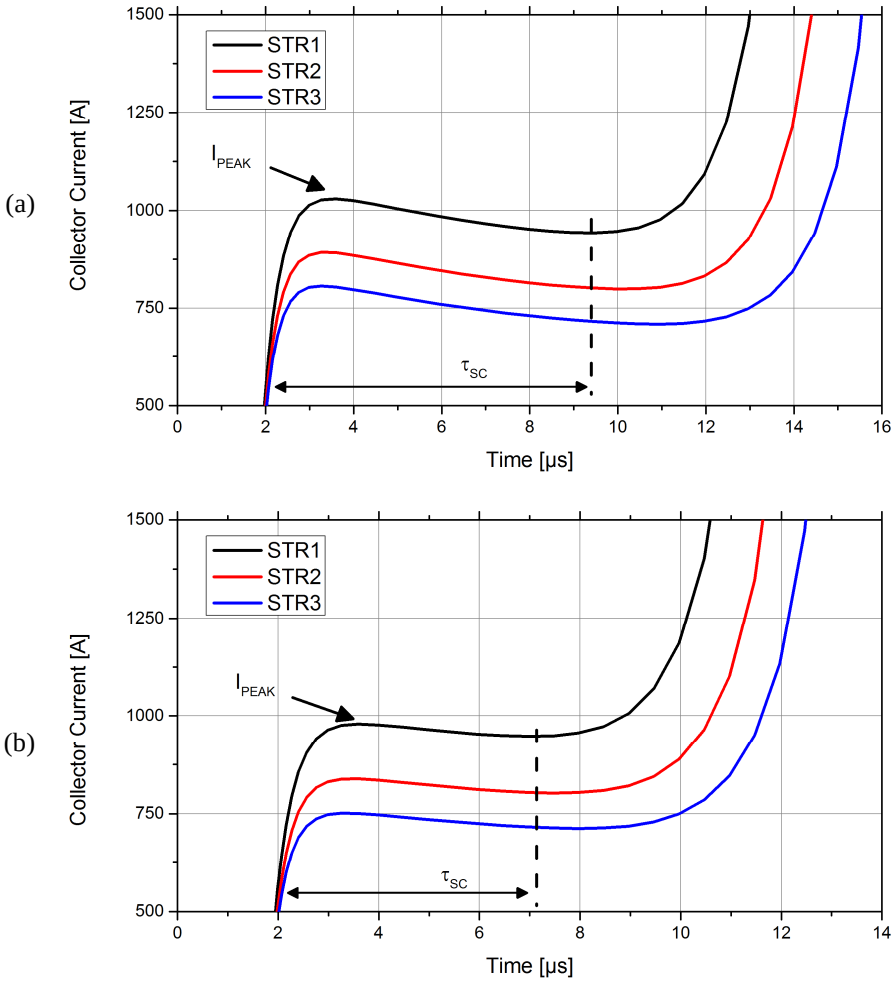


Figure 3.16. Short-Circuit simulations for the proposed structure at different temperature: (a) T = 25°C; (b) T = 150°C.

Finally, the results achieved on the proposed structures are summarized in Table 3.3.

Table 3.3. Short-Circuit results comparison of the proposed structures.

Design	***Ipeak* [A]** **at T=25°C** **at T=150°C**	**V_{ON} [V]** **(at 200A)** **at T=25°C** **at T=150°C**	**τ_{SC} [µs]** **at T=25°C** **at T=150°C**
STR1	1030 979	1.515 1.557	7.8 5.3
STR2	892 838	1.552 1.608	8.5 5.8
STR3	806 750	1.601 1.682	8.7 6.3

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Appendix A

Study and simulation of the state-of-art RC-IGBT devices

In the context of the study of the more modern and innovative power semiconductor devices, part of my research activity was addressed to a new power device named Reverse Conducting (RC)-IGBT. Introduced on market in recent years, the RC-IGBT concept is based on integrating both IGBT and Free-Wheeling Diode (FWD) in a unique monolithic block [1]-[4]. In this mode, the RC-IGBT has the advantages deriving by the state-of-art of IGBT and FWD enclosed in a more compact module able to reduce size and cost, guaranteeing also a reduced thermal ripple [5]-[7]. RC-IGBT is mainly employed in medium voltage regime (600V-1200V) operating at low current in Soft-Switching applications. Due to the generation of extra-voltage during the turn-off and extra-current during the turn-on, the operating in Hard-Switching mode is possible only in limited applications without overcome the SOA limits Figure A.1) [1][5][8].

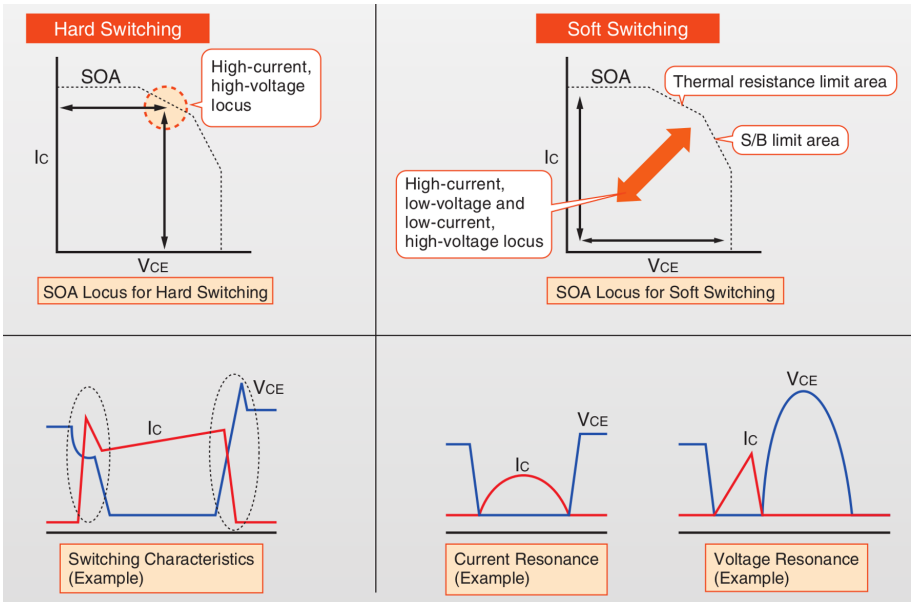


Figure A.1. Comparison between Hard and Soft Switching operating mode of a RC-IGBT device.

In principle, RC-IGBT is achieved as modification of an IGBT device making a series of P/N layout design at the collector backside. Nevertheless, the difficulty of the IGBT mode to fastly approach in conductivity modulation regime has introduced the necessity to adopt a different configuration. As visible in Figure A.2, the device is realized as a hybrid version of an RC-IGBT and an IGBT (Pilot area), where the latter must guarantee the suppression of the snap-back phenomenon [9][10]. One of the main aspects of this technology regards the conflict between the IGBT and FWD performances. The former requires a plasma enhancement near the Emitter/Cathode IGBT to reduce on-state drop and suppress the snap-back, while the latter requires a plasma reduction for a better reverse recovery. Usually, localized lifetime killing techniques are applied to improve the behavior of both IGBT and FWD modes. Another sensitive aspect regards the alignment of the P and N (Short Anode) regions at the backside to minimize the uneven distributions of charge.

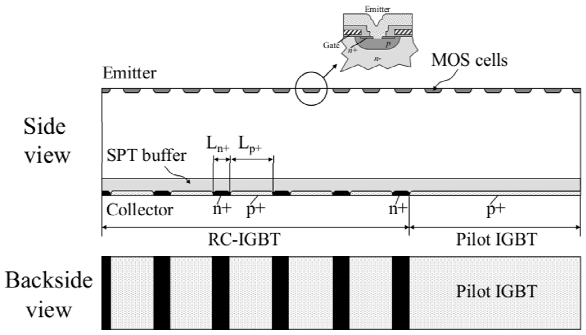


Figure A.2. Geometry of a hybrid RC-IGBT and Pilot IGBT.

Even if the Pilot IGBT offers the possibility to suppress the Snap-back, the presence of the Short Anodes introduces several secondary snapbacks as illustrated in Figure A.3. This is because the transition in bipolar operation occurs when the voltage drop across the Short Anode and Buffer junction overcomes the built-in voltage [11]. This aspect can be appreciate observing FigureA.4, where the holy density distribution is shown during the current increasing. Anyway, the secondary Snap-back can be eliminated using a radial approach of the Short Anodes layout [12].

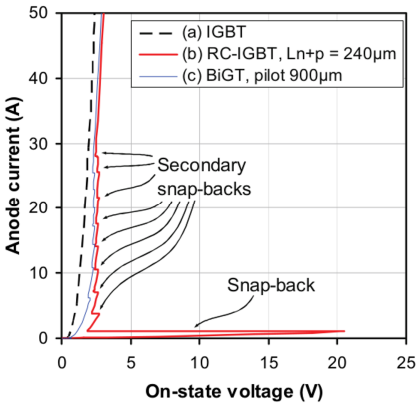


Figure A.3. Simulated typical on-state characteristic comparing IGBT (trace (a)), RC-IGBT (trace (b)) and Hybrid RC-IGBT (trace (c)).

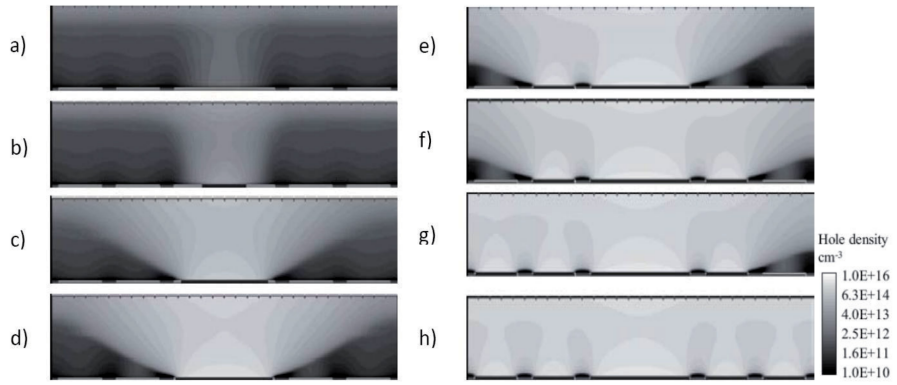


Figure A.4. Hole density distribution in a hybrid RC-IGBT and IGBT device. From *a* to *h* the current density in rising. The Pilot IGBT is located at the center in these images.

It is now provided an analytical analysis on the suppression mechanism of the Snap-back phenomenon [13]. When the Anode is biased, the electron current flowing from the N^+ Short Anode to the Drift region passing through the Buffer layer. The resistivity of this last produces a voltage drop V_{NM} between the two points *M* and *N* indicated in Figure A.5. When the voltage drop between the Anode and M (V_{AM}) becomes higher than the built-in voltage of the P-emitter/N-buffer junction, the holes starts to flow into the Drift layer leading to the conductivity modulation of the region. The voltage at the point M can be seen as:

$$V_M = V_{b-i} + V_{Drift} \tag{A.3}$$

In conductivity modulation: $V_M \sim V_{b-i}$.

The Snap-back voltage V_{SB} due to the unipolar regime can be written:

$$V_{SB} = R_D I_0 + V_{N_{Buffer}/N^+} \tag{A.4}$$

where R_D and I_0 are the resistance and the electron current of the Drift layer, respectively. The voltage drop between the Anode and M is given by:

$$V_{AM} = V_{NM} + V_{N_{Buffer}/N^+} \tag{A.5}$$

The voltage drop across the points N and M is given by:

$$V_{NM} = \frac{LI_0}{Zq\mu_n N_D (L_p + L_n)} \tag{A.6}$$

where Z is the transversal dimension of the structure, L_p and L_n are the lengths of the P-emitter and N^+-Anode region, respectively, L and N_D are the width and doping concentration of the Drift region, respectively.
The device becomes Snap-back free when: $V_{AM} = R_D I_0$.

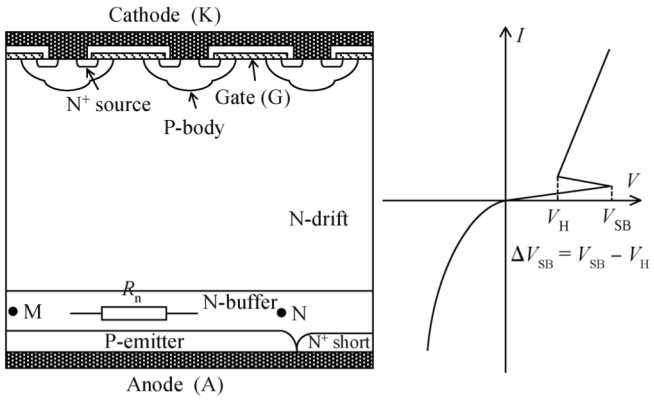


Figure A.5. Schematic of RC-IGBT basic structure.

To support the above mentioned analysis, 2D TCAD simulations have been performed. As visible in Figure A.6, the upper part of the device is achieved replicating an elementary Trench-MOSFET cell, while a Pilot IGBT area and a single Short Anode diffusion constitute the backside. During the forward conduction, the electron current transits within the Buffer from Short Anode generating a voltage drop in accordance to eq.(A.6). The aim of this analysis is to evaluate the influence of the Pilot area dimension on the Snap-back behavior. Figure A.7 illustrates the geometry and the doping profile (extracted along the lines of Figure A.6) which determine the built-in voltage drop of the N-Buffer/P-Collector junction.

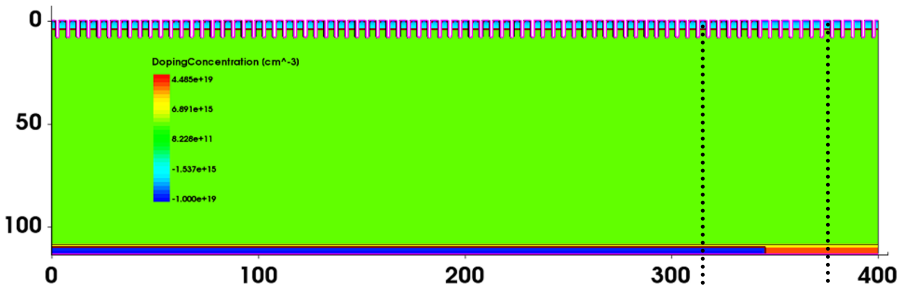


Figure A.6. TCAD RC-IGBT structure to analyze the Snap-back phenomenon.

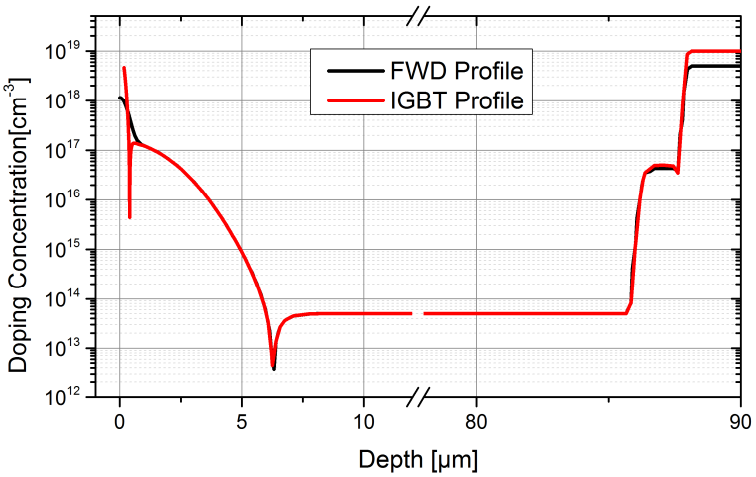


Figure A.7. Vertical doping profile of the analyzed RC-IGBT structure.

The I_C-V_{CE} simulated characteristic of the structure is shown in FigureA.8 for different ratio of the Pilot IGBT length (*Lp*) and FWD length (*Ln*). It can be seen as increasing the Pilot area extension the occurring Snap-back decreases, since the longitudinal extension L_P directly affects the resistance of the Buffer layer on the IGBT side. If the Pilot area is large enough, the bipolar regime rapidly takes place and the on-state characteristic becomes Snap-back free.

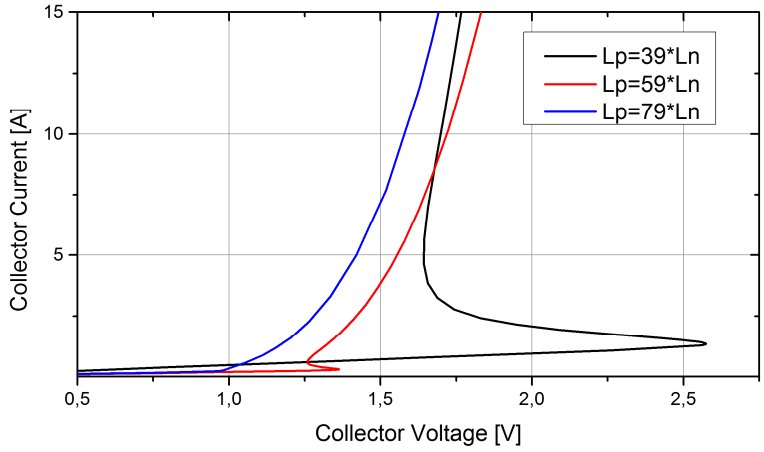
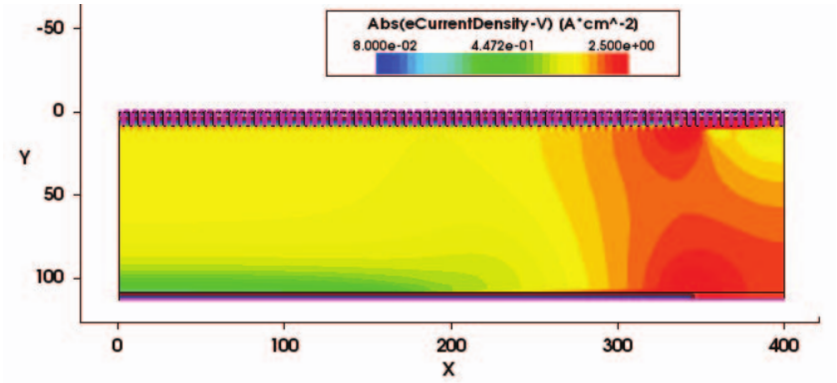


Figure A.8. Simulated I-V output characteristic for different dimensions of the Pilot IGBT.

The inductive turn-on behavior is investigated for a multicellular structure Snap-back free, whose design parameters are reported in Table A.1. The electron current distribution is depicted in Figure A.9 for three instant time. It highlights as the turn-on dynamic is strongly affected the 2D behavior. Indeed, the electron distribution startlingly spread from the Diode side (Short Anode) in both vertical and lateral direction. Due to the symmetry of the boundary conditions, the structure starts operating in bipolar condition to the left of the IGBT area (X=0). At the P-Collector/N-Anode interface, the electron distribution is influenced by the presence of the antiparallel FWD.

(a)



(b)

(c)

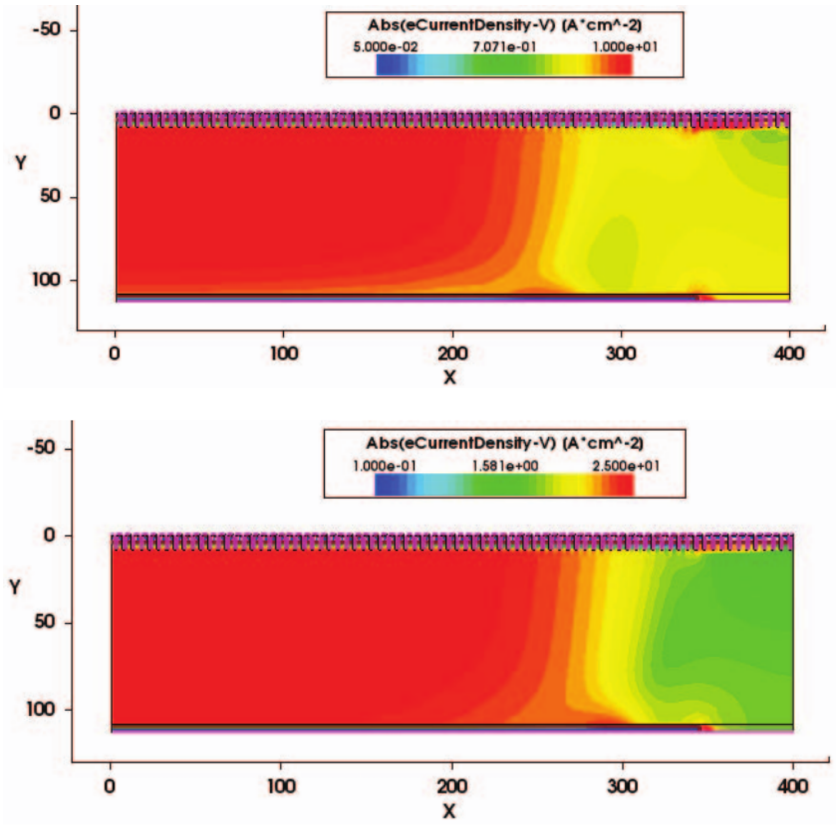


Figure A.9. Electron current distribution during the inductive turn-on simulation of a RC-IGBT at t = 0.5 µs (a); t = 1 µs(b); t = 1.5 µs (c).

Table A.1. RC-IGBT structure parameters for TCAD simulations.

Symbol	***Quantity***	***Value***
L	Total length	400 µm
L_p	IGBT length	345 µm
L_n	FWD length	55 µm
W	Epi-layer thickness	100 µm
W_B	Buffer thickness	1,5 µm
N_{Epi}	Epi-layer doping concentration	$1x10^{14}$ cm^{-3}
N_B	Buffer doping concentration	$5x10^{16}$ cm^{-3}
Pt	Cell pitch	5 µm

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