A 1.8 pJ/b, 12.5–25 Gb/s Wide Range All-Digital Clock and Data Recovery Circuit

Marijn Verbeke, Pieter Rombouts, Hannes Ramon, Bart Moeneclaey, Xin Yin, Johan Bauwelinck, and Guy Torfs

***Abstract*—Recently, there has been a strong drive to replace established analog circuits for multi-gigabit Clock and Data Recovery (CDR) by more digital solutions. We focused on PLL-based All-Digital CDR (AD-CDR) techniques which contain a Digital Loop Filter (DLF) and a Digital Controlled Oscillator (DCO) and pushed the digital integration up to a level where our DLF is entirely synthesized. To enable this, we found that extensive subsampling can be used to decrease the speed of the DLF while maintaining a good operation. Additionally, an Inverse Alexander phase detector and a 5.5-bit resolution DCO complete the AD-CDR architecture. As a result of the low-complexity and digital architecture, the AD-CDR occupies a compact active chip area of 0.050mm^2 and consumes only 46mW at 25Gb/s. This is the smallest area and lowest power consumption compared to the state-of-the-art. In addition, our implementation is highly tunable due to the synthesized logic and supports a wide operating range (12.5Gb/s-25Gb/s), which is a significantly larger range compared to previous work. Finally, thanks to our digital architecture the power dissipation decreases linearly while moving to the lower speeds of our operating range. This is in contrast with most prior work, making our design truly adaptive.**

***Index Terms*—All-Digital Clock and Data Recovery (AD-CDR), Inverse Alexander Phase Detector, Digital Loop Filter (DLF), Digital Controlled Oscillator (DCO), subsampling, synthesis.**

I. Introduction

In multi-gigabit data communication links, the data is serially transmitted to the receiver without any accompanying clock. This clock has to be recovered at the receiver side in order to sample and process the received data. Therefore, a Clock and Data Recovery (CDR) circuit is an essential component in such a high speed receiver, and the design and the performance of the CDR has a significant influence on the overall operation of the link [1].

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The need for low cost and high integration mandates that the CDR should be implemented in a deep-submicron technology. However, it is hard to achieve high performance for classical analog CDRs in today's modern technologies [2]. Therefore, digital CDRs have become increasingly important for high-speed data communication. A digital CDR eliminates the need for a large loop filter capacitor used in classical analog CDRs. Instead, a digital CDR uses a compact digital loop filter which can realize large time-constants without any additional cost in area. Additionally, a digital loop filter is tolerant to process, voltage and temperature variations and is noise insensitive. The filter is also easily scalable, portable across CMOS technologies and highly adaptable. Therefore, a digital CDR is the optimal choice for a high speed receiver implemented in a deep-submicron technology and has been a major area of research interest in recent years [2]–[12].

We focus on a subset of these digital CDRs, i.e. so-called All-Digital Clock and Data Recovery (AD-CDR) circuits. AD-CDRs are derived from the first All-Digital Phase Locked Loop (AD-PLL) introduced in [13] and comprise a phase detector and a digital controlled oscillator in addition to a digital loop filter [2]–[4], [14]–[18]. PLL-based CDR circuits have the advantage over alternative digital friendly CDRs that they have intrinsically a wide frequency capture range due to the ability to adapt both phase and frequency [19]. Additionally, they benefit from a wide bandwidth and have the ability to reject input jitter [20].

The only problem is that the digital loop filter, which consists of a proportional and an integral path, typically cannot operate at the tens of Gb/s data rate. In prior work, the speed of the integral path of the digital loop filter is reduced by using demultiplexing [2], [18] or subsampling [3], [21]. However, the proportional path still runs at a high speed and due to this, these blocks had to be designed and laid out by hand, largely counteracting the advantages of a digital design which ultimately should allow automatic synthesis.

There is only one very recent related work [4] where the digital block is entirely synthesized. To accommodate this synthesis, the input of the digital loop is heavily demultiplexed into many parallel lanes but this has disadvantages: a large amount of parallel samplers are needed to process the high-speed data input and this in turn requires a considerable clock distribution network. Moreover, the huge amount of samples has to be processed by a complex signal processing block. This increases the power consumption and chip area: e.g. the work in [4], which includes a CTLE and a DFE, has an area which is 10 times larger than our work. Additionally, the power consumption per bit is more than 75 % higher than our work.

In this work, we use extensive subsampling [22] instead of demultiplexing to reduce the operating speed of the entire digital loop filter. This enables us to push the digital integration up to a level where our digital loop filter is entirely synthesized without requiring complex signal processing. To demonstrate the correct operation, we implemented a $25\,\mathrm{Gb/s}$ PLL-based all-digital clock and data recovery circuit. This AD-CDR features an Inverse Alexander phase detector which is low-power, simple, fast and accurate. In particular, this phase detector shows improved performance in simulations over the conventional Alexander phase detector when subsampling is used [23]. In this work, we complement the earlier theoretical work by presenting the first experimental verification of this Inverse Alexander phase detector. The last building block of the AD-CDR is a low-resolution digital controlled ring oscillator. We demonstrate that a resolution as low as 5.5 bit can be used without degrading the performance of the AD-CDR.

Thanks to the highly digital architecture, the active die area is very compact and only occupies $0.050\,\mathrm{mm}^2$ which is significantly smaller than competing work [2]–[11]. Moreover, the power efficiency of the CDR core is 1.8 pJ/b which is also better than the state-of-the-art [2]–[11]. Additionally, the AD-CDR is highly adaptable: i.e. the characteristics of the loop filter can be tuned to satisfy multiple jitter tolerance specifications. Moreover, the operating range can be varied from 12.5 Gb/s to 25 Gb/s, which is the broadest operation range of any digital CDR that does not use a high-quality, multi-gigahertz reference clock. Due to the truly digital frequency adaptable nature, the power consumption decreases linearly with the operating data rate. This means that when the data rate is reduced, also the power consumption goes down accordingly and hence an excellent power efficiency is maintained over the entire operating range: e.g. at 25 Gb/s the power consumption is 46 mW while at 12.5 Gb/s this is 23 mW.

The remainder of the paper is organized as follows. Section II presents the used AD-CDR architecture. In section III the detailed circuit implementation in a $40\,\mathrm{nm}$ Low Power CMOS process is discussed. The experimental results of our $12.5\,\mathrm{Gb/s}$ to $25\,\mathrm{Gb/s}$ AD-CDR circuit are summarized in Section IV, and Section V concludes the paper.

II. All-Digital Clock and Data Recovery Architecture

The overall architecture of our AD-CDR architecture is shown in Fig. 1. It consists of a Bang-Bang Phase Detector (BB-PD), a subsampler, a Digital Loop Filter (DLF) and a Digital Controlled Oscillator (DCO). The BB-PD determines the phase difference between edges in the input data stream (D_{in}) and the recovered clock (Clk) signal. When the clock is leading the input data, an $Early$ signal is generated to decrease the frequency of the recovered clock. Alternatively, when the clock is lagging, the BB-PD outputs a $Late$ signal to increase the frequency of the recovered clock. These $Early$ and $Late$ signals are subsampled by a factor of N and then filtered by the Digital Loop Filter (DLF). The resulting signal controls the DCO such that the phase error is reduced. Note that if no data transition occurs, the BB-PD cannot determine if the clock leads or lags the data and therefore does not generate any signal. Consequently, the DCO is not adjusted.

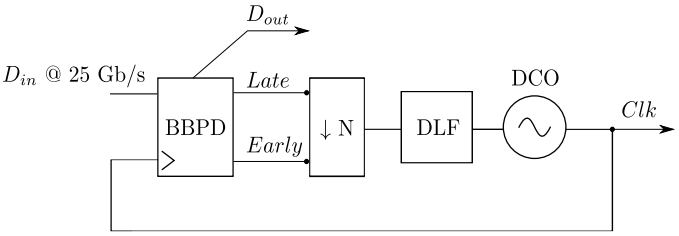


Fig. 1. AD-CDR architecture

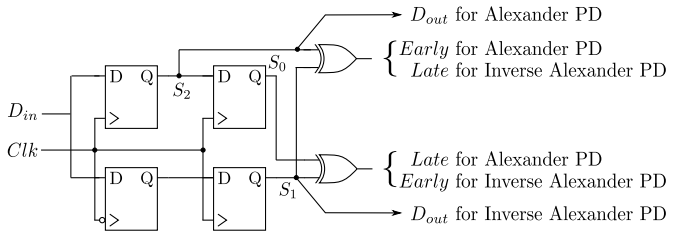


Fig. 2. Basic block diagram of the conventional Alexander PD and Inverse Alexander PD [23].

A. Bang-Bang Phase Detector

Alexander bang-bang phase detectors are typically used in high-speed CDR circuits because they provide simplicity in design, good phase adjustment and can work at high speeds [24]. Additionally, these BB-PDs have the advantage that the output is already digital, making this type of Phase Detector (PD) very suitable to drive the Digital Loop Filter.

Recently, the Inverse Alexander phase detector was proposed as an improvement over this established and well-known circuit [23]. An elaborate comparison between the conventional and Inverse Alexander phase detector is given below.

1) Comparison of Alexander and Inverse Alexander PD: The conventional Alexander phase detection is based on three successive data samples which are sampled at twice the data clock frequency. In the basic block diagram illustrated by Fig. 2, this is done by sampling the data both on the rising and the falling edges of the recovered clock Clk. By monitoring the differences between the three sampled values, it can be detected whether a data edge has occurred and if this data edge occurs before or after the corresponding clock edge. For the actual phase detection, the 3 successive samples, available at nodes S_0, S_1 and S_2 are used. To understand the operation, 3 possible waveforms are considered in Fig. 3. First, the ideal locking condition is shown in Fig. 3(a). In this case, the value of sample S_1 is undefined and in practice due to noise the PD will randomly produce an *Early* or a *Late* pulse. Fig. 3(b) shows the case where the clock edge leads on the data edge (*Early*) and Fig. 3(c) shows the case where the clock edge lags on the date edge (*Late*). In the absence of data transitions

(not shown in the figure), all three samples S_0, S_1 and S_2 are equal and the xor gates (Fig. 2) will set both the *Early* and the *Late* signals to zero. These relations are summarized as [25]:

$$\begin{aligned} \text{Early}: S_0 \oplus S_1 = 0, \quad S_1 \oplus S_2 = 1 \quad &\rightarrow \quad \text{Clk frequency} \downarrow \\ \text{Late}: S_0 \oplus S_1 = 1, \quad S_1 \oplus S_2 = 0 \quad &\rightarrow \quad \text{Clk frequency} \uparrow \\ \text{Others}: S_0 \oplus S_1 = S_1 \oplus S_2 \quad &\rightarrow \quad \text{Do not adjust clk} \end{aligned}$$

Fig. 3(a) shows that once the CDR has settled, the samples S_0 and S_2 correspond to two successive data output (D_{out}) samples, while sample S_1 occurs at the transition of the data.

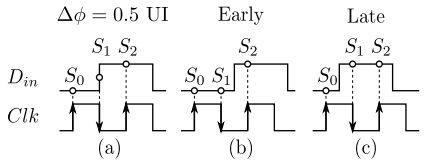


Fig. 3. Waveforms for the locking behavior of the Alexander PD: (a) Ideal locking condition with phase difference $\Delta\phi = 0.5$ UI; (b) *Early* condition; (c) *Late* condition.

The proposed Inverse Alexander PD is also shown in Fig. 2 and obviously has the same schematic as the Alexander PD, but the *Early* and the *Late* signal are interchanged, which leads to an inversion of the sign in the CDR loop:

$$\begin{aligned} \text{Early}: S_0 \oplus S_1 = 1, \quad S_1 \oplus S_2 = 0 \quad &\rightarrow \quad \text{Clk frequency} \downarrow \\ \text{Late}: S_0 \oplus S_1 = 0, \quad S_1 \oplus S_2 = 1 \quad &\rightarrow \quad \text{Clk frequency} \uparrow \\ \text{Others}: S_0 \oplus S_1 = S_1 \oplus S_2 \quad &\rightarrow \quad \text{Do not adjust clk} \end{aligned}$$

The inversion of the sign in the CDR loop causes the CDR to settle to a different equilibrium point. As shown in Fig. 4(a), the Inverse Alexander PD will align the rising edges of the clock signal with the data edges. If the rising edge of the clock leads (is *Early*), the first sample, S_0, is unequal to the last two and the clock frequency must decrease (Fig. 4(b)). Vice versa, if the rising edge of the clock lags (is *Late*), the last sample, S_2 differs from the first two and the clock frequency must increase (Fig. 4(c)). In lock, the middle sample, S_1, corresponds with the data sample D_{out} while the other sample moments S_0 and S_2 occur at the data transitions.

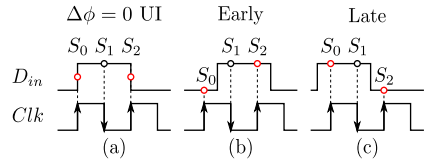


Fig. 4. Waveforms for locking behaviour of the Inverse Alexander PD: (a) Ideal locking condition with phase difference $\Delta\phi$ = 0 UI, (b) Early condition, (c) Late condition

2) PD characteristics comparison – Full-rate operation: The output characteristic of both the conventional and the Inverse Alexander phase detector are shown in Figs. 5(a)-(b). Here it is assumed that all waveforms are ideal (as in Figs. 3 and 4). If an edge occurs, either a 1-bit *Early* or *Late* pulse will be generated, which for both phase detectors results in the well known bang-bang action. For both PDs, there is only one stable locking point, which corresponds to a phase shift of half a UI (unit interval) for the conventional and to zero phase shift for the Inverse Alexander PD (also indicated on the figure).

However, in practice the waveforms are not ideal and several imperfections occur such as phase noise on the recovered clock and non-ideal input data waveforms that exhibit pulse width jitter and unequal rise and fall times, which translates to duty-cycle distortion. All these effects affect the behavior of both PDs. At full rate, the difference between the conventional and Inverse Alexander are negligible, but when the PD is subsampled, the difference becomes pronounced. To illustrate the phenomenon, we will discuss the case of duty-cycle distortion (DCD).

DCD means that the duration of a logic-0 differs from the duration of a logic-1 [26]. The notations T_0 and T_1 are used to represent respectively the duration of an occurrence of a single logic-0 and a single logic-1 affected by DCD; where the sum of T_0 and T_1 always equals 2 UI. Note that when T_1 equals 1 UI, there is no DCD and when $T_1 < 0.5$ UI, the DCD is too large to have any useful operation of the CDR. The reciprocal case when $T_1 > T_0$, is analog. To examine the influence of DCD, the output characteristics of both PDs are determined and shown in Figs. 5(c)-(d) for the artificial case of a data stream with a single logic-1 data pulse. This means that there are two consecutive data transitions. When examining this case, it turns out that apart from the normal *Early* and *Late* cases, two anomalous states occur. The first anomalous case, shown in Fig. 6(a), occurs around the locking point of the conventional PD. Here an *Early* pulse is immediately followed by a *Late* pulse. If the phase detector is operated at full speed, this will be filtered by the lowpass loop filter and essentially translate in a net null action. The second anomalous case is shown in Fig. 6(b) and is most relevant for the Inverse Alexander variant. Both the *Early* and *Late* signal are simultaneously active. This is normally an illegal state, but in practice most loop filters (e.g. the popular charge pump [25] and also the digital loop filter used in our prototype) deal with this situation by interpreting this as a net null action.

Both these anomalous cases occur for phase errors near the equilibrium locking point and broaden the locking point into a locking region which is illustrated in Figs. 5(c)-(d). For the conventional Alexander the locking range corresponds to the *Early immediately followed by Late* case, whereas for the Inverse Alexander the locking range corresponds to the *simultaneous both Early and Late* case. Despite of this difference, both cases are almost equivalent when the PDs are operated at full rate.

3) PD characteristics comparison – Subsampled operation: When the PD is subsampled only one out of N of the PD output values is used. When we study the PD characteristics for the case of ideal waveforms we still obtain the same result as Figs. 5(a)-(b). However, in the case of DCD, the *simultaneous both Early and Late* case remains unchanged but the *Early immediately followed by Late* case is altered: since one of the 2 successive samples will be lost and since the data are not correlated to the subsampling process, either *Early* or *Late* will be randomly selected as shown in Fig. 7. This means that a significant amount of excess random jitter is injected in the loop which will increase the probability

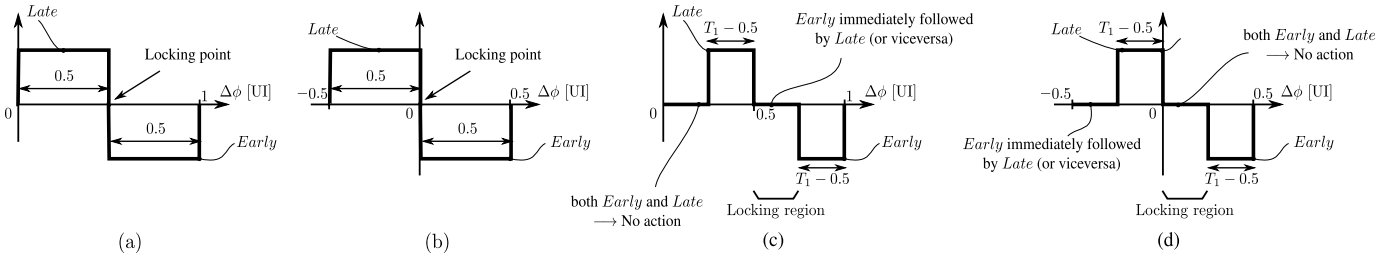


Fig. 5. Simplified (single pulse) PD output characteristics at full rate operation: (a) the Alexander PD for the case of ideal waveforms, (b) the Inverse Alexander for the case of ideal waveforms, (c) the Alexander PD for the case of duty cycle distortion and (d) the Inverse Alexander PD for the case of duty cycle distortion.

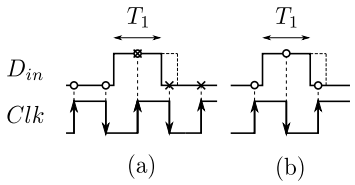


Fig. 6. PD waveforms for data with DCD corresponding to the anomalous cases (a) Alexander *Early* immediately followed by *Late* (most relevant for conventional Alexander), and (b) Simultaneous *Early* and *Late* (most relevant for Inverse Alexander)

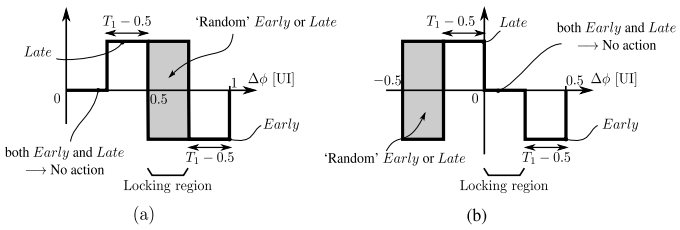


Fig. 7. Simplified (single pulse) PD output characteristics at subsampled rate operation: (a) the Alexander PD for the case of duty cycle distortion and (b) the Inverse Alexander PD for the case of duty cycle distortion.

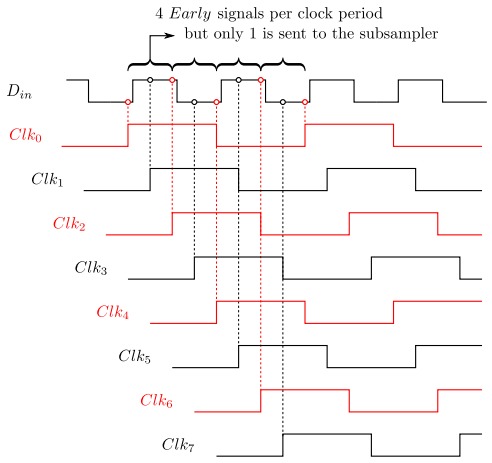


Fig. 8. Waveforms of a '1010' data sequence and the 8 clock phases when the AD-CDR is *Early*. The red clock phases correspond to edge-related samples and the black to data-related samples (as in Fig. 4).

of bit errors. This problem occurs in the locking region of the conventional Alexander PD and not for the Inverse Alexander PD. For this reason the Inverse Alexander PD is expected to have a greatly improved performance when the PD is subsampled [23]. Therefore the Inverse Alexander PD topology, proposed in [23], is chosen to implement the BB-PD.

B. Digital Controlled Oscillator

For the implementation of the DCO in our AD-CDR, a quarter-rate architecture [27] is used. This means that the DCO operates at one fourth of the data speed, and provides the required sample-time resolution in the form of 8 uniformly-phase-shifted clock phases. This can conveniently be realized by a 4-stage differential ring oscillator (see Section III-C) and significantly relaxes the requirements on the clock buffers and BB-PD circuitry. For a $25\,\mathrm{Gb/s}$ data input, this means that the DCO frequency will be $6.25\,\mathrm{GHz}$. To illustrate the quarter-rate operation, the waveforms of a '1010' data sequence and the 8 clock phases are shown in Fig. 8 for the case of an *Early* clock.

In the ideal locking condition, the even clock phases are perfectly aligned with the data edges, while the odd clock phases are in the middle of the data symbol, which is the ideal sample moment. Per clock period, there are 4 sets of three consecutive samples and each set of three consecutive samples can be used by the Inverse Alexander PD operation to generate an $Early/Late$ signal. In our design, only 1 out of these 4 $Early/Late$ signals is used: i.e. we only use clock phases Clk_0, Clk_1 and Clk_2 to gather the phase information ($Early/Late$). Of course, still all the data need to be recovered, which can be done by using the odd clock phases to sample the input data. The net result is that clock phases Clk_4 and Clk_6 are not used and that the phase information is already subsampled by a factor of 4 in the phase detector.

C. Digital Loop Filter

A typical DLF consists of a proportional and integral path and can be described by the discrete-time transfer function $H_{DLF}(z)$ given by:

$$H_{DLF}(z) = K_p \cdot z^{-D_{K_p}} + K_i \cdot \frac{z^{-D_{K_i}}}{1 - z^{-1}} \qquad (1)$$

where K_p and K_i are the respective gains of the proportional path and integral path, and D_{K_p} and D_{K_i} are the corresponding delays. In our implemented DLF, we can adapt both the proportional and integral gain setting, while the delays are hard wired. The delay in the proportional path and in the integral path are respectively $D_{K_p} = 2$ and $D_{K_i} = 9$ digital clock cycles. Especially the delay in the proportional path should be

limited in order to avoid stability issues, but with the expected jitter in the CDR loop, this delay ($D_{K_p} = 2$) is low enough to ensure its stability [28].

Note that this digital loop filter is connected directly following the subsampling block (Fig. 1) to allow automatic synthesis of the entire digital loop filter. Consequently, the proportional and integral path are equally affected by the subsampling.

D. Subsampling

In the $40\,\mathrm{nm}$ Low Power CMOS process used in this work, the maximal clock speed should not exceed $1.75\,\mathrm{GHz}$ to enable an automated design (synthesis, place and route) of this DLF. This means that, even with the subsampling by a factor of 4 that already occurs in our phase detector implementation, the operating frequency at the output of the BB-PD is still too high: e.g. if the CDR operates at $25\,\mathrm{Gb/s}$ the output of the BB-PD operates at $6.25\,\mathrm{GHz}$. Hence, this operating frequency has to be further reduced to facilitate the implementation of the DLF. Therefore, the output of the BB-PD is additionally subsampled by a factor of 4. Overall, this means that the DLF will only receive an output signal of the PD once out of every N (=16) data periods. In Fig. 1, the subsampling corresponds to the block '$\downarrow N$'.

Although a higher level of subsampling would further reduce the area and the power of the DLF, a higher subsample factor will not lead to an overall optimal power efficiency. This is because the CDR should be able to deal with data sequences where the BB-PD does not receive data edges (and hence does not generate *Early* nor *Late* signals) for many clock cycles.

In the case without subsampling, this occurs if the input data contains a long sequence of Consecutive Identical Digits (CIDs). If this happens the output of the phase detector is stuck at zero and the feedback is broken such that the CDR operates temporarily in open loop. This means that the oscillator runs freely and any frequency difference between the input data rate and the recovered clock frequency will cause a linear increase or decrease of the phase difference over time. In a prolonged open-loop situation, this phase drift will exceed a unit interval causing the AD-CDR to lose its lock, which means that the CDR operation is disrupted. For an input sequence of 'k' CIDs, the idle time of the CDR without subsampling is given by:

$$T_{idle} = \frac{k}{f_{data}} \tag{2}$$

where f_{data} corresponds to the input data rate.

To tolerate a long idle sequence, the DCO must have a sufficiently high resolution such that quantization error is small. This way, the DCO frequency will be closer to the desired input data frequency. And hence, when the loop temporarily opens due to an idle sequence, the corresponding phase drift will remain acceptable.

Another effect that lowers the maximum tolerable idle sequence is given by the random walk process of the phase of the recovered clock during open-loop operation [29]. Lowering the phase noise of the DCO will reduce this random walk process.

In the case of subsampling, the loop filter operates at lower frequency and the total idle time T_{idle} corresponding to a CID input sequence of length k will be:

$$T_{idle} = \frac{N \cdot ceil\left(\frac{k}{N}\right)}{f_{data}} \tag{3}$$

This means, that the idle time due to k CID input bits for the case with subsampling is almost equal to the case without subsampling.

However, regardless of the CIDs in the full rate input data, it can happen that after subsampling the phase detection output consists of a long idle sequence of length l (without any *Early* nor *Late* pulse). E.g. for the popular PRBS31 test sequence, it can be shown that for subsample factor that is a power of 2, there will always be an idle sequence in the subsampled PD output of lenght $l = 31$.
Now, the corresponding idle time is proportional to the subsampling factor N:

$$T_{idle} = \frac{N \cdot l}{f_{data}} \tag{4}$$

This means that the tolerance to a long idle sequence will become worse for increasing value of the subsampling factor N. To maintain adequate robustness to long idle sequences for an increasing value of the subsampling factor N, the DCO phase noise and resolution should be improved accordingly. This indicates that there is a trade-off for the subample factor N in the sense that increasing N will decrease the power consumption of the DLF but increase the required power consumption in the DCO. From behavioral simulations, we found that choosing $N = 16$ is an adequate compromise. According to simulation, with this setting, our circuit should be able to tolerate input data streams which after PD subsampling have an idle (subsampled) sequence length l of over 100.

III. Circuit Implementation

The top-level implementation of our AD-CDR is shown in Fig. 9. In our physical partitioning, we tried to maximally exploit automated digital tools. Therefore, we pushed part of the BB-PD after the subsampling such that it could also be automatically synthesized. The result is that the BB-PD and the subsampling block are intertwined. The implementation consists of 6 high-speed samplers followed by a retiming block, a subsampling block and the (automatically synthesized) 'Phase Detection Logic'. Additionally, the AD-CDR comprises an automatically synthesized digital loop filter, a clock divider and a DCO.

The 6 high-speed samplers are driven each by their own $6.25\,\mathrm{GHz}$ clock phase coming from the DCO. 4 samplers out of the 6 are used to sample the data, while the other 2 samplers are used to sample the edges. As mentioned above, 2 out of the 8 uniformly-phase-shifted DCO clock phases are not used.

In the retiming block, all the collected samples (i.e. 4 data samples and 2 edge samples) are aligned to 1 clock phase. The retimed samples of the data constitute the recovered data (the actual CDR output), while the phase information, which

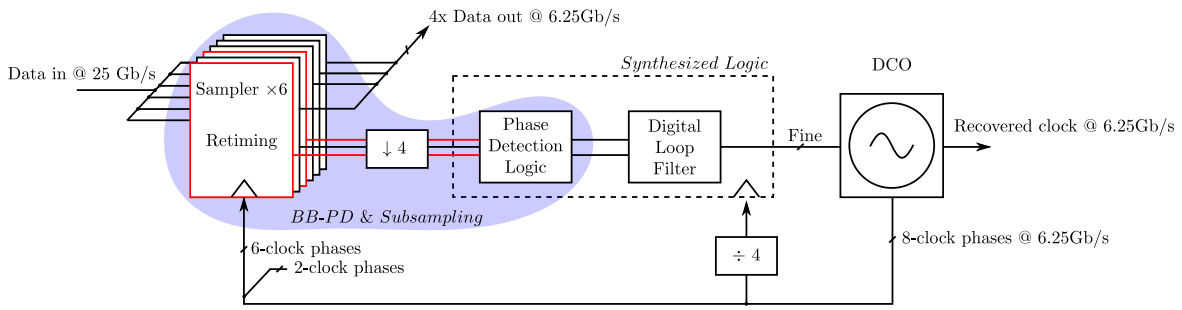


Fig. 9. Block diagram of AD-CDR implementation (speeds are indicated for 25 Gb/s operation). Red is used for edge-related samples and black for data-related samples (as in Fig. 4).

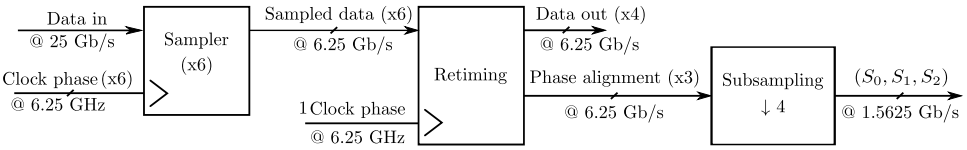


Fig. 10. Detail of the full custom part of the *BB-PD & Subsampling*, which contains 6 samplers, a retiming block and a subsampling block (speeds are indicated for 25 Gb/s operation)

adjusts the CDR to reduce the phase error, is subsampled to 1.56 Gb/s. This phase information is sent to the synthesized digital block (running at 1.56 GHz) where first, the *Phase Detection Logic* calculates the *Early* and *Late* signals. These are then further processed by the DLF which controls the quarter-rate DCO.

A. BB-PD and Subsampling

The implementation of the BB-PD & Subsampling comprises two parts: a full custom designed block and the automatically synthesized *Phase Detection logic*. A more detailed view of the full custom block consisting of the high-speed samplers, the retiming block and the subsampling block is given in Fig. 10.

1) Sampler: First, the incoming data is sampled with a high-speed sampler which is implemented as a Sense Amplifier based Flip-Flop [30]–[35]. The Sense Amplifier based Flip-Flop has a fast sense amplifier input with a short capture window followed by a slower regenerative latch (Fig. 11). This makes it an ideal choice for a subsampling stage, which needs to capture the high-speed input data very quickly, but has relaxed requirements on the clock-to-output delay. The device sizes of the Sense Amplifier based Flip-Flop shown in Fig. 11 are summarized by Table I.

TABLE I
DEVICE SIZES OF THE SENSE AMPLIFIER FLIP-FLOP SHOWN IN FIG. 11

Transistor	L	W
M0	40nm	8.4um
M1 - M4	40nm	2.4um
M5 - M6	40nm	4.8um
M7 - M10	40nm	3.6um
M11 - M12	40nm	1.2um
M13	40nm	0.6um
M14	40nm	1.2um
M15 - M16	40nm	1.8um
Invertor: pmos	40nm	2.4um
Invertor: nmos	40nm	1.2um

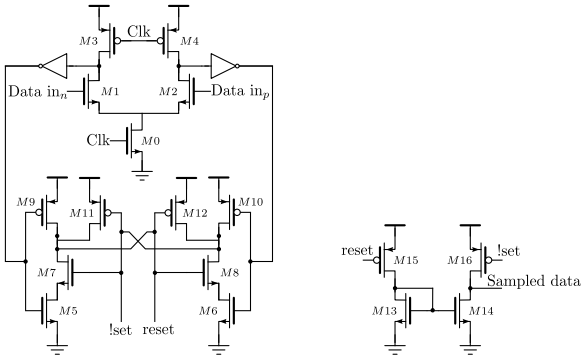


Fig. 11. Sampler circuit: Sense Amplifier based Flip-Flop with a fast sense amplifier input and a slower regenerative latch

2) Retiming: The 6 sampled data signals (4 corresponding to actual data samples and 2 corresponding to edge samples) are sent to the retiming block, which aligns the samples to one clock phase. For this, two types of dynamic flip-flops clocked with the opposite clock edge are used. The sampled input data from clock phases zero to three, is retimed by an array of positive edge triggered dynamic flip-flops of type I (Fig. 12). This is a standard dynamic flip-flop, shown in Fig. 13(a). 3 of these retimed samples that contain the information of two edges ($Edge_0$, $Edge_1$) and one intermediate data symbol (D_{out0}), are used for the phase alignment but first have to be subsampled (see below). To relax the timing requirements of the flip-flops, the sampled input data from clock phases five and seven is retimed by an array of type II (negative edge triggered) dynamic flip-flops (Fig. 12). This type is clocked with the opposite clock edge compared to type I, but an additional half clock cycle delay is incorporated (Fig. 13(b)) such that all samples are retimed to the same clock edge.

The devices sizes of the dynamic flip-flops shown in Fig. 13 are summarized by Table II.

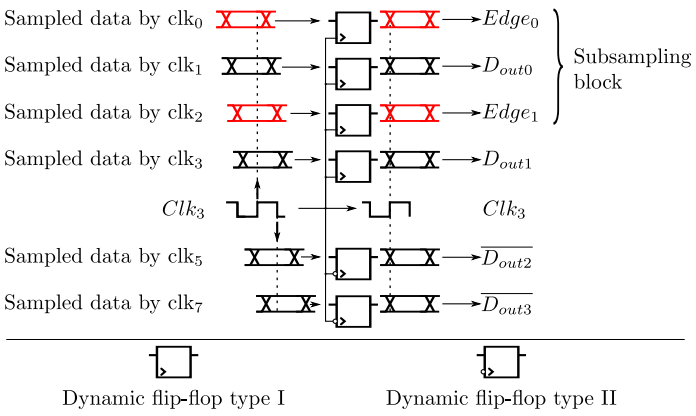


Fig. 12. Retiming circuit consisting of a array of retiming type I (postive edge triggered) flip-flops and an array of type II (negative edge triggered) flip-flops. Red is used for edge-related samples and black for data-related samples (as in Fig. 4).

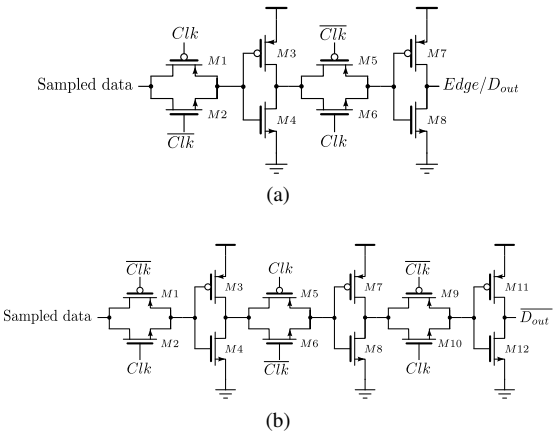


Fig. 13. Flip flops used in Retiming circuit: (a) Type I (positive edge triggered) dynamic flip-flop and (b) Type II (negative edge triggered) dynamic flip-flop

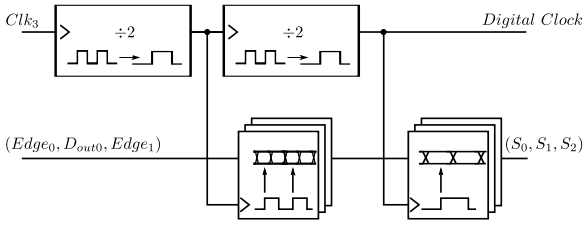


Fig. 14. Subsampling circuit

3) Subsampling: Before the phase alignment information can be sent to the digital block, this information has to be subsampled by a factor of 4 (Fig. 10). The subsampling is performed in two steps (Fig. 14), where for each step the clock frequency is first divided by two and secondly applied as clock signal to an array of three type I dynamic flip-flops. Because the input data of the flip-flops is twice the speed of the corresponding clock input, the data is subsampled by a factor of 2. Overall, the input data is thus subsampled by a factor of 4 and the clock signal is divided by 4. This divided clock is used as clock signal for the digital block.

4) Digital phase detection logic: Next to the full custom blocks, the BB-PD & Subsampler comprises the synthesized

TABLE II
DEVICE SIZES OF THE DYNAMIC FLIP-FLOPS SHOWN IN FIG. 13

Transistor	L	W
M1, M5, M9	40nm	0.6um
M2, M6, M10	40nm	0.6um
M3, M7, M11	40nm	1.2um
M4, M8, M12	40nm	0.6um

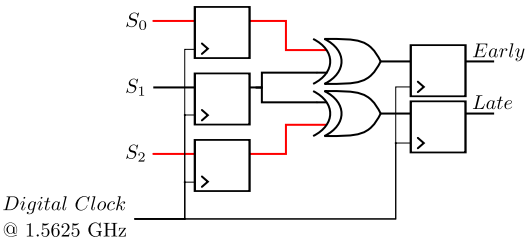


Fig. 15. Digital phase detection logic

Digital Phase Detection logic. This part is automatically generated from a Verilog description, which corresponds to the schematic shown in Fig. 15. It compares the consecutive samples and determines whether the clock leads or lags the data, according to the Inverse Alexander operation [23].

B. Digital Loop Filter

The implementation of the automatically generated DLF is shown in Fig. 16. The DLF receives an $Early/Late$ signal from the phase detection logic and this signal is then processed by a proportional and an integral path. The proportional path directly amplifies the $Early/Late$ signals with $-K_p$ and K_p, respectively. To maintain the stability of the AD-CDR, the delay in this path is minimized and the implementation is made as simple as possible. To achieve this, K_p is always an integer and the output is a 7-bit thermometer code. Now, the proportional path can simply be implemented by selecting or deselecting 'K_p' of the thermometer-coded output bits. These bits directly drive the fine-tuning input of the DCO (see section III-C). This configuration allows the gain K_p to be set between 0 and 7.

The integral path of the DLF is implemented as a multi-rate architecture. That is, a $Clk/2$-domain is created to reduce the clock speed which facilitates the implementation of the accumulator. Therefore, the $Early/Late$ signal is demuxed by a factor of 2. The internal accumulator has a high resolution of 16 bit. This allows the use of a broad range of integral gains K_i, which can be set to integer powers of 2. However, to avoid a bulky DCO design, only the 5 most significant bits of this 16 bit word are converted to a 31 bit thermometer-coded word which drives the DCO. In contrast to a binary-weighted coding, this thermometer coding increases the robustness against parasitic effects and reduces glitches when switching between states. In total, the DCO is controlled (in standard operation) by 45 (=7+7+31) bits each driving a unit varactor which corresponds to a resolution of 5.5 binary-weighted bits. Furthermore, there are some signals shown in Fig. 16 that are not used in normal operation: first there is a *'from FD'* signal, which is used in the calibration process of the DCO (see section III-D) and which can be activated by the control

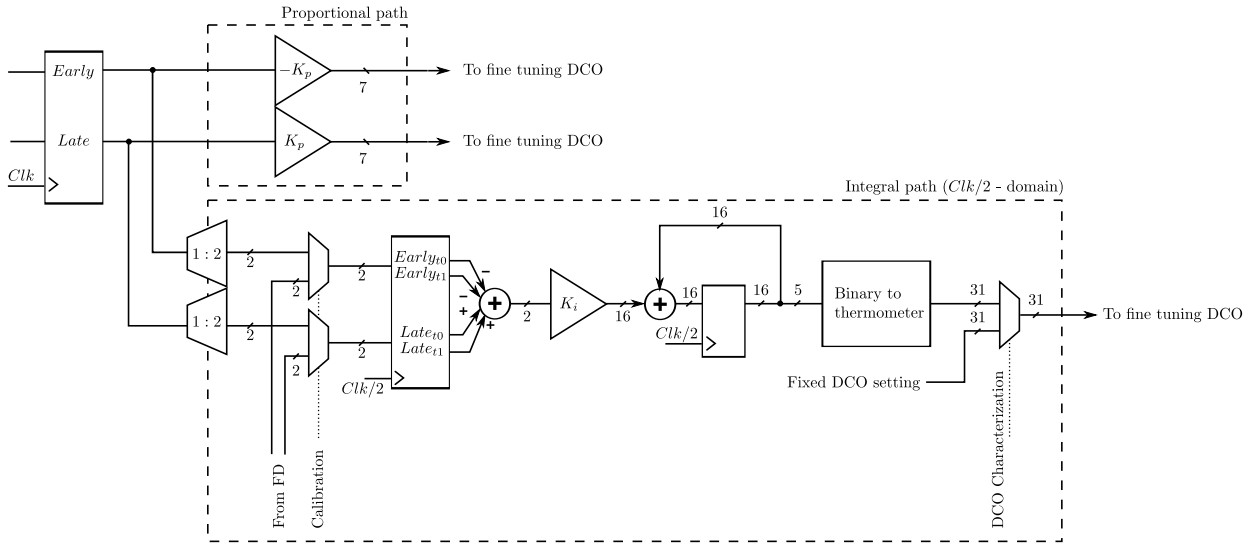


Fig. 16. Digital loop filter implementation

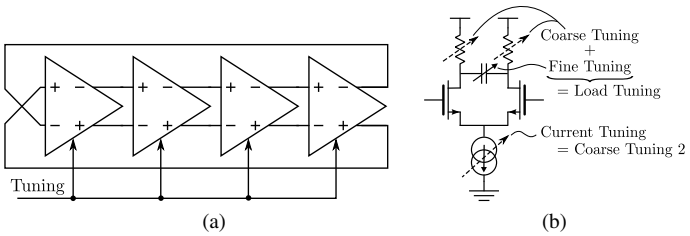


Fig. 17. DCO structure: (a) Ring oscillator and (b) Delay cell

signal *'Calibration'*. Second, there is also a *'a fixed DCO setting'* signal which is only used for debug purposes and gives the ability to characterize the DCO separately. This signal is activated by the control signal *'DCO Characterization'*.

C. Digital Controlled Oscillator

To generate the 8 uniformly-phase-shifted clock phases for the aggregated $25\,\mathrm{Gb/s}$ PD operation, the DCO is implemented as a 4-stage ring oscillator with differential delay cells (Fig. 17) [29].

The delay cell is shown in Fig. 17(b). It can be tuned by tuning the tail bias current or by tuning the load network. For the load, we distinguish a coarse tuning and a fine tuning. The coarse tuning has 6-bit resolution and is only used during calibration of the DCO (see section III-D) and is implemented by switching binary-weighted resistors on or off.

The fine tuning is done by tuning the load varactors. During normal CDR operation only this fine tuning is used. It is implemented as follows: the thermometer-coded words from the DLF (see Fig. 16) switch unit varactors on/off. To reduce the area of the ring oscillator and achieve a good resolution, the varactor units are distributed equally over the 4 delay cells. Per LSB of the fine tuning word, only one varactor is switched. However, the clock phases of the DCO have to be kept equally spaced as much as possible. Therefore, the on/off switching of the varactors is sequenced across the different delay cells: 1. toggle a varactor in the first delay cell, 2. toggle a varactor in the third delay cell, 3. toggle a varactor in the second delay cell, 4. toggle a varactor in the fourth delay cell, etc.

The tune mechanism through the tail bias current is in principle not needed, because according to simulation the entire operating range could be sufficiently covered with the load tuning alone. However, this tuning was added to achieve a larger robustness vs. process variations, such that the entire intended frequency range has sufficient coverage even under unforeseen process conditions. Here, a 4-bit current control was implemented on the chip.

D. Calibration of the DCO

Before normal AD-CDR operation, where only the fine-tuning of the DCO is adapted, the DCO frequency should first be adjusted to within about $\pm\ 30\,\mathrm{MHz}$ of the correct quarter-rate frequency of the data rate (e.g. $6.25\,\mathrm{GHz}$ for $25\,\mathrm{Gb/s}$ input data). For this, a coarse tuning of the DCO is performed in a calibration cycle at startup. This is done through an automatic frequency control loop which is based on an external reference clock and counters [2]: The frequency control loop counts the number of clock cycles of the digital clock and external reference clock. These numbers are compared with SPI configured registers and the coarse settings are then gradually adjusted. This procedure is repeated until the DCO lies within about $\pm 30\,\mathrm{MHz}$ of the correct desired frequency.

The circuit is incorporated in the synthesized digital block. The power overhead of this calibration procedure is negligible: the synthesized circuit is only based on simple counters and comparators and consumes almost no power (approximately 0.75mW).

IV. Experimental Results

The AD-CDR is fabricated in a $40\,\mathrm{nm}$ Low Power CMOS technology. The low power flavor is not favorable for a high-speed circuit, but was selected based on the available tape-outs. Unfortunately, the received samples (all from the same wafer)

were apparently from a slow process corner. This forced us to increase the DCO supply voltage to 1.15V (instead of the nominal value of 1.1V). For the BB-PD and synthesized logic we had to increase the voltage to 1.25V. All the measurements reported in this section were done with these increased supply voltages.

A photo of the fabricated chip together with an annotated layout view, is shown in Fig. 18. The chip area of the CDR core is only $0.050\,\mathrm{mm}^2$.

To test the fabricated CDR, it was wire bonded on a high-speed PCB. The input buffers of the CDR and the transmission lines on the PCB are designed for an input impedance of 50 Ω. The measurements were performed by directly connecting the measurement equipment through this PCB to the ESD protected I/O pads of the CDR.

A. Functional tests

First, basic functional tests were performed on our prototype at 3 different operating frequencies: $25\,\mathrm{Gb/s}$, $20\,\mathrm{Gb/s}$ and $12.5\,\mathrm{Gb/s}$. For this, a 2^{31}-1 pseudo random bit data sequence (PRBS31) was applied to the input of our AD-CDR. Note that with this PRBS31 test sequence, the PD output, after the 16 times subsampling that we have in our circuit, will contain idle paterns with a length l equal to 31 (see Section II-D).

At $25\,\mathrm{Gb/s}$, the CDR core without input and output buffers has a power consumption of $46\,\mathrm{mW}$ of which $11\,\mathrm{mW}$ is dissipated by the samplers, retiming block and subsampling block, $4\,\mathrm{mW}$ is consumed by the digital block and $31\,\mathrm{mW}$ is used for the DCO. The power dissipation at $20\,\mathrm{Gb/s}$ and $12.5\,\mathrm{Gb/s}$ is respectively $38\,\mathrm{mW}$ and $23\,\mathrm{mW}$.

Next a batch of Bit Error Rate (BER) measurements were performed. The full data stream is available as 4 parallel channels at quarter-rate, but due to equipment limitations, we could only do the BER measurement on 1 of the 4 channels at the same time. All the measurement reported underneath are done in this configuration. In a typical measurement the AD-CDR was operated over a time span of $15\,\mathrm{minutes}$ and the bit errors over this time frame were collected. These measurements consistently resulted in an error-free operation of the AD-CDR at $20\,\mathrm{Gb/s}$ and $12.5\,\mathrm{Gb/s}$. At $25\,\mathrm{Gb/s}$ a BER of $3.5{\cdot}10^{-13}$ was measured, well below the error correction capabilities of most applications [36]. In the remainder of this section, the performance of the DCO, the PD (including the experimental comparison of the conventional and Inverse Alexander PD) and the AD-CDR are discussed in more detail.

B. Digital Controlled Oscillator operation

The DCO can be driven independently from the other blocks. This allows to characterize the DCO for different current, coarse tuning and fine tuning settings.

In Fig. 19 the DCO frequency characteristic is shown. The x-axis represents the 6-bit resistor coarse tuning word concatenated with the 5-bit integral path fine tuning word and results in 2048 possible configurations. The measurement was repeated over multiple current settings: ranging from current setting '2' to '15' (for the lowest current settings the results were not meaningful). Fig. 19 demonstrates that the DCO

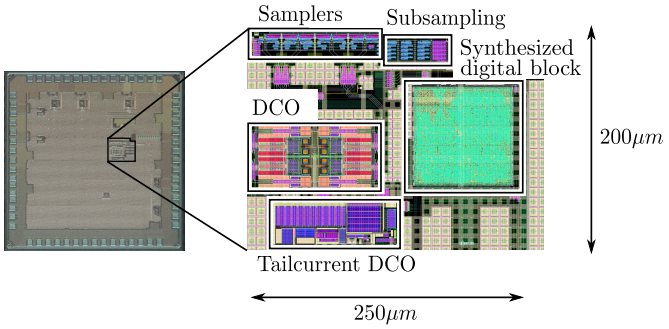


Fig. 18. Photo of the implemented chip with annotated layout view

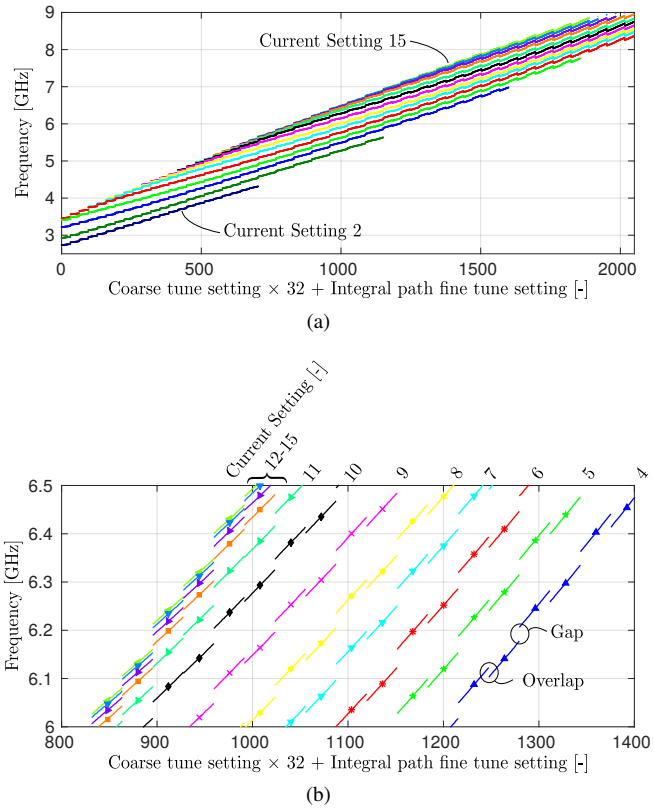


Fig. 19. Free running frequency of the DCO with (a) an overview the complete frequency range and (b) a detail around 6.25 GHz

covers a frequency range from $2.73\,\mathrm{GHz}$ to $8.95\,\mathrm{GHz}$ which corresponds to a data rate range from $10.92\,\mathrm{GHz}$ to $35.8\,\mathrm{GHz}$.

A detail of the characteristic around $6.25\,\mathrm{GHz}$, which is the quarter-rate oscillation frequency for $25\,\mathrm{Gb/s}$ input data, is shown in Fig. 19(b). In this figure the influence of the different settings is more visible: each color/symbol corresponds to different current setting. The different line segments of the same color have a different coarse tuning value and all frequency points within a separate line segment have a different fine tuning value.

The DCO was designed such that for every coarse transition, the output frequency range would overlap between the two adjacent settings. If we now focus on e.g. the rightmost (dark blue) current setting we note that this is the case for some

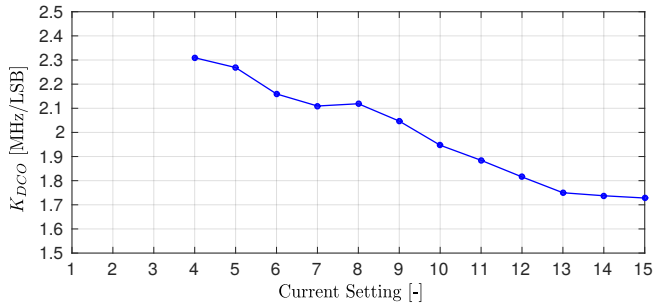


Fig. 20. The gain of the DCO K_{dco} at 6.25 GHz

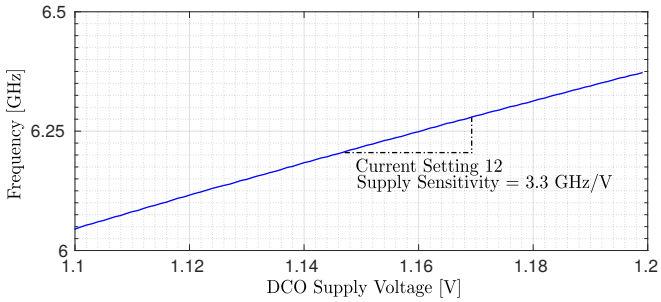


Fig. 21. Supply sensitivity at 6.25 GHz.

coarse transition. However for some coarse transitions there is an undesired frequency gap. This means that for a fixed current setting some oscillation frequencies cannot be generated by changing only the coarse and fine tuning settings. This issue arises from underestimated parasites. Fortunately, this problem was anticipated and can be circumvented by using the coarse current tuning. In this way, the desired frequency range is still completely covered.

The measured DCO gain K_{DCO} at 6.25 GHz for the different current settings is shown in Fig. 20. The figure shows that K_{DCO} is about 1.7 MHz per LSB for high current settings and that K_{DCO} increases to 2.3 MHz per LSB for lower current settings. Clearly, this means that the DCO quantization step is very rough. The measurements reported below are performed for a current setting equal to 12.

The DCO supply sensitivity at 6.25 GHz is shown in Fig. 21. Here, the supply sensitivity equals 3.3 GHz/V. Due to the high supply sensitivity, the phase noise of the DCO is degraded: e.g. at a frequency offset of 10 MHz from the carrier the measured phase noise is equal to -95 dBc/Hz (see dotted line in Fig. 25). In post-layout simulation, however, the corresponding phase noise was only -110 dBc/Hz at 10 MHz from the carrier. We attribute this deterioration to supply noise which leads to excessive phase noise due to the poor supply sensitivity.

C. Phase Detector operation

To determine the performance of the PD, the sensitivity of the samplers is measured. This sensitivity is defined as the time span in which the input data is sampled correctly by the samplers. The measurement is performed by applying an external quarter-rate clock signal together with the input data to the AD-CDR. For this measurement, a 2^7-1 pseudo random bit data sequence (PRBS7) at 25 Gb/s with a rise time of 0.25 UI is applied. The internal DCO is bypassed such that the data is sampled by the external clock. By sweeping the time difference between the external clock and the input data, we could determine the BER for each time difference and the resulting bathtub curve is shown in Fig. 22. The bathtub curve indicates that a time span of 18.8 ps out of a data period of 40 ps gives a BER below 10^{-12}.

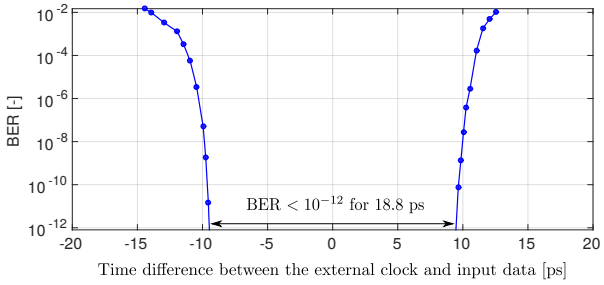


Fig. 22. Sensitivity of the PD with a PRBS7 input data at 25 Gb/s

D. Experimental comparison of the conventional and Inverse Alexander PD

To facilitate the experimental comparison between the conventional and Inverse Alexander PD, our prototype circuit was designed such that it can be configured to operate with the conventional as well as the Inverse Alexander PD. This is done by switching the sign of the control loop of the CDR in the DLF. Furthermore, the subsample factor N can be set to 16 (which is the nominal case) or to 32 (which is a test mode). For these cases comparative bit error rate (BER) measurements were performed. A 25 Gb/s PRBS7 was applied to the CDR and jitter was intentionally applied to the input data stream. For the jitter, Gaussian pseudo-white noise with a bandwidth of 80 MHz (= equipment limit) was used. The jitter level was varied and the CDR was operated over a long time until a sufficient number of bit errors were collected to obtain a reasonably accurate estimation of the bit error rate. The results are summarized in Fig. 23. In the interpretation of the curves it should be noted that at a high jitter level the CDR starts to occasionally lose synchronism (due to cycle slips). This happened in each of the considered configurations, but as the figure shows, much earlier for the conventional PD than for the Inverse PD.

From Fig. 23, we can conclude that the BER performance of both the conventional as well as the Inverse Alexander PD degrades when the subsample factor increases from $N = 16$ (nominal value) to $N = 32$ (test case). For $N = 32$, the conventional PD was in fact not functional at all. It is also obvious from the figure that due to subsampling and non-idealities, the Inverse Alexander PD greatly outperforms the conventional Alexander PD: if we compare the BER at the same jitter level the improvement is not measurable but definitely above a factor 10^5. If we compare the jitter levels

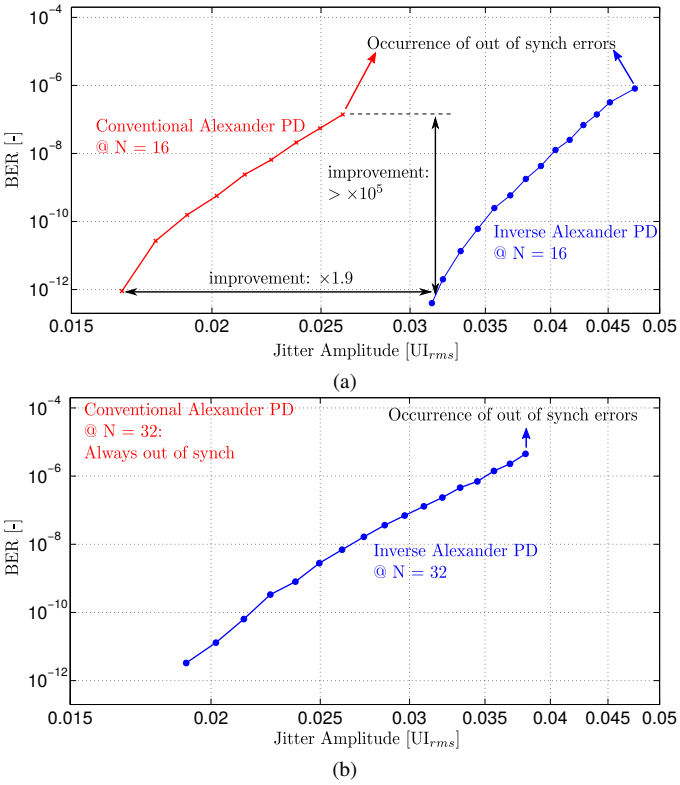


Fig. 23. Measured bit error rates for the conventional and the Inverse Alexander phase detector with a PRBS7 input data sequence at 25 Gb/s: (a) with a subsample factor $N = 16$ and (b) with a subsample factor $N = 32$. (Digital loop filter settings: $K_p = 5$ and $K_i = 2^{-7}$).

where a certain BER occurs, the improvement is about a factor 1.9.

Moreover, the phase noise of the recovered clock is compared between the conventional and Inverse Alexander phase detector for different subsample factors (Fig. 24). In all cases, a PRBS31 data sequence at 25 Gb/s was applied to the input of the CDR and the digital loop filter parameters were held constant. As predicted in Section II-A, the Inverse Alexander phase detector will introduce less noise which leads to smaller phase noise compared to the conventional Alexander phase detector for the same subsample factor. However when the subsample factor is doubled, additionally aliasing effects occur which increases the in-band phase noise with approximately 3 dB for both the conventional and Inverse Alexander phase detector.

E. All-Digital Clock and Data Recovery operation

For the final AD-CDR operation measurements, the standard operation mode (with Inverse Alexander PD and subsample factor N=16) was again selected.

The closed loop phase noise of the recovered clock for different gain settings is shown in Fig. 25 next to the phase noise of the free running oscillator. Here, a PRBS31 data sequence at 25 Gb/s is applied to input of the AD-CDR and the phase noise of the quarter-rate recovered clock is captured. The figure shows that increasing the proportional gain K_p, increases the bandwidth of the AD-CDR. As the ratio of the proportional gain K_p and integral gain K_i decreases,

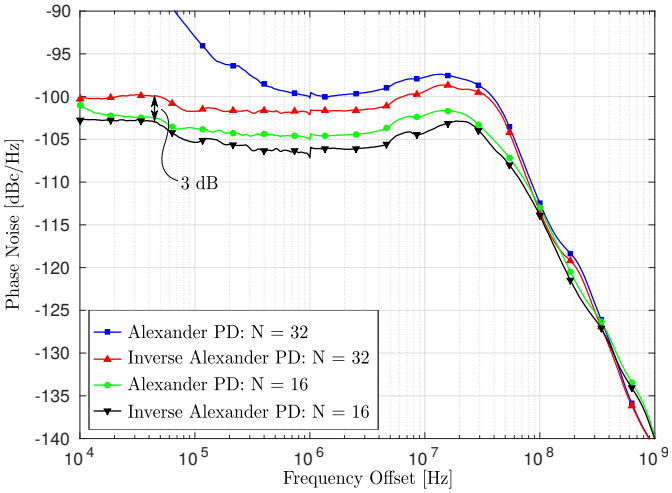


Fig. 24. Phase noise of the recovered clock with a PRBS31 input data sequence at 25 Gb/s: Comparison between Alexander and Inverse Alexander phase detector for different subsample factors (i.e. $N = 16$ and $N = 32$). (Digital loop filter settings: $K_p = 5$ and $K_i = 2^{-7}$).

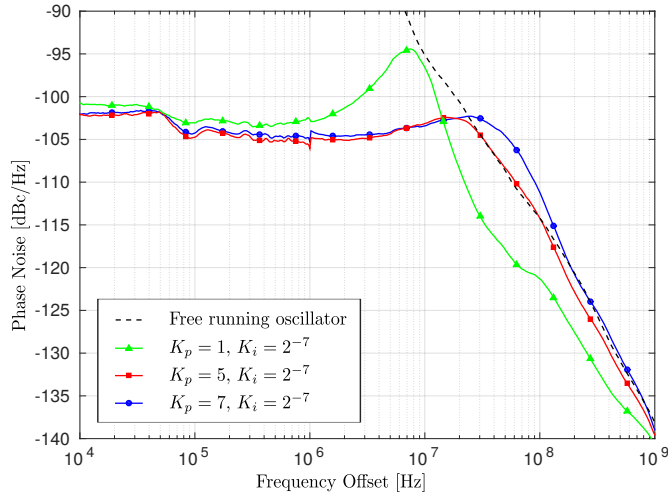
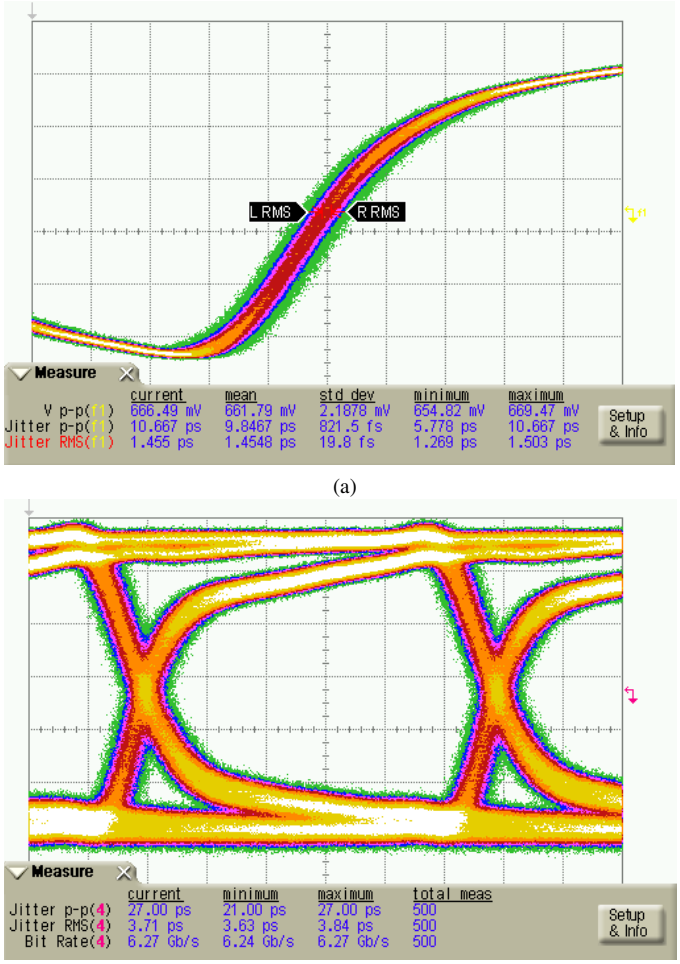


Fig. 25. Phase noise of the recovered clock with a PRBS31 input data sequence at 25 Gb/s: Sweep K_p

peaking starts to occur. Furthermore, the figure also shows that outside the loop bandwidth, the phase noise of the closed loop system approximates the phase noise of the free running clock. In the time domain, the closed loop phase noise was measured as 1.455 ps RMS jitter on the recovered clock as shown in Fig. 26(a). Additionally, the corresponding measured eye diagram of the recovered data is depicted in Fig. 26(b). The RMS jitter is approximately 3.71 ps.

The capture range of the AD-CDR was also measured and is equal to 248 MHz. This corresponds to the tuning range in normal operation and is sufficiently large to allow correct operation from an initial calibration that aligns the DCO frequency within ± 30 MHz of the desired quarter rate frequency.

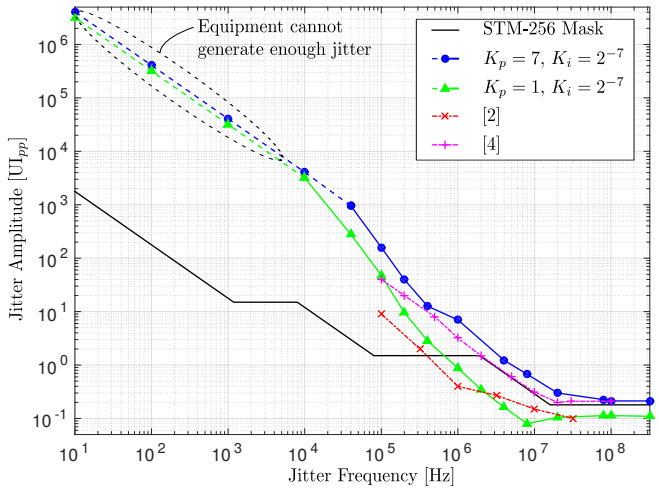
Moreover, the jitter tolerance (JTOL) of the AD-CDR is shown in Fig. 27(a) and Fig. 27(b) for different proportional gains K_p and integral gains K_i, respectively. On both figures, the SDH STM-256 jitter tolerance mask and the jitter



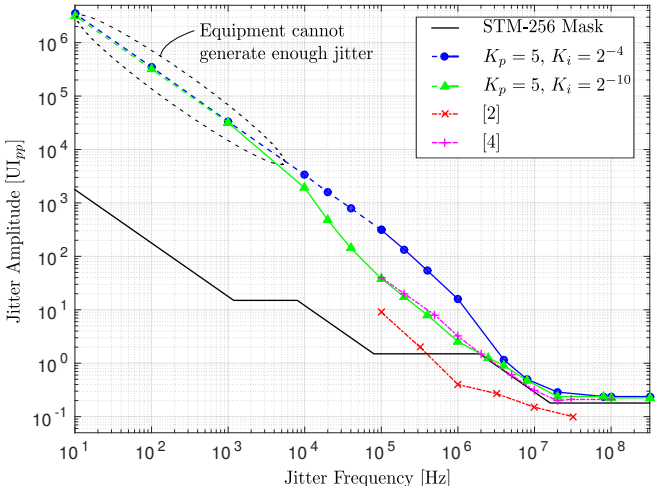
(a)

(b)

Fig. 26. Persistence plots of (a) the recovered (differential) clock (jitter $< 1.5\,\mathrm{ps_{rms}}$) and (b) the recovered data (jitter $\approx 3.71\,\mathrm{ps_{rms}}$)



(a)



(b)

Fig. 27. Jitter tolerance with a PRBS7 input data sequence at 25 Gb/s: (a) Sweep K_p and (b) Sweep K_i

tolerance of [2] and [4] are added for comparison. These jitter tolerance curves are measured by applying a PRBS7 input data sequence at 25 Gb/s with sinusoidal jitter. Each measurement is obtained by increasing the jitter level until the BER becomes $> 10^{-12}$. As shown on the figures, the jitter tolerance curves can be widely tuned by adapting the digital loop parameters. E.g. the jitter tolerance can easily be set such that it satisfies the STM-256 mask and exceeds the jitter tolerance of [2] and [4]. Please note that for the lower jitter frequencies, the jitter tolerance is better than indicated on the figures, since the highest jitter level that our equipment can generate still leads to a BER that is better than 10^{-12}.

Finally, a comparison with the state-of-the-art of digital CDRs is shown in Table III. This summary shows that our design occupies the smallest area and has the highest power efficiency. Although the performance of the DCO is modest and the phase noise and the jitter of the recovered clock are higher than prior work, only our work and [4] satisfy the STM-265 jitter tolerance mask as shown in Fig. 27. Finally, apart from [9] and [11] which have the unattractive requirement that they need a tunable, high-quality, multi-gigahertz frequency reference clock, our design has the highest relative frequency range for digital CDRs.

V. Conclusion

We have presented an AD-CDR in 40 nm Low Power CMOS technology. It can operate in a very wide range of data speeds (from 12.5 Gb/s to 25 Gb/s). The CDR takes in the high-speed data and recovers a quarter-rate clock and demultiplexes the recovered data into 4 parallel data streams. A ring oscillator generates 8 equally spaced quarter-rate clock phases, and provides the necessary timing resolution for an Inverse Alexander phase detector, which captures the recovered data and sends *Early/Late* signal to the automatically-synthesized digital loop filter.

A key enabling element of the presented design is the use of extensive subsampling together with the Inverse Alexander phase detector to reduce the operating speed of the synthesized digital logic and still guarantee good operation of the CDR. By avoiding parallel structures, this simplifies the design, reduces the active die area and decreases the power consumption. The resulting AD-CDR core has an area of $0.050\,\mathrm{mm^2}$ and consumes only 46 mW at 25 Gb/s and 23 mW at 12.5 Gb/s. The implemented CDR is highly tunable and satisfies the jitter tolerance specifications for SDH STM-256.

TABLE III
COMPARE DIGITAL CDRS

	[5]	[6]	[9]	[10]	[11]	[2]	[4]	[This work]
CMOS Technology [nm]	28	40	65	28	90	65	28	40
Data Rate [Gb/s]	40	19-27	1-16	28	6-44	22-26.5	22.5 - 32	12.5-25
relative frequency range [%]	-	29.6	93.8	-	86.4	17	29.7	**50**
Type	Digital CDR	Digital CDR	Digital CDR $^{(**)}$	Digital CDR	Digital CDR	AD-CDR	AD-CDR	AD-CDR
Oscillator type	LC-VCO + PI	QR-VCO + PI	PI	PI	PI	LC-QDCO	DAC + Ring-VCO	Ring-DCO
Power [mW]	927 $^{(*)}$	85$^{(*)}$	89	107	230	218	102	**46**
Power eff. [pJ/bit]	23.2	3.1	5.5	3.8	5.7	8.2	3.2	**1.8**
Area [mm^2]	0.81	0.09	0.088	0.52	0.2	0.46	0.52	**0.050**
Phase noise @ 1MHz [dBc/Hz]	-105	-96	-	-	-	-115	-	-105
Jitter RCLK [ps$_{rms}$]	0.170	1.66	-	-	0.249	1.28	-	1.46
JTOL @ 10 MHz [Uipp]	0.3	0.5	0.4	0.3	0.35	0.16	0.35	**0.6**
Satisfies STM-265 JTOL mask	No	No	No	No	No	No	Yes	**Yes**
Reference clk [GHz]	-	0.1	8 - 16	14	6-11	No	No	**No**
Demux ratio	1:64	1:2	1:16	1:4	1:16	1:64	1:32	1:4
Equalization	CTLE, 17-tap DFE 2-tap Transversal Filter, 3-tap Sampled FFE	CTLE, 2-tap DFE	CTLE	CTLE	No	No	CTLE, 1-tap DFE	No

$^{(*)}$ Power consumption of complete receiver.
$^{(**)}$ Here, the design is described as an AD-CDR. However, according to our definition of an (PLL-based) AD-CDR, this is a digital CDR.

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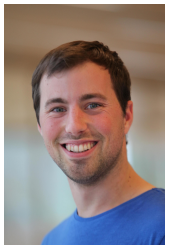

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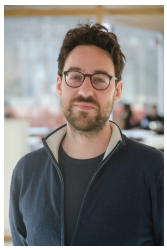

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