PAM-4 VCSEL driver with selective falling-edge pre-emphasis

W. Soenen✉, J. Lambrecht, X. Yin, S. Spiga, M.-C. Amann, G. Van Steenberge, P. Bakopoulos and J. Bauwelinck

Data centre optical links are migrating to four-level pulse amplitude modulation (PAM-4) as a method to extend the data rate while covering longer distances. Vertical-cavity surface-emitting lasers (VCSELs) enable the integration of low-power transmitters, but their non-linear and bias-dependent behaviour makes conventional feed-forward equalisation less effective. This Letter presents a 0.13 μm SiGe BiCMOS PAM-4 driver that boosts the falling-edge to the bottom level through a selective pre-emphasis technique. Experiments at 25 GBd (50 Gb/s) reveal that adding selective pre-emphasis to a 4-tap equalised current driving a 20.6 GHz 1.5 μm VCSEL, relaxes the critical PAM-4 link budget requirements by >1 dB at the KP4 forward error correction threshold of 2.2×10^{-4}. The potential of PAM-4 VCSEL transmitters can be significantly enhanced by including selective pre-emphasis to the equalisation topology while requiring minimal overhead.

Introduction: With the advent of four-level pulse amplitude modulation (PAM-4) modulation being adopted for emerging Ethernet standards such as 100 and 400 GbE, the transmitter technology will have a great impact on cost and energy efficiency. Externally modulated lasers were proposed for PAM-4 transmitters and data rates of 56 GBd per lane have already been demonstrated with a 0.18 μm SiGe transmitter employing 2-tap feed-forward equalisation (FFE) [1]. However, the associated cost and power consumption are still quite high for data centre applications. Vertical-cavity surface-emitting lasers (VCSELs) are a low-cost and low-power alternative, however, hindered by its lower bandwidth with sharp roll-off and non-linear modulation behaviour. This results in a huge discrepancy between the electrical and optical performance of PAM-4 VCSEL drivers. Impressive data rates of 90 and 100 Gb/s are demonstrated electrically without equalisation, however, these quickly degrade to 40 and 56 Gb/s while driving a 20 and 24 GHz VCSEL [2, 3]. Multi-tap FFE is often utilised to bridge the gap, but it is not trivial due to the bias-dependent behaviour of the VCSEL. For example, the fall time tends to be longer than the rise time. This has been dealt with in non-return-to-zero drivers by providing asymmetric pre-emphasis techniques [4–6], which is, however, not straightforward to be applied to PAM-4 modulation. In this Letter, we present an SiGe PAM-4 VCSEL driver IC that combines 4-tap FFE with selective falling-edge preemphasis (SFEP) to speed up the transitions to the bottom level, thereby expanding the lower eye opening.

Selective falling-edge pre-emphasis for PAM-4 modulation: Large signal modulation experiments with a PAM-4 IC driving a long-wavelength VCSEL revealed that the falling edges to the bottom level are typically the slowest [7]. This leads to the bottom eye being less open than the middle and top eyes which negatively impacts the bit-error ratio (BER). Hence, it would be advantageous to pre-emphasise the bottom-level transitions apart from the regular FFE. Particularly, each transition to the bottom level needs to be boosted. Hence, a falling-edge detection circuit needs to sense the instant when both data inputs MSB and LSB become logic low and generate a falling pulse accordingly. Fig. 1 shows a conceptual diagram to realise this functionality, suitable for cathode-driving and multi-level modulation formats. It comprises a NOR-gate, a delay cell with time delay T_d and an OR-gate with one inverted input to create a logic output current I_{SFEP} with pulse width T_{wp}.

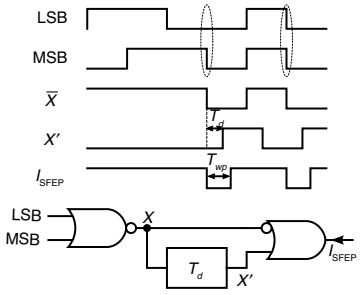

Fig. 1 *Timing and logic gate diagram to generate falling-edge pre-emphasis current pulse I_{SFEP} when MSB and LSB signals transition to bottom level*

This architecture allows I_{SFEP} to be summed with the modulation current by implementing the final OR-gate as a current-mode logic stage, shown in Fig. 2. This is clearly an improvement over [6] that requires a PMOS-stage to insert the falling-edge current pulse at the output, which introduces a speed penalty. The output current I_{SFEP} can be expressed as a function of the inputs V_{iA} (X) and V_{iB} (X')

$$I_{SFEP} = V_{iB} + \overline{V_{iA} + V_{iB}} = \overline{V_{iA}} + V_{iB} \quad (1)$$

leading to an OR-gate with one input being inverted (1). This behaviour is in accordance with the conceptual diagram of Fig. 1. The time delay T_d is set by a programmable delay cell but also includes the fixed propagation time of the level shifter Q_3. The biasing I_{b1} of Q_3 is equipped with cross-coupled cascode transistors Q_4 to provide extra bandwidth with less current. The full width at half maximum of the I_{SFEP} pulse can be set to either 17 or 27 ps. In addition, the amplitude of the current pulse can be modified by the tail current I_{b0} from 0 to 2.4 mA.

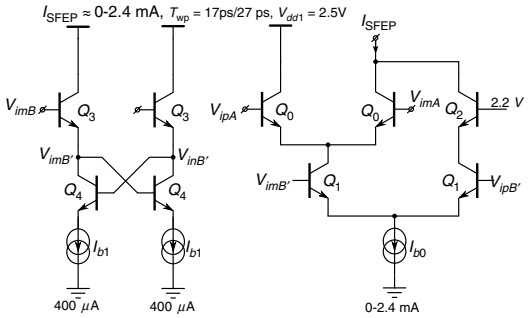

Fig. 2 *SFEP output stage representing OR-gate with inputs $\overline{V_{iA}}$ and V_{iB} and output current I_{SFEP}*

The SFEP circuit is part of a PAM-4 driver incorporating a symbol-spaced four-tap FFE output stage in a cathode drive configuration [8], drawn in Fig. 3. The LSB and MSB inputs from Fig. 1 are taken from the flip-flop outputs and I_{SFEP} is combined with the VCSEL bias current I_{bias} and the FFE current originating from tap drivers A_0–A_3. Remark that the depicted PAM-4 FFE topology scales the amplitude of the pre-emphasis pulse linearly with the level change of the main modulation current by maintaining a fixed ratio of two between the MSB and LSB FFE coefficients. This approach is similar to [9], but no power-hungry encoders and multiplexers are required.

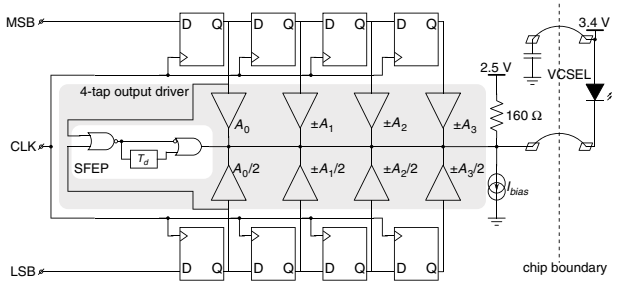

Fig. 3 *Channel architecture of symbol-spaced four-tap FFE PAM-4 driver IC with SFEP*

The complete driver IC is implemented as a dual-channel device in a 0.13 μm SiGe BiCMOS process and measures 1×2.8 mm^2. The driver output is wirebonded to a VCSEL array developed by Technische Universität München, as shown in Fig. 4. The 1.5 μm VCSEL is characterised with a maximum bandwidth of 20.6 GHz and an optical power of 3.9 mW occurring at a roll-over current of 15 mA [10]. The driver and the VCSEL are operated from, respectively, 2.5 and 3.4 V supply voltage.

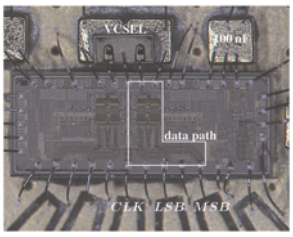

Fig. 4 *PAM-4 driver wire bonded to* 1.5 µm *VCSEL array and mounted on PCB with single-ended* 50 Ω *transmission lines*

Results: The single-ended MSB and LSB binary inputs of the driver are excited with a 25 Gb/s 400 mV_{pp} $2^7 - 1$ pseudorandom bit sequence (PRBS). Both streams are decorrelated to each other by using a cable with an ~12 bit-period delay. The optical output of the VCSEL is aligned to a flat-cleaved single-mode fibre and propagates through a variable optical attenuator before arriving at a 32 GHz linear photoreceiver (DSCR-409). The differential receiver output is captured with a 160 GS/s real-time oscilloscope to allow off-line decoding of the PAM-4 signal. Remark that no receiver equalisation or other digital signal processing is applied before calculating the BER related to the LSB and MSB streams. We first optimised the equaliser and SFEP settings for minimum BER. Afterwards, SFEP was disabled and the bias current increased to maintain the same average current of 10.4 mA through the VCSEL. This methodology allows to extract the impact of SFEP on the system while the VCSEL is biased at a constant modulation bandwidth.

Captured eye diagrams at 25 GBd shown in Fig. 5 reveal that SFEP combined with a four-tap FFE is able to expand the lower eye while simultaneously improving the vertical alignment of the subsequent eyes. This is also reflected in the BER plots of the LSB and MSB data streams, plotted in Fig. 6, of which the total BER is dominated by the LSB data. The MSB data, which directly maps to the middle eye, becomes error-free above −5 dbm. With a record length of 1.25×10^7 bits, this corresponds to an upper BER limit of 2.9×10^{-7} with 95% confidence. Considering a KP4 forward error correction threshold of 2.2×10^{-4} [11], enabling SFEP can increase the link budget by >1 dB. The transmitter power dissipation amounts 455 mW, of which only 18 mW originates from the SFEP circuit. Future work could investigate in extending the selective pre-emphasis technique to all PAM-4 levels to compensate bias-dependent overshoot, in the end replacing the symbol-spaced equaliser to save power.

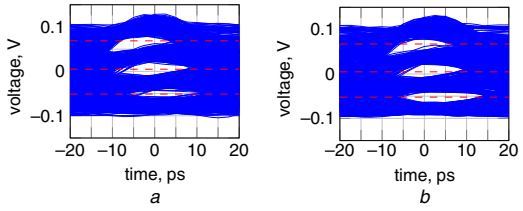

Fig. 5 *Captured eye diagrams using real-time oscilloscope at 25 GBd with annotated decision thresholds for 1000 symbols*

a Equalisation with four-tap FFE
b Equalisation with four-tap FFE and SFEP expands lower eye

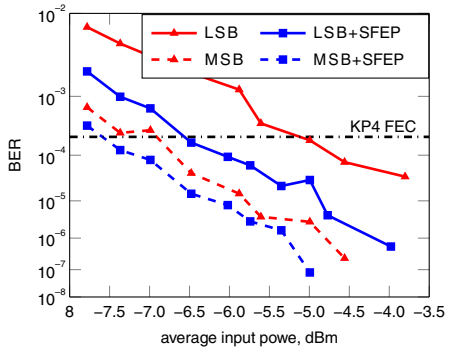

Fig. 6 *Total BER dominated by LSB is lowered with approximately one order of magnitude by enabling SFEP*

Conclusion: We have demonstrated that a selective falling-edge pre-emphasis circuit implemented in a 0.13 µm SiGe BiCMOS PAM-4 VCSEL driver can assist a conventional multi-tap FFE in increasing the link budget of a VCSEL link. The proposed new SFEP circuit is able to restore the lower eye, while consuming only 4% of the transmitter power dissipation.

Acknowledgment: This work was supported by the European project MIRAGE (contr. no. 318228).

Submitted: *20 October 2017* E-first: *18 December 2017*
doi: 10.1049/el.2017.3945
One or more of the Figures in this Letter are available in colour online.

W. Soenen, J. Lambrecht, X. Yin and J. Bauwelinck (*IDLab Department of Information Technology, Ghent University-IMEC, Technologiepark-Zwijnaarde 15, 9052 Gent-Zwijnaarde, Belgium*)

✉ E-mail: wouter.soenen@ugent.be

S. Spiga and M.-C. Amann (*Walter Schottky Institute, Technische Universität München, Am Coulombwall 4, D-85748 Garching, Germany*)

G. Van Steenberge (*Centre for Microsystems Technology (CMST), Ghent University-imec, Technologiepark-Zwijnaarde 15, 9052 Gent-Zwijnaarde, Belgium*)

P. Bakopoulos (*Mellanox Technologies, Hakidma 26, 2069200 Yokneam, Israel*)

References

1 Shahramian, S., Lee, J., Weiner, J., *et al.*: 'A 112 Gb/s 4-PAM transceiver chipset in 0.18 µm SiGe BiCMOS technology for optical communication systems'. IEEE Compound Semiconductor Integrated Circuit Symp. (CSICS), New Orleans, LA, USA, October 2015, pp. 1–4, doi: 10.1109/CSICS.2015.7314464
2 Belfiore, G., Henker, R., and Ellinger, F.: '90 Gbit/s 4-level pulse-amplitude-modulation vertical-cavity surface-emitting laser driver integrated circuit in 130 nm SiGe technology'. IEEE MTT-S Latin America Microwave Conf. (LAMC), Puerto Vallarta, Mexico, December 2016, pp. 1–3, doi: 10.1109/LAMC.2016.7851243
3 Chen, J., He, Z. S., Lengyel, T., *et al.*: 'An energy efficient 56 Gbps PAM-4 VCSEL transmitter enabled by a 100 Gbps driver in 0.25 µm InP DHBT technology', *J. Lightw. Technol.*, 2016, **34**, (21), pp. 4954–4964, doi: 10.1109/JLT.2016.2600591
4 Belfiore, G., Khafaji, M., Henker, R., *et al.*: 'A 50 Gb/s 190 mW asymmetric 3-tap FFE VCSEL driver', *J. Solid-State Circuits*, 2017, **52**, (9), pp. 2422–2429, doi: 10.1109/JSSC.2017.2717918
5 Kucharski, D., Kuchta, D., Guckenberger, D., *et al.*: 'A 20 Gb/s VCSEL driver with pre-emphasis and regulated output impedance in 0.13 µm CMOS'. IEEE Int. Digest of Technical Papers Solid-State Circuits Conf. (ISSCC), San Francisco, CA, USA, February 2005, pp. 222–224, doi: 10.1109/ISSCC.2005.1493949
6 Ohhata, K., Imamura, H., Takeshita, Y., *et al.*: 'Design of a 4 × 10 Gb/s VCSEL driver using asymmetric emphasis technique in 90-nm CMOS for optical interconnection', *Trans. Microw. Theory Tech.*, 2010, **58**, (5), pp. 1107–1115, doi: 10.1109/TMTT.2010.2045574
7 Soenen, W., Vaernewyck, R., Yin, X., *et al.*: '40 Gb/s PAM-4 transmitter IC for long-wavelength VCSEL links', *Photon. Technol. Lett.*, 2015, **27**, (4), pp. 344–347, doi: 10.1109/LPT.2014.2372041
8 Soenen, W., Vaernewyck, R., Yin, X., *et al.*: '56 Gb/s PAM-4 driver IC for long-wavelength VCSEL transmitters'. European Conf. Optical Communication (ECOC), Dusseldorf, Germany, September 2016, pp. 1–3, ISBN 978-3-8007-4274-5
9 Wang, Y., and Gai, W.: 'A 2-tap 40-Gb/s 4-PAM transmitter with level selection based pre-emphasis'. IEEE Int. Symp. Circuits Systems, Lisbon, Portugal, May 2015, pp. 333–336, doi: 10.1109/ISCAS.2015.7168638
10 Spiga, S., Schoke, D., Andrejew, A., *et al.*: 'Enhancing the small-signal bandwidth of single-mode 1.5-µm VCSELs'. 5th IEEE Photonics Society Optical Interconnects Conf., San Diego, CA, USA, May 2016, pp. 14–15, doi: 10.1109/OIC.2016.7482982
11 Bhoja, S., Parthasarathy, V., Wang, Z., *et al.*: 'FEC codes for 400 Gbps 802.3bs'. IEEE P802.3bs 400 GbE Task Force, Plenary Meeting Material. Available at http://www.ieee802.org/3/bs/public/14_11/parthasarathy_3bs_01a_1114.pdf, November 2014