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Modulated Model Predictive Control for Active Split DC-bus 4-leg Power Supply

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Abstract – **This paper proposes a constant switching frequency Finite Control Set Model Predictive Control (FCS-MPC), formally Modulated FCS-MPC or M2PC, for a 4-leg inverter having an Active Split DC-bus on the fourth leg. The great advantage of MPC over linear control schemes is the very fast transient response it is capable to produce; it also can handle general constrained nonlinear systems with multiple inputs and outputs in a unified and clear manner. These features are highly valuable in power electronic converters used to supply the electrical utility loads in micro-grids. However, one of the main drawback of the MPC is its variable switching frequency, above all in system with accurately tuned output power filters (i.e. switching traps), which is the case when stable voltage waveforms with very low harmonic content are required. The proposed investigation relates with the application of a constant switching frequency variant of the MPC to a 4-leg inverter with a specifically tuned filter to assure high quality voltage supply even in case of non-linear and unbalanced loads.**

I. INTRODUCTION

Voltage Source Inverters (VSI) with different topologies are finding increasing utilization in power supplies for electrical utility systems, due for example to the widespread use of UPS for various application as well as for the growing local utilization of renewable energy resources of distributed generation systems. These may be arranged in form of a micro-grid with common DC-bus, as schematically depicted in Figure 1. In such applications, the output inverter is used to supply the electrical utility loads, which can be either single or three phase loads and, in the case of three-phase loads, they can be either balanced or unbalanced. Hence, a four-wire electrical distribution system must be arranged for the supply of such utility loads and, in order to ensure this, a stable and ripple-free neutral connection must be provided, so to avoid recirculation of currents through the system stray capacitances, in particular when the TT grounding arrangement is used.

In the case of the four-leg VSI topology several configurations have been provided in literature; among these, one approach relies on simply adding a fourth leg in the conventional VSI layout so that the middle point of such switching leg is directly used as the inverter N terminal. Alternatively, a filtering inductor is placed between the output N-terminal and the active phase-leg. Such an arrangement allows the neutral voltage to be stabilized with respect to the

fundamental frequency, but a significant voltage ripple still affects the waveform of the voltages measured between the N point and the DC-plus and DC-minus bars. These high frequency oscillations occur at the switching frequency and its related multiple values, so that issues may arise concerning the grounding arrangement (i.e. TT or TN) adopted for the utility system. When the TN arrangement is used, this leads to recirculating currents on the DC-Link side system (in particular through large surface PV units); instead, when TT system is used, high common mode voltage arises at the load-side, leading to possible malfunctions of end-user equipment.

A different arrangement of the fourth-leg can be used to provide a ripple free N-wire at both the fundamental and switching frequencies [1]. Such a novel configuration is the combination of the previously described topologies and leads to the so-called Active Split DC-bus configuration, as shown in

Figure 2, which is the four-terminal VSI topology this technical paper refers to. Inverter output filter configuration is illustrated in Figure 3, which is suggested in both stand-alone and grid-tied applications [2]. Behind the main LC filter, a switching trap tuned at the inverter switching frequency and a selective dumper have been inserted between each phase and the common neutral connection. Such a system imposes to use an absolute constant switching frequency, otherwise the filtering benefits can be strongly reduced.

In recent years, classical Model Predictive Control (MPC) structures have been used in numerous applications in the field of power electronics and drives due to their many advantages, like fast dynamic response, no need of modulation, easy inclusion of system nonlinearities, constraints and requirements in the controller [3]-[5]. MPC considers the system model for predicting its future behavior and determining the best control action according to a cost function representing the desired behavior. Considering that power converters are systems with a finite number of states, the Finite Control Set MPC (FCS-MPC) optimization problem consists in the prediction of the system behavior for each possible state. Then, each prediction is evaluated using the cost function and the state that minimizes it, is selected [6]. This approach has been successfully applied for the current control in three-phase inverters [3], [7], matrix converters [8], power control in an active front end rectifiers

[9], torque and flux control of an induction machine [10]-[13], control Permanent Magnet Syncronous Machines (PMSM) drives, [14], sensorless control [15] and active filters [16].

When FCS-MPC is applied for VSI control, it has the benefit of very fast transient response and high performance in ensuring regulated voltages at the inverter outputs with low harmonic content; however, they exhibit an upper limited switching frequency [17]–[22], resulting in a varying commutation frequency F_{sw}, which is highly not indicated in case of specifically tuned filters. Solutions to keep F_{sw} constant have been proposed in [23], [24] with the so-called Modulated Model Predictive Control (M²PC) which, in addition, enables multi-objective control capabilities within the same feedback loop, while keeping all the desired features of MPC.
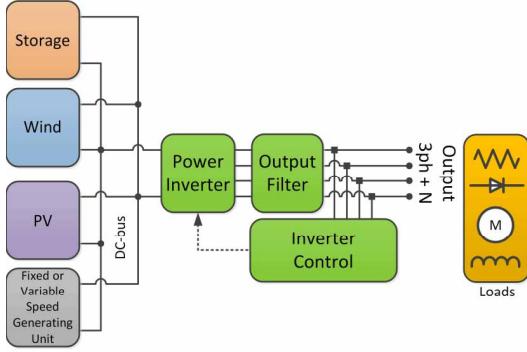

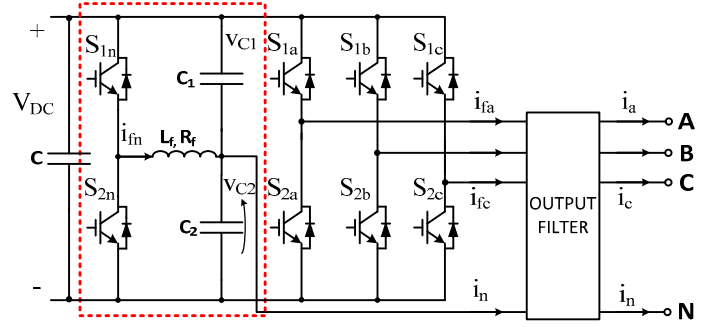Figure 1. Typical application of the front-end inverter.

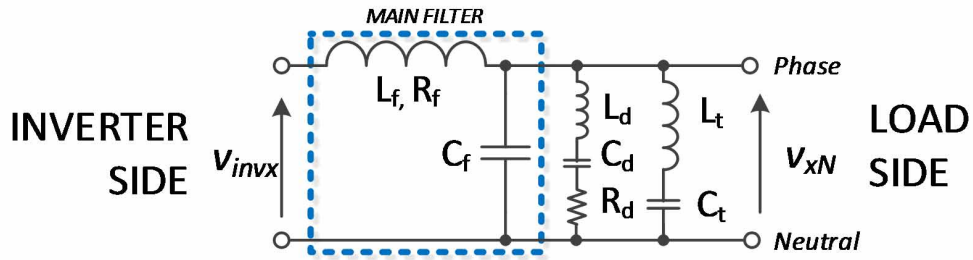Figure 2. VSI 4-leg topology with Active Split DC-bus.

Figure 3. Phase-to-neutral scheme of output power filter.

II. SYSTEM MODEL

The VSI Inverter model can be described by the following differential equations:

$$\frac{di_{fx}(t)}{dt} = \frac{1}{L_f}\left[-R_f i_{fx}(t) + v_{invx}(t) - v_{xN}(t)\right] =$$

$$= \frac{1}{L_f}\left[-R_f i_{fx}(t) + S_{1x}v_{C1}(t) - S_{2x}v_{C2}(t) - v_{xN}(t)\right] \quad (1)$$

$$\frac{dv_{xN}(t)}{dt} = \frac{1}{C_x}\left[i_{fx}(t) - i_x(t)\right]$$

being $x=a$, b, c one of the three inverter phases, i_{fx} the filter current, R_f the parasitic resistance of filter inductor, $v_{invx,}$ the inverter Phase-to-Neutral voltage, v_{xN} the phase-to-Neutral output voltage, S_{1x} and S_{2x} the switching functions, for the upper and lower leg switches respectively. The switching functions assume a value equal to 1, when the corresponding switch is closed, or equal to 0 in the opposite case.

The DC-link Voltage, assumed as a constant and the neutral current i_n are subject to the following constrains:

$$V_{DC} = v_{C1}(t) + v_{C2}(t) \tag{2}$$

$$i_n(t) = -\left(i_a(t) + i_b(t) + i_c(t)\right) \tag{3}$$

Using the same approach as for the Inverter model, the neutral leg n with Active Split DC-bus model can be described by the following differential equations

$$\frac{di_{fn}(t)}{dt} = \frac{1}{L_f}\left[-R_f i_{fn}(t) + S_{1n}v_{C1}(t) - S_{2n}v_{C2}(t)\right]$$

$$\frac{dv_{c2}(t)}{dt} = \frac{1}{C_1+C_2}\left[i_{fn}(t) - i_n(t)\right]$$

$$\tag{4}$$

being $\frac{dv_{c1}(t)}{dt} = -\frac{dv_{c2}(t)}{dt}$ from (2).

III. PROPOSED MODULATED-MODEL PREDICTIVE CONTROL

Finite Control Set (FCS) MPC control is based on the prediction of the system response to a change in control variables in order to minimize a suitable cost function in the next one, two or more sampling periods, depending on the

chosen prediction horizon. The output of this control is a discrete value that can be directly applied to control the converter and it is chosen by minimizing a cost function that represents the error between the current and the desired reference. Applying FCS-MPC to control the AC current, the desired reference is tracked with minimum error at the next sampling period. In order to allow the implementation in a DSP, the continuous-time equations (1)-(4) have to be discretized using sampling interval T_s thus obtaining the following discrete-time model:

$$i_{fx}(k+1) = \left(1 - \frac{R_f T_s}{L_f}\right)i_{fx}(k) + \frac{T_s}{L_f}[S_{1x}(k)v_{C1}(k) - S_{2x}(k)v_{C2}(k) - v_{xN}(k)] \quad (5)$$

$$v_{xN}(k+1) = v_{cx}(k) + \frac{T_s}{C_f}[i_{fx}(k) - i_x(k)]$$

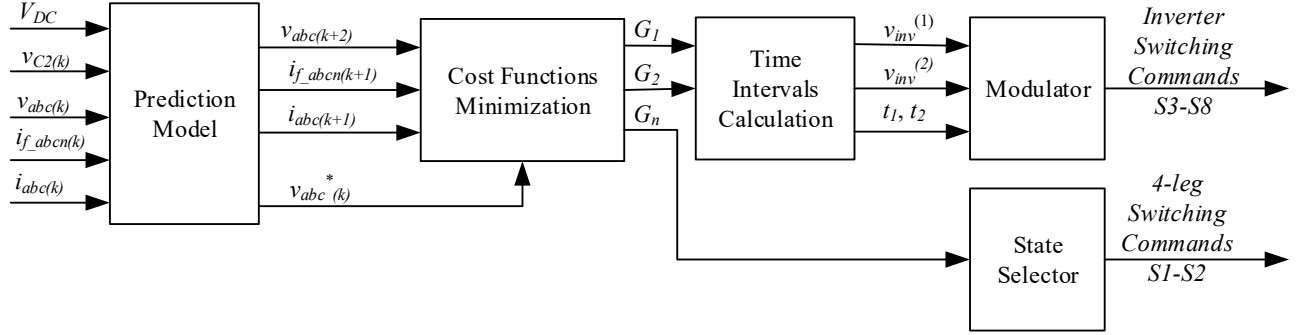$$v_{C2}(k+1) = v_{C2}(k) + \frac{T_s}{C_1 + C_2}[i_{fn}(k) - i_n(k)]$$

Figure 4. M²PC block scheme.

The computation delay introduced by the DSP can be represented as a delay of one sampling interval on the voltages v_{invx} applied on each phase by the converter. To compensate for such a delay, the prediction of two steps ahead is needed.

$$v_{xN}(k+2) = v_{xN}(k+1) + \frac{T_s}{C_f}[i_{fx}(k+1) - i_x(k+1)]$$

To take advantage of the filter traps used to remove the switching component, an approach similar to the Modulated Model Predictive Control (M²PC) proposed in [23], [24] is used in this paper to achieve constant switching frequency. Figure 4 shows the block scheme of M²PC, which includes a suitable modulation scheme in the cost function minimization of the MPC algorithm.

At every sampling instant, two vectors are selected for the three-phase VSI. The first selected vector $v_{inv}^{(1)}$, applied through the switching states S_{1x}^1 and S_{2x}^1, is the one applied at the end of the previous sampling interval; it is calculated on the basis of the current and voltage predictions at time interval $k+2$ and selecting the vector that minimise the cost function G_1 At the following sampling period.

$$i_{fx}(k+2) = \left(1 - \frac{R_f T_s}{L_f}\right)i_{fx}(k+1) + \frac{T_s}{L_f}[S_{1x}^1(k+1)v_{C1}(k+1) - S_{2x}^1(k+1)v_{C2}(k+1) - v_{xN}(k+1)] \quad (6)$$

$$v_{xN}(k+3) = v_{xN}(k+2) + \frac{T_s}{C_f}[i_{fx}(k+2) - i_x(k+2)]$$

$$G_1 = \sum_{x=a,b,c} |v_{xN}(k+3) - v_{xN}^*(k+3)|^2$$

where the references voltages are

$$v_{aN}^*(k+3) = \hat{V}_a^* sin(\theta + 3\omega T_s)$$
$$v_{bN}^*(k+3) = \hat{V}_b^* sin\left(\theta + 3\omega T_s + \frac{2\pi}{3}\right)$$
$$v_{cN}^*(k+3) = \hat{V}_c^* sin\left(\theta + 3\omega T_s + \frac{4\pi}{3}\right)$$

The second vector $v_{inv}^{(2)}$ is chosen between the other available vectors, on the basis of the current and voltage predictions at time interval $k+2$ and selecting the vector that minimise the cost function G_2 at the following sampling period.

$$i_{fx}(k+2) = \left(1 - \frac{R_f T_s}{L_f}\right)i_{fx}(k+1) + \frac{T_s}{L_f}[S_{1x}^2(k+1)v_{C1}(k+1) - S_{2x}^2(k+1)v_{C2}(k+1) - v_{xN}(k+1)] \quad (7)$$

$$v_{xN}(k+3) = v_{xN}(k+2) + \frac{T_s}{C_f}[i_{fx}(k+2) - i_x(k+2)]$$

$$G_2 = \sum_{x=a,b,c} |v_{xN}(k+3) - v_{xN}^*(k+3)|^2$$

Load currents predictions i_x are calculated for times instant $k+1$ and $k+2$ using extrapolation in [25]. The time intervals t_1 and t_2 for the two vectors are calculated by solving the following linear system of equations:

$$\begin{cases} t_1 = \dfrac{K}{G_1} \\ t_2 = \dfrac{K}{G_2} \\ t_1 + t_2 = T_s \end{cases} \qquad (8)$$

Once calculating the value of K from (8), the following expressions of the switching times are obtained:

$$t_1 = T_s \frac{G_2}{G_1 + G_2} \qquad t_2 = T_s - t_1 \qquad (9)$$

The control of the Active Split DC-bus configuration is achieved by maintain balanced voltages across the split capacitors. To this aim, the following current and voltage predictions are used to minimize the cost function G_n.

$$i_{fn}(k+1) = \left(1 - \frac{R_f T_s}{L_f}\right) i_{fn}(k)$$
$$+ \frac{T_s}{L_f}\left[S_{1n}(k)v_{C1}(k) - S_{2n}(k)v_{C2}(k)\right]$$

$$v_{C2}(k+1) = v_{C2}(k) + \frac{T_s}{C_1 + C_2}\left[S_2(k)i_{fn}(k) - i_n(k)\right]$$

$$G_n = |v_{C1}(k+2) - v_{C2}(k+2)|$$

IV. HARDWARE REALIZATION AND RESULTS

The proposed control strategy, has been verified, at first, by a specific simulation model developed in PLECS employing the following main parameters (with reference to figures 2 and 3): $R_f = 50\,\text{m}\Omega$, $L_f = 800\,\mu\text{H}$, $C_f = 5\,\mu\text{F}$, trap filters tuned at 12 kHz as the VSI switching frequency, $T_s = 8.33\,\mu\text{s}$, $L_d = 810\,\mu\text{H}$, $C_d = 7\,\mu\text{F}$ and $R_d = 30\,\Omega$. Figure 5 and Figure 6 shown the behavior of the converter respectively in the case of an unbalanced 3-phase resistive load (2kW, 2kW, 1kW) and when a single-phase diode rectifier load is applied on phase a. The phase-to-neutral voltages waveforms present a good harmonic content with a THD value lower than 5% limit imposed by IEC 61000-3-2 even when an unbalanced non-linear load is applied.

Experimental tests have been then performed on the four-leg hardware setup shown in Figure 7 with the output power filter depicted in Figure 8 and employing the same operating conditions as in simulation. The control algorithm has been implemented in a PED-Board® shown in Figure 7 on the top of the converter. The PED-Board, which is based on the National Instruments System-on-Module sbRIO-9651, has been designed with dedicated peripherals specifically for power electronics and drives applications. NI sbRIO-9651 has a dual-core ARM processor and an Artix7 FPGA. FPGA manages the on-board ADCs, resolver when needed, PWM unit and scheduler, CAN-bus communication and DACs interface. The

Real-Time target (i.e. the ARM processor) takes into account the whole external communication structure forwarding and receiving the corresponding commands and data to/from the FPGA. Results have been achieved implementing the illustrated control structure with a discretization frequency step equals to the inverter switching frequency.
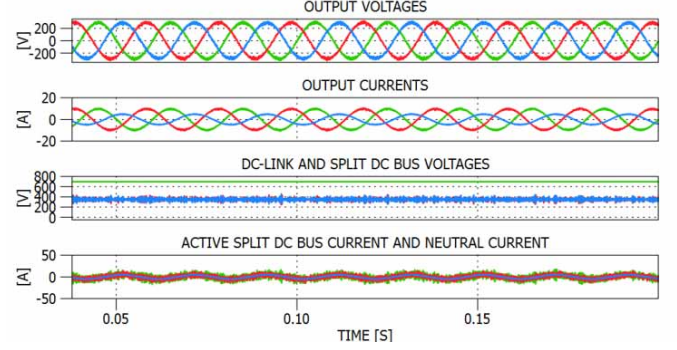

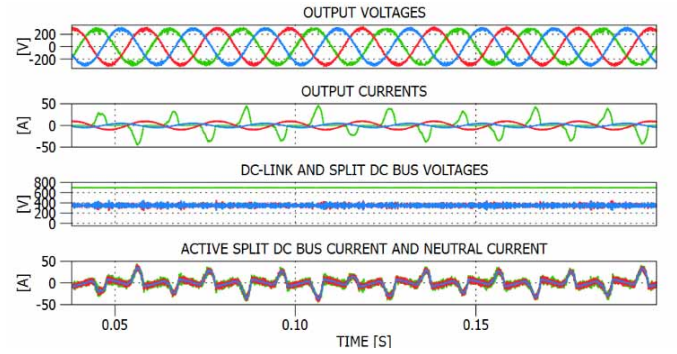Figure 5. Linear unbalanced load.

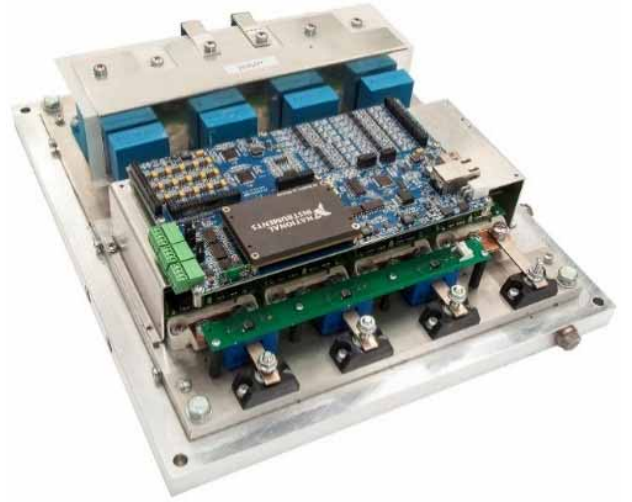Figure 6. Nonlinear single phase diode rectifier load.

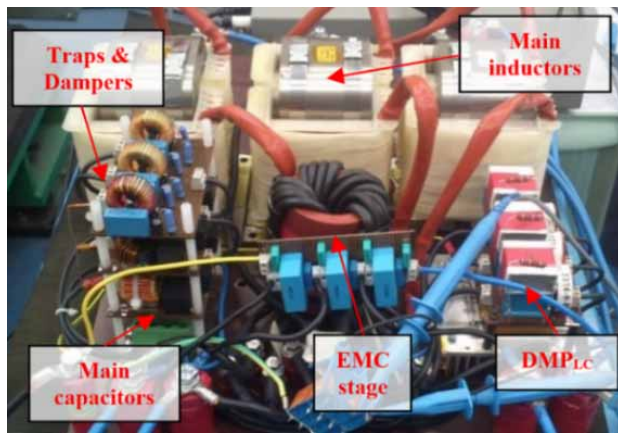Figure 7. Four-leg VSI converter prototype.
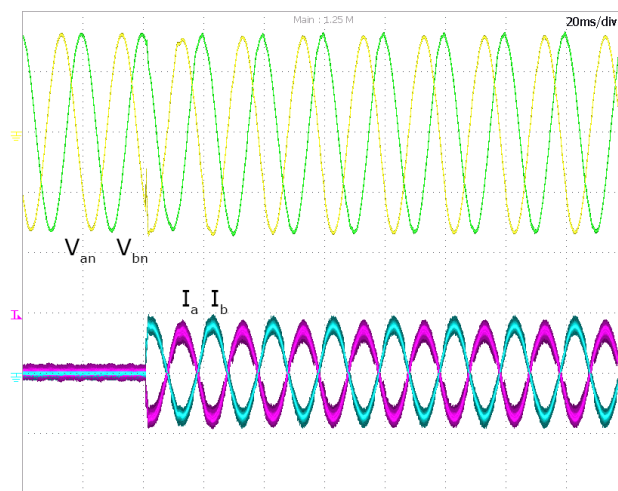
Figure 8. Inverter output power filter.

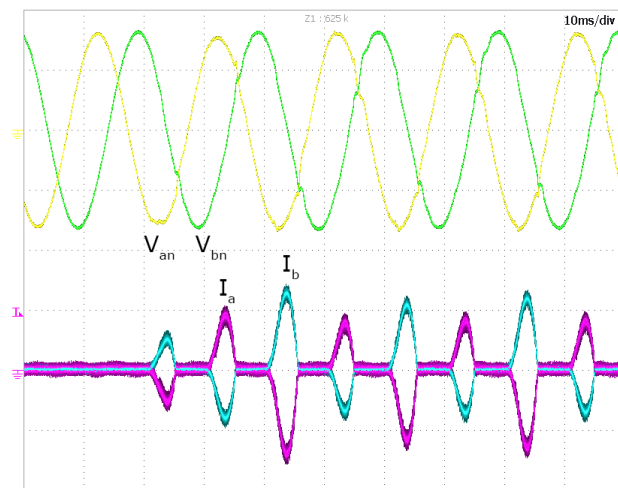Figure 9. Linear balanced load step. (20 A/div, 200 V/div)

Figure 10. Nonlinear single phase diode rectifier load step. (50 A/div, 200 V/div)

The output voltages behavior with linear balanced load is shown in Figure 9 where the load is suddenly changed from no-load condition to around 2 kW per phase. It can be noticed the control good performance even when the load is connected close to the phase voltage peak value, which represents the worst condition. Performance of the M^{2}PC algorithm with unbalanced nonlinear loads are shown in Figure 10 where a single phase diode rectifier has been connected between phase A and the output neutral connector. As soon as the load is fed, the output voltages waveform proves the effectiveness of the M^{2}PC strategy, being able to fast compensate both harmonics and voltage drop.

CONCLUSIONS

The paper investigates the application of modulated Model Predictive Control (M2PC) strategy, a constant switching frequency variant of the Finite Control Set Model Predictive Control (FCS-MPC), to control a 4-leg VSI having an Active Split DC-bus on the fourth leg and used to supply both unbalanced and non-linear electrical utility loads. The M2PC, retains all the desirable characteristics of FCS-MPC, such as fast dynamics, easy inclusion of model non-linearity and control constraints, multi-objective regulation in one single loop. However, it implements a constant switching frequency, allowing its use in power supplies, where output filters are specifically designed to achieve a low output distortion (often including switching traps like in the case of this work). Simulation and experimental tests have validated the proposed method.

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