Behavior of Copper Contamination for Ultra-Thinning of 300 mm Silicon Wafer down to <5 μm

Yoriko Mizushima[1,2], Youngsuk Kim[2], Tomoji Nakamura[1,2],
Ryuichi Sugie[3], and Takayuki Ohba[2]

[1]Fujitsu Laboratories Ltd., 10-1 Morinosato-Wakamiya, Atsugi 243-0197, Japan
[2]Tokyo Institute of Technology, 4259 Nagatsuta-cho, Midori-ku, Yokohama 226-8503, Japan
[3]Toray Research Center Inc., 3-3-7 Sonoyama, Otsu, Shiga 520-8567, Japan
E-mail: ymizu@jp.fujitsu.com

Abstract

Bumpless interconnects and ultra-thinning of 300 mm wafers for three-dimensional (3D) stacking technology has been studied [1, 2]. In our previous studies, wafer thinning effect using device wafers less than 10 μm was investigated [3, 4]. There was no change for the retention time before and after thinning even at 4 μm in thickness of DRAM wafer [5].

In this study, the behavior of Cu contamination on an ultra-thin Si stacked structure was investigated. Thinned Si wafers were intentionally contaminated with Cu on the backside and 250 °C of heating was carried out during the adhesive bonding and de-bonding processing. An approximately 200 nm thick damaged layer was formed at the backside of the Si wafer after thinning process and Cu particle precipitates ranged at 20 nm were observed by cross-sectional transmission electron microscopy (X-TEM). With secondary ion mass spectrometry (SIMS) and EDX analyses, Cu diffusion was not detected in the Si substrate, suggesting that the damaged layer prevents Cu diffusion from the backside.

1. Introduction

Bumpless ultra-thin stacking technology has many benefits such as small form factor, low aspect ratio for TSV processing, small wiring length, RC delay mitigation, and low power consumption. We have developed wafer scale 3DI technology, so-called wafer-on-wafer (WOW) characterized by "*Thinning-First before Bonding*," Back-to-Face bonding and TSV-last process without bump. Only this stacking process is able to use ultra-thin wafer and applicable multilevel stacking.

In our previous studies, electrical characteristics of device wafers were evaluated using ultra-thinned wafer which thickness less than 10 μm. No degradation before and after thinning was demonstrated for CMOS logic at 7-μm-thick wafer and ferroelectric RAM at 9-μm-thick wafer, respectively [3, 4]. Recently, further thinning down to 4-μm-thick using 2 Gbit-DRAM has been succeeded with no degradation of

retention time [5]. Figure 2(a) shows the cross-sectional SEM image of 4-μm-thick DRAM wafer fabricated by WOW process. In addition, the characteristics of backside thinning-induced damage were investigated by laser microscopy, μ-Raman spectroscopy, transmission electron microscopy (TEM), and positron annihilation spectroscopy [6].

Since Cu contamination for the transistors degrades device characteristics, a lot of studies of Cu contamination for the Si wafer were reported [7, 8]. This paper describes the behavior of Cu diffusion from the back side of ultra-thinned wafer <5 μm for the first time.

2. Experimental Procedure

Figure 1 shows the sample preparation as following; edge trimming, bonding to support substrate, thinning of wafer, Cu contamination, bonding to Si wafer, and de-bonding support substrate. 300 mm DRAM device wafers were used for this experiment. Thinning condition of wafer backside was finished with #2000 grit grinding. Wafer thickness was thinned down to less than 5 μm. The Cu contamination was carried out as follows [9]: Cu concentration in the solution was set at 10 ppm of 1% of diluted hydrogen fluoride (DHF) was prepared. Copper nitrate ($CuNO_3$) aqueous solution was used as the Cu contamination material. Wafer backside was dipped into the DHF for 10 min at room temperature. Cu concentration is estimated at the order of 10^{13} atoms/cm^2. Bonding and de-bonding processes were carried out at 250 °C for 1 hour in atmosphere condition. The rest of the processes were performed conventionally. Underneath Si substrate was grounded until 200 μm, and then the wafer was diced by chip size. The sample structure is shown in Fig. 2(b).

For X-TEM analysis, specimens were prepared by focused ion beam (FIB) milling technique after covering the surface with epoxy resin. The thicknesses of samples are prepared approximately 100 nm. Bright field TEM images were observed using a Hitachi H-9000UHR II at 300 kV under the (110) zone axis condition. Energy-dispersive X-ray spectroscopy (EDX) was analyzed using a JEOL ARM200F at 200 kV and Electron Energy-Loss Spectroscopy (EELS) Gatan Imaging Filter GIF Quantum. Beam spot size is 0.2 nm in diameter.

For the depth profile analysis of Cu, time-of-flight secondary ion mass spectrometry (TOF-SIMS), IONTOF TOF-SIMS 5 instrument, was used. A 200 μm thick Si substrate was removed by chemical and mechanical etching for SIMS analysis. $O2^+$ ion beam was configured for sputtering at 2 keV and Bi^+ primary ion beam was configured for analysis at 25 keV.

3. Results and Discussion

Figure 3 shows the X-TEM images of the thinned DRAM sample, which is stacked on the support Si substrate with the adhesive layer. The thinned Si thickness less than 5 μm and thinner than the DRAM device layer were observed. Rough and strained TEM contrast area of approximately 200 nm thick in Fig. 3(b) shows the damaged layer caused by #2000 grit grinding [6].

Cu precipitations introduced by the Cu contamination were confirmed by STEM images and EDX mappings. As shown in Figs. 4(a) and 4(b), dark and bright granular contrasts at the interface between the thinned Si and the adhesive layer were observed in the BF and HAADF STEM images, respectively. The contrast inversion of the granular particles means the element is heavier than Si. Figure 5 shows the EDX mapping images. It was confirmed that the dark particles in Fig. 4(a) indicate the Cu element. Any other elements were not detected in Cu particle areas. These Cu particles

correspond to the mechanism of Cu deposition onto Si surface in solutions [9].

Magnified TEM images of the Cu particles shown in Fig. 6 indicate that the particles consist of poly-crystalline because the diffraction contrast observed each Cu particle strongly depends on electron-beam incident conditions. In some particle areas, amorphous layers are observed at the interface between the crystalline Cu particles and the damaged Si. It means that the amorphous layer could inhibit the direct Cu reacting with the thinned Si layer.

Figure 7 shows TOF-SIMS depth profiles of Si, C, and Cu elements. Backside TOF-SIMS was measured from the side of adhesive layer. High intensity of Cu is detected at the interface between the adhesive and the Si. Cu diffusion occurs slightly in the adhesive layer while detection lower limit ~2 x 10^{17} atoms/cm^3 in the Si layer. Therefore, Cu diffusion can be suppressed by a formation of the interfacial damaged Si layer.

The stress of the strained damaged layer will be discussed using μ-Raman spectroscopy.

4. Conclusions

The behavior of Cu contamination on an ultra-thin Si stacked structure was investigated using an intentional Cu contamination experiment.

The crystal Cu precipitates ranged at 20 nm were observed on the backside of the wafer and they remained at the interface between the adhesive layer and the Si surface. The Cu did not diffuse into the device side even though the wafer thickness less than 5 μm. 200-nm-thick Si damaged layer, formed by #2000 grit grinding, acts as a barrier for Cu diffusion. The light diffusion of Cu was observed in the adhesive layer. Consequently, Cu diffusion can be prevented when the damaged layer formed at the backside of wafer.

Ultra-thin Si 3DI structure having backside damaged layer provides the characteristics that can prevent Cu contamination from diffusing. It enables good performance without device degradation.

Acknowledgements

Part of this work was implemented under the WOW Alliance and the WOW Research Center Corporation. We would like to thank Disco Corporation for wafer thinning, Global Wafers Japan for copper contamination, and Toray Research Center Inc. for TEM and SIMS analyses.

References

[1] T. Ohba et al., Microelectron. Eng., vol. 87, pp. 485–490, 2010.
[2] T. Ohba et al., ECS Trans. vol. 44, no.1, pp. 827–840, 2012.
[3] Y. S. Kim et al., IEDM Tech. Dig., 2009, pp. 365–368.
[4] N. Maeda et al., 2010 Symp. VLSI Tech. Dig., pp. 105–106.
[5] Y. S. Kim et al., 2014 Symp. VLSI Tech. Dig., pp. 1–2.
[6] Y. Mizushima et al., Jpn. J. Appl. Phys., vol. 53, 05GE04, 2014.
[7] A. A. Istoratov et al., J. Electrochem. Soc., Vol.149, No.1, G21, 2002.
[8] K. Hozawa et al., Tech. Dig. IEDM (2002) 737
[9] H. Morinaga et al, IEICE Trans. Electron. E79-C, 343 (1996).

Fig.1 Wafer-on-wafer process flow for Cu contamination experiment.

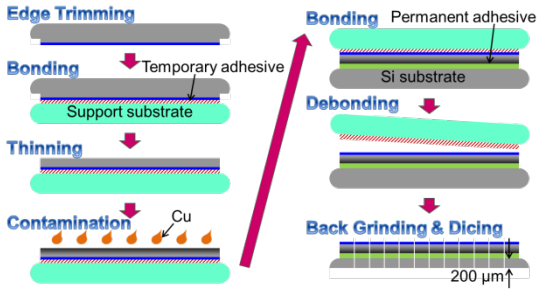


Fig.3 (a) Low magnification cross sectional TEM image. (b) Magnified image of thin Si.

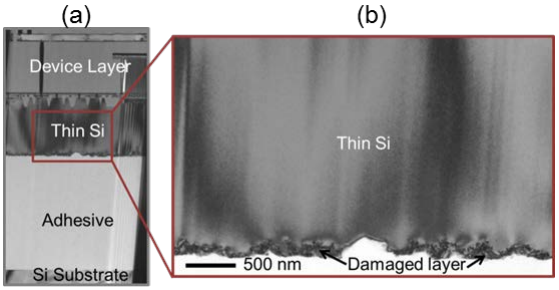


Fig. 5 EDX mapping of thin Si. Cu is detected on the backside and any other elements are not detected on the same position.

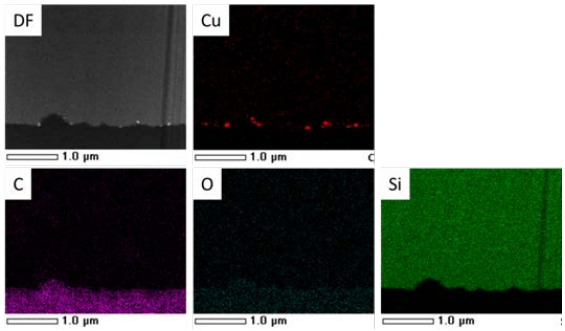


Fig.6 Magnified TEM images of Cu precipitates.

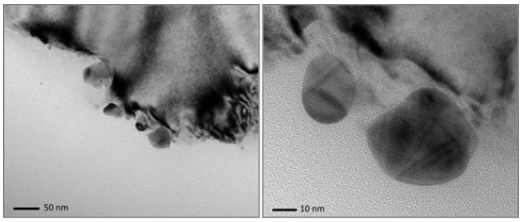
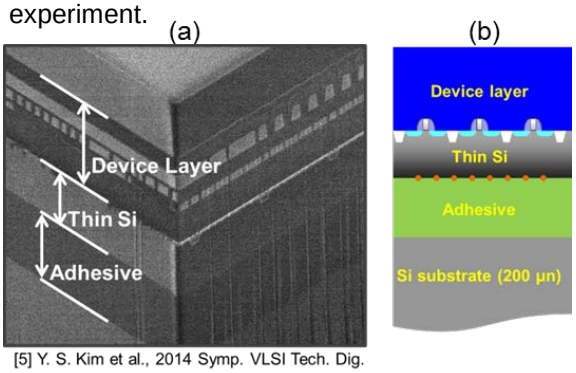


Fig. 2. (a) Cross-sectional SEM image of thinned wafer with thickness of 4 μm fabricated by wow process [5]. (b) Sample structure of this experiment.



[5] Y. S. Kim et al., 2014 Symp. VLSI Tech. Dig.

Fig. 4. (a) BF-STEM image of thin Si. Dark contrast particles are observed on the backside. (b) HAADF-STEM image of thin Si.

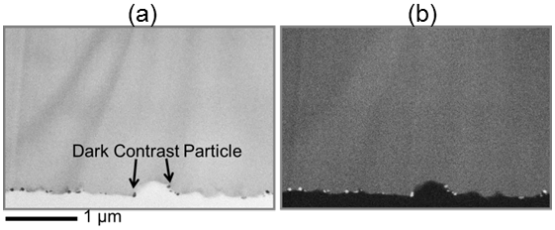


Fig.7 Depth profile of backside TOF-SIMS on adhesive and thin Si layer structure.