Self-aligned graphene on silicon substrates as ultimate metal replacement for nanodevices

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Abstract

We have pioneered a novel approach to the synthesis of high-quality and highly uniform few-layer graphene on silicon wafers, based on solid source growth from epitaxial 3C-SiC films [1,2]. The achievement of transfer-free bilayer graphene directly on silicon wafers, with high adhesion, at temperatures compatible with conventional semiconductor processing, and showing record- low sheet resistances, makes this approach an ideal route for metal replacement method for nanodevices with ultimate scalability fabricated at the wafer –level.

1. Introduction

The large-scale fabrication and exploitation of the outstanding electrical, electronic, thermal, mechanical and optical properties of graphene –based nanodevices have been so far halted by the lack of a suitable method to synthesize graphene in a fashion compatible with semiconductor technology infrastructure and processes.

The reliance on the manipulation of exfoliated or grown graphene flakes to realize devices does not allow for controlled reproducibility, nor defined positioning and dimensions, let alone for a wafer –level fabrication, making graphene integration with the complex structures commonly encountered in nanoelectronics and nano electro-mechanical systems (NEMS) unrealistic. Moreover, the adhesion energy of transferred graphene, although higher than expected, is still so poor for semiconductor technology standards (0.5 J/m^2, [4]) that would make any complex integration or manufacturing efforts void.

Currently, the most realistic route to transfer-free, device-quality graphene directly on semiconductor substrates is based on silicon sublimation from SiC bulk wafers at very high temperatures (1300-1600 ˚C). The high costs of the SiC wafers, as well as their patterning and micromachining, limit this approach to niche applications. Attempts to replicate the success of this methodology through sublimation from the more affordable epitaxial SiC on silicon wafers have invariably shown substantially inferior graphene quality.

2. Graphene on SiC/Silicon through a catalytic alloy

2.1 Synthesis

Silicon carbide films on silicon are an ideal platform for the integration of graphene with silicon technologies, where the SiC acts as a solid source for the graphene. However, in this case, the graphene via silicon sublimation route, which is well- established for bulk silicon carbide wafers, is crucially limited by the lower melting temperature of silicon.

We have explored the sublimation route from epitaxial SiC films on Si and obtained data comparable to the best results available in literature, but realizing the limitations of this technique we have shifted our focus towards the use of metal catalysts.

Earlier efforts in literature using nickel for a catalyst - mediated graphitization at lower temperatures have been dismissed as leading to highly non-uniform graphene. By using a Ni-Cu alloy as opposed to a pure nickel catalyst, we overcome this problem. We report for the first time in literature the achievement of high- quality bilayer graphene around 1050-1100°C on epitaxial SiC on Si by adjusting the ratio of a Ni:Cu alloy catalyst film, and provide explanation through basic Thermodynamics. As the graphene is obtained at the SiC/metal interface, the catalytic layer can be removed via wet etch, leaving behind the graphene on SiC ready to be used in a device with no need for manual transfer (Fig.1) [1]. As a result, the graphene covers uniformly a 2” silicon wafer with a Raman I_D/I_G band ratio below 0.2, indicating low defectivity. Moreover, we show that this approach can be used with both SiC(111) and SiC(100) surface orientations, as opposed to the sublimation technique [2].

2.2 Self-aligned patterning

As the SiC acts as the solid source for the carbon atoms of the graphene, and patterning of the SiC on Si can be carried out through well-established photolithography and etching processes, we demonstrate that this synergy of properties can be used to obtain a graphene patterned through simple

selective, self- aligned processes (Fig.2). Critical dimensions by this simple approach can potentially reaching down to a few nanometers.

To demonstrate the site-selectivity of this approach, we present a demonstration of the wafer-level fabrication of graphitized silicon carbide microstructures. Suspended single- (cantilevers) and double-clamped (bridges) microbeams are used as basic components in MEMS technologies for resonant sensing and energy harvesting applications. Graphene can here replace the conventional metal layer necessary for the actuation and readout of such structures, avoiding limitations given by plastic dissipation in the metal layer, and the strong resistivity limitations of classical metals due to size effects when the conduction is confined to nm thick/wide metal.

3. Properties

TEM cross-sections show that the obtained bilayer graphene is around 1 nm thick (Fig.3). Raman spectroscopy yields an I_D/I_G ratio of about 0.2, indicating this as the highest quality graphene grown in-situ on silicon substrates.

In addition, fracture measurements by four point bending indicate that this bilayer graphene on SiC on silicon system possesses an adhesion/cohesion energy at least an order of magnitude higher than transferred graphene on silicon substrates, which is a property of paramount importance for fabricating reliable devices on silicon.

4. Summary

We demonstrate a transfer-free, self-aligned synthesis of bilayer graphene on silicon carbide, through wafer-level silicon technology processes. In contrast to sublimation-based routes, the synthesis of graphene takes place at a temperature compatible with Si technology, yielding a graphene coating with low defectivity and able to act as an exceptional conducting layer. These results point towards a fundamental paradigm shift, offering the ultimate advantage for miniaturisation of electrical devices: superior performance due to the exceptional conduction at the nanoscale of graphene, superior mechanical reliability together with transfer-free uniform synthesis at the wafer scale on silicon substrates.

Beyond the exemplified impact as metal replacement for SiC based MEMS devices, this process opens the avenue for large-scale fabrication of graphene micro- and nanostructures for countless electronic, photonic, opto-mechanical and sensing applications.

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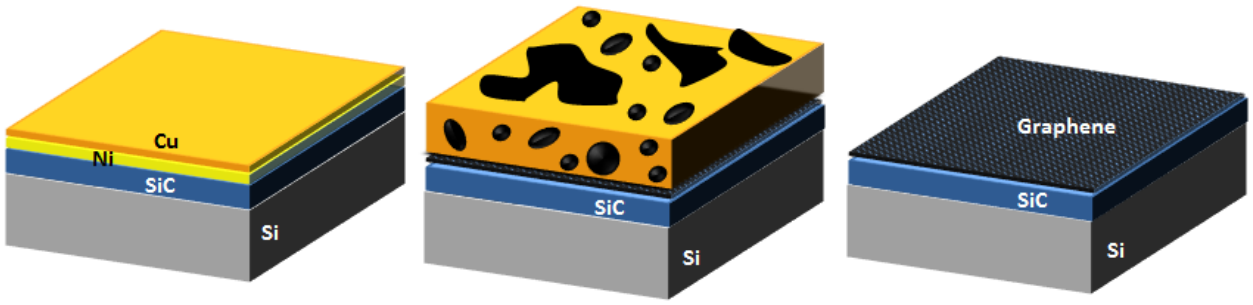

Fig.1 Schematic of the sequence for the catalytic alloy synthesis of graphene on silicon carbide: (left) thin catalyst layers are deposited on the SiC, (centre) as the sample is annealed, silicides are formed and the carbon is released into the metal alloy, while part of it is crystallized as graphene on the surface of the SiC, and (right) the graphene layer on SiC is exposed after the wet etching of the intermixed and reacted alloy.

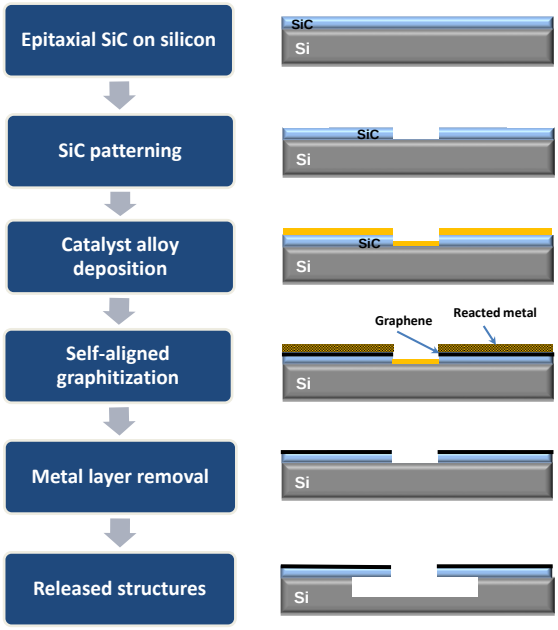

Fig. 2 Schematic of the self-aligned patterning sequence of graphene

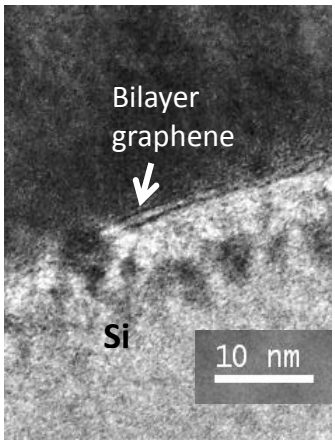

Fig. 3 High resolution transmission electron microscopy micrograph showing the bilayer graphene