NiCo 10 at%: A promising silicide alternative to NiPt 15 at% for thermal stability improvement in 3DVLSI integration

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Abstract

3D VLSI with a CoolCube^{TM} process allows vertically stacking several layers of devices with a unique connecting via density above a million/mm². The thermal budget allowed to process the top transistor is currently limited by NiPt silicide stability of the bottom transistor. To extend the upper transistors thermal process window, Pre-Amorphization Implant (PAI) and Si-Capping were used to improve the stability of $NiPt_{15\%}$ on SiC:P and $SiGe_{30\%}$:B accesses. While PAI enhances the silicide stability on SiC:P substrate from 600°C 2h to 700°C 2h, neither PAI nor Si-Capping improve silicide stability on $SiGe_{30\%}$:B. To provide a solution for P accesses stability, $NiCo_{10\%}$ silicidation has been developed. Combined with PAI and Si-Capping, the germano-silicide offers a higher stability (up to 600°C 2h) than its $NiPtSi_{15\%}$ counterpart.

1. Introduction

3D VLSI, also named 3D sequential integration offers an alternative to traditional scaling challenges providing area and performance gain without scaling the transistors dimensions [1]. In this integration, the stacked transistors are processed sequentially, thus implying the reduction of the top transistors thermal budget in order to preserve the bottom level (Fig.1).

The maximum thermal budget that a transistor can suffer will depend on the technology considered. The stability of FDSOI technology has been evaluated in several studies which furnish evidence that $NiPt_{10\%}$ and $NiPt_{15\%}$ silicide, used in the source and drain contact, are the most unstable components and sets the maximum temperature of upper level process steps around 500 °C for anneals in the hour range [2, 3, 4]. In addition, the use of $SiGe_{30\%}$:B for the p-MOS source and drain transistors exacerbates the silicide instability [5]. This maximal temperature sets important constraints on the top FET process. Indeed, Table 1 lists the critical thermal budgets in a standard FDSOI device process flow that need to be reduced below 500°C. Currently, solutions have been demonstrated to replace the conventional dopant activation (1050°C spike anneals): devices with Solid Phase Epitaxy regrowth reach the performance of standard high temperature activation [6]. Also, nanosecond laser anneal allow efficient activation of dopants and the temperature seen by the bottom MOSFET can be kept below 500°C [3]. For the spacer deposition, low-k dielectrics needed for capacitance reduction offers opportunities of thermal budget reduction. Finally considering epitaxy temperature, 500°C $SiGe_{35\%}$ has been demonstrated [7]. However, the reduction of Si epitaxy temperature below 600°C is still facing some challenges. Therefore, relaxing the maximum thermal budget from 500°C to at least 600°C will enable to have a full process flow for top FET compatible with 3DVLSI.

Different alternatives are proposed in the literature to postpone the morphological silicide degradation on Si: PAI before metal deposition [8, 9], increasing concentration of Pt, Dynamic Surface Anneal (DSA) in place of Rapid Thermal Anneal [10]. In the case of SiGe, the insertion of silicon capping layer (Si-Cap) at metal/SiGe interface has shown promising results [9]. Recently, $NiCo_{10\%}$ salicidation has been demonstrated to extend the silicide stability on $SiGe_{20\%}$ [11].

The aim of this research is to find a silicidation process with the highest stability on in-situ doped accesses for both N& PFET (SiC:P and $SiGe_{30\%}$:B respectively). It compares the thermal stability of both $NiPt_{15\%}$ and $NiCo_{10\%}$ germano-silicides combined with various process improvements such as pre-amorphization implantation (PAI) and the insertion of silicon capping layer at metal/SiGe interface. In addition, the stability of $NiPt_{15\%}$ on Si substrate combined with PAI has been studied.

2. Experiment

Both silicides have been studied on 300 mm blanket Si wafers. At first, 19 nm of SiC in-situ doped with Phosphorous or 15 nm of $SiGe_{30\%}$ in-situ doped with Boron were grown by epitaxy in order to mimic FDSOI source and drain. Fig.2 summarizes all the variants that have been tested including PAI and Si capping for $NiCo_{10\%}$ and $NiPt_{15\%}$ silicidation. After full silicidation process, the samples were annealed with various thermal treatments (Table 2).

Previous investigations have shown the appeal of Si Cap on SiGe in reducing the leakage current by suppressing the migration of Ni inside the channel [9] and the agglomeration of Ni-germano-silicide [9]. In this study, the integration of a 5 nm Si-Cap was performed on several $SiGe_{30\%}$:B samples.

In the literature, PAI was introduced to favor the low resistive phase C49-$TiSi_2$ [8] by increasing the nucleation driving force and to increase the silicidation reaction rate as compared to metal/crystalline silicon layer [12]. This process was adapted to $NiPt_{15\%}$ and $NiCo_{10\%}$ silicides and germano-silicide using Ge implantation at 4keV, $1x10^{15}cm^{-2}$.

7 nm of metal alloy ($NiPt_{15\%}$ or $NiCo_{10\%}$) were deposited by physical vapor deposition (PVD) prior to both rapid thermal anneals (RTA1 and RTA2) performed in N_2 atmosphere for 30 s. The RTA1 for $NiPt_{15\%}$ silicide corresponds to the one employed in the state of the art planar FDSOI integration (230°C 30s). By contrast, $NiCo_{10\%}$ RTA1 temperature (280°C 30s) has been determined from the transformation curve (Fig. 3).

Morphological studies before and after thermal treatments were made by Scanning Electron Microscopy (SEM) observations while silicides phases were characterized by in-plane X-Ray Diffraction (XRD). The quantity of cobalt (Co) incorporated into the silicide was measured by Wavelength Dispersive X-Ray Fluorescence (WDXRF). Finally, the sheet-resistance (Rs) was measured by a four-points-probe system.

3. Results and Discussion

3.1 $NiCo_{10\%}$ salicidation process development

The $NiCo_{10\%}$ transformation curve on silicon determined by sheet resistance as function of temperature process (Fig. 3) can be divided into 4 parts. In the first one, Rs decreases with temperature because the silicide thickness grows. Then, a plateau is reached (part 2), corresponding to the full consumption of $NiCo_{10\%}$ layer forming NiCo-rich phase but the temperature is too low for mono-silicide nucleation. In Part 3, the Rs decrease is linked to the formation of a phase with a lower resistivity (part 4). The transformation curve enable to define the adapted RTA1 and RTA2 conditions respectively fixed to 280°C 30s and 390°C during 30s. Note that the RTA2 conditions are identical for $NiCo_{10\%}$ and $NiPt_{15\%}$. The integration of $NiCo_{10\%}$ is very close from the standard $NiPt_{15\%}$ process. Indeed, similar thermal budgets and same chemistry for metal removal have been used. Thus its integration in a transistor flow does not require additional developments.

3.2 Silicide thermal stability evaluation

The stability of $NiPt_{15\%}$ silicide on SiC:P or $SiGe_{30\%}$:B substrates with and without PAI and Si-Cap is evaluated by sheet resistance measurements (Fig. 5). The $NiPt_{15\%}$ on SiC:P is already stable up to 600 °C 2h. Between 400°C and 600°C, a 15 % sheet resistance improvements is observed. This may be due to the silicide grains enlargement. Thanks to the PAI implant, the $NiPt_{15\%}$ stability is extended to 700 °C 2 hours. The situation is less favorable for the $SiGe_{30\%}$:B substrate, the instability of $NiPt_{15\%}$ appears at 500 °C 2 h, even with a Si-Cap. This is mainly due to the Ge out-diffusion of the NiPtSiGe phase which forms Ge-enriched Si-Ge grains next to the silicide as already described in [12]. Moreover, the PAI has no particular effect on the $NiPt_{15\%}$ stability on $SiGe_{30\%}$ layer. Thus, from this first electrical analysis, it seems that stability improvement for $NiPt_{15\%}$ on SiC:P layer is possible through PAI process step. However a specific focus is needed to improve the silicide stability on $SiGe_{30\%}$ substrate.

$NiCo_{10\%}$ has been proposed in literature as an alternative to $NiPt_{10\%}$ for silicide stability improvement on $SiGe_{20\%}$ [11]. Similar trend is observed here on $SiGe_{30\%}$ with in situ boron doping. Thanks to $NiCo_{10\%}$ silicidation and Si-capping, the stability is ensured up to 600°C while it was limited at 500°C with $NiPt_{15\%}$.

The stability improvement brought by $NiCo_{10\%}$ is even more evident for temperature beyond 600°C. Moreover, the introduction of Si-Cap above $SiGe_{30\%}$ for $NiCo_{10\%}$ further improves the silicide stability. In other words, Rs degradation of 300 % is observed for $NiPt_{15\%}$ at 700 °C 2 h relative to the post RTA2 measurement, while only 5 % of Rs degradation for $NiCo_{10\%}$ is measured. $NiCo_{10\%}$ and $NiPt_{15\%}$ react differently to thermal budget due to the behavior of the additional species: Pt and Co. While Pt is soluble in NiSi and provides the benefit of PtSi thermal stability, Co is not soluble in the Ni mono-silicide [13] and should redistribute at the grain boundary during the formation. This must change surface and interface energies leading to a better morphological stability.

3.3 $NiCo_{10\%}$ silicides identification

In plane XRD configuration was chosen in order to identify the phases formed by the silicide process formation and the phases obtained after a 500°C 2h anneal. This configuration scans the perpendicular plan to the sample surface and thus allows increasing the signal of ultrathin layer. Peak position of $NiCo_{10\%}$ monosilicide has been determined with NiSi patterned diffraction. Positions are shifted to low angle meaning that unit cell parameter is larger than NiSi due to the presence of Co and Ge (Fig. 4). After 500°C, same peaks are observed but display higher intensity and a shift toward high 2 theta. One can conclude that grain growth occurred during the annealing but slight change is observed. However, the change in peak position suggest that Ge, Co or both are probably rejected from the unit cell if no stress effect intervened.

3.4 Morphological observations and WDXRF analyses

SEM top view observations of $NiCo_{10\%}$ and $NiPt_{15\%}$ samples on $SiGe_{30\%}$:B substrate with Si-Cap post RTA2 and post 600 °C 2h anneal are shown in Figure 7. Post RTA2, for both silicides the films are smooth and continuous (Fig. 7-ab). At 600°C 2h both silicides are damaged (Fig. 7-cd). Two phenomena occur with $NiPt_{15\%}$: grain coalescence (consistent with XRD) and agglomeration. By contrast, only grain coalescence occurs with $NiCo_{10\%}$ and the grains are larger. This different behavior can partly explain Rs tendencies (Fig. 6) and confirm the improved stability of $NiCo_{10\%}$ compared to $NiPt_{15\%}$ on $SiGe_{30\%}$:B substrate with Si-Cap.

Note that the percentage of Co in the NiCo target is 10 at%. The WDXRF analyses reveal that deposited NiCo film actually contains 10 at% but after RTA1 280°C 30s, only 8.6 at% of Co has been incorporated in the silicide. This value is lower compared to the 15 at% of Pt in NiPt silicide and confirms the excellent efficiency of cobalt at low concentration.

4. Summary

In order to relax the maximum thermal budget allowed for top processing in CoolCube™ integration, bottom transistors silicide stability must be improved. Thanks to PAI, the thermal stability of $NiPt_{15\%}$ on SiC:P sample is extended from 600°C 2h to 700°C 2h. However on a $SiGe_{30\%}$:B substrate $NiCo_{10\%}$ seems more promising. Thanks to Rs measurement and top view observations, NiCo (with only 8.6% of cobalt) with both Si capping and PAI offers the best stability. This thermal stability could be further improved by incorporating higher cobalt concentration during the NiCo silicide processing.

Acknowledgement

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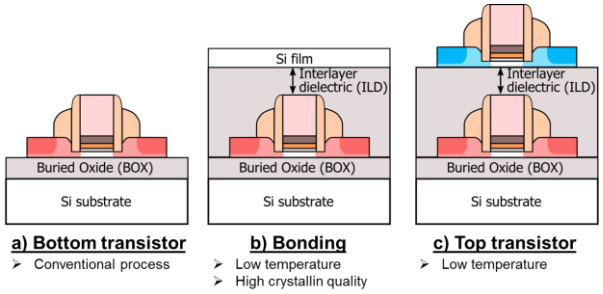

Figure 1: CoolCube integration – a) Conventional process for bottom transistor b) low temperature bonding leading to high Si crystalline quality (from SOI wafer, bond and etch back) c) Low temperature top transistors integration.

Pocess step	Planar Technology
Offset nitride spacer	630°C 3h
Si Epitaxy	750°C 10min
SiGe Epitaxy	650°C 10min
Dopant activation	>1000°C spike

Table 1: Critical thermal budgets in a FDSOI process flow for bottom transistors performance preservation.

Annealing Temperature		
450°C 2h	500°C 2h	600°C 2h
700°C 2h		800°C 2h

Table 2: Thermal treatments performed post RTA2 on both silicides for silicon and silicon-germanium substrates.

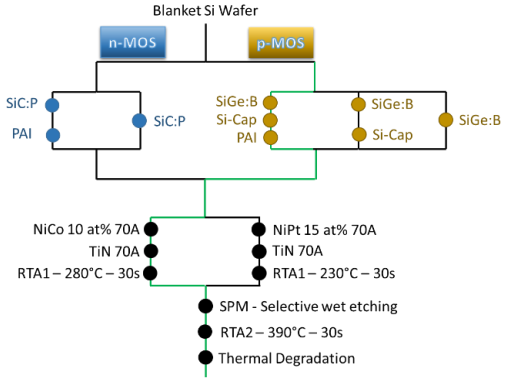

Figure 2: Process flow with all the silicide variants. pMOS best result in term of thermal stability is highlighted in green.

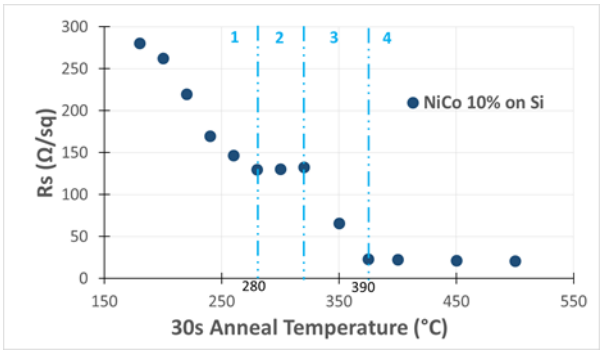

Figure 3: Sheet resistance of $NiCo_{10\%}$ 7 nm on Si substrate as function of 30s RTA temperature after metal selective etch.

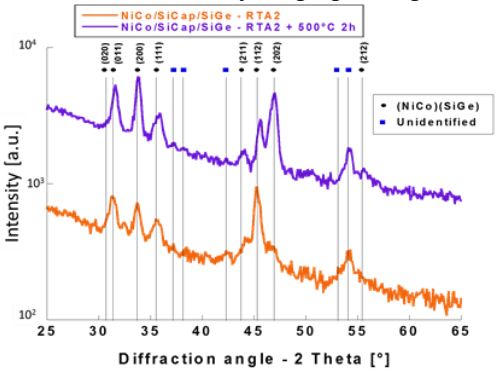

Figure 4 : In plane X-Ray Diffraction of NiCo/Si-Cap/SiGe after silicide formation and an additional annealing at 500 °C 2 h.

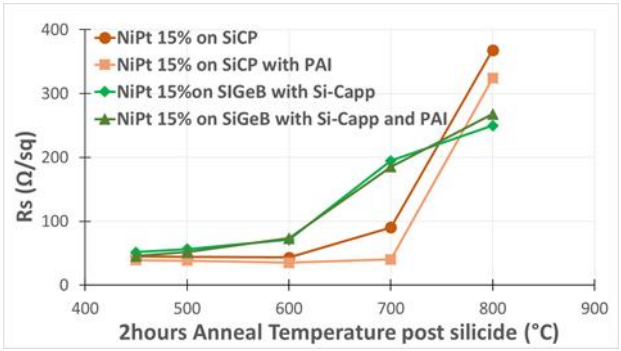

Figure 5: Sheet resistance of $NiPt_{15\%}$ on SIC:P and $SiGe_{30\%}$:B materials versus annealing temperature during 2h.

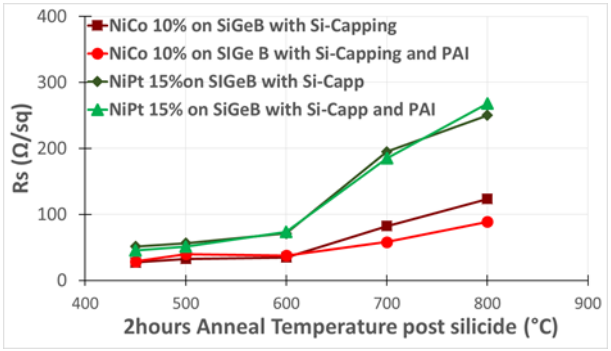

Figure 6: Comparison between $NiCo_{10\%}$ and $NiPt_{15\%}$ germano-silicide versus post silicide annealing temperature.

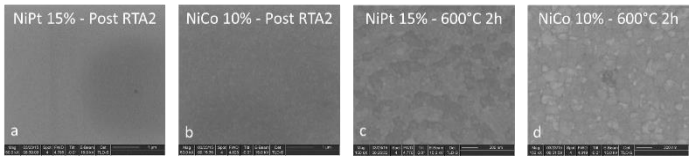

Figure 7: Top view observation of $NiPt_{15\%}$ and $NiCo_{10\%}$ on germano-silicide with Si-Capping and PAI post RTA2 and after annealing at 600°C during 2h.