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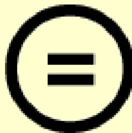

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ULSAN NATIONAL INSTITUTE OF
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Doctoral Thesis

# Epitaxial Graphene and its Electronic Device Applications

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Department of Electrical Engineering

Graduate School of UNIST

2018

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

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ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

# Epitaxial Graphene and its Electronic Device Applications

A thesis/dissertation
submitted to the Graduate School of UNIST
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

Hanbyul Jin

11. 17. 2017

Approved by

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# Epitaxial Graphene and its Electronic Device Applications

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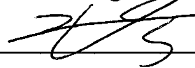

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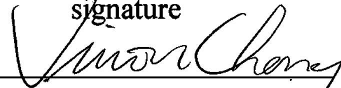

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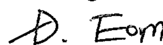

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# Abstract

Graphene is a two-dimensional material in which carbon atoms are bonded in honeycomb lattice. It has a unique electronic band structure that shows zero band gap energy and linear dispersion relation near the Dirac point. Because of to its outstanding electrical and mechanical properties, graphene has been actively studied in various fields. After successfully separating graphene from highly oriented pyrolytic graphite (HOPG), a variety of methods for obtaining high quality and large area graphene have been studied. Especially, a method of growing epitaxial graphene (EG) on a SiC substrate has attracted much attention as a material for next generation electronic devices. This allows the growth of large area graphene and it is not necessary for transfer process because semi-insulating SiC wafer can be used as a substrate. However, it has disadvantages of requiring high temperature (> 1300 °C) for high quality EG growth and the single crystalline SiC substrate are too expensive.

In order to overcome these problem, we propose two effective methods for growth of EG on SiC. Firstly, the high quality EG is grown on 4H-, 6H SiC substrate by molybdenum plate (Mo-plate) capping during annealing process. Mo-plate capping causes the heat accumulation on SiC surface by preventing loss of thermal radiations from SiC surface, and increase the Si vapor pressure on SiC surface by enclosing the sublimated Si atoms. Therefore, the temperature of the SiC surface becomes higher than surrounding temperature, and the Si sublimation rate is reduced. These factors enable high quality EG growth at relatively low power assumption (chamber temperature). The quality enhancement of the grown EG with Mo-plate capping is demonstrated by Raman spectra, compared to EG without Mo-plate capping. Secondly, the graphene is formed on SiC thin film surface at relatively low temperature by electron beam (e-beam) irradiation with low acceleration voltage. The e-beam irradiation with low acceleration voltage induces the heat accumulation within several layers of SiC thin film surface due to its shallow penetration depth. The thermalized electrons weaken the bond strength of the Si-C atoms while staying within a few layers of SiC thin film surface, which reduce the heat energy required for sublimating Si atoms. As the electron fluency increase, the crystallinity and uniformity of grown graphene are improved, which is confirmed by Raman spectra and scanning electron microscopy (SEM) images.

We propose the cleanly patterning method for graphene using Al thin film as etching mask because general patterning methods such as electron beam lithography and photolithography induce the degradation of graphene quality due to polymer residue. The properties of fabricated graphene device using Al thin film are confirmed by Hall measurement and Raman spectra, compared with graphene sample patterned with conventional photolithography. In particular, the apparent Shubnikov-de Haas (SdH) oscillation measured in graphene device patterned with Al thin film demonstrates better homogeneity and 2DEG system. The carrier density and Hall mobility in Al patterned EG device are measured to be $9.16 \times 10^{12}$ $cm^{-2}$ and ~ 2100 $cm^2/Vs$, respectively.

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The complementary logic inverter having graphene channel is fabricated by using selective doping of graphene. Ti or Al adsorbed graphene is doped n-type, because Ti or Al with lower work function than graphene induces the charge transfer from the Ti or Al to graphene. On the other hand, the $SiO_2$ adsorbed graphene is doped to p-type by the dangling bonds of $SiO_2$ surface. The doping concentration and type of graphene are confirmed by Raman spectra and electrical measurements. We fabricated two kinds of inverter doped with Al-$SiO_2$ and Ti-$SiO_2$ materials. These inverters exhibit a clear voltage inversion as function of $V_{in}$ at a wide range of $V_{DD}$ from 0.5 V to 20 V, and the highest voltage gains are ~0.93 and ~0.86, respectively. These properties can be improved by using insulating layer of higher dielectric constant and reducing thickness of gate oxide.

We propose a new structure of multifunctional capacitive sensor to surmount the limitations the previous single-capacitor sensor. The proposed dual-capacitor sensor composes of two capacitors stacking vertically in a pixel which detects strength information and surface-normal directionality of external stimuli, and clearly classifies the types of stimuli. These properties have been demonstrated by detecting and distinguishing the curvature, pressure, touch and strain stimuli through the capacitances changes of the two capacitors.

We successfully fabricated a stable n-type InAs NW FET with a very simple fabrication process using pre-deposition of $Al_2O_3$ layer. This oxide layer of 10 nm thickness is uniformly formed on entire surface of NW channel by ALD. It serves not only as a gate oxide but also as a protective layer of the NW channel. The structure of completed device is demonstrated by TEM images and EDX electron mapping. The n-InAs NW FET shows good current saturation and low voltage operation, the peak transconductance ($g_m$) is extracted to be 13.4 mS/mm, the field effect mobility ($\mu_{FE}$) is calculated to be ~1039 cm$^2$/Vs at $V_{DS}$ = 0.8 V and current on/off ratio is about ~750.

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# Nomenclature

| | |
|---|---|
| **EG** | Epitaxial Graphene |
| **e-beam** | Electron Beam |
| **SEM** | Scanning Electron Microscopy |
| **SdH** | Shubnikov-de Haas |
| **2DEG** | Two-dimensional Electron Gas |
| **TEM** | Transmission Electron Microscopy |
| **HRTEM** | High Resolution Transmission Electron Microscopy |
| **BRTEM** | Bright Field Transmission Electron Microscopy |
| **EDX** | Energy-dispersive X-ray Spectroscopy |
| **QHE** | Quantum Hall Effect |
| **IQHE** | Integer Quantum Hall Effect |
| **FQHE** | Fractional Quantum Hall Effect |
| **HOPG** | Highly Oriented Pyrolytic Graphite |
| **CVD** | Chemical Vapor Deposition |
| **SiC** | Silicon Carbide |
| **UHV** | Ultra High Vacuum |
| **LEEM** | Low-Energy Electron Microscopy |
| **CCS** | Confinement Controlled Sublimation |
| **AFM** | Atomic Force Microscopy |
| **RIE** | Reactive Ion Etching |
| **UV** | Ultraviolet |

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| | |
|---|---|
| **STM** | Scanning Tunneling Microscope |
| **Mo-plate** | Molybdenum plate |
| **FWHM** | Full Width at Half Maximum |
| **FET** | Field Effect Transistor |
| **GFET** | Graphene Field Effect Transistor |
| **MOSFET** | Metal Oxide Semiconductor Field Effect Transistor |
| **XPS** | X-ray Photoelectron Spectroscopy |
| **PECVD** | Plasma Enhanced Chemical Vapor Deposition |
| **PMMA** | Polymethyl-methacrylate |
| **TMA** | Trimethylaluminum |
| **CNP** | Charge Neutral Point |
| **EEG** | Electroencephalogram |
| **ECG** | Electrocardiogram |
| **NW** | Nanowire |
| **AgNW** | Silver Nanowire |
| **PDMS** | Polydimethylsiloxane |
| **IoT** | Internet of Things |
| **MOCVD** | Metal Organic Chemical Vapor Deposition |
| **IPA** | Isopropyl Alcohol |
| **FIB** | Focused Ion Beam |

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# I. Overview

Graphene is a single layer of $sp^2$ bonded carbon atoms arranged in a honeycomb lattice [1-6]. Due to its outstanding electronic properties and unique electronic band structure of zero band gap around Dirac point, graphene has been extensively studied in various application fields for future nanoelectronics and unique physical properties [1-3, 6]. Several methods of synthesizing graphene have been proposed, and studies for high quality graphene growth in a wide area are still being actively conducted [5, 7-10].

Before introducing the research conducted during doctoral course, we introduce the basic characteristics of graphene such as crystal structure and electronic band structure, and explain representative methods for graphene synthesis. I have discussed epitaxial graphene (EG) in more detail, which is main topic in my doctoral research.

Two methods are suggested for effective growth of EG at relatively low temperature. First, the EG of enhanced crystallinity is formed on Hexagonal (4H-, 6H-) SiC substrate by molybdenum plate (Mo-plate) capping [11]. The quality improvement of the grown EG with Mo-plate capping is evidenced by Raman spectra, compared to EG without Mo-plate capping. Mo-plate capping during annealing SiC substrate lead to heat accumulation on SiC surface by preventing loss of thermal radiations, and increase the Si atoms vapor pressure on SiC surface covered with Mo-plate by enclosing the sublimated Si atoms. These factors contributed to the growth of high quality EG. Second, the graphene is grown on surface of amorphous SiC film by irradiation electron beam (e-beam) with low acceleration voltage. As the electron fluency increase, the crystallinity and uniformity of grown graphene are enhanced, which is demonstrated by Raman spectra and scanning electron microscopy (SEM) images. The e-beam irradiation with low acceleration voltage can only anneal a few layers of SiC thin film surface due to the shallow penetration depth. The thermalized electrons stayed within near SiC thin film surface weaken the bond strength of Si-C atoms, which reduces the thermal energy required for sublimation of Si atoms. Through these factors, the graphene can be grown on surface of the SiC thin film by e-beam irradiation at significantly low temperature as compared to conventional heating method.

In order to prevent degradation of graphene quality due to polymer residue during patterning process [12-17], we suggest effective graphene patterning method using Al thin film as an etching mask. The excellence of the proposed patterning method is demonstrated by the Hall measurement and Raman spectrum, compared to graphene device fabricated using conventional photolithography. The Shubnikov-de Haas (SdH) oscillations of an EG device using by Al thin film as an etch mask is very apparent, whereas an EG sample using photoresist as an etch mask by photolithography shows an ambiguous SdH oscillations including a lot of noise signals. It means that the EG device using Al thin film has cleaner, more homogeneous two-dimensional electron gas (2DEG) system because polymer residue is not remained on EG surface [18]. The carrier density and Hall mobility of completed EG device fabricated with Al thin film are measured as $9.16 \times 10^{12}$ $cm^{-2}$ and ~ 2100 $cm^2/Vs$, respectively.

The stable complementary logic graphene inverter is fabricated by graphene doping with Ti, Al, and

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$SiO_2$ thin film. The $Al_2O_3$ is used as passivation layer. The Ti and Al thin films with lower work function than graphene induce the n-doping of graphene by charge transfer from the metal to graphene [19, 20]. By contrast, the graphene adsorbed on $SiO_2$ is doped p-type by the dangling bond of O-terminated $SiO_2$ [21, 22]. The doping concentration and type of graphene are demonstrated by Raman spectra and I-V curve of completed graphene field effect transistor (GFET). The graphene inverter device shows stable operation and clear voltage inversion as function of $V_{in}$ at a wide range of $V_{DD}$ from 0.5 V to 20 V. The highest voltage gain is defined to ~0.93 and ~0.86 for graphene inverters doped with Al-$SiO_2$ and Ti-$SiO_2$ materials. These values can be improved by using gate oxide with lower thickness and higher dielectric constant.

We propose a new structure of multi-functional capacitive sensor compose of two vertically-stacked capacitors (dual-capacitor) [23]. It can clearly detect and distinguish the external stimuli such as curvature, pressure, strain, and touch using changes of $\Delta C_1$ and $\Delta C_2$ of the dual-capacitor multifunctional sensor. In case of curvature, pressure and contact, the information of surface-normal directionality is also detected.

The n-InAs NW field effect transistor (FET) is effectively fabricated by pre-deposing $Al_2O_3$ on whole surface of n-InAs NW channel. The $Al_2O_3$ layer of 10 nm thickness is uniformly coated by atomic layer deposition (ALD), it is used as a passivation layer as well as a gate insulator for the channel. Metal deposition and photoresist coating are performed only once during the entire process. The cross-sectional structure of completed device is confirmed by Transmission electron microscopy (TEM) images and energy-dispersive X-ray spectroscopy (EDX) electron mapping. A fabricated n-InAs NW FET shows good current saturation and low voltage operation, the peak $g_m$ is obtained to be 13.4 mS/mm, the $\mu_{FE}$ is calculated to be ~1039 $cm^2/Vs$ at $V_{DS}$ = 0.8 V and current on/off ratio is about ~750.

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## II. Introduction to Graphene

Graphene is a single layer of $sp^2$ bonded carbon atoms arranged in a hexagonal shape. It is a basic building block of various carbon structure such as 3D graphite, 1D carbon nanotube, and 0D bulky ball as shown in Figure 2.1 [2]. Due to its remarkable electronic properties, graphene has received great attention and has been extensively studied in various fields [1-3, 6]. It is considered a leading material for future nanoelectronic devices. Graphene shows outstanding characteristics such as high mobility over 200,000 $cm^2$/Vs [24], high thermal conductivity about 5000 W/mK [25, 26], transparency of 97.3 % [27], high tensile strength of 1100 GPa and flexibility [28]. Moreover, some novel physical phenomena such as quantum Hall effect (QHE) [3, 4, 29] and Klein tunneling are also observed in graphene [30, 31].

The theoretical study about the band structure of single carbon layer had been accomplished in 1947 by Wallace *et al* [32]. However, it was considered that the single atomic carbon layer could not exist because of its thermal instability. The research group of Andre Geim isolated single carbon layer from graphite by exfoliation method. They won the Nobel Prize for Physics in 2010 for their research on the development of this technology and graphene.

In this chapter, we introduce the basic characteristics of graphene, synthesis methods of graphene, EG on SiC substrate, and QHE. Since EG is important in my graduation dissertation, we have covered it in more detail than other types of graphene.

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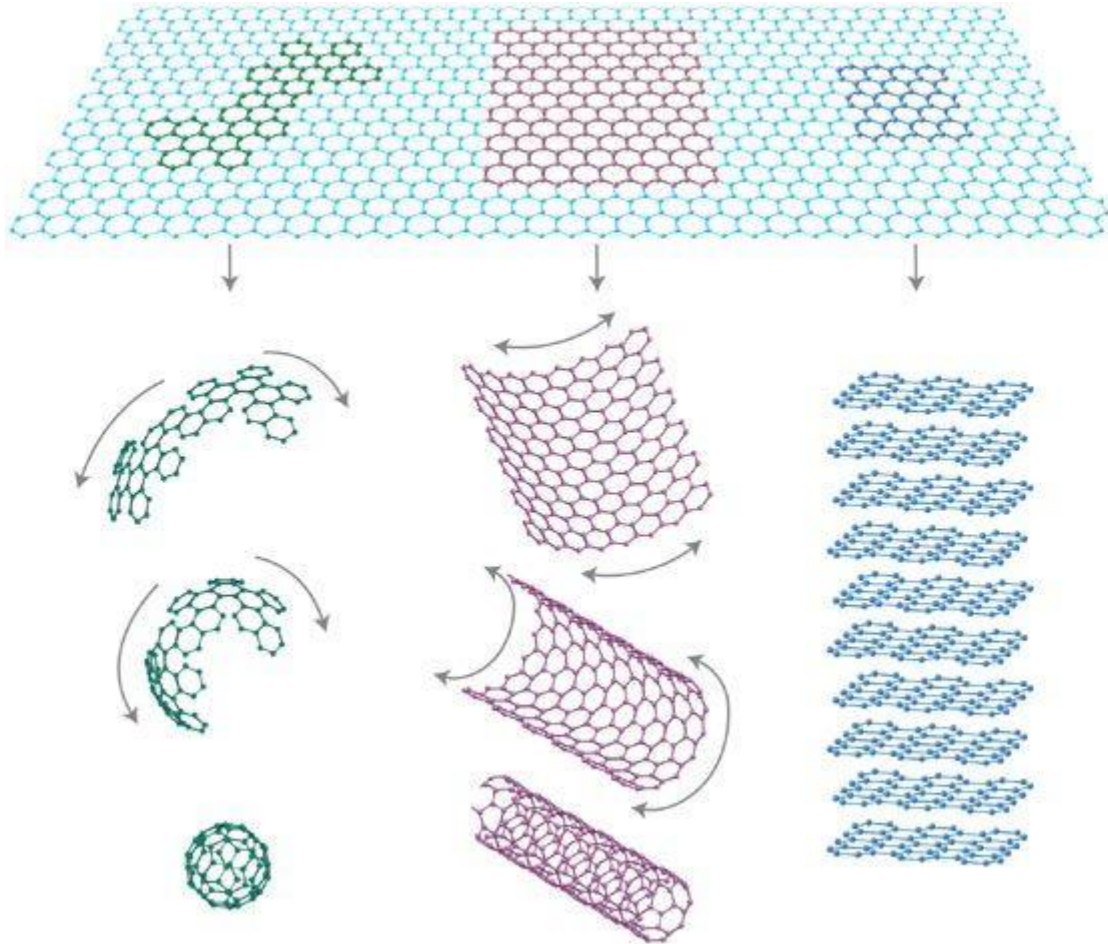

Figure 2.1: Graphene is a component of carbon materials of different dimensions [2].

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## 2.1 Graphene Characteristics

### 2.1.1 Crystal Structure

The graphene is a two dimensional material in which carbon atoms arranged in hexagonal lattice. The carbon atoms have an electronic structure of $1s^2 2s^2 2p^2$ and each carbon atom form $sp^2$ orbitals. These orbitals are arranged at an angle of 120 degree on the X-Y plane, so that the graphene shows a honeycomb lattice. Figure 2.2 shows the graphene lattice structure in real space and corresponding reciprocal lattice with first Brillouin zone [2, 33-35]. The primitive cell comprises two vectors of $\mathbf{a_1}$ and $\mathbf{a_2}$ including two inequivalent atoms. It is represented by green dotted line. (Figure 2.2(a)). The vectors of $\mathbf{a_1}$ and $\mathbf{a_2}$ are expressied by

$$\mathbf{a_1} = a_0\left(\frac{\sqrt{3}}{2}, \frac{1}{2}\right), \quad \mathbf{a_2} = a_0\left(\frac{\sqrt{3}}{2}, -\frac{1}{2}\right) \tag{2.1}$$

where $a_0 = |\mathbf{a_1}| = |\mathbf{a_2}| = \sqrt{3}b$, the space between two nearest carbon atoms (lattice constant) is $b = 0.142$ nm. The vectors of $\mathbf{a_1}$ and $\mathbf{a_2}$ have the same length and an angle of $\pi/3$. The area of primitive cell is $\pi/3$

In the reciprocal *k*-space, the primitive cell of reciprocal graphene is spanned by two vectors of $\mathbf{b_1}$ and $\mathbf{b_2}$, which have the same length and an angle of $2\pi/3$. They are given by

$$\mathbf{b_1} = \frac{2\pi}{a_0}\left(\frac{1}{\sqrt{3}}, 1\right), \quad \mathbf{b_2} = \frac{2\pi}{a_0}\left(\frac{1}{\sqrt{3}}, -1\right) \tag{2.2}$$

Here, the primitive vectors of reciprocal lattice ($\mathbf{b_1}$, $\mathbf{b_2}$) and crystal lattice ($\mathbf{a_1}$, $\mathbf{a_2}$) are related by $\mathbf{a_i} \cdot \mathbf{b_j} = 2\pi\delta_{ij}$ with $i, j = 1, 2$.

### 2.1.2 Electronic Band Structure

Each carbon atom in graphene has four valence electrons, three of which electrons are bonded to neighboring carbon atoms in the plane by strong covalent sigma ( $\sigma$ ) bonding, which provides outstanding mechanical properties of graphene but do not contribute to conduction. The remaining electron forms the pi ( $\pi$ ) bonding that contributes to the electronic properties of graphene at low energy. The energy band structure of $\pi$ -electron for graphene was calculated by using a tight binding approximation in 1947 by Wallace *et al* [32]. If we consider only nearest neighbor interaction, the energy dispersion of $\pi$ -electron is obtained as

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$$E_{\pm}(\mathbf{k}) = \pm\gamma\left[1+4\cos\left(\frac{\sqrt{3}k_x a_0}{2}\right)\cos\left(\frac{k_y a_0}{2}\right)+4\cos^2\left(\frac{k_y a_0}{2}\right)\right]^{1/2} \tag{2.3}$$

where $E_{\pm}$ means the energy, the $\pm$ signs represent conduction and valence band, respectively, and $\gamma$ is the interaction energy between the nearest neighboring carbons ($\approx 2.8$ eV). Figure 2.3 indicates the energy dispersion of graphene according to wave vector ($\mathbf{k}$). The upper conduction ($\pi^*$) and lower valance ($\pi$) bands intersect each other at the $K$ and $K'$ points. These crossing points are called Dirac points which are situated at the edge of Brillouin zone in the momentum space. A linear dispersion relation is observed at the Dirac point within about 1 eV Dirac energy. The location of the Fermi energy level in the intrinsic graphene corresponds exactly to the Dirac point. Therefore, graphene is considered a semi metal or zero bandgap semiconductor material. The energy dispersion can be expanded near the Dirac points and can be expressed as

$$E_{\pm} = \pm\hbar v_F \left|\mathbf{k}-\mathbf{k_0}\right| \tag{2.4}$$

where $\mathbf{k}_0$ is the wavenumber at a Dirac point, $v_F$ is the Fermi velocity ($\approx 0.87 \times 10^6$ m/s) of the $\pi$ -electron and $\hbar$ is the Planck constant.

The valence band of intrinsic graphene is absolutely filled with $\pi$-electrons in the ground state and the energy distribution function of the $\pi$-electron in equilibrium is determined using he Dirac-Fermi function as follows

$$F\left[E_{\pm}\right] = \frac{1}{e^{E_{\pm}/k_B T_0}+1} \tag{2.5}$$

where $k_B$ indicates the Boltzmann constant and $T_0$ means the temperature.

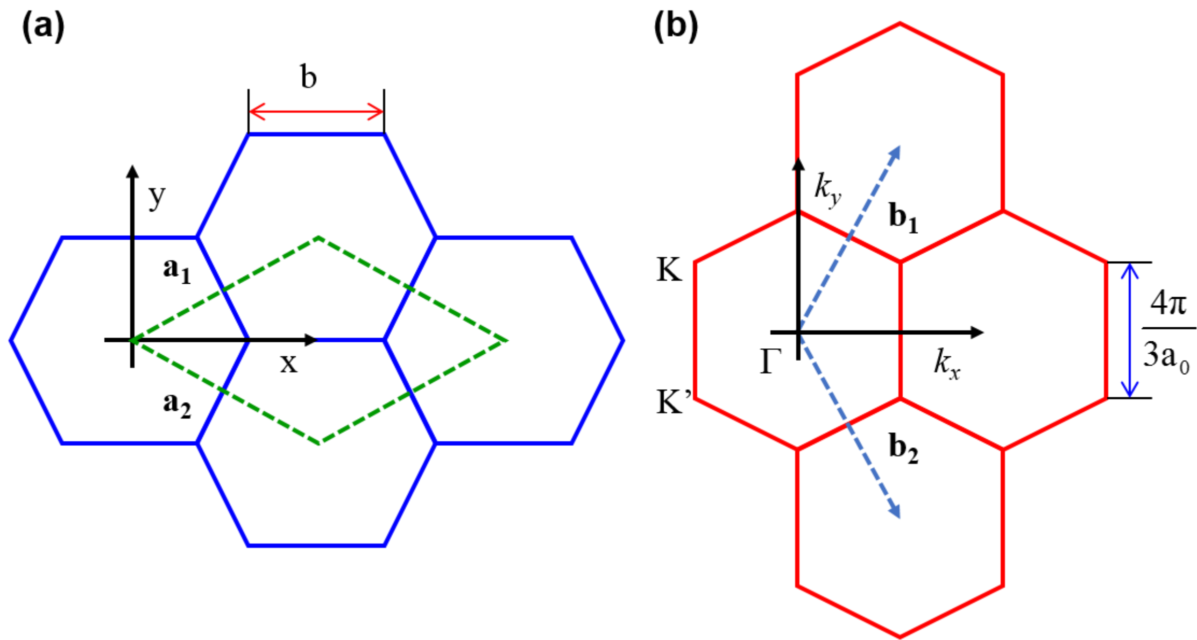


Figure 2.2: (a) Honeycomb lattice structure of graphene in real space. The green dotted line is primitive cell comprising two inequivalent atoms. The $\mathbf{a}_1$ and $\mathbf{a}_2$ are the primitive vectors in x- and y-coordinates. (b) In reciprocal space, graphene Brillouin zone with the reciprocal primitive vectors of $\mathbf{b}_1$ and $\mathbf{b}_2$ [34].

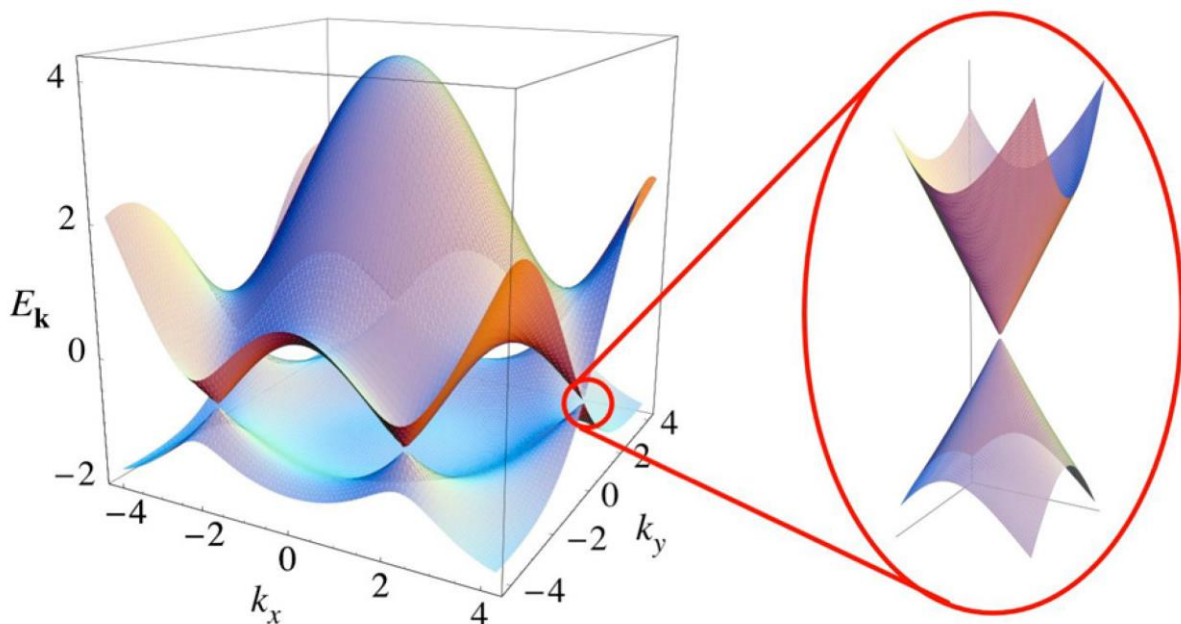


Figure 2.3: Graphene band structure calculated using nearest-neighbor tight binding model. The right enlarged image shows the linear dispersion relation around Dirac point with low energy level [35].

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### 2.2 Graphene Synthesis Methods

Since graphene was firstly discovered by Geim group, various methods have been studied to form large-scale and high-quality graphene. In this section, we have introduced the common techniques such as exfoliation method from highly oriented pyrolytic graphite (HOPG), chemical vapor deposition (CVD). The formation of EG on Silicon Carbide (SiC) is the main point of my PhD study and will be discussed in detail in the next section.

#### 2.2.1 Micromechanical Exfoliation of HOPG

In 2010, Geim and Novoselov won the Nobel Prize in Physics for discovering single carbon-layer using micromechanical cleavage [6]. The graphene was mechanically isolated from the HOPG using by Scotch tape [36]. These exfoliated graphene flakes transferred to substrate. Here, $SiO_2$ having a thickness of 300 nm is preferred because a mono layer graphene can be distinguished by optical microscope as shown in Figure 2.4 [37]. Using this technique, we can get the highest quality graphene with a mobility of over 200,000 $cm^2/Vs$, but the graphene flakes size is too small (micro-scale) to be commercialized. Therefore, exfoliated graphene is mainly used for research purpose.

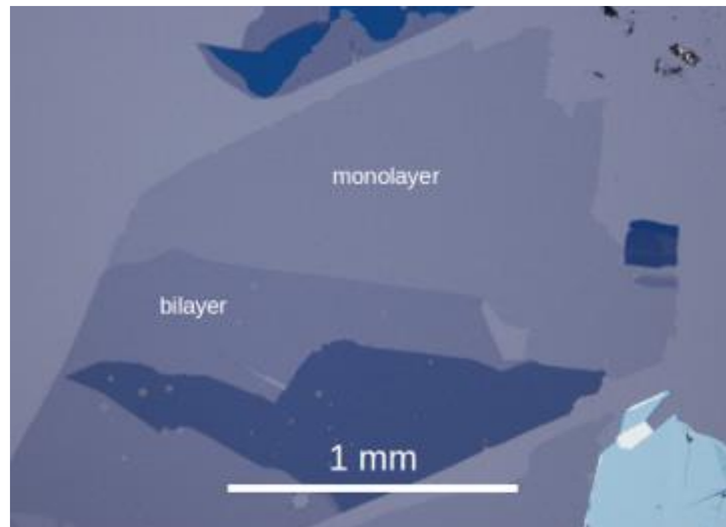


Figure 2.4: The optical microscope image of exfoliated carbon layer flake. The graphene shows different colors depending on its thickness [37].

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### 2.2.2 Metal-catalytic Chemical Vapor Deposition (CVD)

The method of graphene growth on metal film using CVD is the most widely used for mass synthesis of high quality graphene. Numerous methods have been carried out using CVD to form graphene on various types of metals such as Pt, Cu, Au, Rh, Ir, Ni, Co and Ru [38-43]. Since Pt, Au and Ir are expensive materials, Cu [43] and Ni [39] are mainly used.

The growth of large area uniform graphene was conducted on polycrystalline Cu foils by Ruoff group in 2009 [43]. They obtained a uniform monolayer graphene on the Cu foil surface, except for 5 % of the total area representing bilayer or trilayer graphene. The Cu with low carbon solubility can control the graphene layer thickness over wide area. This process shows the strongly self-limiting growth characteristics depending on graphene coverage. When the graphene is fully formed on the entire surface of the Cu, no further growth occurs. Figure 2.5 shows the CVD growth process on Cu foil surface [44, 45]. The Cu foil is firstly heated in Ar and $H_2$ atmosphere at about 1000 ˚C to increase the size of Cu grain, and remove the surface oxide and impurities of Cu foil. Gas precursor (hydrocarbon such as methane) is flowed over Cu substrate at 1000 ˚C to form graphene on Cu foil. The nuclei of carbon atoms formed on Cu are laterally grown and cover the entire surface of the Cu foil as shown in Figure 2.5.

By contrast, the Ni with high carbon solubility cannot limit the thickness of graphene itself. The carbon atoms absorbed at high temperature are released during cooling process because of the temperature dependent solubility, which can lead to the formation of multi-layers graphene on the Ni surface (Figure 2.6) [46]. At this time, the grain boundaries are used as transfer paths of carbon atoms. The thickness of graphene is highly dependent on the quantity of carbon atoms diffused into the Ni and the cooling conditions.

Although uniform graphene formation is accomplished by the CVD method as described above, there are still some disadvantages to overcome for use in device applications. The CVD graphene contains wrinkles formed by the thermal expansion coefficient mismatch between graphene and Cu during the cooling process. These wrinkles cause defect scattering and degrade the device performance [47]. Moreover, the transfer process of graphene grown on conductive metal to the insulating substrate is essential for use in electronic devices, which leads to serious degradation of graphene quality by mechanical damage, polymer contamination and unintended doping.

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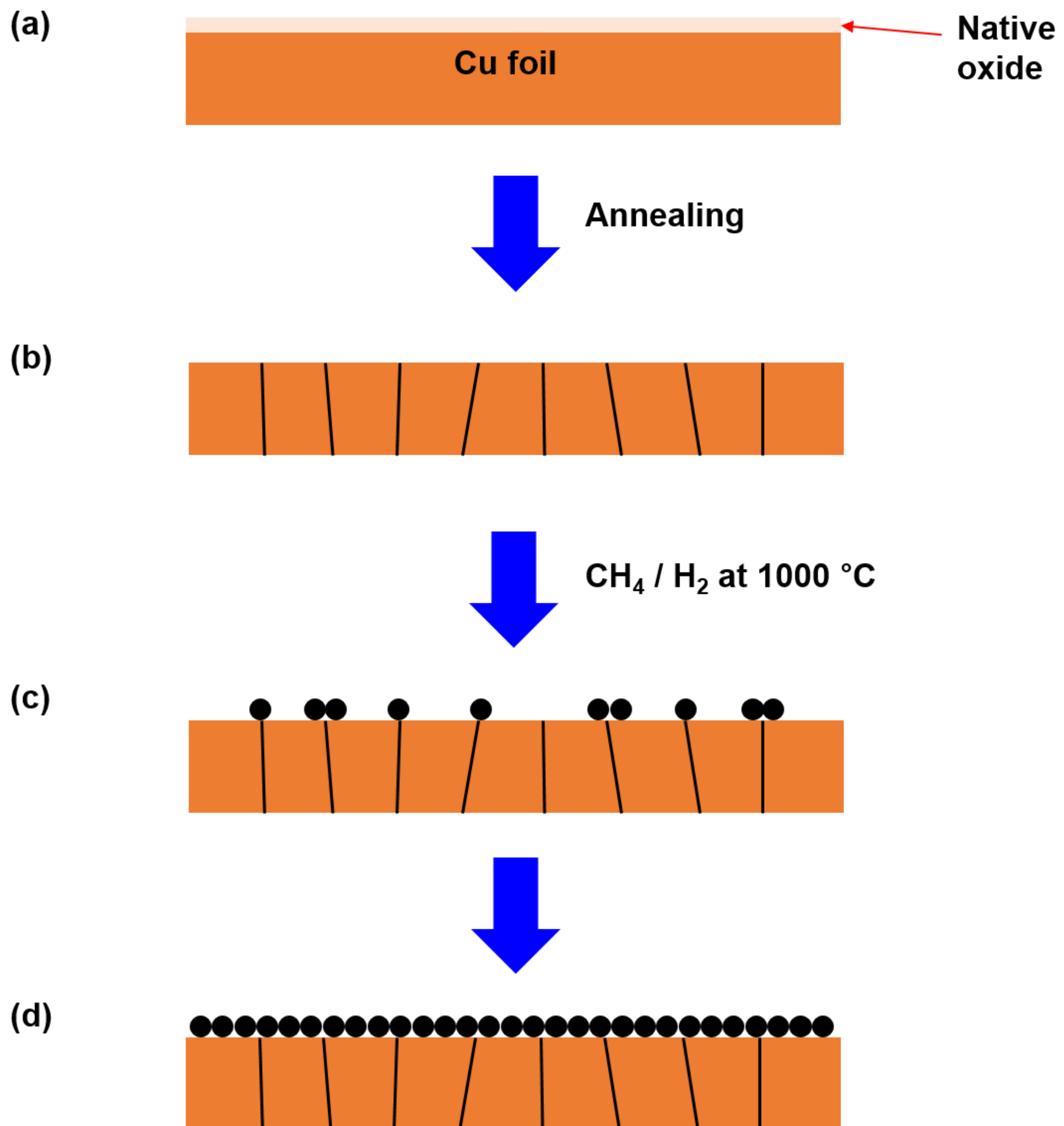


Figure 2.5: Mechanism of graphene formation on Cu foil using CVD. (a) Formation of native oxide on Cu foil. (b) Removing native oxide and developing Cu grains during heating process at high temperature in $H_2$ circumstance. (c) $CH_4/H_2$ flows on Cu foil at 1000 °C and it induces graphene islands nucleation. (d) Lateral growth of graphene based on nucleation with different lattice orientation and coalescence into a continuous graphene [44, 45].

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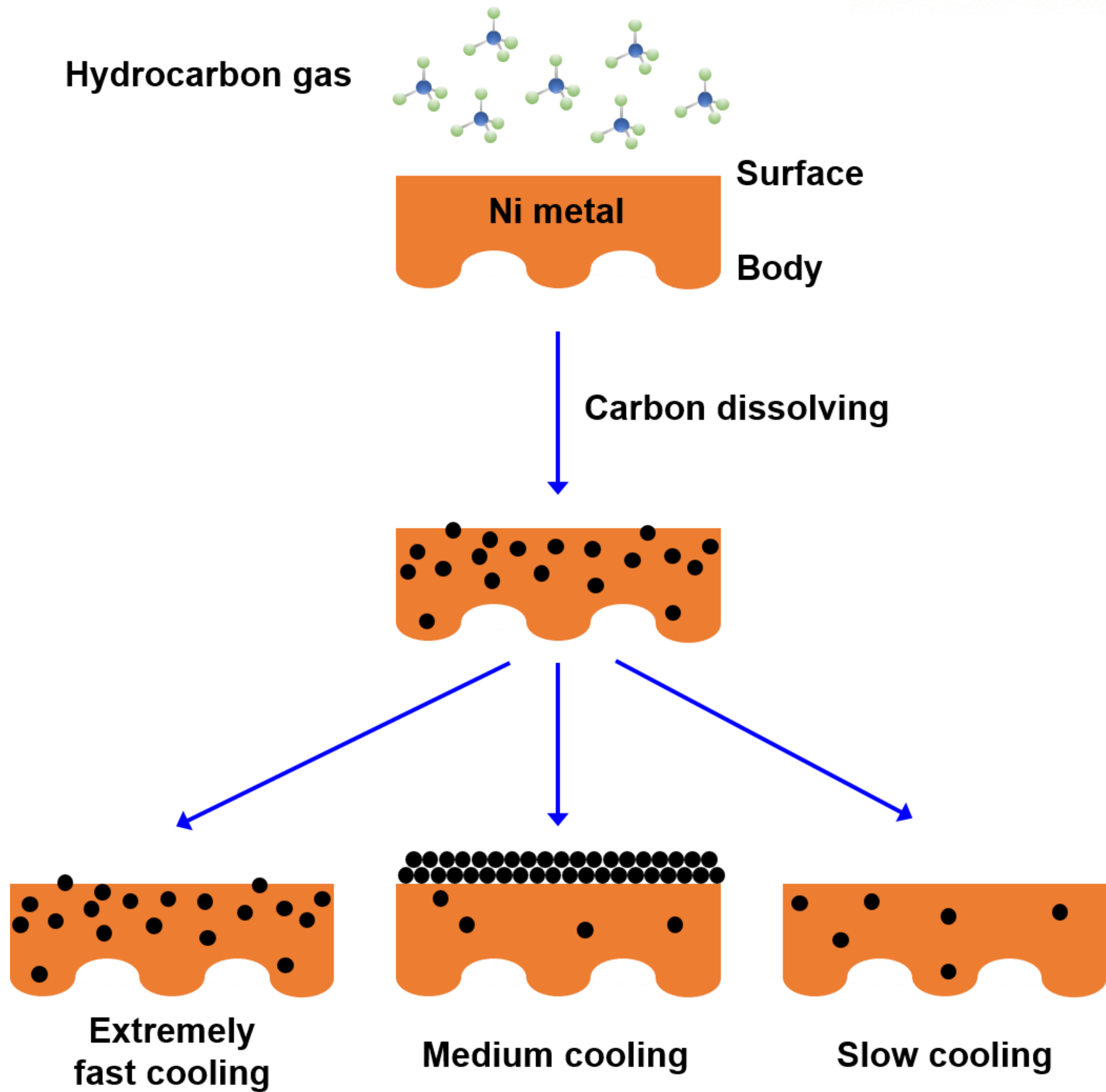


Figure 2.6: Schematic illustration of graphene growth mechanism on Ni foil using CVD. The quantity of carbon segregation from Ni depends on cooling rate [46].

## 2.3 Epitaxial Graphene (EG) on Silicon Carbide (SiC)

The EG on SiC is a promising technique to form high quality wafer scale graphene for use in electronic device application [5, 7-10]. When SiC is heated to high temperature (> 1500 °C) in ultra high vacuum (UHV) [5] or Ar [7] environment, Si atoms are sublimated from the SiC surface and the remaining C atoms are rearranged to form wafer scale EG as shown in Figure 2.7 [48]. This method has advantages that a graphene transfer and cleaning processes are not necessary because semi-insulating SiC is used as a substrate for grown EG. Moreover, SiC has outstanding electrical characteristic such as high breakdown field strength, high saturation electron drift velocity and high thermal conductivity. From this, EG on SiC is believed as a promising material for high speed, electronically graphene devices that can operate in high temperature, high frequency and high voltage environments.

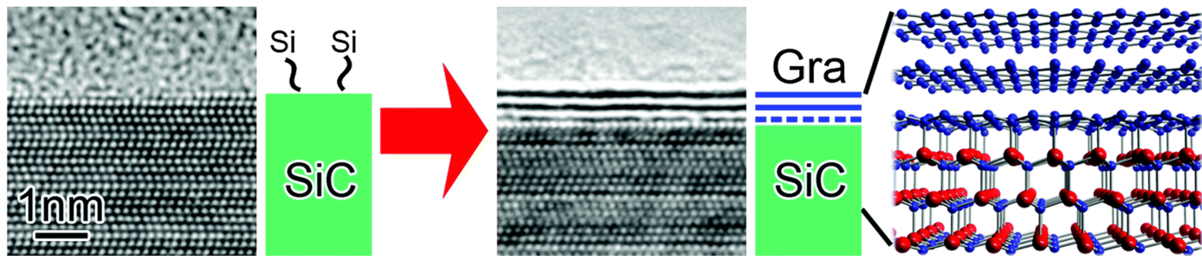


Figure 2.7: Mechanism of EG growth on SiC substrate by thermal decomposition. Si atoms sublimate and remaining carbon atoms form graphene at high temperature [48].

### 2.3.1 SiC Crystal Structure

The basic unit of SiC has tetrahedral structure with a bond length of 1.89 Å which Si (C) atom is connected to four C (Si) atoms in covalent bonds (Figure 2.8(a)) [49]. The planar hexagonal symmetry layer is consisted of periodically repeated individual tetrahedral units (Figure 2.8(b)) [49]. This Si-C bilayer is a basic building block for the SiC crystal structure. The bulk crystal of SiC is formed by stacking bilayers on top of each other with different stacking arrangement such as cubic (C), hexagonal (H) and rhombohedral (R) like 3C, 4H, 6H and 15R. The SiC has more than 200 polytypes [50]. For the growth of EG, the most stable 3C-, 4H- and 6H SiC polytypes are mainly used. Figure 2.9 shows the structure of these polytypes [49]. Letters of A, B and C indicate the stacking order of the Si-C bilayers. The 3C-SiC has cubic structure with three bilayers stacking sequence (ABC) per unit cell (Figure 2.9(a)). The 4H- and 6H-SiC shows the hexagonal structure, which is ideal template for graphene growth. These two polytype unit cells contain four (ABCB) and six (ABCACB) bilayers respectively (Figure 2.9(b) and (c)). Table 2.1 shows the material properties of 3C-, 4H- and 6H-SiC compared to Si and GaAs at room temperature [51]. Here, bandgap energies are affected by the stacking structure, which range varies from 2.2 for 3C-SiC to 3.3 for 4H-SiC.

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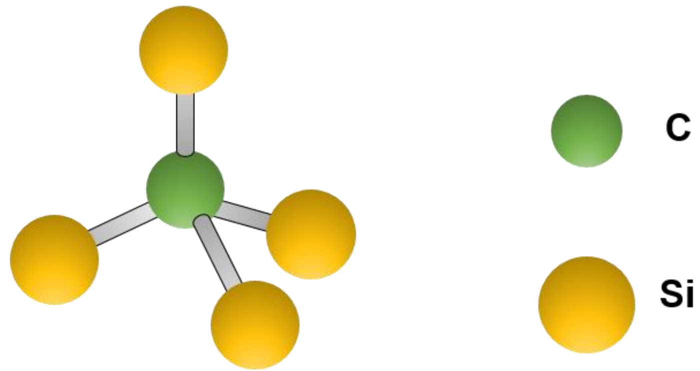
(a)




(b)

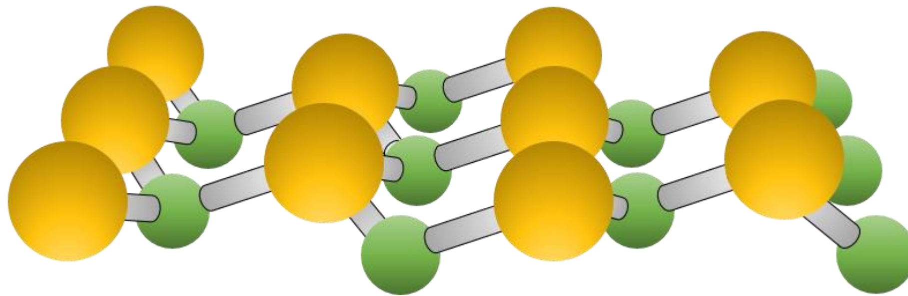


Figure 2.8: (a) Tetrahedral bonding of Si (yellow circle) to the nearest C atom (green circle) (b) hexagonal symmetry Si-C bilayer [49].

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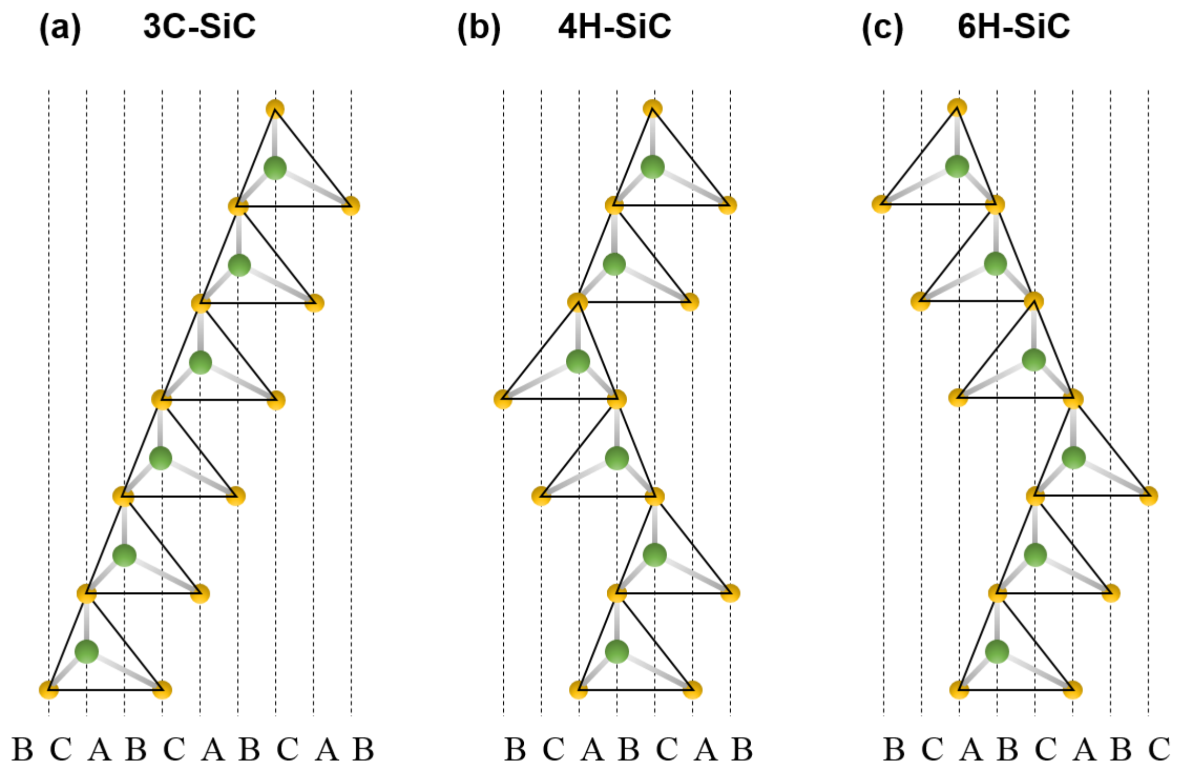


Figure 2.9: The stacking sequences of different SiC polytypes (a) cubic 3C-SiC (b) hexagonal 4H-SiC (c) hexagonal 6H-SiC [49].

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Table 2.1: Material properties of Si, GaAs, 4H-, 6H-, and 3C-SiC at 300 K [51].

| | Si | GaAs | 4H-SiC | 6H-SiC | 3C-SiC |
|---|---|---|---|---|---|
| Crystal Structure | Diamond | Zincblende | Hexagonal | Hexagonal | Zincblende |
| Lattice constant $a$, $c$ (Å) | 5.43 | 5.65 | $a = 3.08$<br>$c = 10.08$ | 3.08<br>15.12 | 4.36 |
| Thermal conductivity (W/cmK) | 1.5 | 0.5 | 5.0 | 5.0 | 5 |
| Energy gap $E_G$ (eV) | 1.11 | 1.43 | 3.26 | 3.02 | 2.2 |
| Hole mobility $\mu_p$ (cm$^2$/Vs) | 600 | 400 | 100 | 50 | - |
| Electron mobility $\mu_n$ (cm$^2$/Vs) | 1400 | 8500 | 900 | 450 | 1000 |
| Saturation drift velocity $v_s$ (cm/s) × $10^7$ | 1 | 2 | 2.7 | 2 | 2.7 |
| Maximum operating temperature $T$ (°C) | 300 | 460 | 1240 | 1240 | 1240 |
| Breakdown field $E_B$ (MV/cm) | 0.3 | 0.4 | 3.0 | 3.0 | - |
| Relative dielectric constant $\varepsilon_s$ | 11.8 | 12.8 | 9.7 | 9.7 | 9.7 |

### 2.3.2 Effects of SiC Polytypes on Growth of EG

The properties of grown EG are affected by SiC polytypes because the SiC surface reconstruction (step bunching) and surface decomposition energy at high temperature (> 1300 °C) are different by SiC polytypes [5]. These results lead in different graphene growth rates and morphologies. Yazdi *et al.* have demonstrated the difference in characteristics of EG grown at identical conditions on Si-face 4H-SiC (0001), 6H-SiC (0001) and 3C-SiC (111) substrate [52]. Figure 2.10(a), (b), and (c) show histograms of the step height probability for graphenized surface of 4H-, 6H- and 3C-SiC substrates after step bunch at 2000 °C. The height of ~ 300 steps for each polytype is measured by atomic force microscopy (AFM). Here, the Si-C bilayer step height is around 0.25 nm. For the 4H-SiC sample, the two bilayers height step occupies the most distribution, followed by the four bilayer height step. For the 6H-SiC substrate, two and three bilayer-height steps are dominant. The 3C-SiC substrate shows that the bilayer height step accounts for about 48 %. Figure 2.10 (d)-(f) show the types of decomposition energies of each substrate. There are two types of terraces in 4H-SiC: 4H1 and 4H2 [53]. The terrace decomposition rate of 4H1 is faster than 4H2 because decomposition energy for removing terrace is smaller. The 4H1 terrace step catches the 4H2 terrace step, and form the two and four bilayer-height step. There are three types of terraces in 6H-SiC: 6H1, 6H2 and 6H3 [53]. With a similar mechanism, the fastest 6H1 terrace catches up with 6H2 terrace, and then the 6H3 terrace combine with the merged two bilayer step. Thus, two and three bilayer height steps are formed. It is identical to the results in Figure 2.10(b). On the other hand, step bunching is not occurred in 3C-SiC because all terraces of 3C-SiC have the identical decomposition energy as shown in Figure 2.10 (c). For this reason, the observed step height is mostly 0.5 nm.

The formation of the epitaxial graphene does not occur evenly over the entire surface of the Si-face SiC substrate. Si atoms firstly desorbed from step edges because Si and C atoms are weakly bonded in the edges rather than on the terraces [54]. Figure 2.11(a) explains the graphene formation processes in 4H-SiC. At the step edges, Si atoms sublimate and remaining C atoms are emitted to terrace surface. These C atoms coalesce into graphene nuclei, which collects further released C atoms and extends graphene laterally [55]. After the 4H2 terraces are caught by the 4H1 terraces, the newly formed two bilayer height step emits more C atoms, resulting in graphene formation along the edges. (step 2). The amount of carbon atoms emitted from four bilayer height step increases, and the bilayer graphene is formed by extra carbon atoms. If 3C-SiC substrate is assumed to be defect free, all terraces of 3C-SiC with the same decomposition velocity provide same amount of carbon atoms which form a uniform thickness of graphene on SiC surface (Figure 2.11(b)). However, defects existing in 3C-SiC lead to step bunching by changing the decomposition rate (Figure 2.11(c)) [56]. The step decomposition rate in defects is relatively faster.

Figure 2.12 shows low-energy electron microscopy (LEEM) images of grown EG on each SiC substrate. The uniform monolayer graphene is formed about ~60% for 4H-SiC, 92 % for 6H-SiC, and

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98% for 3C-SiC. The white, dark gray, and black area represent monolayer, bilayer, and trilayer graphene, respectively. These results are consistent with the graphene growth mechanism according to the substrate as described above.

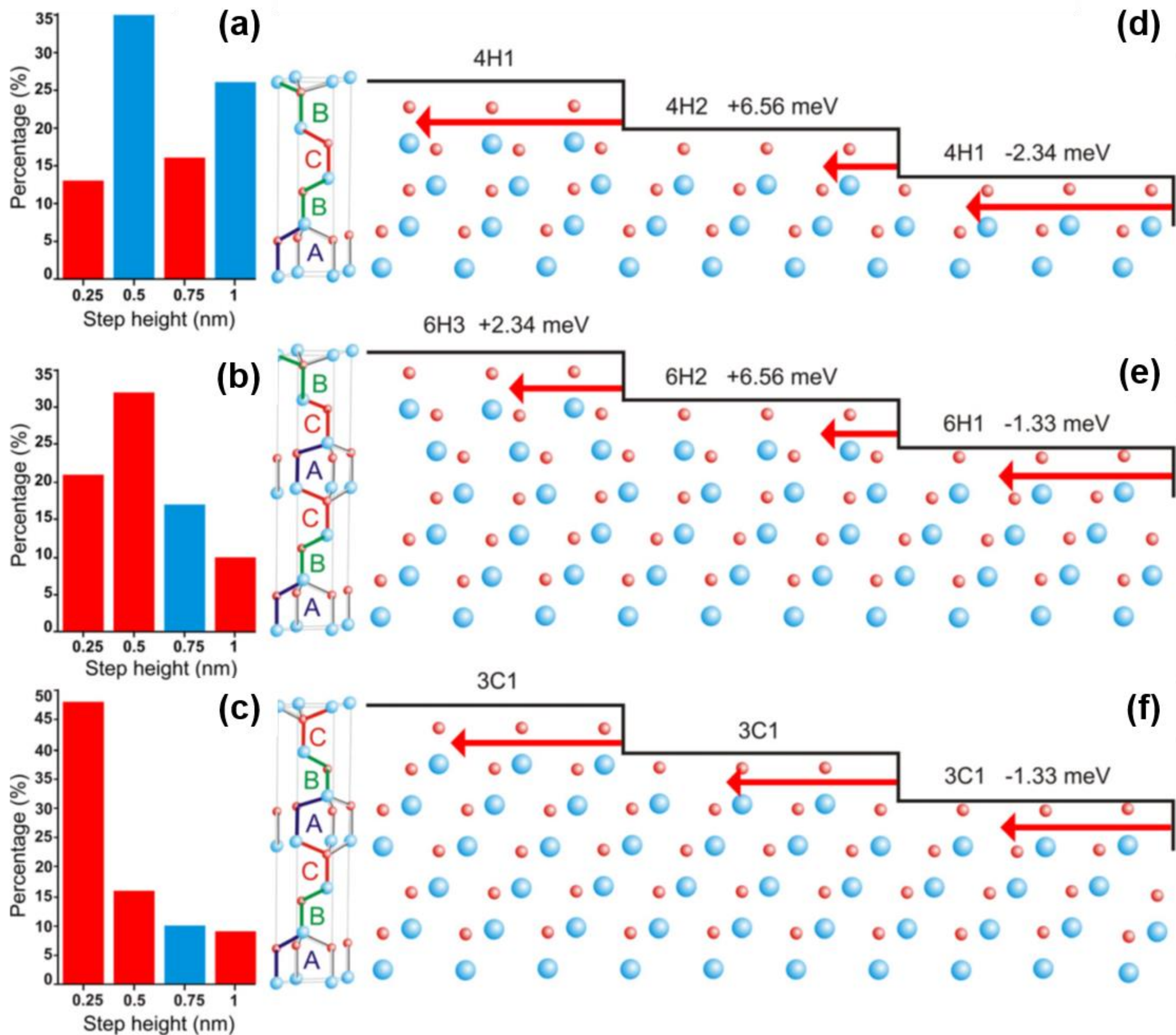


Figure 2.10: Distribution of step heights for (a) 4H-, (b) 6H-, and (c) 3C-SiC. Types of terraces based on decomposition energy in (d) 4H-, (e) 6H-, and (f) 3C-SiC. The blue and red circles indicate the Si and C atoms, respectively. The red arrow lines represent the decomposition velocities [52].

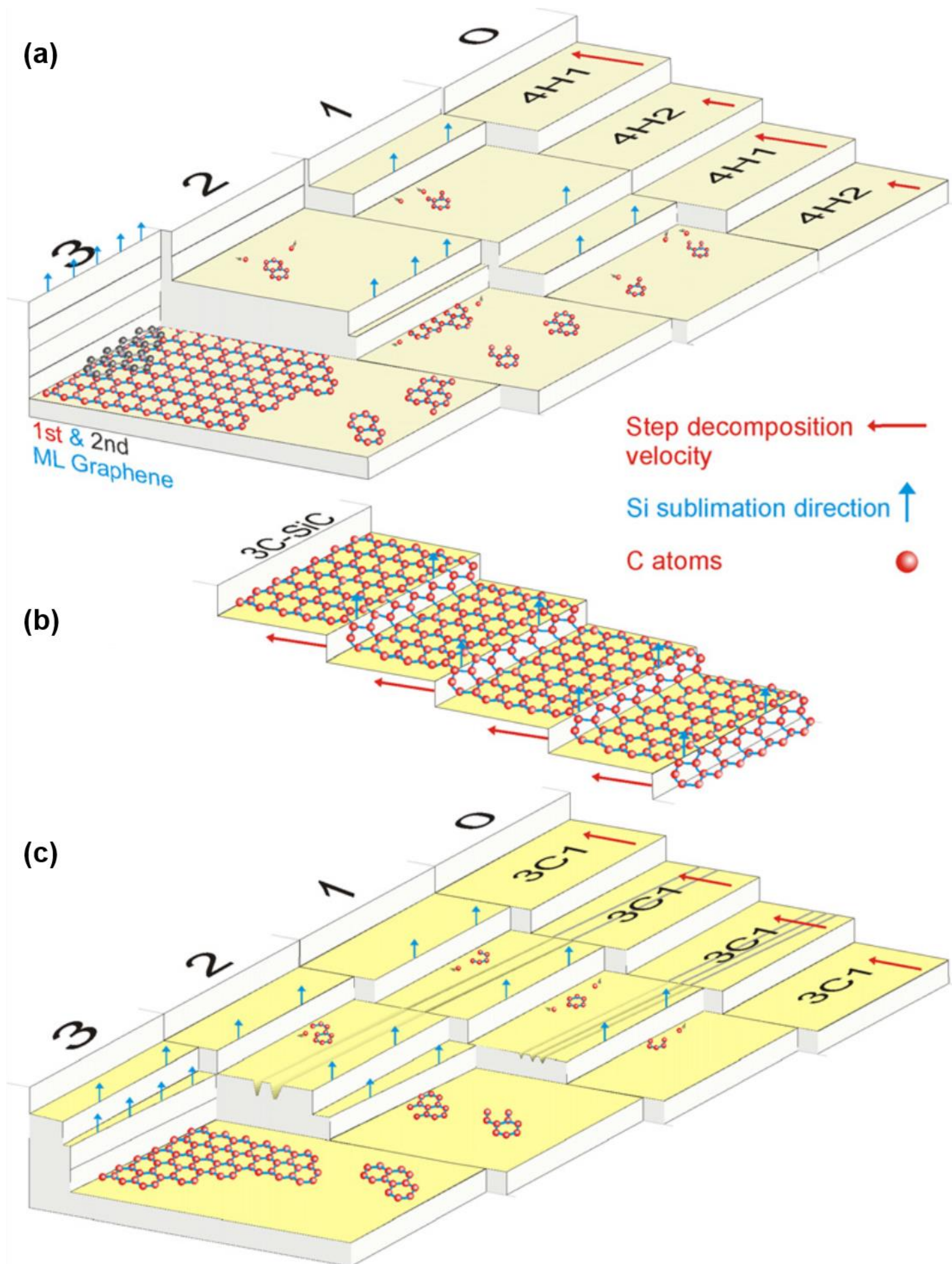


Figure 2.11: EG growth mechanism by thermal decomposition on Si-face (a) 4H-SiC (b) ideal 3C-SiC (c) defects contained 3C-SiC [52].

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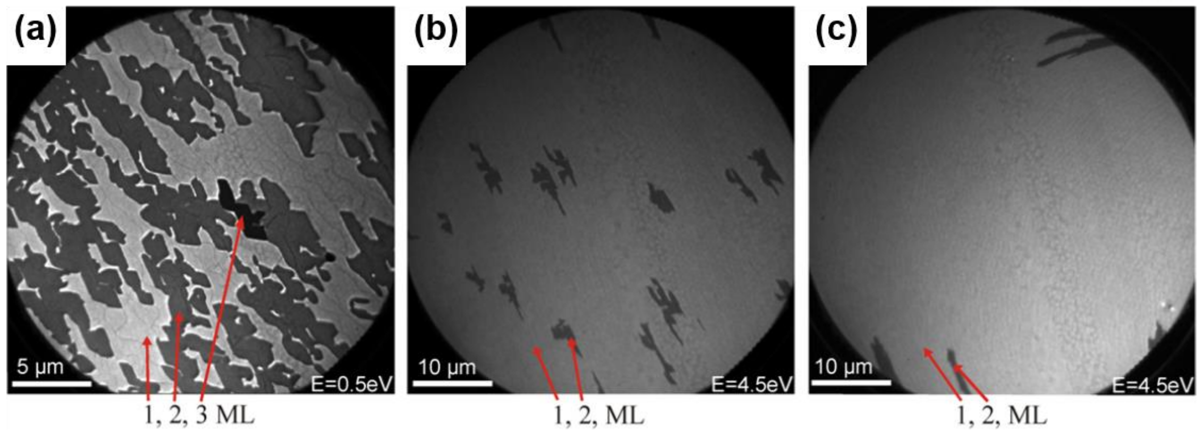


Figure 2.12: LEEM images of grown EG on (a) 4H-, (b) 6H-, and (c) 3C-SiC at same condition by thermal decomposition [52].

### 2.3.3 EG Grown on Si- and C-face SiC

Figure 2.13 shows the two types of surface orientations of SiC perpendicular to the c-axis, Si- face (0001) and C-face (000-1). The growth process and properties of EG are highly influenced by the surface type [57]. On SiC (0001), the graphene growth rate is very slow and monolayer or bilayer graphene is grown on substrate. The graphene formation on the Si-face is achieved by nucleation formation at the step-edge portion and lateral growth on the terrace [58]. The graphene growth mechanism on the C-face is completely different from on the Si-face. Graphene nuclei are formed not only at the step edge but also on the terrace. On SiC (000-1), growth rate of graphene is relatively faster than that of Si-face and multilayer graphene is formed [59]. Therefore, the thickness of the graphene formed on the C-face is much thicker than the Si-face at same condition. Unlike SiC (0001), a buffer layer is not grown on SiC (000-1). In this section, we will discuss the growth mechanism of graphene in detail and the characteristics of grown graphene depending on the surface type of SiC [54, 60].

Figure 2.14 shows the EG formation process on SiC (0001) [54]. When SiC substrate is annealed at a high temperature, the Si atoms in the step location are selectively sublimated first due to the relatively weaker bonding in terrace. The remaining C atoms nucleate and form a graphene on the step edge and extends to the terrace area. The graphene formed on each terrace coalesces and whole surface of SiC is covered with continuous graphene. Prior to the growth of graphene, the first carbon layer of $(6\sqrt{3}\times 6\sqrt{3})$ R30° structure is grown on SiC (0001) [60]. This layer is called buffer layer. It is oriented at 30° to the SiC because of the difference in lattice constant between the graphene (2.46Å) and SiC (3.07Å). Despite being structurally similar to graphene, the electrical properties are very different because the carbon atoms of buffer layer are partially covalently bonded to dangling Si atoms on the Si-face SiC. This covalent bonding affects the $\pi$ -orbital and modifies the linear band structure around the $K$ points. Upon annealing for longer time, the graphene layer is formed on the buffer layer. The

graphene layers grown on Si-face SiC are stacked in AB Bernal, which are oriented with a 60° degree rotation relative to the bottom graphene layer [61]. The EG grown on Si-face SiC is doped to n-type because dangling bonds of Si induces the electron doping.

Figure 2.15 shows the growth mechanism on SiC (000-1) substrate. Unlike on SiC (0001), the formation of graphene begins in all directions not only on step edges but also on terraces and multilayer graphene is formed. This graphene has multiple domains and shows less homogenous than EG on SiC (0001) as shown in Figure 2.16. The stacked multilayer graphene on SiC (000-1) are rotationally random along the stacking direction and adjacent graphene layers are electronically decoupled from each other [62]. Because of this stacking structure, each graphene layer behaves like free-standing which shows outstanding electrical properties. The carrier mobility is observed up to $10^5$ $cm^2/Vs$. There is no buffer layer in graphene on SiC (000-1). The carrier type of graphene differs depending on the stacking depth position. The graphene near the SiC shows n-type by the dangling bond, and the graphene exposed to the air shows p-type because of the charge transfer from water and oxygen molecules [63].

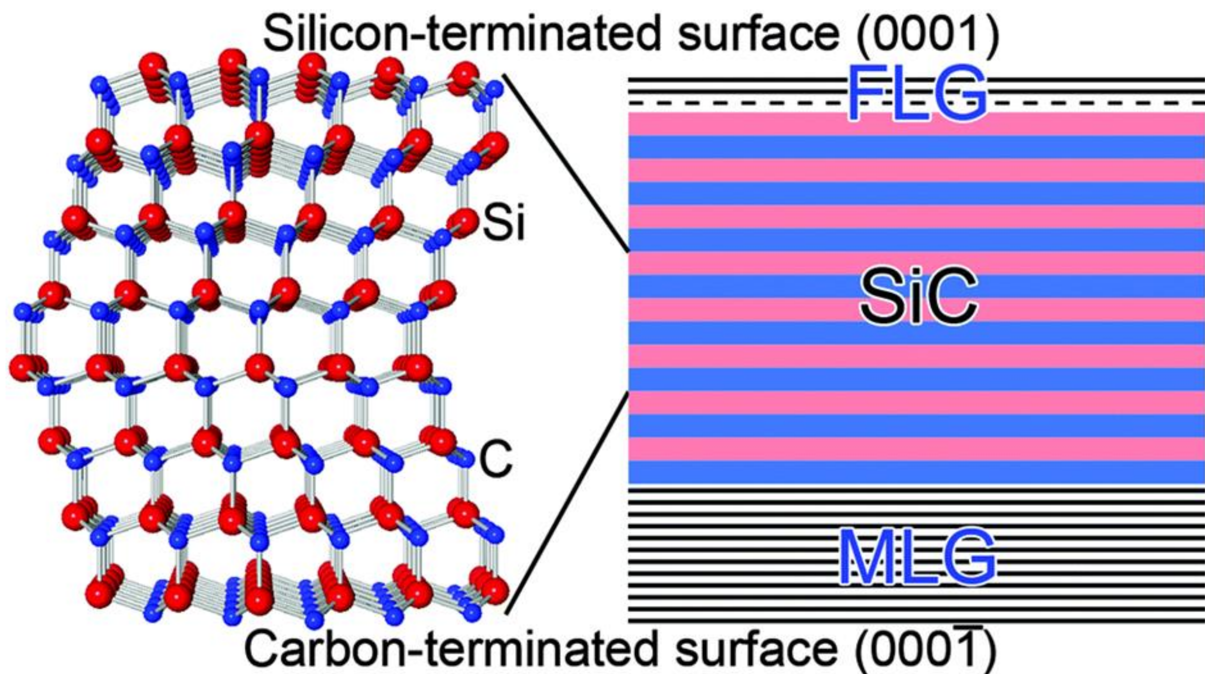


Figure 2.13: Formation properties of EG on both surfaces of SiC substrate (Si-face and C-face) [48].

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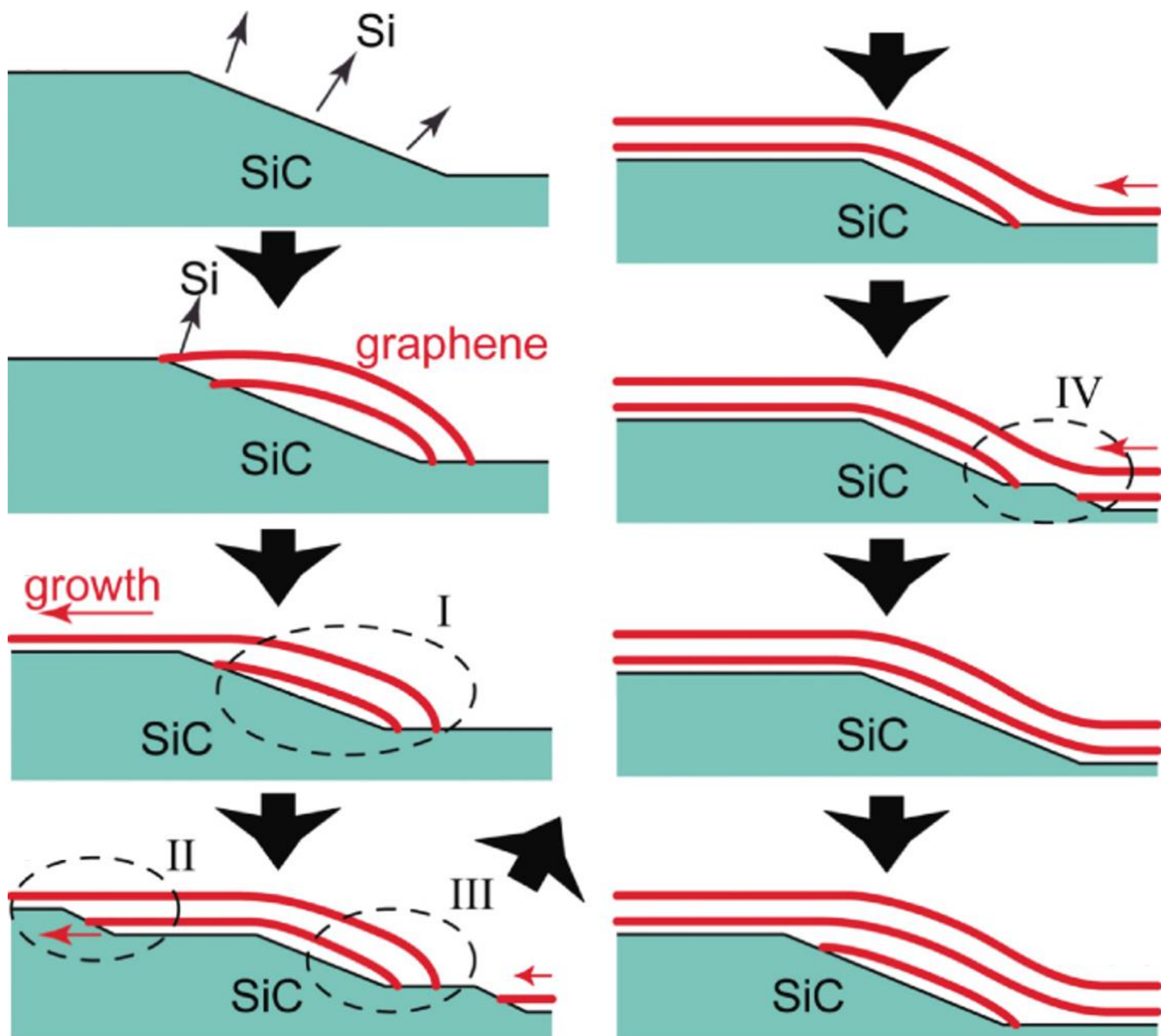


Figure 2.14: The EG growth mechanism on SiC (0001). The red lines represent the EG layers. The EG growth starts from SiC step edge [54].

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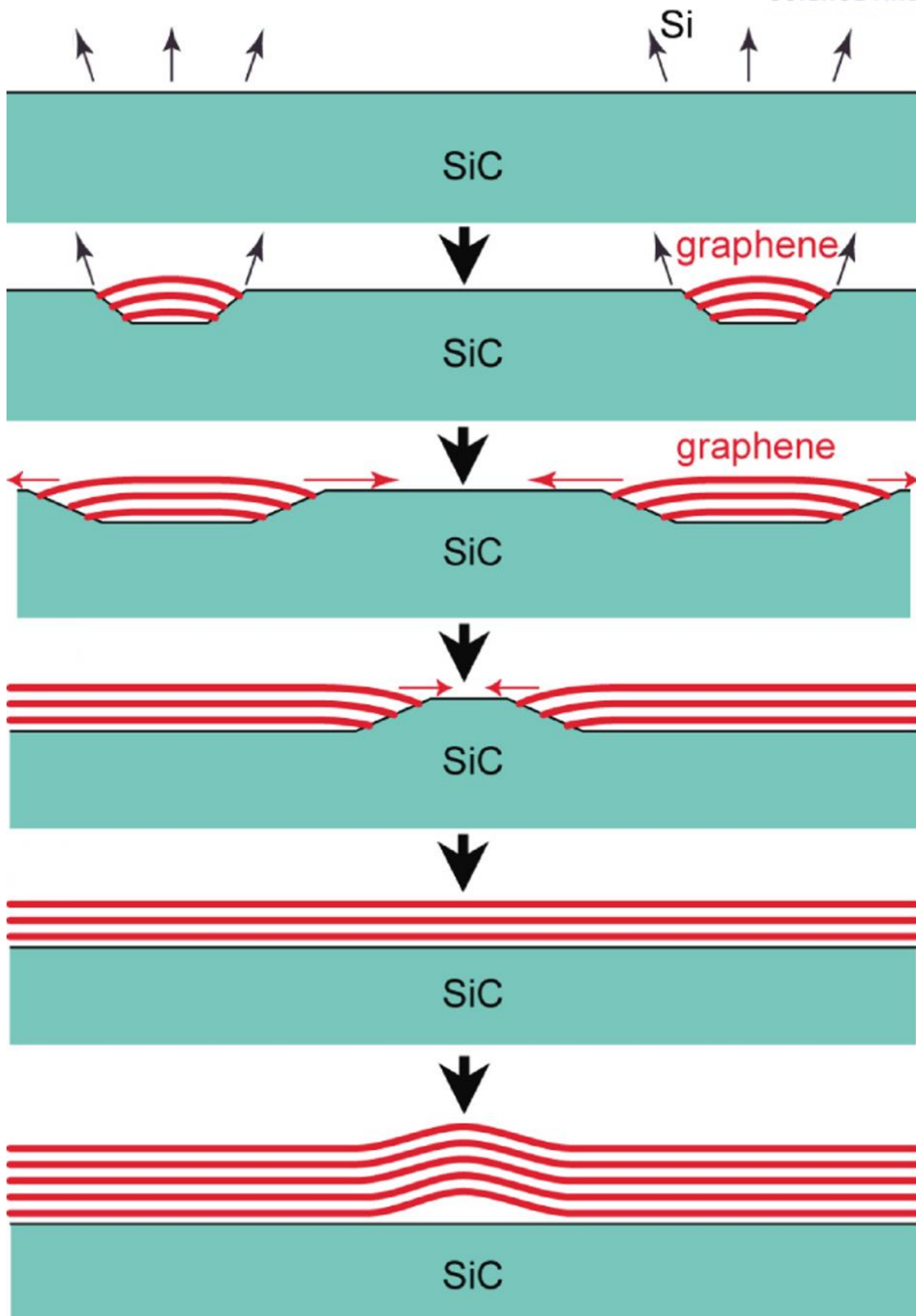


Figure 2.15: The EG growth mechanism on SiC (000-1). Growth of EG (red lines) starts at the terrace as well as at the step edges [54].

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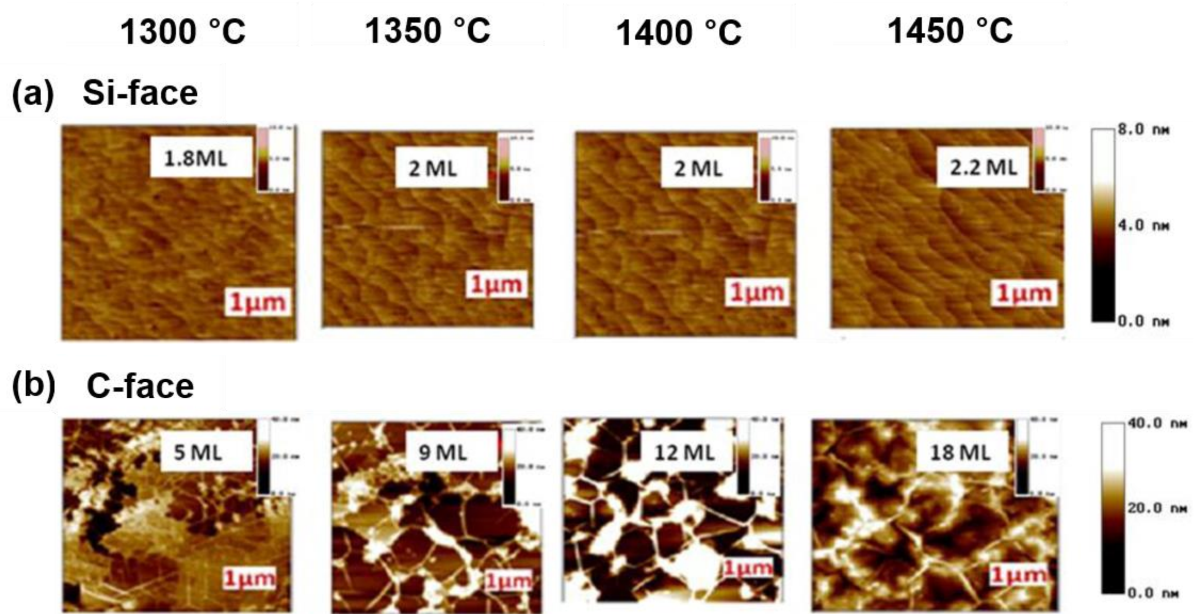


Figure 2.16: AFM images of EG grown on (a) SiC (0001) and (b) SiC (000-1) at different temperatures [64].

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### 2.3.4 Confinement Controlled Sublimation (CCS)

The quality of graphene grown on the SiC surface in UHV is bad because of the high sublimation rates of Si atoms at relatively low temperature [65]. The sublimation of Si at relatively low temperature creates defects in graphene and form many domains with different orientations. Above all, it is hard to form a uniform thickness of graphene over the SiC substrate at extremely fast sublimation rate. Various studies for reducing sublimation rate of Si have been attempted to form high quality graphene on SiC substrate. For example, SiC sample is annealed in a vapor phase disilane environment [66] or in Ar atmosphere [7]. These methods can effectively reduce the sublimation rate of Si atoms by increase working pressure. Alternatively, the Georgia Tech group suggested the CCS method as shown in Figure 2.17 [67]. They enclose a SiC wafer in a graphite enclosure with a leaking hole during high temperature annealing. This decreases the escape rate of Si atoms and retain the high vapor pressure of Si. The Si vapor pressure increases to reach an equilibrium and the growth rate of graphene is reduced. They formed high quality uniform EG using this method compared with UHV. Figure 2.17(c), (d), and (e) indicate AFM images of graphene on SiC grown by CCS method compared with UHV. The graphene formed by the CCS method were grown uniformly along the SiC steps. On the other hand, grown graphene in UHV is very defective and nonuniform. The Sabanci University group also obtained high quality graphene on Si- and C-face SiC substrate using CCS method [68]. They covered the SiC surface with a trenched SiC wafer during UHV annealing as shown in Figure 2.18(a). The sublimated Si atoms are confined in the cavity. The confined Si maintains a high vapor pressure on the sample surface which slow down the growth rate of EG. Figure 2.18(c), (d) and (e) show the AFM images of grown EG on SiC *with* and *without* capping SiC.

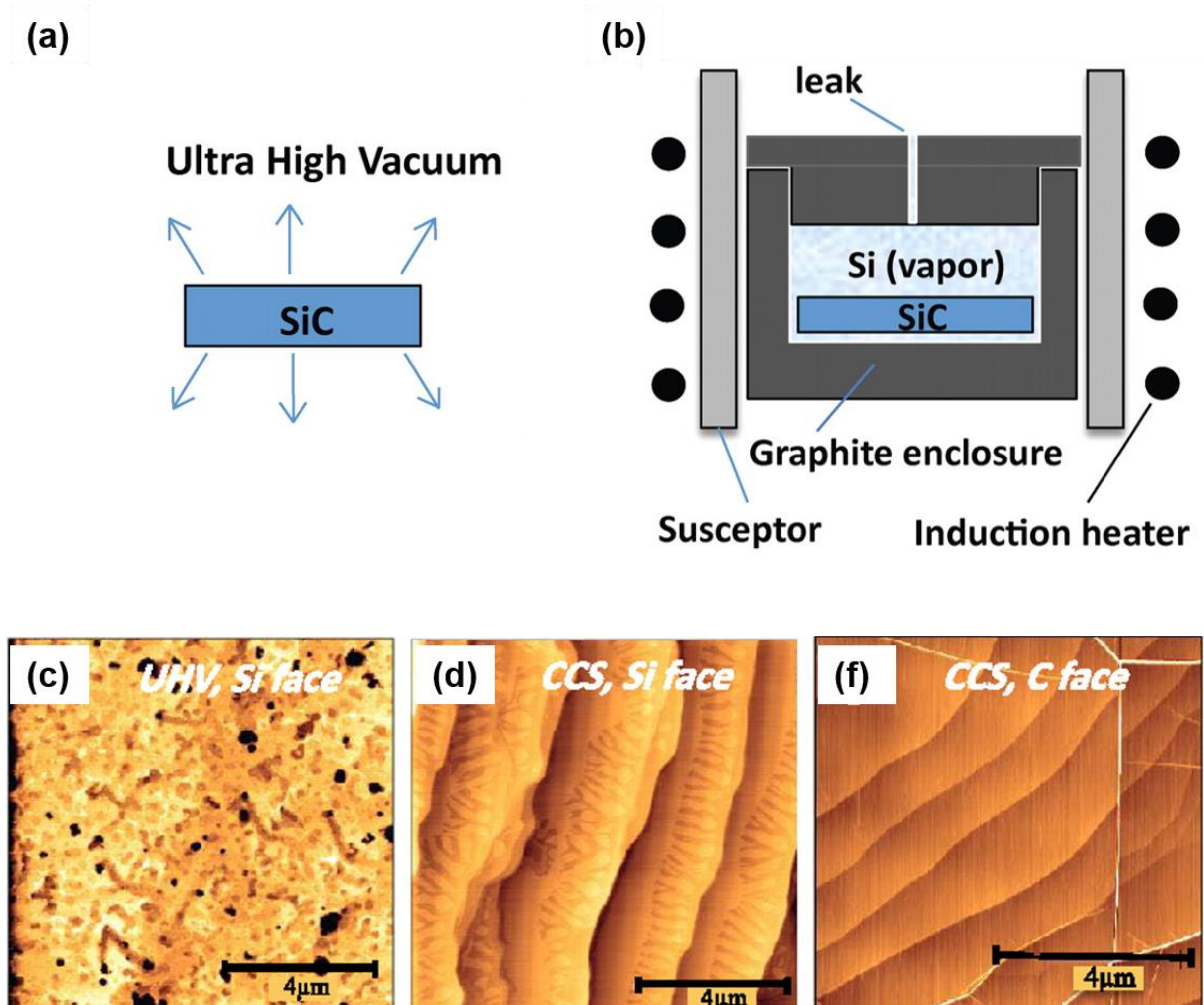


Figure 2.17: Thermal decomposition of SiC in (a) UHV (b) CCS method. AFM images of EG grown on (c) SiC (0001) in UHV, (d) SiC (0001), and (e) SiC (000-1) using CCS method [67].

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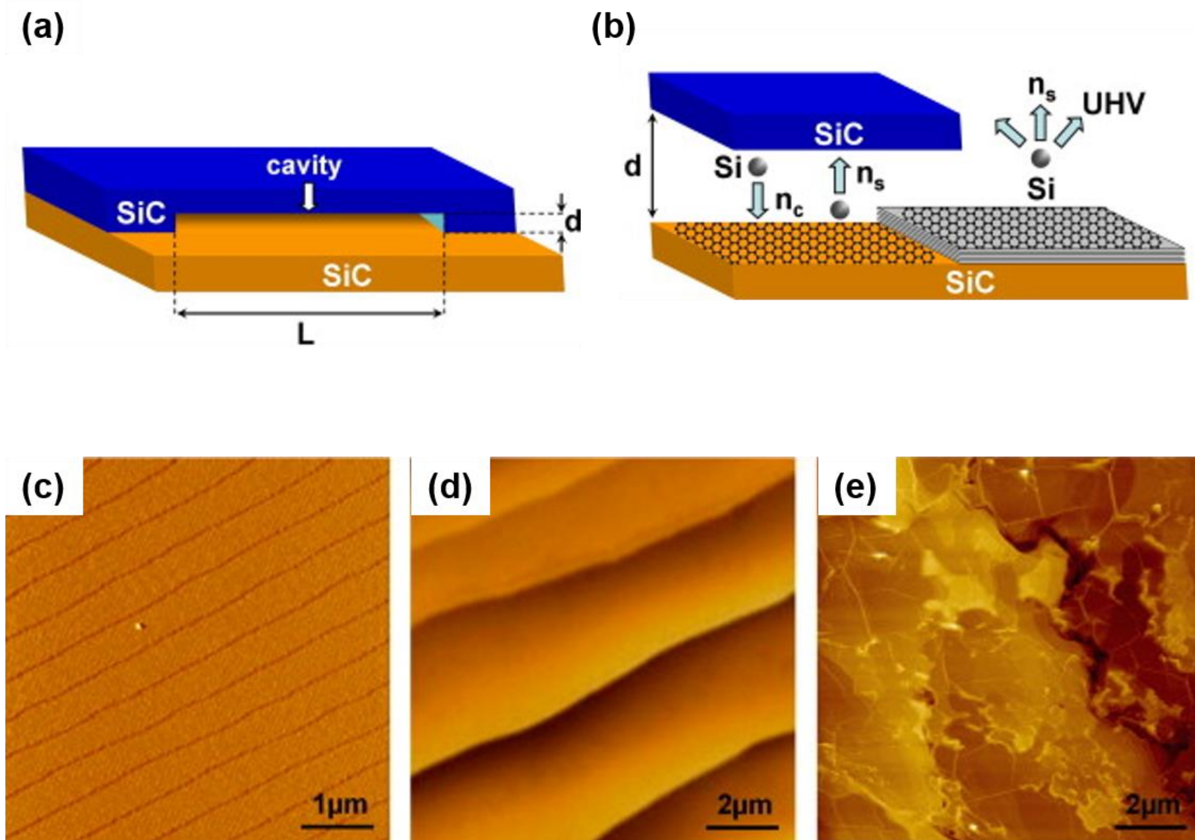


Figure 2.18: (a) The CCS method using SiC trench was proposed Kaya's group (b) The Si atoms sublimation rate is much slower than UHV atmosphere during annealing process. AFM images of (c) as received SiC (d) grown EG on SiC using CCS method. The widen width of SiC during annealing process is demonstrated. (e) AFM image of grown EG on SiC in UHV. The surface is not uniform and is defective [68].

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### 2.4 Quantum Hall Effect (QHE)

The QHE and its relation to fundamental physical constants have received much attention since its discovery in 1980 [69], and won the Nobel prize in 1985. The QHE is observed by measuring the Hall resistance ( $R_H$ ) on two-dimensional charge carrier system at low temperature in strong magnetic fields perpendicular to the plane of two-dimensional system. The $R_H$ exhibits and accurate constant values without depending on the change of the magnetic field or carrier density. These plateaus values are exactly equal to

$$|R_H| = \frac{h}{(\nu e^2)} \tag{2.6}$$

When the QHE phenomenon was discovered in 1980, $\nu$ takes integer numbers. However, additional fraction numbers ( $f$ ) have been observed as pure two-dimensional system is fabricated and QHE was measured at lower temperature [70]. This phenomenon is called Fractional Quantum Hall Effect (FQHE) and received the Novel prize in 1998. At low magnetic field, the $R_H$ increases linearly with magnetic field as following equation.

$$|R_H| = |R_{xy}| = \left|\frac{V_y}{I_x}\right| = \left|\frac{B_z}{(-en_s)}\right| \tag{2.7}$$

#### 2.4.1 Landau Level

Landau quantization is a fundamental component for understanding QHE [71]. Landau quantization is the kinetic-energy quantization of charged particles with cyclotron orbits in magnetic fields. This discrete energy levels are called Landau levels and each energy level is degenerate [72]. The Hamiltonian of a nonrelativistic electron in uniform magnetic can be written [73]

$$H = \frac{1}{2m}\left(\vec{p} + \frac{e}{c}\vec{A}\right)^2 \tag{2.8}$$

where $H$ is Hamiltonian operator, $\vec{p}$ is momentum operator, $\vec{A}$ is magnetic vector potential, $m$ is effective mass of electron, $e$ is charge of electron and $c$ is speed of light.

For uniform external magnetic field along the z-axis, the vector potential is following by proper gauge transformation as follows

$$\vec{A} = -Hy\hat{i} \tag{2.9}$$

The Hamiltonian of equation (2.8) is expressed as

$$\vec{H} = \nabla \times \vec{A} = \begin{vmatrix} \hat{i} & j & k \\ \partial x & \partial y & \partial z \\ -Hy & 0 & 0 \end{vmatrix} \tag{2.10}$$

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$$H = \frac{1}{2m}\left\{\left[p_x - \left(\frac{eH}{c}\right)y\right]^2 + p_y^2 + p_z^2\right\} \tag{2.11}$$

The Schrödinger equation can be solved by assuming a wave function as follow

$$\psi(x,y,z) = e^{i(k_x x + k_z z)} f(x) \tag{2.12}$$

Substitute equation (2.11) and (2.12) into the Schrödinger equation $H\psi = \varepsilon\psi$ , it becomes

$$\frac{1}{2m}\left\{\left[p_x - \left(\frac{eH}{c}\right)y\right]^2 + p_y^2 + p_z^2\right\} e^{ik_x x} e^{ik_z z} f(y) = \varepsilon e^{ik_x x} e^{ik_z z} f(y) \tag{2.13}$$

$$\frac{1}{2m}\left\{p_x^2 - \left(\frac{eH}{c}\right)2yp_x + \left(\frac{eH}{c}\right)^2 y^2 + p_y^2 + p_z^2\right\} e^{ik_x x} e^{ik_z z} f(y) = \varepsilon e^{ik_x x} e^{ik_z z} f(y) \tag{2.14}$$

When this wave function acts as a Hamiltonian, the operator $p_x$ and $p_y$ are replaced by its eigenvalue $\hbar k_x$ and $\hbar k_z$ , and equation (2.14) is expressed as

$$\left\{\frac{1}{2m}(\hbar^2 k_x^2) - \left(\frac{eH}{mc}\right)y(\hbar k_x) + \frac{1}{2}m\left(\frac{eH}{mc}\right)^2 y^2 + \frac{1}{2m}{p_y}^2 + \frac{1}{2m}(\hbar^2 k_z^2)\right\} e^{ik_x x} e^{ik_z z} f(y) = \varepsilon e^{ik_x x} e^{ik_z z} f(y)$$

$$\tag{2.15}$$

The equation (2.15) can be rewritten as following expression

$$\left[\frac{1}{2m}p_y^2 + \frac{1}{2}m\omega_o^2(y - y_o)^2\right] f(x) = \varepsilon' f(y)$$

$$\omega_o = \frac{eH}{mc}, \quad y_o = \left(\frac{\hbar c}{eH}\right)k_x, \quad \varepsilon' = \varepsilon - \frac{\hbar^2 k_z^2}{2m} \tag{2.16}$$

where $\omega_o$ is a cyclotron frequency.

From these operators' point of view, this Hamiltonian take the same form as a harmonic oscillator. The energy levels for electrons in magnetic field can by written as

$$\varepsilon' = \hbar\omega_o\left(n + \frac{1}{2}\right) \quad (n = 0,\ 1,\ 2,\ \cdots) \tag{2.17}$$

$$\varepsilon(p_z, n) = \frac{\hbar^2 k_z^2}{2m} + \hbar\omega_o\left(n + \frac{1}{2}\right) \tag{2.18}$$

These energy levels called Landau levels and these are degeneracy in each Landau levels. The wavefunction depends on both $n$ and $k_x$ but the Landau levels are independent of $k_x$. The number of allowed values of $k_x$ is equal to degeneracy, such that $y_o$ lies within the system. In order to calculate degeneracy, we assume that the system is a large cube with sides of length L and impose periodic boundary conditions.

$$e^{ik_x(x+L)} = e^{ik_x x}, \quad e^{ik_x L} = 1 \tag{2.19}$$

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From the equation (2.19), the $k_x$ can be calculated as following

$$k_x = \frac{2\pi}{L} n_x, \quad n_x = 0,\ \pm 1,\ \pm 2,\ \cdots \tag{2.20}$$

The $y_o$ should be lie between 0 and $L$

$$0 < \left(\frac{\hbar c}{eH}\right) k_x \leq L \tag{2.21}$$

This equation gives the following range of $n_x$

$$0 < n_x \leq \left(\frac{eH}{hc}\right) L^2 \tag{2.22}$$

From this, we can get the degeneracy of a Landau level

$$g = \left(\frac{eH}{hc}\right) L^2 \tag{2.23}$$

When an external perpendicular magnetic field is applied to a two-dimensional system, the energy spectrum associated with the cyclotron motion of electrons in the xy plane is split into landau levels which is a discrete energy level of equal spacing. The energy level spacing is $\frac{e\hbar}{mc} H$ . The degeneracy and energy separation increase with the applied magnetic field. Figure 2.19 indicates the schematic illustration of energy spectra of a charged particle with and without magnetic field.

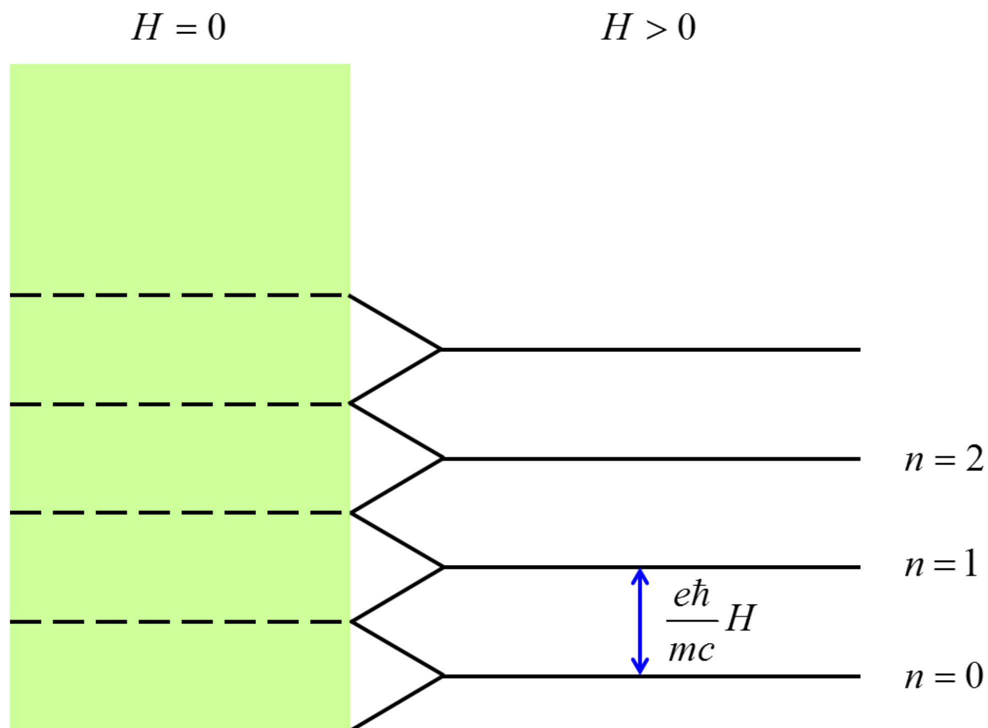


Figure 2.19: Schematic illustration of energy spectra with or without magnetic fields of charged particles.

### 2.4.2 Classical Hall Effect

The Hall effect was discovered in 1879 by Edwin Herbert Hall [74]. When magnetic field is applied perpendicularly to current flowing conductor, a potential difference is generated in the conductor, which is called Hall effect [72]. Figure 2.20 shows the Hall effect.

Because current density $(\vec{j})$ and electric field $(\vec{E})$ are not generally parallel, we can express $\vec{j}$ and $\vec{E}$ using the conductivity tensor $(\overleftrightarrow{\sigma})$ as follow

$$\vec{j} = \overleftrightarrow{\sigma} \cdot \vec{E} \tag{2.24}$$

In matrix form,

$$\begin{bmatrix} j_x \\ j_y \end{bmatrix} = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} \\ \sigma_{yx} & \sigma_{yy} \end{bmatrix} \begin{bmatrix} E_x \\ E_y \end{bmatrix} \tag{2.25}$$

In the case of system with rotational invariance, the $\vec{j_1}$ and $\vec{j_2}$ in two orthogonal electric fields $\vec{E_1}$ and $\vec{E_2}$ are

$$\vec{j_1} = \overleftrightarrow{\sigma} \cdot \vec{E_1} = \begin{bmatrix} \sigma_{xx} E \\ \sigma_{yx} E \end{bmatrix}, \quad \vec{E_1} = \begin{bmatrix} E \\ 0 \end{bmatrix}$$

$$\vec{j_2} = \overleftrightarrow{\sigma} \cdot \vec{E_2} = \begin{bmatrix} \sigma_{xy} E \\ \sigma_{yy} E \end{bmatrix}, \quad \vec{E_1} = \begin{bmatrix} 0 \\ E \end{bmatrix} \tag{2.25}$$

Considering the rotational invariance as shown in Figure 2.21,

$$\begin{bmatrix} j_{2x} \\ j_{2y} \end{bmatrix} = \begin{bmatrix} \cos(\pi/2) & -\sin(\pi/2) \\ \sin(\pi/2) & \cos(\pi/2) \end{bmatrix} \begin{bmatrix} j_{1x} \\ j_{1y} \end{bmatrix} = \begin{bmatrix} -j_{1y} \\ j_{1x} \end{bmatrix} \tag{2.26}$$

We can write above matrix as

$$\begin{bmatrix} \sigma_{xx} E \\ \sigma_{yx} E \end{bmatrix} = \begin{bmatrix} -\sigma_{xy} E \\ \sigma_{xx} E \end{bmatrix} \tag{2.27}$$

From equation (2.27) $\sigma_{xx} = \sigma_{yy}$ and $\sigma_{xy} = \sigma_{-yx}$, and conductivity tensor is

$$\overleftrightarrow{\sigma} = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} \\ -\sigma_{xy} & \sigma_{xx} \end{bmatrix} \tag{2.28}$$

The resistivity is defined as the inverse of the conductivity. The resistivity tensor in matrix form is as follow

$$\overleftrightarrow{\rho} = \frac{1}{\sigma_{xx}^2 + \sigma_{xy}^2} \begin{bmatrix} \sigma_{xx} & -\sigma_{xy} \\ \sigma_{xy} & \sigma_{xx} \end{bmatrix} = \begin{bmatrix} \rho_{xx} & \rho_{xy} \\ -\rho_{xy} & \rho_{xx} \end{bmatrix} \tag{2.29}$$

where $\rho_{xx} = \dfrac{\sigma_{xx}}{\sigma_{xx}^2 + \sigma_{xy}^2}$ and $\rho_{xy} = \dfrac{-\sigma_{xy}}{\sigma_{xx}^2 + \sigma_{xy}^2}$.

In case of magnetic field is off, $\sigma_{xy} = 0$ and we can get the normal relation between conductivity

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and resistivity

$$\rho_{xx} = \frac{1}{\sigma_{xx}} \tag{2.30}$$

If $\sigma_{xx} = 0$, the $\rho_{xx} = \infty$ which means this system is insulating and dissipative.

In case of magnetic field is on, $\sigma_{xy} \neq 0$ and $\rho_{xx} \neq \frac{1}{\sigma_{xx}}$. The conductivity and resistivity have interesting relation as follow

$$\sigma_{xx} = 0 \quad \Rightarrow \quad \rho_{xx} = \frac{\sigma_{xx}}{\sigma_{xx}^2 + \sigma_{xy}^2} = 0 \tag{2.31}$$

This phenomenon can be explained by assuming that the scattering time is infinite in the Drude model. It means there is no scattering. In this situation, the current flows perpendicular to the applied electric field, so $\vec{j} \cdot \vec{E} = 0$.

$$\vec{E} = \begin{bmatrix} 0 & \rho_{xy} \\ -\rho_{xy} & 0 \end{bmatrix} \begin{bmatrix} j_x \\ j_y \end{bmatrix} = \begin{bmatrix} \rho_{xy} j_y \\ -\rho_{xy} j_x \end{bmatrix} \tag{2.32}$$

$$\Rightarrow \quad \vec{j} \cdot \vec{E} = \begin{bmatrix} j_x & j_y \end{bmatrix} \begin{bmatrix} 0 & \rho_{xy} \\ -\rho_{xy} & 0 \end{bmatrix} = \rho_{xy} j_x j_y - \rho_{xy} j_x j_y = 0 \tag{2.33}$$

We can get the following relation by considering the force on the electron carrying the current.

$$\vec{F} \propto \vec{E}, \quad \vec{v} \propto \vec{j}, \quad \Rightarrow \quad \vec{F} \cdot \vec{v} = 0 \tag{2.34}$$

These results mean the electron current flows without doing any work and dissipation. In other words, $\sigma_{xx} = 0$ means that current does not flow longitudinally like an insulator, and $\rho_{xx} = \infty$ means no dissipation of energy as in a perfect conductor. In QHE, the Hall conductivity and Hall resistivity at certain discrete values of $H$ given by

$$\begin{aligned} \sigma_{xx} &= \rho_{xx} = 0 \\ \sigma_{xy} &= -\frac{1}{\rho_{xy}} = \nu \frac{e^2}{h} \end{aligned} \tag{2.35}$$

These equations indicate that the dissipationless current flows with quantized Hall conductance values in unit of $\frac{e^2}{h}$.

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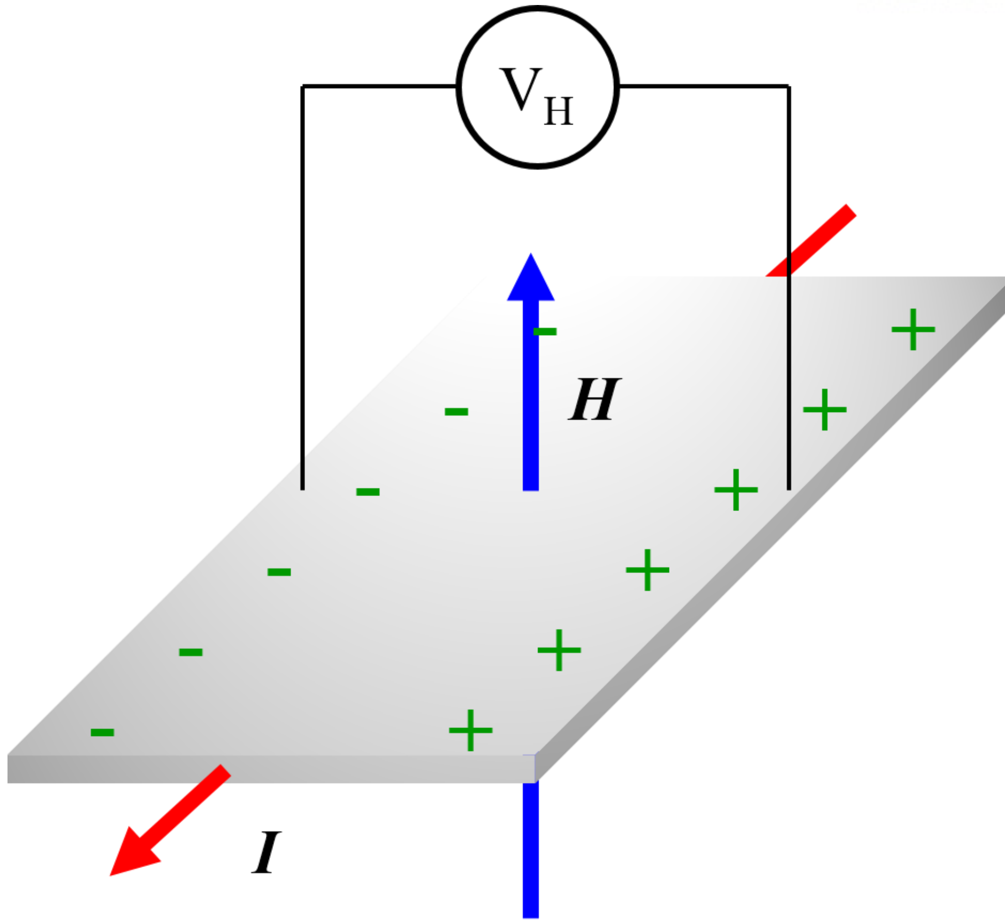


Figure 2.20: Schematic illustration of classical Hall effect [75].

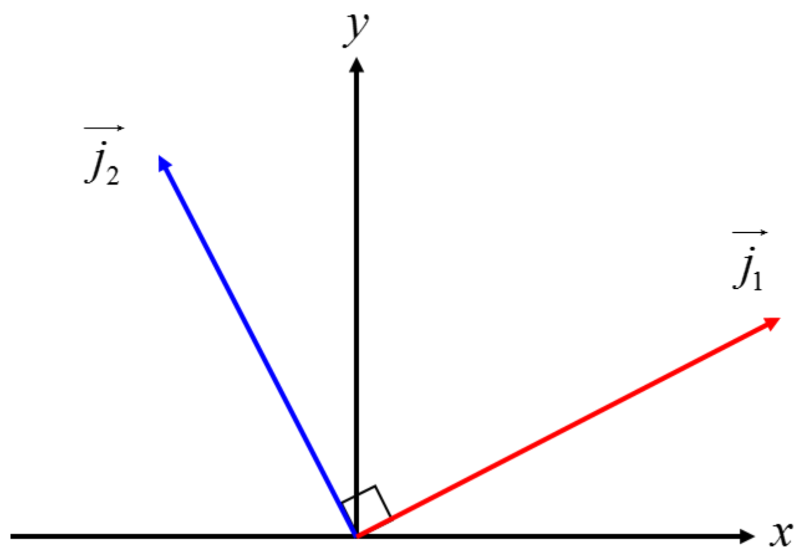


Figure 2.21: Rotational invariance.

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### 2.4.3 The Drude Model

The Drude model was developed by Paul Drude in 1900 to interpret the transport characteristic of electrons in metals [76, 77]. The Drude model's equation of motion is

$$\vec{p} = m\vec{v}, \qquad \frac{d\vec{p}}{dt} = \vec{F} - \frac{\vec{p}}{\tau}$$

$$\Rightarrow \quad \vec{p} = \tau\vec{F}, \quad \vec{v} = \frac{\tau}{m}\vec{F} \quad \text{(in steady state } \frac{d\vec{p}}{dt} = 0) \tag{2.36}$$

In the Hall geometry, the velocity of the particle is obtained as follow

$$\vec{F} = -e\vec{E} - e\frac{\vec{v}}{c} \times \vec{H}$$

$$\Rightarrow \quad \vec{v} = -\frac{e\tau}{m}\vec{E} - \frac{e\tau}{mc}\vec{v} \times \vec{H} \tag{2.37}$$

where $\vec{v} \times \vec{H} = \hat{i}v_y H - jv_x H$ ,

$$\begin{bmatrix} v_x \\ v_y \end{bmatrix} = -\frac{e\tau}{m}\begin{bmatrix} E_x \\ E_y \end{bmatrix} - \frac{eH}{mc}\tau\begin{bmatrix} v_y \\ -v_x \end{bmatrix} \tag{2.38}$$

$$\begin{bmatrix} v_x + \omega_c\tau v_y \\ v_y - \omega_c\tau v_x \end{bmatrix} = -\frac{e\tau}{m}\begin{bmatrix} E_x \\ E_y \end{bmatrix} \qquad \omega_c = \frac{eH}{mc} \tag{2.39}$$

The electric field of matrix form is following as

$$\begin{bmatrix} E_x \\ E_y \end{bmatrix} = -\frac{m}{e\tau}\begin{bmatrix} 1 & \omega_c\tau \\ -\omega_c\tau & 1 \end{bmatrix}\begin{bmatrix} v_x \\ v_y \end{bmatrix} \tag{2.40}$$

The current density $\vec{j}$ is proportional to the velocity

$$\vec{j} = -en\vec{v} \tag{2.41}$$

where $n$ is the electron density. The equation (2.40) then becomes the equation (2.42) using the equation (2.41)

$$\begin{bmatrix} E_x \\ E_y \end{bmatrix} = -\frac{m}{ne^2\tau}\begin{bmatrix} 1 & \omega_c\tau \\ -\omega_c\tau & 1 \end{bmatrix}\begin{bmatrix} j_x \\ j_y \end{bmatrix} \tag{2.42}$$

The resistivity and conductivity are

$$\overleftrightarrow{\rho} = \frac{1}{\sigma_o}\begin{bmatrix} 1 & \omega_c\tau \\ -\omega_c\tau & 1 \end{bmatrix} \tag{2.43}$$

$$\overleftrightarrow{\sigma} = \frac{1}{\overleftrightarrow{\rho}} = \frac{\sigma_o}{1 + (\omega_c\tau)^2}\begin{bmatrix} 1 & -\omega_c\tau \\ \omega_c\tau & 1 \end{bmatrix} \tag{2.44}$$

For the geometry of Hall effect, the current flows the x-direction and associated electric field is y-direction, then the Hall coefficient can be defined

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$$R_H = \frac{E_y}{j_x H} = -\frac{\rho_{xy}}{H} \quad (2.45)$$

In the Drude model, the resistivity tensor is

$$\rho_{xx} = \frac{1}{\sigma_o} = \frac{m}{ne^2\tau}$$
$$\rho_{xy} = \frac{\omega_c \tau}{\sigma_o} = \frac{H}{nec} \quad (2.46)$$

The only $\rho_{xy}$ depends on the magnetic field $H$. Figure 2.22 shows plot of resistivity according to the magnetic field.

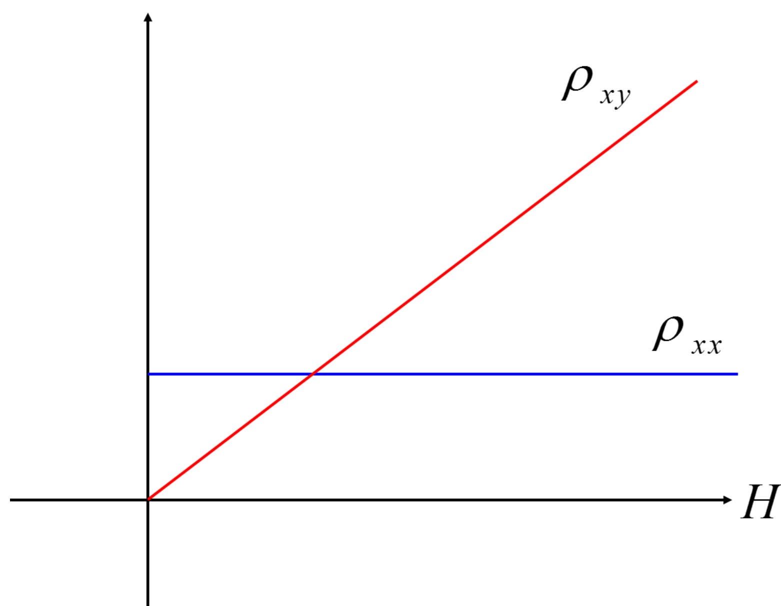


Figure 2.22: The plot of resistivity ( $\rho_{xx}$ and $\rho_{xy}$ ) according to the magnetic field.

### 2.4.4 Integer Quantum Hall Effect (IQHE)

Figure 2.23 shows measurement results of the Hall resistance and longitudinal magneto-resistance in two-dimensional electron gas system according to the magnetic field [78]. The Hall resistance curve has a series of plateaus with values of $\rho_{xy} = \frac{h}{\nu e^2}$ where $\nu$ is integer. The center of plateaus is located at $H$ values of $\frac{n}{\nu}\phi_o$. As the value of $\nu$ decreases, the width of plateaus increases.

$$\rho_{xy} = \frac{h}{\nu e^2} = \frac{H}{nec}$$

$$\Rightarrow H = \frac{n}{\nu}\frac{hc}{e} = \frac{n}{\nu}\phi_o \quad \text{where } \phi_o = \frac{hc}{e} \tag{2.47}$$

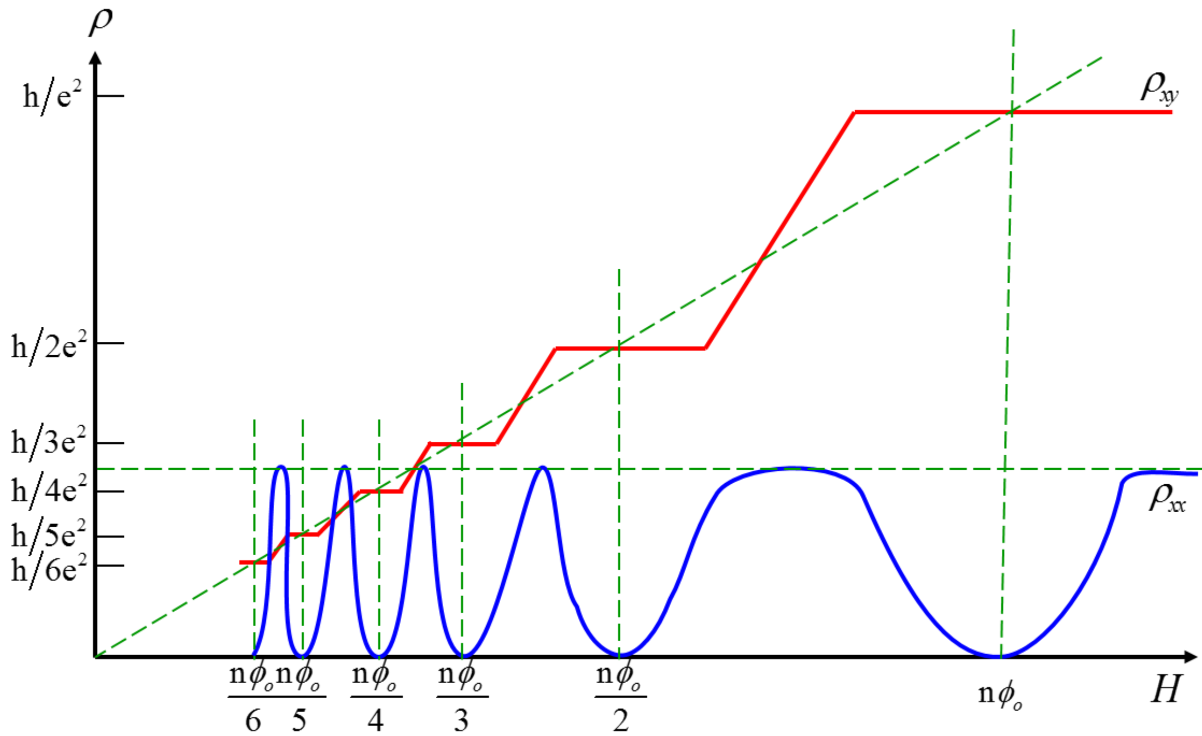


Figure 2.23: Hall resistance and longitudinal magneto-resistance in two-dimensional electron system according to the magnetic field [78].

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## III. Experimental Methodology and Characterization Techniques

The EG Films on SiC substrate is prepared by thermal heating in UHV chamber. The EG device is fabricated using several techniques such as patterning, etching and metal deposition. Here, the photolithography, Reactive Ion Etching (RIE) and e-beam evaporator are used. The properties of samples are analyzed by Raman Spectra, SEM, AFM, Electrical Measurement. In this chapter, we introduce the experiment setup and measurement systems

### 3.1 UHV Chamber Systems for Growth of EG

Our UHV chamber consists with two parts including main chamber and loadlock chamber as shown Figure 3.1. It is isolated by gate valve except for the loading and unloading sample. The sample can be loaded through the loadlock chamber while maintaining vacuum in the main chamber. The transfer arm deliver sample from loadlock chamber to main chamber. Two types of pumps, rotary and turbo, are used to obtain the vacuum circumstance. The pressure in the chamber is reduced to ~$10^{-3}$ torr by a rotary pump and then a turbo pump is used to obtain lower pressure. The base pressure of main chamber is ~$6.0 \times 10^{-9}$ Torr and the loadlock chamber can decrease the pressure to ~$10^{-7}$ Torr. The pressure in the chamber is measured by convection and ion gauge. The working range of convection and ion gauge is down to $10^{-3}$ Torr and $10^{-12}$ Torr. The PBN heater is used as a heating source. The ceramic and heat shield can increase the temperature up to ~1300 °C by preventing thermal radiation loss. The temperature is measured by thermocouple. Cooling water flows the chamber during the annealing sample which prevent the entire system is heated up except for sample. The cooling water circulates through the chamber during heating which prevent other system except for sample is heated. The sample holder is made of Molybdenum for using at high temperature. Figure 3.2 shows the process of sample heating.

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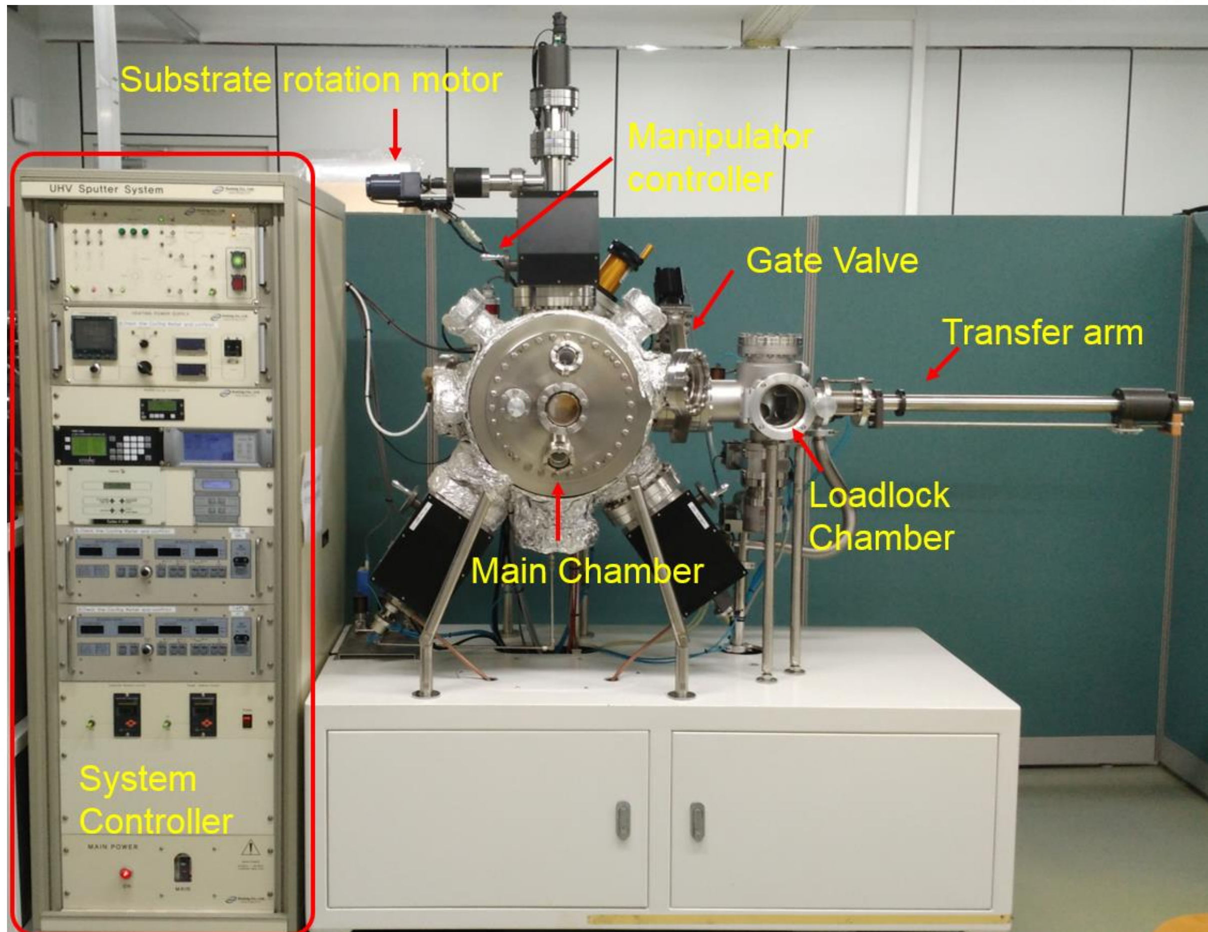


Figure 3.1: Photograph of our UHV system for growth of EG.

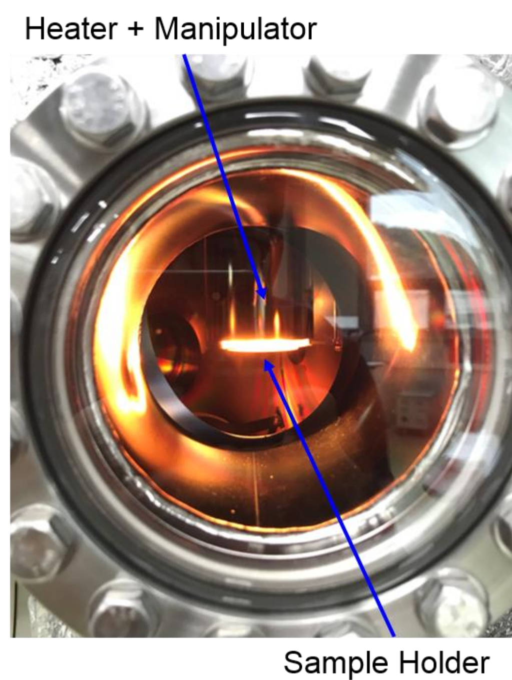


Figure 3.2: Photograph of heating module and sample holder during annealing.

### 3.2 Photolithography

Photolithography means that the transfer of geometry of a mask to the surface of substrate by using light and photoresist. It is used in fabrication of micro-scale device. The process of photolithography involves wafer cleaning, photoresist coating, soft-baking, ultraviolet (UV) light exposure, development, etching, photoresist removal. Before the coating photoresist on the substrate, the surface is cleaned to remove contamination by chemical treatment. This process improves the adhesion between substrate and photoresist.

Photoresists are classified into two types, positive and negative, depending on their response to UV light as show in Figure 3.3 [79-81]. For the photoresist, UV light exposure changes the chemical structure of photoresist to dissolve in the developer. The negative resist shows the opposite tendency. UV light exposed resist become to polymerized and is not dissolved in developing solution. We explain the photolithography process based on commonly used positive photoresist. The photoresist is coated on substrate by spin-coating. The speed (3000-6000 rpm) and period (15-60 sec) of spin-coating are adjusted depending on the kind of photoresist. A small amount of resist in the center of wafer spreads uniformly over the whole area of wafer surface. The typically thickness of layer is between 0.5 μm and 2.5 μm. The coated sample is then prebaked on hotplate or in convection oven to evaporate the solvent in the resist. After prebake, the property of the coated photoresist is sensitive to UV light.

The mask is aligned with the sample. Each mask from second mask has to be aligned with the previous pattern. After aligned process, the photoresist coated sample is exposed to UV light. There are three types of exposure methods: contact, proximity, and projection (Figure 3.4) [82, 83]. In the contact printing, the photoresist coated sample is physically contacted with photomask during UV exposure. Due to the very small gap between the sample and mask, this method has high resolution about 1 μm. The proximity method is similar to contact method but they maintain the small gap about 10~25 μm. From this, the resolution is lower than contact mode, but it can avoid damage from defects. The projection method not only completely avoid damage, but also provides a high resolution of about 1 μm. The exposed photoresist is removed by developer.

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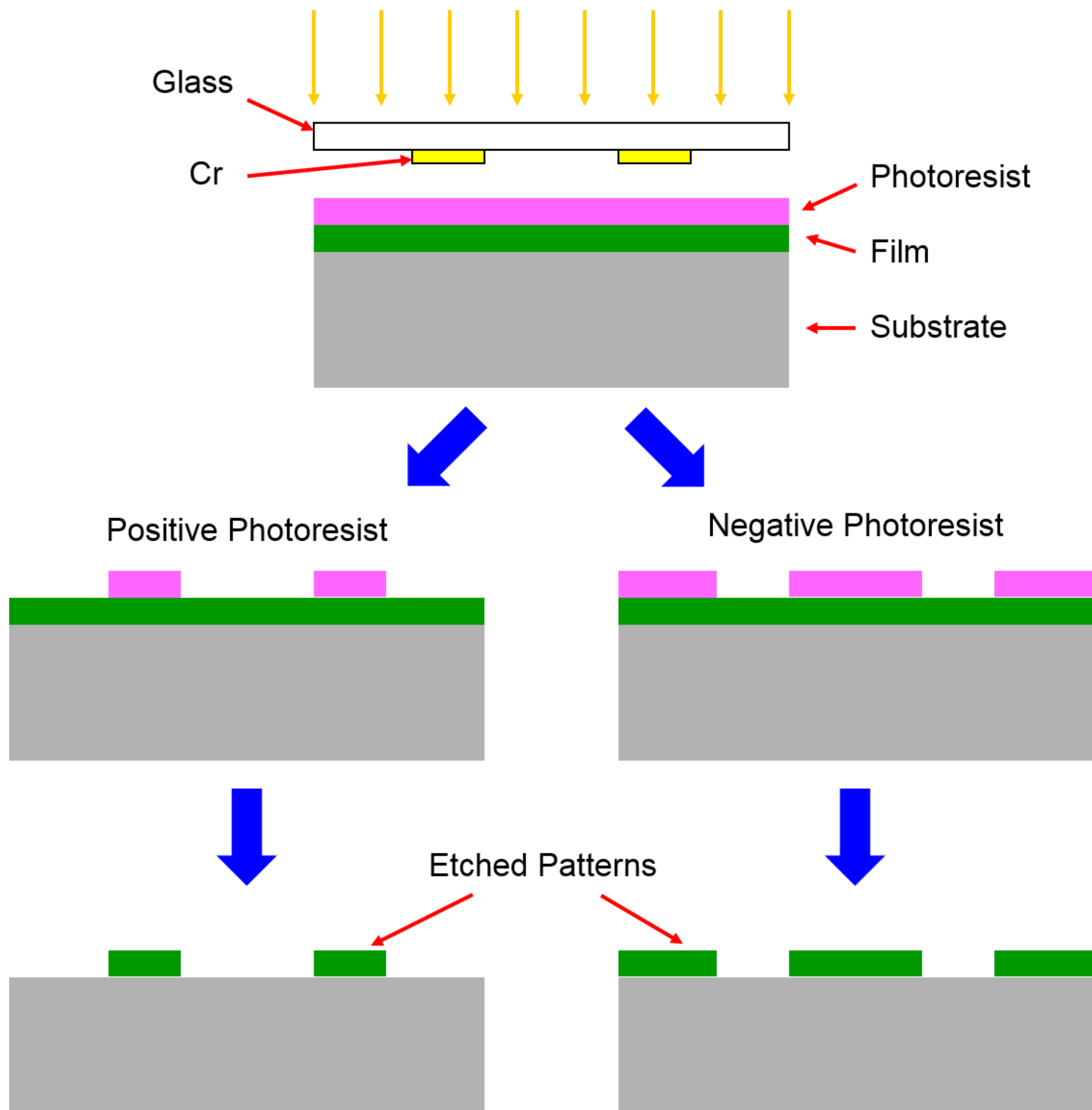


Figure 3.3: Photolithography process with positive and negative photoresist.

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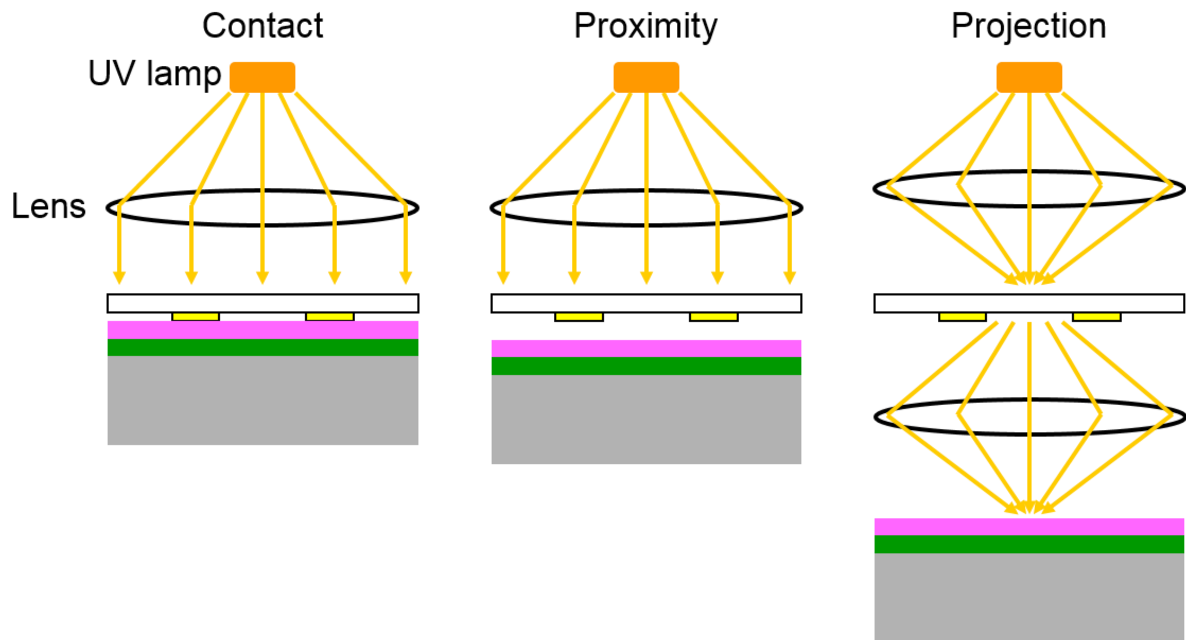


Figure 3.4: Three exposure methods of (a) contact, (b) proximity, and (c) projection mainly used in photolithography [83].

### 3.3 Raman Spectroscopy

Raman spectroscopy is rapid, non-destructive tool that is widely used to analyze the sample structure. It is developed by C. V. Raman in 1928 based on the detection of inelastic scattering light [84].

The incident light absorbed in sample lead to vibrates the electron cloud, which oscillate the atoms. The different energy compared to incident light is reemitted. The frequency of reemitted energy is shifted up or down, which called Raman shift. These results provide the properties information of material about the atomic constitution, bonding structure, and impurity. Figure 3.5 represents the energy level diagram showing the energy transition for Rayleigh, Stokes Raman, and Anti-Stokes Raman scattering. First, when molecule emits photon with the same frequency as the incident light, it is an elastic process and called Rayleigh scattering. Second, the emitted photon energy is less than the incident laser. Third, excited phonon molecules are excited to higher virtual state, and then return to the ground state by emitting more energy than incident photon, which is called Anti-Stokes scattering [85, 86].

Raman spectroscopy is powerful equipment to analyze the graphene characteristic such as thickness, defects, disorder, doping, and stain. Figure 3.6 shows the calculated phonon dispersion relation of the graphene. There are six phonon dispersion bands because unit cell of graphene has two carbon atoms. Three of them are acoustic branches (A) and the other three are optical (O) branches. In case of one acoustic and optical branch, the out of plane (o) phonon modes shows the atomic oscillation being perpendicular to the basal plane of graphene. The vibrations of other four branches shows in-plane (i) of graphene. The atomic vibrations can be classified to longitudinal (L) or transverse (T) mode with the direction of C-C bonds [87].

The Raman spectrum of pristine graphene appears activate peaks near 1580 $cm^{-1}$ (G-peak) and 2670 $cm^{-1}$ (2D-peak). The disordered graphene shows the defect related peak around at 1350 $cm^{-1}$ (D-peak). Figure 3.7 shows schematic illustration of the Raman scattering mechanism at the $K$ and $K'$' points of graphene. The G-peak is related to the doubly degenerate longitudinal and transverse phonon (LO and iTO) modes at the Brillouin zone center. The G and D peak is associated with a secend-order process. The G peak contain ns two iTO phonons near the K point but D peak involves the one iTo phonon and defect [87, 88].

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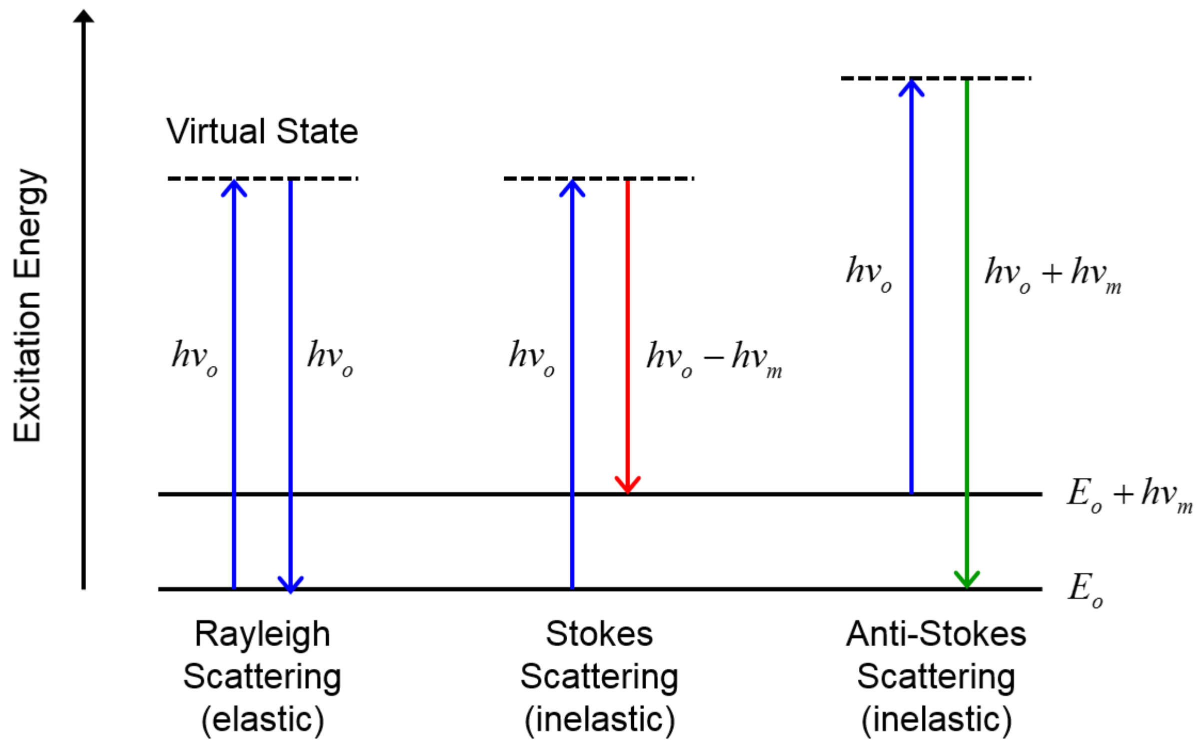


Figure 3.5: Energy level diagram representing different energy states for Rayleigh, Stokes, and Anti-Stokes Scattering [85].

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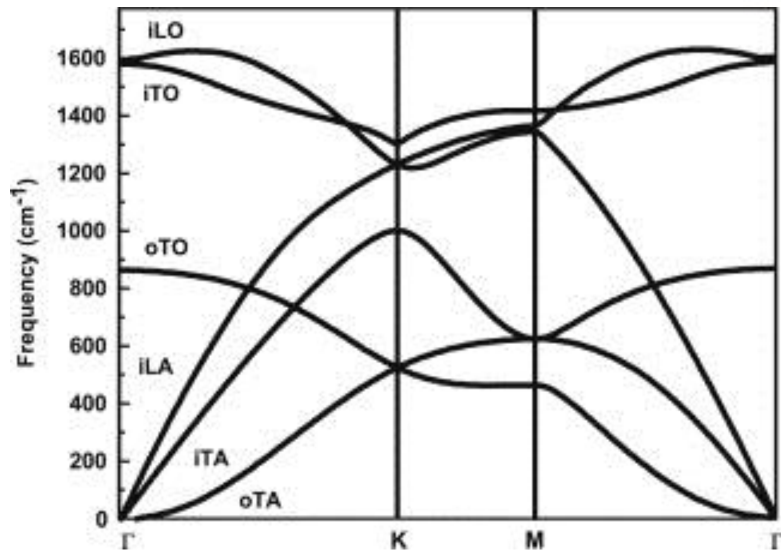


Figure 3.6: Calculated phonon dispersion for graphene. The six phonon dispersion curves show iLO, iTO, oTO, iLA, iTA, and oTA [87].

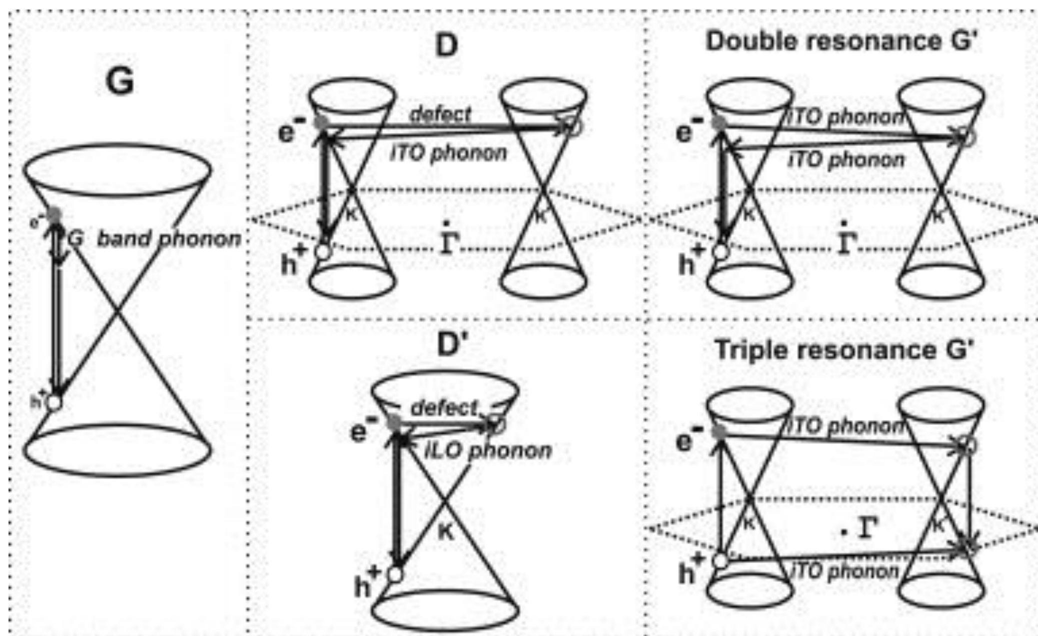


Figure 3.7: Schematic showing the electronic scattering near K and K' points of monolayer graphene. (a) First order for G-band, one phonon second-order double resonance for (b) D (intervally) and (c) D' (intravally), two phonons second order (d) double resonance (e) triple resonance for 2D peak [87, 88].

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### 3.4 Atomic Force Microscopy (AFM)

The AFM was developed in 1986 by G. Binnig and C. F. Quate to analyze the surfaces topography on a similar principle to scanning tunneling microscope (STM) [89]. In constrast to STM, the AFM can investigate the surface of insulating samples as well as conductive samples. The AFM consists of probe, cantilever, scanner, laser, and photodetection as shown in Figure 3.8 [90]. The AFM uses the forces interacting between the atom at the top of sharp tip (< 10 nm radius) and the atoms on sample surface. This force can be explained using Hooke's law as following [91]

$$F = -k \cdot x \tag{3.1}$$

where $F$ is Force, $k$ is spring constant and $x$ is cantilever deflection.

The interatomic force is affected by the distance between the sample and the tip (Figure 3.9). At close distances, the repulsive force (Van der Waals force) is dominant. As the tip moves further away from the surface, the attractive force is applied between tip and surface [91]. Depending on the type of interaction force, the AFM operating modes are divided into three categories: contact, non-contact and tapping mode (Figure 3.10) [92].

In contact mode, the tip is in close contact with the sample surface while scanning the entire surface. At this time, the repulsive force between the tip and the sample is kept constant. This mode is suitable for stable and flat sample because the tip can mechanically damage to the sample surface.

In non-contact mode, the attractive forces are used to scan the sample. The vibrating tip sweeps over the sample without contact. The force from the sample surface affects the tip, which causes a change in the frequency and phase of the vibration. These signals are used to obtain the surface image. Sensitive samples are suitable for this mode. In tapping mode operating between contact and non-contact mode, the tip taps or hits the sample surface at high frequency during the scanning to reduce the risk of mechanical damage from dragging particles.

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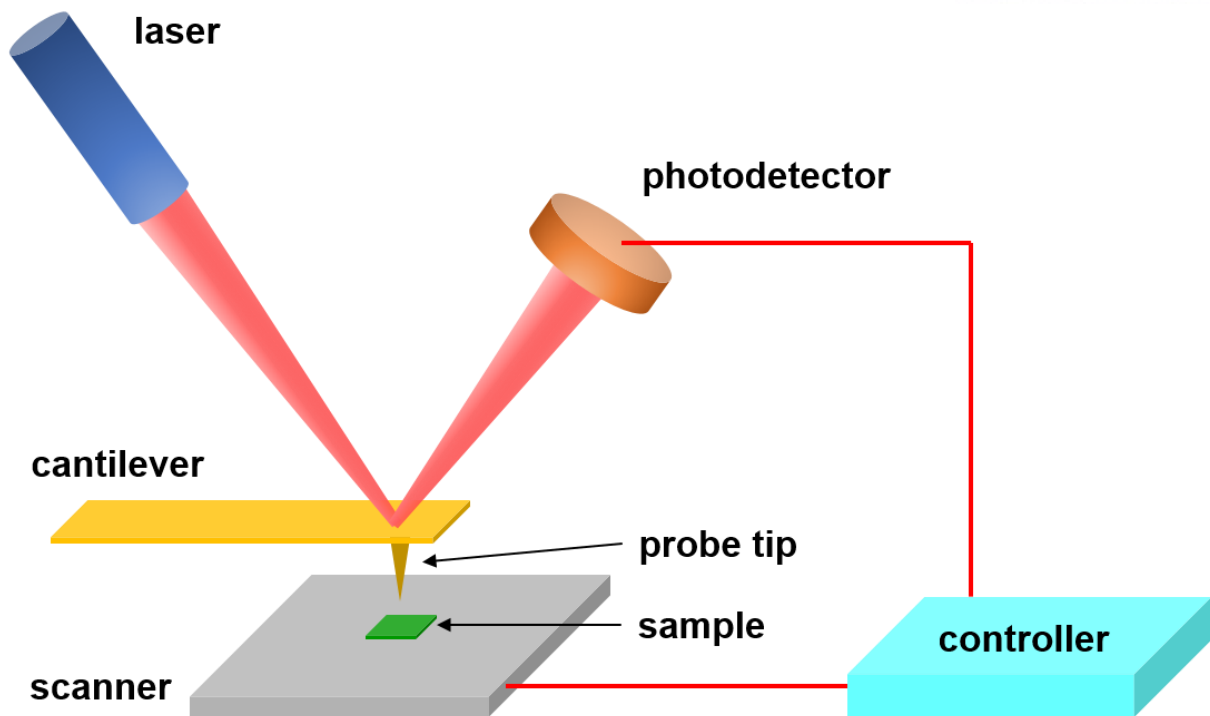


Figure 3.8: Schematic illustration of AFM principle [90].

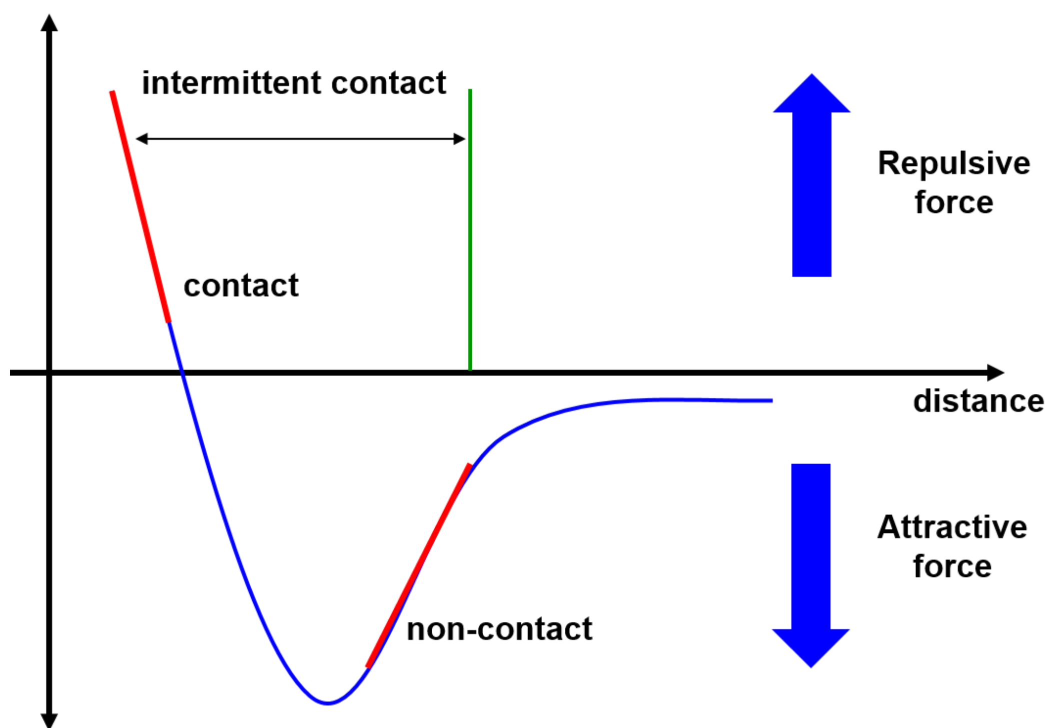


Figure 3.9: Interatomic force according to the distance between tip and sample [91].

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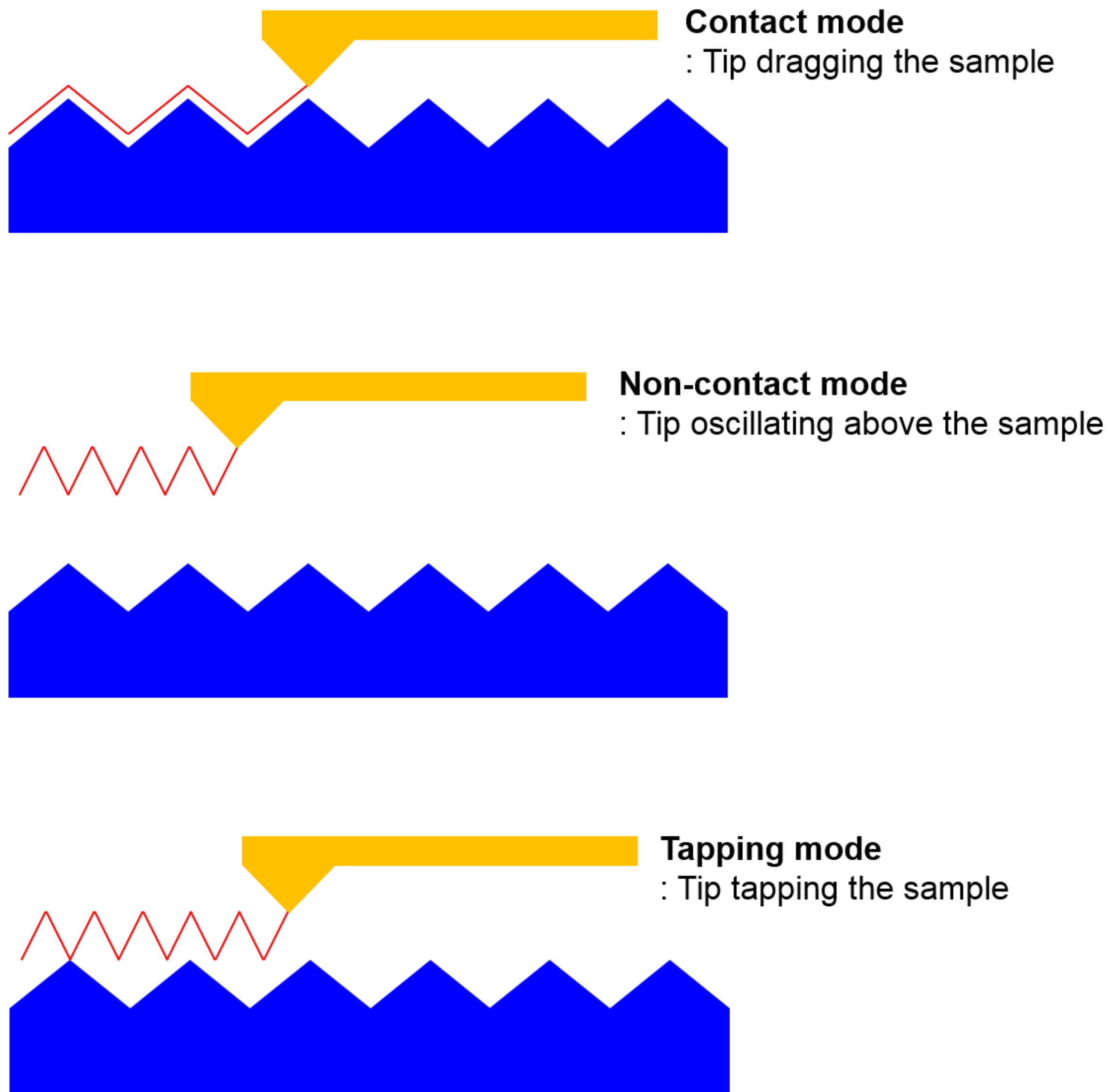


Figure 3.10: Operating modes of AFM: contact, non-contact, and tapping mode [92].

# IV. Growth, Characterization, and Devices of EG on SiC

In this chapter, we will report on research results related to EG during my PhD course. we suggest two methods to grow graphene effectively at low temperatures. First, we introduce effective growth method of high quality EG at relatively low temperature by Molybdenum plate (Mo-plate) capping [11]. This method is very simple and inexpensive compared to other CCS methods. The Mo-plate prevents the heat radiation loss from SiC surface during annealing, so the temperature of Mo-plate capped SiC is higher than UHV exposed SiC. We called it Radiation Mirroring. The Mo-plate also reduces the Si sublimation rate from SiC substrate because it increases the Si atoms vapor density in narrow gap between Mo-plate and SiC surface. From this, high quality graphene is formed at relatively low ambient temperature. Second, we report on growth of EG on amorphous and crystalline SiC substrate at relatively low temperature by e-beam irradiation. The penetration depth of e-beam is very shallow at low electron acceleration voltage, so heat is directly transferred to sample surface or few atomic layers of SiC. Therefore, only thin layer of SiC surface is heated efficiently. The strong electric field formed by accumulated electrons at the penetration depth can induce sublimation of Si atoms. we believe that thickness control of graphene can be adjusted according to the intensity of the accelerating voltage.

One of problems in fabricating graphene device is polymer residue on graphene surface after patterning such as photolithography and e-beam lithography. This polymer residue induces the unintentional doping and degradation of sample quality. In order to solve this problem, Al thin film is used as an etching mask. The contact pads are also deposited using shadow mask without polymer process. The properties of EG sample fabricated with Al thin film and conventional photolithography is analyzed by Hall measurement. The characteristics of the EG samples fabricated with Al thin films were analyzed by the Hall measurement method compared with the EG samples prepared by the conventional photolithography method.

## 4.1 Improved Crystallinity of EG Grown on 4H-, 6H SiC Surface using Molybdenum Plate Capping

Graphene is a two-dimensional material, which consist of single layer C atoms arranged in a honeycomb hexagonal structure [1, 4-6]. Due to its outstanding mobility, graphene has been regarded as a promising candidate for ultra-high speed electronic devices operating in the THz frequency range [93]. The graphene is first obtained by mechanically peeling from HOPG by a Scotch tape method. The purest monocrystalline graphite flakes are obtained by mechanical exfoliation, but are too small to be used in practical devices. In order to overcome this problem, several alternative methods such as CVD [46, 94], solid source deposition [95, 96], and surface graphitization of SiC [5, 7-10, 57] have been studied. Especially, the growth of EG on single crystalline SiC by thermal annealing in UHV [5] or Ar environment [7] is promising method for forming large size graphene. At high temperatures (> 1300 °C), only Si atoms sublimate on the surface and the remaining C atoms rearrange to EG on the Si-face

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(0001) and C-face (000-1) SiC [97]. The EG grown on the C-face SiC is normally thicker than that on Si-face, but the mobility is higher due to the stacking structure. Rotating stacking faults in the multilayer EG on the C-face SiC electrically decouple the adjacent graphene layers and thus the multilayer graphene exhibits electronic properties of an isolated single layer graphene [62]. The large area growth of EG on the SiC surface and its excellent electrical properties clearly show the potential to be applied to the platforms of next generation electronic devices. However, it is essential to decrease the growth temperature of EG to reduce manufacturing costs. It is very important for practical commercialization of EG-based electronic applications. Here, we introduce a novel EG growth method that remarkably enhances the crystallinity of EG by capping the Mo-plate on hexagonal SiC substrate.

### 4.1.1 Growth and Structural Analysis of EG on n-type 4H-SiC (000-1)

The n-type 4H-SiC (000-1) substrate 4-degree miscut to <11-20> is prepared for the EG formation experiment. Before annealing, the SiC substrate and Mo-plate cleaning step are performed as follow. The organic contaminants of SiC substrate is cleaned with acetone and methanol for 10 mins, respectively, and the native oxide on the SiC surface is removed with HF (49 %) for 60 sec. We also performed the Mo-plate cleaning process in HCl : $H_2O$ (2:1) solution for 10 mins and rinsed with deionized (DI) water to remove contaminants generated during the machining processes. In addition, the Mo-plate is heated to 500 °C in UHV for 10 mins. Figure 4.1 shows the experiment setup of Mo capping for growth of EG. To demonstrate the characteristics of the grown EG *with* and *without* Mo-plate capping, the one of the 4H-SiC (000-1) surface is capped with Mo-plate and the other 4H-SiC (000-1) surface is exposed to UHV during heating. These two sample are heated for 10-60 min at 850-950 °C, which is a relatively lower temperature that the previous experiments. The temperature is confirmed by an infrared (IR) pyrometer and thermocouple. Here, the location of measured temperature is near the Mo-plate and the SiC sample. The temperature on the SiC surface covered with the Mo-plate is not directly measurable and is expected to differ from the measured value. The base pressure of chamber is $6.0\times10^{-9}$ Torr, and the working pressure is increased up to $\sim4.6\times10^{-6}$ Torr when the sample is heated for 60 min at 900 °C.

Raman spectroscopy (Alpha 300R, WITec) is used to determine the structural qualities of the grown EG. The laser excitation energy is ~ 2.33 eV (532 nm) and the laser spot size is 1.2 m at the laser power of 3 mW. Figure 4.2 indicates Raman spectra results for EG formed on n-type 4H-SiC (000-1) by thermal annealing at 900 °C *with* and *without* Mo-plate capping. Here, the 4H-SiC substrate signal is subtracted to prevent overlap with the EG signal. The D, G, and 2D peaks indicating EG characteristics are obviously observed. These Raman peaks (D, G, 2D) are obviously observed in both samples, but the relative intensity and location of peaks are different. These results demonstrate that the properties of the EG formed are significantly influenced by the presence of the Mo-plate capping. For EG grown *without* Mo-plate capping, the intensities of the 2D peak and the D peak are about 1.9 times and 0.4

times the intensity of the G peak, respectively, and the D + G peak is also clearly observed. These mean that the grown EG contains a lot of defects and the size of graphene grains is very small in nanoscale units [87, 98]. These results are caused by the rapid sublimation rate of Si atoms at low temperature in UHV environments. In contrast, for EG grown by Mo-plate capping, the 2D peak size is 1.25 times greater than the G peak size and the D and D+G peaks are very small. These differences indicate that Mo-plate capping helps to form high-quality graphene with large particle size and fewer defects. The location and shape of the G and 2D peaks also provide significant information about the thickness and stacking structure of the formed graphene. Generally, the EG shows the blue shifted G-peak because of the compressive strain between substrate and EG [87, 98, 99]. In the obtained Raman spectra, the G-peak of both samples were blue shifted to ~1588 $cm^{-1}$ (*with* Mo-plate) and ~1596 $cm^{-1}$ (*without* Mo-plate), respectively, compared to the G peak (~1580 $cm^{-1}$) of a mechanically exfoliated mono-layer graphene. Here, the G-peak shift of graphene formed by Mo-capping is smaller because the compressive strain is relaxed by the thick thickness of EG. This explanation can also be explained through the location of 2D peak. The 2D peak position (~2680 $cm^{-1}$) of EG grown *without* Mo-plate shows typical characteristic of thin EG on SiC (000-1) substrate. By contrast, the 2D peak position of the EG formed *with* Mo-plate capping is blue shifted to ~2711 $cm^{-1}$ like the bulk graphite of ~2725 $cm^{-1}$ [87, 98]. It is obvious evidence that the EG formed using Mo-plate capping is thicker. The shape of the 2D peak also informs the stacking structure of the graphene layer. The 2D peak shape of the EG formed *with* Mo-plate capping shows fairly symmetric. It is well fitted to a single Lorentzian and its full width at half maximum (FWHM) of ~47 $cm^{-1}$ is larger than value (~24 $cm^{-1}$) of monolayer graphene. It means that the stack of graphene layers has a turbostratic [87, 98] structure which randomly rotates relative to each other rather than AB-Bernal. This is a frequently observed structure in EG grown on SiC (000-1) [62].

The SEM images of grown EG were obtained to analyze the surface characteristics using Hitach Cold FE-SEM. Figure 4.3(a) indicates the SEM image of 4H-SiC surface annealed at 900 °C *without* Mo-plate which is almost the same as the bare SiC surface before annealing. This means that graphitization of the 4H-SiC substrate is localized near the surface and does not lead to any clear change on surface shape. By contrast, the 4H-SiC surface heated *with* Mo-plate capping shows significantly different. The surface is fairly rough, which is believed to be due to the growing EG. The grain size of the EG grown at 900 °C (Figure 4.3(c)) is bigger than at 850 °C (Figure 4.3(b)). As the temperature increased at high temperature, Si atoms actively sublimated from SiC surface and graphene is grown, and step bunching became more active at high temperature.

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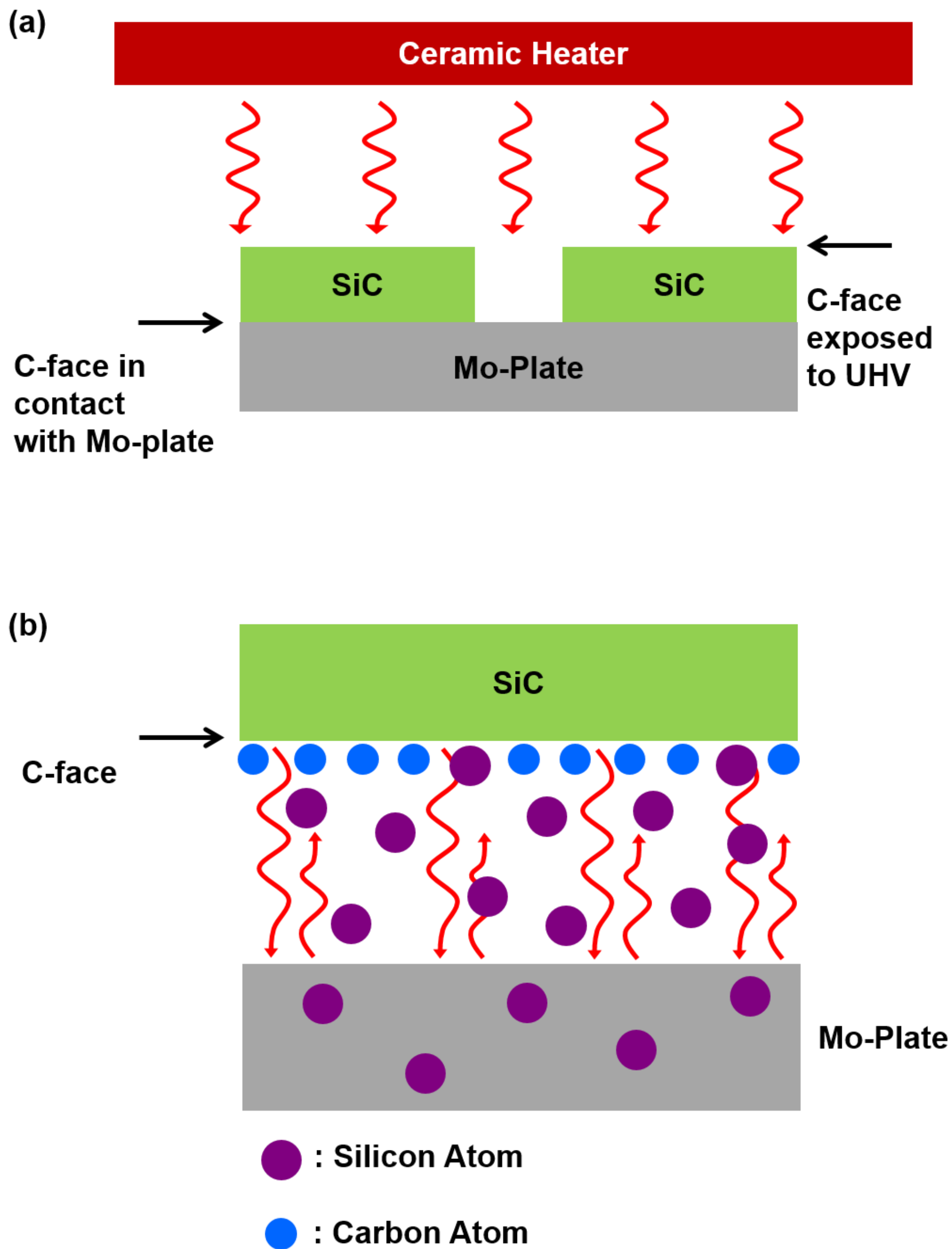


Figure 4.1: (a) Experiment setup for simultaneously annealing SiC substrate in UHV *with* (left) or *without* (right) Mo-plate capping. (b) The enlarged image of the SiC surface covered with Mo-plate during annealing [11].

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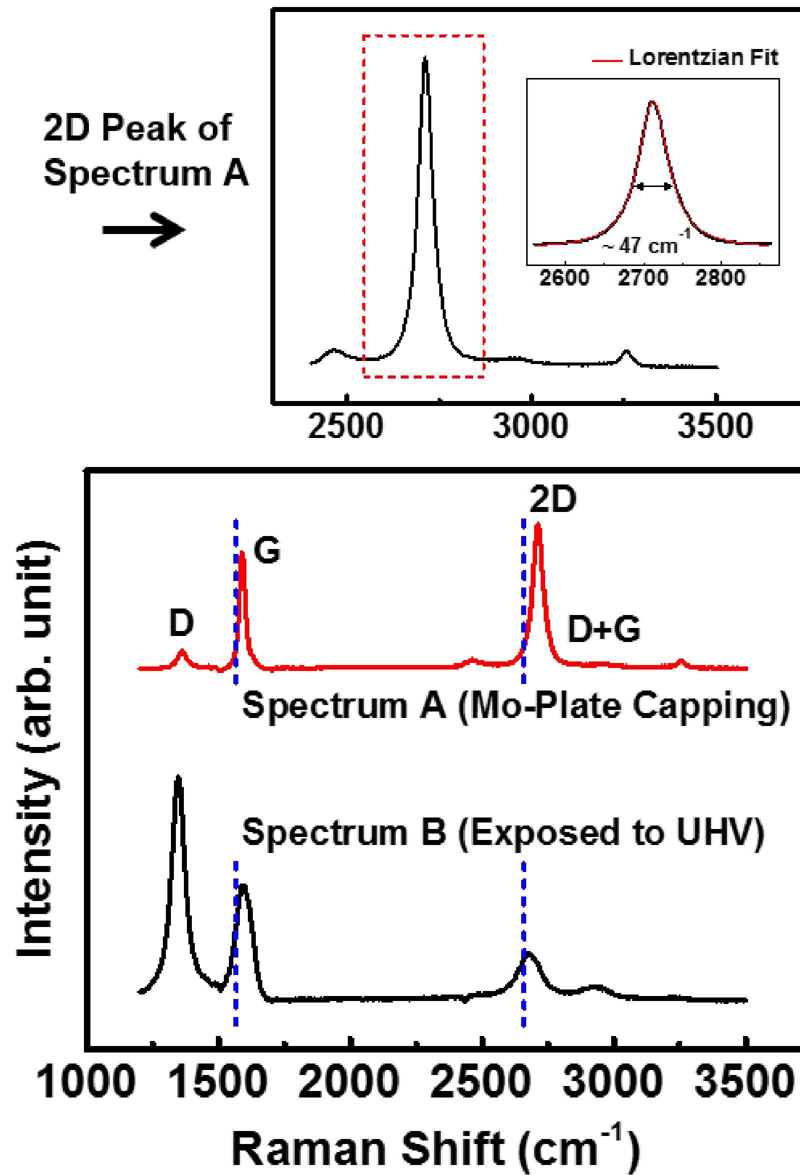


Figure 4.2: Raman spectra of grown EG on n-type 4H-SiC (000-1) *with* and *without* Mo-plate capping [11].

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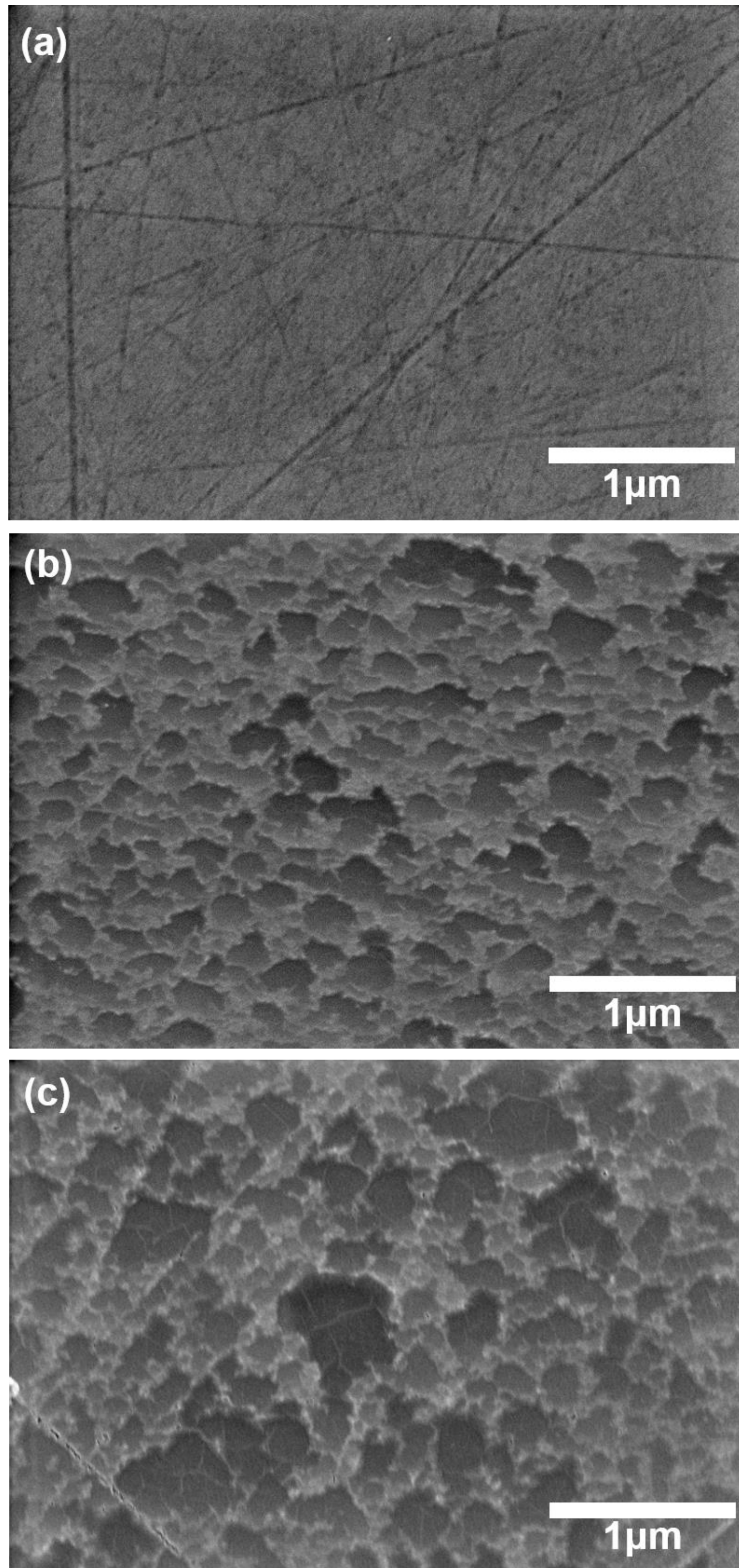


Figure 4.3: SEM images of annealed n-type 4H-SiC (000-1) substrate (a) at 900 °C in UHV circumstance (*without* Mo-plate capping) at (b) 850 °C and (c) 900 °C *with* Mo-plate capping [11].

**4.1.2 Growth and Structural Analysis of EG grown on semi-insulating 6H-SiC (0001) Surface using Mo-plate capping**

Unfortunately, n-type 4H-SiC (000-1) is not suitable substrate for analyzing the electrical characteristic of grown EG due to substrate leakage current and polishing scratches (Figure 4.3). Hence, we re-form EG on semi-insulating on-axis 6H-SiC (0001) without polishing scratches to analyze the electrical properties. The EG on the semi-insulating 6H-SiC (0001) surface was formed in the same method at a temperature of 950 °C as shown in Figure 4.1. Through the Raman spectra (Figure 4.4), improved structural quality of formed EG using Mo-plate capping is demonstrated. The monolayer formation of graphene grown using Mo-plate capping is evidenced by ratio of 2D peak to G peak (~5:1) and the FWHM of 2D peak (~34 $cm^{-1}$). Its electrical characteristic has been demonstrated by top gate FET devices. Figure 4.5 indicates the AFM image of grown EG on 6H-SiC substrate *with* Mo-plate. The width and steps height of terraces are ~2 μm and ~1.5 nm. Uniform thickness of graphene is grown well along the SiC surface. Figure 4.6 indicates the fabrication process of FET devices. The EG channel is defined by photolithography patterning and $O_2$ plasma etching at 100 W. The photoresist is removed by acetone, but photoresist residue of 25 nm thickness is confirmed by surface profiler (KLA Tencor) and optical microscope as shown in Figure 4.6(b). It is used as a seed layer of gate oxide. The source and drain contact pads are formed by deposition of Ti/ Au (10 nm/ 50 nm) and lift-off. The $HfO_2$ gate oxide with 50 nm thickness is deposited by ALD. Finally, the gate contact pads are formed in the same manner as source and drain contact pads. The electrical properties of fabricated FET were confirmed at room temperature in atmosphere. Figure 4.7 shows the current curve according to gate voltage at several drain voltages. The charge neutral point is located around -2 V and the major carrier type of grown EG film is n-type. The field effect mobility ($\mu_{FE}$) is 1800 $cm^2/Vs$ at drain voltage of 0.1 V, which is extracted from measured current-voltage curve. This result is higher than value measured in other groups for grown EG on SiC (0001) by the conventional UHV annealing in the range from 200 to 1200 $cm^2/Vs$. The excellent electrical properties of EG grown by Mo-plate capping are consistent with high structural quality. Here, the $\mu_{FE}$ is defined as following

$$\mu_{FE} = \frac{L_{ch}}{W_{ch}} \cdot \frac{g_m}{C_G V_D} \tag{4.1}$$

where $L_{ch}$ and $W_{ch}$ are channel length and width, $g_m$ is transconductance ($dI_D/dV_G$), and $C_G$ is a channel to gate capacitance. In our device, $C_G$ is calculated as following

$$\frac{1}{C_G} = \frac{1}{C_{photoresist}} + \frac{1}{C_{HfO_2}} \tag{4.2}$$

where $C_{photoresist}$ and $C_{HfO_2}$ are capacitance of photoresist seed layer and gate oxide. They are determined by

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$$\varepsilon_o \varepsilon_r \frac{A}{d} \tag{4.3}$$

where $\varepsilon_o$ is a vacuum permittivity, $\varepsilon_r$ is a dielectric constant (4.0 for photoresist and 12.0 for $HfO_2$), $A$ is the channel area, and $d$ is a thickness of gate oxide.

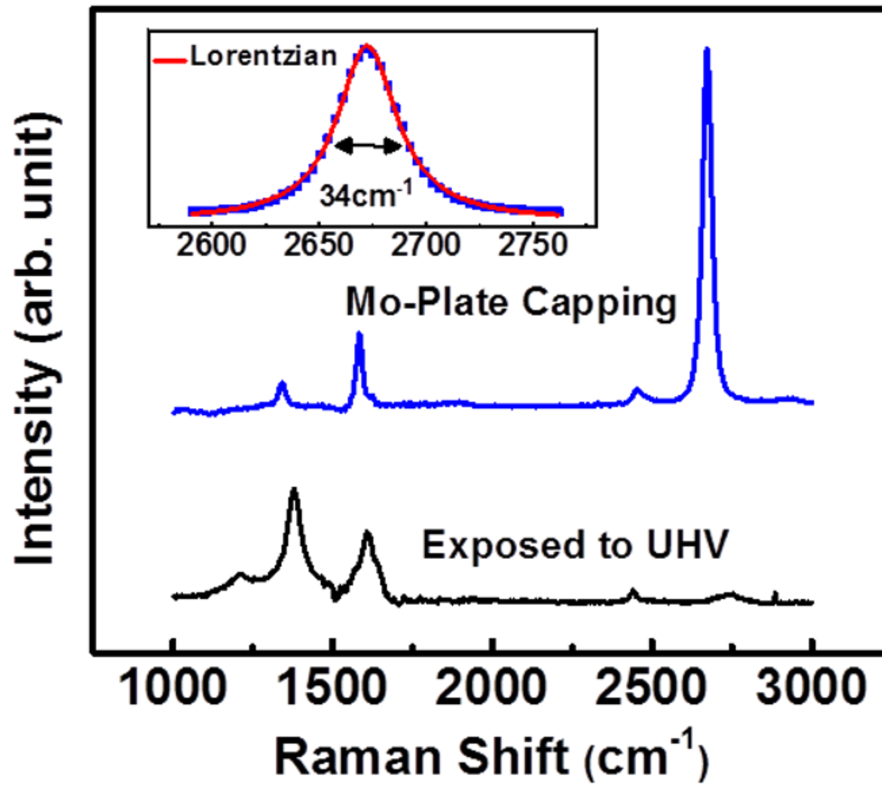


Figure 4.4: Raman spectra of EG formed on semi-insulating 6H-SiC (0001) substrate *with* and *without* Mo-plate capping [11].

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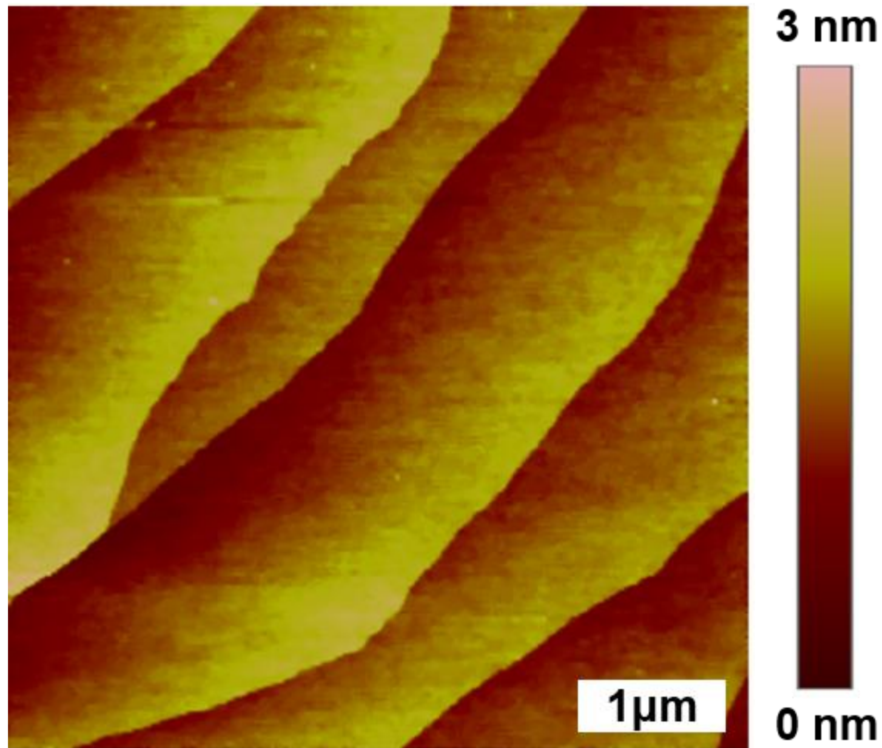


Figure 4.5: AFM image of EG grown on semi-insulating 6H-SiC (0001) *with* Mo-plate capping.

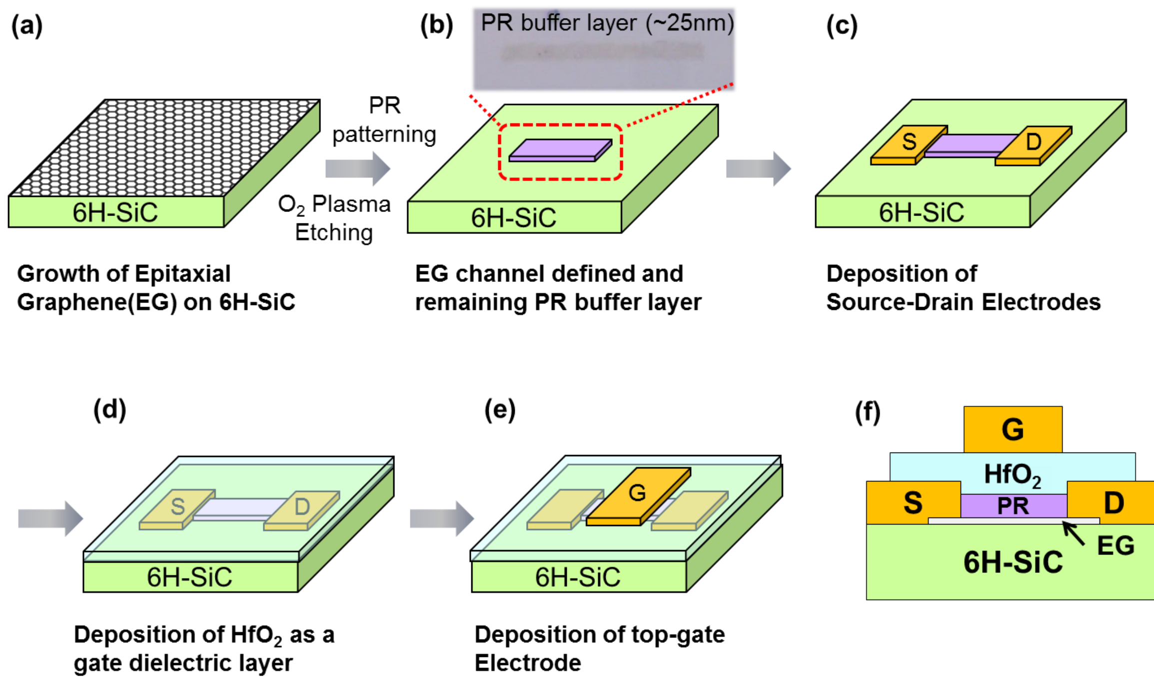


Figure 4.6: Schematic diagram of top-gated EG FET fabrication process [11].

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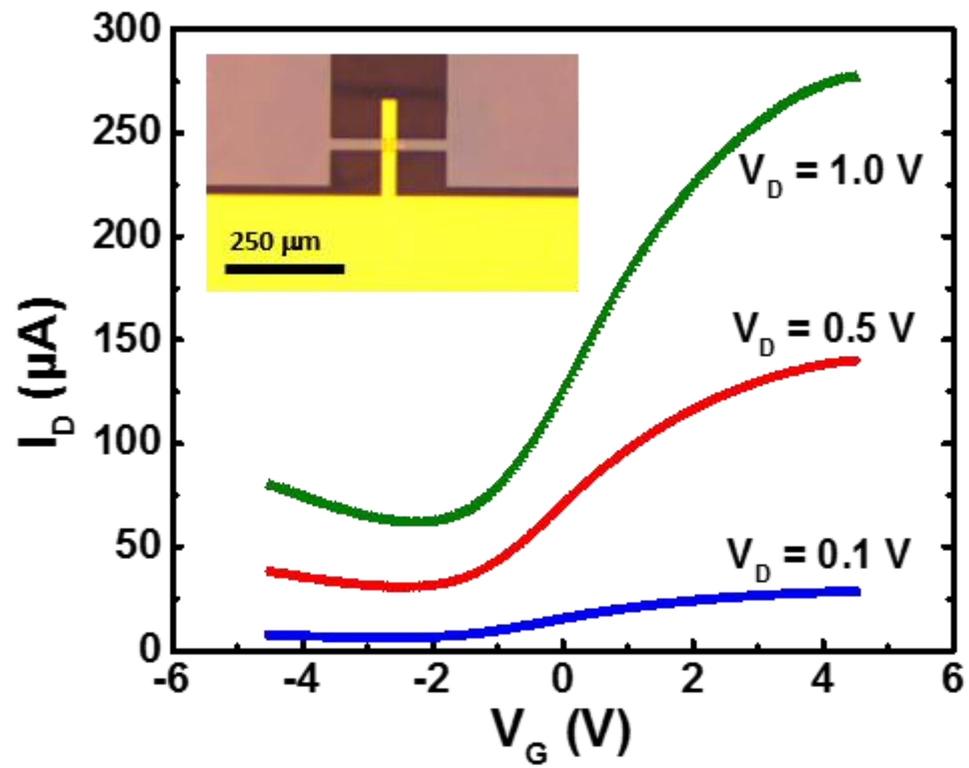


Figure 4.7: The electrical properties of a fabricated EG FET. The EG grown on semi-insulating 6H-SiC (0001) substrate is used as a channel of FET [11].

### 4.1.3 Role of Mo-plate Capping for Improved Crystallinity of Grown EG

Raman spectrum and SEM results demonstrate that Mo-plate capping develops an advantageous environment for growing EG with improved crystalline EG at relatively low temperature. Although not quantitatively certified, the following two mechanisms are considered major contributors based on experimental results. Firstly, the thermal radiation released from the SiC surface during annealing is protected by reflection on Mo-plate surface facing SiC substrate due to metallicity of Mo as shown in Figure 4.1(b). This called *radiation mirroring* and it induces the heat accumulation on SiC surface. Therefore, the temperature on SiC surface covered with the Mo-plate is higher than that on SiC surface without Mo-plate, which provides sufficient thermal energy to grow high quality EG. In other words, the SiC surface exposed to UHV is heated in the temperature near 900 °C, but the temperature of SiC surface covered with Mo is considered to be much higher. Secondly, the sublimated Si atoms during annealing process are confined in narrow space between Mo-plate and SiC substrate, which increase the Si vapor density and reduce the sublimation rate of Si atoms [7, 67, 68, 100, 101]. Therefore, the growth rate of EG is reduced, and EG of high quality and uniform thickness is formed on the SiC surface. However, as mentioned in Çelebi *et al* [68], the sublimated Si atoms have to be escape for the progress of EG formation. Otherwise, the EG growth rate will be stop because of the equilibrium of zero net sublimation of Si atoms. Unlike studies of other groups, the Mo-plate covers the whole surface of SiC substrate without passage for escape of Si atoms. However, the Mo-plate serves as a sink for draining Si atoms by absorbing Si atoms as shown in Figure 4.1(b). This result is confirmed by X-ray Photoelectron Spectroscopy (XPS) analysis in which the Si 2p peak is measured from the surface to the inside of the Mo-plate used for capping. Figure 4.8(a) indicates the XPS spectra obtained from the surface of the Mo-plate used for capping compared to non-used Mo-plate. The Si 2p signals are only found in the Mo-plate used for capping, which are the signals for pure Si and silicate [102]. The silicate signals are generated by oxidation of the Si atoms on the Mo-plate surface due to air exposure. Figure 4.8(b) indicates the XPS measurement results inside the Mo-plate used for capping. The intensity of Si 2p is inversely proportional to the inner depth of the Mo-plate. From this, it is confirmed that sublimated Si atoms are absorbed and diffused in the Mo-plate, and this phenomenon facilitate a non-zero net sublimation.

### 4.1.4 Conclusion

In conclusion, the high quality EG are formed on 4H-, 6H SiC substrate by the capping SiC substrate *with* Mo-plate during thermal annealing process. The Mo-plate reflects the emitted radiation from SiC substrate, which induces the heat accumulation on SiC substrate. The Mo-plate also reduce the Si atoms vapor pressure by confinement of sublimated Si atoms in the narrow space between Mo-plate and SiC substrate. The nonzero gap net sublimation of Si atoms is implemented by absorption and diffusion into Mo-plate. These factors enable growth of high-quality EG at reduced temperature, which is

demonstrated by Raman spectra, SEM images, and electrical characterization.

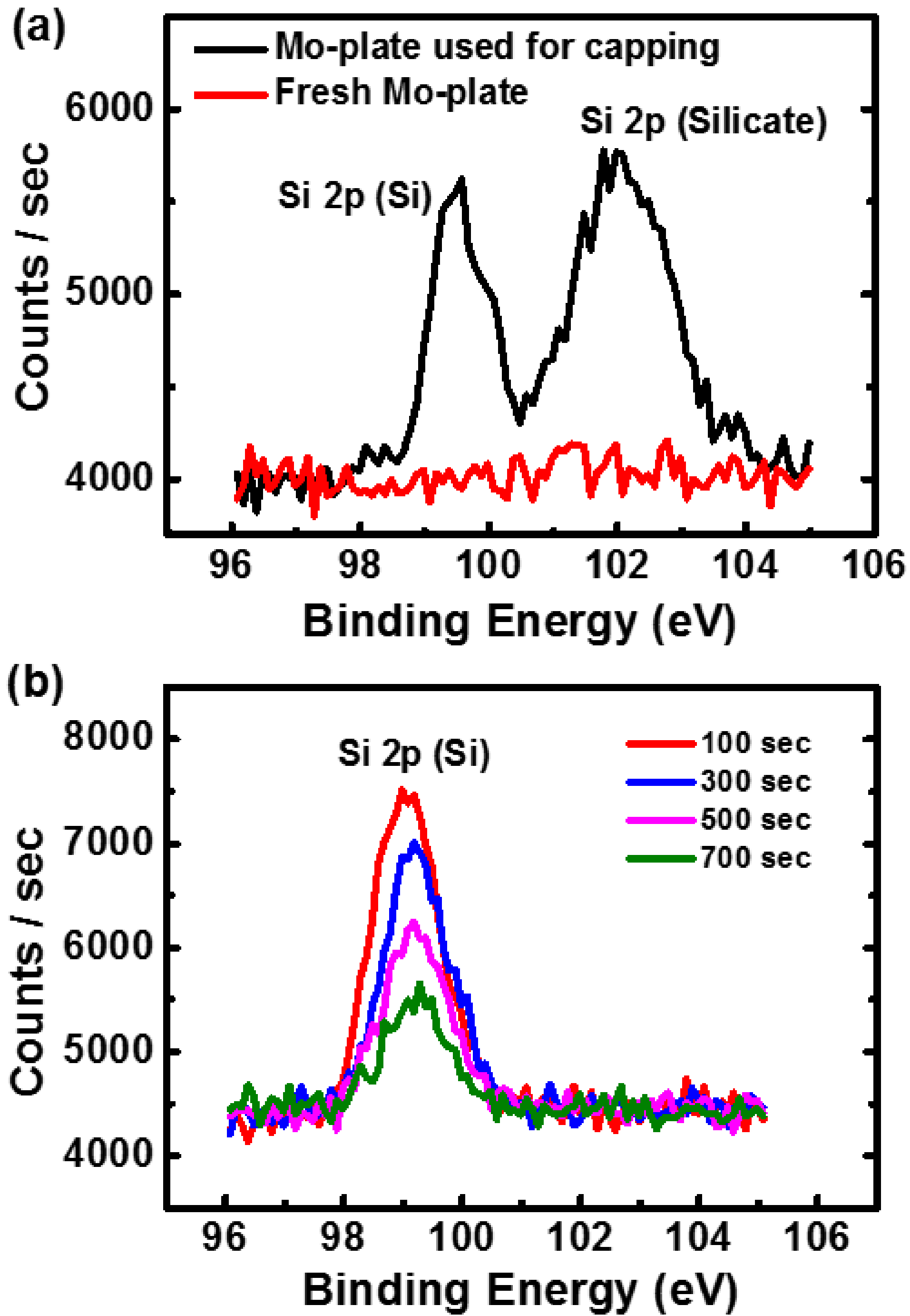


Figure 4.8: (a) XPS spectra of Si 2p signals measured on Mo-plate used for capping and a pure Mo-plate. (b) The Si 2p XPS spectrum measurement results during etching the Mo-plate used for capping from the surface to the bulk [11].

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### 4.2 Formation of EG on Amorphous SiC Film by Surface Confined Heating with Electron Beam Irradiation

The graphene film is formed on the amorphous SiC film by e-beam irradiation at a lower acceleration voltage of 1 kV, assisted by over-coating of the Ni thin film. The penetration depth of the e-beam irradiated at a low acceleration voltage is very shallow about a few nanometers. Therefore, the heat generated by multiple scattering of the irradiated e-beam is transmitted very efficiently near the surface of the SiC thin film. The thermalized electrons travel around the surface until they drain out of the SiC film. This phenomenon induces the weakness of bonding strength between Si and C atoms and decomposition of Si and C atoms can easily occur by thermal agitation. This weakened bond strength can trigger the sublimation of Si atoms at lower temperature than conventional annealing temperature [103-105]. Here, the Ni thin film help to form graphene by absorbing C atoms during e-beam irradiation and releasing the absorbed C atoms in cooling process [106, 107]. These effects allow a good quality graphene film to grow on amorphous SiC film at relatively low temperatures. The amorphous SiC thin film is formed by using Plasma-Enhanced Chemical Vapor Deposition (PECVD) is much cheaper than single crystalline SiC substrate, can be an efficient platform for cost-effective graphene growth.

#### 4.2.1 Sample Preparation for Graphene Growth on Amorphous SiC Film by using E-beam Irradiation

The c-plane sapphire substrate is prepared by cleaning with acetone and methanol before deposition of the SiC film. An amorphous SiC thin film (20 nm) is deposited on c-plane sapphire substrate at 350 °C by PECVD. The precursors of Si and C are $SiH_4$ (5 % diluted with He) and $CH_4$ gases, and their flow rates are 1,600 sccm and 500 sccm, respectively. The working pressure of PECVD chamber is ~800 mTorr and the RF power is 150 W at the frequency of 13.56 MHz. The composition and atomic binding information of deposited SiC thin film is obtained by XPS analysis (ESCALAB 250XI, Thermo Fisher Scientific) using the monochromatic Al-Kα radiation. The SiC film consists of Si, C, and O atoms in a composition ratio of 54.7 %, 26.2 %, and 19.1 %. Si atoms are about twice as many as C atoms, and O atoms are detected by the formation of native oxide on the SiC film surface. The XPS spectra at the C 1s and Si 2p of deposited SiC film is closely measured (Figure 4.9). The XPS spectra of C 1s is observed in two parts of Si-C (282.4 eV) and C-C (284.1 eV) bindings as shown in Figure 4.9(a). For the XPS spectra of Si 2p, the Si-C (101.4 eV) and Si-Si (98.8 eV) bindings are measured (Figure 4.9(b)). From this, we demonstrated that a real SiC film is formed. After completed amorphous SiC film process, the Ni thin film (7 nm) is also deposited on the amorphous SiC film using DC magnetron sputtering.

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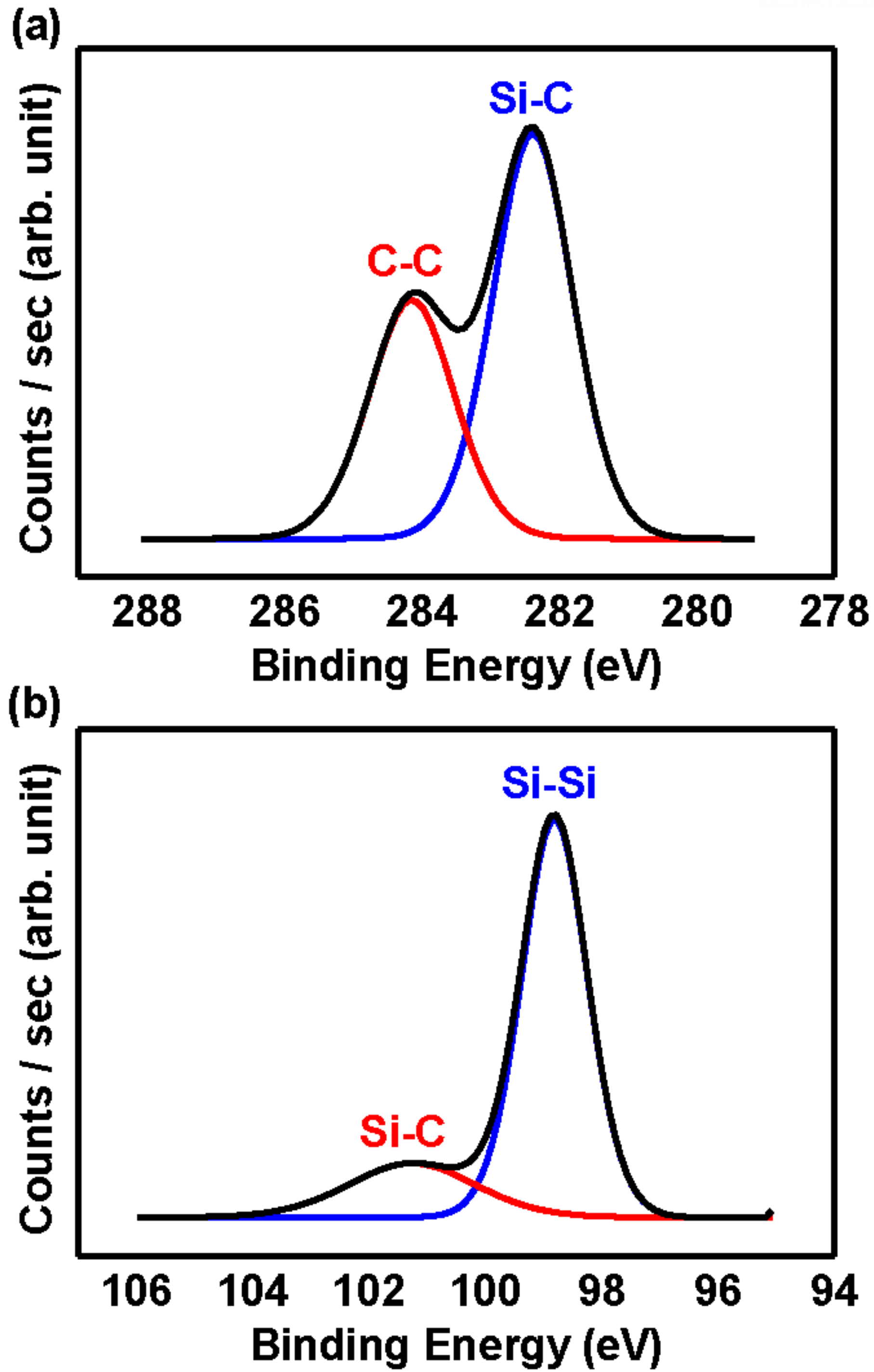


Figure 4.9: The High-resolution XPS data of (a) C 1s and (b) Si 2p for the amorphous SiC film deposited by PECVD [*in preparation*].

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### 4.2.2 Formation of EG Film on Amorphous SiC Film according to Electron Beam Irradiation Fluency and its Structural and Electrical Characteristics

After the SiC and Ni thin films deposition, e-beam with 1 kV acceleration voltage is irradiated at UHV for 10 mins. The three different emission currents (electron fluency) of 5 mA ($0.14 \times 10^{19}$ e/cm$^2$), 20 mA ($0.56 \times 10^{19}$ e/cm$^2$), and 50 mA ($1.4 \times 10^{19}$ e/cm$^2$) are used. Sample temperatures corresponding to emission current are ~700 °C, ~800 °C, and ~900 °C, respectively. The electron fluency is calculated as the number of electrons irradiated per unit area. The sample temperatures during annealing are measured by using a thermocouple and a pyrometer simultaneously. The top Ni film was removed with $FeCl_3$ etchant before analyzing characteristics of the formed graphene.

The structural quality of graphene formed on amorphous SiC films by electron beam irradiation is analyzed by Raman spectrum (Alpha 300R, WITec) in which the laser excitation energy is 2.33 eV (532 nm) and the laser spot size is 1.2 mm at laser power of 3 mW. Figure 4.10 indicates the Raman spectra of e-beam irradiated samples at three different e-beam fluencies. The Raman spectrum of heated sample by conventional thermal annealing at 900 ° C for 10 mins in UHV is also included to demonstrate the e-beam effect. E-beam irradiated SiC samples show typical Raman peaks of graphene at D (~1350 cm$^{-1}$), G (1580–1590 cm$^{-1}$) and 2D peaks (2650–2750 cm$^{-1}$). The measured all Raman spectra are normalized based on the G peak intensity. At low electron fluency ($0.14 \times 10^{19}$ e/cm$^2$), D and G peaks are not clearly separated and 2D peak does not exist. It means that the thermal energy is insufficient for growth of graphene on SiC film due to low electron fluency. The temperature of sample measured at electron fluency of $0.14 \times 10^{19}$ e/cm$^2$ is ~700 °C. For the electron fluency (temperature) of $0.56 \times 10^{19}$ e/cm$^2$ (800 °C), the 2D peak is detected. The intensity of D peak is about twice that of G peak, and 2D peak intensity is found to about 0.1 of the G peak intensity. The large D-peak means that the grown graphene is still defective and its consist of small grains [87, 98, 108]. As the electron fluency increases to $1.4 \times 10^{19}$ e/cm$^2$, the temperature of sample rises to ~900 °C. The measured Raman spectra is confirmed that the 2D peak intensity is 1.2 times higher than G peak intensity, and D peak intensity is almost same to G peak intensity. These results show that the quality of the grown graphene improves with increasing electronic fluency. For comparison, another sample is heated at 900 °C by conventional thermal heating method. At this time, the heating environment is the same to the case of e-beam fluency of $1.4 \times 10^{19}$ e/cm$^2$ except for the heating method. The properties of graphene formed by the conventional annealing is much worse than e-beam irradiated sample even though it is formed at the same temperature of 900 °C. The Raman spectrum of the sample formed by the conventional annealing is almost the same as the Raman spectrum of the graphene grown by e-beam irradiation with an electron fluency (temperature) of $0.14 \times 10^{19}$ e/cm$^2$ (~700 °C). From this, we confirmed that e-beam irradiated sample forms graphene with better properties than the conventional vacuum annealed sample at the same temperature. This means that the e-beam irradiation has other positive effects as well as surface heating for growth of the graphene.

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Figure 4.11 shows the proposed mechanism for graphene growth by e-beam irradiation. When electrons with an accelerating voltage of 1 kV are applied to the sample surface, the kinetic energy of electrons is directly delivered to within few atomic layers of SiC film surface by multiple collisions (thermalization) with Si and C atoms (Figure 4.11(a)) [103-105]. The penetration depth of e-beam with low accelerating voltage is only a few nanometers. Therefore, only few layers near the surface of SiC film is selectively heated by continuous e-beam irradiation. The thermalized electrons with losing kinetic energy move to the edge of the conduction band of SiC film. In the insulating SiC film and the sapphire substrate, the thermalized electrons are not rapidly drained out and are accumulated in the area near the surface of the SiC film. These electrons weaken the bonding strength between Si and C atoms due to their repulsion with the bonding electrons (Figure 4.11(b)). The weakened Si-C bonds reduce the thermal energy required for the sublimation of Si atoms, allowing graphene formation at relatively low temperatures. It is believed that the heat accumulation and weakened Si-C bond strengths induced by the irradiated electrons enable graphene growth on amorphous SiC films at lower temperatures than conventional vacuum annealing. We can confirm the stacking structure of graphene layers through the 2D peak shape. For the sample with the electron irradiation fluency of $1.4 \times 10^{19}$ e/cm$^2$, the 2D peak is fitted well to single Lorentzian and has a FWHM of ~52 cm$^{-1}$. It is broader than typical value (~24 cm$^{-1}$) of single layer graphene. It means that the stacking of the grown graphene has a turbostratic structure that randomly rotates about the adjacent layer [62].

Figure 4.12 indicates morphology of SiC film surface after e-beam irradiation using a Cold Field Emission Secondary Electron Microscopy (FE-SEM, Hitach High-Technologies S-4800). As the electron beam flow rate increased, the size of the graphene flake became larger and covered most of the surface of the SiC film. The graphene pieces of nm size at e-beam fluency of $0.14 \times 10^{19}$ e/cm$^2$ is increased to more than 500 nm at e-beam fluency of $1.4 \times 10^{19}$ e/cm$^2$.

The electrical properties of grown graphene by e-beam fluency of $1.4 \times 10^{19}$ e/cm$^2$ is confirmed by Hall effect measurements at room temperature with Van der Pauw structures. The charge carrier type is n-type (electron) and its carrier density is found to be $1.0 \times 10^{15}$ cm$^{-2}$. The measured sheet resistance is ~70 Ω/sq. It is believed that the high carrier density and the low sheet resistance are due to the formation of several graphene layers. The Hall mobility is measured to be ~92 cm$^2$/Vs, which is significantly lower than conventional graphene. It is considered to be due to strong carrier scattering in polycrystalline graphene boundaries and defects. Further works is essential for improving graphene quality. We should optimize the thickness of SiC thin film and the e-beam irradiation conditions. However, since the sheet resistance is very low, it is expected to be used as a transparent electrode for replacing ITO.

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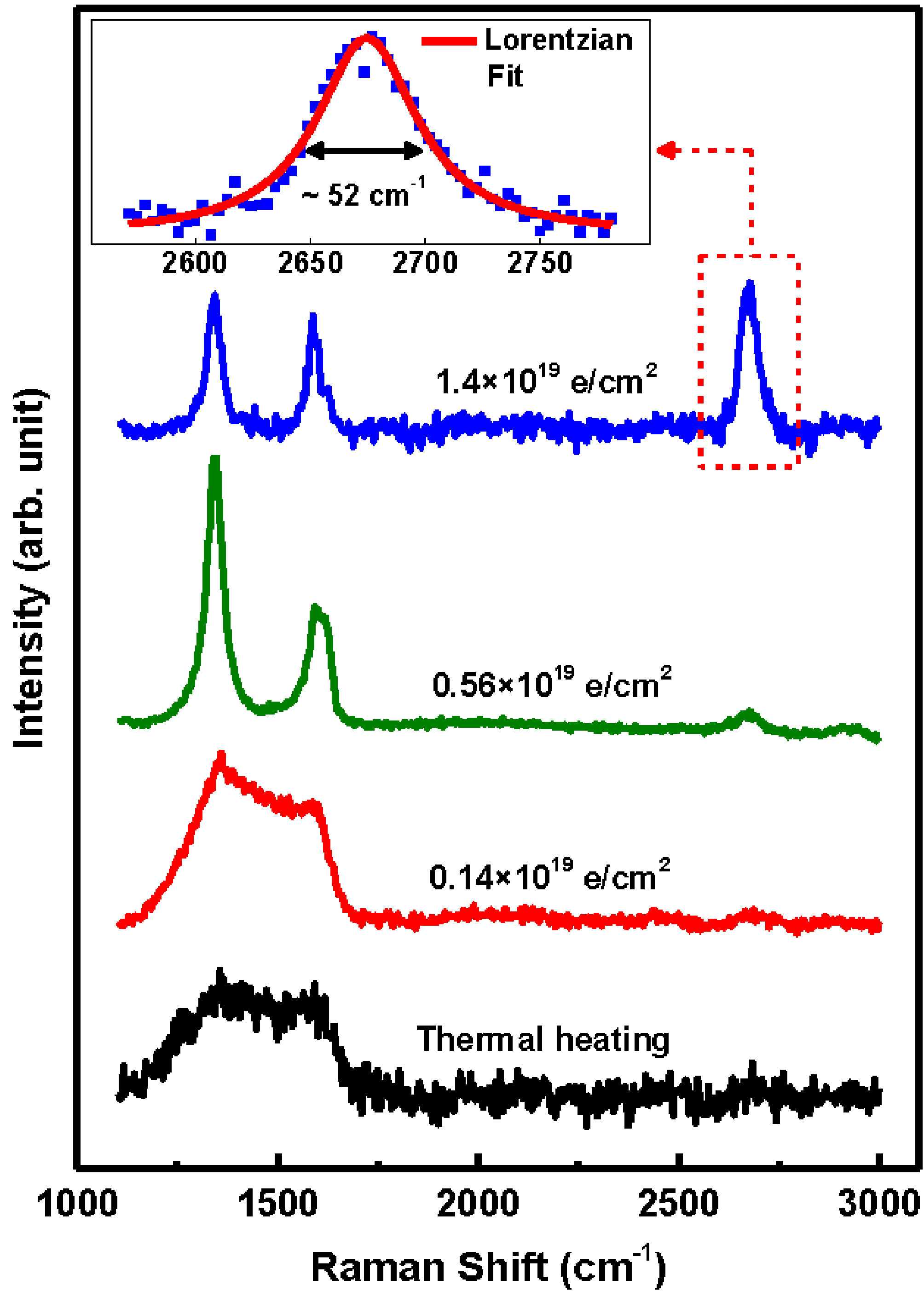


Figure 4.10: The Raman spectra of grown graphene on amorphous SiC thin film by e-beam irradiation and conventional vacuum annealing. [*in preparation*]

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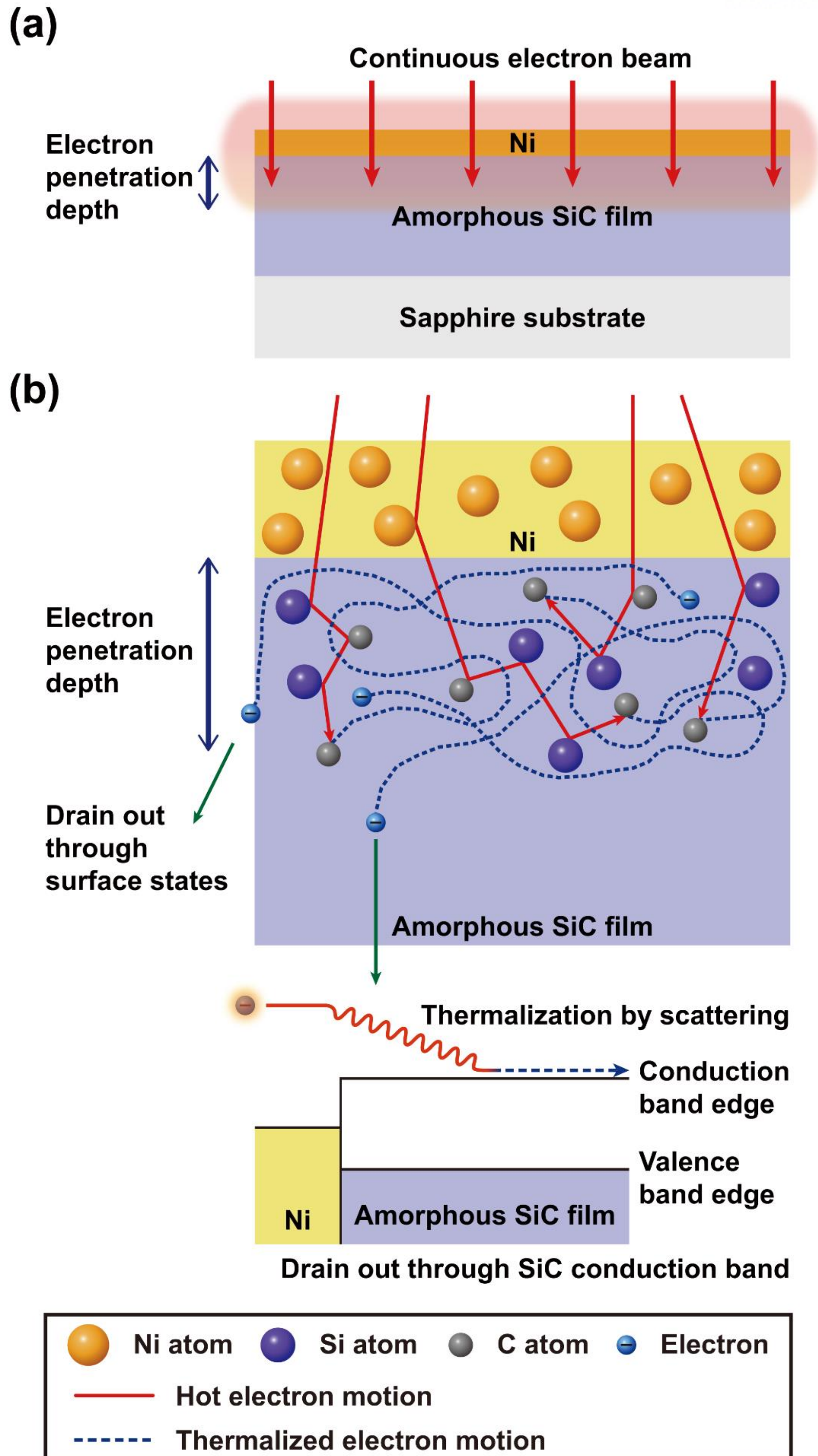


Figure 4.11: Schematic illustrations of the mechanism of graphene grown by e-beam irradiation. (a) The selective heating of SiC thin film surface. (b) Behavior of thermalized electrons within few layers of SiC thin film surface. [*in preparation*]

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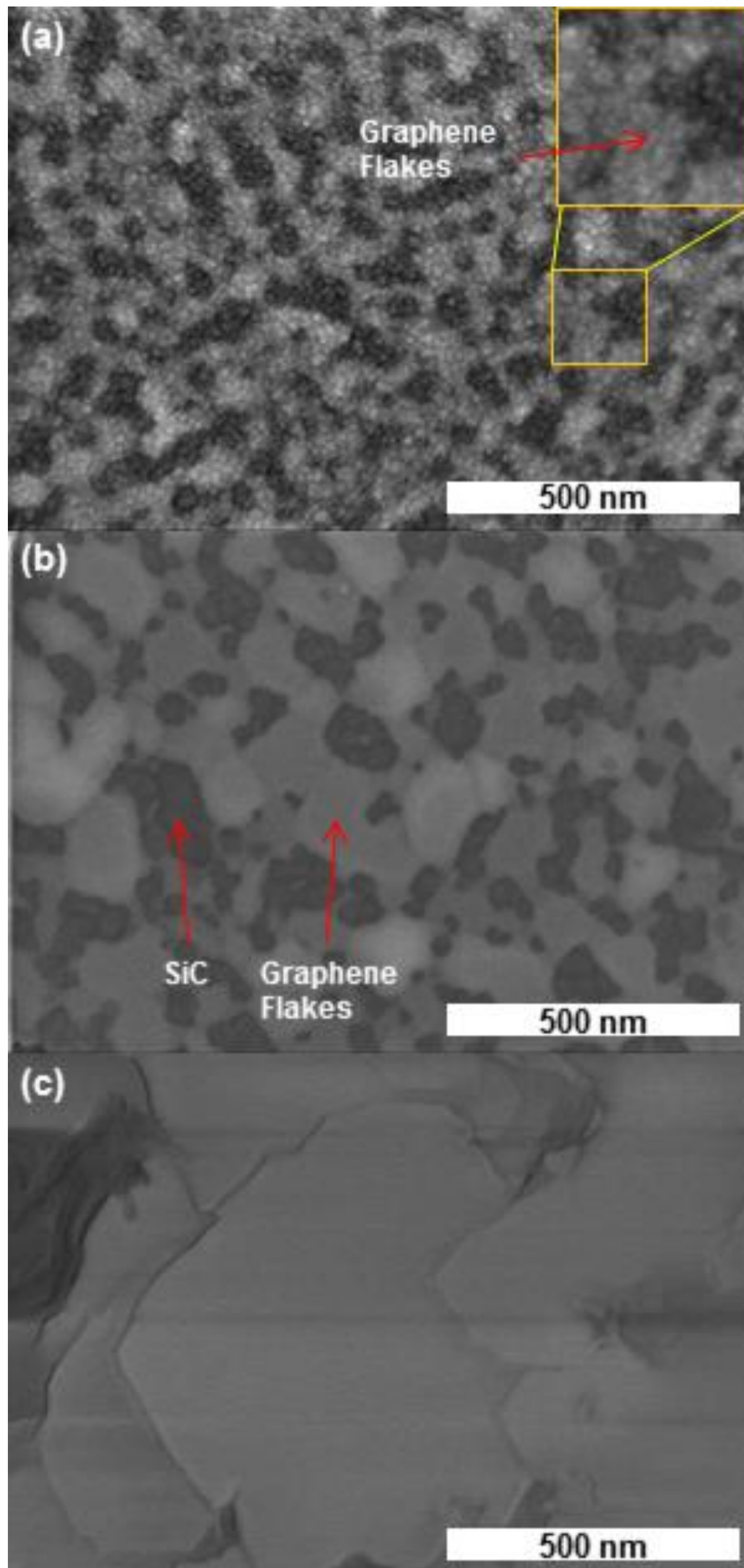


Figure 4.12: SEM images of SiC thin film surface after e-beam irradiation at different electron fluencies of (a) $0.14 \times 10^{19}$ e/cm$^2$, (b) $0.56 \times 10^{19}$ e/cm$^2$, and (c) $1.4 \times 10^{19}$ e/cm$^2$. [*in preparation*]

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### 4.2.3 Growth of EG on 4H-SiC (0001) by low voltage e-beam irradiation and its Structural Characteristics

The EG is grown on single crystalline Si-face 4H-SiC (0001) by e-beam irradiation. Before SiC samples loading to UHV chamber, the SiC substrates are cleaned with acetone and methanol for 10 min, and the native oxide is removed by HF (49 %) for 1 min. Experiment is conducted using the same e-beam irradiation equipment as used in the above thin film experiments. The acceleration voltage of the e-beam is fixed at 2.3 kV, and each sample is irradiated for 10 min at a current of 10 mA, 20 mA, and 30 mA. At this time, each electron fluency (temperature) is $1.4 \times 10^{19}$ e/cm$^2$ (950 °C) for 10 mA, $2.8 \times 10^{19}$ e/cm$^2$ (1000 °C) for 20 mA, and $4.2 \times 10^{19}$ e/cm$^2$ (1030 °C) for 30 mA. The temperature is measured by pyrometer and thermocouple.

The structural properties of EG grown on 4H-SiC by e-beam irradiation is analyzed by Raman spectra (Figure 4.13). As increase the electron fluency, the 2D peak intensity becomes larger and D peak intensity is reduced. In other words, a higher quality EG is formed as the electron fluency increases. For the electron fluency of $4.2 \times 10^{19}$ e/cm$^2$, the intensity ratio of 2D peak to G peak is ~0.6 and D peak intensity is ~0.15 of the G peak intensity. Considering the broad FWHM of ~75 cm$^{-1}$ and asymmetric shape of the 2D peak, it is believed that few layers graphene is formed on 4H-SiC (0001) [87]. It is considered that EG is formed at relatively low temperature by the e-beam irradiation with the same mechanism as illustrated in Figure 4.11. Further studies should be conducted to analysis electrical properties and improve the EG qualities. The electrical properties will be measured by the Hall effect, and the optimal conditions for EG growth will be found by adjusting the acceleration voltage and electron beam amount.

### 4.2.4 Conclusion

In conclusion, we confirmed that graphene can be formed on an amorphous SiC film and single crystalline SiC substrate by e-beam irradiation at low accelerating voltage. The structural properties of grown graphene were investigated by Raman spectroscopy and SEM images. The e-beam irradiation has two positive effects on graphene formation. First, the penetration depth of e-beam is shallow due to the low acceleration voltage, which cause selective heating only on the few layer of SiC thin film surface. Second, the thermalized electrons falling into the edge of the conduction band of the SiC film wander around the region near the surface of the SiC film. These electrons weaken the bonding strength between Si and C atoms due to their repulsion with the bonding electrons, allowing graphene formation at relatively low temperatures.

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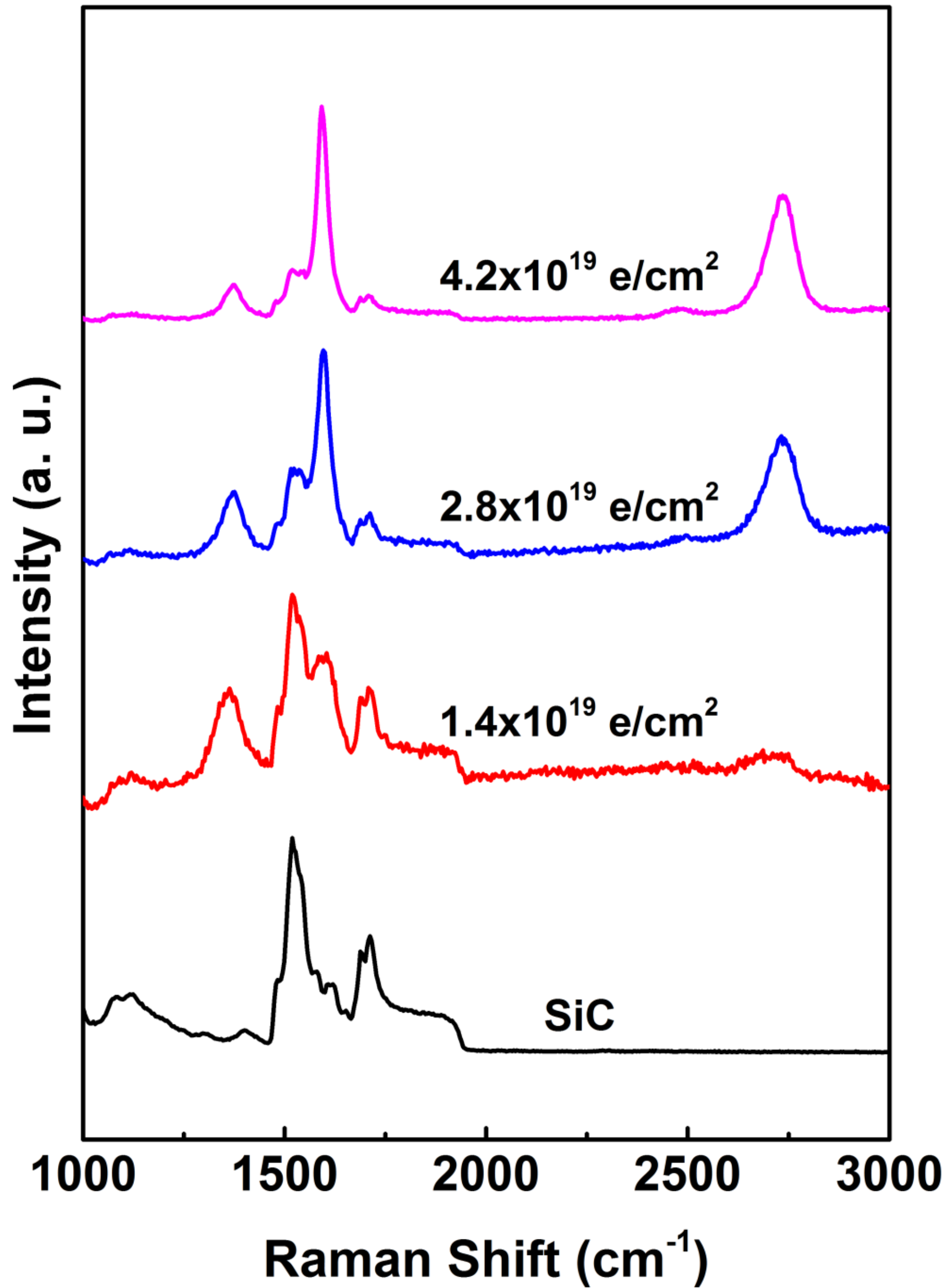


Figure 4.13: The Raman spectra of grown EG on 4H-SiC (0001) thin film by e-beam irradiation, and Raman spectra of bare 4H-SiC.

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### 4.3 Minimized Impurity Scattering in Carrier Transport of EG on 6H-SiC with Non-lithographic Patterning

Patterning processes using polymers film such as electron beam lithography or photolithography are essential for fabricating graphene devices. However, polymer residues cannot be completely removed after patterning, leading to contamination and degradation of graphene [12, 13, 15-17, 109]. Since graphene is a single layer material and its electrical properties are sensitive to surface conditions, polymer residues are an important issue for device fabrication. Various studies such as annealing [15, 16], chemistry [17] and AFM [13] cleaning have been carried out to solve this problem, but there are still limitations. The high temperature annealing method can partially remove polymer residues, but the graphene layer can be damaged due to the high temperature annealing. It has also been reported to eliminate the residue of the graphene surface without chemical reaction using the mechanical force of the AFM tip. This method substantially improves the height roughness ($R_{rms}$) of graphene surface and the enhance the mobility. However, there is a limit to the use of large areas of graphene due to its slow cleaning rate. Therefore, it is necessary to develop fabrication process capable of patterning the graphene without degrading the electrical characteristics of the graphene due to the polymer residue. Here, we propose a polymer free patterning method using an Al thin film as an etch mask to avoid impurity scattering on EG surface due to polymer residue. The etching mask (Al thin film) and the contact pad (Ti / Au) were formed using a shadow mask and an e-beam evaporator. The polymer is not used during the all process.

Here, we propose a polymer free patterning method using an Al thin film as an etch mask to avoid impurity scattering on EG surface due to polymer residue. The etching mask (Al thin film) and the contact pad (Ti / Au) were formed using a shadow mask and an e-beam evaporator. The polymer is not used during the all process. The properties of EG Hall bar device using Al thin film were investigated by Hall measurement and Raman spectra, compared with fabricated sample using conventional photolithography. The carrier density and Hall mobility of EG device patterned using Al thin film etch mask are confirmed as $9.16 \times 10^{12}$ cm$^{-2}$ and ~ 2100 cm$^2$/Vs, respectively. The clean 2DEG system and good homogeneity of this sample are also evidenced by apparent SdH oscillations. In contrast, the EG device patterned by photolithography exhibits the SdH oscillation containing a lot of noise, which is considered to be due to scattering from the polymer residues.

#### 4.3.1 Fabrication of EG Hall bar Devices by using Al Thin Film or Photolithography as an Etch Mask

In order to prove the excellence of our proposed way, samples are fabricated by two different patterning methods. The EGs are prepared on 6H-SiC substrate at substantially reduced temperature using Mo-plate capping method [11]. The 1×1 cm$^2$ diced Si-face SiC substrate covered with Mo-plate was annealed at 950 °C for 10 min in UHV. The 6H-SiC wafer is semi-insulating with orientation is

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<0001>, the double faces are polished and especially Si face was prepared in an epi-ready with surface roughness of less than 0.5 nm. One of the EG samples is made of Hall bar device (120 μm × 35 μm) by using Al thin film as an etch mask without leaving any polymer residue, and the other EG sample is patterned to form Hall bar device (10 μm × 4 μm) by conventional photolithography method using AZ 5214E photoresist (Figure 4.14). Figure 4.15 describes the fabrication process of EG Hall bar devices on semi-insulating 6H-SiC (0001) substrate. The Al thin film of 30 nm thickness is deposited on the EG surface in the form of Hall bar using shadow mask (Figure 4.15(a)). The photoresist etch mask is also formed by conventional photolithography (Figure 4.15(e)). The EG not covered with photoresist or Al thin film is etched by reactive ion etching (RIE) at 50 W for 60 seconds in oxygen ambient circumstance (Figure 4.15(b) and (f)). After that, Al thin film mask is removed by Al etchant type D (TRANSENE) at 50 °C for 2 min (Figure 4.15(c)), and the photoresist is also eliminated by acetone and methanol, but polymer residue still remained on the EG surface (Figure 4.15(g)). The contact pads of Ti/Au (10 nm/50nm) are deposited by an e-beam evaporator, and patterned with shadow mask (Figure 4.15(d)) or photolithography (Figure 4.15(g)).

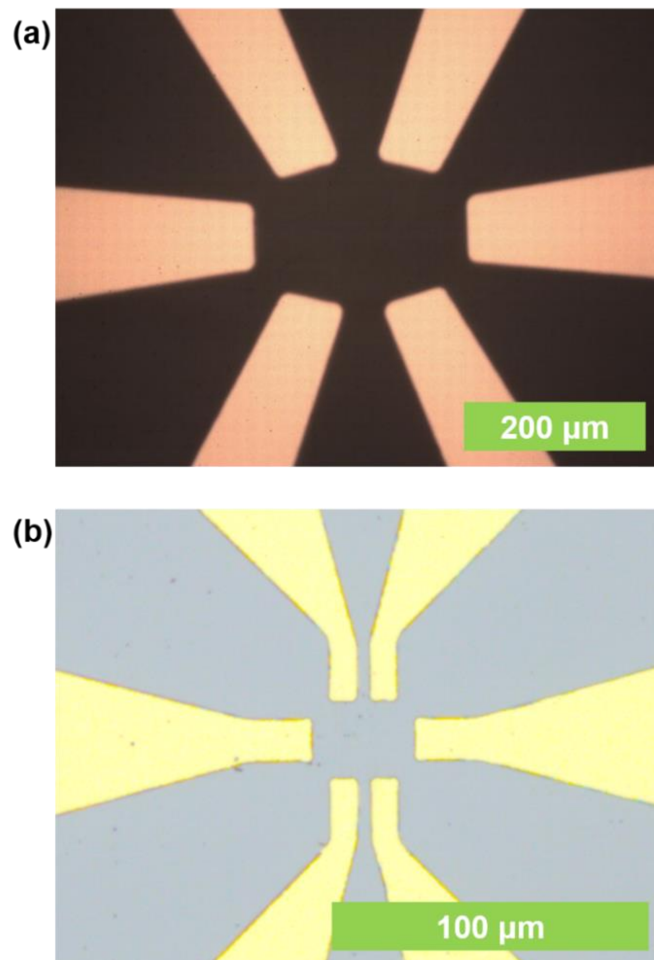


Figure 4.14: Photographs of Hall bar devices by fabricating (a) Al thin film (b) photolithography. [*in preparation*]

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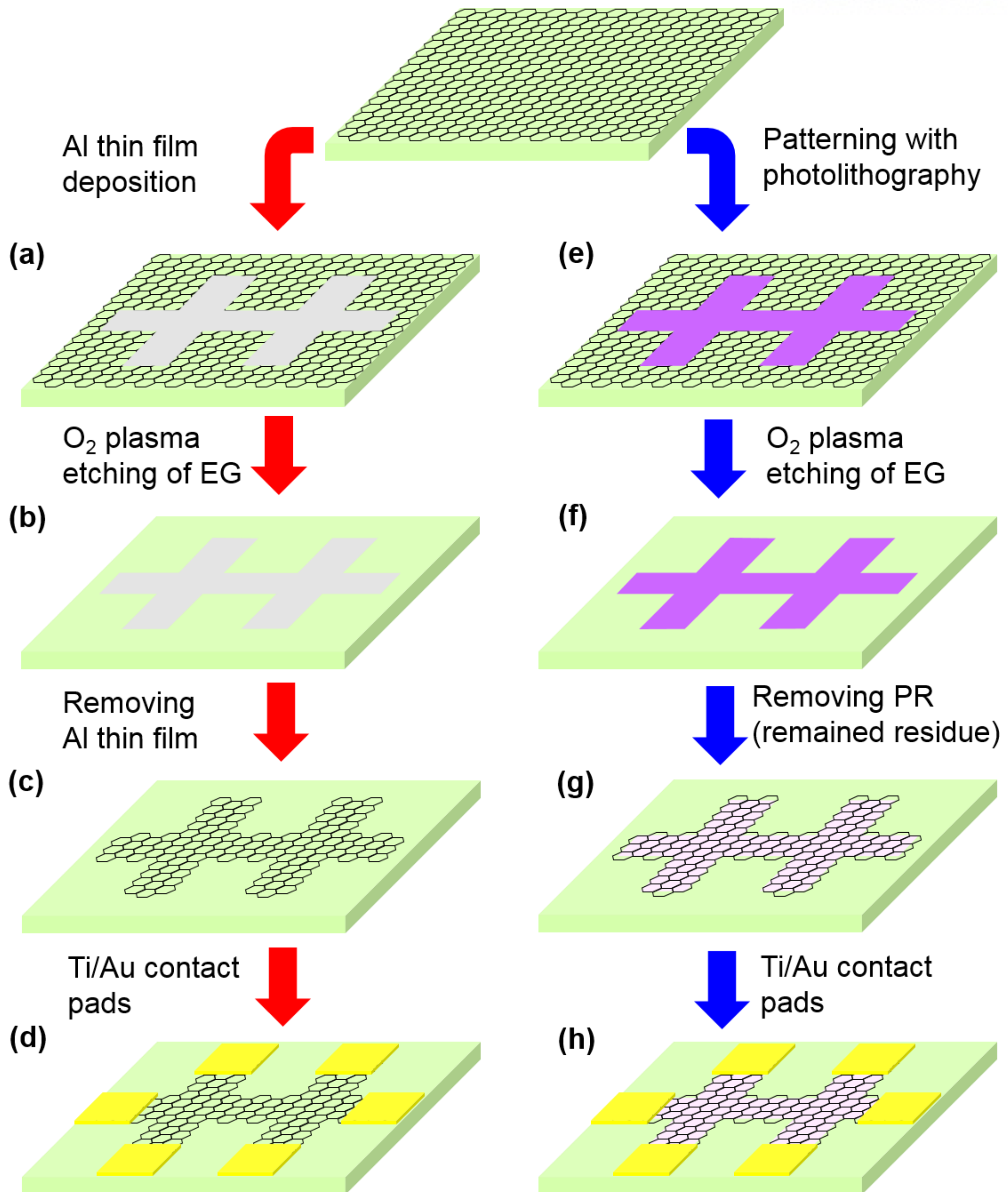


Figure 4.15: Schematic diagram of fabrication process for EG Hall bar device patterned by (a)-(d) Al thin film and (e)-(h) conventional photolithography. [*in preparation*]

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### 4.3.2 Transport Properties of EG Devices depending on Polymer Residue

Hall measurements are performed in PPMS system at high vacuum. The data is obtained by low frequency (17 Hz) lock-in technique as shown in Figure 4.16. Prior to cooling down for measurement, the sample is *in situ* heated in a vacuum chamber at 100 °C for 30 min to evaporate surface contaminants such as water and oxygen molecules. Figure 4.17 shows the results of magnetoresistance ( $R_{xx}$ ) and Hall resistance ( $R_{xy}$ ) on EG Hall bar samples patterned with photoresist (Figure 4.14(a) or Al thin film (Figure 4.14(b)) at 1.9 K and 0 T < magnetic field ( $B$ ) < 14 T. The sheet carrier density is obtained from the slope of $R_{xy}$ with change of $B$ in the classical Hall effect as following [110]

$$n_s = \frac{dB}{dR_{xy} \cdot q} \tag{4.4}$$

The Hall mobility ( $\mu_H$ ) is calculated as [110]

$$\mu_H = \frac{1}{\rho_s n_s q} = \frac{dV_H}{dB} \frac{L}{W} \frac{1}{R_{xx} I} \tag{4.5}$$

The filling factor ( $\nu$ ) in the SdH oscillations is given by [78, 111, 112]

$$\nu = \frac{hn_s}{eB} \tag{4.6}$$

Figure 4.17(a) shows Hall measurement results of EG patterned with photolithography. The carrier density and Hall mobility at 1.9 K are calculated to be 3.62 × $10^{12}$ $cm^{-2}$ and 2100 $cm^2$/Vs, respectively. The SdH oscillations with minimum value of $\nu = 14$ in the magnetic field of ~11 T is confirmed, but this SdH oscillations are not clear and contain a lot of noise signal. This result is considered that the residual polymers on EG surface serve as scattering sources when electrons of 2DEG move in the magnetic field. The $R_{xy}$ represents plateau-like shape when $R_{xx}$ is the minimum value in SdH oscillation in $B$ between 10 T and < 13 T. Figure 4.17(b) shows the Hall measurement results of EG device patterned with Al thin film. The carrier density of this sample is 9.16 × $10^{12}$ $cm^{-2}$, which value is ~2.5 times bigger than the sample patterned using photolithography. This difference in carrier density can be demonstrated by the residues present on the surface of the sample. Water and oxygen molecules are trapped between the photoresist residue and EG, which induce hole doping (electron reduction). It is believed that water and oxygen molecules were not removed during thermal annealing because photoresist residue has covered them up. The Hall mobility is measured as ~ 2100 $cm^2$/Vs, which is similar to the photoresist patterning sample despite having a high carrier density [113]. Unlike the device patterned using photolithography, SdH oscillations are clearly present without noise, which indicates that the EG channel without residue has better homogeneity and clean 2DEG system [18]. The minimum value of $\nu = 30$ is observed in SdH oscillations at ~12 T. It has a higher value of $\nu$ due to its high carrier density. From this Hall measurement result, it was confirmed that EG can be cleanly

fabricated without polymer residue by using Al thin film as an etching mask. This method makes it possible to prevent unintentional doping and deterioration of the device performance from the polymer residue.

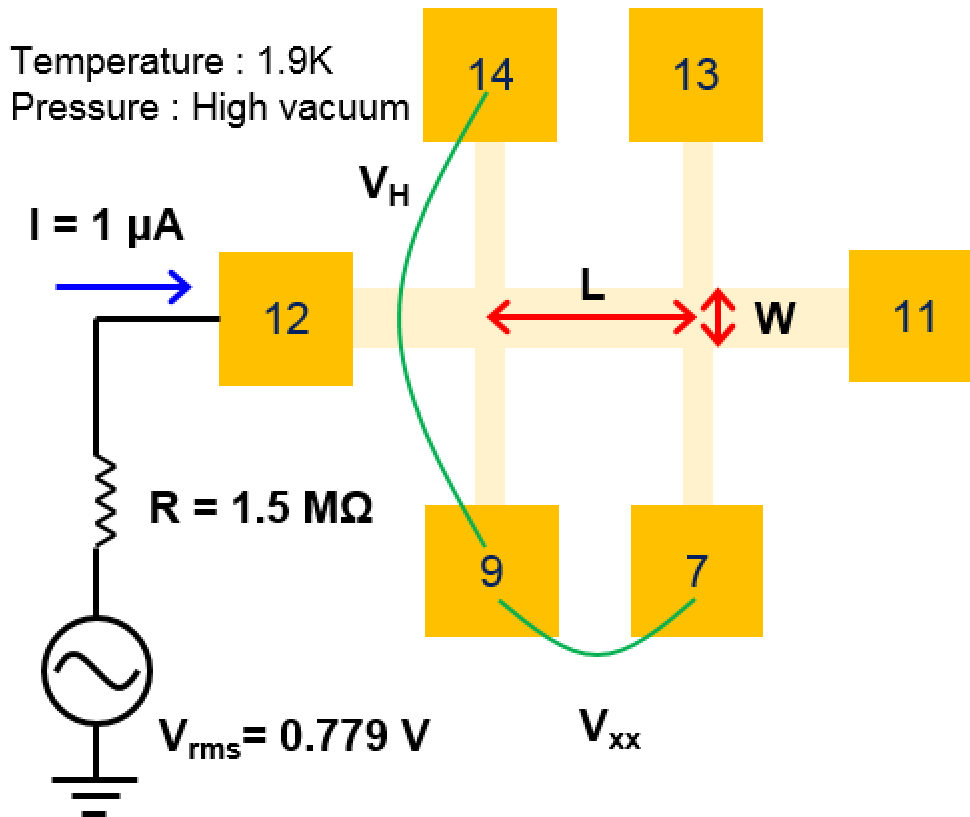


Figure 4.16: The setup of measurement system for Hall measurement at 1.9 K in high vacuum [*in preparation*].

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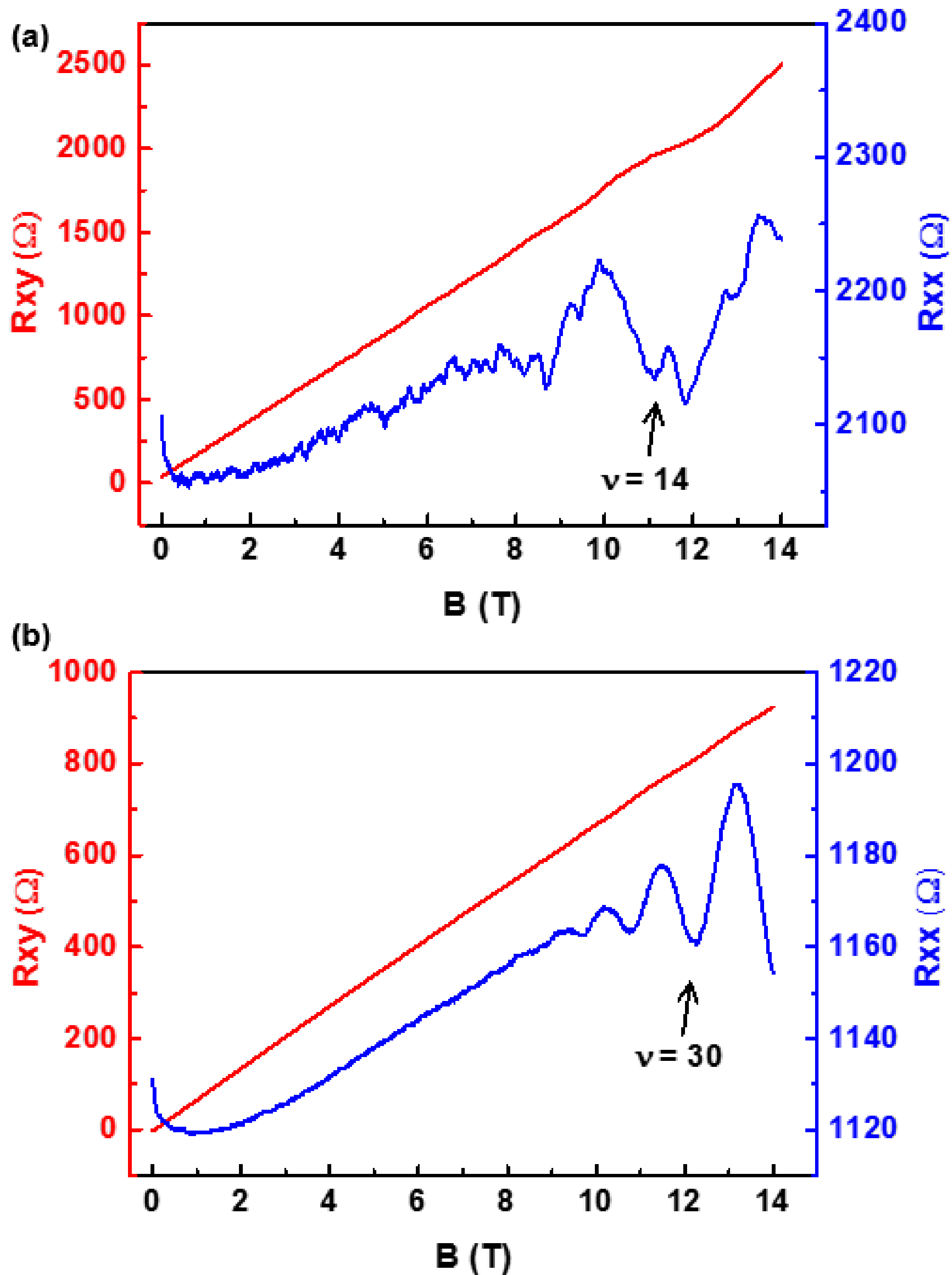


Figure 4.17: The measurement results at 1.9 K of magnetoresistance and Hall resistance for EG Hall bar devices patterned by using (a) photolithography and (b) Al thin film as an etching mask. [*in preparation*]

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### 4.3.3 Electron Effective Mass ($m^*$) and Quantum Lifetime ($\tau_q$) of EG

The electron effective mass ($m^*$) is calculated using the temperature dependence of the $R_{xx}$ oscillation peak. The amplitude of $R_{xx}$ is inversely proportional to temperature. The ratio between the amplitudes of SdH oscillations $A(T_1)$ and $A(T_2)$ at temperature $T_1$ and $T_2$ ($T_1 > T_2$) for the same magnetic field $B = B_n$ is following as [27, 28]

$$\frac{A(T_2)}{A(T_1)} = \frac{T_2}{T_1} \frac{\sinh\left(\frac{2\pi^2 k_B m^* T_1}{\hbar e B_n}\right)}{\sinh\left(\frac{2\pi^2 k_B m^* T_2}{\hbar e B_n}\right)}, \quad T_1 > T_2 \tag{4.7}$$

where $eB/m^* = \omega_c$ is the cyclotron frequency and $k_B$ is the Boltzmann constant. Equation (4.7) is a transcendental equation which can be simplified at $T_1 = T_2$ for obtaining $m^*$. The $m^*$ is obtained by [18, 114, 115]

$$m^* = \frac{e\hbar B_n}{2\pi^2 k_B T_2} \operatorname{arccosh} \frac{A(T_2, B_n)}{A(T_1, B_n)}, \quad \text{at } T_1 = 2T_2 \tag{4.8}$$

The $m^*$ of EG patterned with Al thin film is determined to be 0.0763 $m_o$. Figure 4.18 indicates the results of the normalized amplitude of oscillation peaks of EG patterned with Al thin film at the different temperatures. The magnetic field and current are fixed to 13.27 T and 1 μA, respectively.

The quantum lifetime ($\tau_q$) is obtained using the amplitude change of the SdH oscillation (i.e., the Dingle plot) according to the magnetic field at a constant temperature [115, 116]

$$\ln\left(\frac{A(T, B_n) \cdot B_n^{-1/2} \cdot \sinh(\chi)}{\chi}\right) = -\frac{\pi m^*}{e\tau_q} \frac{1}{B} + C \tag{4.9}$$

where $\chi = 2\pi^2 k_B T / (\hbar\omega_c)$ and $C$ is a constant.

Figure 4.19 indicates the results of Dingle plot for EG patterned with Al thin film where $\tau_q$ is extracted from the slope of graph using equation (4.9) and the obtained value of $m^*$. In the graph, the slope corresponds to the $-\pi m^*/e\tau_q$, and the $\tau_q$ is calculated to be 0.0165 ps.

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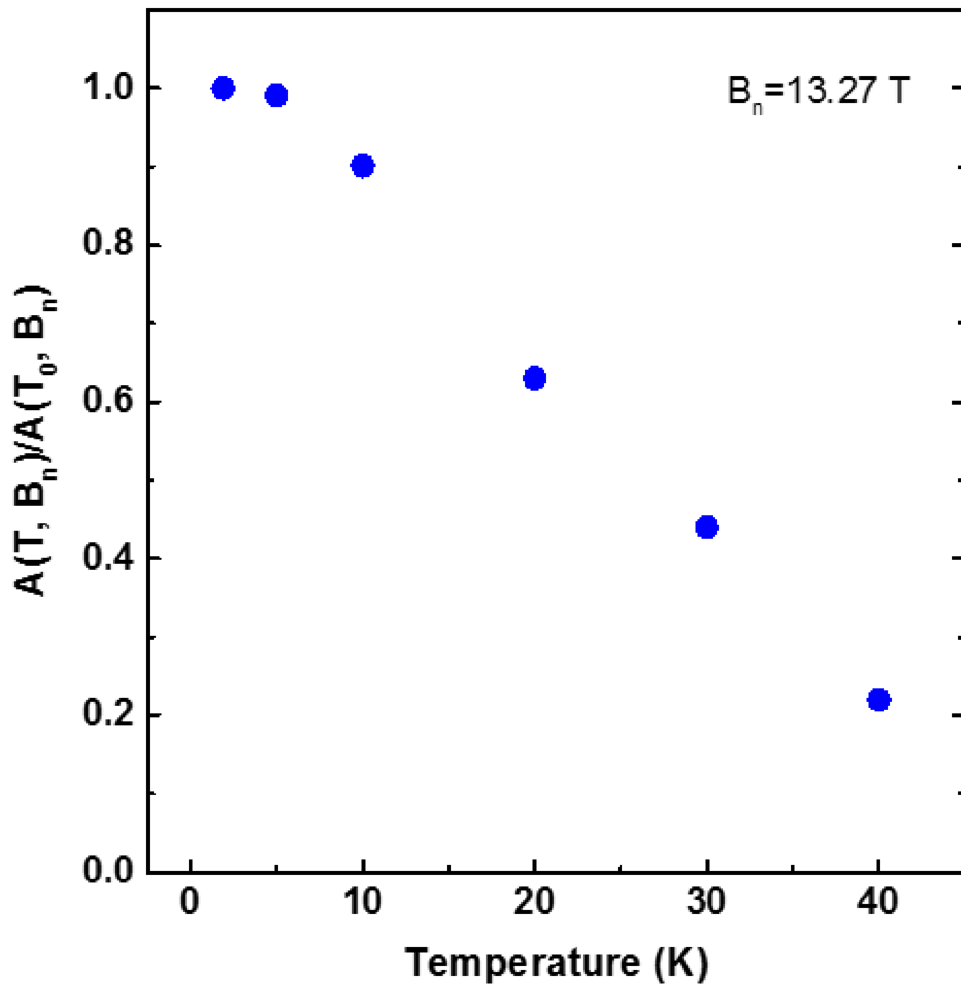


Figure 4.18: The normalized amplitude of the SdH oscillations peak for EG sample patterned with Al thin film according to the temperature at fixed magnetic field of 13.27 T. [*in preparation*]

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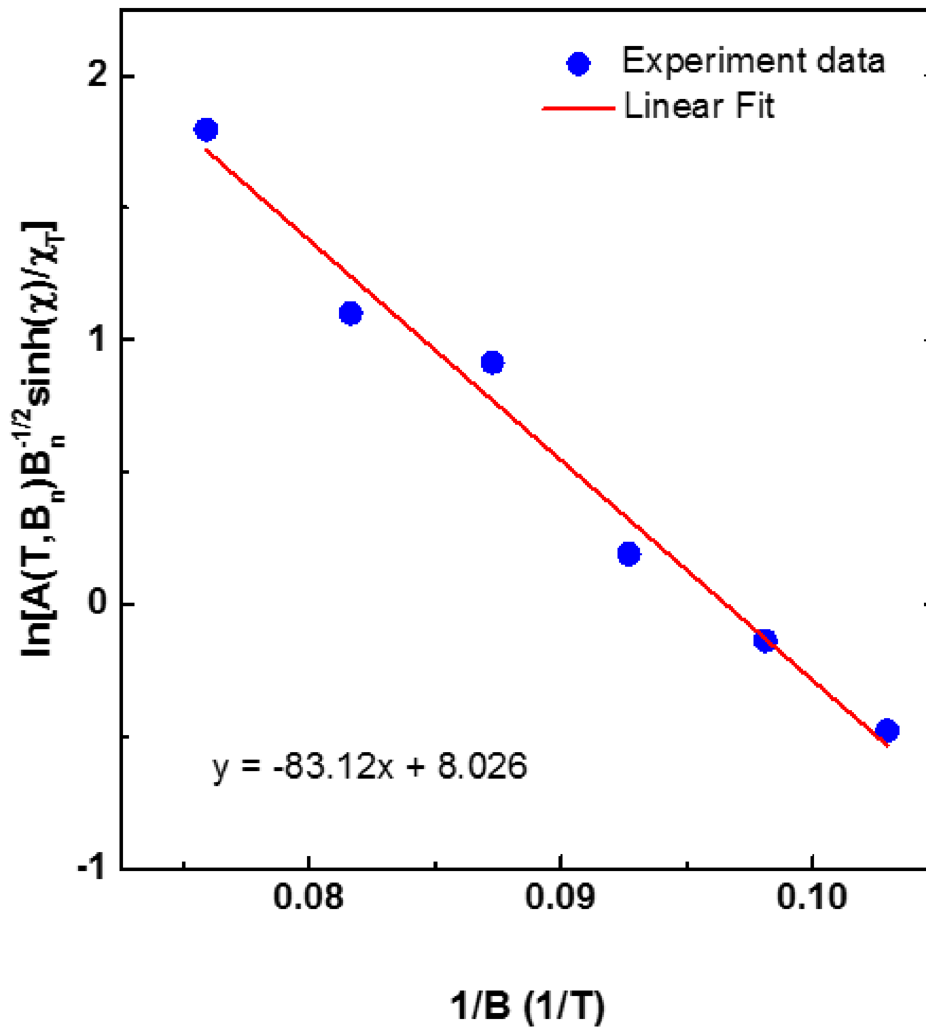


Figure 4.19: Dingle plot at 1.9 K for amplitude of the SdH oscillations. The slope of graph represents $-\pi m^* / e\tau_q$ where $\tau_q$ is the quantum transport time. [*in preparation*]

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**4.3.4 Raman Spectra Analyses**

Figure 4.20 indicates the Raman spectra of EG on 6H-SiC substrate before and after Hall bar fabrication process. Raman spectra were measured using a Raman microscope (Alpha 300R, WITec) with a laser excitation energy of 2.33 eV (532 nm), a laser power of 3 mW, and a laser spot size of 1.2 μm. Raman spectra are very sensitive to material properties such as number of layers, strain, defects, temperature and doping level, which is a very useful technique for nondestructive investigation of graphene properties [117-119]. The Raman spectra of graphene shows major peaks of D peak (~1350 $cm^{-1}$), G peak (~1580 $cm^{-1}$) and 2D peak (~2680 $cm^{-1}$). The thickness of graphene can be distinguished by FWHM of 2D peak and intensity ratio of 2D/G peak. The intensity of the D peak gives information about the degree of graphene defects [117, 118]. Since the Raman signals of the graphene and SiC substrate overlap, the signals of the SiC substrate are substracted from the measured Raman spectra to clarify changes. For the as-grown EG on 6H-SiC by Mo-plate capping (before patterning), the 2D peak is fairly symmetric and well fitted to a single Lorentzian with FWHM of ~ 35 $cm^{-1}$. The intensity ratio of 2D peak to G peak is ~ 4.5, and the intensity of D peak is almost zero. These results mean that the grown EG is a high-quality monolayer. The position and width of the G band varying with doping concentration are related to the Kohn anomaly and electron-phonon coupling [117]. As the doping concentration of holes or electrons increases, the frequency location of the G peak is upshifted and the width of the G peak is reduced. The location of the 2D peak depends on the type of doping. The 2D peak frequency position is upshifted with increasing electron doping, while is downshifted with the hole doping increase. The intensity ratio of 2D/G peaks decreases as hole or electron doping concentration increases [117, 118].

After pattering, the G peak position of EG is upshifted to 1591.5 $cm^{-1}$ for photoresist pattern and 1600.1 $cm^{-1}$ for Al thin film pattern compared to as-grown EG of 1586 $cm^{-1}$, and FWHM of G peak is reduced to 13.7 $cm^{-1}$ for photoresist pattern and 11.1 $cm^{-1}$ for Al thin film pattern compared with as grown EG of 28.7 $cm^{-1}$ (Figure 4.18(a) and (c)). Figure 4.18(b) and (d) also demonstrate that Raman spectra of 2D peak is dependent on the fabrication methods. After patterning with photolithography and Al thin film, the 2D peak position of the EG is upshifted from 2679 $cm^{-1}$ to 2682 $cm^{-1}$ and 2683 $cm^{-1}$, respectively. The intensity ratio of 2D/G peaks after pattern of photolithography and Al thin film is also reduced to 2.8 and 2.0, respectively. From these results, it is confirmed once again that the electron doping concentration of EG patterned with photolithography is lower than that of EG patterned with Al thim film. The main reason is believed that polymer residue induces hole doping by trapping water or oxygen molecules. The EG patterned by photolithography shows a broad background Raman peak, which signifies typical amorphous properties. It indicates that photoresist residue still remains on the EG surface.

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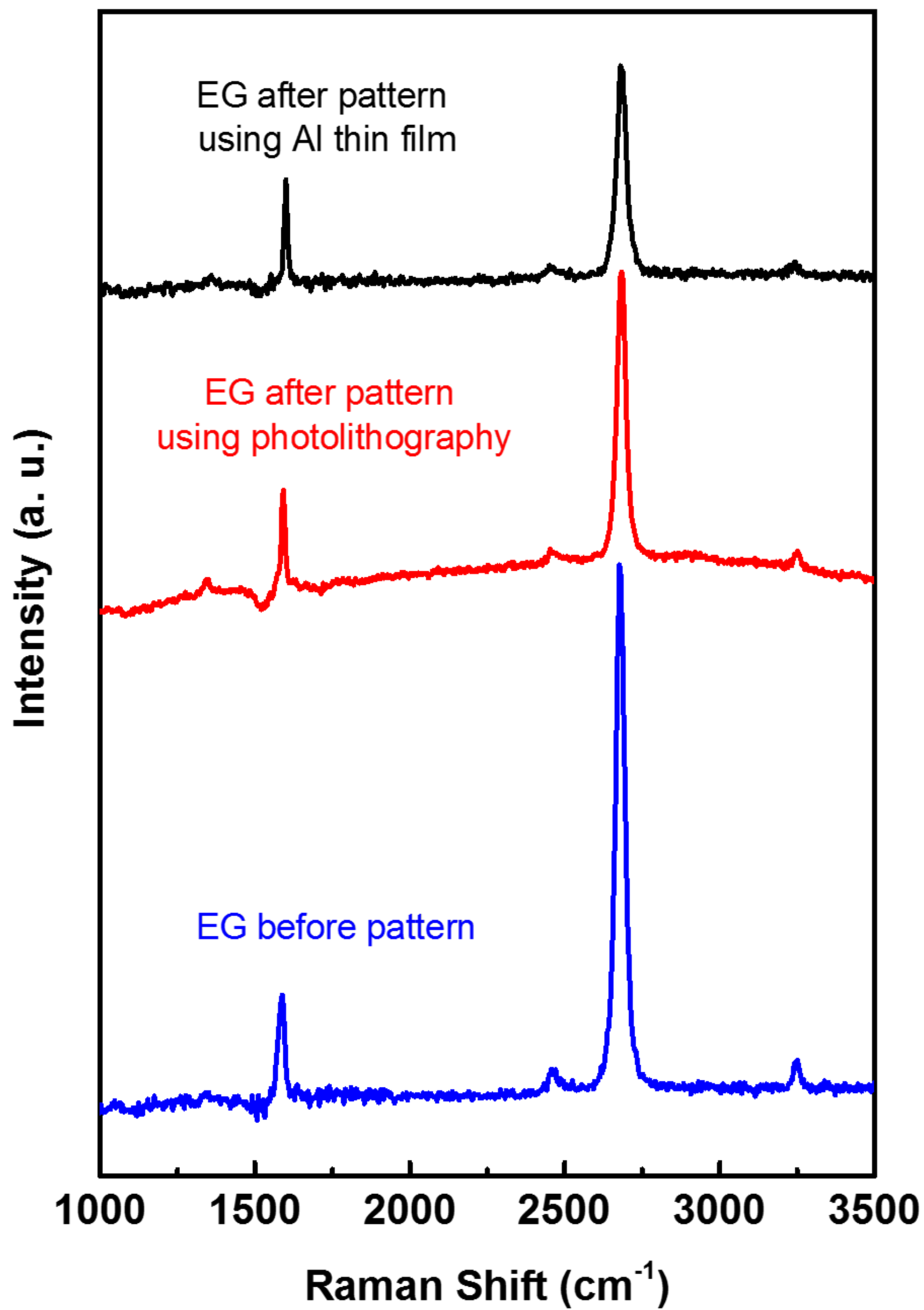


Figure 4.20: Raman spectra of as-grown EG (blue line) and patterned EG by photolithography (red line) and Al thin film (black line). Here, the Raman peaks of SiC is substracted. [*in preparation*]

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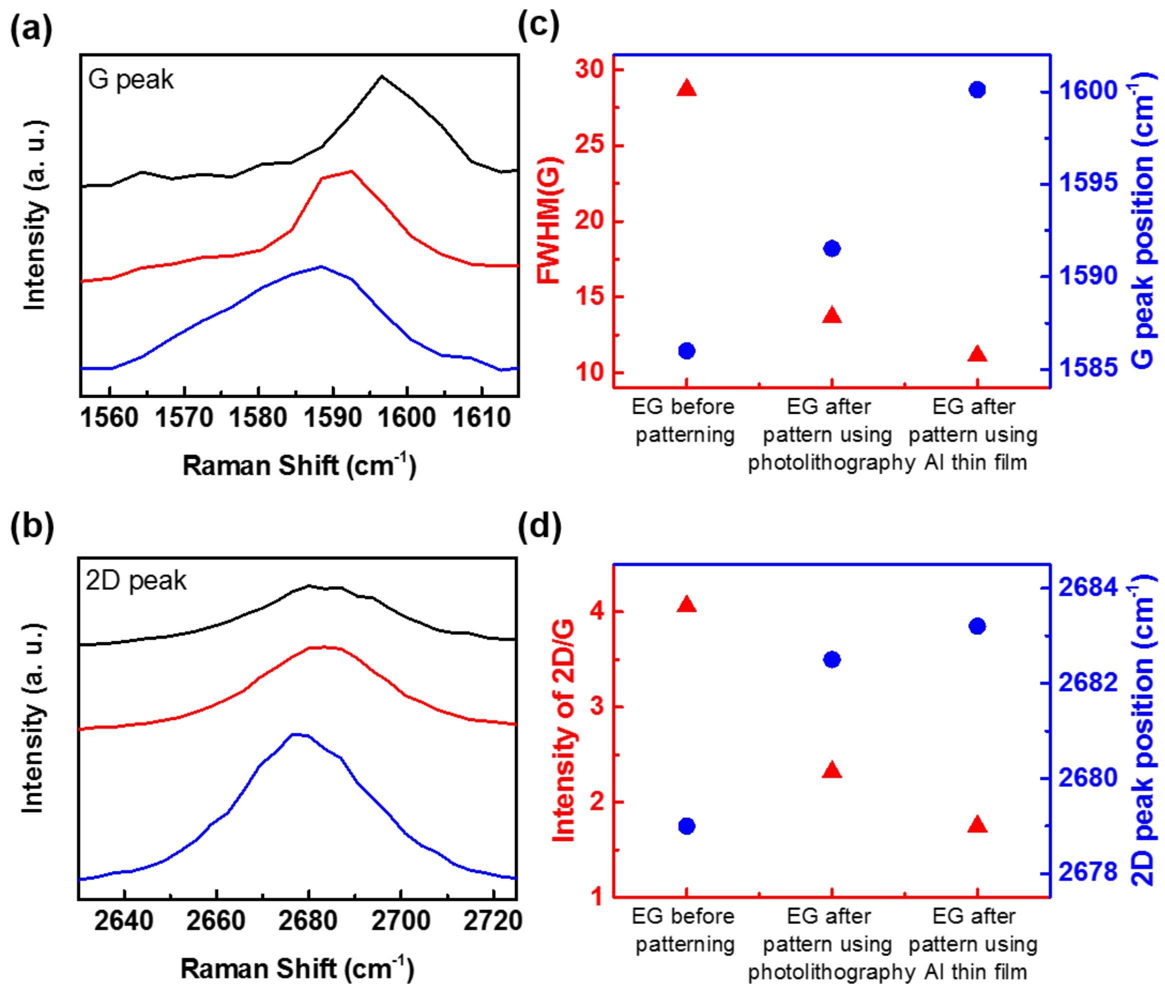


Figure 4.21: The change of Raman spectra in (a) G peak and (b) 2D peak before and after pattering. (c) Changes in position and FWHM of G-peak before and after patterning. (d) Changes in intensity ratio of 2D to G peak and 2D peak position depends on patterning. *[in preparation]*

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#### 4.3.5 Conclusion

In conclusion, we proposed a method for cleanly patterning EG without polymer processes using Al thin films as etch masks. This method does not leave polymer residues on the EG surface after the process, thus preventing scattering and unintentional doping arising from the residues. It has been confirmed by results of Hall measurement and Raman spectra. In particular, the apparent SdH oscillation seen in Al patterned EG devices demonstrates that this sample has much better homogeneity and a 2DEG system than photolithographically patterned EG device. The carrier density and Hall mobility in Al patterned EG device were determined to be $9.16 \times 10^{12}$ $cm^{-2}$ and ~ 2100 $cm^2/Vs$, respectively. We expect that this patterning method will contribute to analysis of intrinsic physical properties of graphene, and provide the ideal fabrication tool for next generation graphene based device applications.

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## V. Complementary Logic Inverter with CVD graphene

The use of graphene in digital logic devices is limited by the off-state currents resulting from unique zero bandgap structure. Nonetheless, graphene is still attractive material as a material for logic device in integrated circuits because it is easily doped by the contact material as a single atomic structure [120, 121]. Selective doping graphene is an essential process for using graphene in devices such as diodes, oscillators, and inverters [122, 123]. For this reason, studies on interaction between graphene and substrate [21, 124], and metal surface are actively being conducted. Particularly, since metal is used as contact electrodes of a graphene devices, studies on interaction and charge transfer between metal and graphene have been actively conducted by density functional theory. The graphene in contact with the metal is doped n- or p-type by equilibrium separation and the work function difference between them [19, 20]. It is expected that Al, Ag, Cu, Co, Ni and Ti metals with low work function would induce n-type doping while Au and Pt with high work function would induce p-type doping of graphene, and this theory has been confirmed by experiments [125, 126]. Graphene is unintentionally doped to p-type by absorbing water and oxygen molecules in the atmosphere, so passivation is essential for stable operation of graphene devices [127, 128].

In this study, we fabricate stable graphene transistors and inverters using nondestructive doping method and $Al_2O_3$ passivation layer. A metal (Al or Ti) thin film of 2 nm thickness having a lower work function than graphene is deposited on graphene surface to dope graphene to n-type. Graphene p doping is achieved by depositing a $SiO_2$ thin film on the graphene surface, which induces charge transfer from graphene to $SiO_2$. The $Al_2O_3$ film is uniformly coated on the doped graphene by ALD and serves as a passivation layer. Here, materials such as Al, Ti and $SiO_2$ should be selected for use as a seed layer for $Al_2O_3$ passivation layer deposition as well as doping [129]. Because of the high hydrophobicity and chemical inertness of graphene, it is impossible to deposit uniform $Al_2O_3$ directly on graphene surface using $H_2O$-based precursors [130]. The doping type and concentration are confirmed by Raman spectra and electrical measurements. A logic inverter device composed of a combination of p- and n-type graphene FETs with $Al_2O_3$ passivation is driven by the back gate and shows a clear voltage reversal characteristic of the inverter according to $V_{in}$ at various $V_{DD}$. The voltage gain of the inverter doped with Al-$SiO_2$ and Ti-$SiO_2$ has values of ~0.93 and 0.86 at back gate oxide 100 nm.

### 5.1 Fabrication of Graphene Inverter

Figure 5.1 indicates the fabrication process of graphene inverter. The graphene formed on Cu foil using CVD method is transferred onto $SiO_2$ (100 nm) / high-doped Si wafer layer. One side of the graphene formed on Cu foil is spin-coated with polymethyl-methacrylate (PMMA), and Cu foil is removed by ammonium phosphate. Graphene covered with PMMA is transferred onto $SiO_2$ substrate and PMMA is eliminated with acetone. The graphene channel region is masked with photoresist, and the other open region is etched by $O_2$ plasma for 1 min at 50 W in the RIE. The photoresist is removed

with acetone and methanol. Then, contact pads of $V_{DD}$, $V_{out}$, and $GND$ for inverter are formed by photolithography, Ti/Au (10nm/50nm) deposition, and lift off process. The patterned graphene channels between $V_{DD}$ and $V_{out}$ electrodes are covered with $SiO_2$ thin film using thermal evaporator for p-doping, and the other graphene channels between $V_{out}$ and $GND$ electrodes are coated with Al or Ti thin film (2 nm) using e-beam evaporator for n-doping. The formed Al and Ti thin films are naturally oxidized at room temperature and air pressure for 24 hours. The $Al_2O_3$ protective layer (30 nm) is uniformly deposited on the whole surface of substrate at 250 °C by ALD. The trimethylaluminum (TMA) and $H_2O$ are used as precursors of Al and O, respectively. The $SiO_2$, naturally oxidized Al and Ti layers act as seed layer for growth of uniform oxide on the graphene surface.

The work function difference and interaction between graphene and metal causes electron transfer between, which forms a potential barrier by induced dipole at graphene metal surface [19, 20]. It also changes the Fermi energy level and doping concentration of graphene. According to this mechanism, when Ti (4.33 eV) and Al (4.28 eV) with work function less than graphene (4.6 eV) are adsorbed to graphene, the charge is transferred from metal to graphene and the graphene is n-doped as shown in Figure 5.1(b) [131]. In our experiment, the electron doping concentration of graphene adsorbed on Al is smaller than that of Ti, even though Al has a lower work function than Ti. It is believed that graphene has weaker interaction with Al than Ti.

Dangling bonds on the $SiO_2$ surface induce coupling with graphene, causing charge transfer and band structure change of graphene. An O-terminal $SiO_2$ surface interacting strongly with graphene caused charge transfer from graphene to SiO2, resulting in p-doping of graphene (Figure 5.1(c)). By contrast, the graphene on Si-terminated $SiO_2$ surface behaves in a free standing state due to inactive dangling bond. It does not affect the charge transfer [21, 22].

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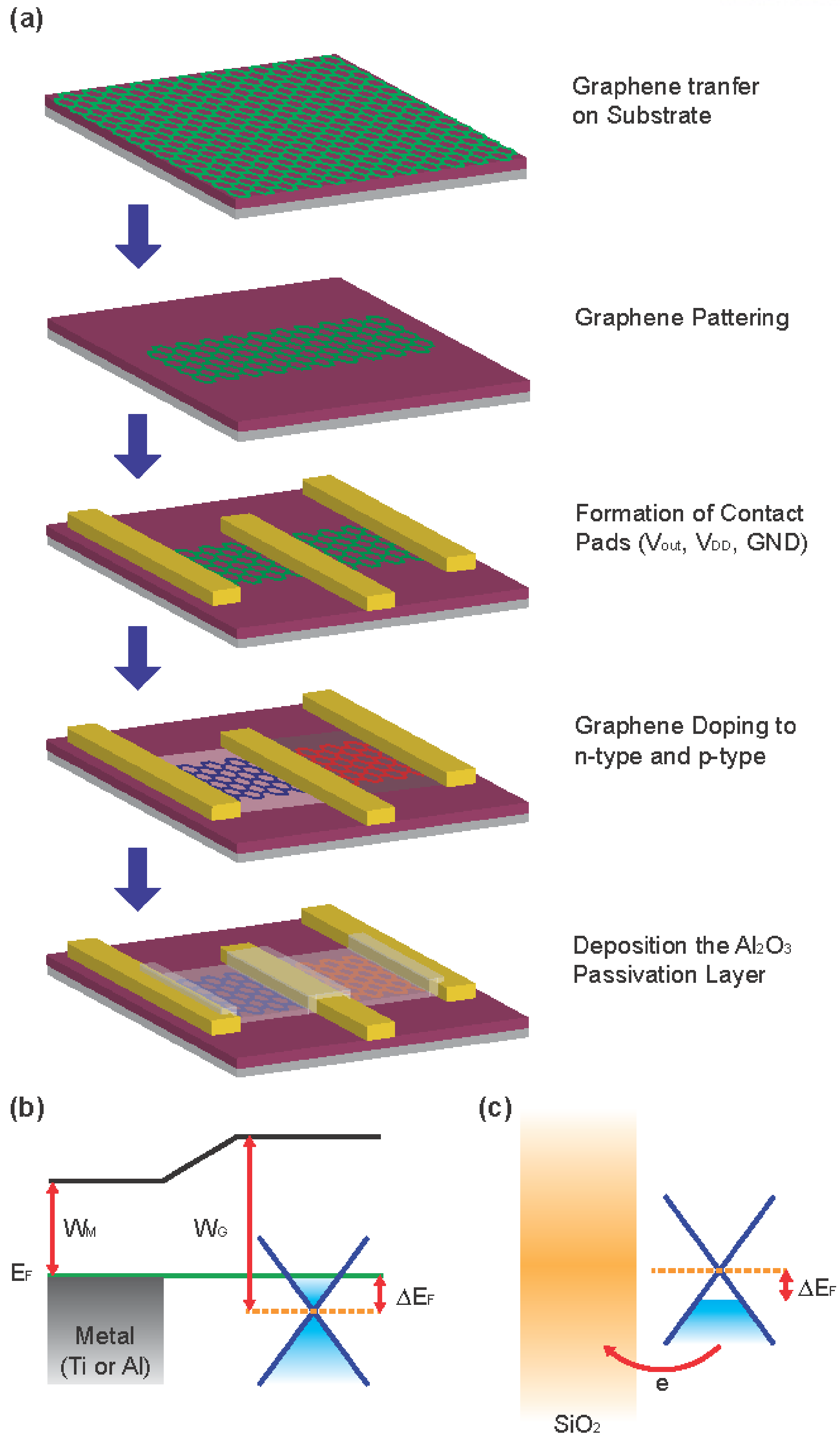


Figure 5.1: (a) Schematic illustration of graphene inverter fabrication process. Fermi energy level change of graphene adsorbed (b) Ti or Al thin film and (c) $SiO_2$. *[in preparation]*

### 5.2 Electrical Properties of n- and p-type graphene FET

Figure 5.2(a) indicates the resistance ( $R$ ) according to the gate bias ($V_G$) applied at $V_D$ = 0.01 V of the completed graphene device. As described above theoretical mechanism, graphene adsorbed on $SiO_2$ is p-doped with charge neutral point (CNP) of 0.6 and graphene adsorbed on Ti and Al are n-doped with CNP of -4.8 and -1.3, respectively. Here, $V_D$ is fixed at 0.01 V. As the value of $V_D$ increases, the position CNP move to a positive voltage. When $V_D$ increase from 0.01 V to 20 V, the CNP is shifted from 0.06 V to 11.3 V, -4.8 V to 6.2 V, and -1.3 V to 9.5 V for $SiO_2$, Ti, and Al adsorbed graphenes, respectively as shown in Figure 5.3. When $V_D$ is applied, the potential of the channel increases, which causes an additional amount of positive charge to be generated in the channel. Therefore, the higher gate bias should be applied to offset the increased potential of the channel, which seems to be a positive shift of CNP [132]. Here, the increased gate bias has a value of 1/2 of $V_D$, which is consistent with our experimental data (Figure 5.2(b)). The field effect mobility ( $\mu_{FE}$ ) is given as

$$\mu_{FE} = \frac{L_{ch} g_m}{W_{ch} C_G V_D} \tag{5.1}$$

where $L_{ch}$ and $W_{ch}$ are the length and width of graphene channel, $C_G$ is the capacitance between channel and gate, and $g_m$ is transconductance which is determined by $dI_D/dV_G$ [93]. The completed graphene FET shows enhanced electrical properties compared to before deposition of doping and the protective layer. The $\mu_{FE}$ is measured to 1051 (716) $cm^2/Vs$, 838 (352) $cm^2/Vs$ and 855 (481) $cm^2/Vs$ at room temperature for $SiO_2$, Ti, and Al film with $Al_2O_3$ passivation layer as shown in Figure 5.2(c). It is considered that contaminants such as oxygen and water molecules on the graphene surface are eliminated by heating process at 250 °C for 30 mins in the ALD vacuum chamber prior to the $Al_2O_3$ deposition.

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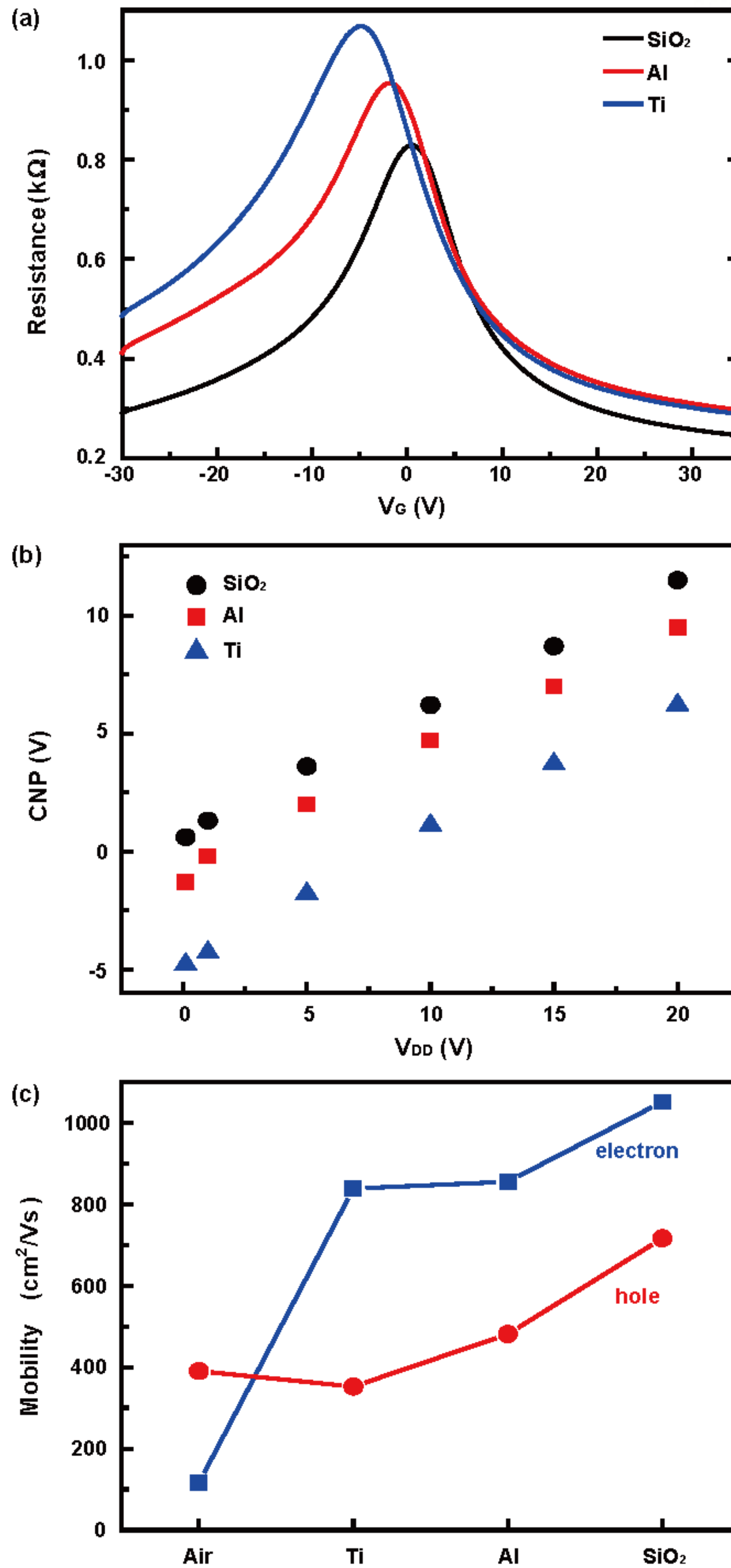


Figure 5.2: (a) Electrical properties of graphene doped with $SiO_2$, Ti, and Al thin films. (b) The change in CNP at different value of $V_D$. (c) Mobilities of graphene doped with $SiO_2$, Ti, Al thin films and air exposed. *[in preparation]*

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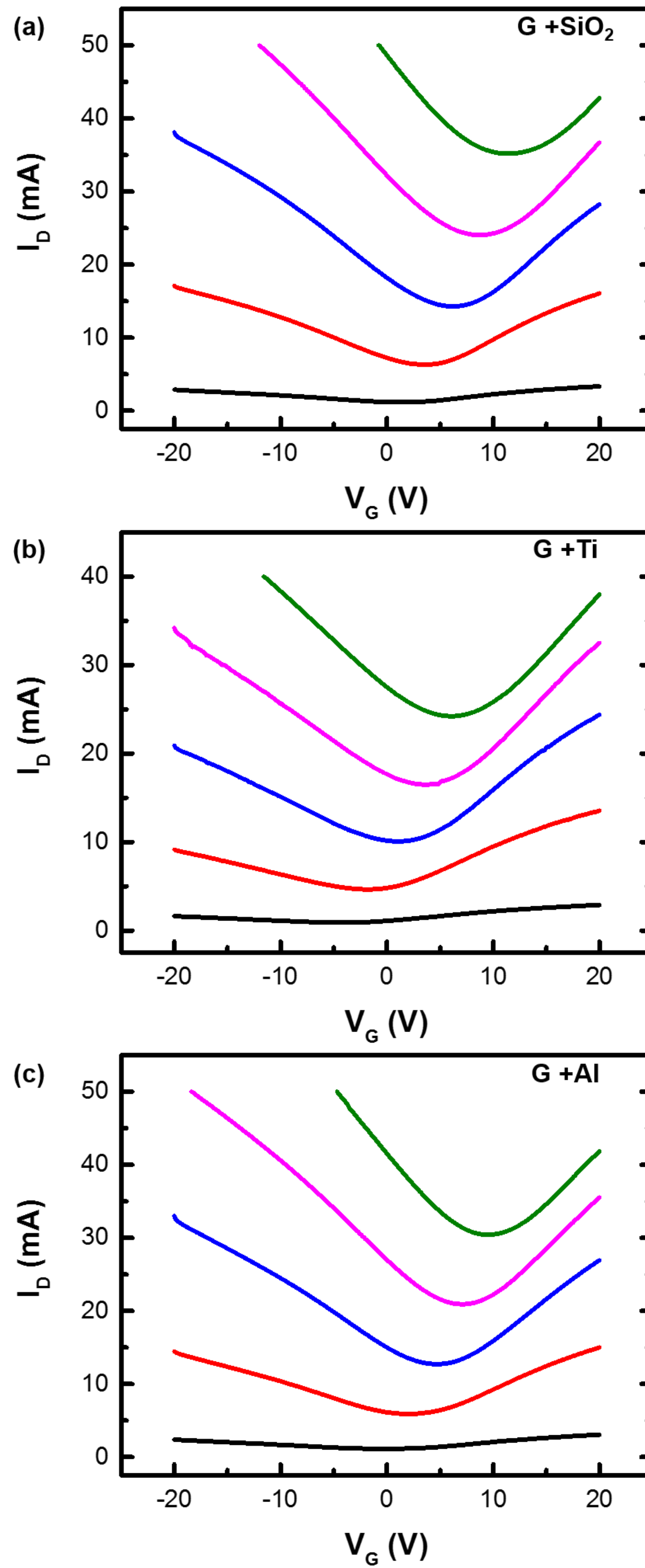


Figure 5.3: The $I_D - V_G$ curve of graphene FETs doped with $SiO_2$, Ti and Al at $V_D$ = 1 V, 5 V, 10 V, 15 V, 20 V. *[in preparation]*

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### 5.3 Raman Spectra Analysis of Doped Graphene

The doping characteristics of completed graphene device are also demonstrated by the Raman spectra [117]. Figure 5.4 show the Raman spectra of doped graphene channel by Ti, Al and $SiO_2$ with $Al_2O_3$ passivation. The width and position of G peak are changed by doping type and concentration because of electron-phonon coupling and the Kohn anomaly[30]. As the carrier density of holes or electrons increases, the position of the G peak shifts in the positive direction and the width decreases. The position of the 2D peak shifts in different directions depending on the type of doping. The position of the 2D peak is upshifted by n-doping and downshifted by p-doping, but the shift range is very small when the electron doping level is low. Figure 5.5 shows the Raman spectra changes in G and 2D peaks with adsorbed materials (Ti, Al, and $SiO_2$). G peak position are measured at ~1592.1 $cm^{-1}$ for Ti, ~1590.5 $cm^{-1}$ for Al, and ~1587.8 $cm^{-1}$ for $SiO_2$, which results is shifted from pristine graphene of ~1583.1 $cm^{-1}$. The higher the doping concentration, the lower the FWHM of G peak, which is ~ 14.9 for Ti, ~ 17.1 for Al, and ~ 20.9 for $SiO_2$ (Figure 5.5(a) and (c)). The position of the 2D peak of graphene adsorbed Ti (2686.2) and Al (2686) is slightly higher than that of $SiO_2$ (2684.3) adsorbed as shown in Figure 5.5(b). We have confirmed the doping concentration and type of fabricated graphene devices by Raman spectra, which is correspond to the electrical measurement results. The Ti and Al are lead to electron doping of graphene, while $SiO_2$ induce the hole doping. The doping concentration of graphene adsorbed Ti is higher than that of Al deposited.

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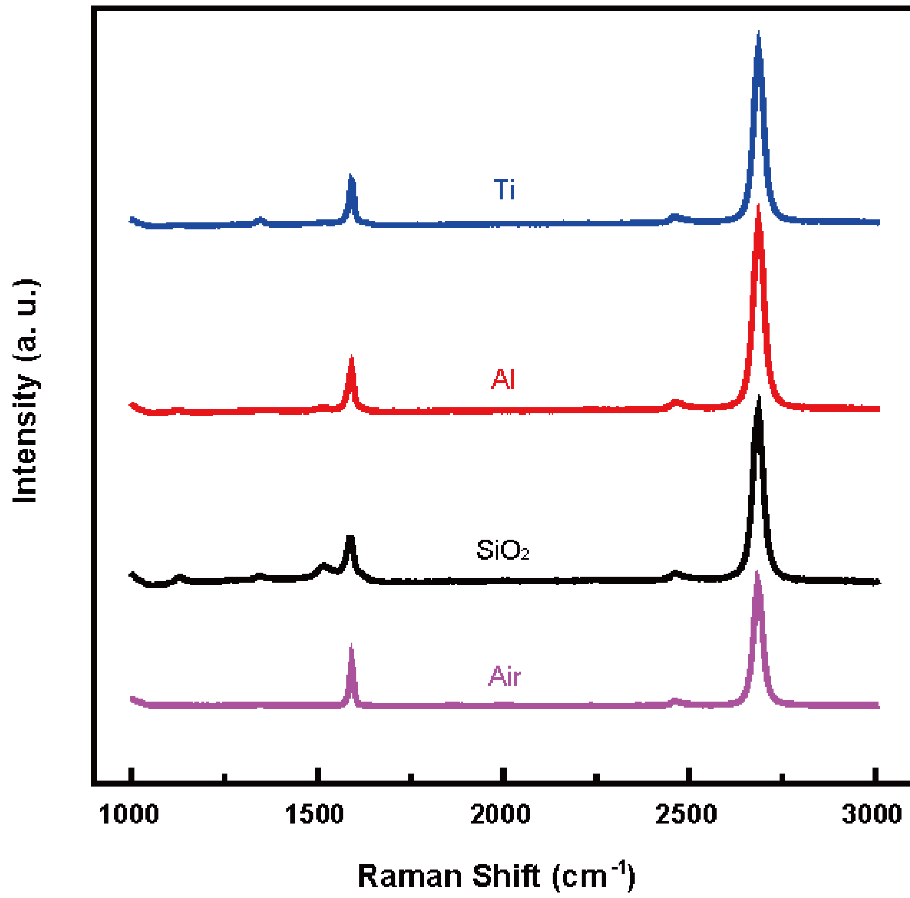


Figure 5.4: Raman spectra of graphene exposed to air and adsorbed Ti, Al and $SiO_2$. *[in preparation]*

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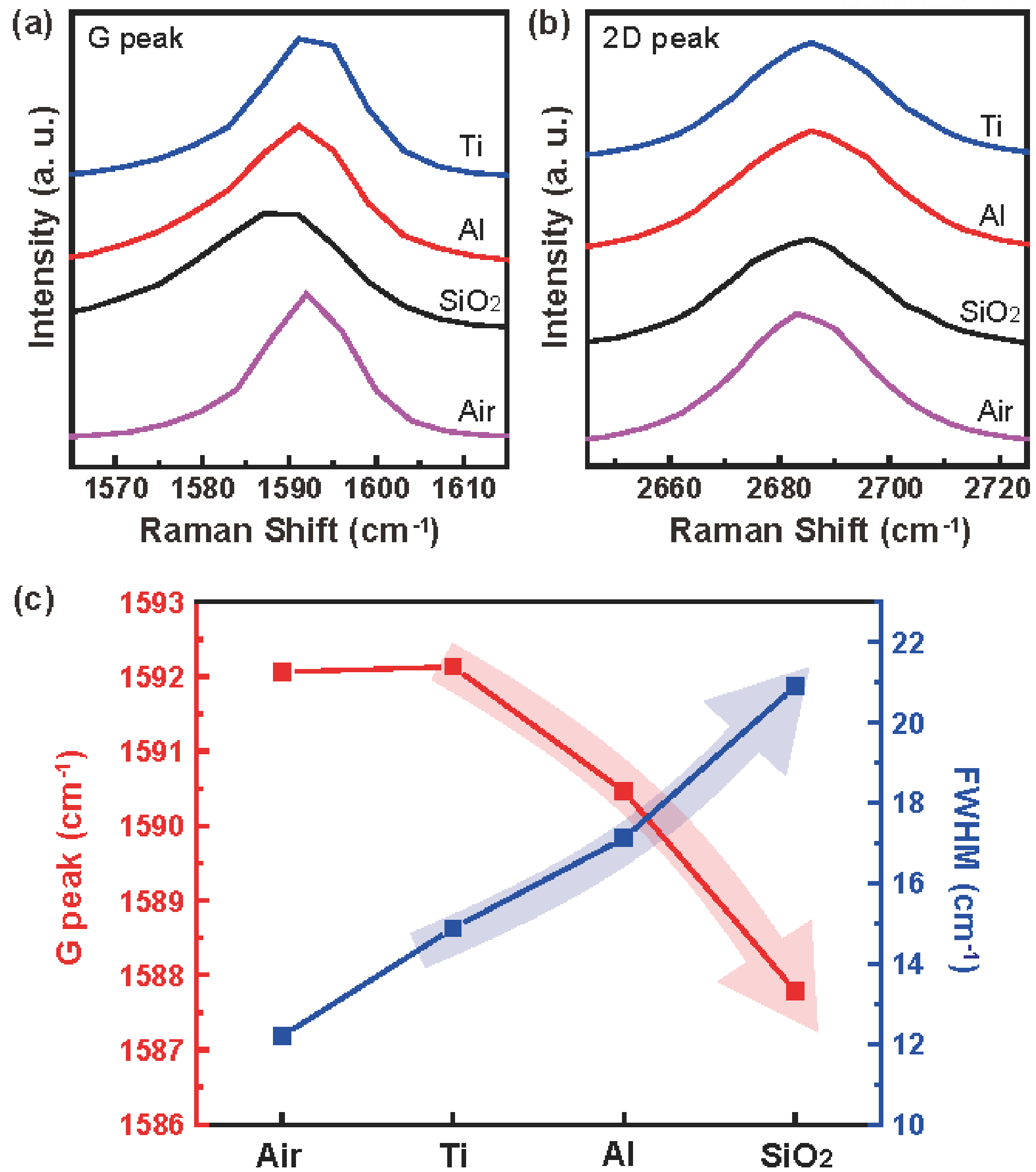


Figure 5.5: Raman spectra at (a) G peak, (b) D peak of air exposed and doped graphene. (c) graph of G peak position and FWHM according to the doping methods. *[in preparation]*

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**5.4 Operation Properties of Graphene Inverter**

The sources of the n-GFET and p-GFET are connected to $GND$ and $V_{DD}$, respectively, and the drains of both GFETs together form $V_{out}$ to fabricate the inverter. Here, the $V_{out}$ is determined as following [132, 133]

$$V_{out} = V_{DD} / (1 + R_p / R_n) \tag{5.2}$$

where $R_p$ and $R_n$ are the total resistance of p-GFET and n-GFET. Figure 5.6 shows operation properties of completed inverters, which demonstrates the typical $V_{out}$ inversion and its voltage gain according to the $V_{in}$ with several steps of $V_{DD}$ at 1 V, 5 V, 10 V, 15 V and 20 V. Figure 5.6(a) shows the operating properties of inverter consist of n-GFET and p-GFET doped with Ti and $SiO_2$, respectively. Here, the same bias $V_{in}$ is applied to the both n-GFET and p-FET by back-gate voltage. The increase of bias voltage $V_{in}$ induce the current increase of n-FET and current decrease of p-GFET, resulting in increase of $R_p/R_n$ and decrease of $V_{out}$. On the contrary, the decrease of bias voltage $V_{in}$ lead to current decrease of n-FET and current increase of p-GFET, resulting in reduction of $R_p/R_n$ and increase of $V_{out}$. Unlike a conventional CMOS inverter, the $V_{out}$ of graphene inverter is not constantly maintained at $V_{DD}$ or zero because neither n-GFET nor p-GFET cannot be perfectly turned off because of zero bandgap structure of graphene. When the bias voltage is applied to the graphene channel, the potential of the channel increases and CNP behaves as though it is shifted in the positive direction as shown in Figure 5.2 (b). Therefore, the inverted region of the inverter is shifted to a positive $V_{in}$ with increasing $V_{DD}$. Figure 5.6(b) indicates the operating properties of inverter consist of n-GFET and p-GFET doped with Al and $SiO_2$, respectively. Since the CNP positions of graphene adsorbed Ti or Al are different, the distance between $V_{in}$ values at high and low states of $V_{out}$ is different (Figures 5.6 (a) and (b)). Figure 5.6(c) and (d) show the absolute voltage gain ($|A| = dV_{out}/dV_{in}$) corresponding to Figure 5.6(a) and (b) according to the $V_{in}$. The voltage gain is proportional to the value of $V_{DD}$. The maximum voltage gain is measured at 0.93 and 0.86 in Figure 5.6(c) and (d), respectively. Here, the used gate oxide is 100 nm $SiO_2$ with dielectric constant of 3.9. The maximum voltage gain can be improved by using gate oxide with lower thickness and higher dielectric constant. Figure 5.7 shows the dynamic pulse response signals according to square-waveform input signals at $V_{DD}$ = 10 V of graphene inverter (doped with Ti and $SiO_2$). Figure 5.7(a) shows input signals of square waveform with the highest voltage ($V_H$) of 9.4 V and the lowest voltage ($V_L$) of -1.8 V. Figure 5.7(b) shows the response square signals with $V_L$ of 2.71 V and $V_H$ of 6.41 V corresponding to the input signals of Figure 5.7(b).

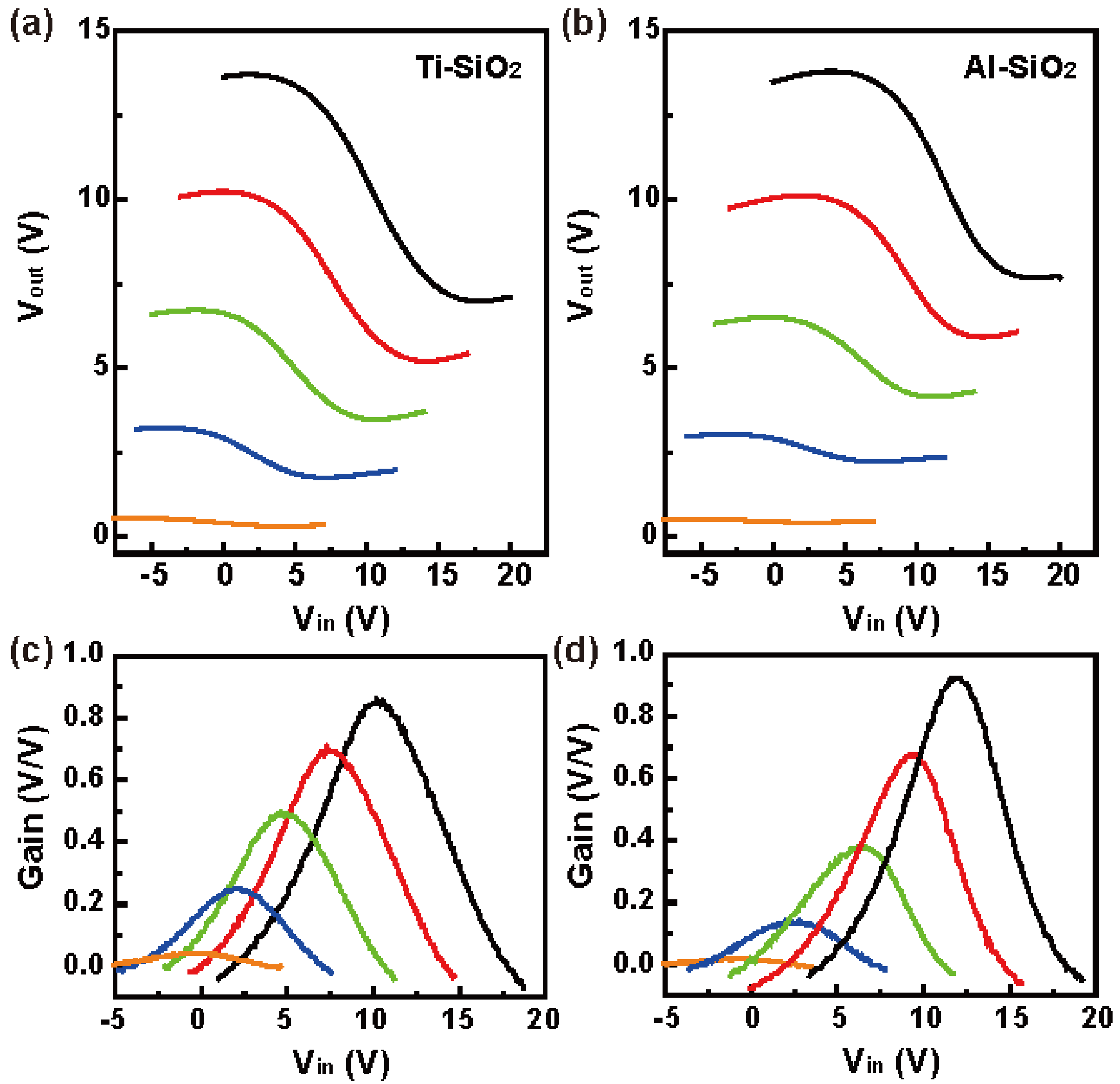


Figure 5.6: Voltage inversion properties of inverters doped with (a) $SiO_2$-Ti and (b) $SiO_2$-Al. Absolute voltage gain of inverters doped with (c) $SiO_2$-Ti and (d) $SiO_2$-Al. *[in preparation]*

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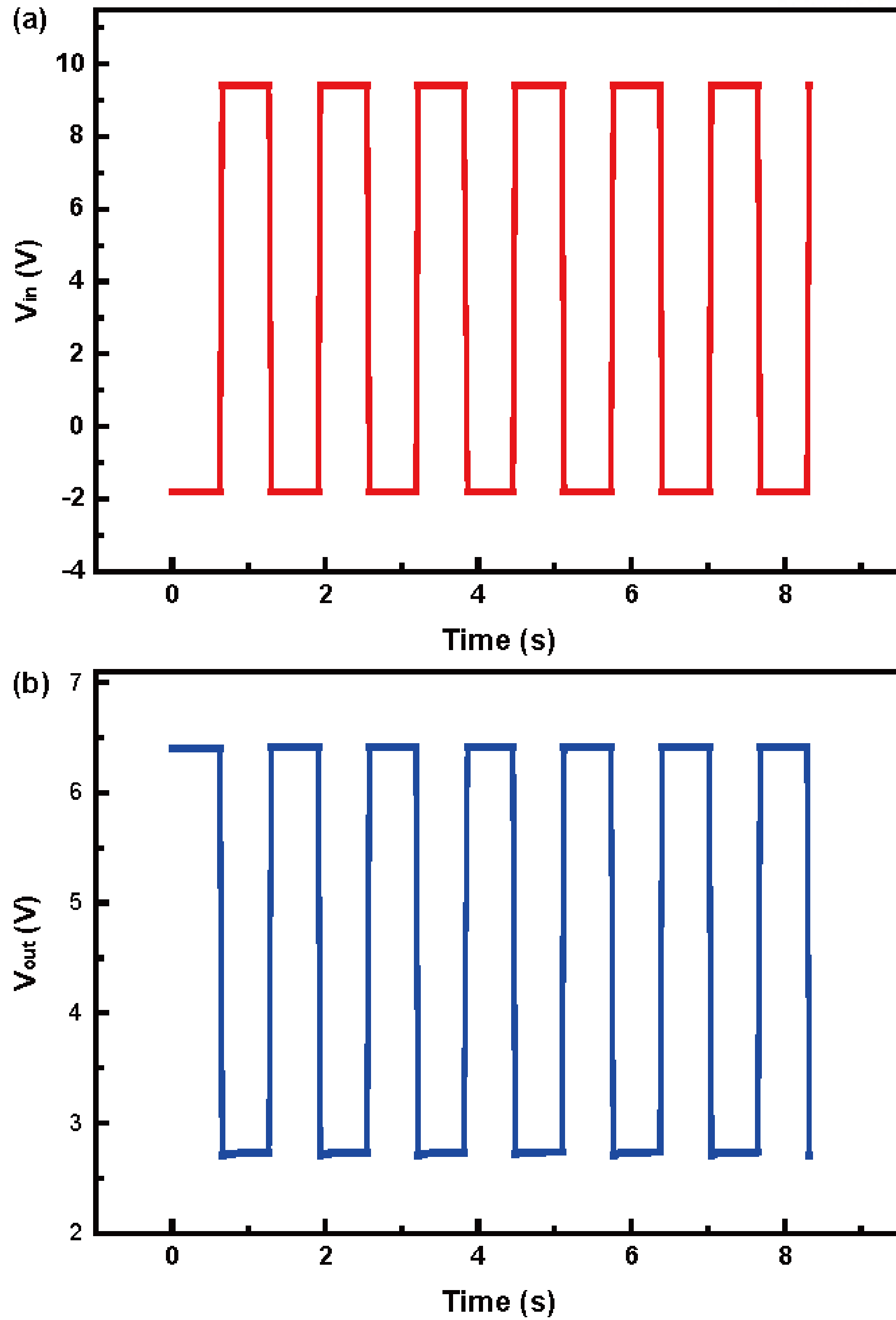


Figure 5.7: (a) Input signals of square waveform and (b) response square signals of inverter. *[in preparation]*

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### 5.5 Conclusion

The stable complementary logic graphene inverter is fabricated by doping with Ti, Al, and $SiO_2$ thin film and $Al_2O_3$ passivation. The Ti and Al thin film having lower work function than graphene cause charge transfer from the metal to graphene, which induce the n-doping and $\Delta E_F > 0$ of graphene. On the other hand, the graphene adsorbed on $SiO_2$ is doped p-type by the dangling bond of O-terminated $SiO_2$. The doping concentration and type of graphene are confirmed by Raman spectra and I-V curve of GFETs. The completed inverter device shows clear $V_{out}$ inversion properties as function of $V_{in}$ at wide range of $V_{DD}$ from 0.5 V to 20 V. The highest voltage gain is obtained about 0.93 and 0.86 for the inverter fabricated with Al-$SiO_2$ and Ti-$SiO_2$ at gate oxide of 100 nm $SiO_2$

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# APPENDIX A

## A. Stretchable Dual-Capacitor Multifunctional Sensor for Touch, Curvature, Pressure and Strain Sensing

As the demand for human-computer interface system used in robotics [123, 134, 135], internet of things (IoT) [136, 137], and personal medical systems [138-142] increases, the performances and functionalities of related sensors must be improved accordingly [35, 143-150]. In these interface systems, sensors play important role in recognizing human signals such as bio-signals in electroencephalogram (EEG) [151-155] and electrocardiogram (ECG) [155-158] and body motions [143, 159-164], and then sending them to equipment correctly. Through the sensor device, the machine can have human-like sensing capabilities and also be operated as intended by signals [165]. For elaborate sensing, sensors have to notice and discriminate different input signals (Multi-functionality). The stretchability is also required for mounting sensors on skin or clothes [109, 166-170]. In order to develop sensitive and portable sensor, in-depth research about skin-mountable multi-functional capacitive sensor have been studied by using variety of materials. The Zhu's group recently introduced wearable multifunctional sensors using silver nanowire (AgNW), which can sense strain (up to 50 %), pressure (sensitivity of 1.62 $MPa^{-1}$), touch motion and several human motions such as walking, running, squatting and jumping[16] [147]. The Lacour's group also proposed a stretchable multifunctional sensor using gold thin films embedded in polydimethylsiloxane (PDMS) that accomplished uniaxial strain (up to 20 %), pressure (sensitivity of 0.4 $MPa^{-1}$) and finger touch motion sensing[14] [150]. However, most of former studies are structure of single-capacitor sensors, which have some inevitable limitations. Firstly, they are able to only detect the intensity of the stimulus without detecting directional information. Secondly, the types of detected stimuli cannot be clearly distinguished by a single capacitance change alone. For example, single-capacitor sensors exhibit the same tendency of increasing capacitance with respect to pressure and strain.

Here, we propose a new structure of dual-capacitor multifunctional sensor to overcome weaknesses of sensors studied so far. Unlike the single-capacitor sensor mentioned above, our dual-capacitor sensor is composed of two capacitors stacking perpendicularly in each pixel which allow to clearly distinguish the kinds of external stimulus and also can sense its strength information and surface-normal directionality. These abilities have been demonstrated for various sensing such as curvature, pressure, touch and strain [23].

### A.1 Selective Surface Treatment for Fabrication of Dual-Capacitor Sensor without Lithography and Etching

Figure A.1 shows the fabrication processes for 5×5 array of dual-capacitor multi-functional sensor. Basically, our dual-capacitor sensor is made of AgNW and PDMS only. The all insulating layers, and

protective layer consist of PDMS film. The all electrodes of bottom, middle, and top are prepared by AgNW film. A PDMS (Sylgard 184, Dow Corning) are prepared by blending the "base" with the "curing agent" in the weight ratio of 10 : 1 and stirring for 5 mins. Then, the mixed PDMS is stored at -4 °C for 24 hours to eliminate the air bubbles present in the PDMS. The PDMS film is uniformly coated by spin-coating and its thickness is easily controlled by adjusting speed and time of spin-coating. As a final step, coated PDMS layer is harden in an oven at 100 °C for 20 mins for solidification. Before AgNW (0.3 wt. % of AgNW dispersed in distilled water) coating, the surface properties of PDMS should be changed from hydrophobic to hydrophilic to improve the adhesion between AgNW and PDMS surface. It is performed by $O_2$ plasma treatment with 100 W power for 5 mins [171]. Here, we selectively activate the unblocked PDMS surface in shadow mask as shown in Figure A.2. Because of the selective $O_2$ plasma treatment, the patterned AgNW electrodes can be formed simultaneously with spin-coating of AgNW solutions without etching and lithography processes. After that, the coated AgNW is heated at 110 °C for 10 mins to evaporate the DI water, and the shadow mask is detached to form a patterned AgNW electrodes. The line width and spacing of completed AgNW electrodes are 2 mm. Finally, the contact pads of Ti (10 nm) and Au (50 nm) sequentially formed on patterned sample. Figure A.3 indicates the I-V curve and the optical microscope image in dark field mode of AgNW electrode. The structure of the AgNW electrode is ~ 7.5 cm in length and ~ 0.22 cm in width and line resistance of ~ 650 Ω is measured in the I-V curve. The thickness of lower and upper PDMS dielectric layers are ~400 μm. Unlike other group's fabrication methods where two PDMS films with patterned AgNW electrodes are physically attached together to form a pixelated single-capacitor sensor [143, 147, 148], all layers of dual-capacitor sensor are formed continuously starting from the substrate to protective layer. This improves the bonding force between the stacked layers and make it easy to align the stacked capacitors accurately. We pour liquid PDMS on cured underlying PDMS layer and spin-coat it to control thickness, and harden it at oven. In this case, the liquid PDMS is firmly bonded to the underlying PDMS layer while being cured, and thereby providing excellent adhesion between adjacent layers. The cross-sectional image (Figure A.4) of the completed dual-capacitor sensor shows a strong bonding force between the layers. It has a total of 25 pixels and the average capacitance of each capacitor is ~ 2.2 pF. Figure A.1(b) indicates the schematic illustration of dual-capacitor sensor during convex shape with the curvature radius of $r(\theta)$ where $\theta$ is the corresponding curvature angle. Figure A.1(c) and (d) shows the photograph of dual-capacitor sensor bent and stretched.

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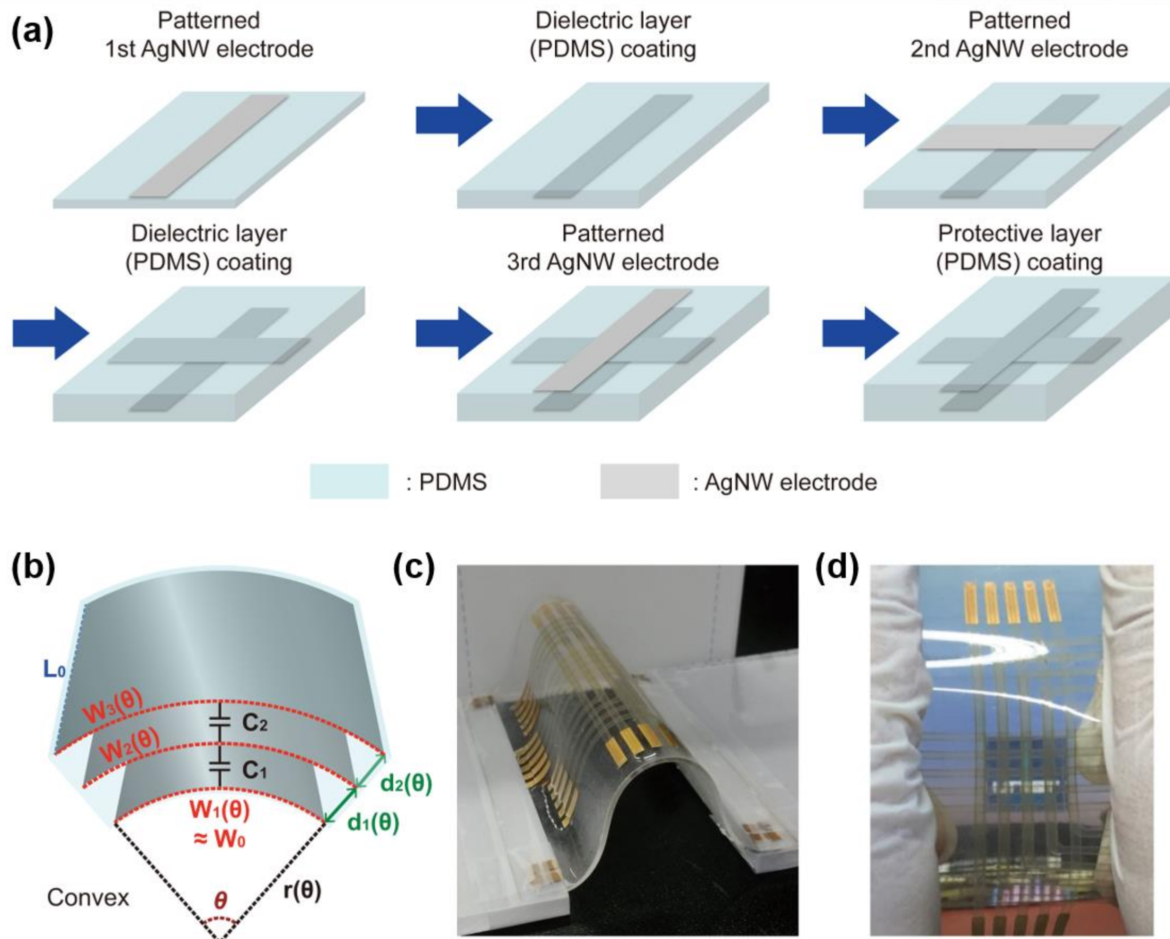


Figure A.1: (a) Schematic diagrams of fabrication process flow of dual-capacitor sensor (b) Schematic illustration of convex shaped dual-capacitor sensor with curvature radios of $r(\theta)$ (c) Photograph images of dual-capacitor sensor (a) curved in convex shape and (b) stretched with hands [23].

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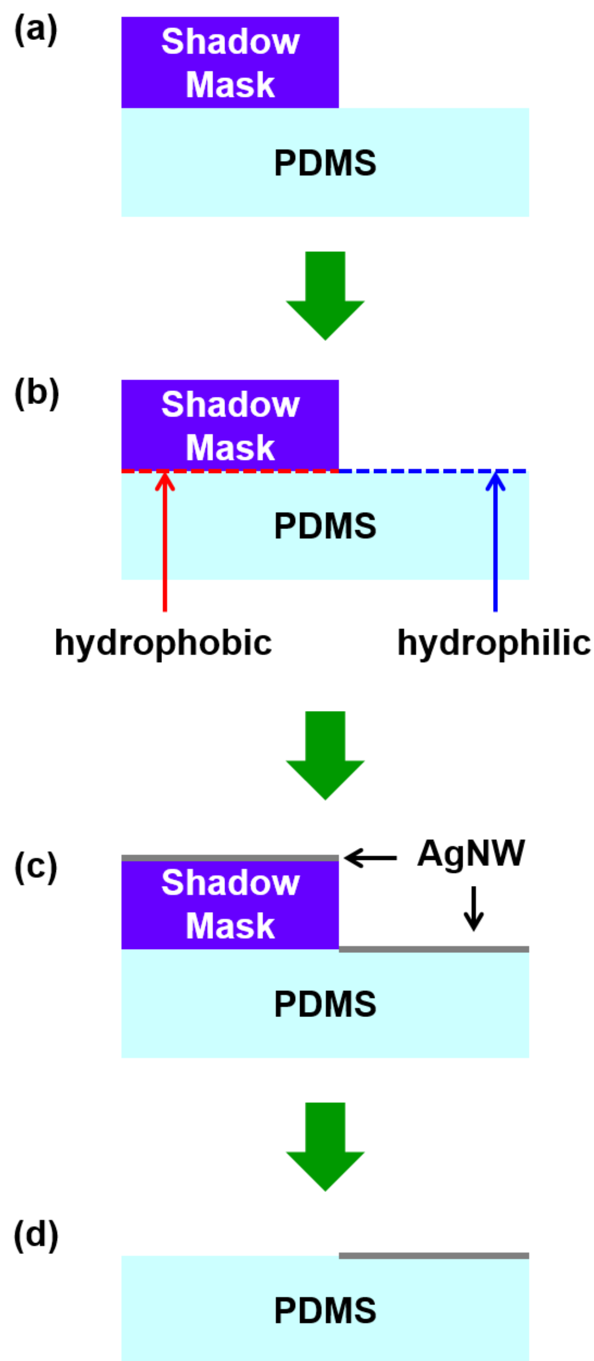


Figure A.2: Schematic diagrams of AgNW film patterning process using selective $O_2$ plasma treatment method [23].

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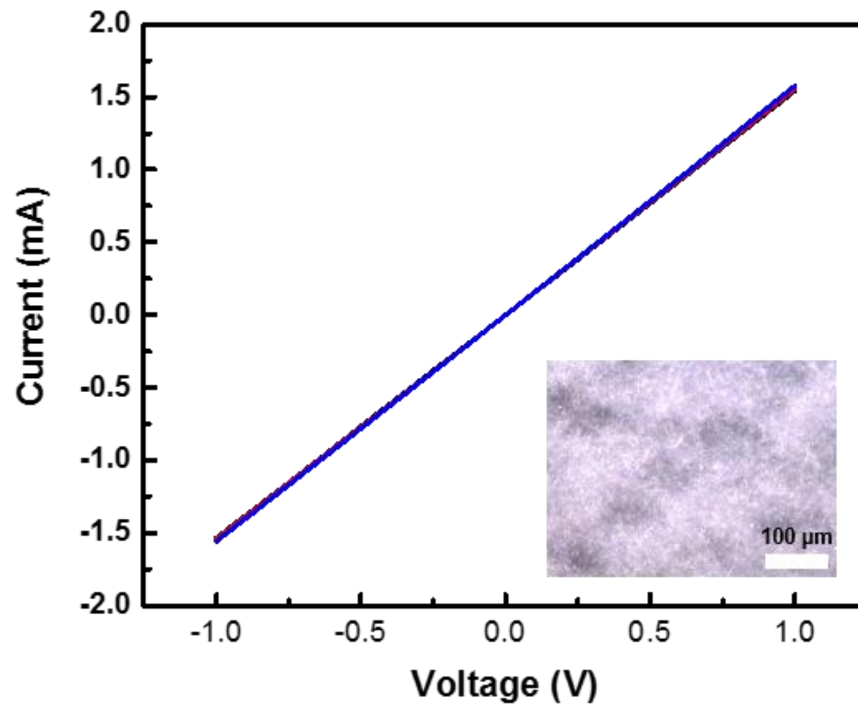


Figure A.3: The I-V curve and optical microscope image of patterned AgNW electrode (Length: ~7.5 cm, Width: ~0.22 cm) [23].

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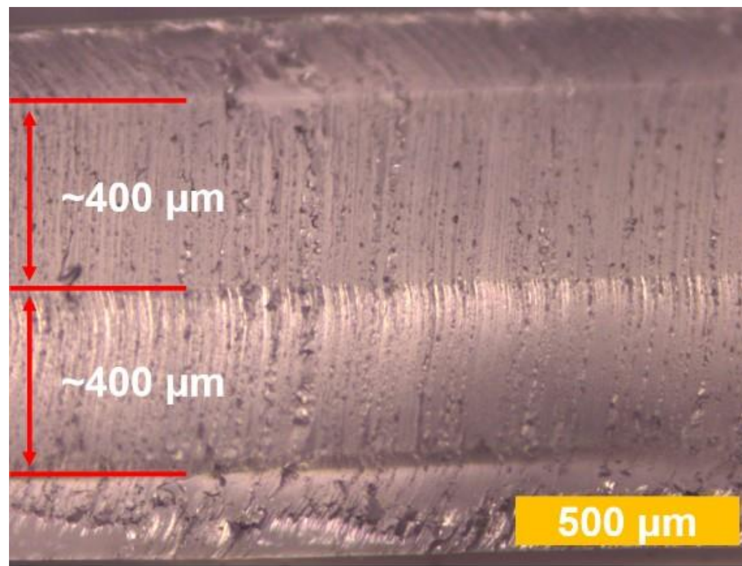


Figure A.4: The cross-sectional image of dual-capacitor multi-sensor, which demonstrate the strong bonding strength between adjacent layers [23].

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### A.2 Capacitance Changes Depend on Sensing Modes

We measure capacitance changes of dual-capacitor sensor while applying stimulus such as curvature, pressure, strain, and touch. The pressure is applied by loading acrylic block onto the surface of dual-capacitor sensor and the intensity of pressure is adjusted by changing the quantity of acrylic blocks. The radius of curvature is controlled by adjusting the spacing between the two acrylic clamping jigs holding both ends of sensor (Figure A.1(c)). The tensile strain is applied by fixing both ends of sensor to two clamping jigs and pulling them in opposite directions. Finally, the touch is performed with minimal force on the sensor and gentle contact of the finger on the sensor surface.

The capacitance change of the dual-capacitor sensor is confirmed using the Precision LCR meter (E4980A, Agilent) at the frequency of 1 MHz with a 50 mV dithering voltage operated by homemade LabView program. Since the LCR meter can only measure one capacitance at a time, the measurements of upper and lower capacitances are conducted individually while holding external stimuli on the dual-capacitor sensor. For curvature sensing mode, capacitances of upper and lower capacitors are sequentially confirmed while maintaining the shape of the curved sensor. The capacitance change of the touch sensing mode according to the time are measured in the following manner: First, touch and untouch motions are performed periodically at fixed time intervals while the capacitance change of the upper (or lower) capacitor is measured. Then, the capacitance of the other capacitance is measured in the same way. In the end, capacitance changes of the upper and lower capacitors are displayed on one graph along the same time axis.

The intrinsic capacitance of a parallel plate capacitor is defined by

$$C = \varepsilon_r \varepsilon_o \frac{L_o W_o}{d_o} \tag{A.1}$$

where $\varepsilon_o$ is vacuum permittivity (F/m), $\varepsilon_r$ is dielectric constant of insulating layer, $d_o$ is thickness of insulating layer, $L_o$ and $W_o$ are lateral sizes of capacitor.

#### A.2.1 Curvature Sensing

With no external stimulation, the pixel sizes ($L_o$ and $W_o$) and insulating layer thicknesses ($d_o$) of the two parallel-plate capacitors of dual-capacitor sensor are equal to each other. For convex shape (Figure A.1(b)), the width of top electrode ($W_3(\theta)$) is stretched more than that of middle electrode ($W_2(\theta)$). On the other hand, the width of lower electrode is hardly deformed ($W_1(\theta) \approx W_o(\theta)$). Here, a PDMS elastomer having a Poisson ratio of approximately 0.5 is incompressible for plastic deformation in a relatively small deformation and hence the bottom electrode is not compressed by plastic bending for detecting curvature [150, 172, 173]. Considering the cylindrical capacitor equation, the capacitances of lower ($C_1$) and upper ($C_2$) capacitors curved at $r(\theta)$ is as follow

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$$C_1(\theta) = \frac{2\pi\,\varepsilon_r\varepsilon_0 L_0}{\ln\left[\dfrac{r(\theta)+d_1(\theta)}{r(\theta)}\right]} \times \frac{W_0}{2\pi\, r(\theta)}$$
$$C_2(\theta) = \frac{2\pi\,\varepsilon_r\varepsilon_0 L_0}{\ln\left[\dfrac{r(\theta)+d_1(\theta)+d_2(\theta)}{r(\theta)+d_1(\theta)}\right]} \times \frac{W_0}{2\pi\, r(\theta)} \tag{A.2}$$

where $\varepsilon_o$ is vacuum permittivity and $\varepsilon_r$ the dielectric constant of dielectric layer. Assuming that the cross-sectional area of the dielectric layer is equal to those of the initial state (No bending), the following relation for the thickness of the dielectric layer is established.

$$W_0 d_0 = \left[\pi\{r(\theta)+d_1(\theta)\}^2 - \pi\{r(\theta)\}^2\right] \times \frac{W_0}{2\pi\, r(\theta)}$$
$$\Rightarrow d_1(\theta) = -r(\theta) + \sqrt{\left[r(\theta)\right]^2 + 2d_0 r(\theta)}$$
$$W_0 d_0 = \left[\pi\{r(\theta)+d_1(\theta)+d_2(\theta)\}^2 - \pi\{r(\theta)+d_1(\theta)\}^2\right] \times \frac{W_0}{2\pi\, r(\theta)}$$
$$\Rightarrow d_2(\theta) = -\left[r(\theta)+d_1(\theta)\right] + \sqrt{\left[r(\theta)\right]^2 + 4d_0 r(\theta)} \tag{A.3}$$

By substituting equation (A.3) into equation (A.2), the capacitance of the two capacitors is represented more simply by the $r(\theta)$.

$$C_1(\theta) = \frac{2\varepsilon_r\varepsilon_0 L_0 W_0}{\ln\left[1+2d_0/r(\theta)\right]} \times \frac{1}{r(\theta)}$$
$$C_2(\theta) = \frac{2\varepsilon_r\varepsilon_0 L_0 W_0}{\ln\left[1+2d_0/\{r(\theta)+2d_0\}\right]} \times \frac{1}{r(\theta)} \tag{A.4}$$

When the capacitor is bent concave, the same equation as in equation (A.4) applies, but the values of $C_1$ and $C_2$ are exchanged. Figures A.5 (a) and (b) indicate the capacitance change of the lower ($\Delta C_1$) and upper ($\Delta C_2$) capacitors depending on the radius of curvature $1/r$ when the dual-capacitor sensor is curved into a convex and concave shape. For convex shapes (Figure A.5(a)), $\Delta C_2$ is greater than $\Delta C_1$ in all curvature ranges. By contrast, for concave shapes, $\Delta C_2$ is less than $\Delta C_1$ (Figure A.5(b)). Figure A.5 (c) indicates the difference between $\Delta C_2$ and $\Delta C_1$ with a change in 1 / r, and this difference has been shown to increase with increasing $1/r$. From these measured results, the dual-capacitor sensor demonstrated that the surface-normal directionality and curvature radius can be measured through comparison of $\Delta C_1$ and $\Delta C_2$ with proper calibration.

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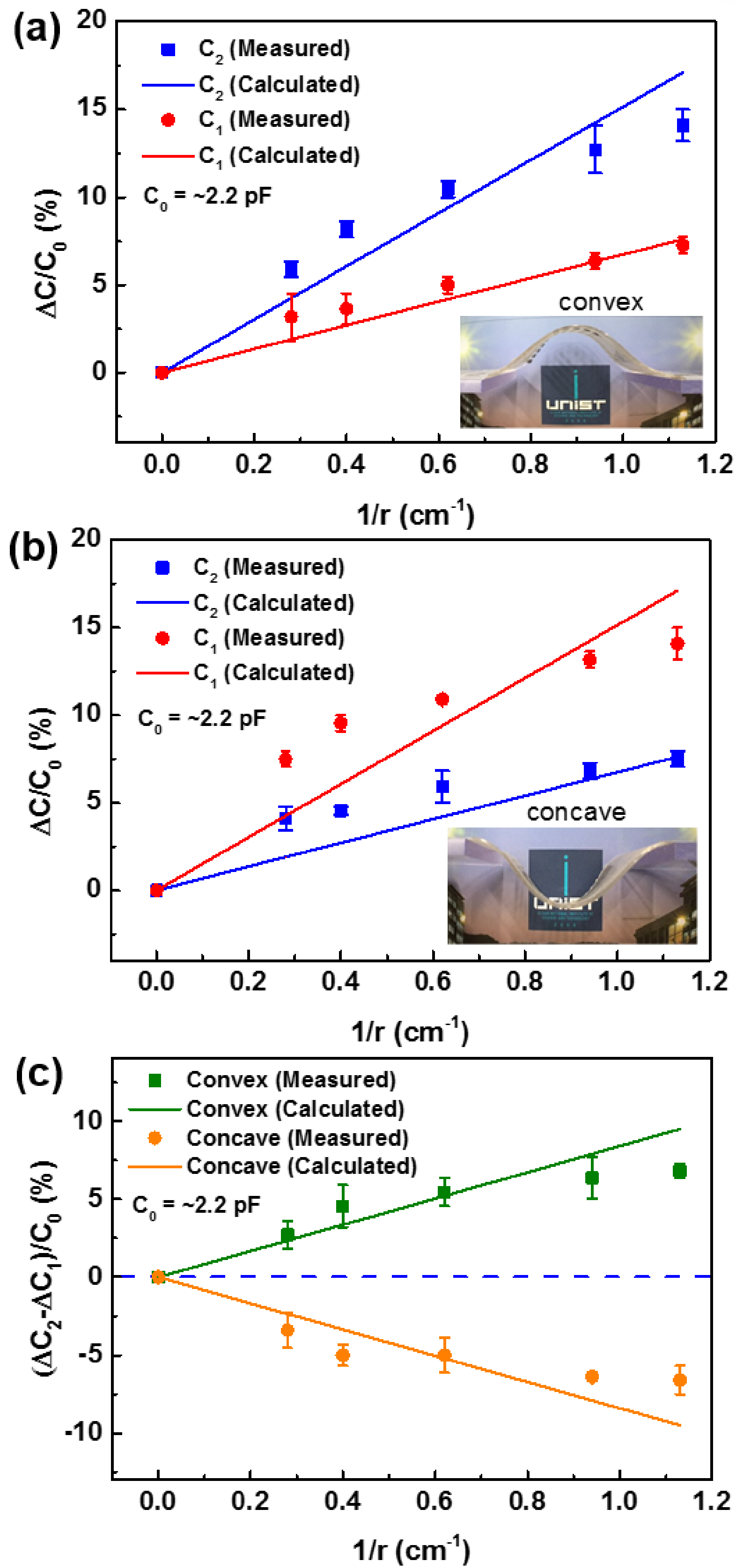


Figure A.5: Measured and calculated results of dual-capacitor sensor in (a) convex and (b) concave shape. (c) The difference of $\Delta C_2$ and $\Delta C_1$ according to $1/r$ in convex and concave shape [23].

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**A.2.2 Pressure Sensing**

Dual-capacitor sensor is able to detect both the magnitude and the surface-normal directionality of applied pressure by comparing $\Delta C_1$ and $\Delta C_2$ with proper calibration. When pressure is applied to the sensor, the insulating layer gets thinner, meaning that $d_o$ decreases. Hence, the capacitance will increase in accordance with the equation (A.1). If a localized pressure is applied to the upper (lower) side of the dual capacitor sensor, the applied force is distributed laterally as it goes down (up) through the insulator. Therefore, the magnitude of pressure (force dividing by area) becomes smaller as it passes through the insulator layer as shown in Figure A.6. If the insulator layer of the upper capacitor is thick enough to distribute the applied pressure, the pressure delivered to the lower capacitor is substantially reduced. In other words, only the insulator thickness of the upper capacitor is reduced while that of the lower capacitor is hardly changed. The PDMS layer of ~400 µm thickness absorbs perfectly the applied pressure up to ~75 kPa. This pressure value is the maximum pressure that can be applied in our experiment system. As a result, only one of the two capacitors is compressed by the applied pressure, and the change in capacitance occurs only on one capacitor (Figure A.7(a)). Figure A.7(b) indicates the $\Delta C_1$ and $\Delta C_2$ in our dual-capacitor sensor according to the applied pressure on upper side. The only $\Delta C_2$ has increased and $\Delta C_1$ is almost zero, which is exactly what we expected. Pressure sensitivity ($S$) can be calculated as following [174]

$$S = \frac{\delta(\Delta C / C_0)}{\delta p} \quad \text{(A.5)}$$

where $P$ is the applied pressure, $C_o$ is the initial capacitance without applied pressure, and $\Delta C$ is the capacitance variation from the initial value $C_o$. For the pressures below 10 kPa, $S$ is very high and decreases slightly with increasing pressure. For the pressures above 10 kPa, $S$ has a constant value of 1 MPa$^{-1}$. It is higher than other studies suing PDMS as a dielectric layer [150]. A very thin protective layer is considered a major factor in high pressure sensitivity by transferring pressure to a buried capacitor with minimizing pressure loss.

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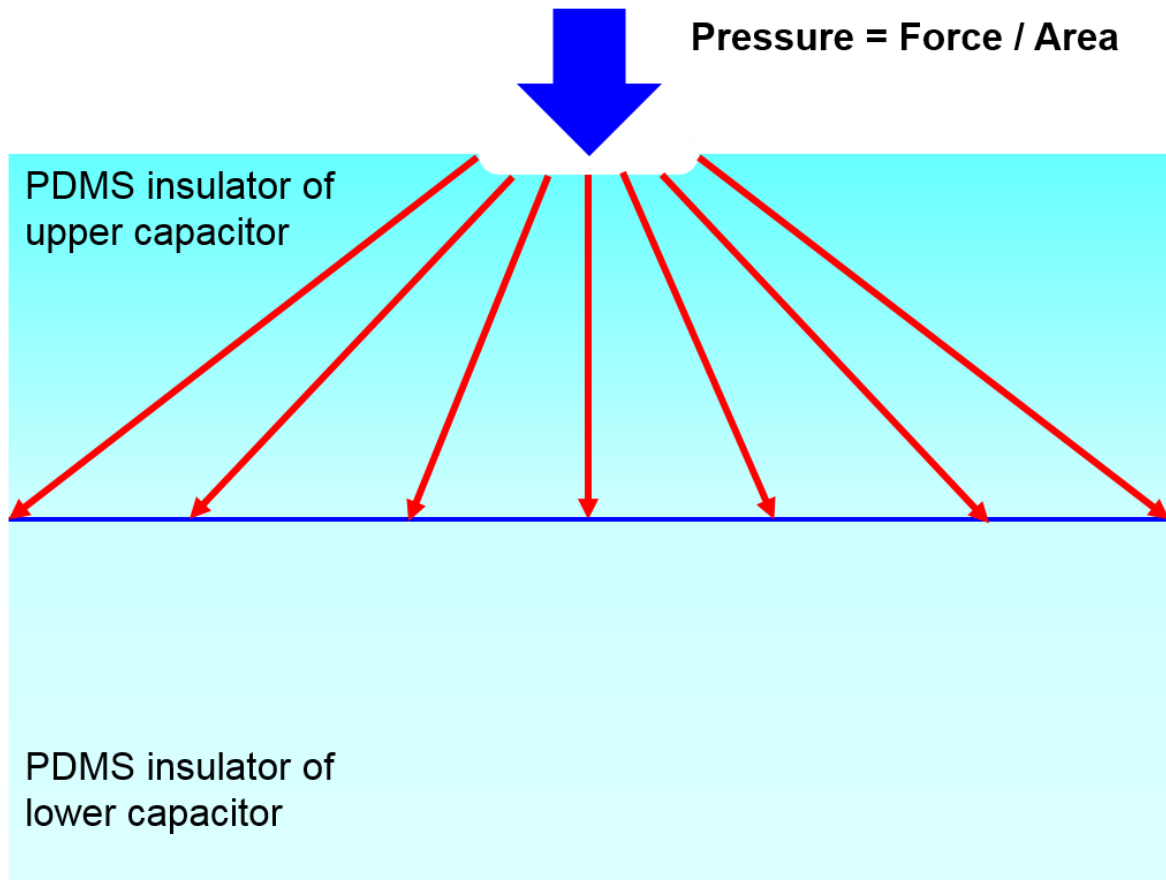


Figure A.6: Schematic view of dispersion of applied pressure according to depth of PDMS insulating layer.

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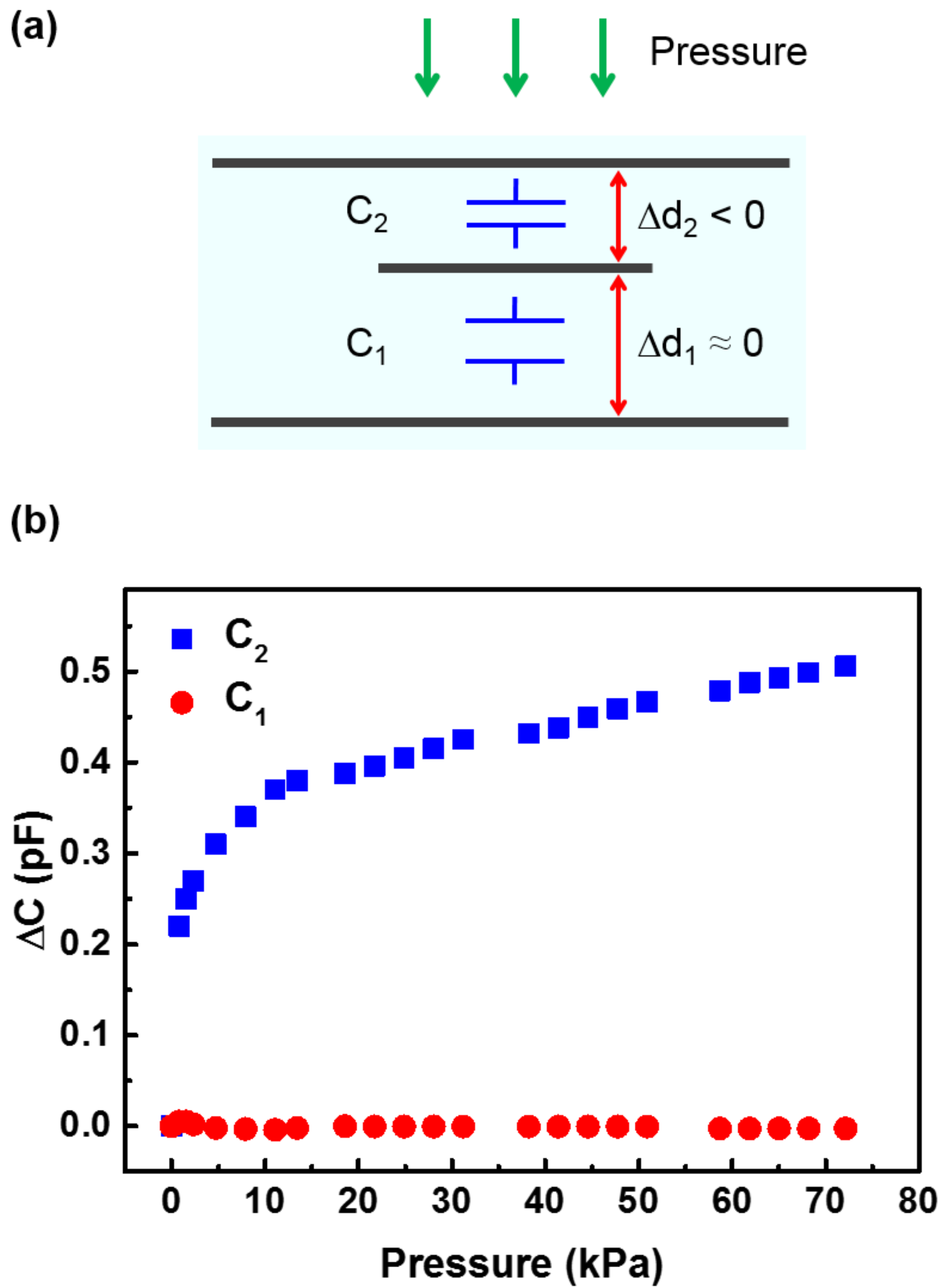


Figure A.7: (a) Schematic view of principle of pressure sensing in dual-capacitor sensor. (b) The upper ($\Delta C_2$) and lower ($\Delta C_1$) capacitance changes according to applied pressure on top surface [23].

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### A.2.3 Strain Sensing

In case of tensile strain, the capacitance can be expressed with the following relation for relatively small strains [147]

$$\begin{aligned} C &= \varepsilon_r \varepsilon_o \frac{L_o(1+\varepsilon)W_o}{(1-\nu_{PDMS}\varepsilon)d_o} \\ &= \varepsilon_r \varepsilon_o \left( \frac{1+\varepsilon}{1-\nu_{PDMS}\varepsilon} \right) \frac{L_o W_o}{d_o} \\ &\approx \varepsilon_r \varepsilon_o \left[ 1+(1-\nu_{PDMS})\varepsilon \right] \frac{L_o W_o}{d_o} \end{aligned} \tag{A.6}$$

where $\nu_{PDMS}$ is Poisson's ratio of PDMS and $\varepsilon$ is tensile strain. Pulling the dual capacitor sensor sideways reduces the thickness of the two insulating layers equally, resulting in increasing $C_1$ and $C_2$ equally (Figure A.8(a)). Figure A.8(b) indicates $C_1$ and $C_2$ as function of applied strain. Both of them increase linearly to almost same values up to 25 % strain. The stretchability of a dual-capacitor sensor is confirmed by repeatedly peforming stretching (~20 %) and relaxing cycles test. The $C_1$ and $C_2$ of the dual-capacitor are measured every 100 cycles in the relaxed state, and this repetition cycle test is performed a total of 1,000 times. As shown in Figure A.9, the rate of $\Delta C_1$ and $\Delta C_2$ in dual-capacitor is always less than 2 % after stretchability test, which demonstrate outstanding stability of dual-capacitor sensor. Figure A.10 shows the rate of $\Delta C$ by stretching and relaxing motion of dual-capacitor sensor. The value of $C$ responds directly to the shape of the sensor, which means that residual strain is not exist after release and stretching motions.

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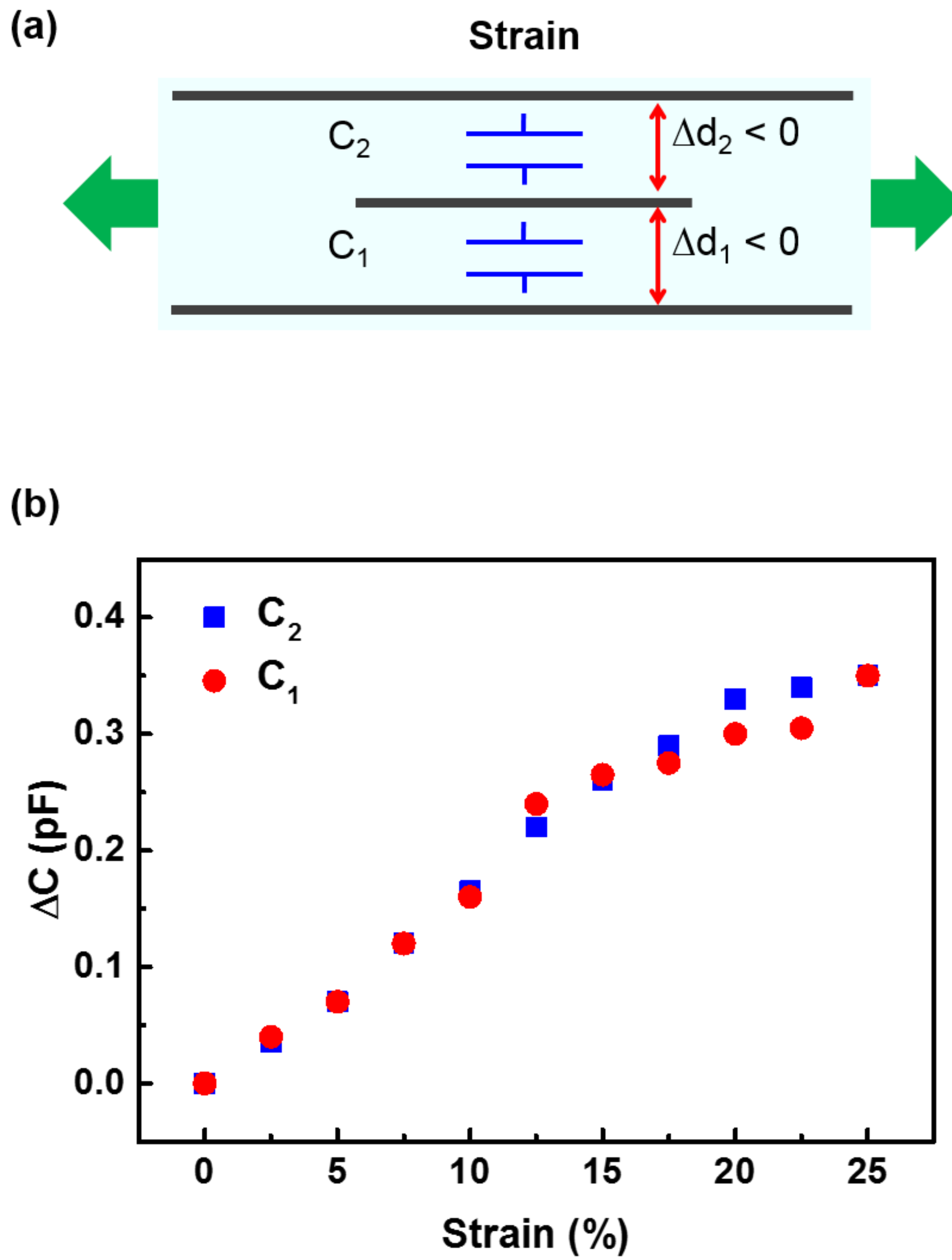


Figure A.8: (a) Schematic view of principle of strain sensing in dual-capacitor sensor. (b) The upper ($\Delta C_2$) and lower ($\Delta C_1$) capacitance changes according to applied tensile strain [23].

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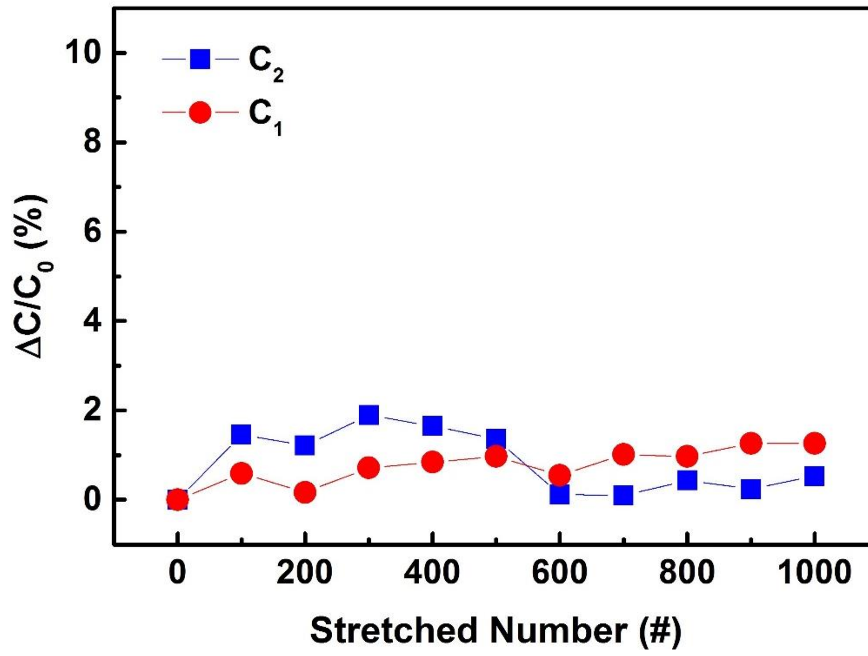


Figure A.9: The rate of upper ($\Delta C_2$) and lower ($\Delta C_1$) capacitance changes depends on the stretch and release cycle test [23].

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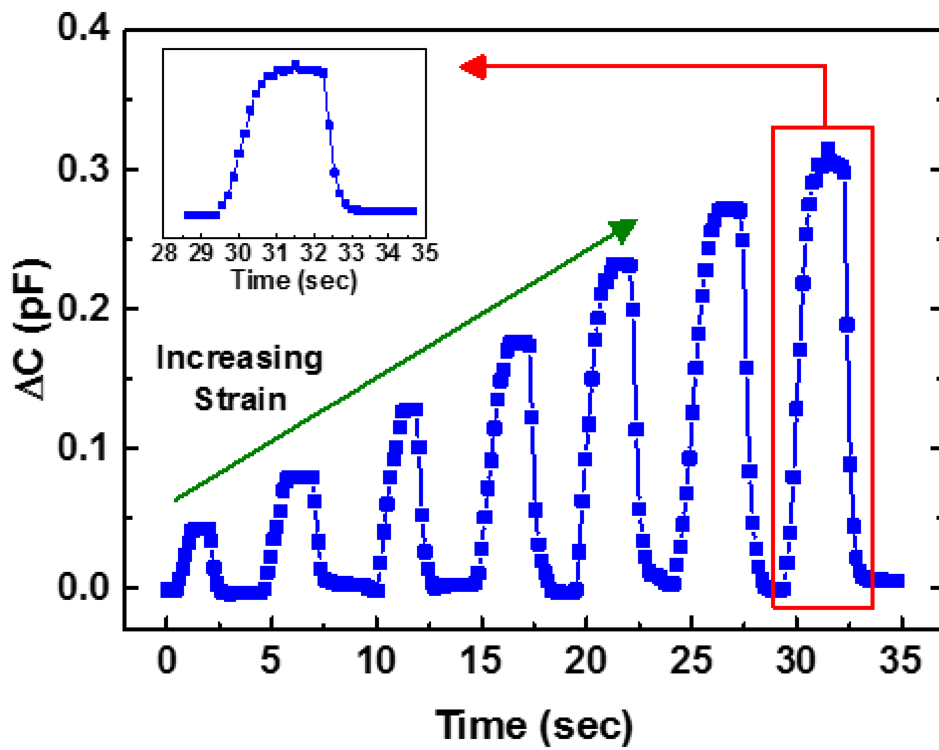


Figure A.10: The capacitance changes ( $\Delta C$ ) as function of time when stretching and releasing stimuli are applied [23].

### A.2.4 Touch Sensing

Unlike the curvature, pressure, and strain sensing modes, which use structural deformation of capacitor to detect changes in capacitance, touch sensing mode utilizes the redistribution of the fringing electric field lines [175]. When a finger (or a grounded conductive object) contacts the top surface of sensor, part of the fringing electric field lines existing in the insulating layers of two capacitors are grounded through the finger, resulting in the decrease of capacitance. Figure A.11(a) indicates the change of fringe electric field lines when the finger touches the upper surface of the dual-capacitor sensor. The upper capacitor close to finger loses more electric field lines than the lower capacitor, so $\Delta C_2$ (~19.0 %) is higher than $\Delta C_1$ (~15.5 %) as shown in Figure A.11(b). Touch sensitivity is also superior to other studies due to the thin protective layer [147, 148]. Thin protective layer reduces the gap between the touching finger and embedded sensor, which lead to more absorption of the fringing electric fields by finger touch. Therefore, the amount of change in capacitance becomes larger and the touch sensitivity increase.

## A.3 Clear Classification of External Stimuli

So far, we have found that our dual-capacitor sensor is able to sense stimuli of curvature, pressure, strain, and touch. In this section, we will demonstrate that the $\Delta C_1$ and $\Delta C_2$ values can be used to clearly distinguish the various sensing modes. This is really important for dual-capacitor sensors to be used as multiple sensor application. In curvature, pressure, strain, and touch sensing modes, the signs and magnitudes of $\Delta C_1$ and $\Delta C_2$ have unique combinations as shown in Table A.1. We can distinguish what external stimuli are applied based on $\Delta C_1$ and $\Delta C_2$ of the dual-capacitor sensor as shown in logical flow of Figure A.12. The applied physical stimuli are able to clearly distinguished into curvature, pressure, strain, or touch.

## A.4 Conclusion

In conclusion, the 5×5 array of stretchable multifunctional dual-capacitor sensor is fabricated by using AgNW electrodes and PDMS insulators and its curvature, pressure, strain, and touch sensing properties also demonstrated. Unlike the previously studied single-capacitor multifunctional sensor, our dual-capacitor sensor consisting of two vertically stacked capacitors cand detect both strength and surface-normal directionality of several external stimuli such as curvature, pressure, strain, and touch. The type of external stimulus can be unambiguously classified along a properly designed logic flow based on $\Delta C_1$ and $\Delta C_2$ of the dual capacitor sensor. Therefore, dual-capacitor sensors are expected to be used extensively in a variety of applications such as robots, medical monitoring systems, and Internet of Things (IoT).

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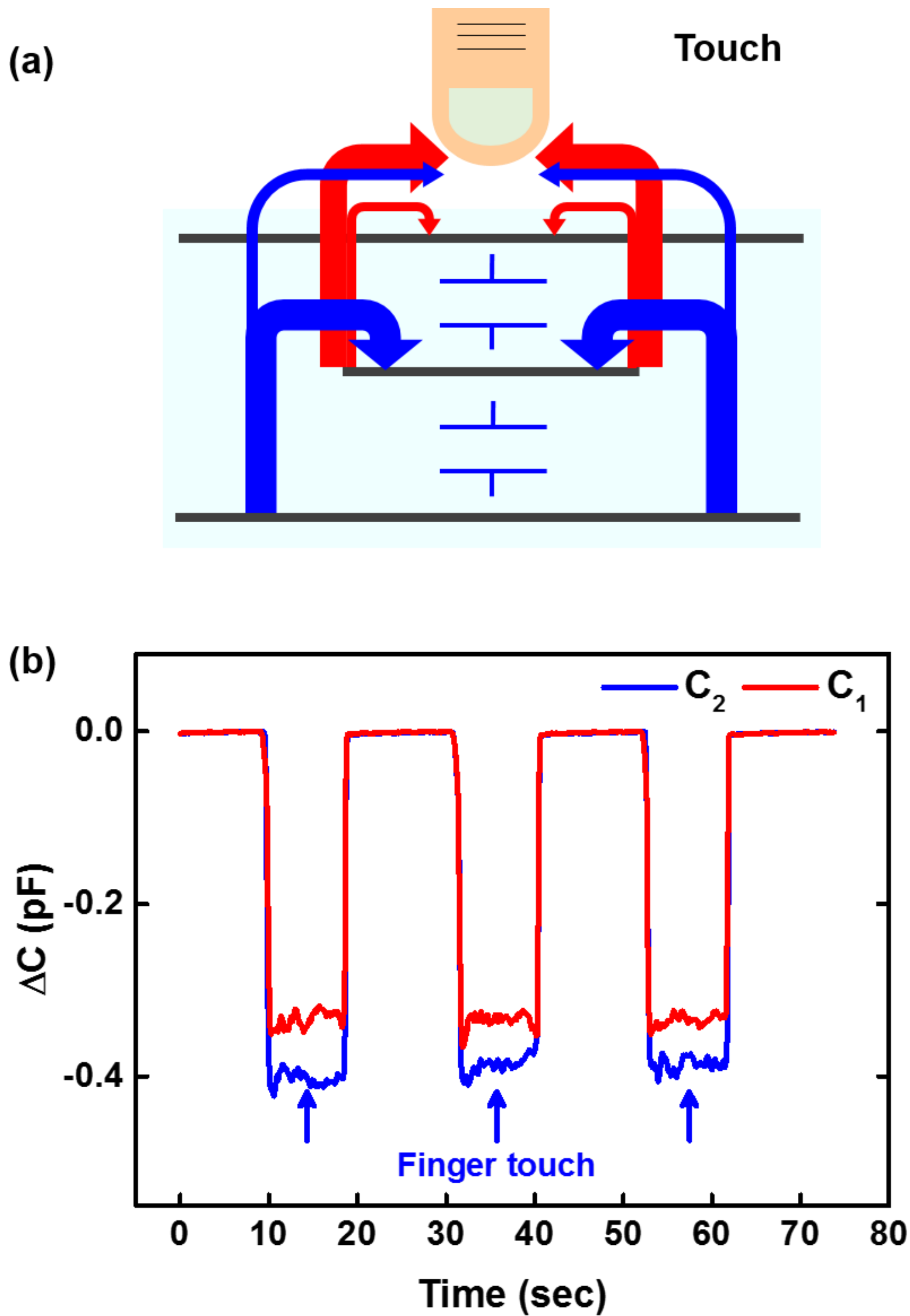


Figure A.11: (a) Schematic view of principle of touch sensing in dual-capacitor sensor. (b) The upper ($\Delta C_2$) and lower ($\Delta C_1$) capacitance changes *with* and *without* touch according to time [23].

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Table A.1: Summary of capacitances changes ( $\Delta C_1$ and $\Delta C_2$ ) for curvature, pressure, touch, and strain sensing modes [23].

| Sensing mode | Direction | Lower capacitor ($C_1$) | Upper capacitor ($C_2$) | $\Delta C_1$ vs. $\Delta C_2$ |
|---|---|---|---|---|
| Curvature | convex | $\Delta C_1 > 0$ | $\Delta C_2 > 0$ | $\Delta C_1 < \Delta C_2$ |
| | concave | $\Delta C_1 > 0$ | $\Delta C_2 > 0$ | $\Delta C_1 > \Delta C_2$ |
| Pressure | upper side | $\Delta C_1 = 0$ | $\Delta C_2 > 0$ | $\Delta C_1 < \Delta C_2$ |
| | lower side | $\Delta C_1 > 0$ | $\Delta C_2 = 0$ | $\Delta C_1 > \Delta C_2$ |
| Touch | upper side | $\Delta C_1 < 0$ | $\Delta C_2 < 0$ | $\|\Delta C_1\| < \|\Delta C_2\|$ |
| | lower side | $\Delta C_1 < 0$ | $\Delta C_2 < 0$ | $\|\Delta C_1\| > \|\Delta C_2\|$ |
| Strain | uniaxial | $\Delta C_1 > 0$ | $\Delta C_2 > 0$ | $\Delta C_1 = \Delta C_2$ |

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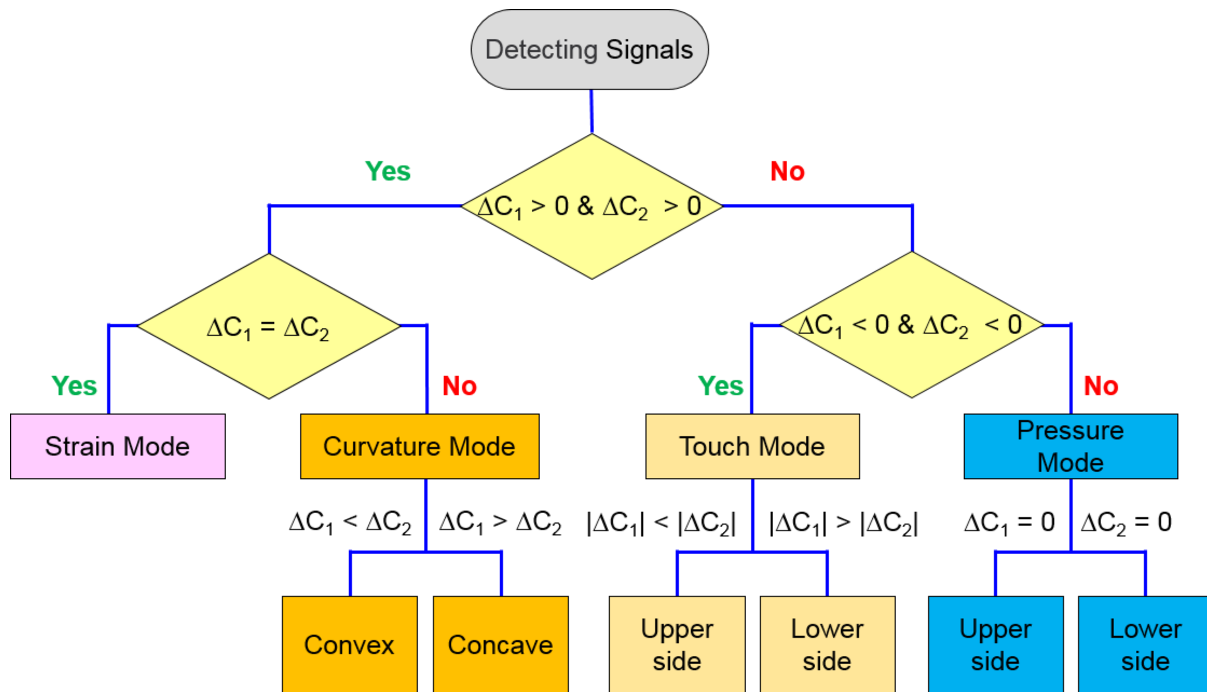


Figure A.12: Logical flow chart for classifying sensing modes from external stimuli [23].

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# APPENDIX B

## B. High Operational Stability of InAs Nanowire FET Achieved with Pre-Deposited All-around Gate Insulator

The semiconductor nanowire (NW) has been actively studied as potential materials for next-generation electronic devices because of its excellent material characteristics despite of nano size [176-181]. Since the structural and electrical characteristics such as composition, diameter, length, and doping concentration can be adjusted during nanowire growth, NWs can be easily manufactured to suit the application [182, 183]. Due to these advantages, NWs are used in a variety of applications such as FET [184, 185], photonic device [186-188], photodetector [92, 189, 190], chemical and biological sensor [191-194], and laser [195-198]. In particular, the InAs NW is widely used as a channel material of FET because of its high electron mobility [184, 185], and easy ohmic contact with various metals by strong Fermi-level pinning in conduction band [199, 200]. Various types of FET, such as wrap-gated FET [184, 201, 202], heterostructure FET [178, 203], tunnel FET [204, 205], and single electron transistor [206] have been studied by using InAs NW. The shape of the gate electrodes of the NW FET has a significant effect on the electrical characteristics of the device [185, 207]. The wrap-gated NW FET shows excellent device performance by applying the gate voltage to the entire surface of the NW channel [208]. However, the fabrication process is complicated. The top-gated NW FET has a slightly lower performance than wrap-gated NW FET [209-211], but the fabrication process is very simple [185, 207, 209, 212].

Here, we fabricated a high-performance pseudo-wrap-gated n-type InAs NW FET with significantly reduced process steps by forming a uniform $Al_2O_3$ thin film using ALD on the entire surface of the NW grown vertically on the Si substrate. Device processing is possible with a single metal deposition and photoresist coating, which can reduce fabrication costs and time. This oxide film also serves as a passivation for preventing deterioration of the device due to air exposure of the NW channel. The layer structure of the completed n-type InAs NW FET is investigated by cross-sectional high-resolution transmission electron microscopy (HRTEM) images. The fabricated n- type InAs NW FET demonstrates the stable operational performance with $\mu_{FE}$ of ~1039 $cm^2$/Vs at room temperature and current on/off ratio of ~750.

### B.1 Fabrication of n-InAs NW FET

The n-doped InAs NWs of single-crystal Wurzite structure in <111> direction formed by metal organic chemical vapor deposition (MOCVD) vertically on Si substrate are used. Figure B.1 indicates the SEM images of n-type InAs NWs, which has an average diameter of 150 nm and a length of 50 µm.

Figure B.2 shows the fabrication process on n-type InAs NW FET. The $Al_2O_3$ dielectric layer (10 nm)

is uniformly deposited on whole surface of n-type InAs NW channels formed vertically on the Si substrate by ALD at 250 °C, using TMA and $H_2O$ as precursors (Figure B.2(a) and (b)). The n-type InAs NWs covered with $Al_2O_3$ are dispersed in isopropyl alcohol (IPA) solution by ultrasonication for 10 secs and they are moved to $SiO_2$/Si substrate. The thickness of $SiO_2$ is 300 nm. (Figure B.2(c) and (d)). The photoresist is coated on the substrate, and the source and drain portions of AgNW are opened by UV irradiation. This sample is treated with buffered oxide etch (BOE) for 30 secs to eliminate oxide layers ($Al_2O_3$ and native oxide) and is immersed in ammonium polysulfide $(NH_4)_2S_x$ solution for 5 min to passivate with sulfur atoms which prevent post-oxidation (Figure B.2(e)) [213]. The $(NH_4)_2S_x$ solution is made by mixing concentrated 20 % ammonium sulfide $(NH_4)_2S$, sulfur, and $H_2O$ at a weight ratio of 1: 1: 9 at 40 °C. The sample is rinsed with DI water until $(NH_4)_2S_x$ solution is completely removed. Then, a gate pattern is formed using previously coated photoresist. (Figure B.2(f)) Finally, the contact pads are completed by depositing Cr/Au (10 nm/50 nm) metals and lift-off processes (Figure B.2(g)).

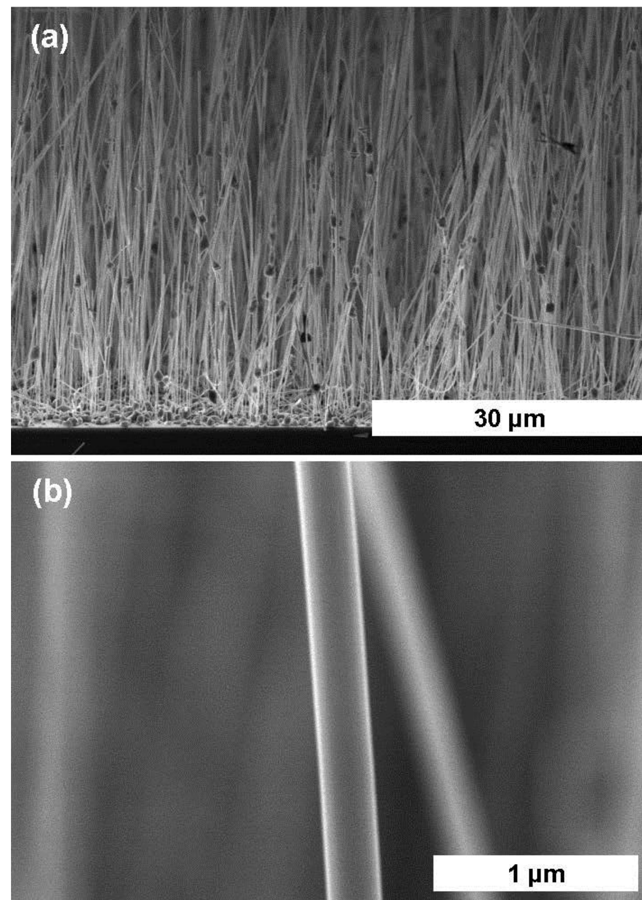


Figure B.1: SEM images of (a) n-type InAs NWs vertically formed on Si substrate and (b) enlarged n-type InAs NW having average diameter of 150 nm and length of 50 μm. [*in preparation*]

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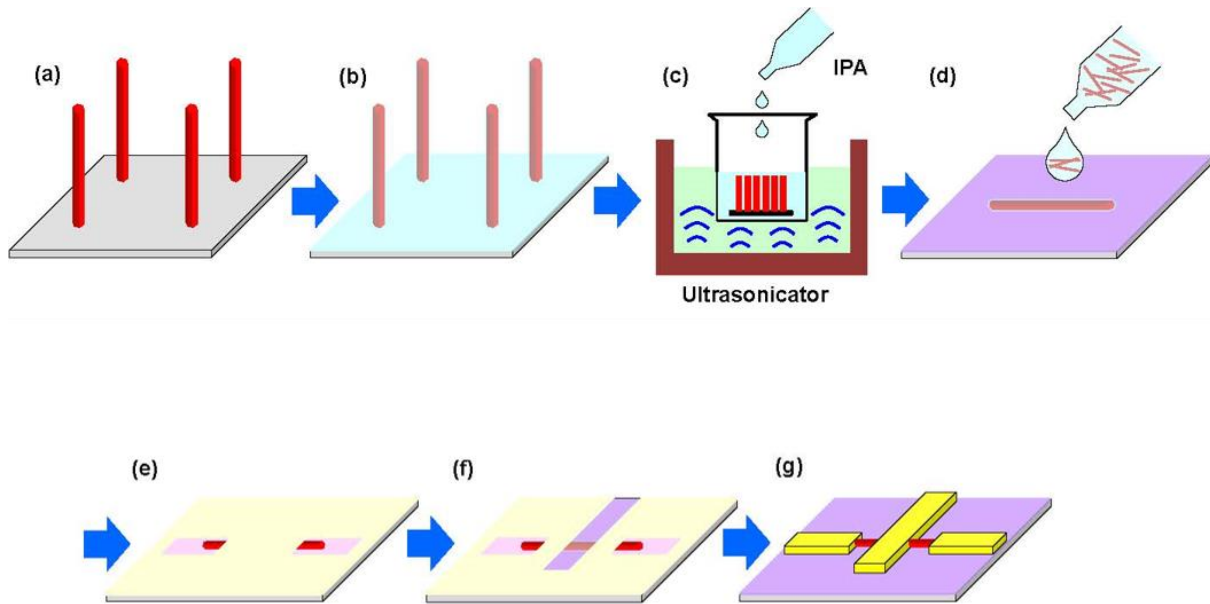


Figure B.2: The schematic views of a top-gated n-type InAs NW FET fabrication process. (a) Array of n-type InAs NWs vertically grown on Si substrate. (b) The whole surface of n-type InAs NWs is deposited with $Al_2O_3$ gate dielectric layer (10 nm) by ALD. $Al_2O_3$ coated n-type InAs NWs are (c) dispersed into IPA and (d) transferred on to $SiO_2$/Si substrate. (e) The source and drain points of n-type InAs NW are patterned by photolithograph for removing oxide layers and forming passivation layer using $(NH_4)_2S_x$ solution. (f) The patterning for gate electrode. (g) Formation of contact pads. [*in preparation*]

**B.2 High Resolution Transmission Electron Microscopy (HRTEM) Analysis**

Figure B.3(a) shows the photograph image of fabricated n-type InAs NW FET. The gate electrode (11 μm) is located between source and drain (33 μm). We can identify the n-type InAs NW in the yellow dotted circle line. After the red dotted line area is milled by focused ion beam (FIB), cross-section TEM images are obtained by the bright field TEM (BFTEM) and HRTEM images of milled area (Figure B.3(b) and (c)). The cross section of n-InAs NW is hexagonal and the plane length is ~ 75 nm. It has been confirmed that $Al_2O_3$ deposited using ALD is uniformly formed at a thickness of 10 nm on all surfaces of the InAs NW. The surfaces of the n-InAs NW coated with $Al_2O_3$ are surrounded by a gate metal except for the bottom surface contacted with substrate. The EDX electron mapping in Figure B.4(a)-(d) represents the InAs NW and the $Al_2O_3$ layer formed around it.

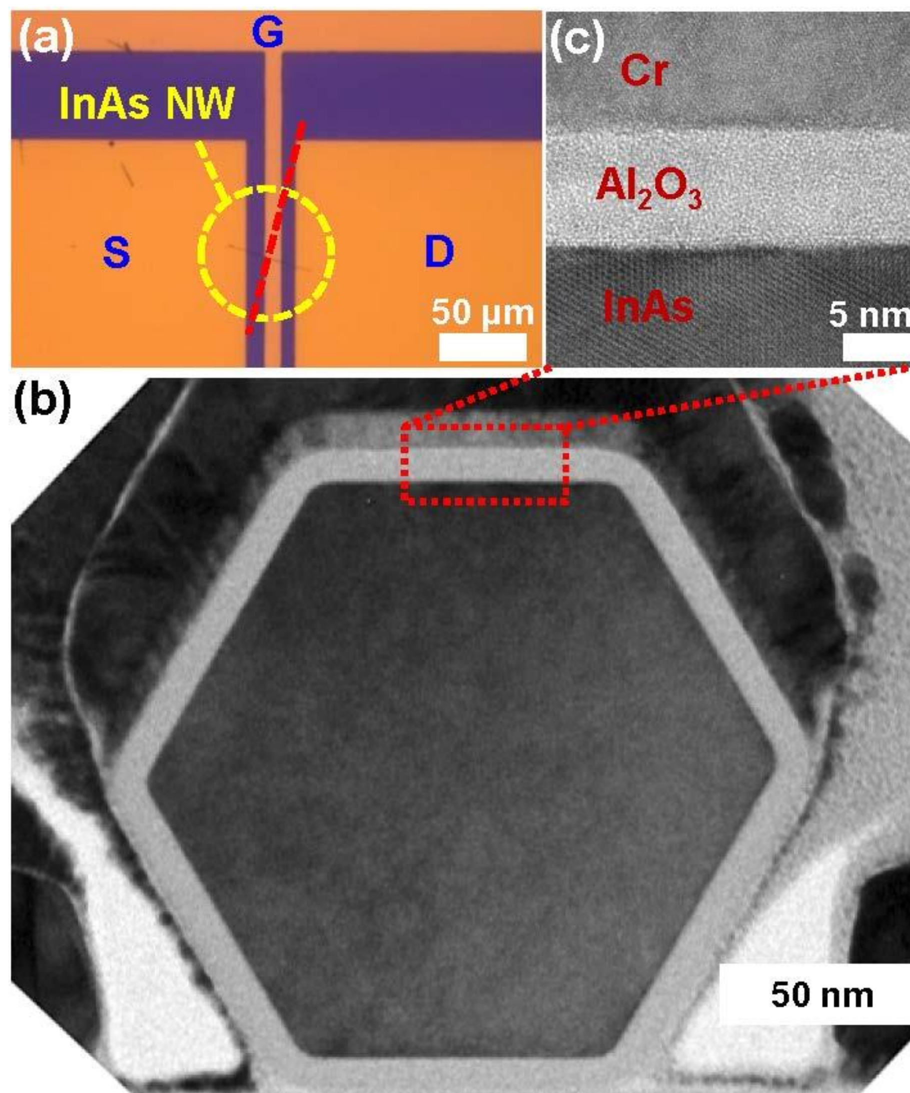


Figure B.3: (a) Microscope image of the completed n-type InAs FET. (b) Cross-sectional structure BFTEM image of the n-InAs NW FET device. (c) The HRTEM image of oxide interface region. [*in preparation*]

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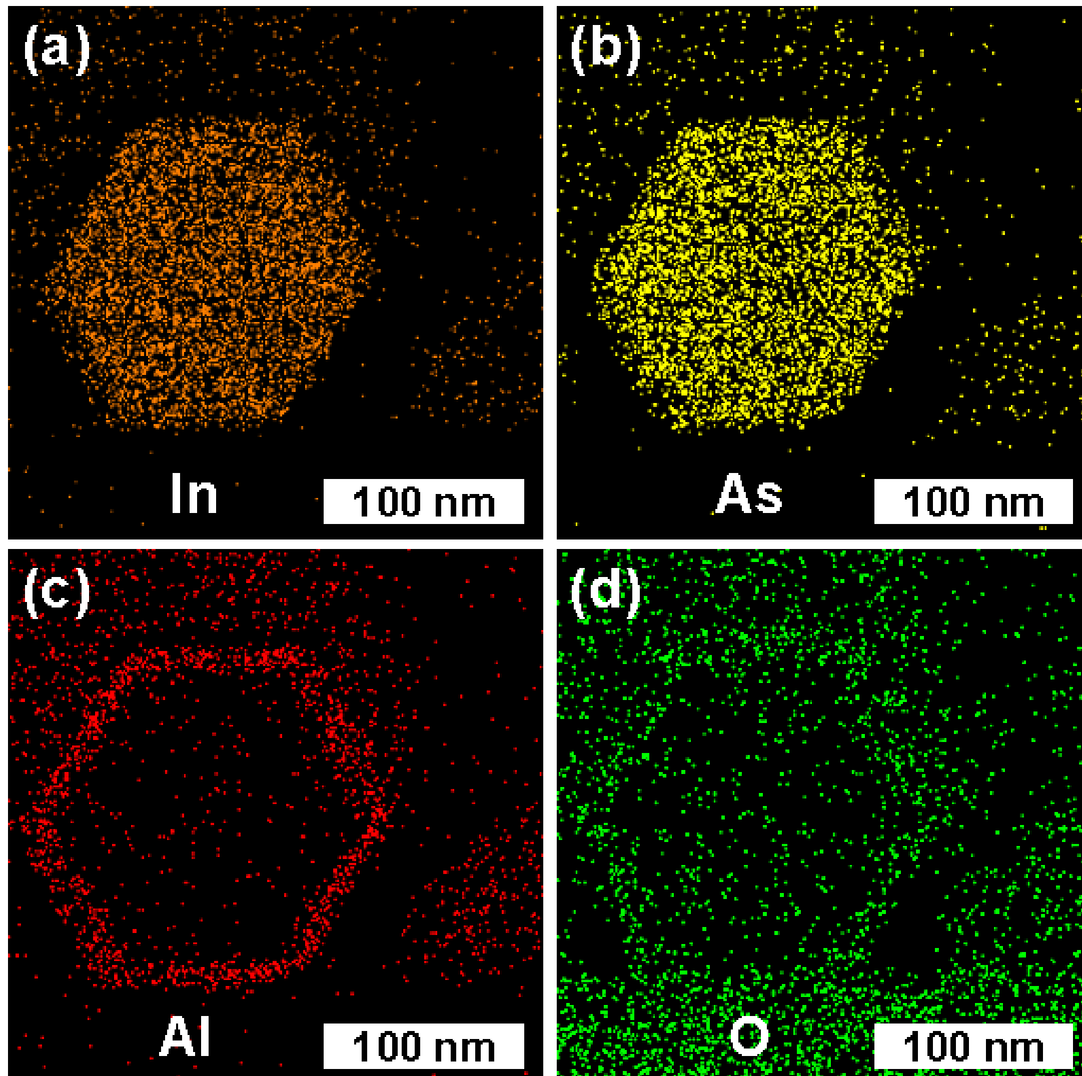


Figure B.4: EDX elemental mapping images of (a) In, (b) As, (c) Al and (d) O for fabricated n-type InAs NW FET. [*in preparation*]

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### B.3 Electrical Properties

Figure B.5 shows electrical properties of completed n-type InAs NW FET at room temperature. The fabricated device operates as an n-type MOSFET and exhibits excellent current saturation and low voltage operation. The drain current ($I_{DS}$) is measured at different drain voltages ($V_{DS}$) (from 0.1 V to 1.0 V with step of 0.1 V) according to gate voltage ($V_{GS}$) as shown in Figure B.5(a). Figure B.5b shows the $I_{DS} - V_{DS}$ curve at various $V_{GS}$ (-5 V to +5 V), where the linearity of graph indicates that ohmic contact has been formed between the InAs NW and the contact metals.

The transconductance ($g_m$) and field effect mobility ($\mu_{FE}$) are extracted from the $I_{DS} - V_{GS}$ curve. The $g_m$ is determined as $g_m = dI_{DS}/dV_{GS}$ at the maximum slope of graph. The $\mu_{FE}$ is defined as

$$\mu_{FE} = \frac{L_{ch} L_G g_m}{C_{ox} V_{DS}} \tag{B.1}$$

where $W_{ch}$ is the channel width and $C_{ox}$ is the gate oxide capacitance per unit area [214]. This equation is derived from the conventional 2D MOSFETs equation

$$\mu_{FE} = \frac{L_{ch} g_m}{W_{ch} C V_{DS}} \tag{B.2}$$

where $C$ is defined as $C = C_{ox}/W_G L_G$.

As shown in Figure B.3(b) and (c), the gate oxides cover five sides of the hexagonal n-type InAs NW with a thickness of ~10 nm. Thus, the $C_{ox}$ of our device can be defined as a general equation for a parallel plate.

$$C_{ox} = \frac{\varepsilon \varepsilon_o L_G W_G}{d} \tag{B.3}$$

where $\varepsilon$ is the insulating layer dielectric constant (6.0 for $Al_2O_3$), $\varepsilon_o$ is the vacuum permittivity, $W_G$ is the width of gate and $d$ is the gate oxide thickness. The highest value of $g_m$ is 13.4 mS/mm at $V_{DS}$ = 0.8 V and $V_{GS}$ = -1.4 V, the $\mu_{FE}$ is calculated to be ~1039 $cm^2/Vs$. The current on/off ratio is about ~750. The off-current for the $I_{DS} - V_{GS}$ curve is measured to be very low, from 1.01 to 0.014 pA at $V_{DS}$ = 1V. The threshold voltage ($V_T$) is calculated by linear extrapolation at the highest $g_m$ value as shown in Figure B.5(c). The $V_T$ of our device represents negative and is shifted according to $V_{DS}$. When $V_{DS}$ changed from 0.1 to 1V, the value of $V_T$ is changed from -2.73 V to -2.35 V.

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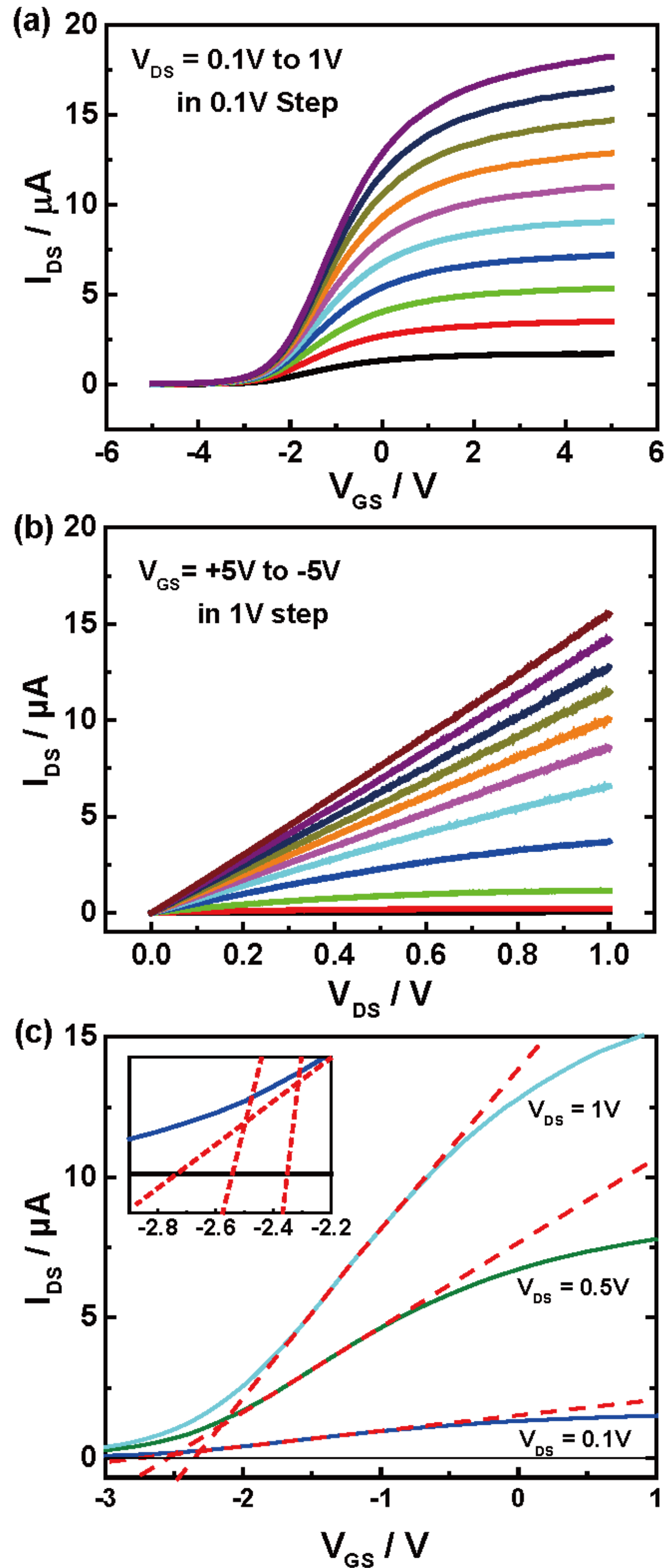


Figure B.5: (a) The $I_{DS}-V_{GS}$ curves at various $V_{DS}$ from 0.1 to 1 V with 0.1 V step. (b) The $I_{DS}-V_{DS}$ curves at range of $V_{GS}$ from +5 to -5 V with 1 V step. (c) Extraction of $V_T$ at the $V_{DS}$ = 0.1 V, 0.5 V and 1 V using linear extrapolation at the highest $g_m$ point. [*in preparation*]

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### B.4 Conclusion

We have successfully completed n-InAs NW FET with reduced fabrication process using pre-deposition of surrounding gate oxide. The $Al_2O_3$ layer of 10 nm thickness is deposited by ALD, it is used as a passivation layer as well as a gate insulator for the channel. All contact pads are formed with only one metal deposition and photoresist coating. The structural properties of completed device are confirmed by TEM images and EDX electron mapping. The surface of the n-type InAs NW is uniformly covered with $Al_2O_3$ and gate electrode deposited on all surfaces except for bottom surface of the InAs NW. A fabricated n-InAs NW FET shows good current saturation and low voltage operation, the peak $g_m$ is obtained to be 13.4 mS/mm, the $\mu_{FE}$ is calculated to be ~1039 cm$^2$/Vs at $V_{DS}$ = 0.8 V and current on/off ratio is about ~750.

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