Power-aware system-on-chip test scheduling using enhanced rectangle packing algorithm

Abstract :

The current semiconductor technology allows integration of all components onto a single chip called system-on-chip (SoC), which scales down the size of product and improves the performance. When a system becomes more complicated, testing process, such as test scheduling, becomes more challenging. Recently, peak power has also been considered as constraints in the test scheduling problem. Besides these constraints, some add-on techniques including pre-emption and non-consecutive test bus assignment have been introduced. The main contribution of each technique is the reduction of idling time in the test scheduling and thus reducing the total test time. This paper proposes a power-aware test scheduling called enhanced rectangle packing (ERP). In this technique, we formulate the test scheduling problem as the rectangle packing with horizontally and vertically split-able items (rectangles) which are smaller to fill up more compactly the test scheduling floor plan. Experimental results conducted on ITC'02 SoC benchmark circuits revealed positive improvement of the power-aware ERP algorithm in reducing total SoC test time.