Spring 5-28-1957

The Rating of a Power Type Transistor

Richard Lee Mann

POWER TYPE TRANSISTOR - MANN

NAME AND ADDRESS	DATE

THE RATINGS OF A POWER TYPE TRANSISTOR

A Thesis

Presented to

the Faculty of the Department of Electrical Engineering

University of New Mexico

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

---

by

Richard Lee Mann

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[illegible]

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This thesis, directed and approved by the candidate's committee, has been accepted by the Graduate Committee of the University of New Mexico in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

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MASTER OF SCIENCE

Date

Thesis committee

THE RATINGS OF A POWER TYPE TRANSISTOR

by
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Electrical Engineering Department
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TECHNICAL REPORT EE-2

Report No. 1 on Project 56-2EE

September, 1956

The work described in this report was performed under Sandia Corporation Purchase Order No. 53-4020.

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*This paper is also being used as a thesis in partial fulfillment of the requirements for the Degree of Master of Science in Electrical Engineering at the University of New Mexico.

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CHAPTER I

INTRODUCTION

The transistor, first publicly announced in June 1948, is an offshoot of the germanium crystal rectifier which played an important role in World War II in radar receivers. The germanium crystal rectifier had high-inverse-voltage characteristics which were lacking in preceding type rectifiers, thus making it the center of attraction of electronic interest. By adding an electrode to the crystal rectifier in order to control the surface charges, a new semi-conducting device, the "transistor" (TRANSfer resISTOR) came into existance.

Transistors are replacing electronic vacuum tubes in many applications since they are much smaller in size and weight and the power requirements are much less. They are capable of being used in circuits to provide amplification, oscillation, pulse generation, gating, and many other functions. The miniaturization of electronic equipment has even furthered the importance of the transistor. Great efforts are being made to extend the useage of transistors by increasing their current carrying capacity and useful frequency range.

The large transistors, which are very small compared with an equivalent tube, are referred to as power type transistors. While all transistors, in a general sense, are power transistors, they have been referred to as being capable of carrying 0.5 amperes or greater[1].

---

[1]LeRoy A. Griffith, Germanium Power Transistors (Minneapolis-Honeywell Regulator Company, Minneapolis 8, Minnesota, Transistor Division, paper dated February 9, 1955, TR73pl.)

CHAPTER I

INTRODUCTION

The transistor, first publicly announced in June 1948, is an offshoot of the germanium crystal rectifier which played an important role in World War II in radar receivers. The germanium crystal rectifier and high-back-voltage semiconductor [illegible] in preceding type results [illegible] is the center of much attention of electronic interest. In making an alteration in the crystal rectifier in order to control the current flowing, a new solid conducting device, the "transistor" (TRANSfer resISTOR) has been developed.

Transistors are replacing electronic vacuum tubes in many applications since they are much smaller, more rugged, and the power requirements are much lower.[1] They are capable of being used in circuits to provide amplification, oscillation, pulse generating, gating, and many other operations. The miniaturization of electronic equipment has been furthered with the development of the transistors. Great efforts are being made to expand the ranges of the transistors by increasing their current carrying capacity and their frequency range.

The large transistors [illegible], in very small compared with their equivalent tube, are referred to as power type transistors. While all transistors, in a general sense, are power transistors, they have been referred to as being capable of handling [illegible].

---

[1]LeRoy A. Griffith, "Germanium Power Transistor Development," Honeywell Regulator Company, Minneapolis [illegible] Transistor Division, paper dated February [illegible].

Like most new devices, the standardization of terms and ratings is a slow process. Manufacturing skills and methods are continually changing in an attempt to perfect a device which can be mass-produced with reasonably similar characteristics so that they will be interchangeable. The problem of interchangeability of power type transistors has not been solved as yet which makes transistor circuit design more difficult than tube circuit design. As this paper will show, the characteristics of a type transistor may vary widely from one transistor to another.

Ratings for a type of transistor are furnished by the manufacturer. These ratings are direct current ratings only and the characteristic curves furnished are typical characteristics which may be quite useless as far as a specific circuit design is concerned.

Sandia Corporation personnel have witnessed failures of transistors in their circuitry design due to what was thought of as being large amplitude current pulses of short time duration. In an effort to establish definitely the causes of these failures and the permissible limits of these pulses, a contract was negotiated with the University of New Mexico to do the research described in this paper.

The purpose of this paper, then, is to describe the tests performed and present the results obtained in an attempt to establish the maximum permissible direct current and pulse ratings for the type CTP-1003 (Clevite Transistor Products) power transistors under typical operating conditions. The manufacturer's specifications for the type CTP-1003 power transistor are located in Appendix A.

Like most new devices, the [illegible] of transistors is [illegible] a slow process. Transistors [illegible] and [illegible] are constantly changing in many ways, so that a [illegible] made one year can be made later with reasonably [illegible] characteristics so that they will be interchangeable. The problem of interchangeability of power transistors has not been solved [illegible] because transistor circuit design more difficult than that of [illegible]. As this paper will show, the characteristics of a power transistor may vary widely as the transistor is [illegible].

Ratings for a type of transistor are [illegible] by the manufacturer. These ratings are [illegible] only and characteristic curves furnished [illegible] the device may be quite useless as far as a specific circuit design is concerned.

Sandia Corporation [illegible] were experiencing difficulties with transistors in their circuitry design. One problem was [illegible] as being large amplitude current pulses of short time duration. In an effort to establish definitely the causes of these failures and the permissible limits of these pulses, a contract was negotiated with the University of New Mexico to do the research described in this paper.

The purpose of this paper, then, is to describe the tests performed and present the results obtained in an attempt to determine the maximum permissible direct current (and pulse current) for the CTP-1003 (Clevite Transistor Products) power transistor under typical operating conditions. The results from the examinations of the types CTP-1003 power transistor are included in [illegible].

Tests were performed at 165°F. ambient temperatures to establish the maximum permissible ratings (i.e., current, voltage, and dissipation or combinations of these quantities applied to any terminals of the transistor) over the active operating region of the transistor characteristics. Maximum permissible ratings are defined as those values at which the transistor may operate with good stability, long life and no irreversible changes in characteristics.

The effects of duty cycle, heat sink characteristics, spread of transistor properties, ambient temperature, and transistor connection on the ratings were established for

1. Ambient temperature: +165°F.
2. Duty cycle range: Pulse widths between 10 microseconds and 10 milliseconds; pulse repetition frequencies between 60 CPS and 2000 CPS.

Tests were performed [illegible], [illegible] to establish the maximum permissible ratings (i.e., current, voltage, and dissipation or combinations of these quantities applied to the terminals of the transistor) over the widest operating region of the transistor characteristics. Maximum permissible ratings are defined as those values at which the transistor may operate with good stability, long life and no [illegible] decrease in [illegible] characteristics.

The effects of [illegible] [illegible] such measurements [illegible] of transistor [illegible], ambient temperature, and [illegible] [illegible] [illegible] section on the results were evaluated [illegible]:

1. Ambient temperature [illegible]

2. Duty cycle [illegible] pulse [illegible] between [illegible] and 10 [illegible] pulse repetition [illegible] between [illegible] and [illegible]

CHAPTER II

THE METHOD OF TEST

I. PREPARATION OF TESTING

Each transistor was numbered with red paint such as, C-1. "C" for Clevite to distinguish from other transistors being tested in the laboratory.

Prior to all testing, the transistor was securely fastened to a 6" x 6" heat sink by 3 - #6 x 3/8" machine screws and placed in the temperature chamber and allowed to reach ambient temperature. A thermocouple (iron-constantan) was placed in a small groove cut in the heat sink just under the base of the transistor to measure the transistor temperature. Care was taken so that no air gap existed between the transistor and the heat sink. A picture was then taken of the transistor characteristics as the thermocouple passed through a temperature, ten degrees above ambiant temperature. This is necessary since the curve tracer, operating intermittently at two amperes or better (collector current), causes a heating of the transistor, thus changing the transistor characteristics.

II. TESTING PROCEDURE

Pulse testing at 165° F. This test was designed for the purpose of establishing the maximum permissible pulse ratings and the effects of duty cycle on the power transistor at 165° F. ambient temperature.

Pulse widths and repetition rates shown in Table I were used in establishing the maximum pulse ratings.

PART II

EXPERIMENTAL DATA

I. PRESERVATION OF TRANSISTORS

Each transistor was subjected to the pulse test as [illegible] "C" for Glenite to distinguish them from transistors being tested in the laboratory.

Prior to all testing, the transistor was mounted [illegible] a 5" x 6" heat sink by 1-72 nylon machine screws and [illegible] in the temperature chamber and allowed to reach chamber temperature. A thermocouple (iron-constantan) was placed in a small groove cut in the heat sink just under the base of the transistor to measure the transistor temperature. Care was taken to [illegible] between the transistor and the heat sink. A picture was then taken of the transistor characteristics on the [illegible] at a temperature, ten degrees above ambient temperature. This is necessary since the curve tracer, operating [illegible] or better (collector currents), causes heating of the transistor, thus changing the transistor characteristics.

II. TESTING PROCEDURE

Pulse testing at 200° F. This test was designed for the purpose of establishing the maximum permissible pulse ratings and the effects of duty cycle on the power handling of [illegible]

Pulse widths and repetition rates given in Table I were used in establishing the maximum pulse ratings.

TABLE I

PULSE WIDTHS AND REPETITION RATES

Repetition Rates, CPS	60	200	600	2000
Pulse Widths in Microseconds	10	10	10	10
	100	100	100	100
	1000	1000	1000	---
	10000	----	----	---

The pulse widths in Table I at a given repetition rate was applied to the base of the transistor connected common emitter. The pulse amplitude was then varied in steps from a minimum value to a value which destroyed the transistor. The size of the pulse steps was decreased as the temperature of the transistor increased. The amplitude of the collector pulse was held constant until a constant transistor temperature was maintained prior to advancing to the next step. Continuous observation of the input and output pulses, transistor and ambient temperatures was made throughout the pulsing test.

Where feasible, at least one transistor was made to fail at each of the above repetition rates and pulse widths by increasing the pulse amplitude. Where time allowed, not less than five transistors were pulsed at each repetition rate and pulse width and they were pulsed where possible beyond the point where failure existed on the preceding transistor. The transistor characteristics were checked against the original characteristics whenever there was any indication of an unusual change in output or sharp temperature change. Figure 1

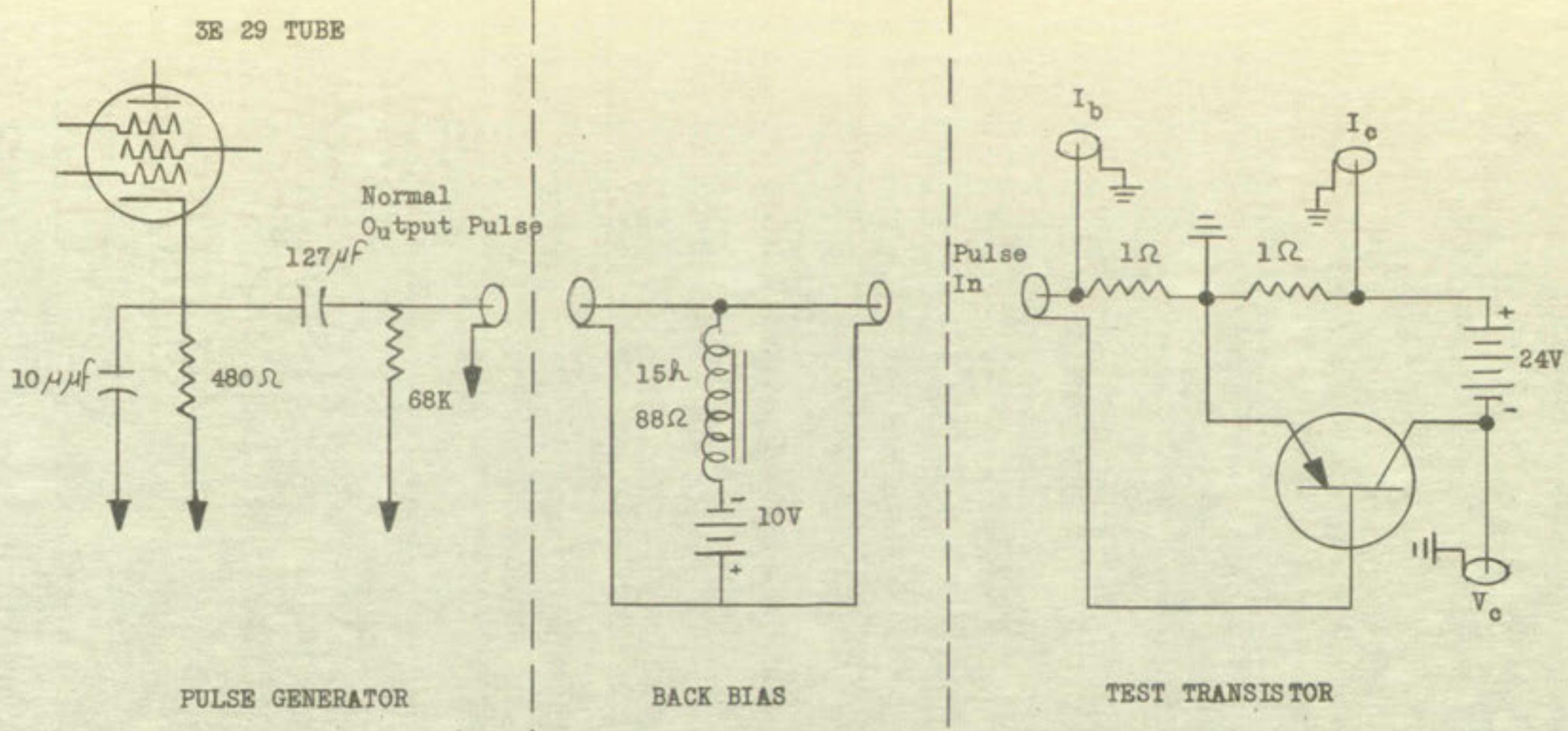
TABLE I

[illegible]

Repetition Rate, CPS	[illegible]	[illegible]	[illegible]	[illegible]
Pulse Widths	[illegible]	[illegible]	[illegible]	[illegible]
Microseconds	[illegible]	[illegible]	[illegible]	[illegible]

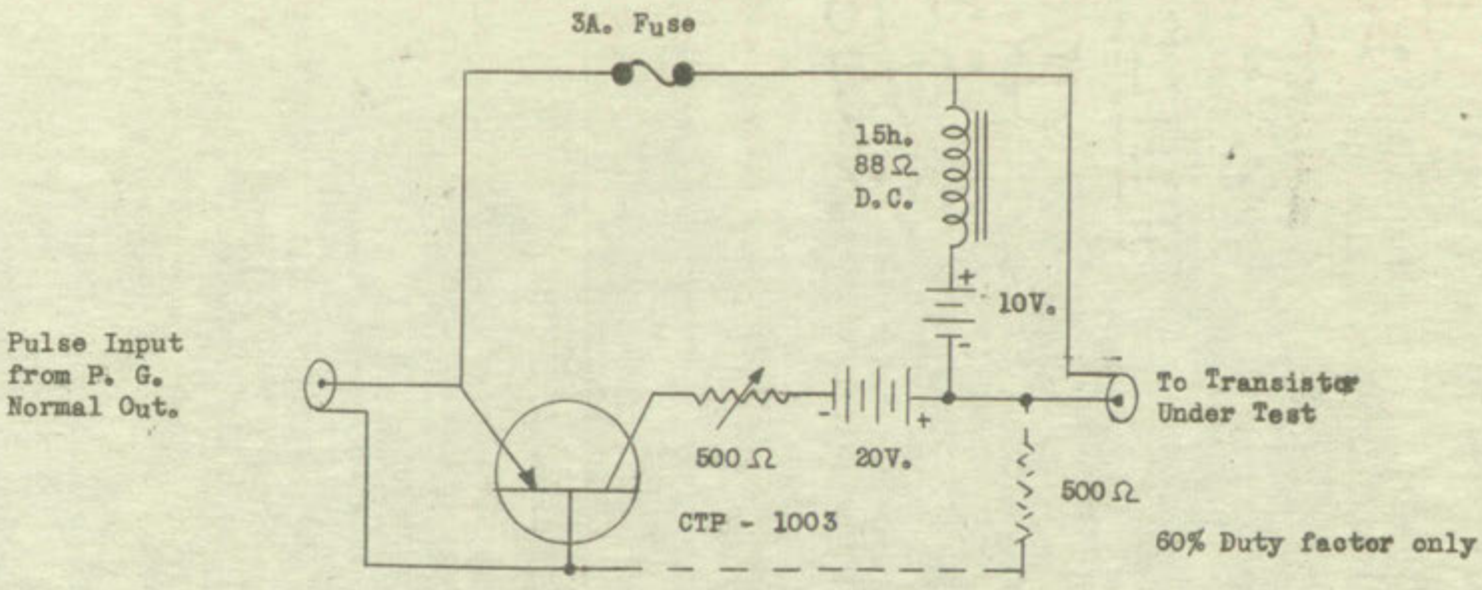
The pulse widths in Table I were first [illegible] applied to the base of the transistor connected common emitter. The pulse amplitude was then adjusted upward from [illegible] to a value which destroyed the transistor. [illegible] of the pulse [illegible] was decreased as the temperature of the transistor increased. The amplitude of the applied pulse was held constant until a [illegible] transistor temperature was maintained prior to adjusting to the next step. Continuous observation of the input and output pulses, transistor and ambient temperature was made throughout the [illegible].

Where feasible, at least [illegible] transistors were made to fail at each of the above repetition rates and pulse widths by increasing the pulse amplitude. [illegible] allowed [illegible] that [illegible] transistors were pulsed at each repetition rate and pulse width and [illegible] were pulsed [illegible] the preceding [illegible] against the [illegible] of an [illegible]



PULSE TEST CIRCUIT

Figure 1



AMPLIFIER & BACK BIAS STAGE

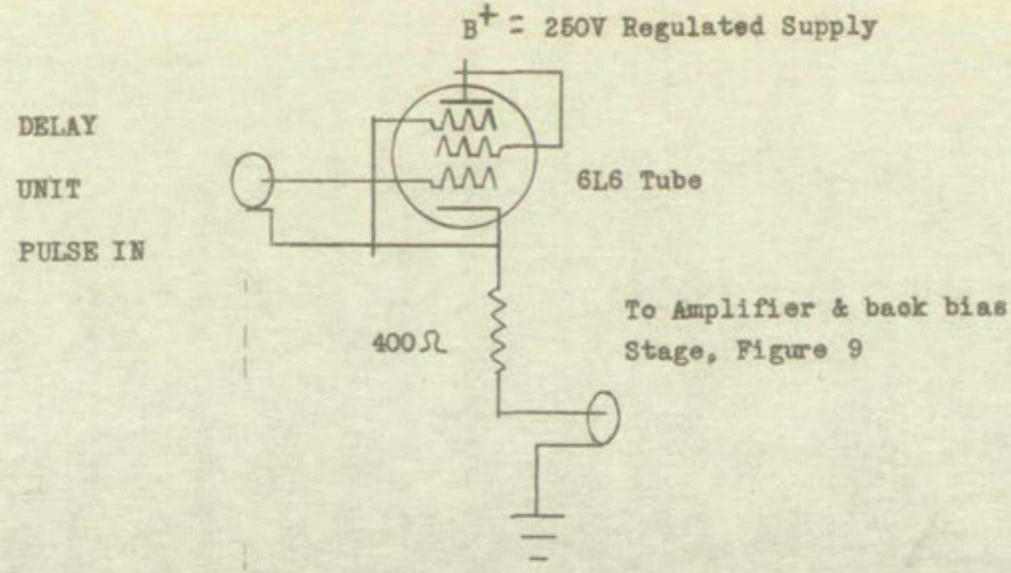
FIGURE 2

shows the pulse testing circuit. In order to obtain greater pulse amplitudes for the 100 microsecond pulses and larger, a transistor stage of amplification was used. This circuit is shown in Figure 2.

The pulse generator's normal output pulse is limited to twenty-five percent duty factor. Where the duty factor exceeded this rating, pulses were taken from the delay unit of the pulse generator. The dash line and 500 ohm in Figure 2 shows the positive feedback circuit required for the sixty percent duty factor pulses. This feedback circuit eliminates the deleterious signals between the 250 volt power supply ground and the oscilloscope ground which caused a distorted signal in the test circuit. Figure 3 shows an interstage of amplification required for the sixty percent duty factor pulses.

Direct current test at 165° F. This test is designed for the purpose of establishing the maximum D. C. power rating of the power transistor. In the circuit shown in Figure 4, the collector voltage and current was varied until the failure point was reached. In this case, the base circuit is open. Transistor and ambient temperatures were recorded at each step. Using the circuit in Figure 5, I_b (base current) was held at 200 milliamperes while V_c and I_c were varied until failure. Five randomly picked transistors were used for each of these tests. V_c was measured by a calibrated oscilloscope and I_b and I_c by laboratory instruments.

Heat sink characteristics at 165° F. This test was designed to establish the effects of the heat sink on the power ratings of the transistor.



60% DUTY FACTOR CIRCUIT

FIGURE 3

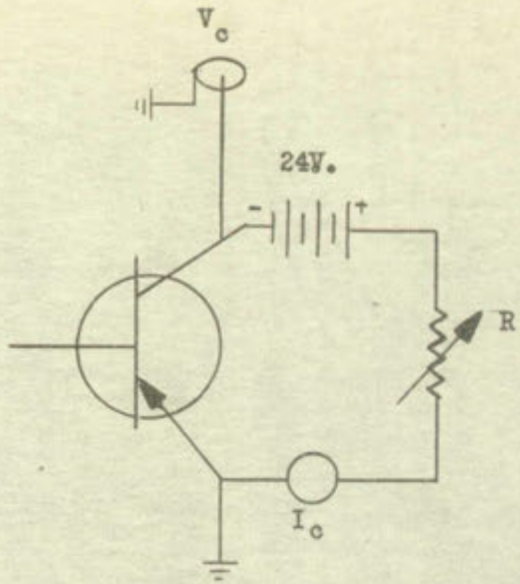


FIGURE 4

D. C. Test - I_b = 0

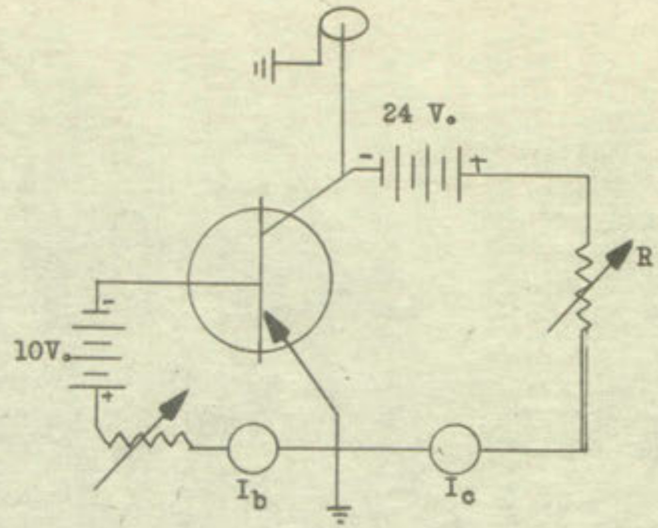


FIGURE 5

D. C. Test - I_b = 200 ma.

The heat sinks for this test were made from AN-A-13 Alclad, S-T 24 Alcoa Aluminum, .064" thick. Three sizes of heat sinks were used: (1) 3" x 3", (2) 4 1/4" x 4 1/4", and (3) 6" x 6". The circuit in Figure 4 was also used for this test. Three sets of data were taken for each heat sink using a different transistor for each set of data. Heat sink characteristics were also taken at room temperature.

The heat shields for these tests were made from [illegible] 24S-T Alclad aluminum, [illegible]. Three sizes of heat shields were used: (1) 3" x [illegible], (2) [illegible], and (3) [illegible]. The circuit in Figure 5 was used [illegible] temperatures [illegible] were taken for each test [illegible] thermocouple for each set of data. [illegible] were all [illegible] at room temperature.

CHAPTER III

THE DESCRIPTION OF THE TEST EQUIPMENT

I. TEMPERATURE CHAMBER

An electric oven, 9 1/2" x 11 1/2" x 9 1/2", thermostatically controlled, manufactured by Schaar & Company was used for the temperature chamber. A few additions were made to the original oven: (1) an aluminum sheet, 0.40" thick, was placed above the heating elements to diffuse the heat, (2) a four-inch cage type fan was placed on the rear wall of the chamber to circulate the heat in effort to prevent hot spots, (3) two strands of asbestos covered wire spaced four inches apart were suspended 3 1/2" from the top of the chamber as supports for the heat sink containing the transistor under test, (4) coaxial receptacles and metering resistors were installed on the outside surface of the oven, and (5) the interior was wired with 50 ohm coax cable, all wiring being as short as possible and free from sharp bends.

Two mercury type, 30 - 180° F. thermometers, designated by X_1 and X_2, and three iron-constantan thermocouples, designated by T_2, T_3, and T_4 were used for measuring the ambient temperature. Figure 6 shows the location of these temperature measuring devices. A potentiometer calibrated for 0-400° F., was used in obtaining the thermocouple temperatures.

During a test, the thermostat was adjusted so that thermometer X_1 maintained a reading of 165° F. ± 1° F. The thermocouple T_1 located in a groove cut in the heat sink just under the base of the transistor,

APPENDIX [illegible]

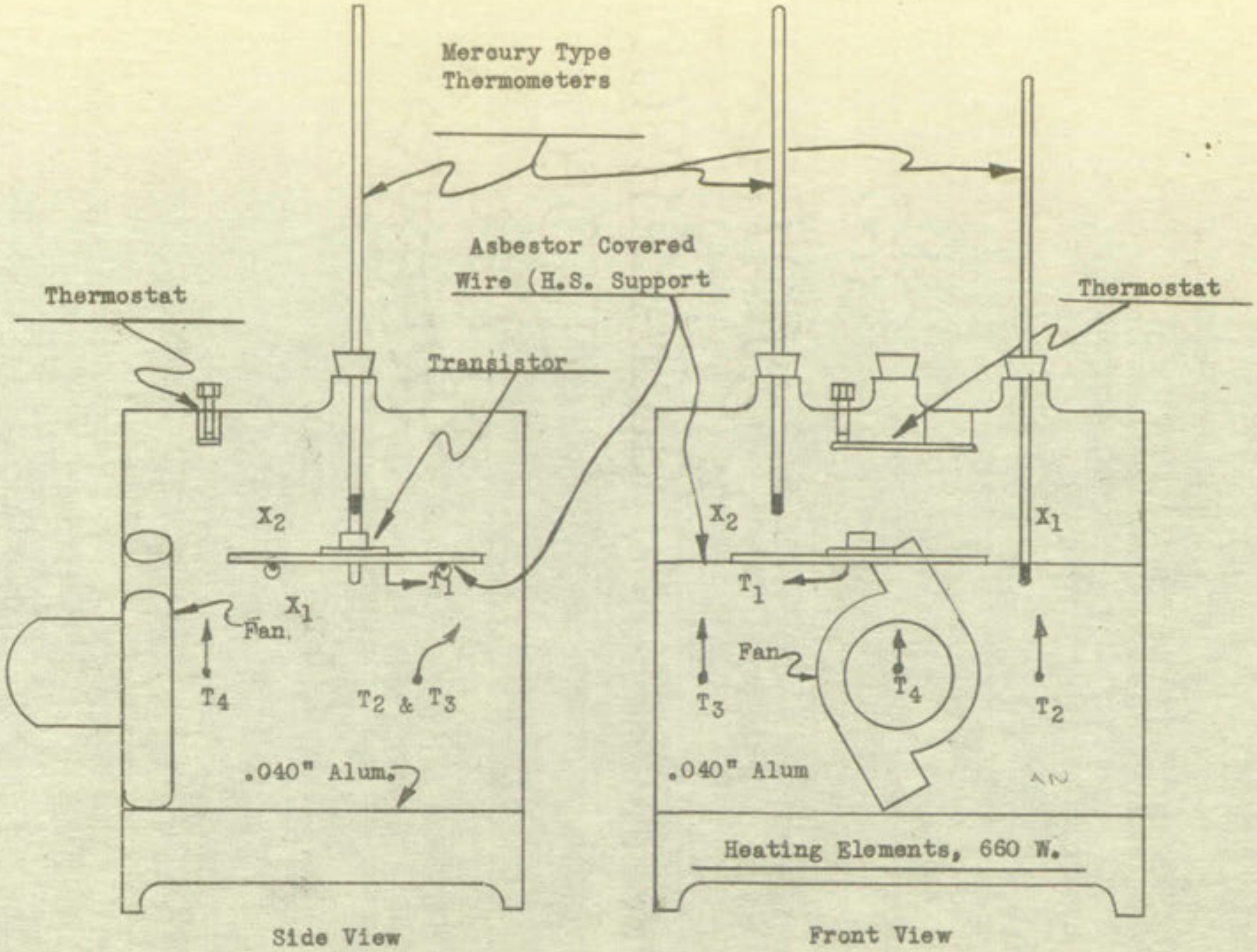
THE HEAT FLOW OF THE [illegible]

[illegible]

An electric oven, [illegible] thermostatically controlled, manufactured by [illegible] was used for the [illegible] above chamber. A few additions were made to the [illegible] an aluminum sheet, [illegible] was placed over the [illegible] to diffuse the heat, [illegible] rear wall of the chamber [illegible] spots, (3) two strands of [illegible] apart were suspended [illegible] for the heat sink [illegible] receptacles and [illegible] face of the oven, and (5) the [illegible] cable, all wiring [illegible]

Two mercury [illegible] and M_2, and three [illegible] and T_3 were used for [illegible] the location of these temperature measuring devices. [illegible] calibrated for [illegible] T_1, was used to [illegible] atures.

During a test, the thermostat was adjusted so that thermometer M_1 maintained a reading of [illegible] in a groove cut in the [illegible]



Scale 1/4" = 1' - 0"

165° F. TEMPERATURE - (Figure 6)
CHAMBER (Interior)

was employed to read transistor temperature.

The following shows the temperatures at the various locations inside the temperature chamber in a typical case:

Prior to test

X_1 = 165° F. X_2 = 161° F. T_1 = 169° F.

T_2 = 177° F. T_3 = 171° F. T_4 = 176° F.

While the transistor is dissipating 135 watts peak power at a duty cycle of six percent

X_1 = 165° F. X_2 = 164° F. T_1 = 206° F.

T_2 = 175° F. T_3 - 176° F. T_4 - 177° F.

Figure 7 shows the temperature chamber in operation, except the door is open to display the interior. The metering resistors on the exterior of the chamber are the non-inductive type (Koolohm) used in measuring the collector current and base current by using a calibrated oscilloscope.

II. EQUIPMENT FOR OBTAINING TRANSISTOR CHARACTERISTICS

The equipment used in obtaining the characteristics of the transistor is shown in Figure 8. A block diagram, Figure 9, is a general circuit description of this equipment. Figure 10 shows three sets of curves describing the transistor characteristics with the transistor connected common emitter. These curves were displayed on the face of the cathode ray tube and photographed with a polaroid land camera. The circuitry used in building the transistor characteristics curve tracer is shown in Figure 11.

was employed to read temperatures in degrees.

The following shows the temperature where the resistors [illegible] inside the temperature chamber [illegible]:

Prior to [illegible]:

T_1 = 105° F [illegible] T_3 = 123° F

T_2 = 117° F [illegible]

While the transistor is dissipating [illegible] peak at a duty cycle of six percent

T_1 = [illegible] T_2 = [illegible] T_3 = [illegible] F

T_4 = 115° F [illegible]

Figure 7 shows the temperature chamber in operation [illegible] the door is open to display the apparatus. The [illegible] on the exterior of the chamber are the controlling [illegible] used in measuring the collector current and [illegible] by using a calibrated oscilloscope.

11. EQUIPMENT FOR OBTAINING [illegible] CHARACTERISTICS

The equipment used in obtaining the curves [illegible] of the transistor is shown in Figure 8 [illegible] Figure 9 [illegible] general circuit description of this equipment. Figure 10 shows [illegible] of curves describing the [illegible] connected common emitter. These curves were [illegible] the cathode ray tube and [illegible] The circuitry used [illegible] transistor is shown in Figure 11.

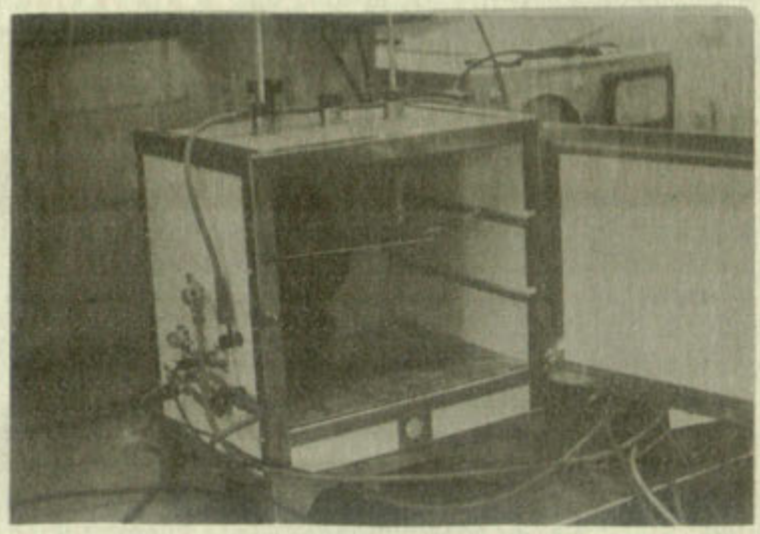


FIGURE 7

TEMPERATURE CHAMBER

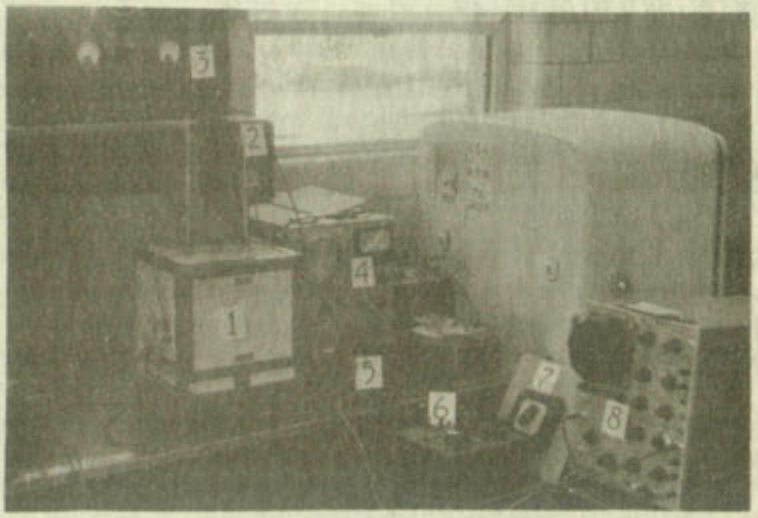


FIGURE 8

TEMPERATURE CHAMBER AND CURVE TRACER EQUIPMENT

1. Oven, electric.
2. Collector voltage supply (Battery Booster 6-12 volt).
3. Power Supply, D. C., 300 volt regulated, 250 milliampere capacity.
4. Step generator (Tektronix type 570 curve tracer).
5. Chassis, terminating including 6L6 cathode variable 500 ohm resistor and metering resistors for taking characteristics at room temperature.
6. Potentiometer, temperature measuring, direct reading 0-400° F.
7. Switch, 8 point multiple for use with the potentiometer.
8. Oscilloscope, (Tektronix type 545).

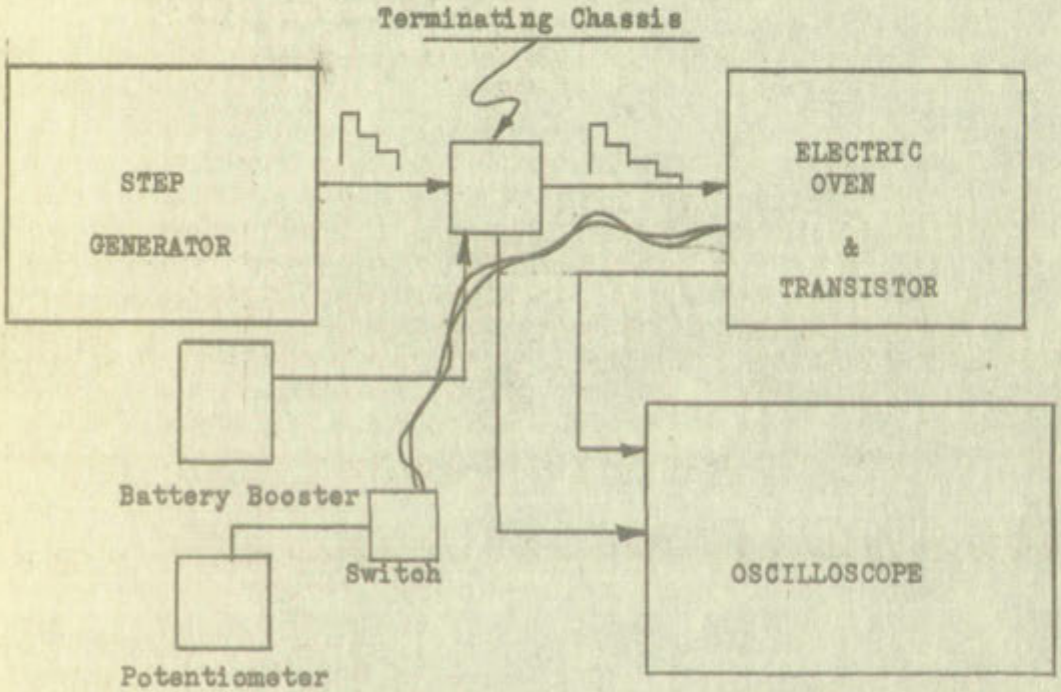
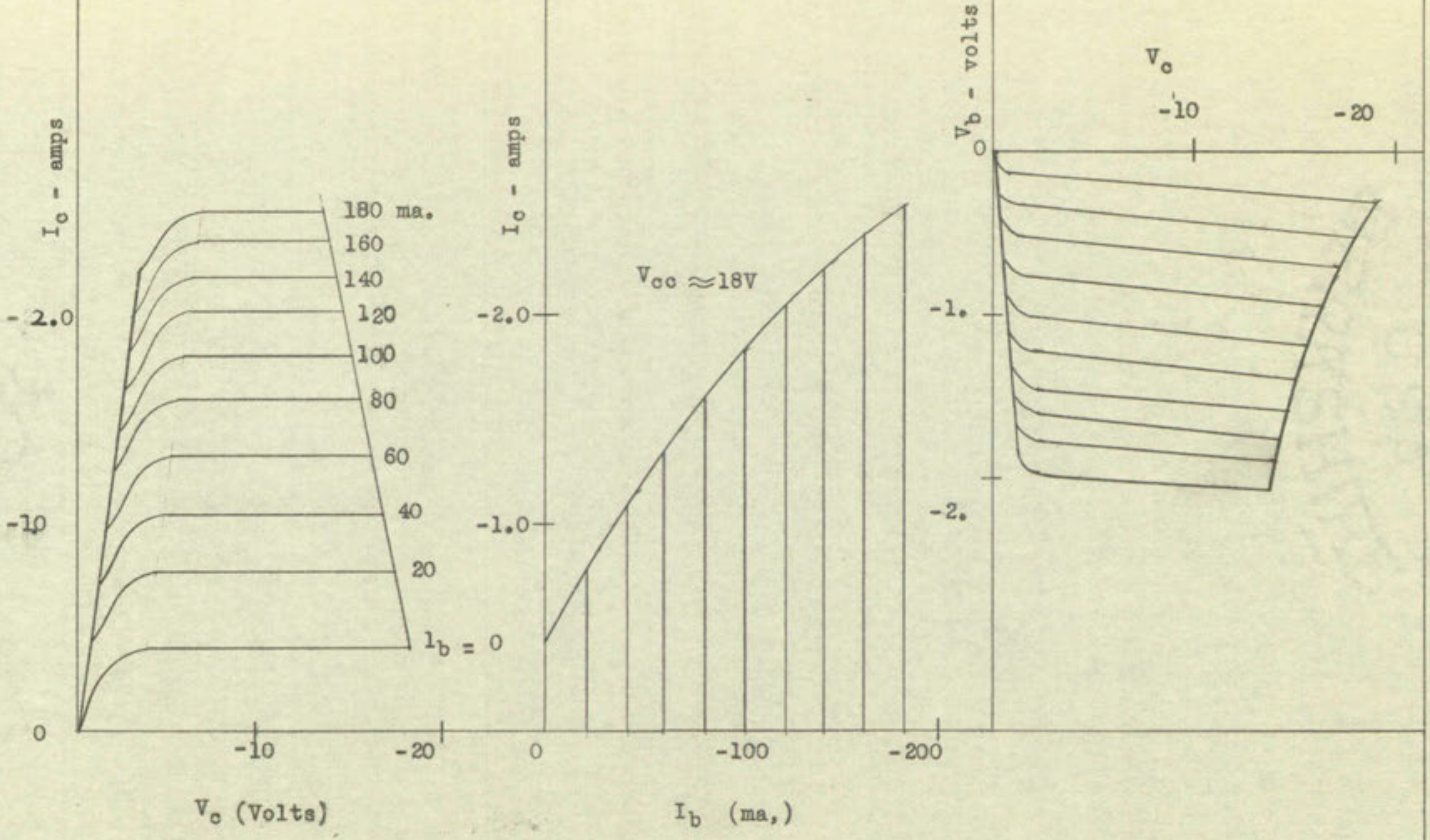


FIGURE 9
CIRCUIT DESCRIPTION OF THE
TRANSISTOR CHARACTERISTIC
EQUIPMENT



TRANSISTOR CHARACTERISTICS

FIGURE 10

R_1 = Resistor, 0-500 Ohm for Var ying steps

R_2 = 5 Ohm, 5 Watt non-inductive for meter-bass current.

R_3 = 1 Ohm (4 ea. 4 Ohm, 5 Watts) noninductive metering Collector Current.

V_{cc} = Rectifier, full wave 18 volt peak (Battery Booster 6--12 Volt.

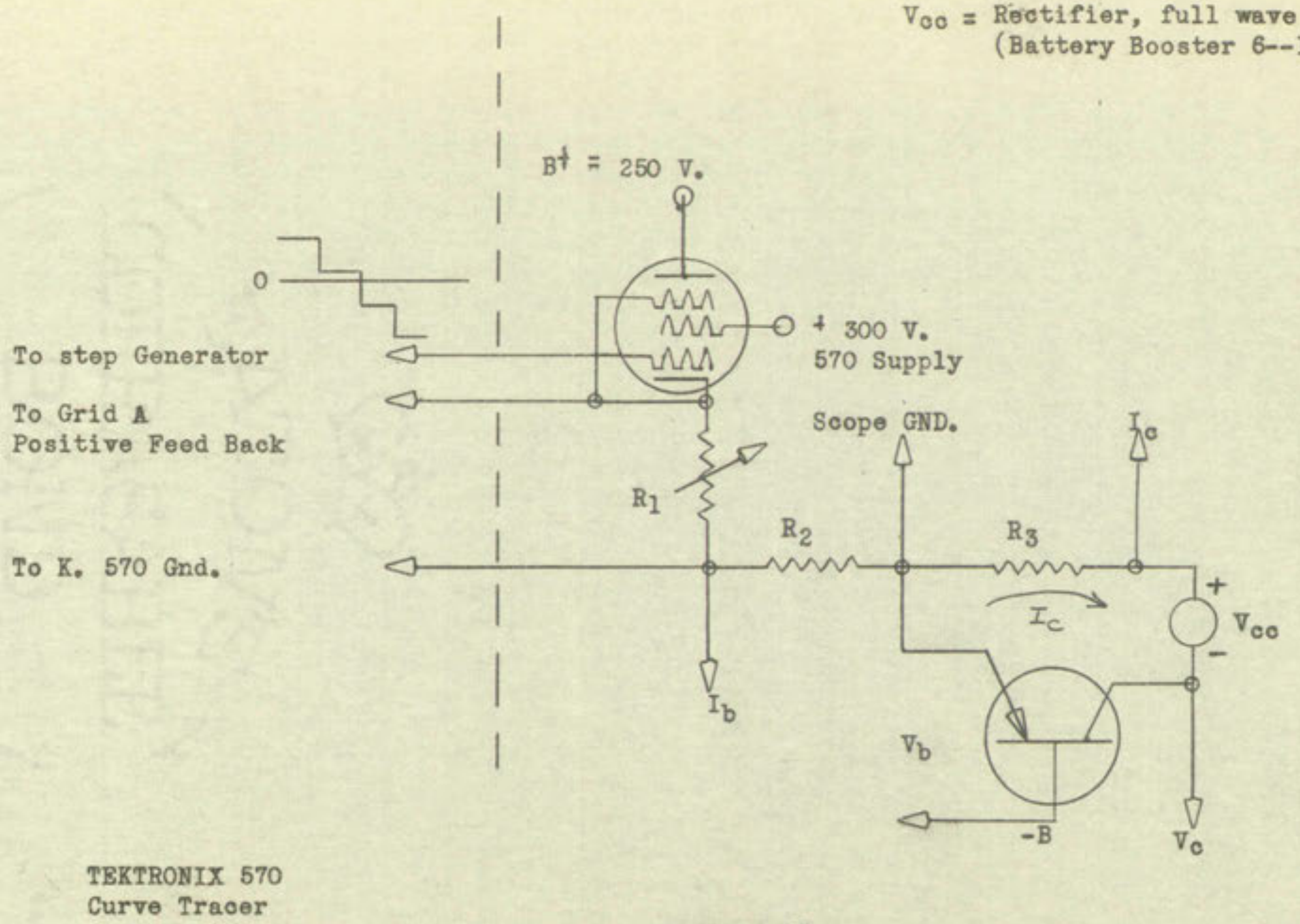


FIGURE 11
CURVE TRACER CIRCUIT

Theory of the Curve Tracer Circuit (General). Voltages of equal steps are impressed on the grid of the 616 tube, thus causing constant current steps in the base circuit of the transistor. A sweeping voltage of 18 volts, is impressed on the collector circuit. The base current steps are 1/120 second in duration but timed so that the step comes during the time that the collector voltage is a maximum or the change of collector voltage $\frac{dV_c}{dt}$ is a minimum and the fall time of the current steps are not so critical. Figure 12 shows this time relationship of the base current, collector voltage and the collector current.

III. PULSE TESTING EQUIPMENT

The overall pulse testing set up is shown in Figure 13 and a general description of the pulse testing circuit is shown in Figure 14.

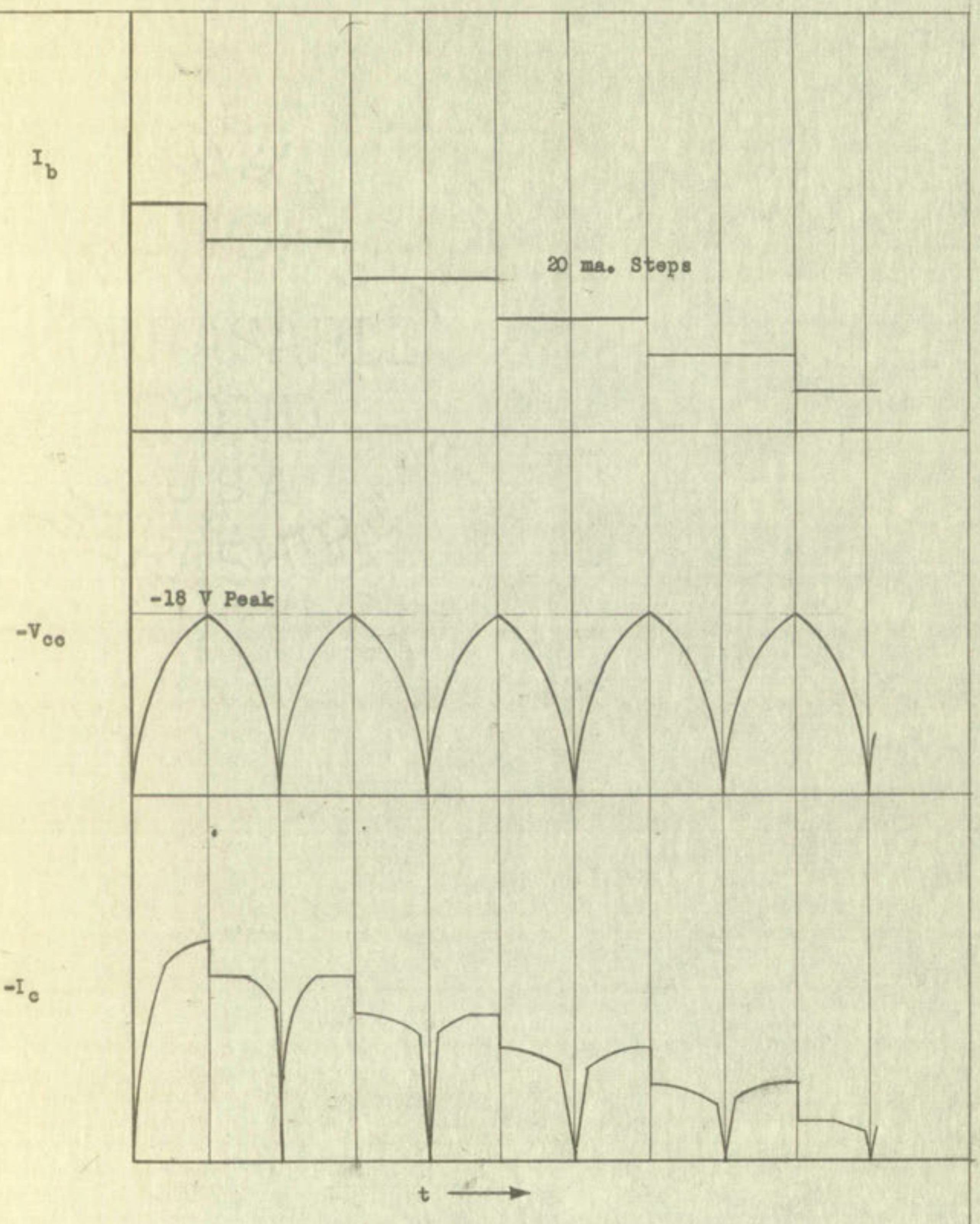


FIGURE 12

WAVEFORM-TIME RELATIONSHIP

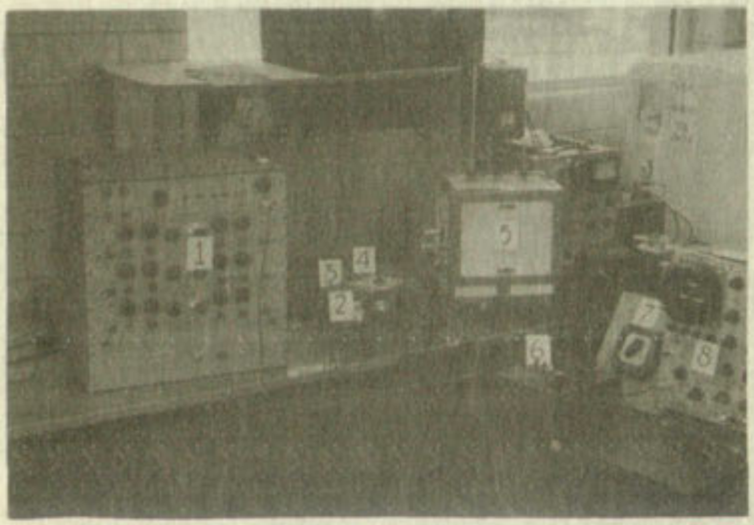
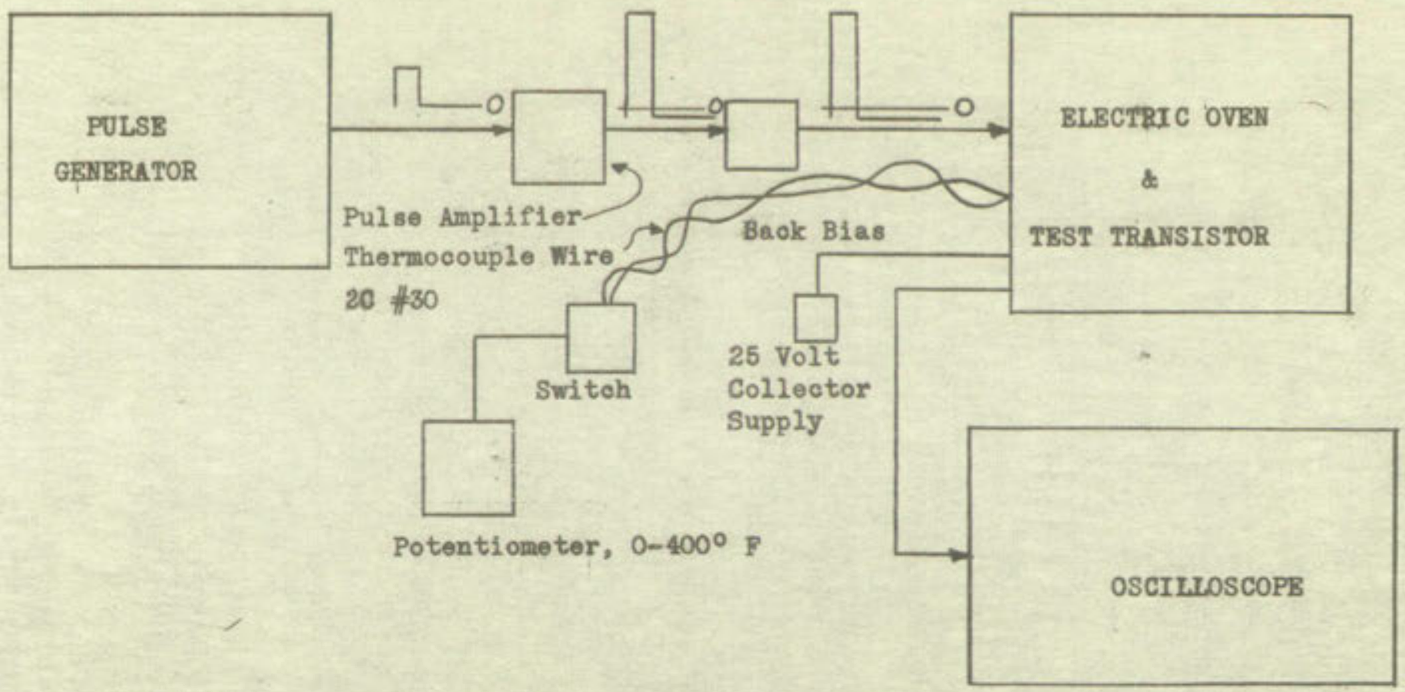


FIGURE 13

PULSE TEST SET UP

1. Pulse generator
2. Transistor (pulse) amplifier
3. Back bias battery and 15 henry inductor
4. Battery, 20 volt collector supply
5. Temperature chamber
6. Potentiometer
7. Switch, 8 point multiple
8. Oscilloscope



PULSE TEST CIRCUIT (GENERAL)

FIGURE 14

CHAPTER IV

THE RESULTS

I. PULSE TESTING

The transistors were placed in the temperature chamber and tested as described in Chapter II, The Method of Test. Where the available input pulse was too small in amplitude to cause an appreciable change in transistor temperature, the number of transistors pulsed at this duty factor was decreased expecting to devise a pulse generator at a later date which would extend these amplitudes.

The permissible peak power in the pulses at various repetition frequencies and pulse widths are presented in Figures 15, 16, 17, and 18. The solid flat-topped lines are the last peak power readings at which the transistor reproduced stable pulses and reached a constant temperature. The dash lines extending the flat-topped lines are the points where either the transistor failed completely or became unstable. The pulsing circuit, in many cases, would not provide pulses of large enough amplitude to destroy the transistor. These points are designated by a pointed line.

The maximum transistor temperature, average power of the permissible peak power reached, and the transistor used is also placed on the graphs.

The effects of duty factor or duty cycle are shown in Figure 19. Since failures occur in the temperature region of 200° F. and 216° F. transistor temperature, this information is plotted from curves in

CHAPTER IV

TEST RESULTS

1. STATIC TESTING

The transistors were placed in the temperature chamber and tested as described in Chapter II. The [illegible] were [illegible] and [illegible] [illegible] [illegible] [illegible] [illegible] the [illegible] of appreciable change in transistor [illegible], the [illegible] intervals at which data were taken was increased [illegible] a pulse generator [illegible] [illegible] [illegible] [illegible].

The [illegible] at the [illegible] [illegible] frequencies and [illegible] are [illegible] in Figures 13, 14, [illegible] and 15. The [illegible] lines are the [illegible] at which the transistor [illegible] and [illegible] temperature. The [illegible] lines [illegible] the [illegible] points where [illegible] [illegible] [illegible] unstable. The [illegible] [illegible] of large enough [illegible] to [illegible] the transistor. [illegible] points are designated by a pointed line.

The [illegible] [illegible] [illegible] [illegible] [illegible] [illegible] on the graphs.

The effects of [illegible] [illegible] in Figure 24. Since [illegible] [illegible] [illegible] [illegible] of 200°C, and [illegible] transistor [illegible] [illegible] [illegible] [illegible] [illegible] [illegible].

Appendix C at the 200° F. temperature point. Scarcely any failures occurred from pulsing below 200° F., the majority failed just after 200° F. For this reason then, in order to overcome the difference in transistor characteristics, the effects of duty cycle are taken at a safe operating temperature, 200° F., which is only slightly different from the maximum pulse ratings.

Since it was impossible to destroy the type CTP-1003 transistor in the small duty factor range with the existing pulsing equipment, peak power versus transistor temperature was plotted at these duty factors so that the curves could be extrapolated into the failure region. This set of curves is present in Appendix C. The six percent and smaller duty factor curves deviate from the expected power-temperature curves in that they have a tendency to droop or flatten out in the upper temperature region. Above six percent, the curves are straight lines as would be expected since dissipated energy is directly related to temperature and also to power. That is energy = power times time (Joule's law). Figure 20 is a typical curve showing this drooping effect in a manner to emphasize the reason for this deviation from the straight line relationship between dissipated power and temperature. This is to say that base current cannot be ignored in calculating the total power dissipated in a transistor at small duty factors in the upper temperature region.

II. DIRECT CURRENT TESTING

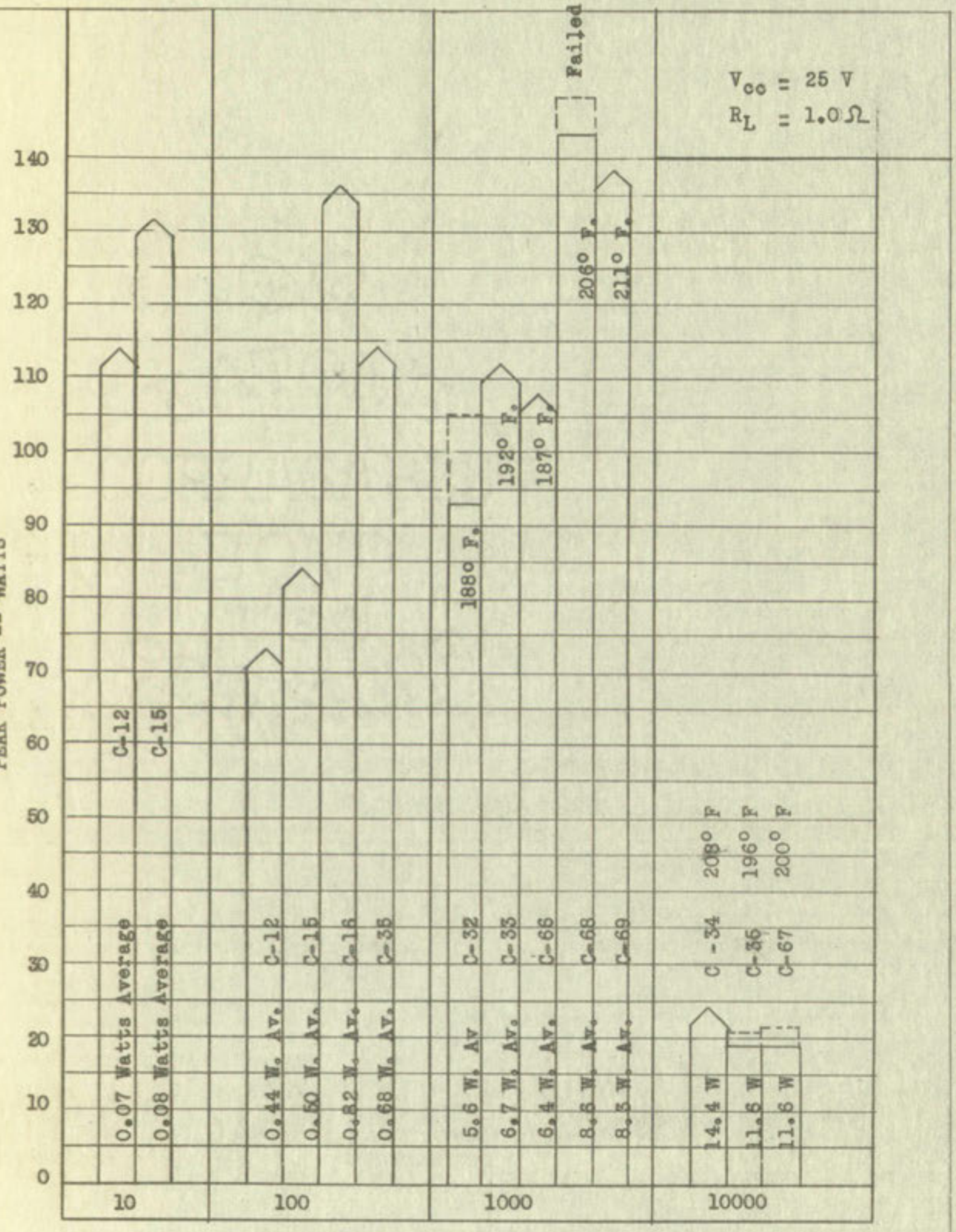
The two D. C. tests were performed as previously described in Chapter II, The Method of Test. With these tests, the transistors can

Appendix C at the 200° F temperature point. Not only was [illegible] occurred from pulsing units 200° F., the major [illegible] [illegible] 200° F. For this reason then, it [illegible] to estimate the difference in transistor characteristics [illegible] of [illegible] the safe operating temperature, 100° F., which is [illegible] from the maximum pulse reading.

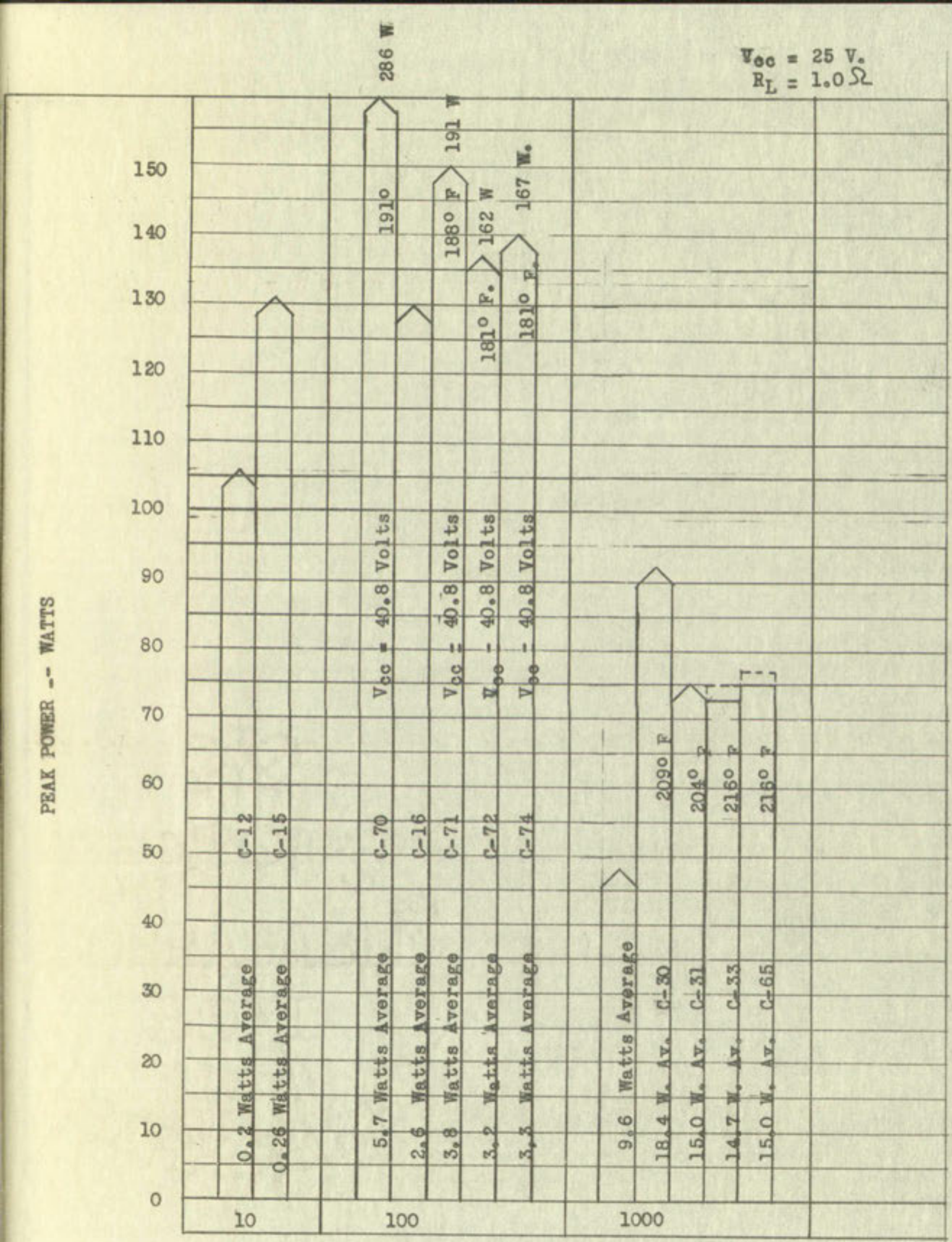
Since it was [illegible] to [illegible] the [illegible] in the small duty factor range with the [illegible] pulses [illegible], peak power versus transistor temperature was [illegible] factors so that the curves could be [illegible] region. This set of curves is [illegible] in [illegible] and smaller duty factor curves [illegible] from the [illegible] temperature curves [illegible] out in the upper temperature region. [illegible] are straight [illegible] directly related to temperature and [illegible] power [illegible] this [illegible] tion from the straight line relationship between [illegible] power and temperature. This [illegible] calculating the total power dissipated [illegible] factors in the [illegible] region.

[illegible]

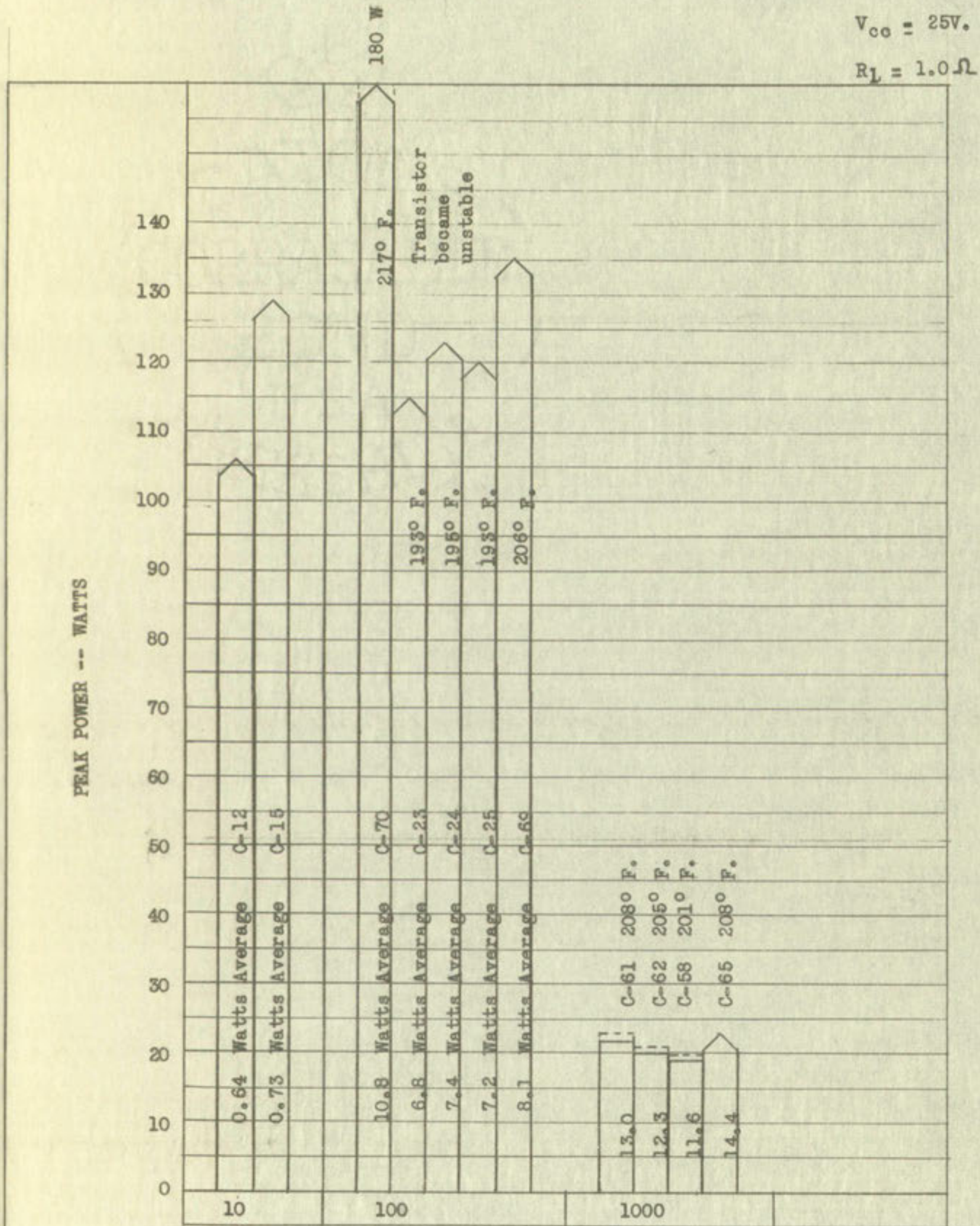
The two [illegible] tests [illegible] Chapter II, The [illegible] Test. [illegible] are



PULSE WIDTHS - MICROSECONDS
FIGURE 15
PULSE POWER RATINGS -- 60 CPS



Pulse Widths -- Microseconds
Figure 16
Pulse Power Ratings - 200 CPS
165° F. Ambient



PULSE WIDTHS -- MICROSECONDS

FIGURE 17

PULSE POWER RATINGS -- 600 CPS

165° F. Ambient

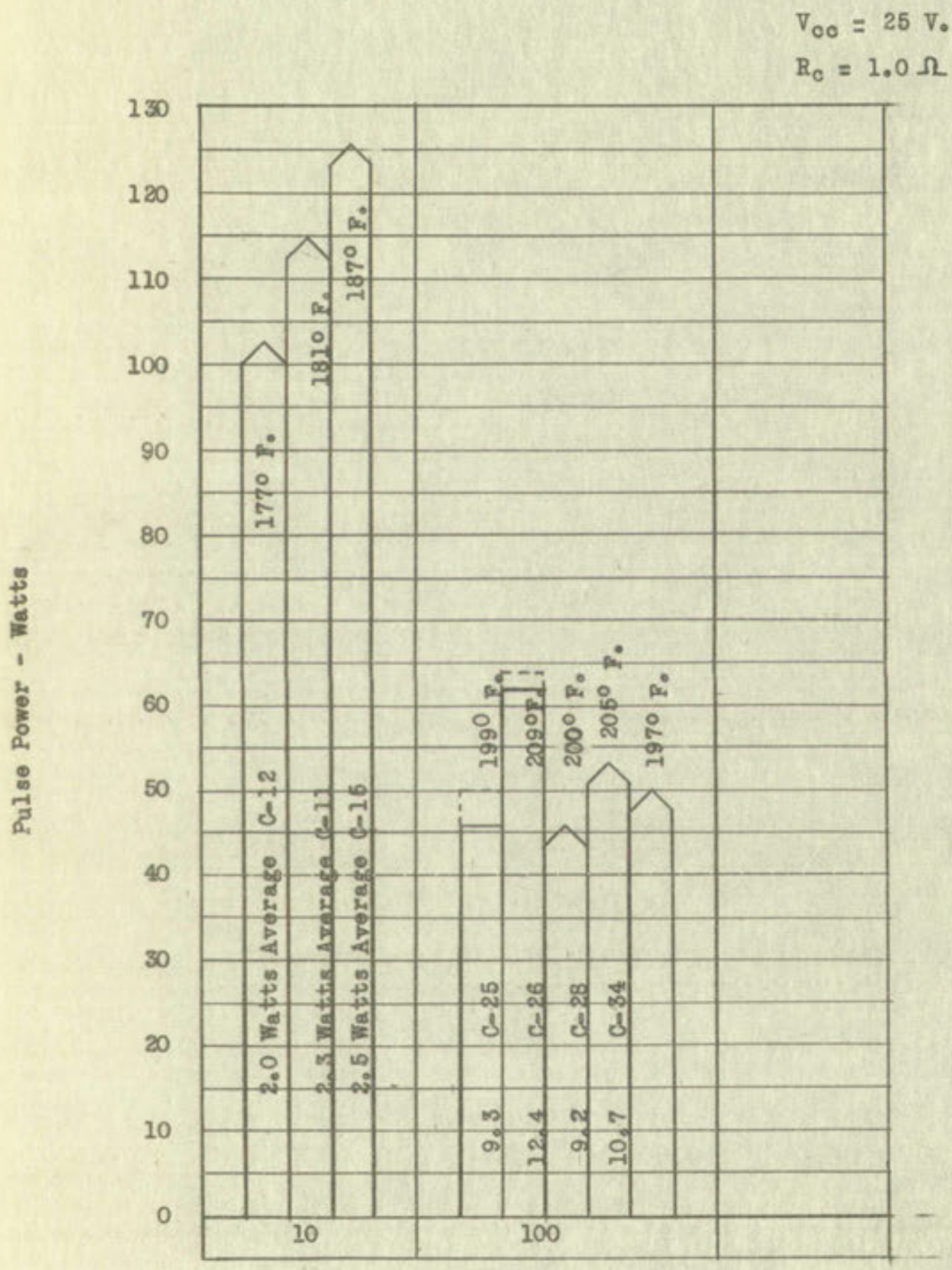
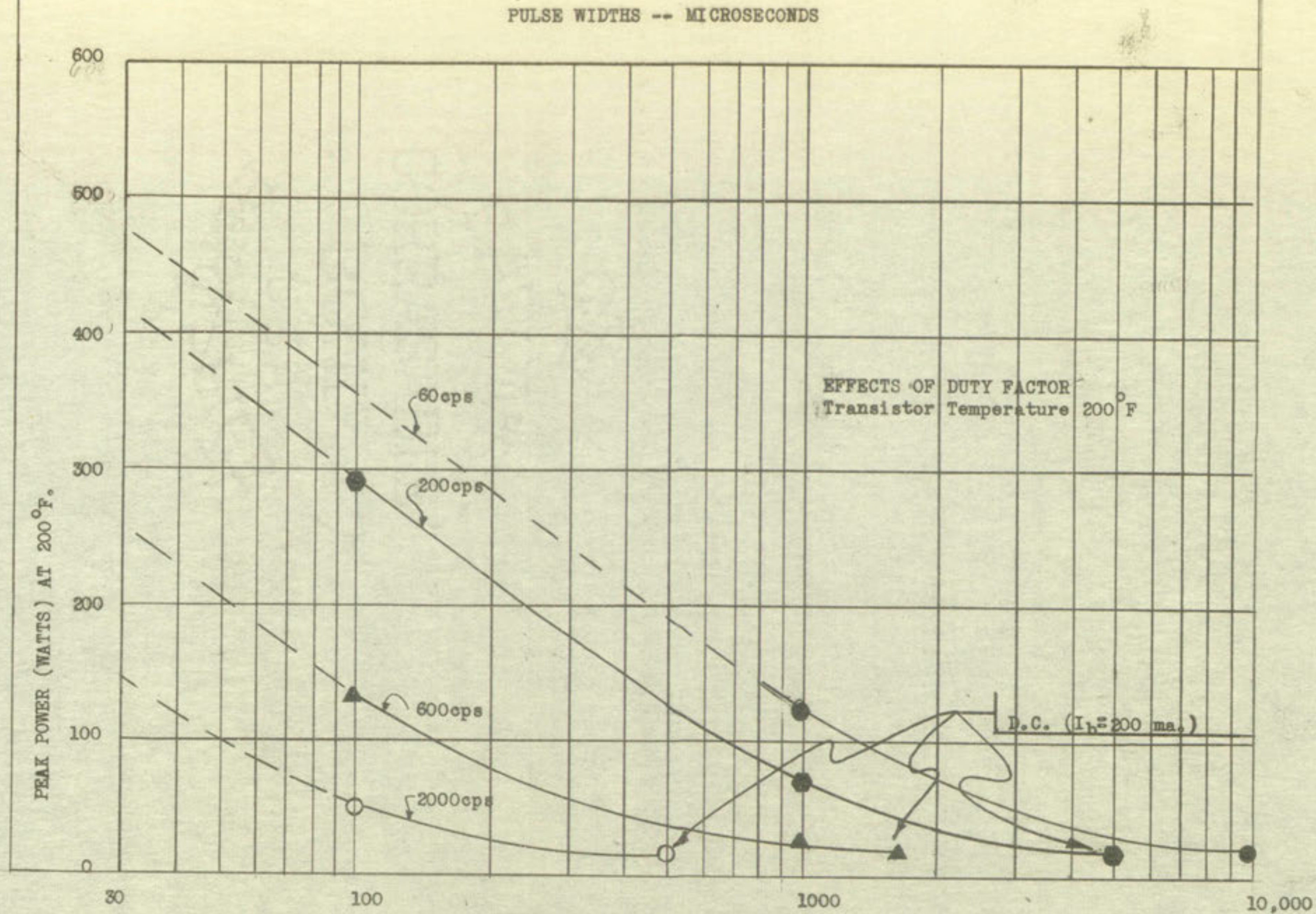
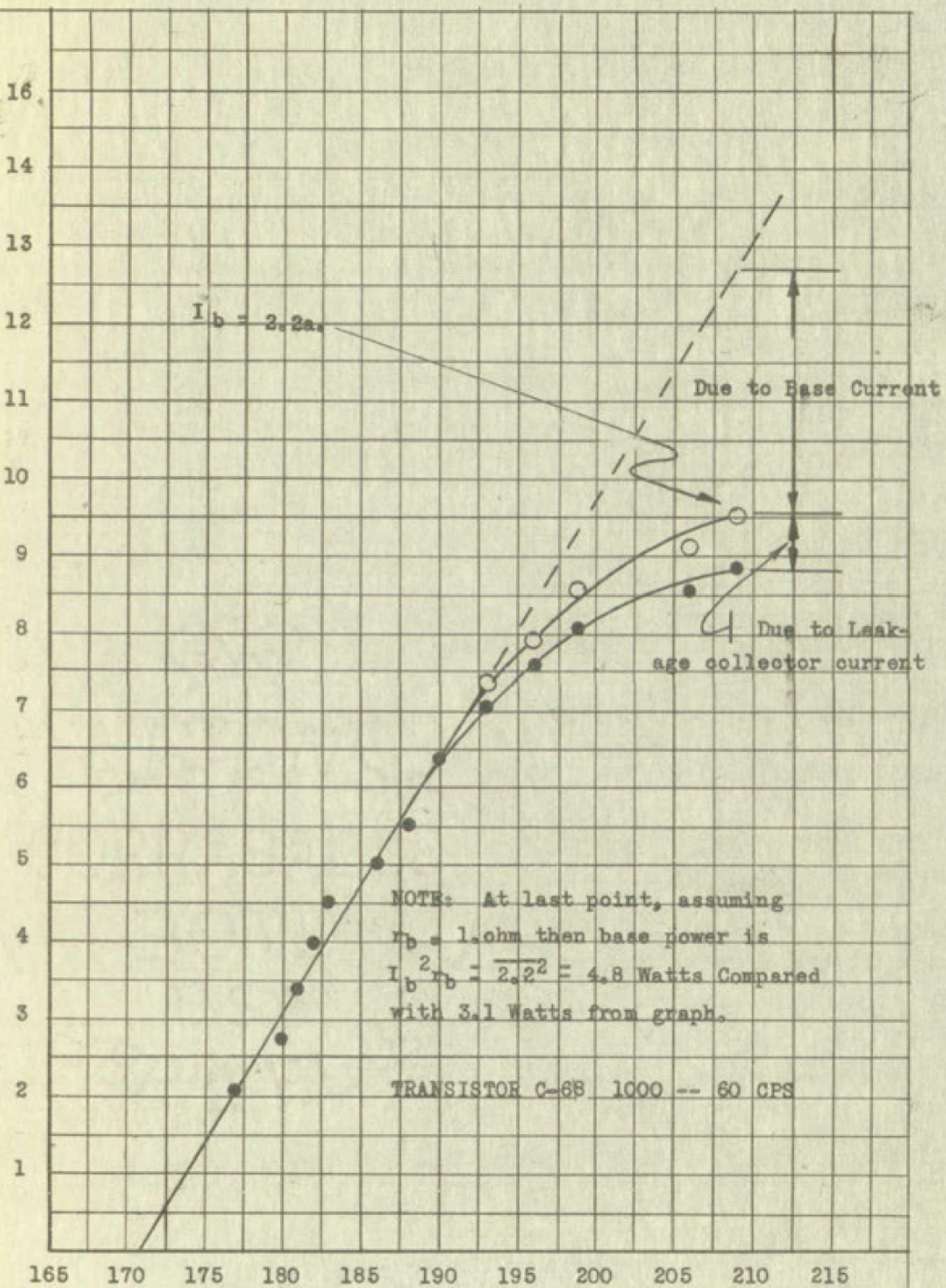


Figure 18
Pulse Rower Ratings -- 2000 CPS
165° F. Ambient


PULSE WIDTHS -- MICROSECONDS
600
500
400
300
200
100
0
PEAK POWER (WATTS) AT 200°F.
60cps
200cps
600cps
2000cps
EFFECTS OF DUTY FACTOR
Transistor Temperature 200°F
D.C. (Ib=200 ma.)
30
100
1000
10,000
PULSE WIDTH -- MICROSECONDS
Figure 19



TRANSISTOR TEMPERATURE--DEGREES FAHRENHEIT

FIGURE 20

AVERAGE POWER - TEMPERATURE RELATIONSHIP

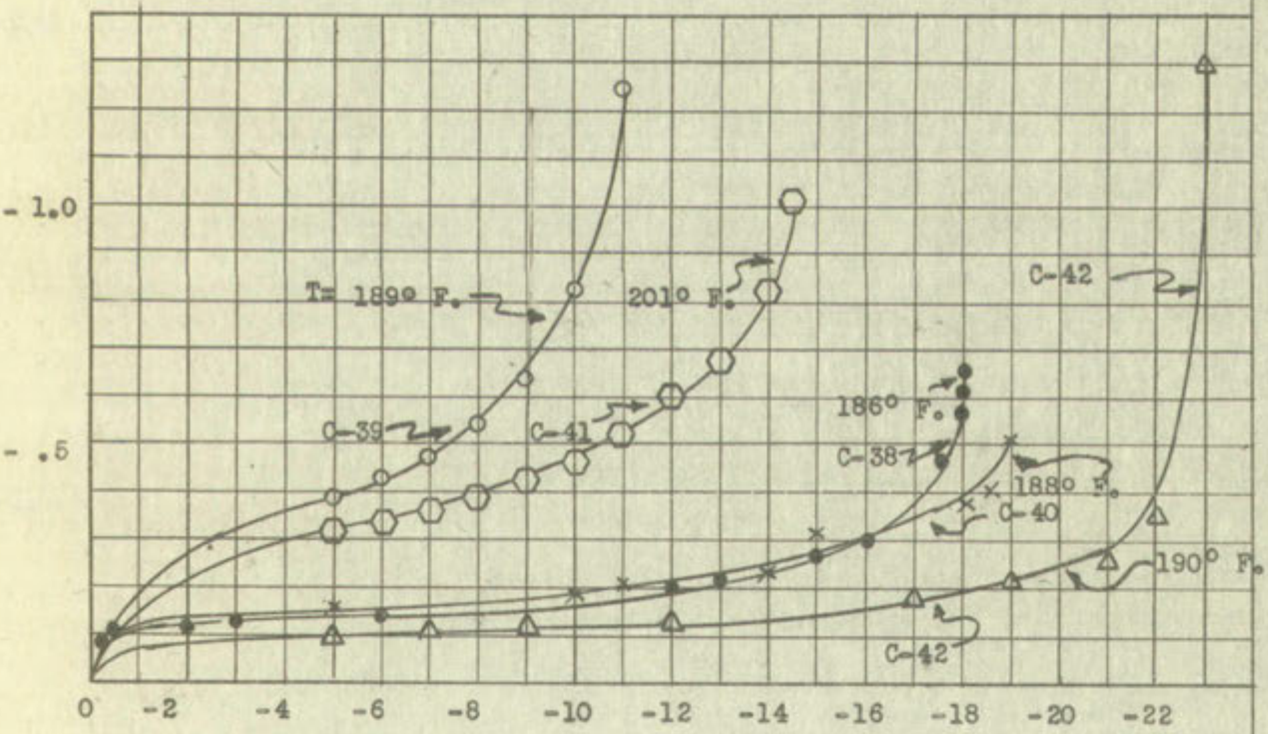
be controlled to prevent failure and yet the failure point can be determined. This makes it possible to use the same transistors for both tests.

The results of these tests are presented in Figures 21 and 22.

III. HEAT SINK CHARACTERISTICS

This test shows that approximately fifty percent more power can be dissipated in the transistor by doubling the area of the heat sink (in the heat sink range tested) and approximately three hundred percent more power can be dissipated in going from no heat sink to a three inch square sink. This information is contained in Figure 23. A comparison of heat sink characteristics of 85° F. and 165° F. ambient temperatures is made in Figure 24.

Average Collector Volts = 16.4
" Collector Current = 660 ma.
" Collector Power = 10.8 Watts
6" sq. Heat Sink
165° F. Ambient



COLLECTOR VOLTAGE - VOLTS

Figure 21

DIRECT CURRENT RATINGS -- $I_b = 0$

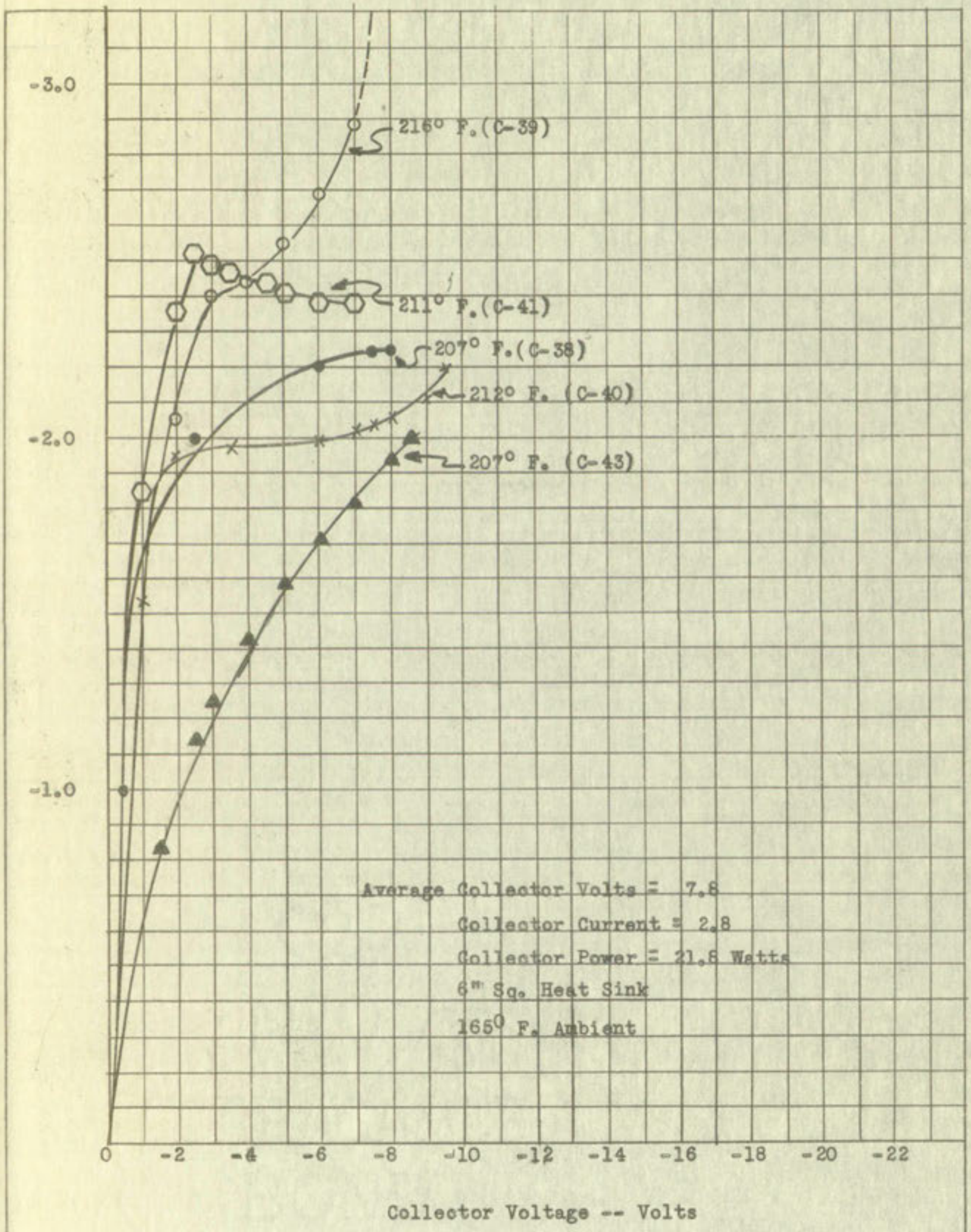


FIGURE 22

DIRECT CURRENT RATINGS -- I_b = 200 ma.

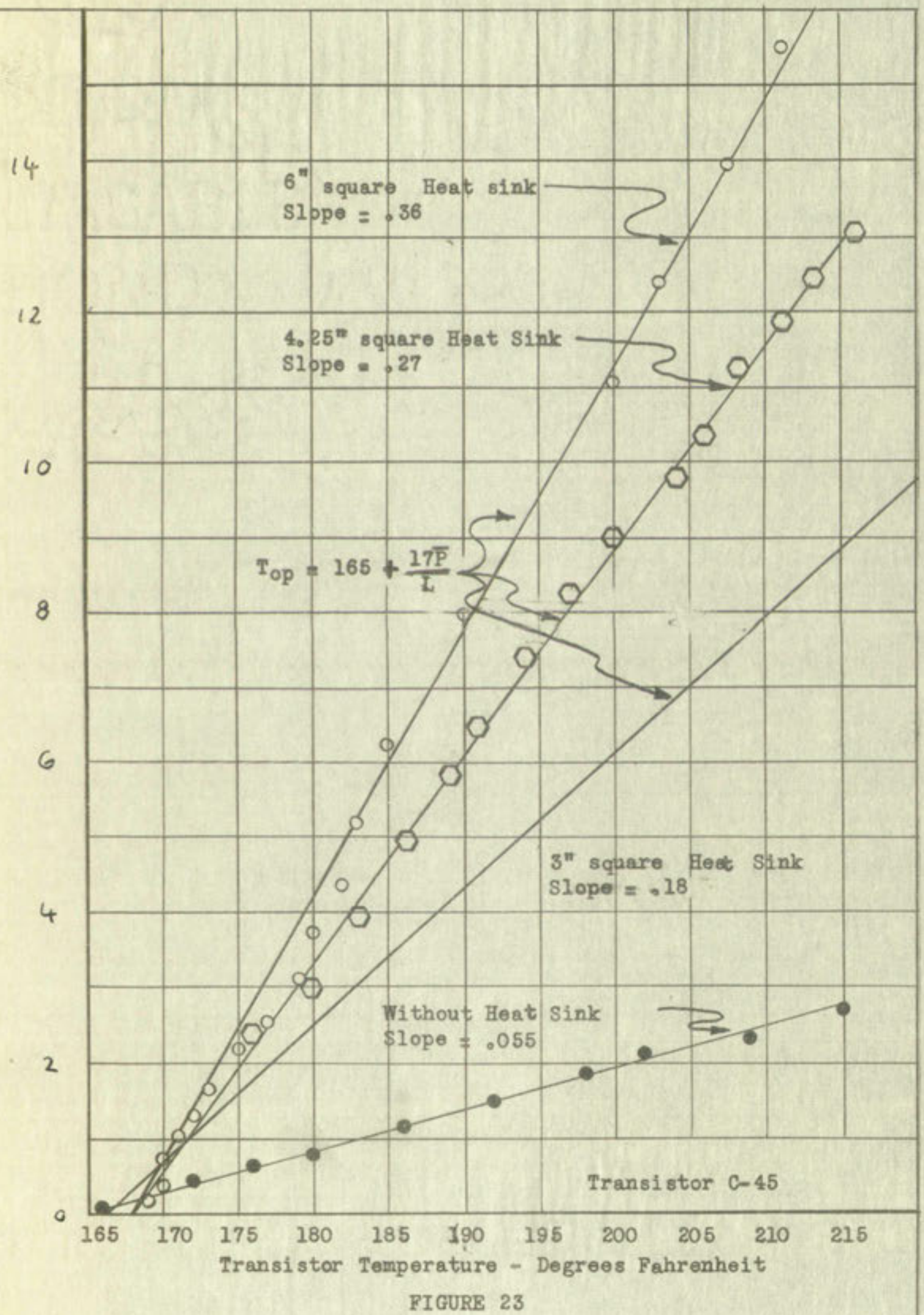


FIGURE 23

HEAT SINK CHARACTERISTICS -- 165° F. Ambient

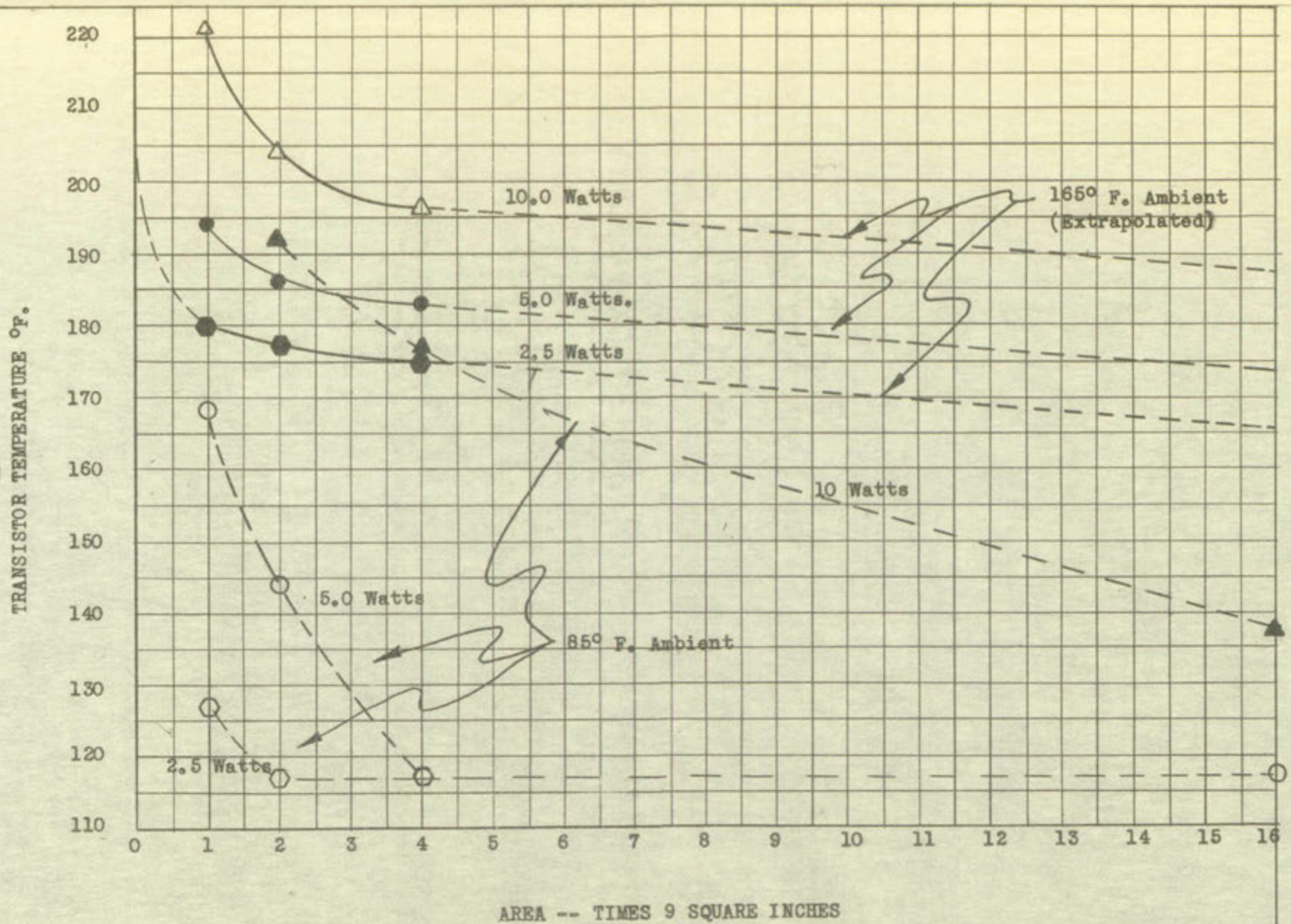


FIGURE 24

HEAT SINK CHARACTERISTICS - 85 & 165° F. AMBIENT

CHAPTER V

DISCUSSION OF RESULTS AND CONCLUSIONS

The results of the pulse and D. C. tests point strongly in the direction that temperature destroys transistors. It could be stated further that average collector power destroys transistors except for the low duty cycle cases. If the collector power is assumed to be the only power increasing the temperature of the transistor, then less average power is required to raise the transistor temperature at the low duty factors than at the higher duty factors. This certainly can not be possible. That is to say that although the base resistance is quite small the base current becomes very large for the low duty factor pulses, thus increasing the total power input to the transistor and affecting the transistor temperature. The base power then, cannot be overlooked in the low gain region.

Efforts were made to pulse the transistor with 0.1 microsecond pulses but it was found that reproductionwas very poor below 100 microsecond pulses. Ten microsecond pulses could be amplified but the rise time was equal to the pulse width while the fall time was usually about four times the pulse width.

The spread of transistor characteristics (taken from the characteristics of approximately seventy transistors) located in Appendix B, is so wide that a sample of five transistors does not give a very reliable picture of the maximum permissible ratings. Possibly a sample of twenty-five at each duty factor would be more reliable.

CHAPTER V

DISCUSSION OF RESULTS AND CONCLUSIONS

The results of [illegible] further point the way in the direction that [illegible] (from [illegible]), it would be attained further than average collector power can be [illegible] for the low duty cycle cases. If the collector power is assumed to be the only power [illegible] the [illegible] then lower average power is required to raise the [illegible] junction temperature at the low duty factors than at the higher duty factors. This may not be possible. [illegible] although the base resistance [illegible] quite small the base current becomes very large at the low duty factor pulses, thus increasing the [illegible] power [illegible] and affecting the transistor temperature. The base power should not be overlooked in the low duty region.

Efforts were made to raise the [illegible] for narrower pulses but it was found that [illegible] below [illegible] microsecond pulses. [illegible] rise time was equal to the pulse width [illegible] about four times the pulse width.

The spread of transistor characteristics [illegible] characteristics of [illegible] Appendix B [illegible] gives a very [illegible]. Possibly a [illegible] reliable.

The D. C. tests show clearly that in order for the transistor circuit to be stable at 165° F. ambient with the collector voltage of any size that the base circuit must be back biased. Back bias of ten volts was used for all tests except the D.C. tests which did not require back bias since a large resistor was used in the collector circuits to limit the collector current.

From the heat sink characteristics at 165° F. ambient an equation was developed which makes it possible to predetermine the operating temperature of a transistor at an average D. C. power dissipated in the transistor for an arbitrary heat sink. The equation

$$T_{op} = 165 + \frac{17\,\overline{P}}{L}$$

is developed in Appendix D. T_{op} is the operating temperature of the transistor when dissipating an average power, $\overline{P}$ using a square heat sink with L the length of a side.

Thus, if an average power of five watts were to be dissipated in a transistor using a square heat sink of a length of three inches.

then

$$T_{op} = 165 + \frac{17\ (5)}{3} = 165 + \frac{80}{3} = 193^{\circ}\ F.$$

as compared with 194° F. from Figure 23.

The failures witnessed by the Sandia Corporation as mentioned in Chapter I, Introduction, were most likely due to a large D. C. component of power which did not exceed the limits of the transistor until the large current spikes were induced.

The [illegible] clearly that in order for the [illegible] circuit to be stable at 100° F. [illegible] any size that the base circuits were [illegible]. [illegible] volts was used [illegible] require [illegible] circuits to limit the collector [illegible].

From the [illegible] equation was developed [illegible] operating temperature of a transistor [illegible] in the [illegible]

$$T_{op} = [illegible]$$

is developed in Appendix [illegible]. T_{op} is the operating temperature of the transistor when dissipating an average power [illegible] sink with [illegible].

Thus, if [illegible] power of [illegible] in a transistor [illegible] square [illegible]

then

$$T_{op} = 100 + \frac{[illegible]}{[illegible]} = 100 + \frac{[illegible]}{[illegible]} = [illegible]$$

as compared with [illegible] Figure [illegible].

The [illegible] in Chapter [illegible]. In [illegible] component of power which did not [illegible] until the [illegible].

Further testing could be done to prove this point by pulsing the collector circuit with large power pulses which were known not to contain a D. C. component.

BIBLIOGRAPHY

BIBLIOGRAPHY

Griffith, LeRoy A., Germanium Power Transistors, Minneapolis-Honeywell Regulator Company, Minneapolis 8, Minnesota, Transistor Division, paper dated February 9, 1955, TR73pl.

APPENDICES

APPENDIX A

MANUFACTURER'S SPECIFICATIONS OF THE TYPE CTP-1003 TRANSISTORS

Description. The CTP-1003 transistor is a hermetically sealed PNP germanium power transistor designed for general use at nominal collector voltage up to 28 volts D.C. It is characterized by low collector saturation voltage, moderate current gain, and high current handling capacity. The collector is electrically connected to the metal housing. Where the collector must be insulated from the chassis, the large area of the mounting flange permits adequate heat flow through the insulating medium (e.g., mica).

Electrical Specifications.

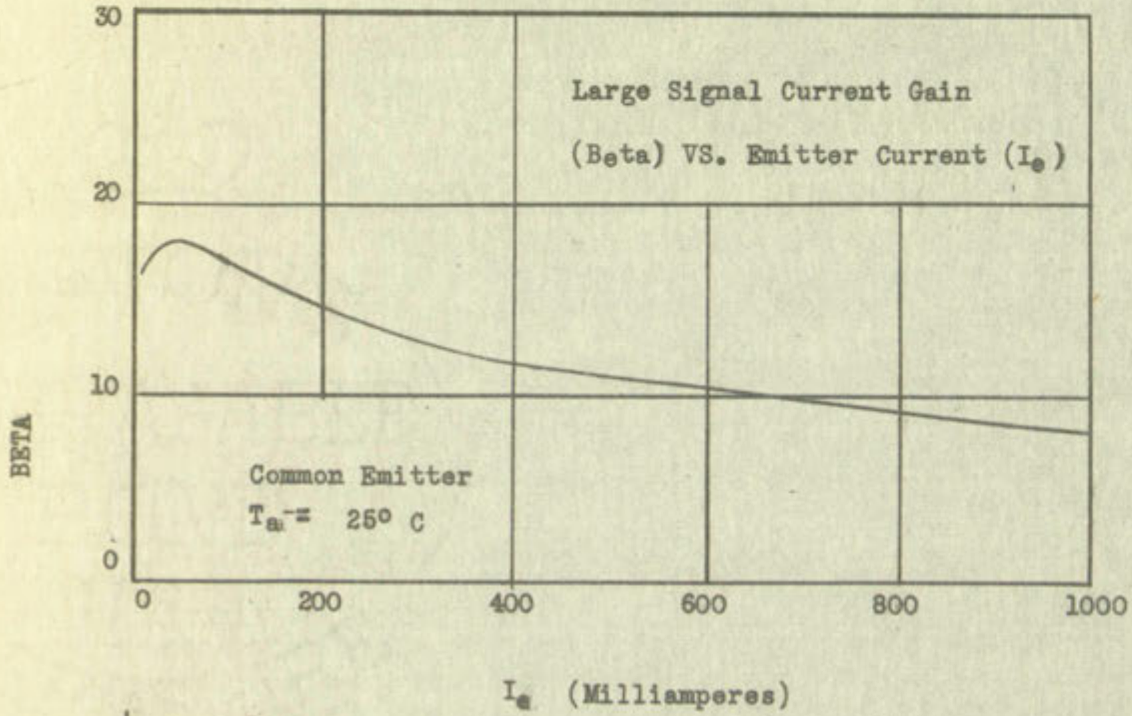
Absolute maximum ratings

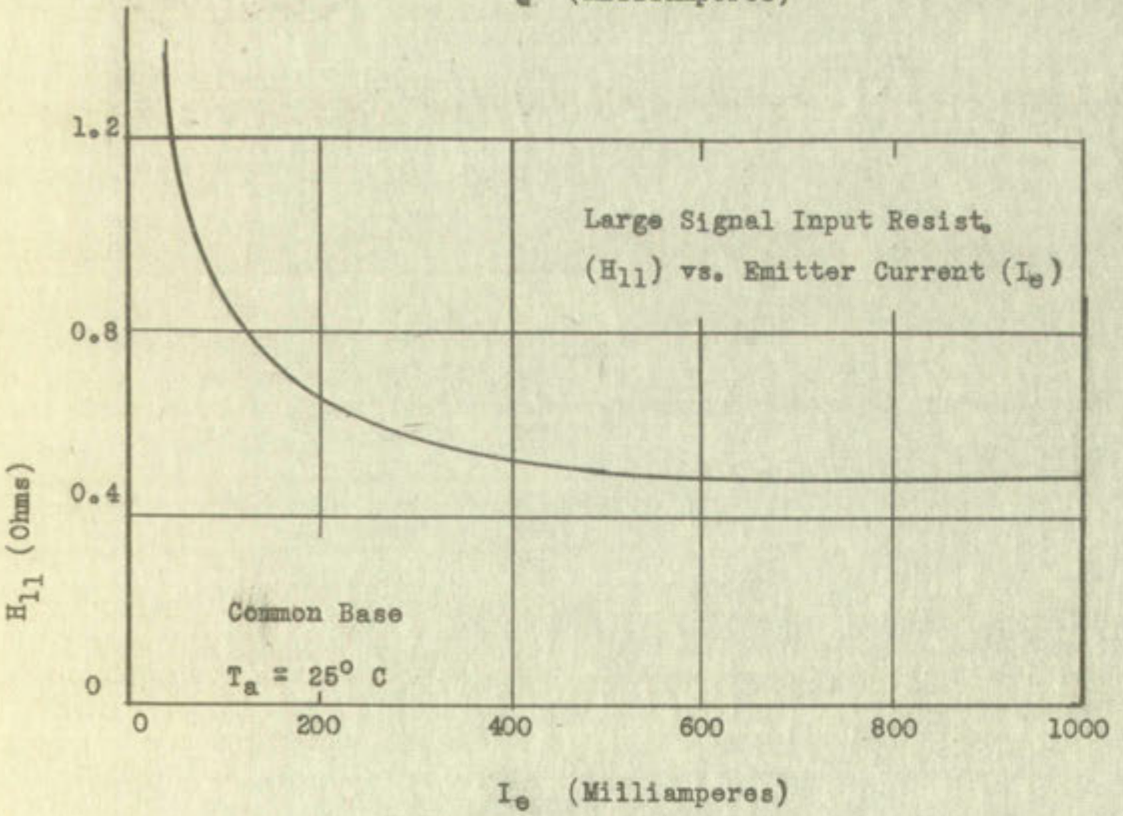
Instantaneous collector to base voltage	60 V.
Collector supply voltage	30 V.
Junction temperature	85° C.
Instantaneous total peak power	25 W.
Average total power with infinite heat sink at 25° C.	25 W.
Average total power (no heat sink) in free air at 25° C.	2.25 W.

Characteristics at 25° C.*

Test	Conditions	Symbol	Min	Max	Unit
Collector cut-off current	V_{cb} - -60V	I_{co}		2.0	ma
	I_e - 0				
Emitter cut-off current	V_{eb} - 6 V	I_{eo}		.20	ma
	I_c - 0				
Power gain, common	V_{cc} - 14.2 V	P_g	23.0		db
emitter, transformer	I_c - .37 A				
coupled	R_L - 30 ohms				
	R_g - 10 ohms				
Power gain cut-off	Same as for	f_{P_g}	4 (250 M.S.)		Kc
frequency	Power gain				

*Cooling must be provided equivalent to mounting the transistor in the center of a 3" x 3" piece of aluminum, 1/16" thick, suspended in free air.

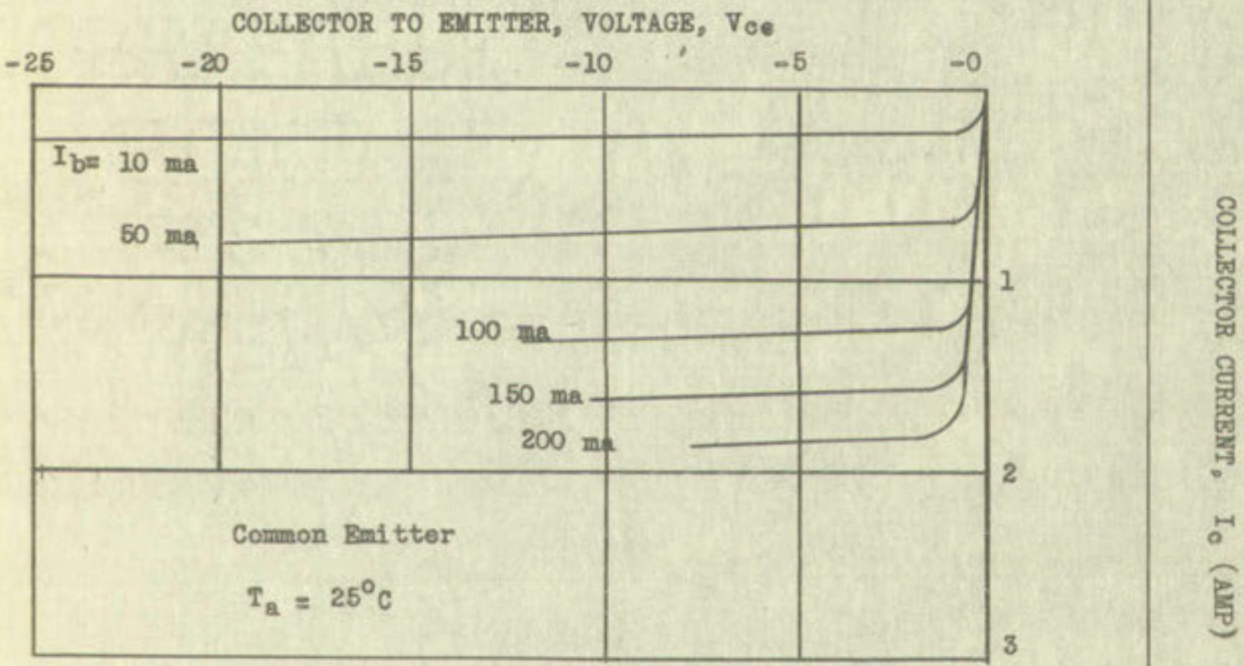




CLEVITE TRANSISTOR PRODUCTS

CTP-1003

TYPICAL CHARACTERISTICS



CLEVITE TRANSISTOR PRODUCTS

APPENDIX B

THE SPREAD OF TRANSISTOR CHARACTERISTICS

Preceding all tests, a photograph of the input (base) and output (collector) characteristics of each transistor as taken with the transistor connected common emitter.

It is from these characteristics that the following spread of collector and base characteristics was taken.

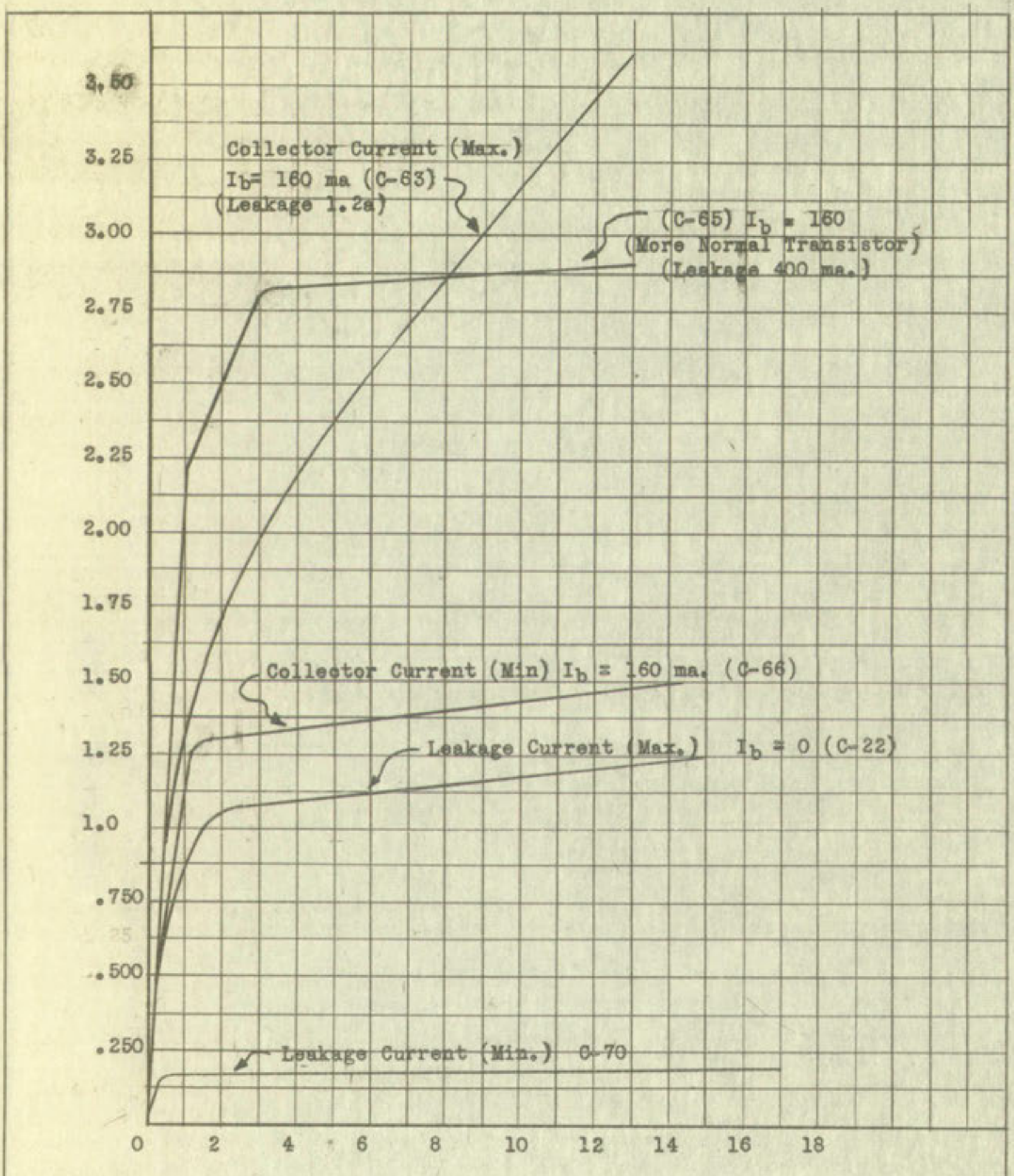
APPENDIX [illegible]

[illegible] CURVES OF TRANSISTOR CHARACTERISTICS

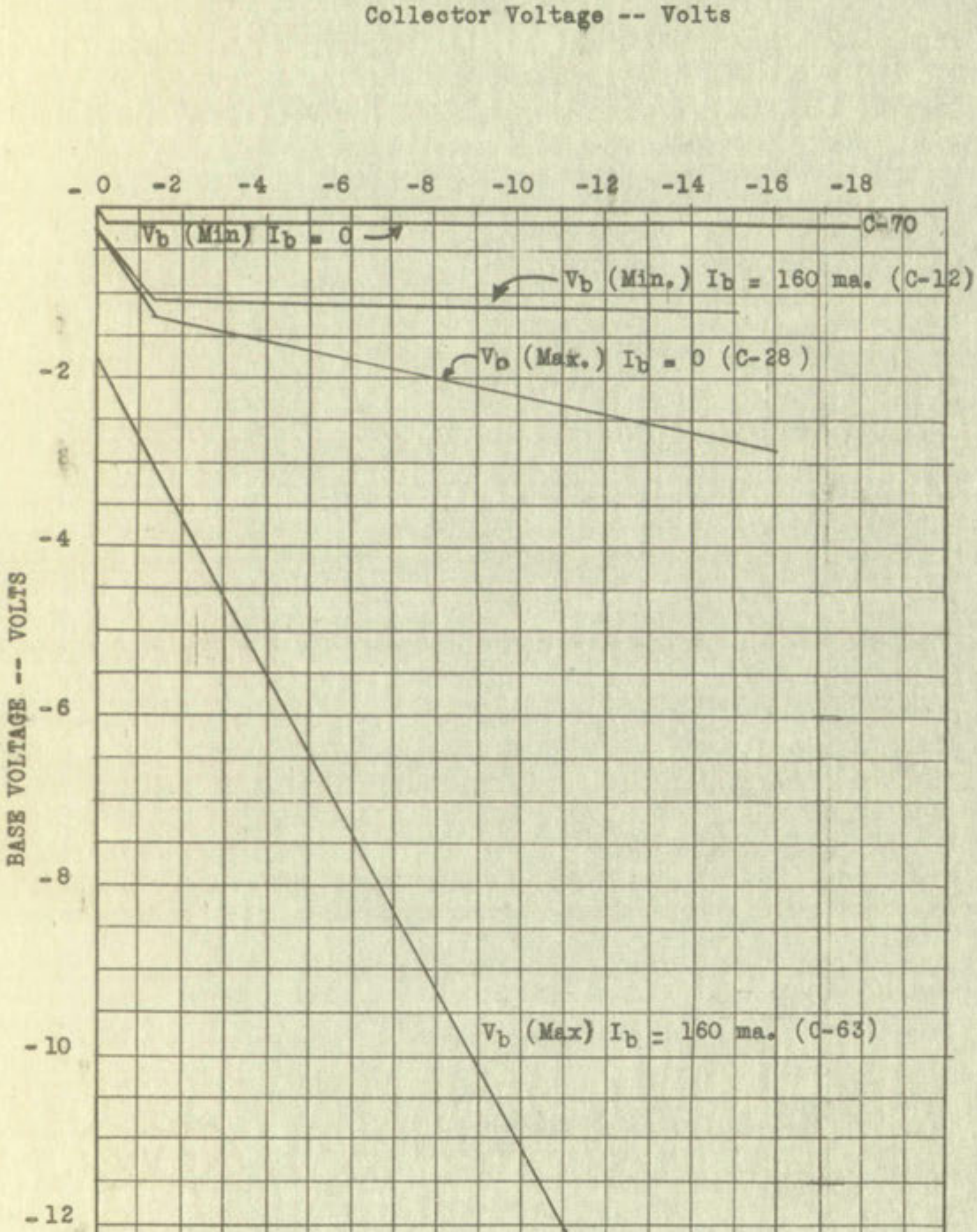
Procedure: All tests, a photograph of the [illegible] output (collector) characteristics of each transistor [illegible] with the transistor [illegible] common emitter.

It is from these [illegible] that the following values of collector and base characteristics was taken.

THE SPREAD OF COLLECTOR CHARACTERISTICS



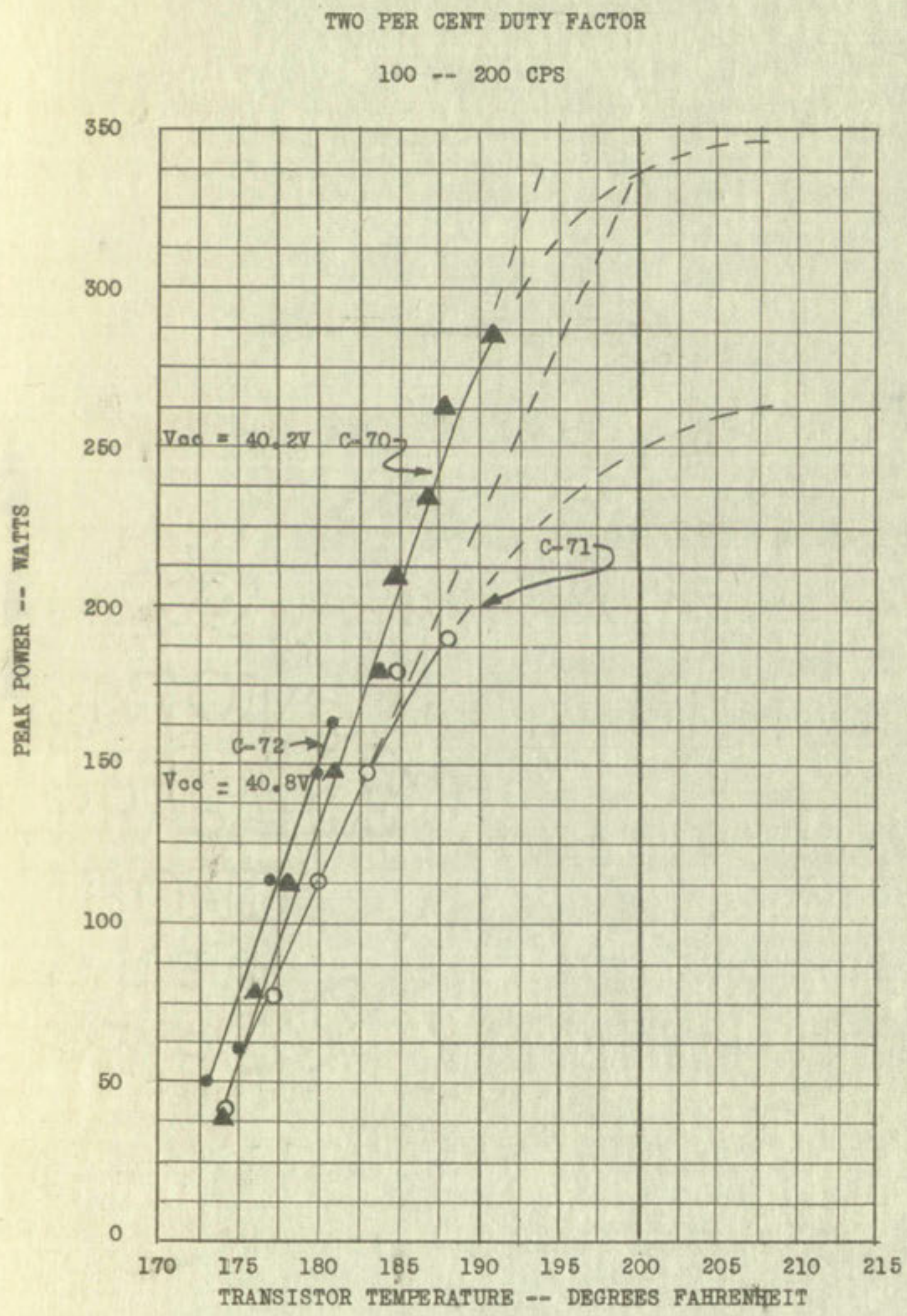
THE SPREAD OF BASE CHARACTERISTICS



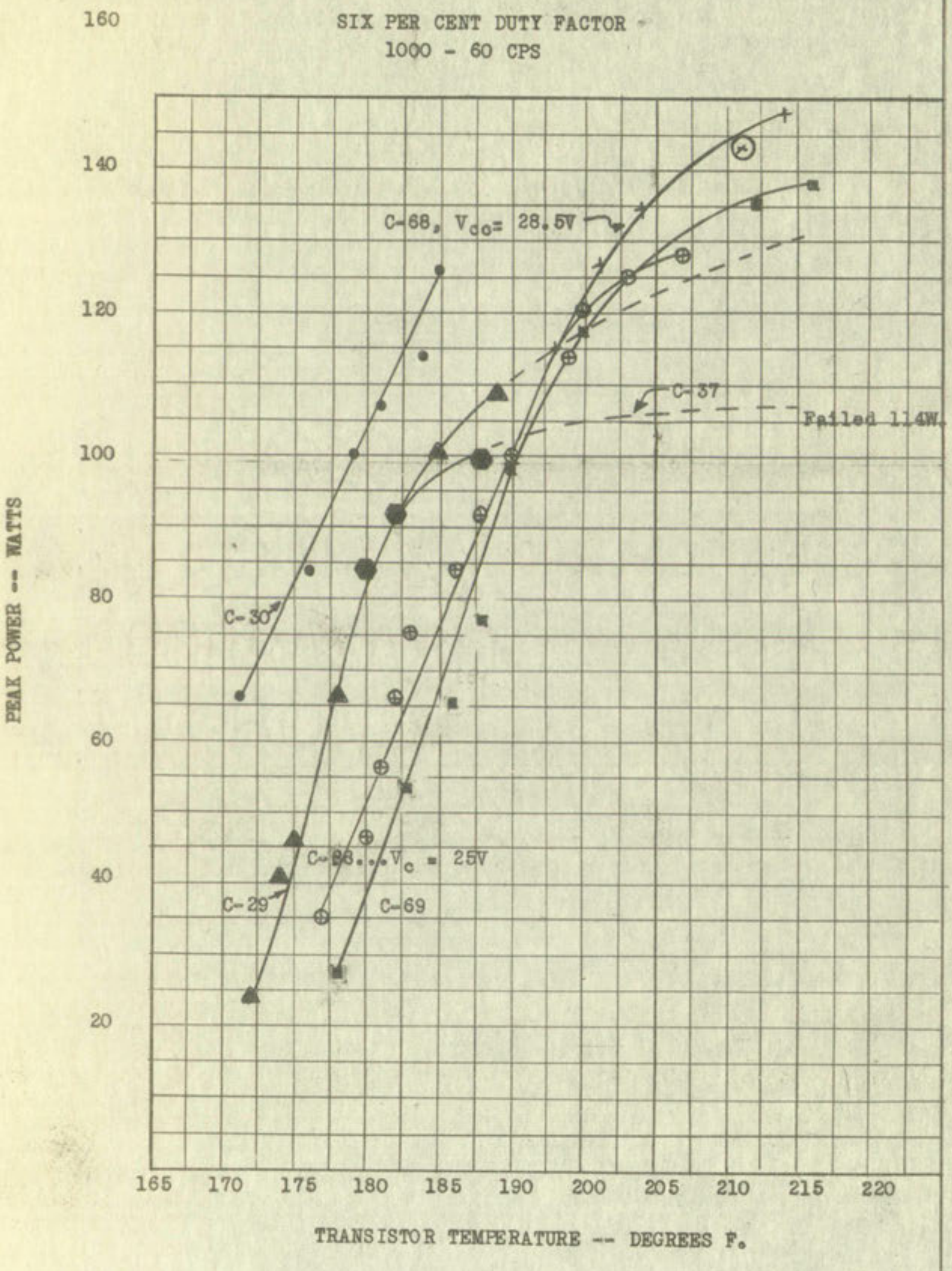
APPENDIX C

PERCENT DUTY FACTOR CURVES

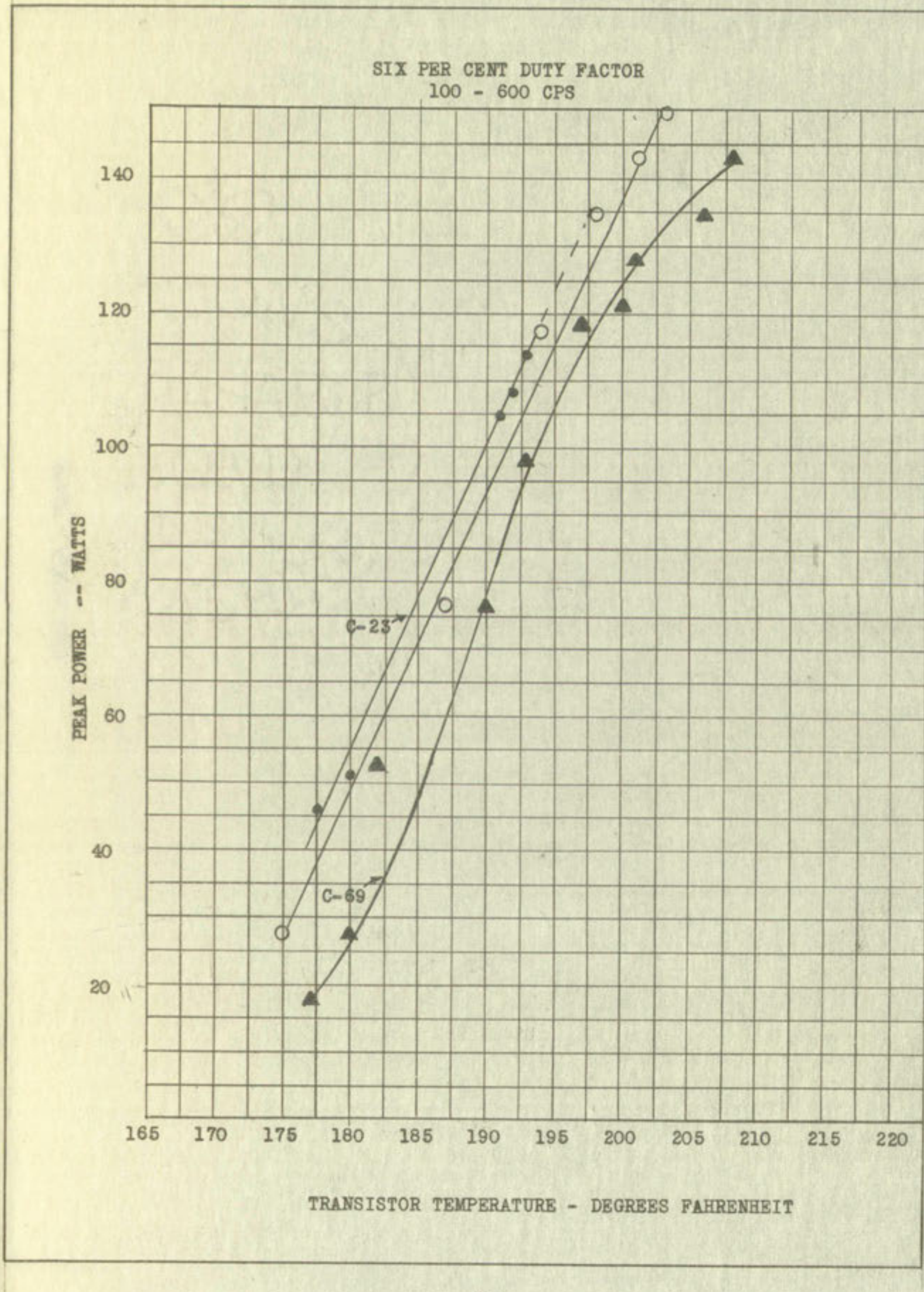
The curves contained in this appendix are the plot of the various collector peak power points against transistor temperature taken directly from the experimental data. This set of curves was plotted for the purpose of extending the pulse power into the failure region which had not been done experimentally.

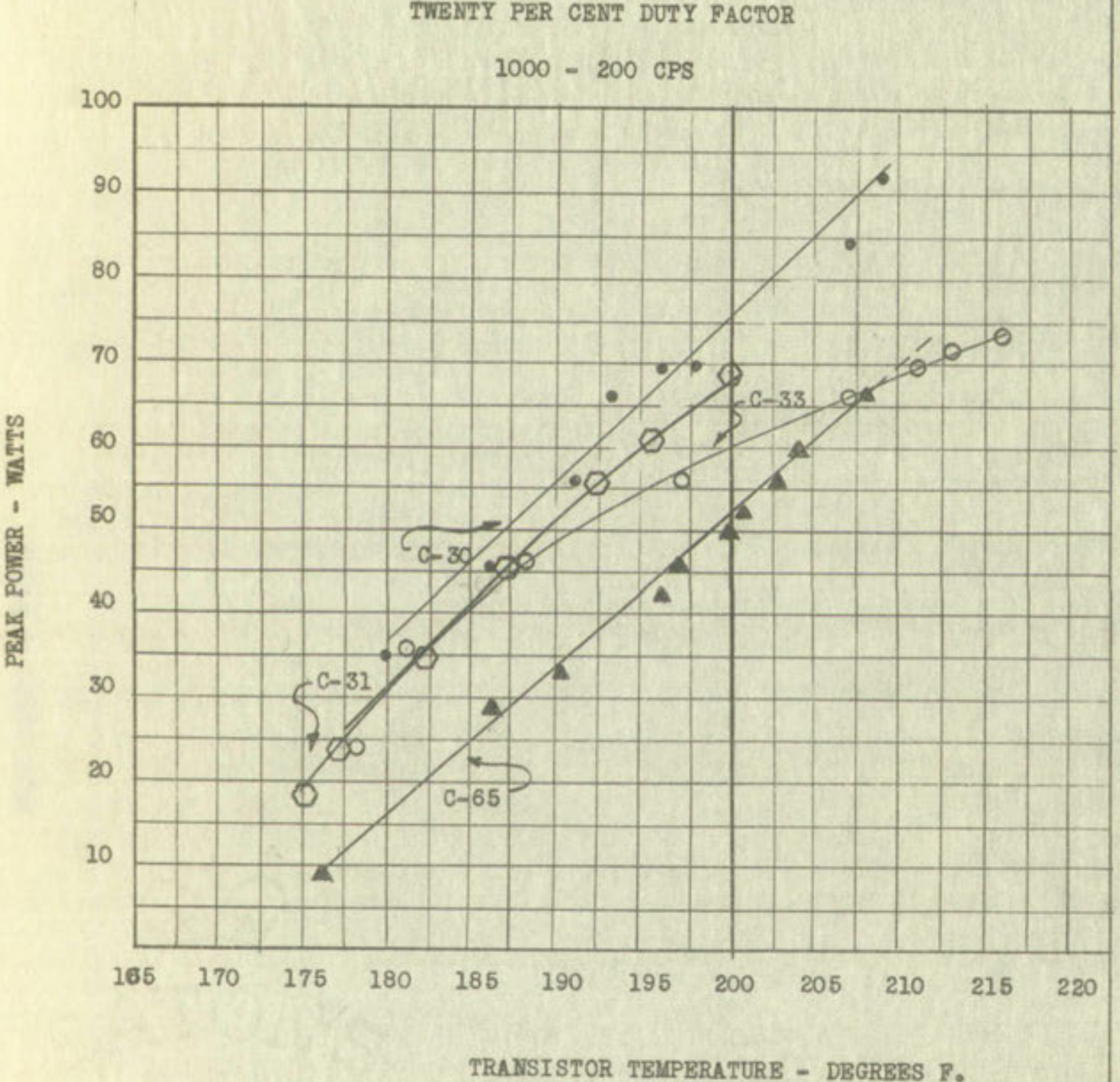


TWO PER CENT DUTY FACTOR
100 -- 200 CPS
PEAK POWER -- WATTS
350
300
250
200
150
100
50
0
Vcc = 40.2V C-70
C-71
C-72
Vcc = 40.8V
170
175
180
185
190
195
200
205
210
215
TRANSISTOR TEMPERATURE -- DEGREES FAHRENHEIT



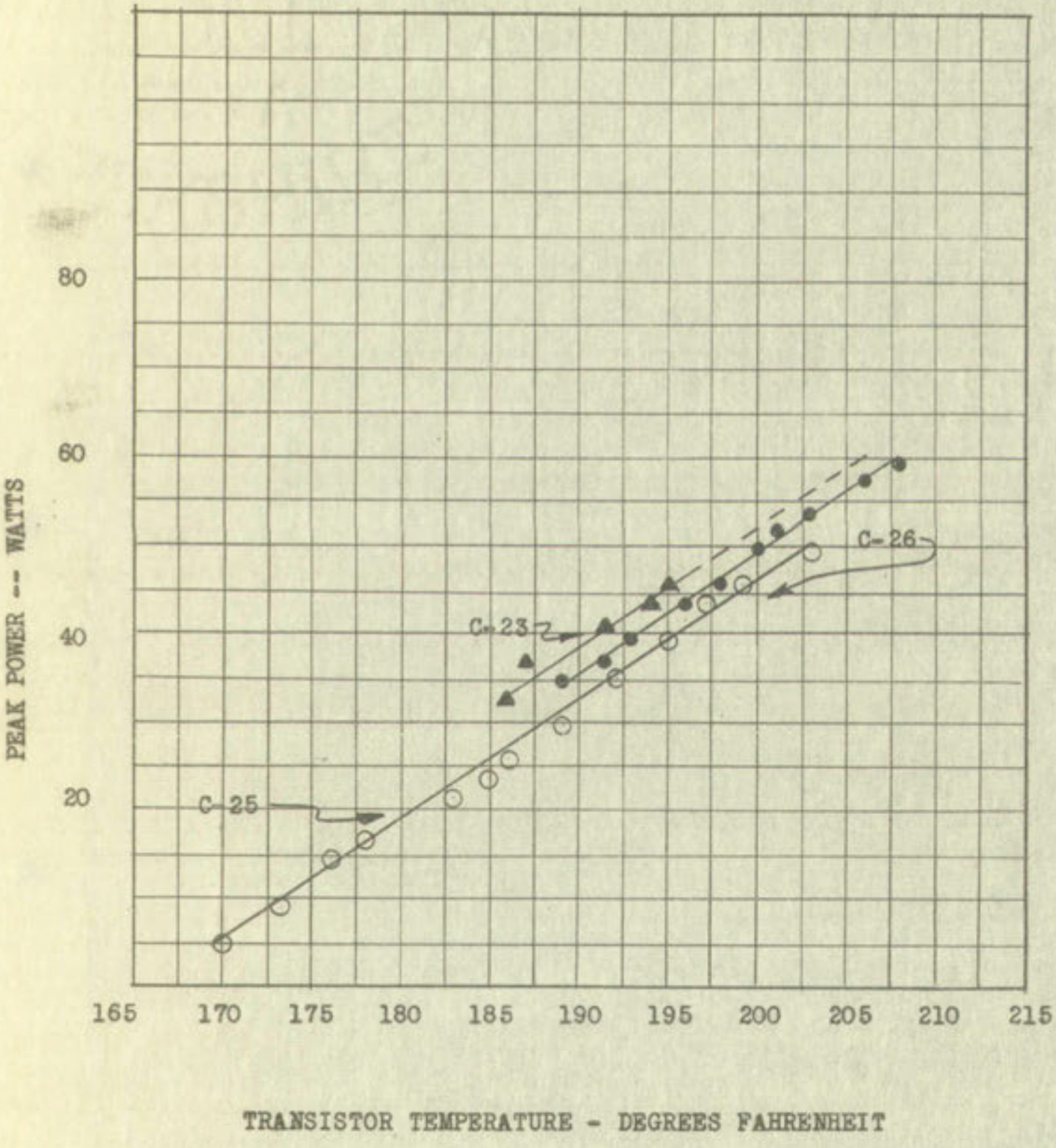
SIX PER CENT DUTY FACTOR
1000 - 60 CPS
PEAK POWER -- WATTS
TRANSISTOR TEMPERATURE -- DEGREES F.
160
140
120
100
80
60
40
20
165
170
175
180
185
190
200
205
210
215
220
C-68, V_{co}= 28.5V
C-37
Failed 114W.
C-30
C-68...V_c = 25V
C-29
C-69


SIX PER CENT DUTY FACTOR
100 - 600 CPS
PEAK POWER -- WATTS
140
120
100
80
60
40
20
C-23
C-69
165
170
175
180
185
190
195
200
205
210
215
220
TRANSISTOR TEMPERATURE - DEGREES FAHRENHEIT

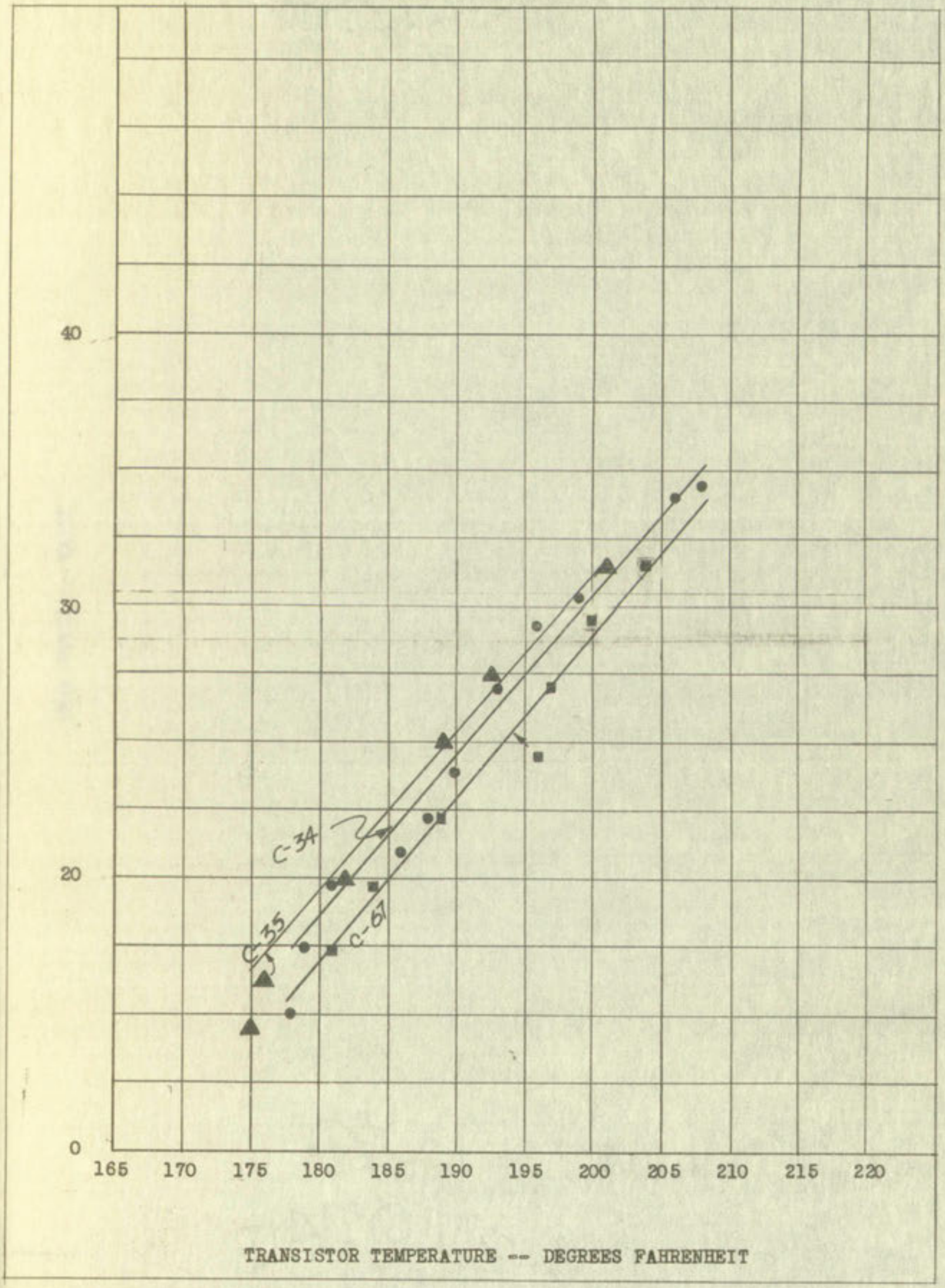

TWENTY PER CENT DUTY FACTOR
1000 - 200 CPS
PEAK POWER - WATTS
TRANSISTOR TEMPERATURE - DEGREES F.
100
90
80
70
60
50
40
30
20
10
165
170
175
180
185
190
195
200
205
210
215
220
C-33
C-30
C-31
C-65

TWENTY PER CENT DUTY FACTOR

100 - 2000 CPS

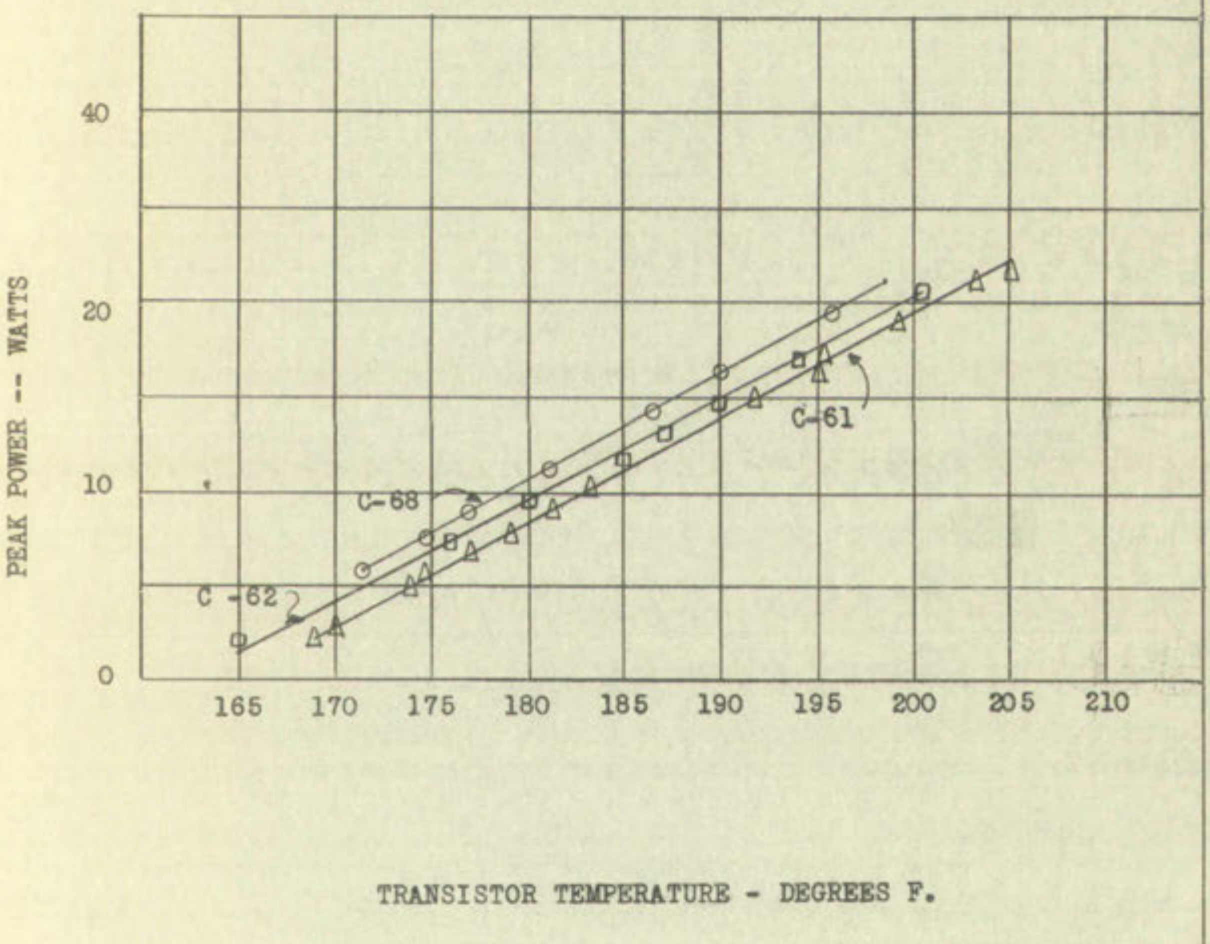


SIXTY PER CENT DUTY FACTOR
10000 -- 60 CPS



SIXTY PER CENT DUTY FACTOR

1000 - 600 CPS



APPENDIX D

DEVELOPMENT OF THE OPERATING TEMPERATURE EQUATION

The equation for the power-temperature curves in terms of temperature is

$$T_{op} = 165 + \frac{\overline{P}}{\tan \theta} \qquad (2)$$

where θ is the angle between the curve and the temperature axis. The transistor temperature rise per watt of average power is dependent on the thermal resistance of the transistor and the heat sink used. $\frac{1}{\tan \theta}$ is a measurement of this thermal resistance which is dependent on the area and material used in making the transistor and heat sink. Since only one type of transistor and heat sink is involved here, then $\frac{1}{\tan \theta}$ is directly proportional to K, a constant dependent on thermal resistance of the materials, and inversely proportional to the area of the heat sink.

Then an equation can be developed using the length of the side of the heat sink which should be helpful in circuit design.

First using a 6" square sink, the slope of the curve is $\frac{1}{.36}$.

Then using only the last part of the equation

$$\frac{\overline{P}}{\tan \theta} = \frac{\overline{P}}{.36}$$

let equal $\frac{K\overline{P}}{L^2}$ where $K = kL$, both k's are constant; so for the 6" sink

$$\frac{k_1 L_1 \overline{P}}{(\text{area})_1} = \frac{k_1 L_1 \overline{P}}{L_1^2} = \frac{\overline{P}}{.36}$$

APPENDIX I

DEVELOPMENT OF THE LENGTH [illegible] IN THE EQUATION

The equation for the power dissipated versus the ambient temperature is

$$T_{A} = 125 + \frac{P}{\tan\theta} \qquad (1)$$

where θ is the angle between the power and the temperature axis. The transistor temperature rise per watt of power is dependent on the thermal resistance of the transistor and the heat sink used. $\frac{1}{\tan\theta}$ is a measurement of this thermal resistance which is dependent on the size and material used in making the transistor and heat sink. Since only one type of transistor and heat sink is involved here, then $\frac{1}{\tan\theta}$ is directly proportional to K, a constant dependent on thermal resistance of the materials, and inversely proportional to the area of the heat sink.

Then an equation can be developed using the length of the side of the heat sink which should be helpful in circuit design.

First using a 6" square sink, the slope of the curve is [illegible]

Then using only the last part of the equation

$$\frac{P}{[illegible]} = \frac{P}{\tan\theta}$$

Let equal [illegible] where K = [illegible], both K and [illegible] are constants so for the 6" sink

[illegible]

then

$$k_1 = \frac{L_1}{\tan \theta} = \frac{6}{.36} = .167 \approx 17$$

for the 4.25" sink

$$\frac{k_2}{L_2} = \frac{1}{\tan \theta_2} = \frac{1}{.27}, \quad k_2 = \frac{L_2}{.27} =$$

$$\frac{4.25}{.27} = 15.7 \approx 17$$

for the 3" square sink

$$\frac{k_3}{L_3} = \frac{1}{.18}, \quad k_3 = \frac{3}{.18} = 16.6 \approx 17$$

Since $k_1 \approx k_2 \approx k_3$, equation 2 can be expressed as follows:

$$T_{op} = 165 + \frac{17\overline{P}}{L}$$

where

T = temperature indegrees fahrenheit of a transistor with a square heat sink of side L inches long dissipating as average power $\overline{P}$. The heat sink material is described in Chapter II, THE METHOD OF TEST.

IMPORTANT!

Special care should be taken to prevent loss or damage of this volume. If lost or damaged, it must be paid for at the current rate of typing.